Beetle – A radiation hard readout chip for LHCb

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**Outline**

- LHC accelerator / LHCb experiment
  - Beetle 1.3
    - Overview / Architecture
    - Lab measurements
    - Test beam
  - “Unsightly” behaviours
    - patches and workaround
  - Outlook

16 Beetle 1.3 on a VELO hybrid attached to Si-sensor
LHC accelerator at CERN

- **Large Hadron Collider (LHC)**
- 27 km circumference
- switch on 2007
- collide beams of protons at an energy of 14 TeV, lead nuclei smashing together with a collision energy of 1150 TeV

1 TeV = energy of a flying mosquito,

but energy is squeezed into a space about million million times smaller than a mosquito.
LHC experiments

- 5 LHC experiments:
  - ATLAS
  - CMS
  - TOTEM
  - ALICE
  - LHCb
LHCb experiment

- Single-arm spectrometer, \( pp \)-collisions
- precision measurement experiment for CP-violation and rare decays in B-meson system
- 100,000 B-mesons/s at an interaction rate of 40 MHz, hidden in 200 times more non-B events
- Key Specifications:
  - 40 MHz sampling / 40 MHz analog readout
  - max. latency \( 4 \mu s \)
  - fast shaping:
    \[ t_{\text{rise}} \leq 25 \text{ ns} \]
    remainder 25 ns after peak \( \leq 30\% \)
  - accept up to 16 consecutive triggers
  - readout time \( \leq 900 \text{ ns} \)
  - radiation hard \( \geq 10 \text{ Mrad} \)
LHCb detector

- **Silicon Tracker (ST):**
  - silicon-strip detector
  - ~ 200 µm pitch
  - 350,000 channels
  - 11 m²

- **Trigger Tracker (TT):**
  - Input load up to 50 pF
  - 22 to 33 cm strip length

- **Inner Tracker (IT):**
  - Input load ~ 33 pF
  - up to 22 cm strip length

- **Vertex Locator (VeLo):**
  - R-Ö-silicon sensor
  - 37 µm to 92 µm pitch
  - Input load < 10 pF
  - 205,000 channels

Beetle - a readout chip for LHCb
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3 Beetle 1.2 on a TT prototype hybrid attached to Si-ladder
Beetle: Architecture

- **modes of operation:**
  - analog pipelined readout (VELO, ST)
  - binary pipelined readout (RICH)
  - prompt binary readout (Veto)
### History

<table>
<thead>
<tr>
<th>chip name</th>
<th>submission</th>
<th>size [mm²]</th>
<th>description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BeetleFE 1.0</td>
<td>May 1999</td>
<td>2 x 2</td>
<td>front-end test chip</td>
</tr>
<tr>
<td>BeetleBG 1.0</td>
<td>May 1999</td>
<td>2 x 2</td>
<td>bias generator test chip</td>
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<td>Beetle 1.0</td>
<td>April 2000</td>
<td>5.5 x 6.1</td>
<td>readout chip</td>
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<tr>
<td>BeetleCO 1.0</td>
<td>April 2000</td>
<td>2 x 2</td>
<td>comparator test chip</td>
</tr>
<tr>
<td>BeetlePA 1.0</td>
<td>April 2000</td>
<td>2 x 2</td>
<td>pipeamp and I²C-interface test chip</td>
</tr>
<tr>
<td>BeetleMA 1.0</td>
<td>April 2000</td>
<td>2 x 2</td>
<td>front-end test chip for RICH option</td>
</tr>
<tr>
<td>Beetle 1.1</td>
<td>March 2001</td>
<td>5.5 x 6.1</td>
<td>readout chip</td>
</tr>
<tr>
<td>BeetleFE 1.1</td>
<td>May 2001</td>
<td>2 x 2</td>
<td>front-end test chip</td>
</tr>
<tr>
<td>BeetleFE 1.2</td>
<td>May 2001</td>
<td>2 x 2</td>
<td>front-end test chip</td>
</tr>
<tr>
<td>BeetleSR 1.0</td>
<td>May 2001</td>
<td>2 x 2</td>
<td>SEU robust I²C-interface test chip</td>
</tr>
<tr>
<td>Beetle 1.2</td>
<td>April 2002</td>
<td>5.1 x 6.1</td>
<td>readout chip (now SEU robust)</td>
</tr>
<tr>
<td>Beetle 1.2 MA0</td>
<td>December 2002</td>
<td>5.2 x 6.1</td>
<td>readout chip (RICH)</td>
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<tr>
<td>Beetle 1.3</td>
<td>June 2003</td>
<td>5.4 x 6.1</td>
<td>readout chip</td>
</tr>
<tr>
<td>Beetle 1.4</td>
<td>May 2004</td>
<td>5.4 x 6.1</td>
<td>readout chip</td>
</tr>
</tbody>
</table>
Layout

• 0.25 µm standard CMOS technology
  • 3 metal layers
  • with MIMCAP and ZeroVt option

• 30.06.2003  Submission of Beetle 1.3
• 22.09.2003  Beetle arrived in Heidelberg

Beetle 1.3 layout
Beetle 1.3 Lab Setup (1)

- Beetle I²C
- Id jumpers
- Analog In
- Daughter board with 2 Beetle chips
- Input signals (digital, LVDS)
- AnalogOut (Beetle)
- AnalogOut (Receiver)

Beetle - a readout chip for LHCb

ASIC-Laboratory, Max-Planck-Institute for Nuclear Physics Heidelberg
Beetle 1.3 Lab Setup (2)

I²C level shifter
(unnecessary for Beetle 1.3)

Analog In
Voltage divider

4 Analog Receiver for 2nd Beetle (AD8130)

LVDS receiver (DS90C032)

4 Analog receiver for 1st Beetle (AD8130)

Bottom view
First readout

- analog readout with 40 MHz
- all 128 channels
- 2 readout frames
  - 1. readout with external signal
  - 2. readout without external signal

non-consecutive readout
## Total Power Consumption

<table>
<thead>
<tr>
<th>Power consumption [mW/ch.]</th>
<th>Minimal</th>
<th>Nominal</th>
<th>Max. operation</th>
<th>Max. DAC</th>
</tr>
</thead>
<tbody>
<tr>
<td>#AO drivers</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td><strong>without clock</strong></td>
<td>0,48</td>
<td>3,49</td>
<td>4,76</td>
<td>14,21</td>
</tr>
<tr>
<td><strong>only 40 MHz clock</strong></td>
<td>1,26</td>
<td>4,28</td>
<td>5,54</td>
<td>14,95</td>
</tr>
<tr>
<td><strong>clocked + 1.1 MHz trigger</strong></td>
<td>1,26</td>
<td>4,36</td>
<td>5,62</td>
<td>15,12</td>
</tr>
</tbody>
</table>
Power Supply Operation

- Analog / Digital: 1.5V to 3.5V
Overclocking Test

- Digital: perfect operation up to 100 MHz
- Analog: nearly 40% gain loss @ 100 MHz

Sclk [MHz]

peak / peak (40 MHz) [%]

Nominal
Maximum

frequency test
Random Trigger Test

- 2 Beetle 1.3 @ 40 MHz
- 2 x $2.34 \cdot 10^{12}$ random triggers
  - 172h ($1.778 \cdot 10^{12}$, $\Rightarrow 2.87$ MHz)
  - 75h ($3.039 \cdot 10^{11}$, $\Rightarrow 1.12$ MHz)
  - 92h ($2.550 \cdot 10^{11}$, $\Rightarrow 0.77$ MHz)
- no triggers lost

Beetle 1.3 random trigger test setup
Temperature Test

**Start-up tests (~15 times each chip):**
- 2 Beetle 1.3
- @ T= -44°C, 60°C, 75°C  (facility temperature)
- Programming (I²C)
- 1.1 MHz trigger + analog readout

**Longtime operating tests (~3 days):**
- 1 Beetle 1.3
- @ T= -44°C, 60°C, 75°C  \(T_{\text{surface}}= -4°C, 94°C, 107°C\)
- 1.1 MHz + analog readout

**Max. stress test:**
- 1 Beetle 1.3
- max. DAC settings
- @ T= 60°C  \(\Rightarrow T_{\text{surface}}= 126°C\)
- Operating over ~ 12 hour
Front-end pulse characterization:
- peaking time $t_p$ (0-100)
- rise time $t_r$ (10-90)
- gain $V_p$
- remainder 25 ns after peak $R = V_{25+} / V_p$
Front end: Pulse-Parameter (2)

Beetle - a readout chip for LHCb

ASIC-Labor, Max-Planck-Institute for Nuclear Physics Heidelberg

Sven Löchner
Front end: ENC - Beetle 1.3

Beetle 1.3 ENC
(FE, Pipeline, Pipeamp, Readout)

ENC_{Vfs=0}\: 547.7 \text{ e}^- + 52.6 \text{ e}/\text{pF}
ENC_{Vfs=100}\: 539.1 \text{ e}^- + 51.9 \text{ e}/\text{pF}
ENC_{Vfs=400}\: 542.8 \text{ e}^- + 49.9 \text{ e}/\text{pF}
ENC_{Vfs=1000}\: 465.1 \text{ e}^- + 45.2 \text{ e}/\text{pF}
Front end: Temperature

FE parameters vs. temperature

\[ C_p = 3\text{pF} \]
I²C - Input Pads

New 5V tolerant I²C-Pads for Beetle 1.3

- SCL / SDA input level tested:  
  min. HIGH: 1.5V  
  max. HIGH: 7.0V (only tested up to 7.0V)  
  min. LOW: -0.7V  
  max. LOW: 1.1V @ 2.5V HIGH level  
  1.2V @ 3.3V  
  1.3V @ 5.0V

- SDA output delay (ACK): 500ns  
  (I²C specification: delay > 300ns)
Done at the X-ray facility of CERN’s Microelectronic Group

**Irradiated Chips:**
- **4 Beetle 1.1 chips**
  - 2 chips being kept at room temperature
  - 2 chips being annealed at 100 °C
- **2 BeetleFE 1.1 chips**
  containing FE prototypes with a NMOS input transistor
- **2 BeetleFE 1.2 chips**
  containing FE prototypes with a PMOS input transistor

**Accumulated Dose:**
- **Beetle 1.1:** 10 Mrad, 10 Mrad, 30 Mrad, 45 Mrad
- **BeetleFE 1.1:** 10 Mrad
- **BeetleFE 1.2:** 10 Mrad
Total Ionizing Dose results

Beetle showed full functionality beyond 45 Mrad

- full trigger and readout functionality
- full slow control functionality
- performance degradations are small
  - peaktime: up to 30 Mrad: $\leq 1$ ns
    up to 45 Mrad: $\leq 4.5$ ns
  - gain: up to 45 Mrad: $\leq 10\%$

No tuning of bias settings
SEU beam test (1)

- **SEU beam test at Proton Irradiation Facility (PIF)**
  Paul-Scherrer Institute, Switzerland

- **Irradiate of 3 chips:**
  - 65 MeV protons
  - mean flux: $1.56 \times 10^9$ p/cm²/s
  - fluence: $5.51 \times 10^{13}$ p/cm²
  - accumulated dose: 7.93 Mrad

- **Check for bit-flips in Beetle registers**
SEU beam test (2)

- 4 SEU flips found
- time distribution not yet understood, but
  SEU cross section is not a problem !!!

65 MeV proton irradiation

setup on top of the irradiation facility
Sticky Charge

Consecutive readout

- External signals on 5 channel in 1st readout frame
- No sticky charge in 2nd readout frame

but still a different baseline
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X7 beam test with different sensors, attached to Beetle 1.2 chips
Readout (Baseline) (1)

- Consecutive readout
- Non-consecutive readout

Different baseline
correlation plot of
RO[n-1], ch[127] vs. RO[n], ch[127]

previous readout vs. current readout

→ only 2 different baseline-types
Channel Crosstalk (1)

Channel crosstalk

- measured a even/odd dependency
- this effect is also present in 1.2

Clarification of crosstalk:

typical Testpulse for a odd channel (e.g. 63): crosstalk into predecessor channel is larger than into successor channel

typical Testpulse for a even channel (e.g. 68): crosstalk into successor channel is larger than into predecessor channel

Testpulse (63. & 68) is standardised to 100%
Channel Crosstalk (2)

Channel crosstalk is a superposition of at least two different cross talks:

- general “remainder” into next readout channel (order of 2% to 2.5%)
  → reason yet not understood (maybe MUX?)

- odd channel: crosstalk into predecessor ch.
  even channel: crosstalk into successor ch.
  (order of 2.5%)

→ readout line from Pipeline into Pipeamp

→ capacitance between adjacent lines ~ 60fF
  - verified in simulation
  - easy to fix
Channel Crosstalk (3)

Pipeline length: ~ 2 mm
Readout header: parity bit

• Parity bit (I1) is wrong encoded in 4 port mode and Rclk divider = 0 (LHCb mode)

all other modes or Rclk divider settings

⇒ Parity bit is OK

• problem is understood in verilog
  • not so easy to fix
  • simple workaround: swap position I1 with I5
    could be tested on a 1.3 with a FIB patch
Parity bit - workaround (1)

schematic of parity-bit generation (part of MuxScheduler)
Parity bit - workaround (2)

new schematic of parity-bit patch
- Layout modification in FastControl of Beetle (could be done by a FIB)
  - 2 cuts
  - 2 connections

Output device of ParityPCN generation - E_XNor2 (U1126)
FIB patch (1)

- Swap header bit I1 with I5
- done with a FIB patch (FEICO Munich)

Output device of ParityPCN generation - E_XNor2 (U1126)
FIB patch (2)
FIB patch (3)
Outlook

• Beetle 1.3 was tested and characterized substantially in the lab.
• Up to now no bugs were found on the chip which would prevent a use of the Beetle in LHCb.

next steps:
• Preparation of Engineering run in May 2004
  • untouched version of Beetle 1.3
  and
  • slightly modified Beetle 1.4 (parity of PCN, cross-talk in pipeline)