RUPRECHT-KARLS-UNIVERSITÄT HEIDELBERG

Cristian Ovidiu Chitu

Development of Fast Sampling Transient Recorders with Custom ASICs

Dissertation

HD-KIP-01-27

KIRCHHOFF-INSTITUT FÜR PHYSIK

Development of Fast Sampling Transient Recorders with Custom ASICs

Inaugural-Dissertation
zur Erlangung des akademischen Grades eines
Doktors der Naturwissenschaften
der Universität Mannheim

vorgelegt von
Dipl.-Ing. Cristian Ovidiu Chiţu
aus Ploieşti
Rumänien

Mannheim, 2000

Dekan:	Professor Dr. Guido Moerkotte, Universität Mannheim
Referent:	Professor Dr. Reinhard Männer, Universität Mannheim
Korreferent:	Professor Dr. Werner Hofmann, Max-Planck-Institut für Kernphysik Heidelberg

Tag der mündlichen Prüfung: 06. November 2000

Development of Fast Sampling Transient Recorders with Custom ASICs

A Dissertation
Submitted to the Faculty of Mathematics and Computer Science
of the University of Mannheim
for the Degree of Doktor der Naturwissenschaften (Dr. rer. nat.)

By
Dipl.-Ing. Cristian Ovidiu Chiţu
from Ploieşti
Romania

Mannheim, 2000

Zusammenfassung

Analoge Speicher aus geschalteten Kapazitäten sind für eine Vielzahl von Anwendungen geeignet, sofern keine fortlaufende Digitalisierung der analogen Signale notwendig ist. In Datennahmesystemen, die auf einem analogen Speicher basieren, werden die Eingangssignale mit hoher Rate abgetastet und für begrenzte Zeit zwischengespeichert. Die analogen Abtastwerte werden dann mit einer geringeren Rate ausgelesen und mit einem langsamen ADC digitalisiert, bevor neue Signale aufgenommen werden. Die Vorteile eines analogen Speichers sind ein geringerer Leistungsverbrauch, geringere Kosten, eine große Dichte und ein höherer dynamischer Bereich bei hohen Abtastraten. Ein analoger Speicher führt die Abtastung und Zwischenspeicherung von Werten mit höheren Raten und grösserer Genauigkeit durch, als dies durch eine direkte digitale Umwandlung bewerkstelligt werden könnte.

Diese Dissertation untersucht detailliert die wichtigen Komponenten zweier analoger Speicher. Die Forschungsarbeit hat zum Entwurf von zwei analogen Speichern geführt, die Analogsignale mit einer Abtastrate von einigen hundert MHz aufnehmen können. Dies wird durch eine Speicherarchitektur bewerkstelligt, in der die Sockelwerte der Speicherzellen und die Abtastzeiten unabhängig vom Signalpegel sind. Die Ansteuerung der Schreibadresse für diese Speicher wurde durch Inverter-Verzögerungsketten realisiert, die eine hohe Güte bezüglich der Abtastrate und der Zeitgenauigkeit gewährleisten.

Auf Grundlage der in dieser Arbeit entwickelten Konzepte wurden zwei analoge Speicher entworfen und in der AMS 0.8 μm CMOS Technologie mit Poly-zu-Poly Kapazitäten integriert. Ausgedehnte Messungen dieser Prototypen bei einer Abtastrate von 500 MHz werden dargestellt. Nachdem ein einfaches Multiplikations - und Additionskorrekturverfahren durchgeführt wurde, entspricht der dynamische Bereich, die Linearität, der Offset und die Verstärkung einer Genauigkeit von 8 Bit.

Abstract

Switched capacitor analog memories are well suited to a number of applications where a continuous digitisation of analog signals is not needed. In data acquisition systems based on the use of an analog memory, the input waveforms are sampled and stored at a high rate for a limited period of time, and the analog samples are then retrieved at a lower rate and digitised with a slow ADC before new waveforms are acquired. The advantages of using an analog memory are lower overall power dissipation and cost, high density, and potentially superior dynamic range at high sampling rates. The analog memory shows the fact that the sampling and storage of samples in analog memory cells can be accomplished at a higher rate and with a greater precision than direct digital conversion.

This dissertation examines the important components of two analog memories in detail. The research has led to the design of two analog memories that can acquire analog waveforms at sampling rates of several hundred MHz. This is accomplished by a memory architecture in which the memory cell pedestals and sampling times are independent of the signal level. The write address control for these memories has been realised with inverter delay chains that provide high performance with respect to sampling rate and timing accuracy.

Based upon the concepts developed in this work, two analog memories were designed and integrated in a AMS 0.8 μm CMOS technology with poly-to-poly capacitors. Extensive measurements of these prototypes at a sampling rate of 500 MHz are presented and demonstrate a dynamic range, linearity, offset, and gain accuracy corresponding to a precision of 8 bits after a simple multiplication and addition correction procedure.

Acknowledgements

This work was supported by the Max-Planck-Institut für Kernphysik in Heidelberg and has been done at ASIC Labor in Heidelberg.

I extend my sincere appreciation to my work supervisor, Prof. Dr. W. Hofmann, which enabled the completion of this research. I am particularly grateful to him for extending to me the freedom in defining and directing my research, and I also appreciate his insightful and constructive help to write with clarity and precision.

I am also indebted to my Ph.D. supervisor, Prof. Dr. R. Männer. I would like to point out his positive attitude to all attractive and perspective ideas born during my work.

Many thanks go to Prof. Dr. N. Fliege for serving on my oral examination committee.

I like to thank my colleagues from ASIC Labor and Cherenkov group of the Max-Planck-Institut für Kernphysik for many valuable discussions and for help during the research.

Also many thanks to my professors from the Faculty of Electronics and Telecommunications of Bucharest, Romania, who offered me a solid basis in electronics, from where I could develop and build further.

Very important for me was the support and love of my parents who were so far away from me.

Finally, I want to give special thanks to my wife, Cristina. Without her support and understanding, this dissertation would not have been possible.

Contents

List of Tables **v**

List of Figures **vii**

1 Introduction **1**
1.1 Motivation 1
1.2 Outline 2

2 Switched Capacitor Analog Memory Cell **5**
2.1 Overview 5
2.2 Analog Memory Architectures 5
2.3 Analog Memory Concept 6
2.4 CMOS Technology 7
2.5 NMOS Transistor Switch 8
2.5.1 NMOS Switch Resistance 8
2.5.2 Error Voltage 9
2.5.3 Distortion and Timing Errors 11
2.6 CMOS Transmission Gate Switch 13
2.6.1 CMOS Switch Resistance 13
2.6.2 Error Voltage 14
2.7 Capacitors 18
2.8 Matching Properties of Memory Cell 19
2.9 Summary 20

3 Analog Memory Circuit **23**
3.1 Overview 23
3.2 Chips Architecture 23
3.3 Analog Memory Core 24
3.3.1 Architecture 24
3.3.2 Description 26
3.3.3 DC Transfer Function 29
3.3.4 Signal Range 31
3.3.5 Small Signal Acquisition Bandwidth 32
3.3.6 Acquisition Time 34

3.3.7 Leakage Current . . . 35
3.4 Summary . . . 35

4 Readout Operational Amplifier 37
4.1 Overview . . . 37
4.2 Amplifier Circuit . . . 37
4.3 Simulation Results . . . 39
4.4 Amplifier Noise . . . 42
4.5 Summary . . . 43

5 Control Circuits 45
5.1 Overview . . . 45
5.2 High Speed Addressing Circuit . . . 45
5.2.1 Circuit Description . . . 45
5.2.2 Timing Accuracy . . . 48
5.3 Read Addressing Circuits . . . 48
5.3.1 Read Control Circuit for FASTSAMP-EV chip . . . 48
5.3.2 Read Control Circuit for FASTSAMP-V1 chip . . . 50
5.4 Summary . . . 53

6 Memory Calibration and Correction Procedures 55
6.1 Introduction . . . 55
6.2 DC Calibration . . . 56
6.2.1 Subtraction Method . . . 56
6.2.2 Multiplication and Addition Method . . . 57
6.2.3 Piece-Wise Linear Approximation Method . . . 58
6.3 AC Calibration . . . 59
6.4 Method to Calibrate Signals from Cherenkov Telescopes . . . 61
6.5 Summary . . . 61

7 Simulation and Experimental Results 63
7.1 Overview . . . 63
7.2 Chips Layout . . . 63
7.3 Simulation Results . . . 68
7.4 Analog Memory Noise . . . 69
7.5 Experimental Results . . . 71
7.5.1 DC Transfer Characteristic . . . 71
7.5.2 Dynamic Range . . . 76
7.5.3 AC Response . . . 76
7.6 Summary . . . 80

8 Conclusions and Suggestions 81
8.1 Conclusions . . . 81
8.2 Suggestions for Future Work . . . 82

A Parameters **85**

B Analysis of Charge Injection in MOS Analog Switches **87**

C FASTSAMP-EV Chip Test Setup **91**

D FASTSAMP-V1 Chip Test Setup **97**

Bibliography **103**

List of Tables

3.1 Architectures for both chips. 24

4.1 Dc operating points of MOS transistors. 38
4.2 Simulation results. 38
4.3 Simulation and calculation results at 10 pF load capacitance. 41

6.1 Calibration and correction parameters. 59

7.1 Calculation and measurement results for both devices. 71
7.2 Performances for both devices. 80

A.1 AMS 0.8 μm CMOS Process Parameters [40]. 85
A.2 Analog Memory Core Parameters. 85

C.1 Test setup equipment list for FASTSAMP-EV chip. 92

D.1 Test setup equipment list for FASTSAMP-V1 chip. 98

List of Figures

1.1 Signal acquisition in an analog memory. 2

2.1 Simplified representation of an analog memory. 7
2.2 Physical structure of an NMOS and PMOS transistor in a n-well CMOS technology. 8
2.3 NMOS switch placed in (a) signal and (b) signal return path. 9
2.4 Pedestal voltage as a function of input voltage for NMOS switch. 10
2.5 Timing errors when the sampling switch is placed in signal path. 11
2.6 Timing errors when the sampling switch is placed in signal return path. . . 12
2.7 Schematic of the CMOS switch placed in signal path. 14
2.8 Schematic of the CMOS switch placed in signal return path. 16
2.9 Pedestal voltage as a function of input voltage for CMOS switch. 17
2.10 Physical structure of poly-to-poly capacitor. 18

3.1 Block diagram for (a) FASTSAMP-EV and (b) FASTSAMP-V1 chips. . . . 25
3.2 Memory architecture with one amplifier per channel. 26
3.3 Simplified schematic of one analog memory channel. 26
3.4 Timing diagram for (a) write and (b) read phases. 27
3.5 Analog memory channel with parasitic capacitances. 28
3.6 Circuit configuration before the memory cell is addressed for readout. . . . 30
3.7 Circuit configuration when the memory cell is addressed for readout. . . . 31
3.8 (a) Triangle input waveform. (b) Waveforms at node x_i in Figure 3.5 with the write switch turned off at time t_1 (solid line) and t_2 (dashed line). . . . 32
3.9 Equivalent circuit of a memory cell during signal acquisition. 33
3.10 Time response of the analog memory cell to a step input. 34

4.1 Schematic of the folded cascode amplifier. 38
4.2 Amplifier in the (a) voltage follower and (b) inverter configuration. 39
4.3 Upper: Input voltage as a function of output voltage. Lower: Residuals from a fit to a 2.5 V output voltage range. The amplifier is in the inverter configuration. 40
4.4 Output voltage plotted as a function of input voltage. The amplifier is in the follower configuration. 40
4.5 Amplitude (upper) and phase (lower) plotted as a function of frequency. . . 41

5.1 Inverter delay chain of 32 cells and servo feedback circuit. 46
5.2 Timing diagram of the write signals in one delay chain. 47
5.3 Timing diagram of the inverter chain showing the falling edge of the last write signal $w < 32 >$ which can be (a) before or (b) after the raising edge of the reference pulse $Aref1$. 47
5.4 Timing errors after simulations in one delay chain. 48
5.5 A 32 stage dynamic two-phase shift register with timing diagram. 49
5.6 Two-phase clock generator. 50
5.7 Read control circuitry with timing diagram. 51
5.8 Schematics of the (a) 1 of 4 decoder and (b) 1 of 8 decoder. 52

6.1 Dc correction procedure using a subtraction method. 56
6.2 Dc correction procedure using a multiplication and addition method. . . . 57
6.3 Dc correction procedure using a piece-wise linear approximation method. . 58
6.4 Effect of sample time error on the reconstructed output of four write signals showing the actual sample time of the write signal $w < 2 >$ which can be (a) after or (b) before the nominal sample time. 60
6.5 Input signal as (a) ramp wave or (b) signal from Cherenkov telescope. . . . 60

7.1 Layout view (3.26 mm × 3.37 mm) of the FASTSAMP-EV chip. 64
7.2 Layout view (3.26 mm × 3.39 mm) of the FASTSAMP-V1 chip. 65
7.3 Schematic (upper) and layout (lower) of an analog memory cell. 66
7.4 Response after simulations of one channel to a 2 V peak-to-peak, 3.906250 MHz sine wave sampled at 500 MHz. The pulse is plotted on the (a) read and the (b) write time scale. 67
7.5 Response after simulations of one analog memory cell to a 2 V peak-to-peak, 3.906250 MHz sine wave sampled at 500 MHz after (a) ideal and (b) parasitic simulations. The pulse is plotted on the read time scale. 68
7.6 Circuit for analysis of analog memory noise during the (a) write and (b) read phase. 69
7.7 Picture taken from the oscilloscope representing three channels Ch1: $AnalogOutputCh1$, Ch2: $TriggerScope$ and Ch3: $ComIn$ or $ComInOut$ depending of the chip version. 70
7.8 Cell pedestals after calibration as a function of input voltage for the 128 memory cells. Dc measurements for FASTSAMP-EV device. 72
7.9 Cell pedestals before calibration as a function of input voltage for the 32 memory cells. Dc measurements for FASTSAMP-V1 device. 73
7.10 Cell pedestals after calibration as a function of input voltage for the 32 memory cells. Dc measurements for FASTSAMP-V1 device. 73
7.11 Cell gain (upper) and cell offset voltage (lower) as a function of cell number for FASTSAMP-EV device. 74
7.12 Cell gain (upper) and cell offset voltage (lower) as a function of cell number for FASTSAMP-V1 device. 74

7.13 Upper: Output plotted as a function of input voltage. Lower: Deviations for the selected 1.5 V input signal range. Dc measurements for FASTSAMP-EV device. 75
7.14 Upper: Output plotted as a function of input voltage. Lower: Deviations for the selected 1.5 V input signal range. Dc measurements for FASTSAMP-V1 device. 75
7.15 Response after measurements of 32 cells to a 1.5 V peak-to-peak (a) gaussian pulse sampled at 500 MHz. The pulse is plotted on the (b) read and the (c) write time scale. Ac measurements for FASTSAMP-V1 device. . . . 77
7.16 Response after measurements of 32 cells to a 1.5 V peak-to-peak (a) rectangle pulse sampled at 500 MHz. The pulse is plotted on the (b) read and the (c) write time scale. Ac measurements for FASTSAMP-V1 device. . . . 78
7.17 Results of 20 measurement sets from a 1.5 V peak-to-peak, 3.906250 MHz sine wave sampled at 500 MHz. Residuals are plotted as a function of cell number for FASTSAMP-EV device. 79
7.18 Results of 20 measurement sets from a 1.5 V peak-to-peak, 15.625 MHz sine wave sampled at 500 MHz. Residuals are plotted as a function of cell number for FASTSAMP-V1 device. 79

B.1 Schematic of the NMOS switch placed in signal return path. 88
B.2 Analysis of clock feedthrough effect for NMOS switch placed in signal return path when (a) $V_G = V_C + V_T$ and (b) $V_G = V_L$. 89

C.1 Experimental setup for FASTSAMP-EV chip. 92
C.2 Schematic of the Printed Circuit Board of FASTSAMP-EV chip. Power supply connections. 93
C.3 Schematic of the Printed Circuit Board of FASTSAMP-EV chip. Connections between the chip and other components. 94
C.4 Vector diagram for write phase of FASTSAMP-EV chip. 95
C.5 Vector diagram for read phase of FASTSAMP-EV chip. 96

D.1 Experimental setup for FASTSAMP-V1 chip. 98
D.2 Schematic of the Printed Circuit Board of FASTSAMP-V1 chip. Power supply connections. 99
D.3 Schematic of the Printed Circuit Board of FASTSAMP-V1 chip. Connections between the chip and other components. 100
D.4 Vector diagram for write phase of FASTSAMP-V1 chip. 101
D.5 Vector diagram for read phase of FASTSAMP-V1 chip. 102

Chapter 1

Introduction

1.1 Motivation

In many modern data acquisition systems the analog waveforms need only to be captured as snap shots and continuous digitisation is not necessary. Such applications include pulse echo phenomena (radar, ultrasonics), pulse shape recording (high energy physics experiments), and laboratory instrumentation (oscilloscopes, transient digitisers). In these applications an input waveform can be sampled at a high sampling frequency for a limited period of time, and the samples are stored in an analog memory. The analog samples are then retrieved at a lower rate and digitised with a slow analog-to-digital (ADC) converter before a new waveform is acquired. Advantages of using an analog memory include low overall power dissipation and cost, high density, and potentially superior dynamic range at high sampling rates.

A block diagram of a typical waveform acquisition system is shown in Figure 1.1. The electrical signal generated in the detector or sensor is amplified and shaped. The analog waveform is then sampled at high speed rate by using a fast write clock and stored in the analog memory. The stored information is read out at slow rate and is converted into digital form. Because the readout speed and latency are not crucial, a commercial ADC can be used to convert data from analog into digital form. In addition, many signal channels can be multiplexed onto one ADC. The use of an analog memory eases the speed required of the ADC considerably and therefore significantly reduces the cost and the power dissipation.

Specific application for the memories proposed in this work appears for the camera electronics of the Cherenkov telescopes [1] in the *H*igh *E*nergy *S*tereoscopic *S*ystem (HESS) project [2]. Cameras for these telescopes and their readout systems were developed at Max-Planck-Institut für Kernphysik in Heidelberg. A large part of the trigger electronics, analog signal storage, and monitoring electronics are integrated in the camera electronics of the Cherenkov telescope. Fast photomultipliers (PMTs) are used to convert the Cherenkov light from the sky into electrical signals. The proposed analog memories are an alternative for the camera electronics of the Cherenkov telescopes where continuous data acquisition is not required.

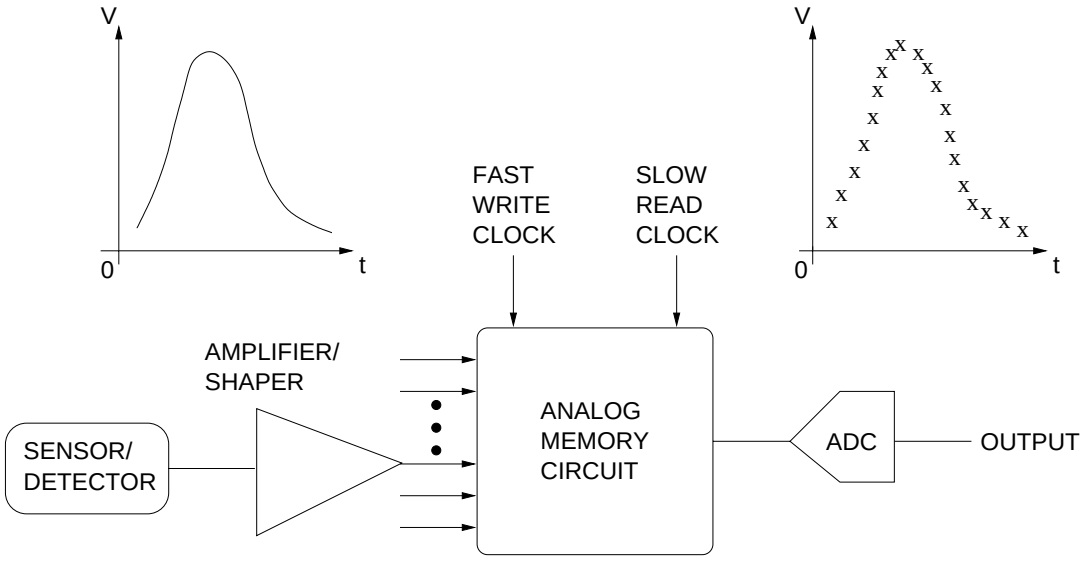

Figure 1.1: Signal acquisition in an analog memory.

A number of concepts and circuits considered in this thesis have been taken from [26] and adapted for the Cherenkov application. This is the case of the analog memory architecture, of the readout operational amplifier and of the control circuits. Changes in the design from [26] can be found in the high speed addressing circuit and read control circuit.

In this thesis the basic characteristics of integrated transistor switches and capacitors are reviewed and two circuits for waveform sampling at rate of 500 MHz are introduced. Each circuit consists of four channels with 128 cells in each channel for acquiring analog waveforms. The architectures of these circuits are investigated in detail with respect to their theoretical dc and ac performances. Both switched capacitor analog memories for capturing fast signals from Cherenkov telescopes have been integrated in the Austria Microsystems (AMS) 0.8 μm complementary metal oxide semiconductor (CMOS) process with poly-to-poly capacitors. The chips have been tested at ASIC laboratory in Heidelberg and the experimental results are presented in this thesis.

1.2 Outline

The implementation of analog memory cells using switched capacitor circuits is described in Chapter 2. Several analog memory architectures that have been implemented are examined briefly. The chapter then describes the MOS transistor explored with respect to its use as a voltage switch. The error voltages are evaluated for several memory cell configurations wherein the switch is inserted in the signal or signal return paths. The limiting factors governing the matching of the signal responses among individual memory cells are identified.

Chapter 3 introduces an analog memory core architecture. The operation of this

memory and its expected performance are discussed. Performance parameters such signal range, small signal acquisition bandwidth, and acquisition time are presented. The memory circuit's transfer function is derived, illustrating the effect of component mismatch within a memory channel on the memory response.

The folded cascode amplifier architecture is described in Chapter 4. The amplifier is examined and its gain, bandwidth, and noise are investigated. The simulation results are compared to the calculated parameters.

The control circuits which provide the write and read addresses for analog memory core are described in Chapter 5. A write control circuit comprising delay chains with feedback control circuits is proposed. Depending of the chip version, the read control circuit is implemented with shift registers or decoders.

Calibration and correction procedures that can be used for high precision data acquisition are reviewed in Chapter 6.

The simulation and experimental results of two circuits are presented in Chapter 7. These circuits were integrated in a AMS 0.8 μm CMOS technology with poly-to-poly capacitors. The test setups used for the characterisation of the memories are explained and experimental results are presented. A dynamic range of 8 bits has been achieved for sampling rate of 500 MHz.

Chapter 8 summarises the contributions of this research and identifies areas of future study.

Chapter 2

Switched Capacitor Analog Memory Cell

2.1 Overview

In this chapter the operation of the MOS transistor is investigated with emphasis on its use in sample and hold configuration. The chapter starts with a short description of some architectures that have been realised in switched capacitor technologies. In the following section the analog memory concept is explained. In Section 2.5 and Section 2.6 are expressed the error voltages for MOS transistors and CMOS transmission gates as a function of the circuit parameters. Implementation of poly-to-poly capacitors for the storage of the sampled signal is reviewed in Section 2.7. For many analog memory applications the uniformity of the memory cell transfer characteristic in a channel is more important than the absolute channel offset and gain. The parameters limiting this uniformity are discussed in Section 2.8.

2.2 Analog Memory Architectures

Strong cost and performance incentives especially encourage the use of analog switched capacitor memories in high energy physics experiments [3]. Fast analog waveform capture for thousands of channels must be provided with a minimum of power dissipation. The design challenge is to produce an uniform and linear response in large number of memory cells at a level of performance comparable to the accuracy inherent in the technology. Principal performance issues are cell-to-cell offset and gain variations within a memory channel, which are governed by the circuit architecture and its sensitivity to the matching properties of its constituent transistors and capacitors [4]–[6]. In high precision applications, the lowest achievable cell non-uniformities may not be acceptable and must therefore eliminated by correcting the data. In large systems, it is essential that the number of correction constants and the computational effort to be minimised.

Early analog memory circuits based on a sample and hold topology contain a sampling switch, a storage capacitor, and a readout buffer in each memory cell [7]–[10]. In order to

meet the need for lower power and higher density, architectures based on switched capacitor circuits were introduced [11]–[17]. In these circuits, each channel comprises a bank of capacitors that are switched to a single operational amplifier for readout. Architectures in which the sampling transistors are placed in the signal path [7]–[13] exhibit signal dependent charge injection in each cell. Cell pedestals are then a function of the input signal and may require individual offset, gain, and linearity corrections. In addition, a serious disadvantage of these implementations in high speed applications is the dependence of the sampling transistor turn off time on the signal level [8].

In circuits based on traditional charge redistribution switched capacitor techniques [17], sampling switch charge injection can be made independent of the signal level, but the cell gain is a linear function of the size of the storage capacitor. Cell-to-cell gain matching of better than 0.5 % across an entire channel is therefore difficult to achieve, and both offset and gain corrections are commonly needed for each cell.

An analog memory architecture published in [26] was used in this thesis and described in Chapter 3. It will be shown that for this architecture the memory cell pedestal voltages are independent of the input signal voltage.

2.3 Analog Memory Concept

The concept of an analog memory circuit comprising M signal channels with N cells in each channel is shown in Figure 2.1. Each cell of the memory $C_{j,i}$ is located on the column address i $(1 \leq i \leq N)$ and the row address j $(1 \leq j \leq M)$. An analog input signal $V_{inj}(t)$ is applied to all N memory cells in the channel j. The write control signals $w < 1 >$ through $w < N >$ as well as the read control signals $r < 1 >$ through $r < N >$ are common to all channels. The analog waveforms are stored in the analog memory by sequentially addressing the memory cells within a channel via the write control signals $w < 1 >$ through $w < N >$. After the write phase is finished, the readout phase is initiated by applying sequentially the read addresses $r < 1 >$ through $r < N >$. The analog output $V_{outj}(t)$ can be digitised by an on or off-chip ADC converter which provides the digital information V_{outj}.

The maximum number of the analog values which can be stored in the array represented in Figure 2.1 is the number of rows M times the number of columns N. Usually in analog memory applications [8, 9] the number of channels is large compared with the number of cells in one channel $(M \gg N)$. In such applications, the minimum time between the acquisition of two consecutive input waveforms must be long enough to permit a sequential read out of the data.

This thesis focuses on analog waveform sampling applications in which the number of cells in a channel is large compared to the number of channels on one chip $(N \gg M)$.

For both types of applications where $(M \gg N)$ and $(N \gg M)$ the time between the readout of two adjacent memory cells can be much larger than the time between the acquisition two consecutive input samples. This facilities the use of a low speed high resolution ADC converter. Generally, a single converter is sufficient for digitisation of the analog waveforms from many memory cells.

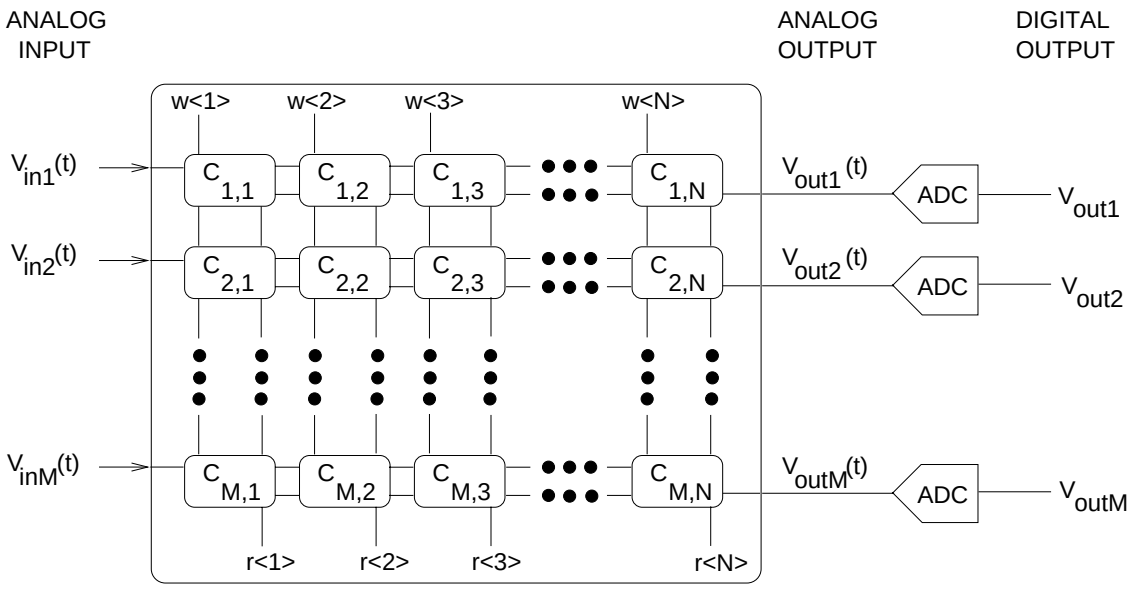

Figure 2.1: Simplified representation of an analog memory.

2.4 CMOS Technology

The AMS 0.8 μm CMOS process is a *twin*-well technology on p-substrate with double metal and double poly [40]. In a *twin*-well technology, there are created individual wells for NMOS and PMOS transistors and the substrate may be either n-type or p-type. The structure of an n-channel and p-channel MOS transistor using a n-well technology is shown in Figure 2.2. The n-channel device is formed with two heavily doped n^+ regions diffused into a lighter doped p-substrate. The two n^+ regions are called d (drain) and s (source), and are separated by a distance, L (referred to as the device length). At the surface between the drain and source lies a gate electrode g that is separated from the silicon by a thin dielectric material (silicon dioxide). The b terminal is the bulk, or substrate, which contains the drain and source diffusions. Similarly, the p-channel transistor is formed by two heavily doped p^+ regions within a lightly doped n for n-well processes. It, too, has a gate on the surface between the drain and source separated from the silicon by a thin dielectrical material (silicon dioxide). For a n-well process, the p-substrate connection is common throughout the integrated circuit and is connected to the lowest potential. Multiple n-wells can be fabricated on a single circuit, and they can be connected to different potentials in various ways depending upon the application. Essentially both NMOS and PMOS transistors have four terminals as identified in Figure 2.2 by g (gate), d (drain), s (source) and b (bulk).

An interesting observation can be made from the layout of the MOS transistor in Figure 2.2. The MOS devices are totally geometrically symmetric with respect to drain and source and so must also be electrically symmetric. The designation of drain and source is thus arbitrary. In many applications a convention has evolved for convenience and consistency in device modelling in regard to drain and source designation.

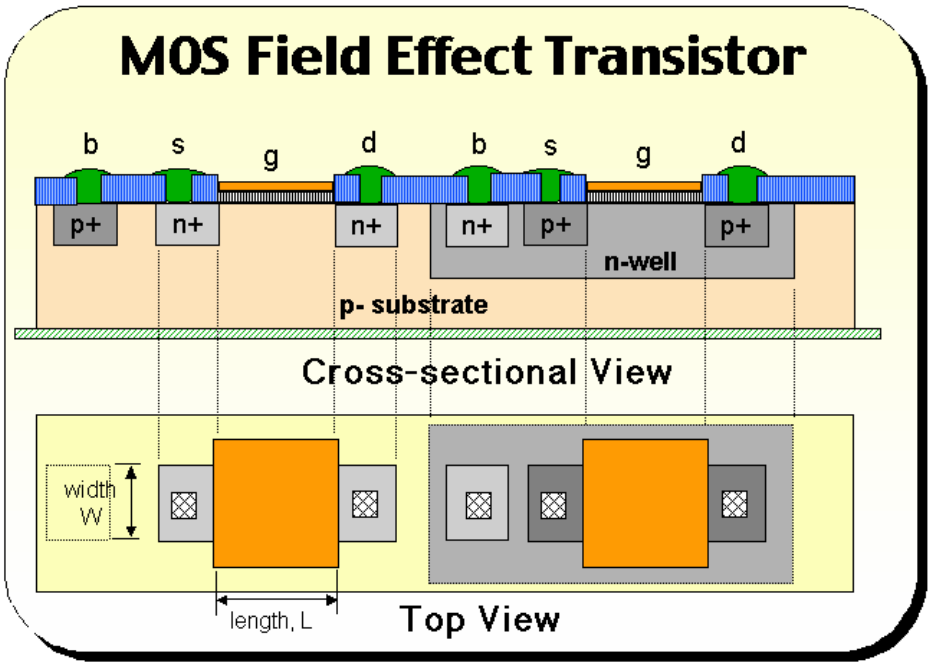

Figure 2.2: Physical structure of an NMOS and PMOS transistor in a n-well CMOS technology.

2.5 NMOS Transistor Switch

2.5.1 NMOS Switch Resistance

In an analog memory cell the MOS transistor can be used as a voltage switch. Two sample and hold configurations were proposed in Figure 2.3 using an NMOS transistor as switch and a storage capacitor C_S.

An expression of the on channel resistance can be found as follows. In the on state of the switch, the voltage across the switch should be small, and the gate-to-source voltage V_{GS} should be large. Therefore, the NMOS transistor is assumed to be in the ohmic region [18]–[21] ($V_{DS} < V_{GS} - V_T$) and the current through the device is given by

$$I_{DS} = \mu_n C_{ox} \frac{W}{L} \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS}, \tag{2.1}$$

where V_{DS} is the drain-to-source voltage, μ_n is the electron mobility in the channel, W and L are the width and length of the channel, V_T is the threshold voltage and C_{ox} is the oxide capacitance per unit area. The on resistance of the channel can be approximated by

$$R_{DS} = \frac{1}{\frac{\partial I_{DS}}{\partial V_{DS}}} \approx \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)}. \tag{2.2}$$

The on resistance is inversely proportional to the W over L ratio and is nonlinear since it depends on the gate-to-source voltage.

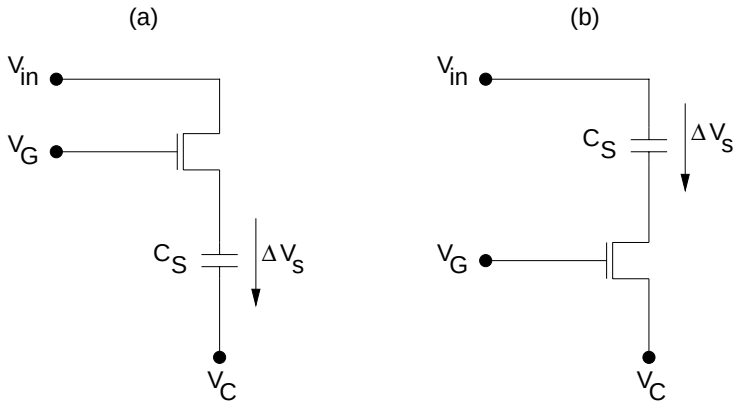

Figure 2.3: NMOS switch placed in (a) signal and (b) signal return path.

2.5.2 Error Voltage

As long as the the NMOS switches are conducting, the voltage across the storage capacitor in Figure 2.3 is given by

$$\Delta V_s = V_{in} - V_C, \tag{2.3}$$

where V_{in} is the input voltage and V_C is the reference voltage. The NMOS transistor turns off when the gate-to-source voltage is less than the threshold voltage. The voltage across the capacitor after turn off of the sampling switch is

$$\Delta V_s = V_{in} - V_C - V_p, \tag{2.4}$$

where V_p is the pedestal voltage due to charge injection and clock feedthrough effect [22]–[25]. In Appendix B these effects are explained in detail and the expression of the pedestal voltage for an NMOS switch placed in signal return path is derived. The magnitude of the pedestal voltage differs for the two cell arrangements represented in Figure 2.3.

In the configuration shown in Figure 2.3(a) the pedestal voltage can be derived in similar way than in Appendix B and written as follows

$$V_p = \frac{\alpha C_{ox} W L}{2C_S}(V_H - V_{in} - V_T) + \frac{C_{ov}}{C_{ov} + C_S + C_p}(V_{in} - V_L + V_T). \tag{2.5}$$

C_p is the parasitic capacitance to ground, C_{ov} is the gate overlap capacitance, α is a coefficient ($0 < \alpha < 1$), V_L and V_H are the low and high levels of the transistor gate voltage. The pedestal voltage can be split into a gain error and an offset,

$$V_p = \varepsilon V_{in} + V_{of}. \tag{2.6}$$

The gain error in the circuit is

$$\varepsilon = \frac{C_{ov}}{C_{ov} + C_S + C_p} - \frac{\alpha C_{ox} W L}{2C_S}, \tag{2.7}$$

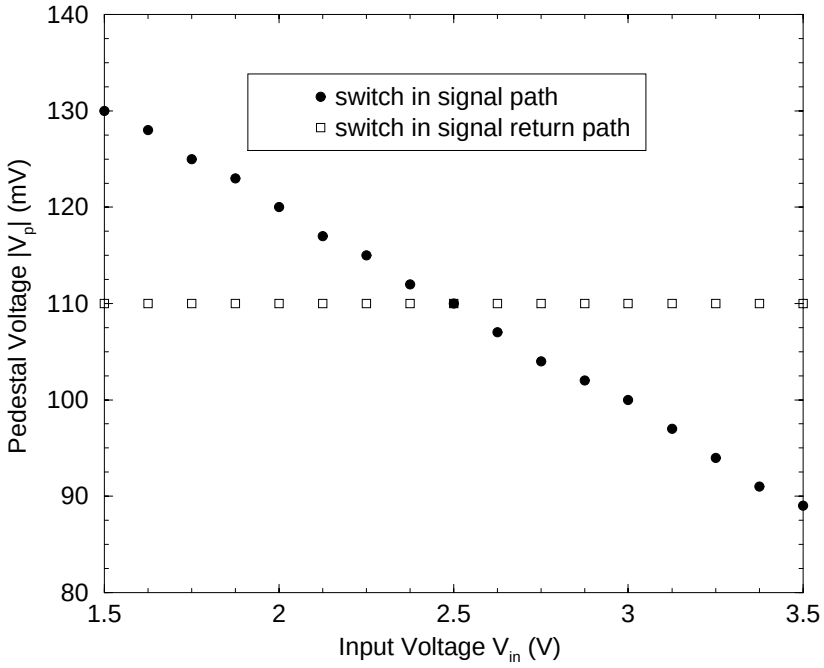

Figure 2.4: Pedestal voltage as a function of input voltage for NMOS switch.

while the offset voltage is

$$V_{of} = \frac{\alpha C_{ox} WL}{2C_S}(V_H - V_T) - \frac{C_{ov}}{C_{ov} + C_S + C_p}(V_L - V_T). \tag{2.8}$$

Following (2.5) through (2.8) for the circuit configuration shown in Figure 2.3(a), the error voltage V_p during turn off depends on the input signal level.

The circuit shown in Figure 2.3(b) can be analysed in the same manner as the circuit in Figure 2.3(a), with the result that the pedestal voltage (see Appendix B) is for this configuration

$$V_p = -\frac{\alpha C_{ox} WL}{2C_S}(V_H - V_C - V_T) - \frac{C_{ov}}{C_{ov} + C_S + C_p}(V_C - V_L + V_T). \tag{2.9}$$

The gain error and offset voltage can be written as

$$\varepsilon = 0 \tag{2.10}$$

$$V_{of} = -\frac{\alpha C_{ox} WL}{2C_S}(V_H - V_C - V_T) - \frac{C_{ov}}{C_{ov} + C_S + C_p}(V_C - V_L + V_T). \tag{2.11}$$

It is evident from (2.9) through (2.11) that the error voltage is independent on the input signal voltage.

The results of SPICE [43]–[46] simulations for the two circuits in Figure 2.3 when they are implemented in the AMS 0.8 μm CMOS technology are illustrated in Figure 2.4. The

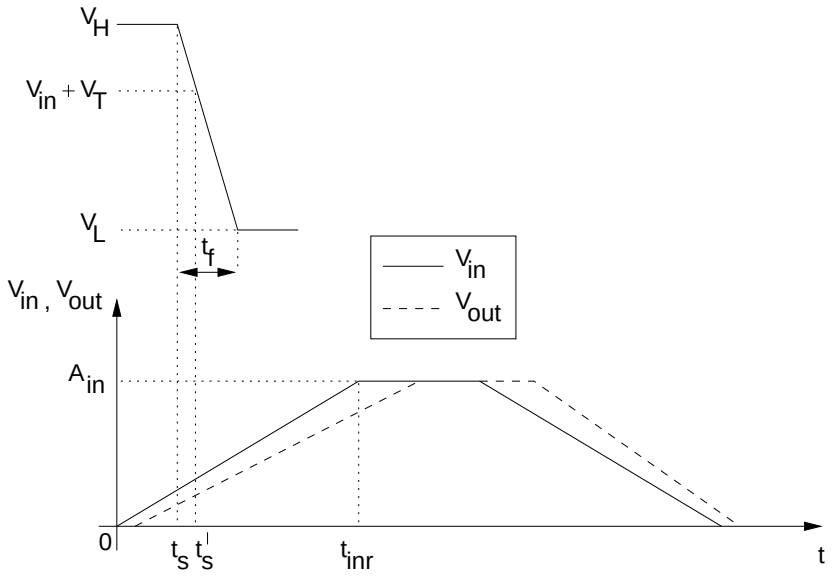

Figure 2.5: Timing errors when the sampling switch is placed in signal path.

absolute values of the simulated pedestal voltages are plotted as a function of the input voltage. The W/L ratio of the NMOS transistor was set to 25 μm/0.8 μm and the size of the sampling capacitance was 500 fF. The gate voltage was a ramp which fell from the high value 5 V toward the low value 0 V in 300 ps. The pedestal voltage varies by 40 mV across an input voltage range of 2 V when the switch is inserted in signal path (Figure 2.3(a)) or is constant (Figure 2.3(b)).

2.5.3 Distortion and Timing Errors

In the preceding subsection the responses of two sample and hold cells to dc input signals were evaluated. This subsection proposes an analysis of distortion and timing errors for ac input signals.

For the configuration shown in Figure 2.3(a) an ac input pulse with an amplitude of A_{in} and rise and fall times of t_{inr} was considered. The process is illustrated in Figure 2.5. The gate control voltage of the NMOS transistor fell from the high value V_H to the low value V_L with the fall time of t_f. At the ideal sampling time t_s the switch is supposed turned off at high level V_H of the gate control voltage. In reality, the switch turns off when the gate control voltage reaches $(V_{in} + V_T)$ and the actual sampling time t'_s is given by

$$t'_s = t_s + \frac{t_f}{V_H - V_L}(V_H - V_{in} - V_T). \tag{2.12}$$

For the rising input signal when

$$V_{in} = \frac{A_{in}}{t_{inr}} t \tag{2.13}$$

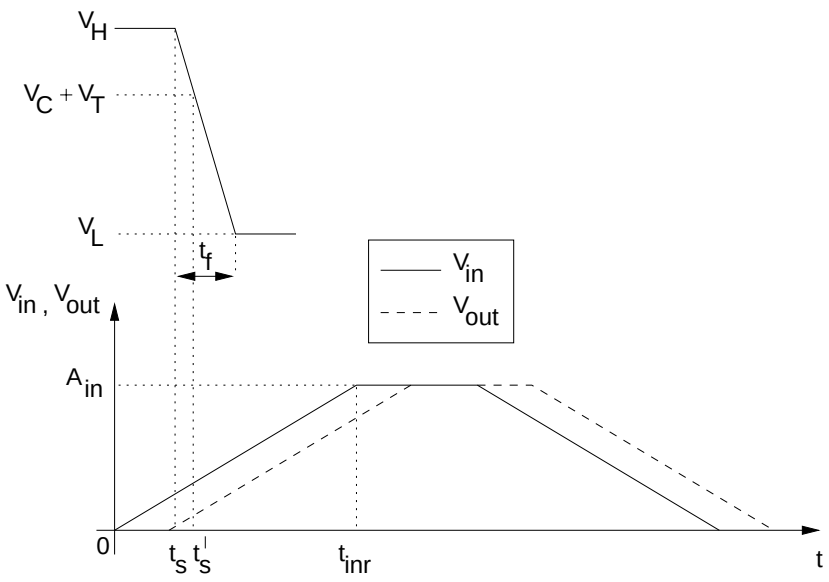

Figure 2.6: Timing errors when the sampling switch is placed in signal return path.

the output signal after changing the time scale can be written as follows

$$V_{out} = \frac{A_{in}}{t_{inr}} \left[t + \frac{t_f}{V_H - V_L}(V_H - V_{in} - V_T) \right]. \tag{2.14}$$

Inserting (2.13) into (2.14), the dependence dV_{out}/dt on dV_{in}/dt can be expressed as

$$\frac{dV_{out}}{dt} = \left(1 - \frac{A_{in}}{t_{inr}} \frac{t_f}{V_H - V_L} \right) \frac{dV_{in}}{dt}. \tag{2.15}$$

The ratio A_{in}/t_{inr} is positive for a rising input signal and negative for a falling input signal. The resulting signal slope dV_{out}/dt is smaller for rising input signals and larger for falling signals, as indicated with dashed lines in Figure 2.5. The sample and hold configuration wherein the switch is inserted in the signal path introduces timing errors and signal distortion.

For sinusoidal input signals, $V_{in} = A_{in} sin(2\pi ft)$, the output waveform V_{out} is given by

$$V_{out} = A_{in} sin \left\{ 2\pi f \left[t + \frac{t_f}{V_H - V_L}(V_H - V_T) - \frac{A_{in} t_f}{V_H - V_L} sin(2\pi ft) \right] \right\}. \tag{2.16}$$

The output result is an analog waveform which is harmonic distortioned in comparison with the input signal.

For the circuit of Figure 2.3(b), where the sampling switch is placed in the signal return path, the actual sampling time is given by

$$t'_s = t_s + \frac{t_f}{V_H - V_L}(V_H - V_C - V_T), \tag{2.17}$$

as illustrated in Figure 2.6. In the same manner can be determined

$$\frac{dV_{out}}{dt} = \frac{dV_{in}}{dt} \tag{2.18}$$

and for sinusoidal input signals, $V_{in} = A_{in}sin(2\pi ft)$,

$$V_{out} = A_{in}sin\left\{2\pi f\left[t + \frac{t_f}{V_H - V_L}(V_H - V_C - V_T)\right]\right\}. \tag{2.19}$$

Thus, there is a constant time delay for pulse inputs and a constant phase shift for input sine waves. As a conclusion, the circuit in Figure 2.3(b) exhibits superior performance in respect to amplitude and timing errors.

2.6 CMOS Transmission Gate Switch

The CMOS transmission gate simply consists of a complementary pair of MOS transistors connected in parallel. In comparison with MOS transistors, the CMOS transmission gates require the generation of complementary control signals, which could be difficult to implement in high speed sampling circuits. In the following subsection the error voltage terms for the complementary switch are described.

2.6.1 CMOS Switch Resistance

In Figure 2.7 is represented a basic sample and hold configuration of a CMOS transmission gate switch placed in signal path. The on resistances of the NMOS and PMOS transistors are

$$R_{DSn} = \frac{1}{\dfrac{\partial I_{DSn}}{\partial V_{DSn}}} \approx \frac{1}{\mu_n C_{ox}\dfrac{W_n}{L_n}(V_{GSn} - V_{Tn})} \tag{2.20}$$

$$R_{DSp} = \frac{1}{\dfrac{\partial I_{DSp}}{\partial V_{DSp}}} \approx \frac{1}{\mu_p C_{ox}\dfrac{W_p}{L_p}(-V_{GSp} + V_{Tp})} \tag{2.21}$$

where μ_p is the hole mobility. The conductance of the complementary CMOS switch is simply the sum of the individual NMOS and PMOS conductances

$$\frac{1}{R_{DS}} = \frac{1}{R_{DSn}} + \frac{1}{R_{DSp}}. \tag{2.22}$$

With $V_{GSn} = V_{Gn} - V_{in}$, $V_{GSp} = V_{Gp} - V_{in}$, and $V_{Tn} = -V_{Tp} = V_T$, this equation can be rewritten as

$$\begin{aligned}\frac{1}{R_{DS}} \approx \left(\mu_p\frac{W_p}{L_p} - \mu_n\frac{W_n}{L_n}\right)C_{ox}V_{in} + \\ +\mu_n C_{ox}\frac{W_n}{L_n}(V_{Gn} - V_T) + \mu_p C_{ox}\frac{W_p}{L_p}(-V_{Gp} - V_T).\end{aligned} \tag{2.23}$$

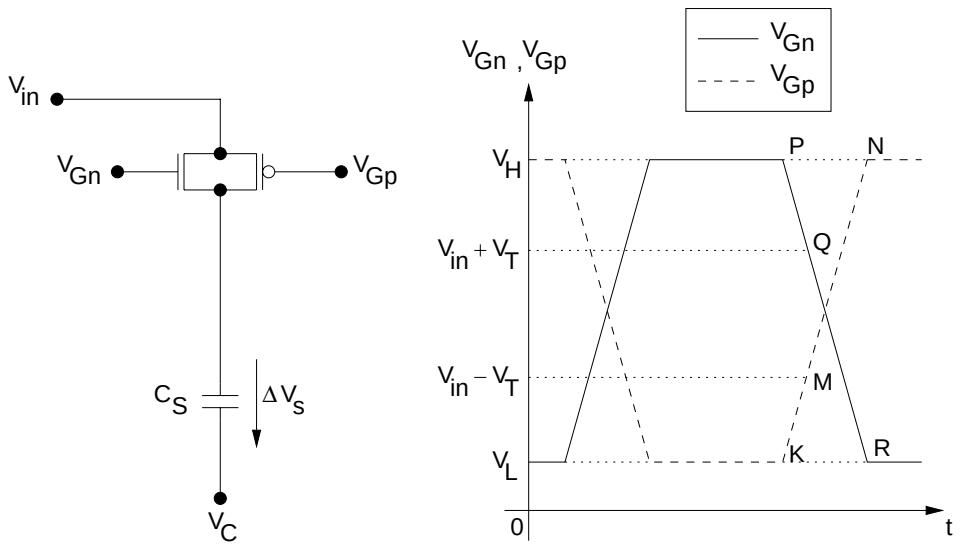

Figure 2.7: Schematic of the CMOS switch placed in signal path.

The conductance of the transmission gate depends on the input signal level as expressed in (2.23). However, the first term in this equation can be eliminated by choosing the width over length ratios of the transistors according to their mobility ratio

$$\frac{W_n}{L_n} = \left(\frac{\mu_p}{\mu_n}\right)\frac{W_p}{L_p}. \tag{2.24}$$

In practice, a fraction of the input level dependence will remain since the ratio of the mobilities can not be accurately controlled in the fabrication process.

2.6.2 Error Voltage

It is assumed that both transistors NMOS and PMOS turn off simultaneously and therefore the error voltages can be summed. For the circuit configuration in Figure 2.7 the voltage ΔV_s across the storage capacitor becomes

$$\Delta V_s = V_{in} - V_C - V_p \tag{2.25}$$

with

$$V_p = V_{pn} + V_{pp} \tag{2.26}$$

where V_{pn} and V_{pp} are pedestal voltages for NMOS and PMOS transistors due to charge injection and clock feedthrough effect. The error voltage V_{pn} can be written as in (2.5)

$$V_{pn} = \frac{\alpha C_{ox} W_n L_n}{2C_S}(V_H - V_{in} - V_T) + \frac{C_{ov}}{C_{ov} + C_S + C_p}(V_{in} - V_L + V_T) \tag{2.27}$$

and the error voltage V_{pp} can be derived in a similar fashion to that for the NMOS transistor with the following result:

$$V_{pp} = -\frac{\alpha C_{ox} W_p L_p}{2C_S}(V_{in} - V_L - V_T) - \frac{C_{ov}}{C_{ov} + C_S + C_p}(V_H - V_{in} + V_T). \tag{2.28}$$

The total pedestal error voltage V_p is

$$V_p = \left[\frac{2C_{ov}}{C_{ov} + C_S + C_p} - \frac{\alpha C_{ox}}{2C_S}(W_n L_n + W_p L_p)\right] V_{in} +$$
$$+\frac{\alpha C_{ox}}{2C_S}\left[W_n L_n (V_H + V_L) + (W_p L_p - W_n L_n) V_T\right] - \frac{C_{ov}}{C_{ov} + C_S + C_p}(V_H + V_L). \tag{2.29}$$

The total pedestal voltage can be split into the gain error ε and offset voltage V_{of},

$$V_p = \varepsilon V_{in} + V_{of}. \tag{2.30}$$

Minimum error voltage in (2.29) is achieved for equivalent areas of both transistors

$$W_n L_n = W_p L_p. \tag{2.31}$$

Under this condition the pedestal voltage becomes

$$V_p = \left(\frac{2C_{ov}}{C_{ov} + C_S + C_p} - \frac{\alpha C_{ox} W_n L_n}{C_S}\right) V_{in} +$$
$$+\frac{\alpha C_{ox} W_n L_n}{2C_S}(V_H + V_L) - \frac{C_{ov}}{C_{ov} + C_S + C_p}(V_H + V_L) \tag{2.32}$$

and the gain error and offset voltage are

$$\varepsilon = \frac{2C_{ov}}{C_{ov} + C_S + C_p} - \frac{\alpha C_{ox} W_n L_n}{C_S} \tag{2.33}$$

$$V_{of} = \frac{\alpha C_{ox} W_n L_n}{2C_S}(V_H + V_L) - \frac{C_{ov}}{C_{ov} + C_S + C_p}(V_H + V_L). \tag{2.34}$$

The pedestal voltages introduced in the circuit shown in Figure 2.8 can be written for NMOS transistor as in (2.9)

$$V_{pn} = -\frac{\alpha C_{ox} W_n L_n}{2C_S}(V_H - V_C - V_T) - \frac{C_{ov}}{C_{ov} + C_S + C_p}(V_C - V_L + V_T) \tag{2.35}$$

and for PMOS transistor as

$$V_{pp} = \frac{\alpha C_{ox} W_p L_p}{2C_S}(V_C - V_L - V_T) + \frac{C_{ov}}{C_{ov} + C_S + C_p}(V_H - V_C + V_T). \tag{2.36}$$

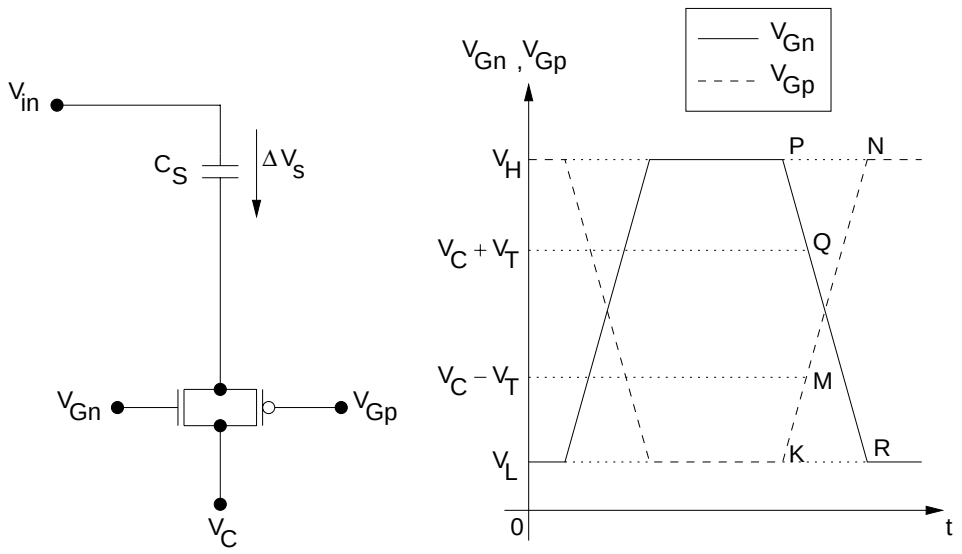

Figure 2.8: Schematic of the CMOS switch placed in signal return path.

The total pedestal voltage V_p is the sum of the individual contributions as in (2.26)

$$V_p = \frac{\alpha C_{ox}}{2C_S}\left[W_pL_p(V_C - V_L) - W_nL_n(V_H - V_C) + (W_nL_n - W_pL_p)V_T\right] + \\ + \frac{C_{ov}}{C_{ov} + C_S + C_p}(V_H + V_L - 2V_C) \qquad (2.37)$$

and is independent of the input signal level. Under the condition that $W_nL_n = W_pL_p$ for the circuit simplifies to

$$V_p = \frac{\alpha C_{ox}W_nL_n}{2C_S}(2V_C - V_L - V_H) + \frac{C_{ov}}{C_{ov} + C_S + C_p}(V_H + V_L - 2V_C). \qquad (2.38)$$

Thus the gain error and offset voltage become

$$\varepsilon = 0 \qquad (2.39)$$

$$V_{of} = \frac{\alpha C_{ox}W_nL_n}{2C_S}(2V_C - V_L - V_H) + \frac{C_{ov}}{C_{ov} + C_S + C_p}(V_H + V_L - 2V_C). \qquad (2.40)$$

As is the case for a single transistor switch, the circuit configuration with the switch in the signal path has a pedestal voltage that is dependent on the input signal voltage (2.32), whereas V_p is constant when the switch is inserted in the signal return path (2.38).

In this subsection it was assumed that the two complementary switches turn off simultaneously and part of the injected channel charge thus cancels. In practice, this is hard to accomplish, and the error voltages may be larger than suggested by (2.32) and (2.38). An important remark is that the gain error of the CMOS transmission gate is larger than the gain error of the MOS transistor when the switches are placed in signal path.

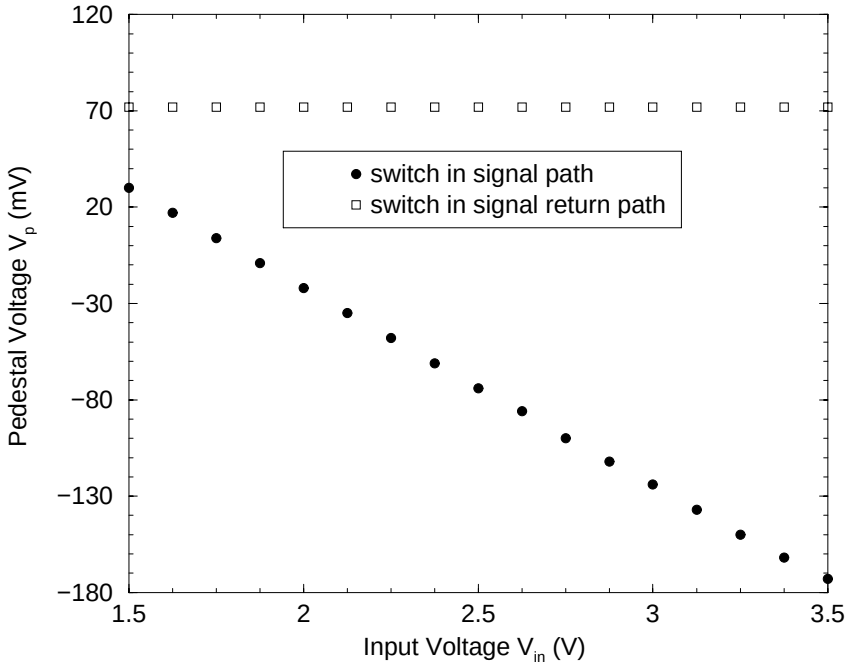

Figure 2.9: Pedestal voltage as a function of input voltage for CMOS switch.

The optimum performance for a CMOS transmission gate can be achieved using (2.24) and (2.31) to determine the geometry of the transistors. These relations give

$$L_n = L_p\sqrt{\frac{\mu_n}{\mu_p}} \tag{2.41}$$

and

$$W_p = W_n\sqrt{\frac{\mu_n}{\mu_p}}. \tag{2.42}$$

For AMS 0.8 μm CMOS technology the mobilities are listed in Table A.1 of Appendix A and therefore (2.41) and (2.42) can be rewritten as

$$L_n \approx 1.665L_p \tag{2.43}$$

and

$$W_p \approx 1.665W_n. \tag{2.44}$$

The two circuits in Figure 2.7 and Figure 2.8 have been implemented in AMS 0.8 μm CMOS technology and simulated with SPICE. The values of the pedestal voltages are plotted as a function of the input voltage and the results are shown in Figure 2.9. The storage capacitor was 500 fF. W_n and L_p were set to 25 μm and 0.8 μm, respectively. L_n and W_p were calculated from (2.43) and (2.44) with the values 1.33 μm and 41.6 μm. The gate voltages were two ramps of 300 ps each one. For an input voltage range of 2 V, the pedestal voltage varies by 140 mV when the switch is inserted in signal path (Figure 2.7), or is constant for the alternative configuration (Figure 2.8).

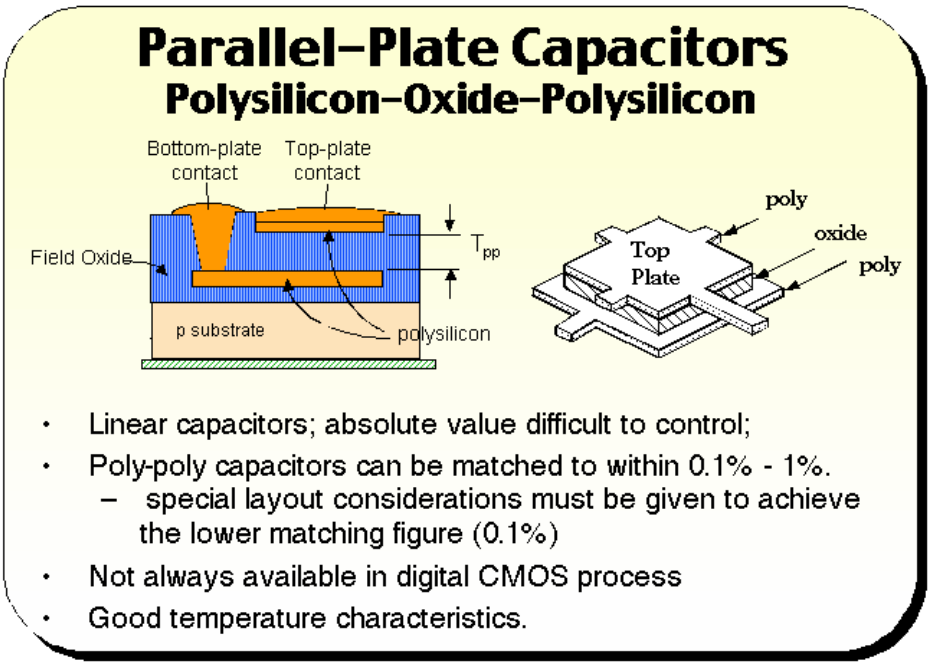

Figure 2.10: Physical structure of poly-to-poly capacitor.

2.7 Capacitors

The quality of capacitors determines the performance of an analog memory. Important issues are the matching of nominally identical capacitors and the absolute sizes and matching of associated parasitic capacitances. There are basically three types of capacitors suitable for analog circuit design available in CMOS processes: poly-over-diffusion capacitors, metal-to-metal capacitors and poly-to-poly capacitors. The first type of capacitor is formed using a polysilicon layer on top of crystalline silicon separated by a dielectric (silicon dioxide layer). In order to achieve a low voltage coefficient capacitor, the bottom plate must be heavily doped diffusion, which generally requires an extra implantation step in the fabrication process. The second type of capacitor is that formed by two metal layers separated by a dielectric. The advantages of this capacitor are its low voltage dependence and a good temperature characteristic. Finally, the third type of capacitor consists of two polysilicon layers separated by silicon dioxide, as illustrated in Figure 2.10. It can be seen that a double polysilicon process is needed to implement this capacitor since both the upper and lower plates are formed with polysilicon. The dielectric is formed by a thin silicon dioxide layer which can only be produced by using several steps beyond the usual single polysilicon process. The advantages of this capacitor are nearly voltage independent parasitic capacitance, good matching (up to 1 %) and a good temperature characteristic. A typical value for the capacitance in AMS 0.8 μm CMOS technology with poly-to-poly capacitors is 1.77 fF/μm^2, while the associated bottom plate parasitic capacitance is 0.066 fF/μm^2 [40].

2.8 Matching Properties of Memory Cell

In analog memory applications the uniformity of the memory cell response in one channel is more important than the absolute channel gain and offset. The uniformity is affected by two principal sources of error: inaccuracies in the fabrication process [4]–[6] and control signal feedthrough.

The analog memory cells are designed with the geometry identically but the imperfections in the fabrication process determine a mismatching degree from cell to cell. In addition, there are variations in the area of the storage capacitor plates and the thickness of the dielectric. The characterisation of mismatch in MOS transistors is more complex than that in the case of capacitors. The matching of transistor characteristics on a chip is determined by the matching of threshold voltages, mobilities, oxide and gate overlap capacitances, and the widths and lengths of the transistor gates. The main contribution to cell response variations within a memory channel is the mismatch in the charge injection during turn off of the switch.

Assuming that the variations in width δW and length δL of two mismatched transistors in a channel are equal $\delta W = \delta L = \delta P$ then

$$\delta(WL) = (W + \delta P)(L + \delta P) - WL \approx (W + L)\delta P, \tag{2.45}$$

where $\delta(WL)$ is the variation in area. For the circuit configuration in Figure 2.3(b) the pedestal voltage due to the charge injection from (2.9) is

$$V_{p1} = -\frac{\alpha C_{ox} WL}{2C_S}(V_H - V_C - V_T). \tag{2.46}$$

The variation in pedestal voltage δV_{p1} can be written as

$$\delta V_{p1} = -\frac{\alpha C_{ox}\delta(WL)}{2C_S}(V_H - V_C - V_T). \tag{2.47}$$

Inserting (2.45) in (2.47) yields

$$\delta V_{p1} \approx -\frac{\alpha C_{ox}(W + L)\delta P}{2C_S}(V_H - V_C - V_T). \tag{2.48}$$

The variation in error voltage due to the nonuniform charge injection δV_{p1} is thus proportional to the channel width and length of the sampling transistor.

The time constant τ with which the voltage across C_S follows a change in the input voltage depends on the on resistance R_{DS} of the sampling switch and the size of the capacitor,

$$\tau = R_{DS} C_S. \tag{2.49}$$

If it is assumed that $W \gg L$, (2.2) and (2.48) are inserted into (2.49), the time constant τ can be approximated as

$$\tau \approx -\frac{\alpha L \delta P}{2\mu_n \delta V_{p1}}. \tag{2.50}$$

Thus, switches with smaller W/L ratio yield smaller pedestal mismatches but limit the signal bandwidth of the sampling cell.

In some analog memory applications CMOS transmission gates are used as switches because their absolute pedestal voltages reduced, as discussed in Section 2.6. However, the use of CMOS switches does not improve the matching of the sampling cell performance, since the pedestal error voltages δV_{p1} of the PMOS and NMOS transistors are independent and the resulting pedestal error is therefore not cancelled. If the mismatch of the PMOS and NMOS transistors is uncorrelated, the total error voltage is then given by the square root of the sum of the squares of the individual error voltages.

Another potential source of charge injection mismatch is the variation in sampling capacitance. If δC_S is the variation in the sampling capacitance, the voltage error δV_{p1} from charge injection onto mismatched capacitors can be written as

$$\delta V_{p1} \approx -\frac{\alpha C_{ox} W L}{2C_S}\left(\frac{\delta C_S}{C_S}\right)(V_H - V_C - V_T). \tag{2.51}$$

Typically, this error is small compared to the error from the mismatch of the sampling switches and can therefore be neglected.

The second principal source of error is the feedthrough of control signals via the substrate and parasitic inter-layer capacitances. In analog memories, the input waveform is sampled sequentially onto a bank of memory cells. The capacitive coupling from control signal lines to individual memory cell nodes may not be uniform across the chip and therefore the layout of the circuit must be carefully designed to minimise coupling through parasitic inter-layer capacitances and through the substrate. In addition, perturbations in the power supply, ground, signal, buses can be the cause of memory cell performance mismatch, since the signal is captured at different times in the memory cells of the channel.

2.9 Summary

The MOS transistors make one of the best switch realisations available in integrated circuit form. They require small area, dissipate very little power, and provide zero offset, low on resistance and high off resistance. Together with storage capacitors, the NMOS transistors create basic sample and hold circuits necessary for acquiring analog waveforms. A voltage switch can be realised by a single NMOS or PMOS transistor, or with a CMOS transmission gate. One of the most serious limitations of the MOS switches is that error voltages are introduced due to the charge injection and clock feedthrough effect. The CMOS transmission gate shows a lower absolute error voltage when compared to a single MOS transistor. The clock circuitry for CMOS switches is more complex because of the requirement for a complementary clock which may be difficult to implement in high speed analog circuits. In addition, it is more important to have an uniformity of the individual memory cell responses in one channel than the absolute error voltage. Therefore the use of a MOS transistor as voltage switch in place of a CMOS transmission gate is suitable to assure an uniformity in the channel.

In a sample and hold circuit the voltage switch can be inserted in signal path or in signal return path. The error voltage is independent of the input signal level when the switch is placed in signal return path and can therefore be cancelled by a simple subtraction procedure. Furthermore, the sample and hold configuration wherein the switch is placed in signal return path introduces a constant time delay for ac input signals.

The analysis of sample and hold configurations presented in this chapter provides basic ideas for the design of analog memory circuits, as proposed in the following chapter.

Chapter 3

Analog Memory Circuit

3.1 Overview

In this chapter an analog memory circuit for use in high speed data acquisition systems has been introduced. A circuit implementation of the architecture and its theoretical performance are investigated in detail. A short description of the architectures of two chips implemented is presented in Section 3.2. The architecture of the analog memory core is identical for both chips implemented and is described in detail in the following section. The performances of the analog memory are evaluated through a theoretical analysis of dc transfer function, signal range, small signal acquisition bandwidth, acquisition time and leakage current.

3.2 Chips Architecture

Two chips for camera electronics of the Cherenkov telescope have been integrated in the Austria Microsystems (AMS) 0.8 μm complementary metal oxide semiconductor (CMOS) process with poly-to-poly capacitors. In Table 3.1 are presented the architectures for both chips. The write control circuit as well as the analog memory core are identically for both chips while the read control circuit is different. The analog memory core is described in detail in the following section and the write and read control circuits are discussed in Chapter 5. FASTSAMP-EV was the first experimental chip implemented followed by FASTSAMP-V1 which is more approached to the camera electronics requirements of the Cherenkov telescope.

The block diagrams of the chips are shown in Figure 3.1. The analog input signals are $AnalogInputCh1$ through $AnalogInputCh4$ while the analog outputs are $AnalogOutputCh1$ through $AnalogOutputCh4$. The analog waveforms applied at the four inputs are sampled and stored in the analog memory core which consists of four channels with 128 cells in each channel. The write address signals $w < 1 >$ through $w < 128 >$ are generated in the high speed write control circuit implemented to achieve 500 MHz sampling frequency. The read address signals $r < 1 >$ through $r < 128 >$ are generated in the read control circuit which operates at 100 kHz readout frequency. The

<table>
<tr><td colspan="2">Chip Name</td><td>FASTSAMP-EV
(Fast Sampling
Transmission Recorder
- Experimental Version)</td><td>FASTSAMP-V1
(Fast Sampling
Transmission Recorder
- First Version)</td></tr>
<tr><td rowspan="4">Architectures</td><td>Analog
Memory
Core</td><td colspan="2">- 4 channels with 128 memory cells in each channel
was proposed for acquiring analog waveforms</td></tr>
<tr><td>Write
Control
Circuit</td><td colspan="2">- sampling rate of 500 MHz
- consists of four 32 cell delay chains</td></tr>
<tr><td rowspan="2">Read
Control
Circuit</td><td>- implemented with
4 two-phase shift registers</td><td>- implemented with
a 1 of 128 decoder</td></tr>
<tr><td colspan="2">- readout frequency of 100 kHz</td></tr>
</table>

Table 3.1: Architectures for both chips.

other signals which appear in the block diagrams are provided externally.

The two control signals $ComIn$ and $ComOut$ which appear in the block diagram of FASTSAMP-EV chip in Figure 3.1(a) have been replaced by a single external signal $ComInOut$ necessary for FASTSAMP-V1 chip, as illustrated in Figure 3.1(b). Internally, this replacement has been done by using an inverter.

3.3 Analog Memory Core

3.3.1 Architecture

The proposed architecture of one channel of the analog memory core [26] is shown in Figure 3.2. V_B and V_C are dc reference voltages. The operation of the analog memory channel can be described into write and read phases. During the write phase, the switches S_{in} and S_{reset} are closed while S_{out} and read switches S_{r1} through S_{r128} are open. The input waveform is then sampled and stored on the storage capacitors C_1 through C_{128} by sequentially closing and opening the write switches S_{w1} through S_{w128}. After the analog input waveform has been stored, the switch S_{in} is opened and S_{out} is closed. The analog waveform recorded can be read out by consecutively closing and opening the read switches S_{r1} through S_{r128}.

The architecture presented in Figure 3.2 with a single readout amplifier offers a low power dissipation, small area, and minimum cell-to-cell variations. The use of independent write and read address switches for each cell simplifies the write and read control circuits considerably. As suggested in Chapter 2, the write switches are inserted in the signal return path. The capacitors are switched across the amplifier during readout in order to obtain a cell gain that is insensitive to the size of the sampling capacitor. The description and operation of the architecture shown in Figure 3.2 are analysed in the following subsections.

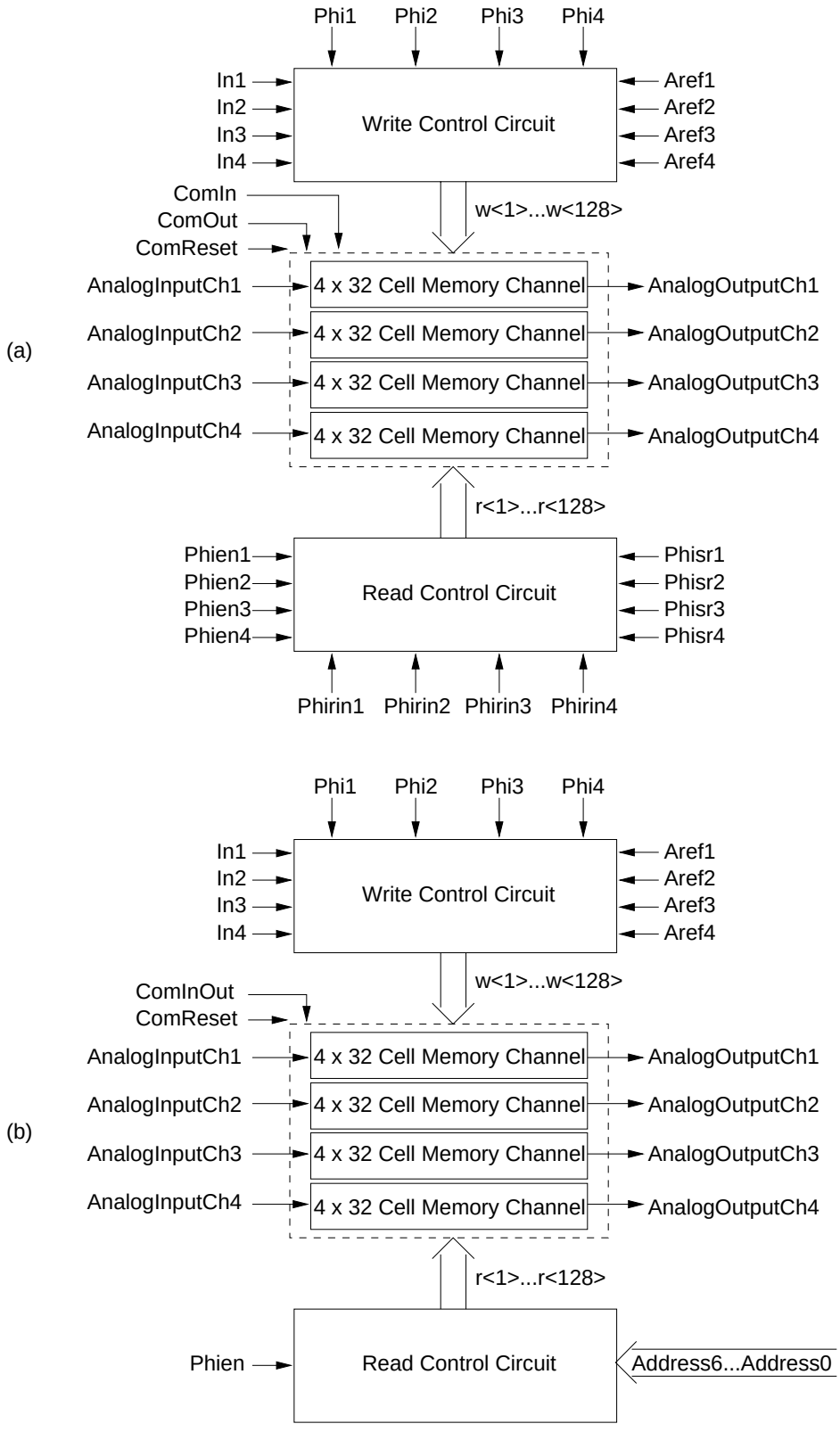

Figure 3.1: Block diagram for (a) FASTSAMP-EV and (b) FASTSAMP-V1 chips.

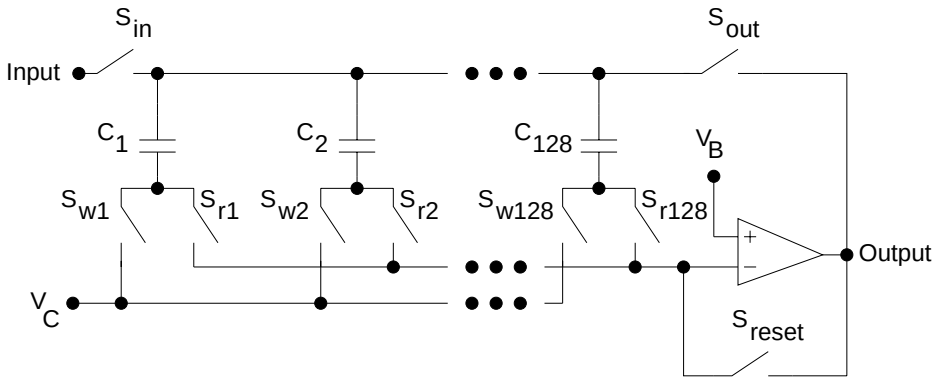

Figure 3.2: Memory architecture with one amplifier per channel.

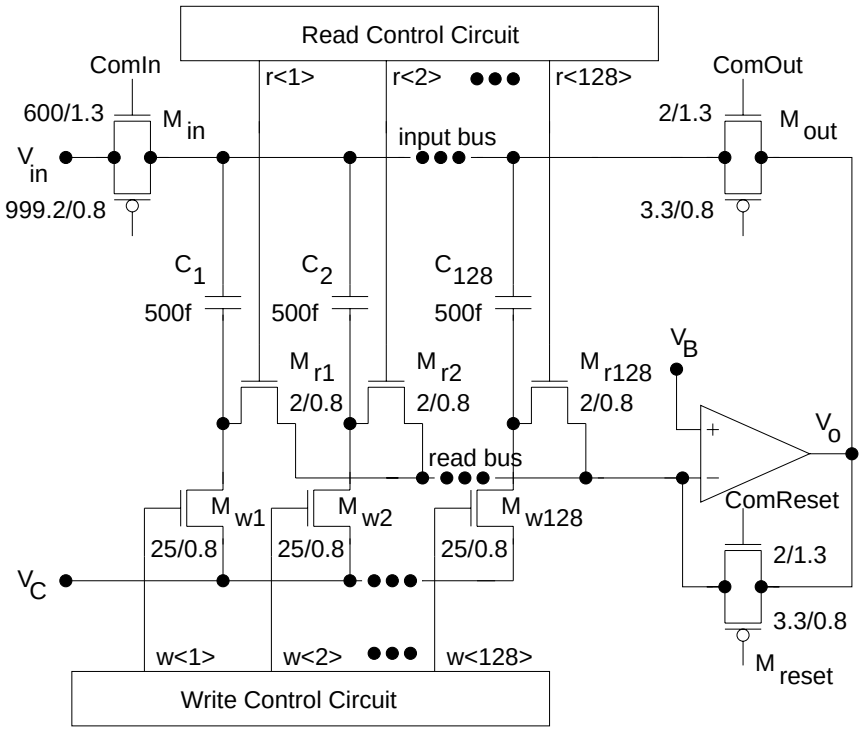

Figure 3.3: Simplified schematic of one analog memory channel.

3.3.2 Description

A simplified schematic of one channel of the proposed analog memory [27, 28], comprising 4 blocks of 32 cells, is shown in Figure 3.3. Each memory cell consists of a large write transistor M_{wi}, a minimum size read transistor M_{ri}, and a sampling capacitor C_i. The cells are addressed via write lines $w < 1 >$ through $w < 128 >$ and read lines $r < 1 >$ through $r < 128 >$. The voltage V_C is a dc reference common to the sources of all write transistors, M_{wi}.The switch M_{reset} serves to configure the operational amplifier as

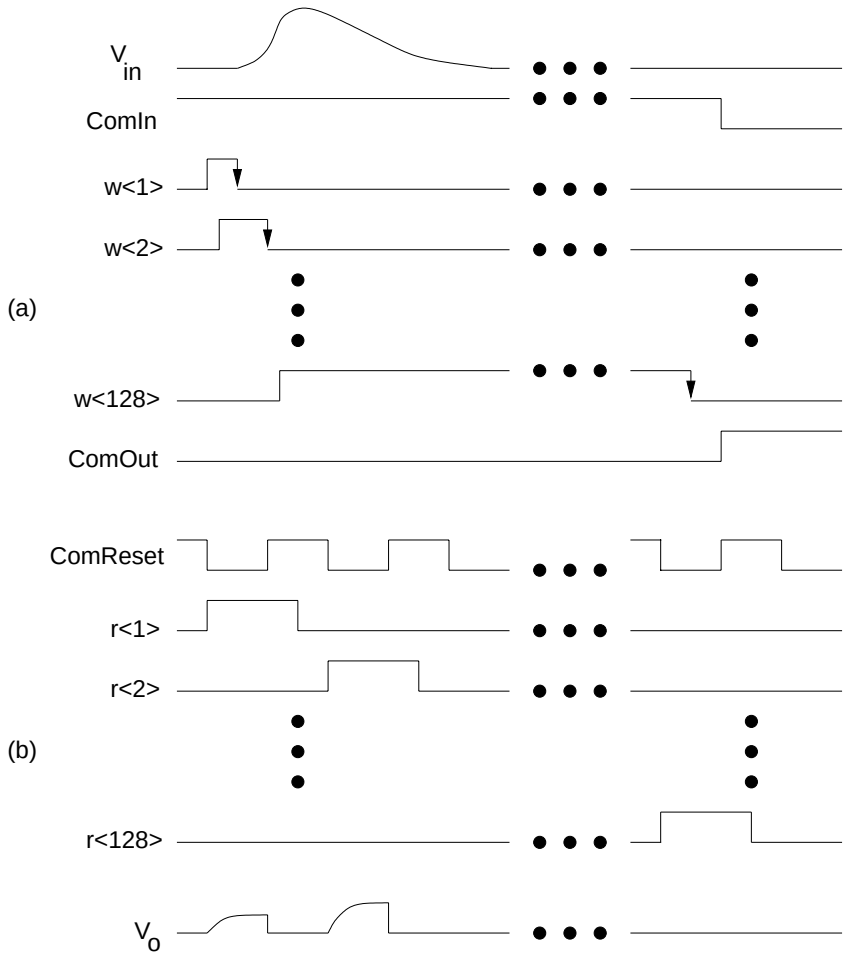

Figure 3.4: Timing diagram for (a) write and (b) read phases.

a voltage follower in order to force the nodes of the amplifier input and output to the dc bias level V_B during reset.

The channel dimensions of the NMOS and PMOS transistors comprising the input switch M_{in} are $W/L = 600$ μm/1.3 μm and $W/L = 999.2$ μm/0.8 μm, respectively. As suggested by (2.41) through (2.44), the relative sizes of these devices were chosen so as to minimise the signal dependence of the switch on resistance and the total error voltage. The drawn dimensions of the write and read transistors are $W/L = 25$ μm/0.8 μm and $W/L = 2$ μm/0.8 μm (minimum size), respectively. The storage capacitor was chosen of 500 fF and the output amplifier is a folded cascode design of the type described in Chapter 4.

The operation of the circuit can be described into write and read cycles. In the write phase, analog signals applied at the channel input, V_{in}, are sampled and stored in the memory cells at a high rate. The stored analog information is subsequently read out serially at the channel output, V_o, at a lower speed.

During the write phase, the switch M_{in} is turned on, connecting the signal V_{in} to the input bus, while the switch M_{out} and the read switches M_{r1} through M_{r128} are all off,

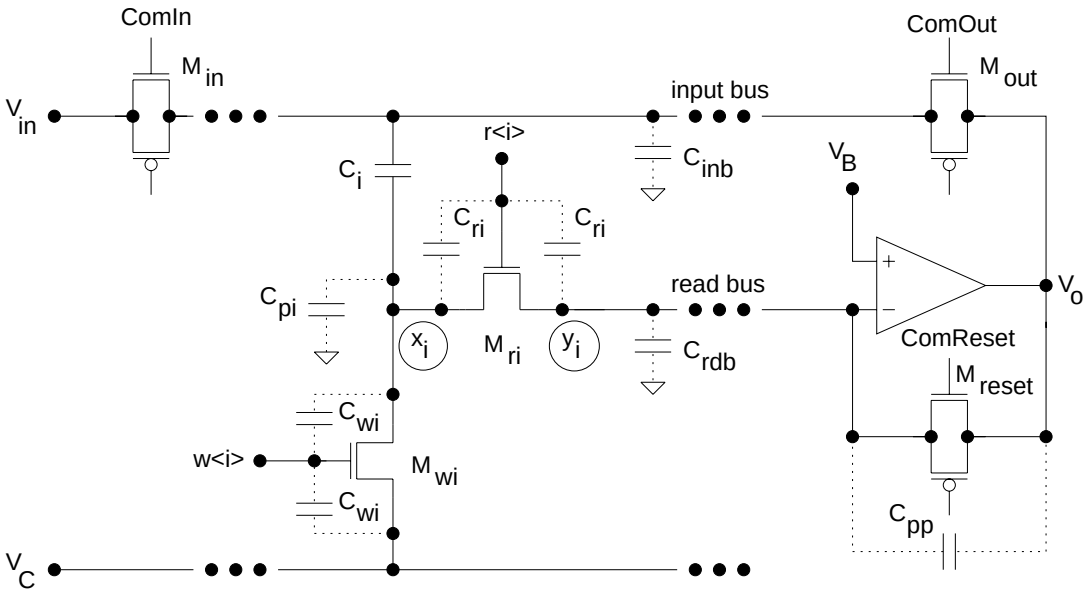

Figure 3.5: Analog memory channel with parasitic capacitances.

isolating the input bus from the read bus. The switch M_{reset} is on to keep the read bus at a defined potential $V_B = V_C = 2.5$ V during the entire write phase. An analog signal applied at the circuit's input is sampled onto the cell capacitors C_i by sequentially turning transistors M_{w1} through M_{w128} on and off, as illustrated in Figure 3.4(a). Samples of the input waveform at 128 discrete times are thereby stored in the memory channel.

The voltage ΔV_{si} stored across the capacitor C_i in the memory cell i, $1 \leq i \leq 128$, is after the sampling

$$\Delta V_{si} = V_{in} - V_C - V_{pwi}, \tag{3.1}$$

where V_{pwi} is the voltage error due to the charge injection and clock feedthrough effect in the switch M_{wi} during turn off. As derived in Appendix B, with the source and drain terminals of the write transistor at reference voltage V_C at turn off, the pedestal voltage V_{pwi} can be written as

$$V_{pwi} = -\frac{C_{wi} + \frac{C_{ox} W_{wi} L_{wi}}{2}}{C_{tot}} \sqrt{\frac{\pi U C_{tot}}{2\beta}} erf\left[\sqrt{\frac{\beta}{2UC_{tot}}}(V_H - V_C - V_T)\right] - \\ - \frac{C_{wi}}{C_{wi} + C_{pi} + C_i}(V_C - V_L + V_T) \tag{3.2}$$

where C_{wi} is the write transistor gate overlap capacitance, C_i is the sampling capacitance, V_T is the threshold voltage, V_L and V_H are the low and high levels of the write transistor gate voltage, C_{ox} is the oxide capacitance per unit area, W_{wi} and L_{wi} are the width and length of the write transistor, U is the slew rate of the gate voltage, C_{pi} is the capacitance associated with the cell sampling capacitor terminal connected to the write switch M_{wi},

$\beta = \mu_n C_{ox} W_{wi}/L_{wi}$, and μ_n is the electron mobility in the channel. The capacitance C_{tot} is

$$C_{tot} = C_i + C_{pi} + C_{wi} + \frac{C_{ox} W_{wi} L_{wi}}{2}. \tag{3.3}$$

The important fact of this investigation is that V_{pwi} remains independent of the input voltage, V_{in}.

The parasitic capacitances for one analog memory channel are illustrated in Figure 3.5 and listed in Table A.2 of Appendix A. The values have been extracted from the layout of the analog memory core which is identically for both chips. The slew rate of the gate voltage U with a typical value of 5 V/300 ps corresponds to the falling edges (300 ps) of the write address signals. The pedestal voltage V_{pwi} has been calculated from (3.2), $V_{pwi} = -130$ mV, in which (-80 mV) represents the charge injection contribution and (-50 mV) due to the clock feedthrough effect.

After the write phase has been completed and the input waveform is stored in the analog memory, the read cycle is initiated. During the readout, the switch M_{in} is turned off while M_{out} and M_{reset} are turned on, forcing both the input bus and the read bus to V_B. The switch M_{reset} is then turned off and the voltage stored in the first cell is read out by turning M_{r1} on as illustrated in Figure 3.4(b). This cycle is repeated for all cells. The input bus must always be forced back to V_B before a new cell is read out, otherwise the charge and parasitic capacitances will seriously degrade the circuit's performance. By turning the cell read switches off after the reset switch is turned on, the potential across the capacitors is initialised to nominally 0 V for the next write phase.

3.3.3 DC Transfer Function

Once the write switch is turned off, the cell capacitor nodes connected to the cell transistors are left in a high impedance state for the remainder of the write phase and the entire read phase. Therefore the charge at these nodes is conserved and only three parasitic capacitances influence the dc transfer function of a memory cell. One is the capacitance C_{pi}, the second parasitic capacitance is the gate overlap capacitance of the read switch, C_{ri}, and the third parasitic to be considered is the capacitance, C_{pp}, between the inverting input and the output of the amplifier.

The dc transfer function of the memory can be derived using the schematics illustrated in Figure 3.6 and Figure 3.7, which show a memory cell together with the readout amplifier before and after the cell is addressed for readout, respectively. The total charge stored at memory cell node x_i in Figure 3.6 after the write transistor M_{wi} is turned off is

$$Q_{x_i} = C_i(V_C + V_{pwi} - V_{in}) + C_{pi}(V_C + V_{pwi}) + C_{ri}(V_C + V_{pwi} - V_L). \tag{3.4}$$

The charge Q_{y_i} stored at the inverting input node y_i of the amplifier before the memory cell is addressed for readout is

$$Q_{y_i} = C_{ri}(V_B - V_L). \tag{3.5}$$

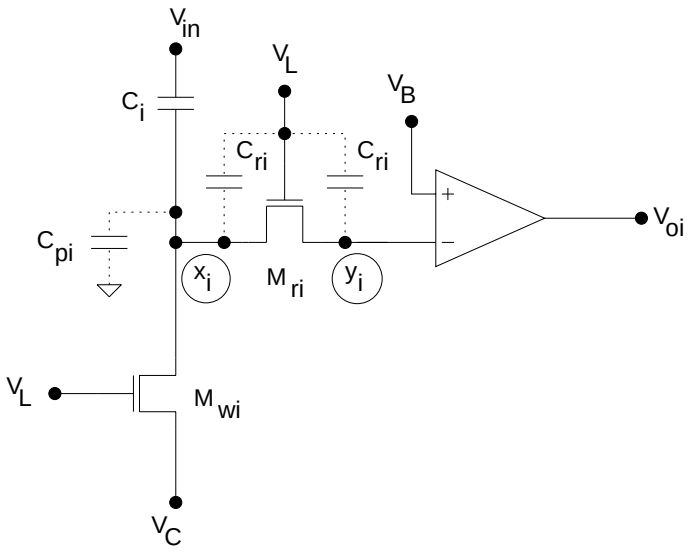

Figure 3.6: Circuit configuration before the memory cell is addressed for readout.

After the read switch has been turned on, as illustrated in Figure 3.7, the node x_i and node y_i are shorted and the total charge is

$$Q_{x_i y_i} = Q_{x_i} + Q_{y_i}. \tag{3.6}$$

The charge $Q_{x_i y_i}$ can be expressed as

$$\begin{aligned} Q_{x_i y_i} = (C_i + C_{pp})(V_{opm} - V_{oi}) + 2C_{ri}(V_{opm} - V_H) + \\ + C_{pi}V_{opm} - C_{ox}W_{ri}L_{ri}(V_H - V_{opm} - V_T), \end{aligned} \tag{3.7}$$

where W_{ri} and L_{ri} are the channel width and length of the read transistor. V_{opm} is the voltage of the inverting input of the amplifier,

$$V_{opm} = V_B - \frac{V_{oi} - V_B}{G}, \tag{3.8}$$

and G is the open-loop gain of the amplifier.

When memory cell i is selected for readout, the voltage at the output of the amplifier, V_{oi}, can be described as a function of the input voltage V_{in} in the form

$$V_{oi} = A_i V_{in} + V_{offi} \tag{3.9}$$

where A_i is the gain factor and V_{offi} is the offset voltage. By solving (3.4) to (3.8), the gain factor A_i is

$$A_i = \frac{1}{1 + \frac{C_{pp}}{C_i} + \frac{1}{G}\left(1 + \frac{C_{pp} + C_{pi}}{C_i} + \frac{2C_{ri}}{C_i} + \frac{C_{ox}W_{ri}L_{ri}}{C_i}\right)} \tag{3.10}$$

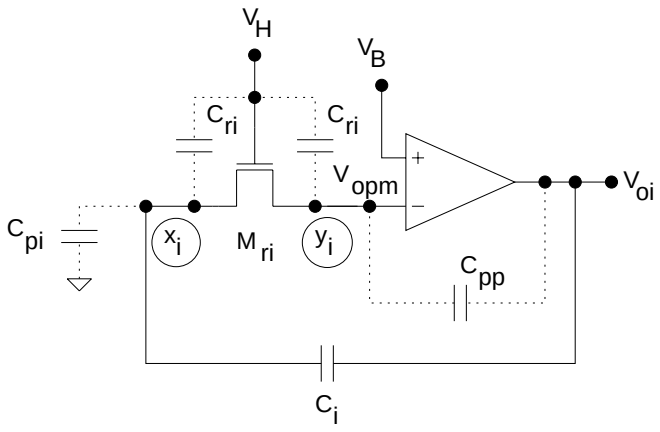

Figure 3.7: Circuit configuration when the memory cell is addressed for readout.

and the offset voltage V_{offi}

$$V_{offi} = V_B - \frac{C_i}{C_i + C_{pp}} V_C + \frac{C_{pi}}{C_i + C_{pp}} (V_B - V_C) - \frac{C_i + C_{pi} + C_{ri}}{C_i + C_{pp}} V_{pwi} - \\ - \frac{C_{ri}}{C_i + C_{pp}} (2V_H - 2V_L - V_B + V_C) - \frac{C_{ox} W_{ri} L_{ri}}{C_i + C_{pp}} (V_H - V_B - V_T). \qquad (3.11)$$

The sampling capacitance C_i can be made large compared to C_{pp} and to C_{ri}. Also, the open-loop amplifier gain G is large enough in practical CMOS circuits. With these approximations and supposing that the reference voltage V_C is set to the bias voltage V_B, (3.10) and (3.11) can be rewritten as

$$A_i = \frac{1}{1 + \dfrac{C_{pp}}{C_i}} \qquad (3.12)$$

and

$$V_{offi} = -\left(1 + \frac{C_{pi}}{C_i}\right) V_{pwi}. \qquad (3.13)$$

Because both A_i and V_{offi} are independent of the input voltage V_{in}, as indicated by (3.9) to (3.13), it follows that the output voltage of the analog memory V_o is a linear function of V_{in}. With the parasitic capacitance values listed in Table A.2 of Appendix A and V_{pwi} of (-130 mV), the gain cell and offset voltage have been calculated from (3.12) and (3.13) and their values are 0.979 and 141 mV, respectively.

3.3.4 Signal Range

Since the cell capacitor nodes connected to the cell transistors remain floating after the write switch is turned off, care must be taken to ensure that no leakage occurs at those nodes, for all possible ac and dc input signals, during the write and read

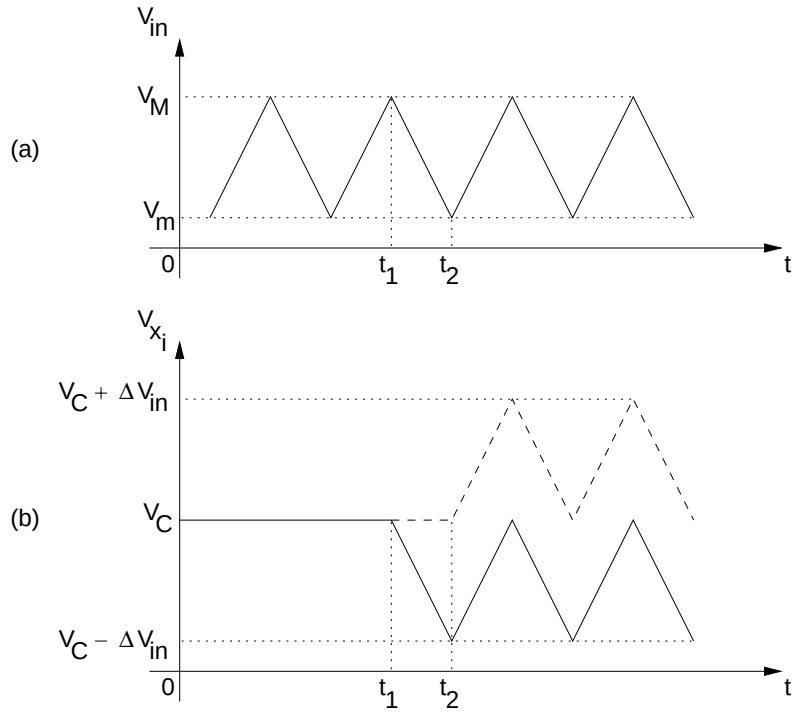

Figure 3.8: (a) Triangle input waveform. (b) Waveforms at node x_i in Figure 3.5 with the write switch turned off at time t_1 (solid line) and t_2 (dashed line).

phases. In Figure 3.8(a) is represented a triangle input waveform with a voltage swing of $\Delta V_{in} = V_M - V_m$. Shown in Figure 3.8(b) are the waveforms at node x_i in Figure 3.5 with the write switch turned off at times t_1 and t_2, respectively. The voltage V_{x_i} at node x_i must not fall below the low level of the gate voltage V_L to avoid subthreshold leakage. Therefore $V_{x_i} \geq V_L$ and the maximum input voltage swing ΔV_{in} in the write phase is limited to

$$\Delta V_{in} \leq V_C - V_L. \tag{3.14}$$

In the read phase, the maximum voltage swing ΔV_{oi} at the output of the amplifier must be less than $(V_B - V_L)$ to avoid the subthreshold leakage. It follows from (3.9) that the corresponding limit for the input voltage swing during the write phase is then

$$\Delta V_{in} = \frac{\Delta V_{oi}}{A_i} \leq \frac{V_B - V_L}{A_i}. \tag{3.15}$$

3.3.5 Small Signal Acquisition Bandwidth

The small signal bandwidth of the analog memory is governed by the impedances of the MOS switches, the size of the sampling capacitance, and the size of associated parasitic capacitances. The equivalent circuit of a memory cell during signal acquisition is shown in Figure 3.9. R_{wi} and R_{is} represent the write and input switch on resistances. Their values are calculated by (2.2) and (2.20) to (2.22) and given in Table A.2 of Appendix A.

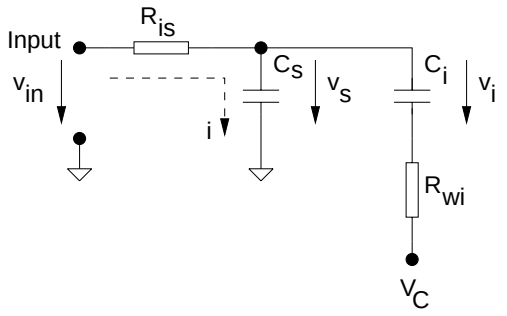

Figure 3.9: Equivalent circuit of a memory cell during signal acquisition.

In general, the on resistance of the input switch should be low. The capacitance C_s is given by

$$C_s = C_{is} + C_{inb} \tag{3.16}$$

where C_{is} is the drain capacitance of the input switch and C_{inb} is the capacitance between the input bus and ground. The values of these capacitances have been extracted from the analog memory core layout and are also given in Table A.2.

As long as $R_{is} \ll R_{wi}$ the current i is flowing through R_{is} and C_s. Therefore the following transfer functions in Laplace can be written as

$$\frac{v_s}{v_{in}}(s) = \frac{1}{1 - \dfrac{s}{p_s}} \tag{3.17}$$

and

$$\frac{v_i}{v_s}(s) = \frac{1}{1 - \dfrac{s}{p_i}} \tag{3.18}$$

with $p_s = -1/R_{is}C_s$ and $p_i = -1/R_{wi}C_i$. Thus the frequency dependence of the voltage v_i across the sampling capacitor C_i is given by

$$\frac{v_i}{v_{in}}(s) = \frac{1}{\left(1 - \dfrac{s}{p_i}\right)\left(1 - \dfrac{s}{p_s}\right)}. \tag{3.19}$$

Because $|p_s|$ is much larger than $|p_i|$, (3.19) can be approximated by a single pole expression

$$\frac{v_i}{v_{in}}(s) \approx \frac{1}{1 - \dfrac{s}{p_i}}. \tag{3.20}$$

The cell bandwidth B for the circuit is given by

$$B = f_{-3dB} = -\frac{p_i}{2\pi}, \tag{3.21}$$

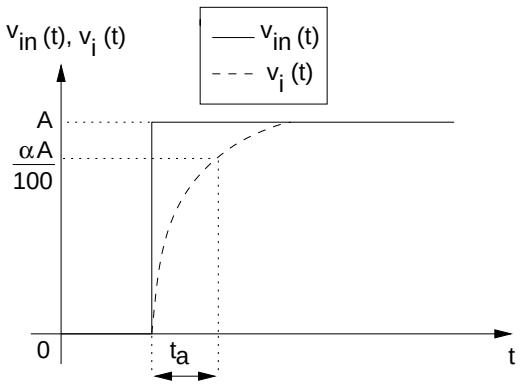

Figure 3.10: Time response of the analog memory cell to a step input.

where f_{-3dB} is the -3 dB frequency. The on resistance R_{wi} can be expressed as in (2.2) with $V_{GS} = V_H - V_C$ and therefore (3.21) becomes

$$B = \frac{\mu_n C_{ox} \frac{W_{wi}}{L_{wi}} (V_H - V_C - V_T)}{2\pi C_i}. \tag{3.22}$$

For applications where a high input bandwidth is required, the write transistor must be made large because the cell bandwidth B is determined by the size of the sampling capacitor and the resistance of the write transistor.

3.3.6 Acquisition Time

The acquisition time is the length of time that the write address switch must stay on in order to acquire a full scale step at the input to a specified accuracy. The small signal transfer function of the analog memory can be approximated by a single pole expression as in (3.20). The circuit response illustrated in Figure 3.10 to a voltage step $v_{in}(s) = A/s$ at the input is

$$v_i(s) = A\left(\frac{1}{s} - \frac{1}{s - p_i}\right). \tag{3.23}$$

The time response to a step input is therefore

$$v_i(t) = A(1 - e^{p_i t}). \tag{3.24}$$

For a given accuracy α in %, (3.24) can be rewritten as

$$\frac{\alpha A}{100} = A(1 - e^{p_i t_a}), \tag{3.25}$$

where t_a is the acquisition time. Inserting $p_i = -1/R_{wi}C_i$ in (3.25) yields

$$t_a = -R_{wi}C_i ln\left(1 - \frac{\alpha}{100}\right). \tag{3.26}$$

For instance, for a given accuracy α of 99%, $R_{wi} = 180\ \Omega$ and $C_i = 500$ fF, the acquisition time calculated by (3.26) is $t_a \approx 415$ ps. In conclusion, the acquisition time of the analog memory for a given accuracy is less than 0.5 ns.

3.3.7 Leakage Current

Leakage currents across drain-bulk and source-bulk *pn*-junctions occur in both PMOS and NMOS transistors. The leakage currents depend of temperature and double for every 8 °C rise in temperature [26]. At room temperature, a typical value of the leakage current is $I_{leak} = 15$ fA/μm^2. For the write switch transistor M_{wi} with W_{wi}/L_{wi} ratio of 25 μm/0.8 μm the leakage current is $I_{leak}W_{wi}L_{wi}$ (0.3 pA). The rate of discharge for a 500 fF storage capacitor C_i is then $I_{leak}W_{wi}L_{wi}/C_i$ (6 μV/μs). The magnitudes of leakage currents are below the nanoampere range, so that they have a negligible effect in the analog memory core.

3.4 Summary

In this chapter an analog memory circuit for use in high speed data acquisition systems has been introduced. Each channel in this memory consists of 128 memory cells for storing samples of the input waveform and a single operational amplifier for reading out the stored samples. Each memory cell comprises a storage capacitor, a write switch and a read switch.

The dc transfer function of the analog memory circuit was derived and it was shown that the output voltage is a linear function of the input voltage. In order to achieve a high input bandwidth the write transistors must be made large, which may increase the cell-to-cell response variations. However, in the proposed analog memory architecture the pedestal voltages are not dependent on the input signal level. The pedestal voltage is governed by charge injection and clock feedthrough effect at turn off of the large write switch and a theoretical expression for this voltage is derived in Appendix B.

The main analog memory core has been designed so that the sampling time of the individual memory cells is independent of the input signal level. This removes the need for an extensive ac calibration and sampling time error correction procedures.

Chapter 4

Readout Operational Amplifier

4.1 Overview

Each channel of the analog memory architecture presented in the previous chapter includes an on-chip operational amplifier which is used during the readout phase. The amplifier must provide sufficient gain, speed, and noise performance for the intended analog memory application. In addition, the noise contribution of the amplifier to the total circuit noise should be small compared to the noise of the analog memory. The folded cascode architecture chosen is simple and attractive because the load capacitance provides the frequency compensation. The amplifier must drive off-chip several picofarads and therefore the stability is assured. The folded cascode amplifier is capable of achieving a high stable loop bandwidth with a large capacitive load. The circuit of the amplifier is described in detail in Section 4.2. In Section 4.3 the folded cascode architecture is examined with respect to gain and bandwidth. Simulation results are presented with the amplifier in both follower and inverting amplifier configurations. In the following section is analysed the total noise including flicker and thermal noise.

4.2 Amplifier Circuit

The schematic of the folded cascode amplifier [28] with a p-channel differential input pair is shown in Figure 4.1. The circuit comprises a cascade of a common source and a common gate stage. The use of this configuration improves the frequency response and power supply rejection. The small signal impedance at the output node is increased and the voltage gain is simply the product of the transconductance of the input transistors and the impedance of the output node. An important performance advantage of this circuit is that the load capacitance contributes the dominant pole and performs the function of compensation capacitor. The transistors M_3 and M_4 operate as current sources and M_7 through M_{10} operate as an improved Wilson current source. The currents through M_3 and M_4 equal the sum of the currents from the differential pair, M_1 and M_2, and from the cascode mirror formed by M_7 through M_{10}. The reference voltages V_{ref1}, V_{ref2}, V_{bias} are generated by the bias generator formed by the transistors $M_{11} - M_{16}$. The drawn

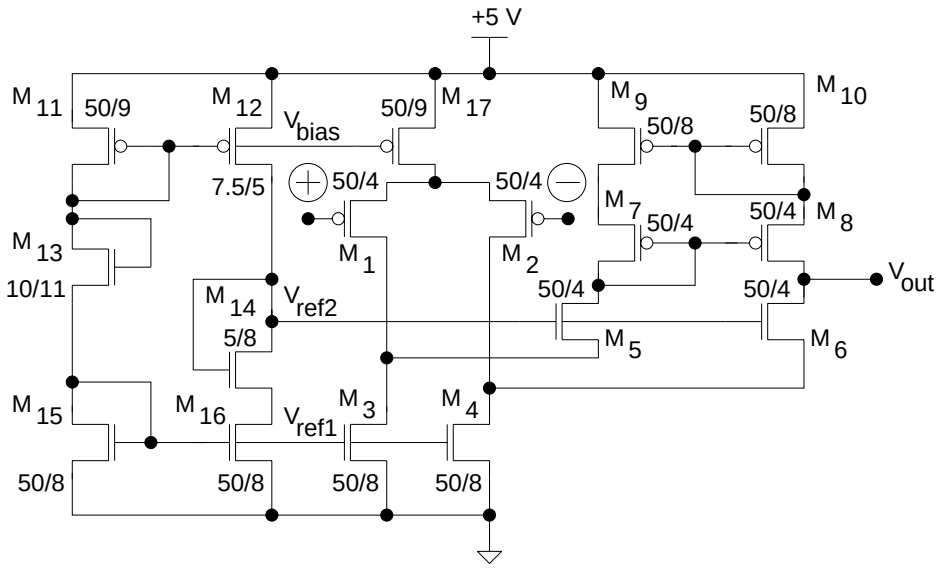

Figure 4.1: Schematic of the folded cascode amplifier.

Transistors	Current [μA]	Transconductance [μA/V]	Conductance [nA/V]
M_1, M_2	20	124.8	147.2
M_3, M_4	40	192.5	1130
M_5, M_6	20	206.7	176.9
M_7, M_8	20	122.3	357.4
M_9, M_{10}	20	84.12	210.3

Table 4.1: Dc operating points of MOS transistors.

Variable	Simulation
V_{bias}	3.554 V
V_{ref1}	1.242 V
V_{ref2}	1.614 V
Power Dissipation	653 μW

Table 4.2: Simulation results.

dimensions of the channel lengths and widths of MOS transistors are illustrated in Figure 4.1.

The dc voltage gain G of the amplifier [29, 30] in Figure 4.1 can be approximated by the product of the transconductance of the input transistor, g_{m1}, and the impedance at the output node, r_{out},

$$G \approx g_{m1} r_{out} \approx \frac{g_{m1}}{\frac{g_{ds6}(g_{ds2}+g_{ds4})}{g_{m6}} + \frac{g_{ds8}g_{ds10}}{g_{m10}}} \tag{4.1}$$

where g_{ds2}, g_{ds4}, g_{ds6}, g_{ds8}, g_{ds10} and g_{m6}, g_{m10} are conductances and transconductances of the MOS transistors. The dominant pole p_1 of the circuit is determined by the impedance

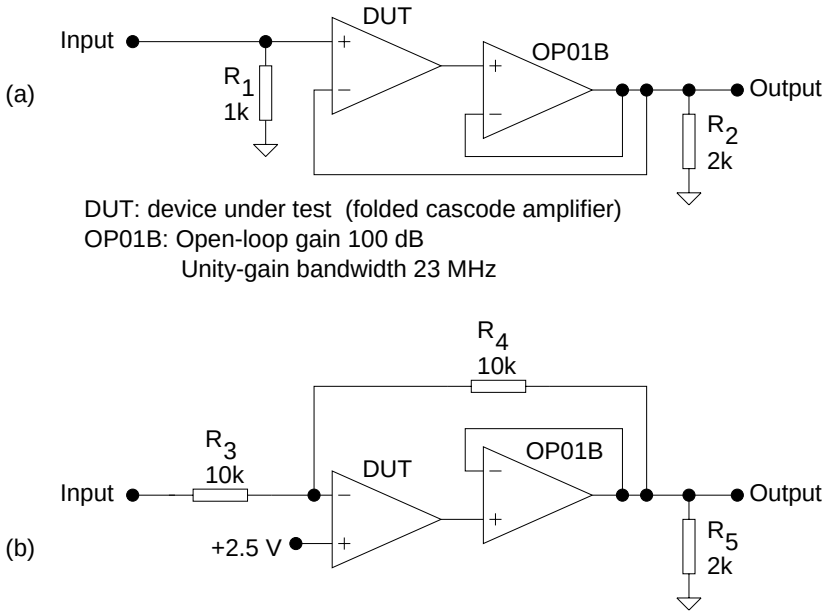

Figure 4.2: Amplifier in the (a) voltage follower and (b) inverter configuration.

at the output node together with the output capacitance C_{out},

$$p_1 = \frac{1}{2\pi r_{out} C_{out}} \tag{4.2}$$

where C_{out} consists of the load capacitance and the parasitic capacitance at the output node.

The dc operating points of the MOS transistors were determined after simulations with SPICE [43]–[46] and listed in Table 4.1. The simulation results for the reference voltages are illustrated in Table 4.2. For a +5 V power supply the power dissipation of the operational amplifier is 653 μW. With the values listed in Table 4.1 and Table 4.2, the open loop gain and the output resistance can be calculated from (4.1) and their values are 62828 (96 dB) and 503.425 MΩ, respectively. Assuming that for the simulations a 10 pF load capacitance was used, the dominant pole p_1 calculated from (4.2) is 32 Hz.

4.3 Simulation Results

The amplifier was simulated with SPICE in two different configurations in order to investigate performance parameters such as linearity, slew-rate, unity-gain bandwidth and open-loop gain. The schematics of the amplifier connected as a voltage follower and as an inverter are shown in Figure 4.2(a) and (b), respectively. As indicated, the amplifier was evaluated in closed-loop using an operational amplifier $OP01B$ [42] provided by AMS 0.8 μm technology library. This CMOS amplifier operates as a buffer and has high input impedance, low offset, high open-loop gain (100 dB) and unity-gain bandwidth of 23 MHz.

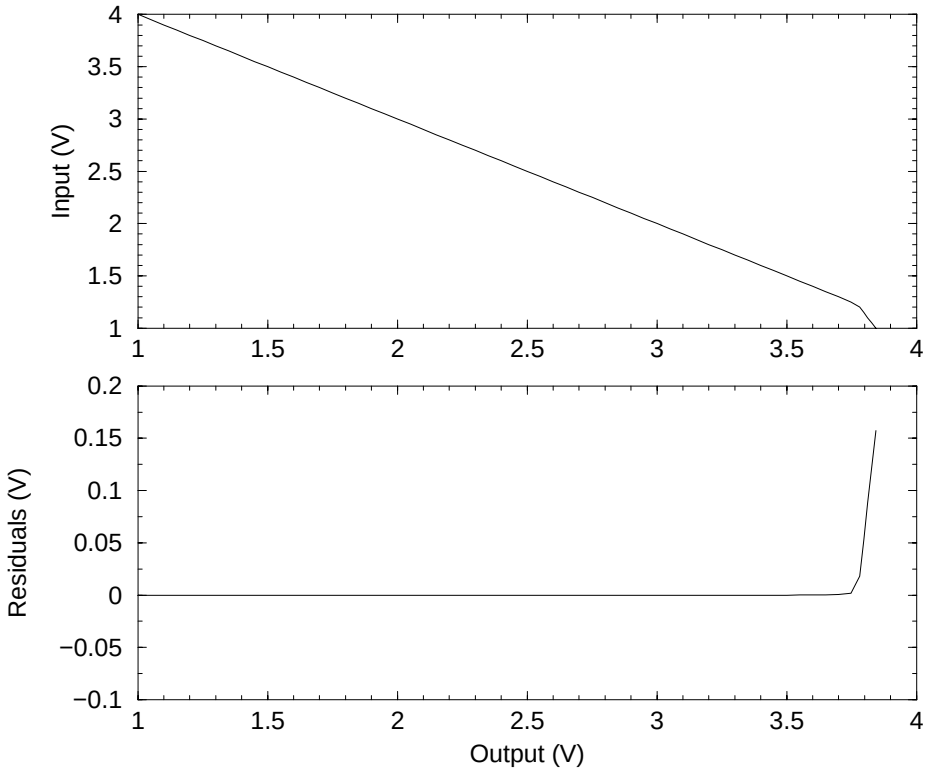

Figure 4.3: Upper: Input voltage as a function of output voltage. Lower: Residuals from a fit to a 2.5 V output voltage range. The amplifier is in the inverter configuration.

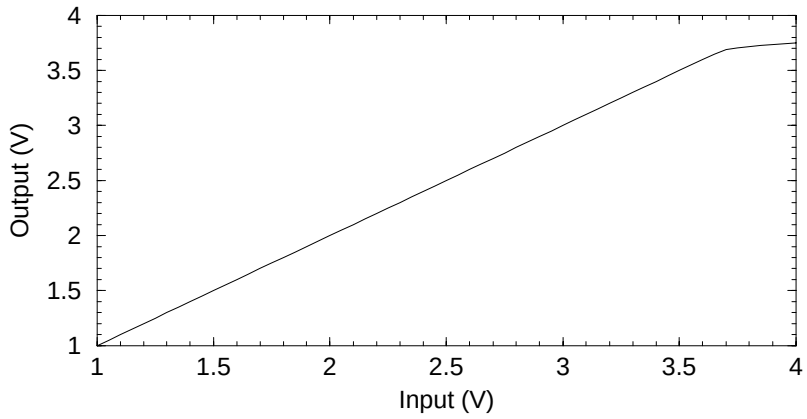

Figure 4.4: Output voltage plotted as a function of input voltage. The amplifier is in the follower configuration.

The amplifier output voltage range and its linearity were simulated with the amplifier in the inverter configuration, as illustrated in Figure 4.2(b). In Figure 4.3 the input voltage is plotted as a function of the output voltage together with the deviations from a linear fit across a 2.5 V output voltage range. The non-inverting input of the amplifier

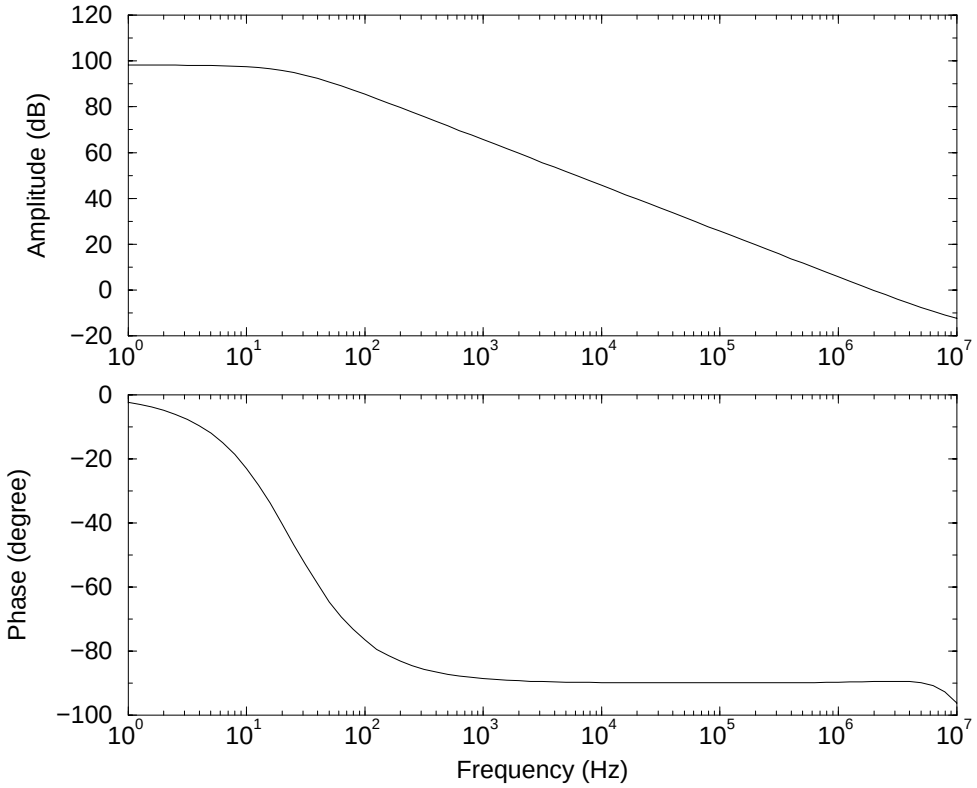

Figure 4.5: Amplitude (upper) and phase (lower) plotted as a function of frequency.

Variable	Simulation	Calculation
Open-loop gain	98 dB	96 dB
−3 dB bandwidth	25 Hz	32 Hz
Unity-gain bandwidth	1.92 MHz	–
Integral linearity	0.03 %	–
Slew-rate	3.83 V/μs	–
Phase margin	90 degree	–
Output resistance	–	503.425 MΩ
Equivalent input referred noise @ f=100 kHz	30 nV/$\sqrt{\text{Hz}}$	33 nV/$\sqrt{\text{Hz}}$

Table 4.3: Simulation and calculation results at 10 pF load capacitance.

was set to 2.5 V. The integral linearity error is the maximum deviation from a linear fit to the output voltage versus the input voltage over the full scale input voltage range, expressed as a percentage of the input voltage range. The calculated non-linearity is 0.03 % (700 μV/2.5 V) over an output voltage range of 2.5 V.

Other amplifier parameters such slew-rate and frequency dependence of the open-loop gain were determined after simulations with the amplifier in the follower configuration. In Figure 4.4 the output voltage is plotted as a function of input voltage with the amplifier in the follower configuration, as shown in Figure 4.2(a). For the simulations it

was assumed that the input transistors are identical (no mismatch), corresponding to a zero offset voltage. The slew-rate of 3.83 V/μs was calculated after simulations at 10 pF load capacitance. Figure 4.5 shows the open-loop gain and phase represented as a function of frequency. The simulations show an open-loop gain of 98 dB, a phase margin of 90 degree, a unity-gain bandwidth of 1.92 MHz and a -3 dB bandwidth of 25 Hz. For the simulations a 10 pF load capacitance was used, which approximately represents the output load capacitance in the test setups described in Appendix C and Appendix D. This capacitance accounts for the chip package and socket (68 pin CLCC), traces on the printed circuit board, and the input capacitance of the AD645 amplifier (1 pF).

The simulations and calculations agree well and are summarised in Table 4.3.

4.4 Amplifier Noise

The noise introduced by the amplifier consists of the thermal and the flicker (1/f) noise. The thermal noise is due to random thermal motion of the electron and is independent of the dc current flowing in the component. The flicker noise is associated with carrier traps in the semiconductor which capture and release carriers in a random manner. The spectral noise density for a NMOS transistor [44]–[46] can be written as

$$S_{fn}(f) = \frac{\overline{v_{thn}^2} + \overline{v_{fn}^2}}{\Delta f} = \frac{\overline{i_{thn}^2} + \overline{i_{fn}^2}}{g_{mn}^2 \Delta f} = \frac{8kT}{3g_{mn}} + \frac{K_{fn} I_{DSn}^{A_{fn}}}{g_{mn}^2 C_{ox} W_n L_n f}, \tag{4.3}$$

where g_{mn} is the transconductance of the transistor, I_{DSn} is the drain-to-source current, $k = 1.38 \times 10^{-23}$ [J/K] is the Boltzmann's constant, and K_{fn} and A_{fn} are the flicker noise coefficient and exponent, respectively. In the same manner as for a NMOS transistor, the spectral noise density for a PMOS transistor is given by

$$S_{fp}(f) = \frac{\overline{v_{thp}^2} + \overline{v_{fp}^2}}{\Delta f} = \frac{\overline{i_{thp}^2} + \overline{i_{fp}^2}}{g_{mp}^2 \Delta f} = \frac{8kT}{3g_{mp}} + \frac{K_{fp} I_{DSp}^{A_{fp}}}{g_{mp}^2 C_{ox} W_p L_p f}. \tag{4.4}$$

The first term in (4.3) or (4.4) represents the thermal noise of the transistor due to the finite resistance of the channel. The second term in (4.3) or (4.4) represents the contribution from the flicker noise.

The input referred thermal noise generated in the folded cascode amplifier is the sum of the statistically independent mean square noise currents from the transistors M_1 through M_{10}. The input referred thermal noise spectral density is then

$$\frac{\overline{v_{th}^2}}{\Delta f} = \frac{\sum_{j=1}^{10} \overline{i_{thj}^2}}{g_{m1}^2 \Delta f} = \frac{\overline{i_{th1}^2} + \overline{i_{th2}^2} + \overline{i_{th3}^2} + \overline{i_{th4}^2} + \overline{i_{th5}^2} + \overline{i_{th6}^2} + \overline{i_{th7}^2} + \overline{i_{th8}^2} + \overline{i_{th9}^2} + \overline{i_{th10}^2}}{g_{m1}^2 \Delta f}. \tag{4.5}$$

With matched transistors in each of the pairs $M_1 - M_2$, $M_3 - M_4$, $M_5 - M_6$, $M_7 - M_8$, and $M_9 - M_{10}$, the input referred thermal noise spectral density for the folded cascode amplifier can be expressed as

$$\frac{\overline{v_{th}^2}}{\Delta f} = \frac{2(\overline{i_{th1}^2} + \overline{i_{th3}^2} + \overline{i_{th5}^2} + \overline{i_{th7}^2} + \overline{i_{th9}^2})}{g_{m1}^2 \Delta f}. \tag{4.6}$$

Inserting the thermal noise terms from (4.3) and (4.4) into (4.6) yields

$$\frac{\overline{v_{th}^2}}{\Delta f} = \frac{16kT}{3g_{m1}}\left(1 + \frac{g_{m3} + g_{m5} + g_{m7} + g_{m9}}{g_{m1}}\right). \tag{4.7}$$

The spectral density of the input referred flicker noise generated in the amplifier circuit can be written as

$$\frac{\overline{v_f^2}}{\Delta f} = \frac{\sum_{j=1}^{10} \overline{i_{fj}^2}}{g_{m1}^2 \Delta f} = \frac{2(\overline{i_{f1}^2} + \overline{i_{f3}^2} + \overline{i_{f5}^2} + \overline{i_{f7}^2} + \overline{i_{f9}^2})}{g_{m1}^2 \Delta f}. \tag{4.8}$$

In the similar way as for the thermal noise, the spectral density of the input referred flicker noise can be derived and is given by

$$\frac{\overline{v_f^2}}{\Delta f} = \frac{2K_{fp}}{g_{m1}^2 f C_{ox} W_1 L_1}\left[I_{DS1}^{A_{fp}} + W_1 L_1\left(\frac{K_{fn} I_{DS3}^{A_{fn}}}{K_{fp} W_3 L_3} + \frac{K_{fn} I_{DS5}^{A_{fn}}}{K_{fp} W_5 L_5} + \frac{I_{DS7}^{A_{fp}}}{W_7 L_7} + \frac{I_{DS9}^{A_{fp}}}{W_9 L_9}\right)\right]. \tag{4.9}$$

The total spectral noise density in the operational amplifier is the sum of the spectral density of the thermal and flicker noise

$$S_{op}(f) = \frac{\overline{v^2}}{\Delta f} = \frac{\overline{v_{th}^2} + \overline{v_f^2}}{\Delta f}. \tag{4.10}$$

The W/L transistor ratios are given in Figure 4.1 while the drain-to-source currents and transconductances for M_1 through M_{10} are listed in Table 4.1. Also, noise parameters such as flicker noise coefficients and exponents of the PMOS and NMOS transistors in AMS 0.8 μm CMOS technology are listed in Table A.1 of Appendix A. For the folded cascode operational amplifier the spectral noise densities of the thermal and flicker noise at 100 kHz have been calculated from (4.7) and (4.9) and their values are 32 nV/$\sqrt{\text{Hz}}$ and 5 nV/$\sqrt{\text{Hz}}$, respectively. Therefore the total spectral noise density in the operational amplifier calculated from (4.10) is 33 nV/$\sqrt{\text{Hz}}$. The noise in the operational amplifier has been also determined after simulations with SPICE. The simulation and calculation values of the noise agree well and are given in Table 4.3.

4.5 Summary

In this chapter the folded cascode amplifier has been examined and its gain, bandwidth, and noise performance have been characterised. One of the advantage of the folded cascode amplifier is that its frequency response is dominated by the pole associated with its load capacitance. Therefore no internal compensation is needed to ensure stability. The amplifier is used in the analog memory architecture introduced in Chapter 3. The amplifier provides sufficient gain, bandwidth, and low noise compared with the noise of the analog memory.

The amplifier operates from a single +5 V power supply with a power dissipation of 653 μW. The bias circuitry that generates the reference voltages for the amplifier was included on the chips. The amplifier characteristics were simulated in both voltage follower and inverter configurations. The simulations predict an open-loop gain of 98 dB, a phase margin of 90 degree, a unity-gain bandwidth of 1.92 MHz, and a -3 dB bandwidth of 25 Hz with a 10 pF load capacitance.

Chapter 5

Control Circuits

5.1 Overview

The control circuits are necessary to provide the write and read addresses for the analog memory core. The write and read control circuits are included on-chip and described in detail in this chapter. The write control circuit was implemented to achieve 500 MHz sampling frequency and its architecture is presented in Section 5.2. The following section describes the read control circuits which operate at 100 kHz readout frequency. The write control circuit is identical for both chips while the read control circuit is different. The performance of the control circuits is also evaluated.

5.2 High Speed Addressing Circuit

5.2.1 Circuit Description

Generally, shift registers are used for write address control in analog memory circuits. At sampling rates above 150 MHz (depending of the technology) this approach is difficult to implement and therefore delay chains are used instead. Such inverter chains have been employed previously in digital applications. The high speed write control circuit proposed for the analog memory consists of four 32 cell delay chains [27, 28]. An inverter delay chain of 32 cells together with a servo feedback illustrated in Figure 5.1 were implemented to reach 500 MHz sampling frequency. Each delay element in the chain consists of five MOS transistors, as indicated by the shaded box in Figure 5.1. A write pulse applied at input $In1$ propagates through the delay elements, producing the write address signals $w < 1 >$ through $w < 32 >$ for the analog memory core. The minimum width of the write pulse $In1$ is constrained by the accuracy with which the analog signal is to be acquired and the input time constant of the sampling cell. The delay of the write pulse through the chain is set by the control voltage $Vctr1$ which determines the on resistance of the PMOS transistor M_1. The resistance together with the gate capacitance of the following inverter stage, M_4 and M_5, provide an adjustable RC time delay that governs the sampling frequency of the memory.

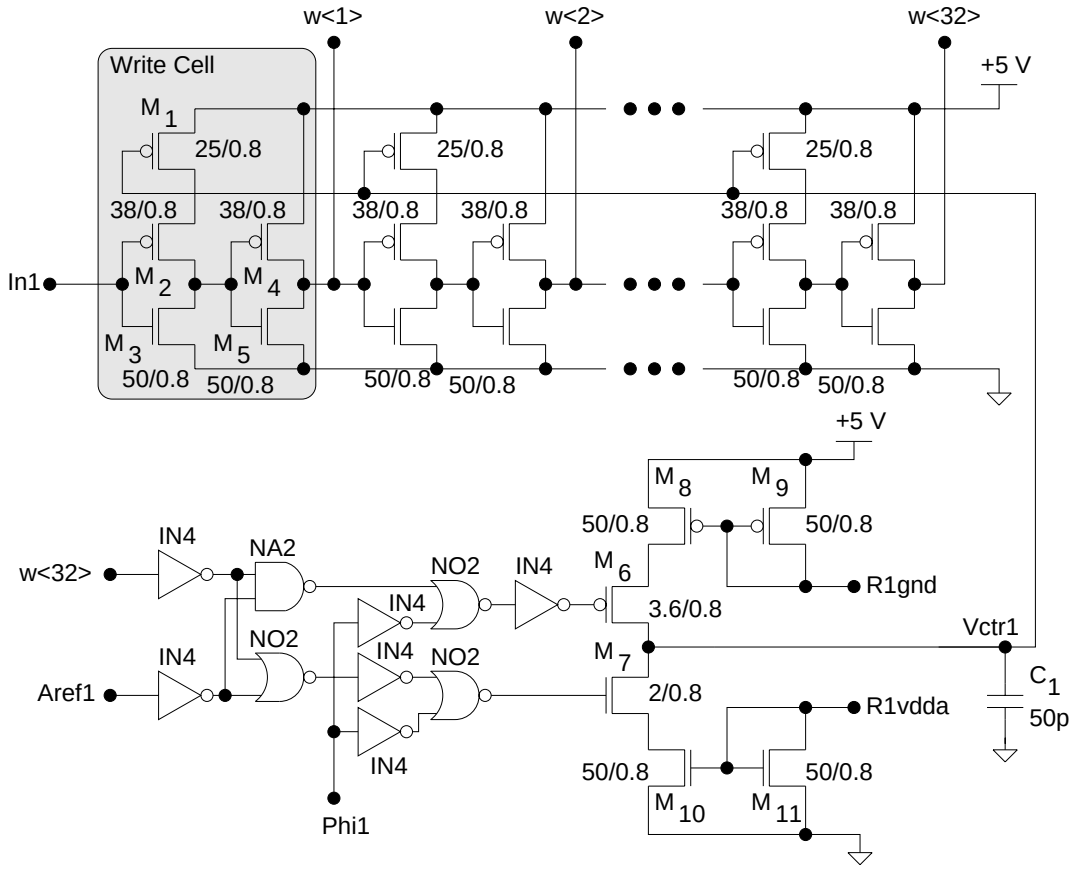

Figure 5.1: Inverter delay chain of 32 cells and servo feedback circuit.

Shown in Figure 5.2 is a timing diagram of the write signals in one delay chain. In this mode several memory cells are addressed simultaneously. It should be noted that only the timing of the falling write clock edges is controlled by the circuit shown in Figure 5.1.

In order to ensure a delay, and thus the sampling frequency, a servo feedback circuit, also shown in Figure 5.1, is used. The raising edge of a reference input signal $Aref1$ is compared to the falling edge of the last write signal $w < 32 >$. When the delay is less than the intended value, as shown in Figure 5.3(a), the transistor M_6 turns on, which connects the current generated by $M_8 - M_9$ mirror current to the capacitor C_1. The voltage across C_1 is increased, thereby slowing the inverter chain via the control voltage $Vctr1$. The signal $Phi1$ is included in such a way that the voltage across C_1 is modified only while the delays are being compared during the write phase. In the same way, as illustrated in Figure 5.3(b), when the delay is larger than the intended value, the voltage across C_1 is decreased. The time difference $t_{ref} - t_{in}$ determines the resulting write sample frequency, $f_s = 32/(t_{ref} - t_{in})$. This feedback circuit eliminates the sensitivity of the delay chain to process parameters and compensates for the effect of temperature and supply variations.

The dimensions of the transistors in the delay chain and servo feedback circuit are indicated in Figure 5.1 in microns. The control logic which enables the transistors M_6 and M_7 was implemented with digital gates provided by the standard digital gates

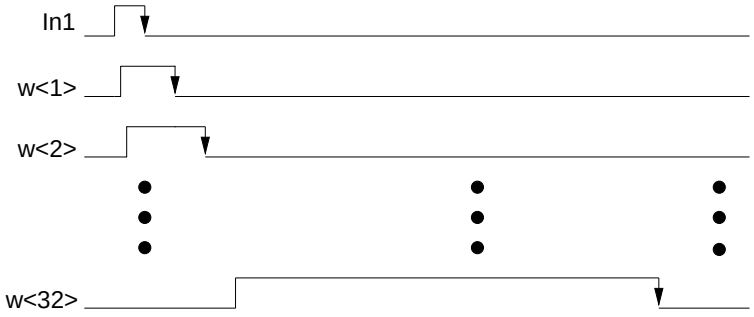

Figure 5.2: Timing diagram of the write signals in one delay chain.

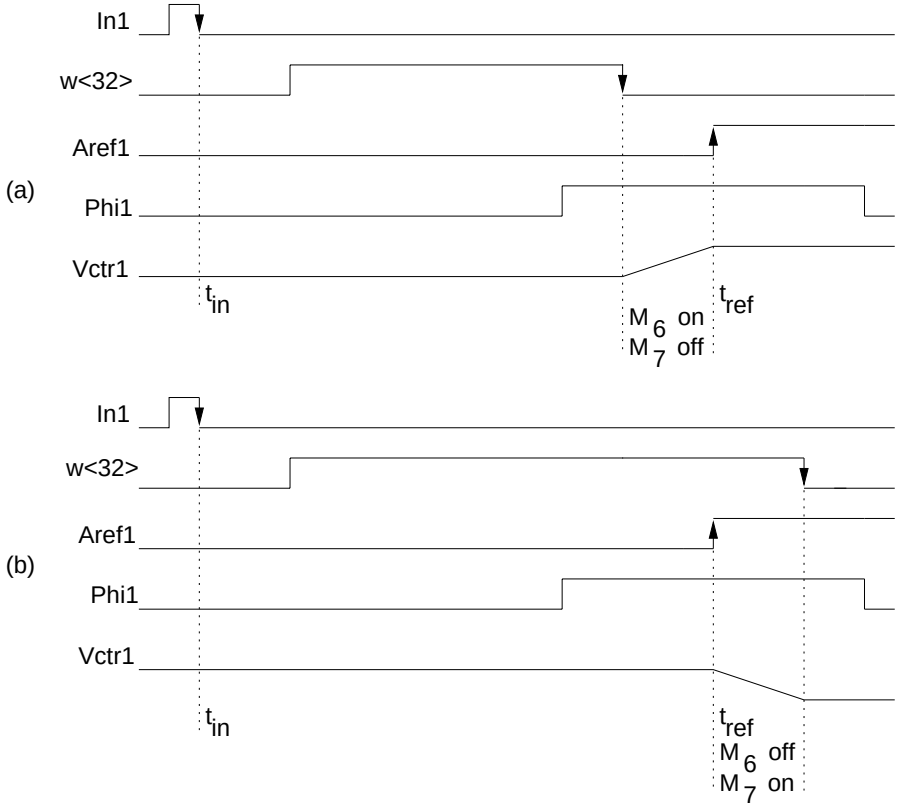

Figure 5.3: Timing diagram of the inverter chain showing the falling edge of the last write signal $w < 32 >$ which can be (a) before or (b) after the raising edge of the reference pulse $Aref1$.

library [39] of AMS 0.8 μm CMOS technology. The magnitudes of the currents for the two mirrors $M_8 - M_9$ and $M_{10} - M_{11}$ are set by external resistors through $R1gnd$ and $R1vdda$. The size of the resistors determines the speed of charge or discharge of the capacitor C_1 during the write phase.

This dynamic servo feedback delay circuit can be used only for synchronous repetitive signal acquisition. Otherwise, the discharge of C_1 by leakage currents will introduce timing errors.

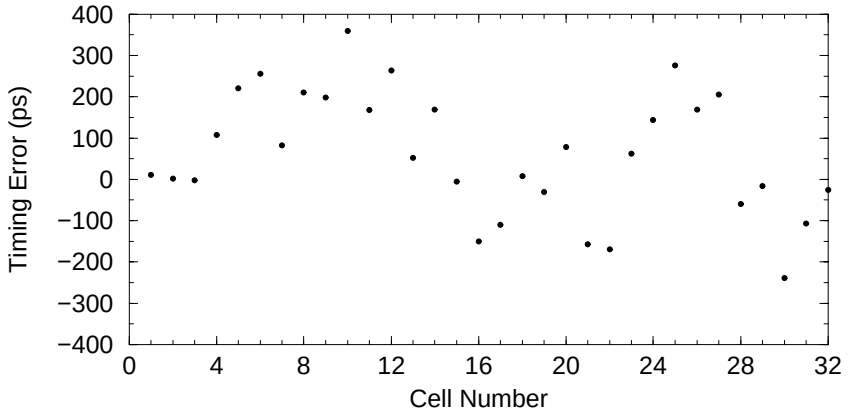

Figure 5.4: Timing errors after simulations in one delay chain.

5.2.2 Timing Accuracy

The timing accuracy within a signal channel is affected by delay variations among cells. The deviations from the nominal delay arise from inaccuracies in the fabrication process and are thus constant over time. The individual delay values shown in Figure 5.4 have been determined after simulations with SPICE [43]–[46] by applying a sine waveform to the input of the signal channel and fitting the output response to an ideal sine curve. It results a rms value of 160 ps for the element delay variation across 32 cells. This jitter corresponds to a sampling frequency error of 8 % at the 500 MHz sampling rate. It should be noted that the jitter is independent of the input signal level and can be corrected for if required.

The total delay of the inverter chain is regulated by the feedback control circuit. Inaccuracies in this circuit manifest themselves as variations of the control voltage level $Vctr1$, and thus in a variation in the delay of the entire inverter chain. As a consequence, the sampling frequency may vary from one measurement cycle to the next.

It should be again noted that in the proposed analog memory design the turn off time of the sampling switches is independent of the input signal level, eliminating a timing error that would otherwise be present for high frequency input signals.

5.3 Read Addressing Circuits

5.3.1 Read Control Circuit for FASTSAMP-EV chip

The read control circuit for FASTSAMP-EV chip consists of four 32 stage dynamic two-phase shift registers. Figure 5.5 illustrates one of the 32 stage dynamic two-phase shift register [26] configurations with the timing diagram. In this figure, $Phis1$ and $Phis2$ are the two non-overlapping clocks controlling the shift register, and $Phirin1$ is the serial input to the register. The schematic of the two-phase clock generator which provides the non-overlapping clocks is shown in Figure 5.6. The non-overlapping characteristic of the

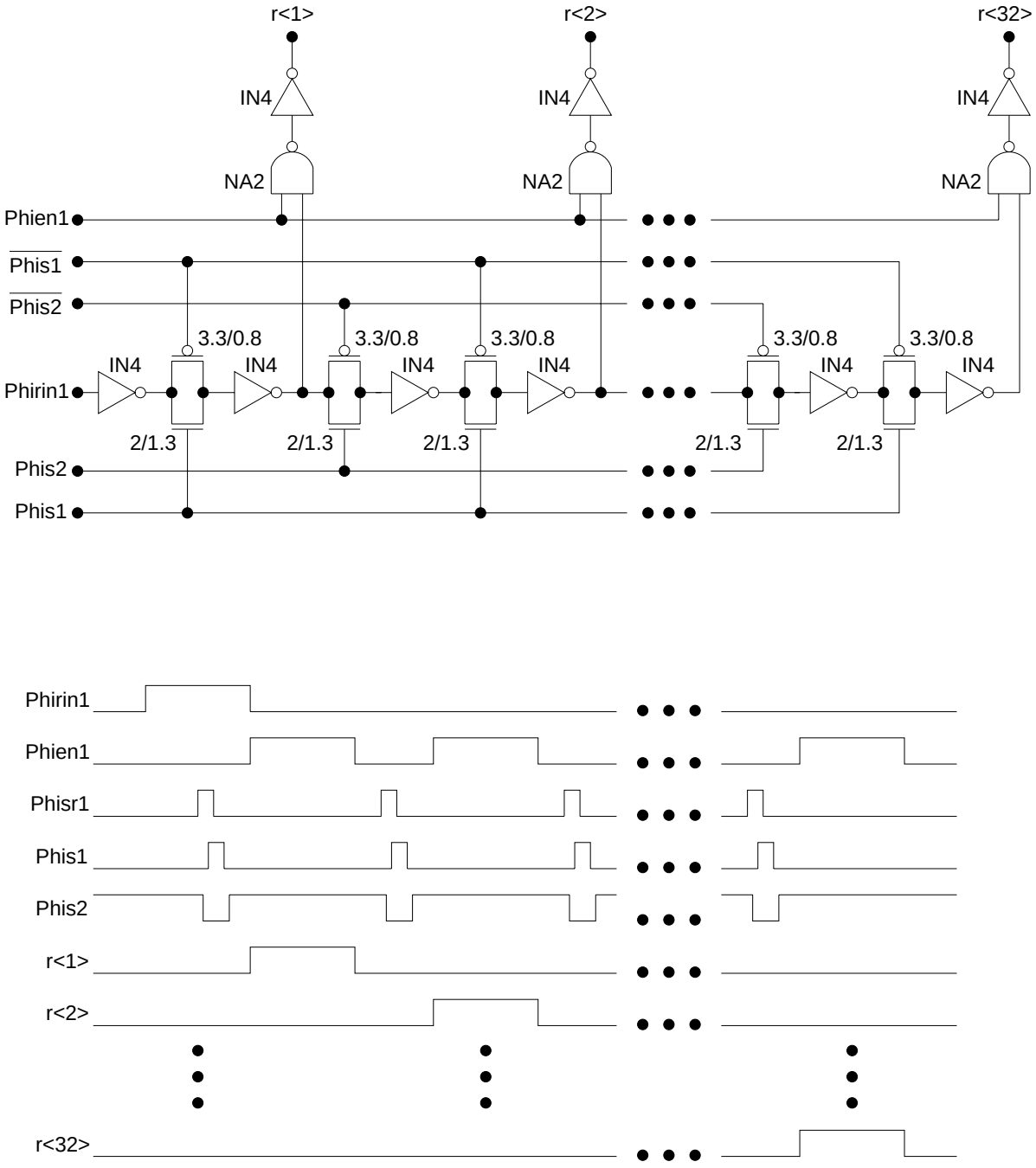

Figure 5.5: A 32 stage dynamic two-phase shift register with timing diagram.

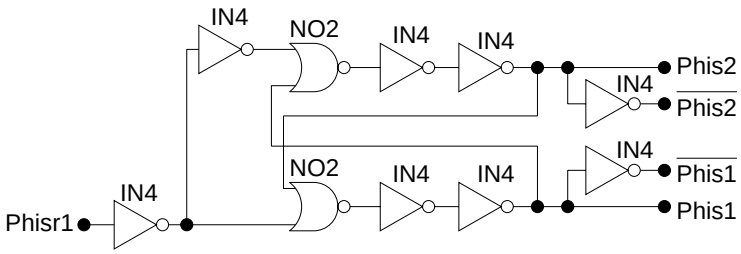

Figure 5.6: Two-phase clock generator.

resulting shift register clocks, $Phis1$ and $Phis2$, is ensured by the delays of the extra inverters. The signals $r < 1 >$ through $r < 32 >$ are the read address control signals for the analog memory core. The enable signal $Phien1$ is used to disable the read addresses, $r < 1 >$ through $r < 32 >$, while the analog memory is reset between readout of two successive memory cells, as shown in Figure 3.4(b).

The shift register is initialised by raising both of the clocks, $Phis1$ and $Phis2$, and the serial input $Phirin1$ low, as shown in Figure 5.5. This sets the read address signals $r < 1 >$ through $r < 32 >$ to their low state. The shift register proceeds as follows. The serial input $Phirin1$ is set to high, and with a raising edge of clock $Phis1$, the first read address $r < 1 >$ becomes high. After clock $Phis1$ is returned to low, a $Phis2$ pulse advances the logic level of $Phirin1$ to the second inverter in the register. The serial input $Phirin1$ is then raised to the low state and, after another $Phis1$ pulse, the first address signal, $r < 1 >$, goes low, while the second address signal, $r < 2 >$, goes high. Consecutive clock pairs, $Phis1$ and $Phis2$, advance the logic levels within the shift register until the last read address control signal, $r < 32 >$, rises and falls, as illustrated in Figure 5.5. It is important to note that the shortest period of the non-overlapping shift register clocks must stay high is determined by the time required to adequately charge or discharge the inverter input gate capacitances through the pass transmission gates. The minimum time between two successive write clocks is therefore simply the sum of two inverter delays plus the timing overhead required to ensure that the shift registers clocks are non-overlapping.

The transistor dimensions for the transmission gates used as switches in Figure 5.5 are given in microns. To calculate the drawn dimensions of the PMOS and NMOS transistors, the relations (2.43) and (2.44) were used. Also, the inverters and the gates are provided by the standard digital gates library in AMS 0.8 μm CMOS technology.

5.3.2 Read Control Circuit for FASTSAMP-V1 chip

The readout of the FASTSAMP-V1 chip is controlled by an on-chip 1 of 128 decoder [28] shown in Figure 5.7. The decision to replace the four 32 stage dynamic two-phase shift registers by a 1 of 128 decoder was taken to approach more to the camera electronics requirements of the Cherenkov telescope. The schematic of the read control circuit consists of 1 of 4 decoders and 1 of 8 decoders. Both types of decoders with the schematics represented in Figure 5.8 were implemented with digital gates using the standard digital gates library of AMS 0.8 μm CMOS technology. A microcontroller which exists in the

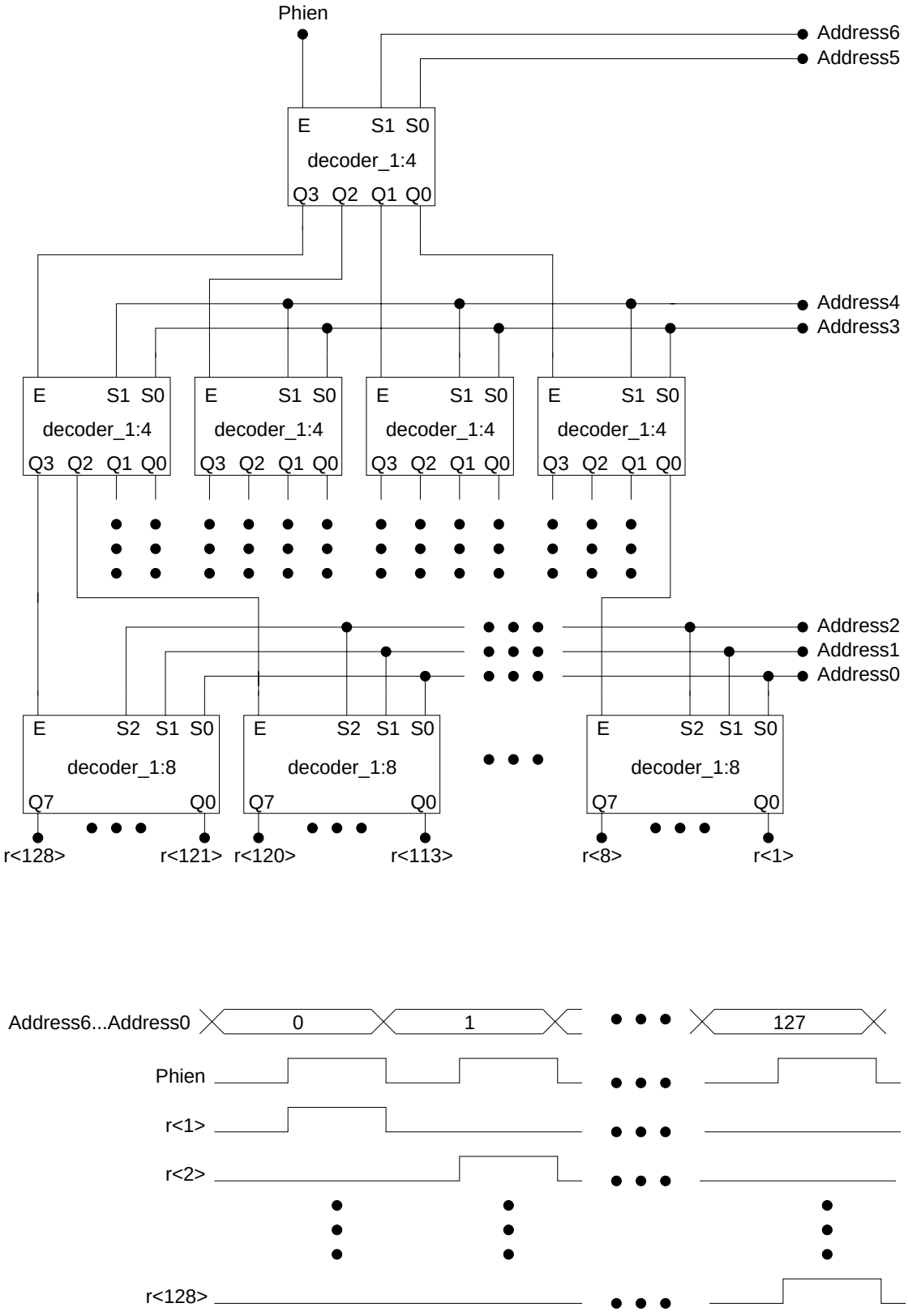

Figure 5.7: Read control circuitry with timing diagram.

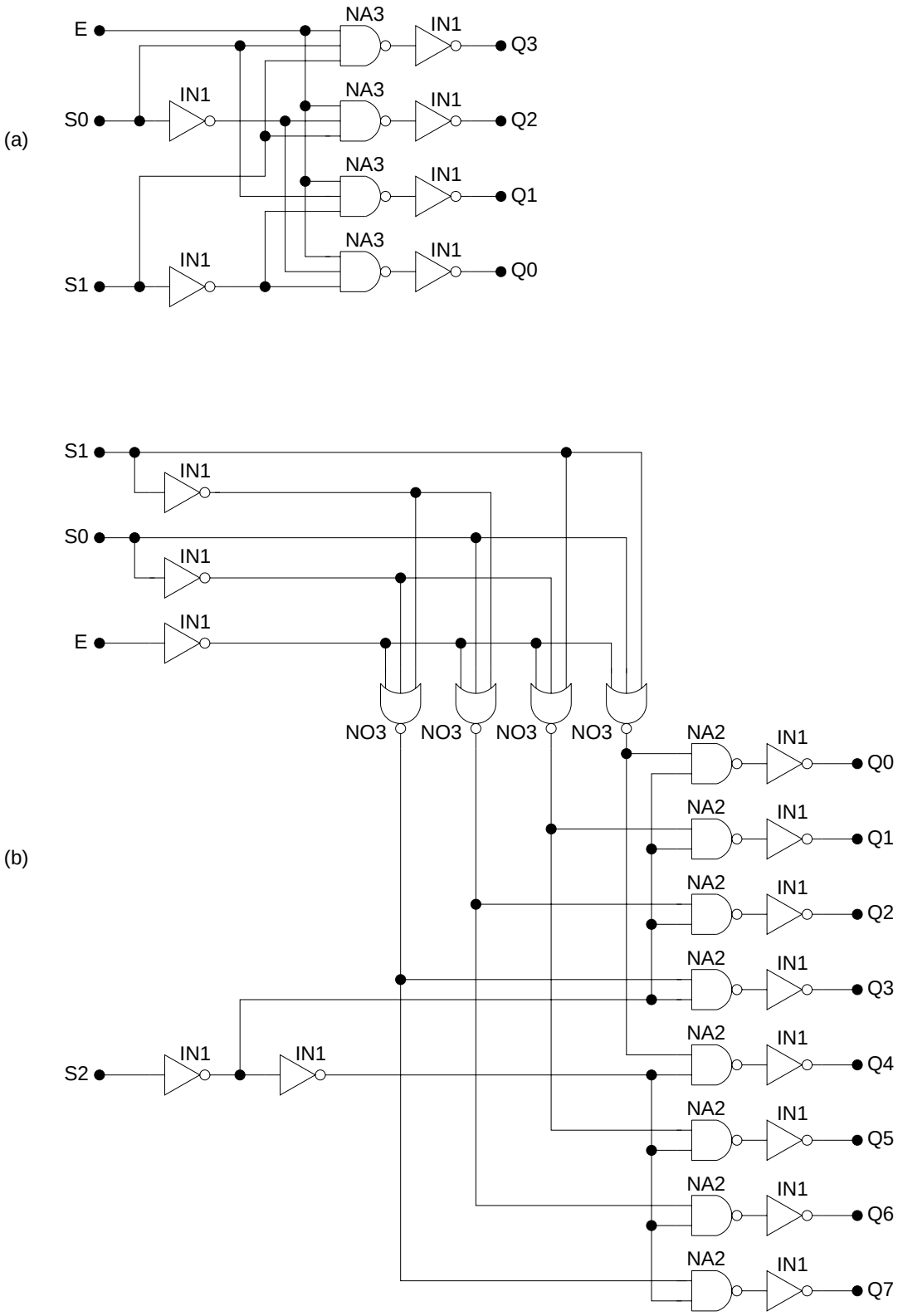

Figure 5.8: Schematics of the (a) 1 of 4 decoder and (b) 1 of 8 decoder.

camera electronics design of the Cherenkov telescope [1] provides 7 bit address signals *Address*0 through *Address*6, as illustrated in Figure 5.7. The signal *Phien* activates the decoders and thus enables the read signals $r < 1 >$ through $r < 128 >$. For the Cherenkov application is necessary to read out only a few samples depending of the analog input waveform. This decision is given by the microcontroller which provides the start and stop addresses through the address signals *Address*0 to *Address*6.

5.4 Summary

Commonly shift registers are used for write addressing in an analog memory. At high sampling speeds, the variations in cell-to-cell sampling times due to the sensitivity of on-chip delays are considerable, and extensive ac timing correction procedures are required. In addition, a high speed sampling clock must be provided to the circuit. This chapter proposed the use of inverter delay chains for write control circuit, which avoid the need for a high speed external clock. This write control circuit is insensitive to variations in the fabrication process, temperature and supply levels because servo feedback circuits are used to adjust the sampling rate. The sampling clock period is derived by a division of time delay between two external control signal edges by the number of sampling cells in one delay chain. The variations in cell-to-cell sampling times were estimated to be after simulations 160 ps rms which corresponds to a sampling frequency error of 8 % at the 500 MHz sampling rate. This jitter is independent of the input signal level and can be corrected.

The read control circuit was implemented with dynamic two-phase shift registers or with a 1 of 128 decoder depending of the chip version.

Chapter 6

Memory Calibration and Correction Procedures

6.1 Introduction

It is essential to have in analog memory an uniform response in a large number of memory cells according with the accuracy of the technology. The parameters which characterise an analog memory are cell-to-cell offset and gain variations within a memory channel. In high precision applications the cell non-uniformities may not be adequate and must therefore be cancelled by correcting the data. Dc correction procedures and ac calibration [26] may be required if the memory does not satisfy the performance objectives. The calibration and correction procedures are needed to eliminate variations of the cell offsets, gains and nonlinearities. In large systems is necessary to reduce the computational effort and the number of components required to store the correction constants.

The voltage V_{oi} read out from a given memory cell i can be expressed as a function of the input voltage V_{in},

$$V_{oi} = H_i V_{in}, \tag{6.1}$$

where H_i is referred to as the transfer function of memory cell i. Ideally, the transfer function of all cells are identical and equal to one but in reality will not because of gain, nonlinearity, and offset variations among cells. The origin of these variations can be inaccuracies in the fabrication process and control signal feedthrough while the circuit is being operated.

In large systems is necessary to reduce the computational effort and the number of components required to store the correction constants. The calibration is performed by applying known sets of signals at the analog input and storing the resulting output values. The transfer function H_i is then calculated, and the inverse function of H_i is used to correct the acquired data. The cell correction values are expressed in the form of calibration constants. The time needed to determine these constants during the calibration procedure is generally not crucial and the correction can be done on-line. The goal is to minimise the number of calibration constants and the time required to correct the signal data.

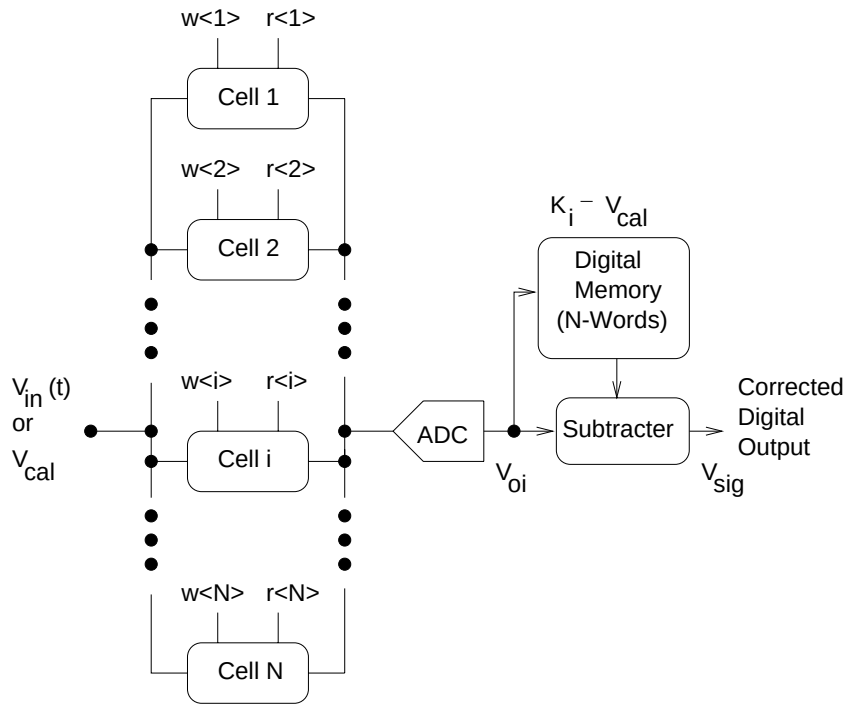

Figure 6.1: Dc correction procedure using a subtraction method.

6.2 DC Calibration

Three dc correction procedures such as subtraction, multiplication and addition, and piece-wise linear approximation are presented in the following subsections. Each procedure is described in detail.

6.2.1 Subtraction Method

A subtraction procedure can be implemented with a digital circuit as illustrated in Figure 6.1. The correction steps for cell i are the following.

During calibration, the reference calibration voltage V_{cal} is applied at the input and the digitised output voltage levels are transferred into the digital memory. The known reference voltage V_{cal} is identical for the entire acquisition system. The corresponding output voltage of cell i, V_{oci}, is

$$V_{oci} = V_{cal} + V_{offi} = K_i, \tag{6.2}$$

where V_{offi} is the memory cell offset voltage and K_i is the calibration constant to be stored for cell i.

During data acquisition, the input signal voltage V_{sig} is applied and the corresponding output voltage V_{oi} of cell i is

$$V_{oi} = V_{sig} + V_{offi}. \tag{6.3}$$

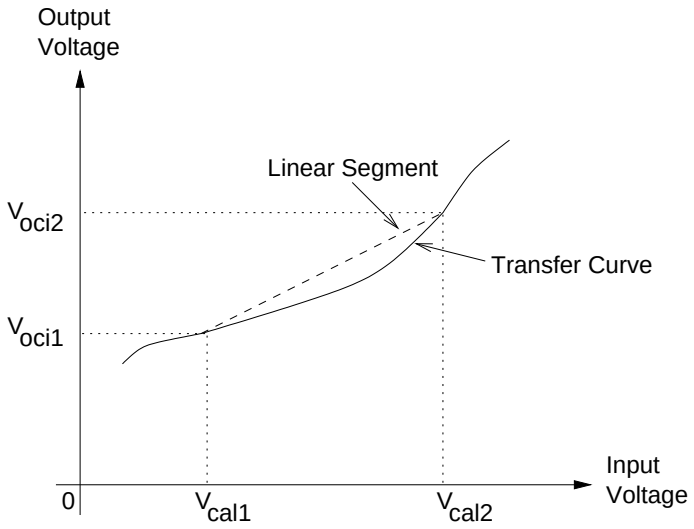

Figure 6.2: Dc correction procedure using a multiplication and addition method.

The input voltage V_{sig} can be determined by subtracting $(K_i - V_{cal})$ from the output response V_{oi},

$$V_{sig} = V_{oi} - V_{offi} = V_{oi} - (K_i - V_{cal}). \tag{6.4}$$

The subtraction is done by a digital subtracter in Figure 6.1.

If the analog memory has N cells then N constants need to be stored. It should be noted that the subtraction method corrects the offset voltage errors for dc input signals.

6.2.2 Multiplication and Addition Method

The multiplication and addition method requires two reference voltages, as illustrated in Figure 6.2. The circuit response to the reference voltages is

$$V_{oci1} = A_i V_{cal1} + V_{offi} \tag{6.5}$$

and

$$V_{oci2} = A_i V_{cal2} + V_{offi}, \tag{6.6}$$

where A_i is the voltage gain of cell i, V_{oci1} and V_{oci2} are the responses of the circuit to reference voltages V_{cal1} and V_{cal2}, respectively. When the input voltage V_{sig} is applied, the corresponding output voltage V_{oi} is

$$V_{oi} = A_i V_{sig} + V_{offi}. \tag{6.7}$$

Therefore the input voltage V_{sig} can be determined,

$$V_{sig} = K_{1i} V_{oi} + K_{2i}, \tag{6.8}$$

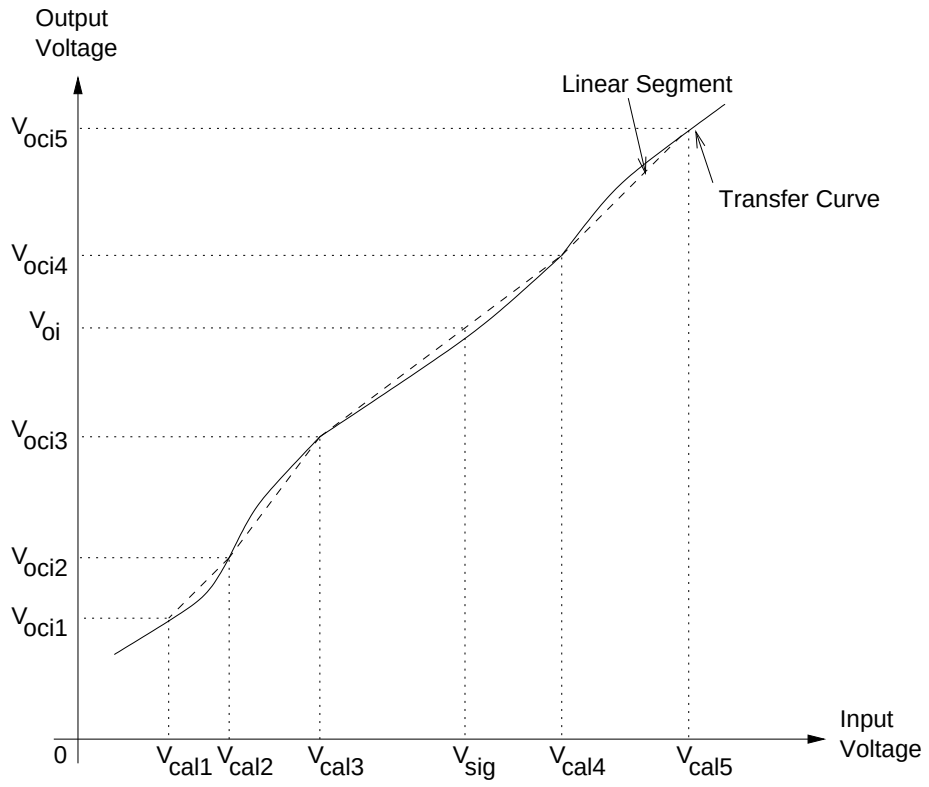

Figure 6.3: Dc correction procedure using a piece-wise linear approximation method.

where K_{1i} and K_{2i} are two calibration constants for each cell. These calibration constants are derived from (6.5) through (6.7) and written as follows

$$K_{1i} = \frac{1}{A_i} = \frac{V_{cal2} - V_{cal1}}{V_{oci2} - V_{oci1}} \tag{6.9}$$

$$K_{2i} = -\frac{V_{offi}}{A_i} = V_{cal1} - K_{1i}V_{oci1}. \tag{6.10}$$

An analog memory channel with N cells requires $2N$ constants need to be stored. The number of constants required can be reduced when the gain matching among cells is satisfactory. The input signal V_{sig} can be expressed

$$V_{sig} = K_1 V_{oi} + K_{2i} \tag{6.11}$$

and only $(N + 1)$ constants need to be stored. The multiplication and addition method corrects both cell-to-cell gain and offset voltage errors for dc input signals.

6.2.3 Piece-Wise Linear Approximation Method

The nonlinearities in the circuit response can be corrected using a piece-wise linear approximation method. The number of calibration voltage levels is determined by the number

Non-Ideal Parameter	Correction Procedure	Number of Calibration Voltage Levels	Number of Constants per Memory Cell
Offset	Subtraction	1	1
Gain and Offset	Multiplication and Addition	2	2
Linearity	Piece-Wise Linear Approximation	Number of Segments + 1	2 × Number of Segments

Table 6.1: Calibration and correction parameters.

of linear segments needed to obtain the desired accuracy, as shown in Figure 6.3. In this figure a nonlinear transfer curve is approximated by four linear segments. The five calibration voltages are V_{cal1} through V_{cal5}, and the corresponding memory responses are V_{oci1} through V_{oci5}. During data acquisition, the input signal voltage V_{sig} can be approximated from the measured output voltage V_{oi} by a linear interpolation between the nearest calibration output values.

The procedures listed in Table 6.1 are sufficient to cancel cell offset, gain and nonlinearity errors for dc input signals. In table are listed the operations that must be performed to correct offset, gain, and linearity errors, with the number of reference voltage levels and constants needed for these operations.

6.3 AC Calibration

A variation in the sampling time interval from cell to cell generates an amplitude error, as is illustrated in Figure 6.4. In this example, a ramp input signal is sampled at four distinct times, t_1 through t_4, on the falling edges of write signals $w<1>$ through $w<4>$ and stored in four consecutive analog memory cells. The time t_2' is the nominal sample time and t_2 is the actual sample time when the second sample is stored. A deviation $\Delta t_2 = t_2 - t_2'$ results in an amplitude error

$$\Delta V_{o2} = \frac{dV_{in}}{dt}\Delta t_2, \tag{6.12}$$

where dV_{in}/dt is the slope of the input voltage signal. Typical values for deviations Δt_i in one delay chain of 32 cells are shown in Figure 5.4.

It should be noted that the time deviations Δt_i are stable and independent of the input signal level. The sample time t_i associated with a given memory cell location i is simply adjusted by a correction factor Δt_i that is obtained from a single ac input waveform during calibration. These correction factors can be determined from a ramp or sine wave input signal and are applicable to all input signal shapes and frequencies.

The high frequency input signals generate timing errors, as was investigated in Chapter 2. Complex ac calibration and dc correction procedures may be required if the memory does not satisfy the performance objectives.

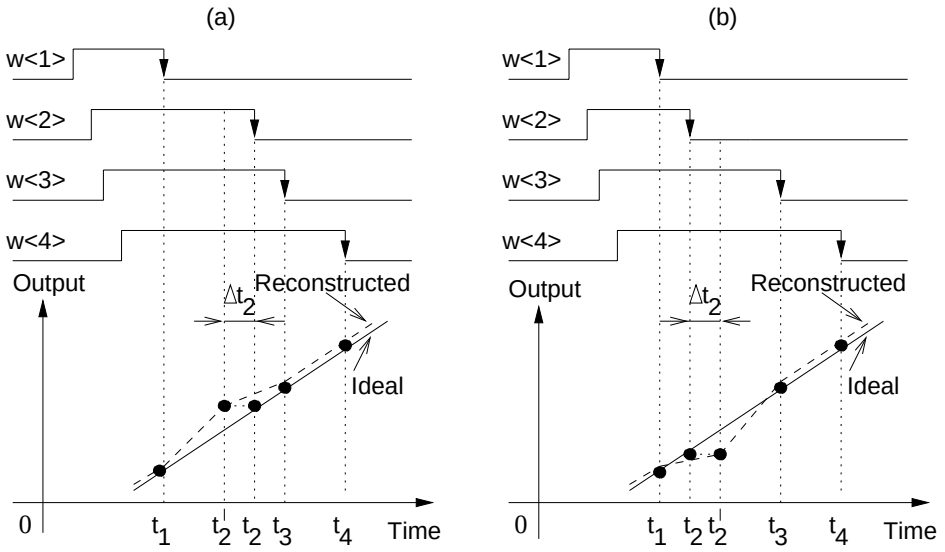

Figure 6.4: Effect of sample time error on the reconstructed output of four write signals showing the actual sample time of the write signal $w < 2 >$ which can be (a) after or (b) before the nominal sample time.

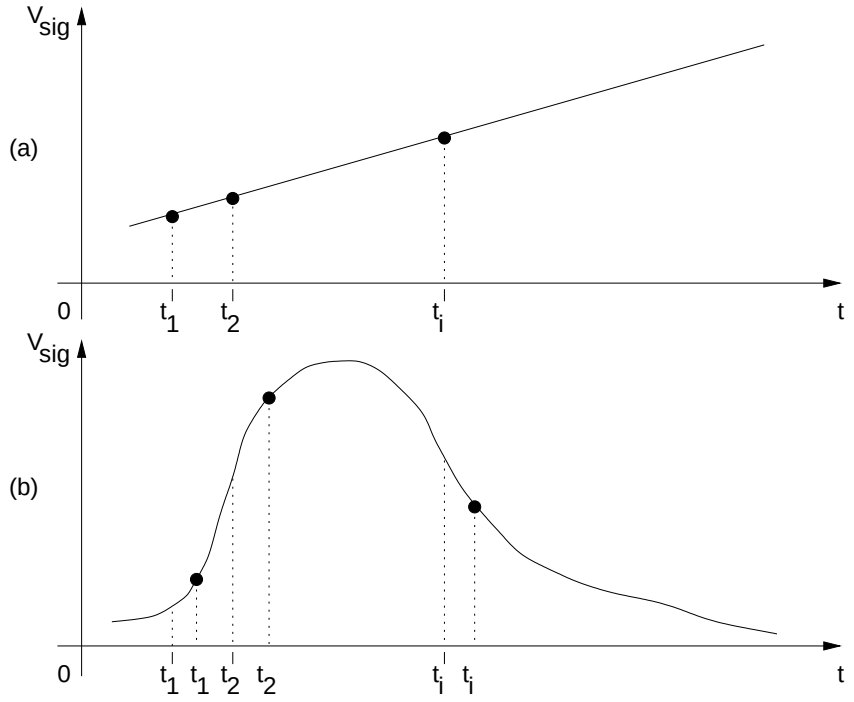

Figure 6.5: Input signal as (a) ramp wave or (b) signal from Cherenkov telescope.

6.4 Method to Calibrate Signals from Cherenkov Telescopes

The signals provided by Cherenkov telescopes are short pulses and is necessary mixed calibration (dc and ac calibration). The correction steps for cell i are the following:

- A dc calibration using multiplication and addition method or piece-wise linear approximation method should be performed.
- After dc calibration, a ramp wave input signal is applied, as illustrated in Figure 6.5(a). The slope dV_{sig}/dt, the nominal sample time t_i', and the amplitude error ΔV_{oi} can be easily determined. It is known that

$$\Delta t_i = t_i - t_i' \tag{6.13}$$

and

$$\Delta V_{oi} = \frac{dV_{sig}}{dt}\Delta t_i. \tag{6.14}$$

Therefore the actual sample time t_i can be calculated from (6.13) and (6.14)

$$t_i = t_i' + \frac{\Delta V_{oi}}{\frac{dV_{sig}}{dt}}. \tag{6.15}$$

- At the input of the analog memory is applied a Cherenkov pulse. The signal must be reconstructed on t_i, as illustrated in Figure 6.5(b).

6.5 Summary

The challenge in analog memory design is to produce an uniform and linear response in a large number of memory cells. Principal issues are cell-to-cell offset and gain variations within a memory channel, which are governed by the circuit architecture and its sensitivity to the matching properties of its constituent components.

The performance of an analog memory and the desired accuracy determine the complexity of the inverse function of H_i, and therefore the number of calibration voltage levels to be applied during calibration. The cancellation of memory cell offset voltages requires a subtraction procedure with one calibration constant for each cell. The multiplication and addition method corrects both cell-to-cell gain and offset voltage errors and requires two reference voltages while the nonlinearities are corrected by piece-wise linear approximation method. Complex ac calibration and data correction procedures are required to calibrate signals from Cherenkov telescopes.

Chapter 7

Simulation and Experimental Results

7.1 Overview

In this chapter the simulation and experimental results for two devices are presented. Section 7.2 describes the layouts of the chips together with some design optimisations. The results after ideal and parasitic simulations with a common simulation setup are reported in Section 7.3. The noise performance of the analog memories is limited by the noise in amplifiers, as will be shown in Section 7.4. The test setups used to measure the performance of the experimental circuits are described in Appendix C and Appendix D, and the results from these measurements are reported in Section 7.5. The output responses of the two versions to dc inputs are different. A significant improvement in dc response has been reached for FASTSAMP-V1 device compared with FASTSAMP-EV device.

7.2 Chips Layout

Two chips FASTSAMP-EV and FASTSAMP-V1 were designed [47, 48] at the Heidelberg ASIC laboratory in the Austria Microsystems (AMS) 0.8 μm CMOS technology [41] with poly-to-poly capacitors. The prototypes were produced by Nordic VLSI ASA company in Norway. The first chip designed was FASTSAMP-EV followed by FASTSAMP-V1. Figure 7.1 and Figure 7.2 show the layout views of the FASTSAMP-EV and FASTSAMP-V1, respectively. The layouts measure 3.26 mm $\times$ 3.37 mm and 3.26 mm $\times$ 3.39 mm, respectively. The layouts of the chips are approximatively the same with minor changes. The reason is that the write control circuit and the analog memory core are identically for both chips while the read control circuit is different. The circuits have been carefully laid out to minimise the parasitic capacitances and coupling between the control and signal traces. The large input transistors are seen on the left and the amplifiers appear on the right of the analog memory channels. The feedback delay control circuits are located near to the operational amplifiers. The power supply is uniform distributed and separated into analog ($Analog1vdda$ through $Analog4vdda$) and digital ($Digital1vdd$ through $Digital4vdd$). The corresponding grounds are identified by $Analog1gnd$ through $Analog4gnd$ and $Digital1gnd$ through

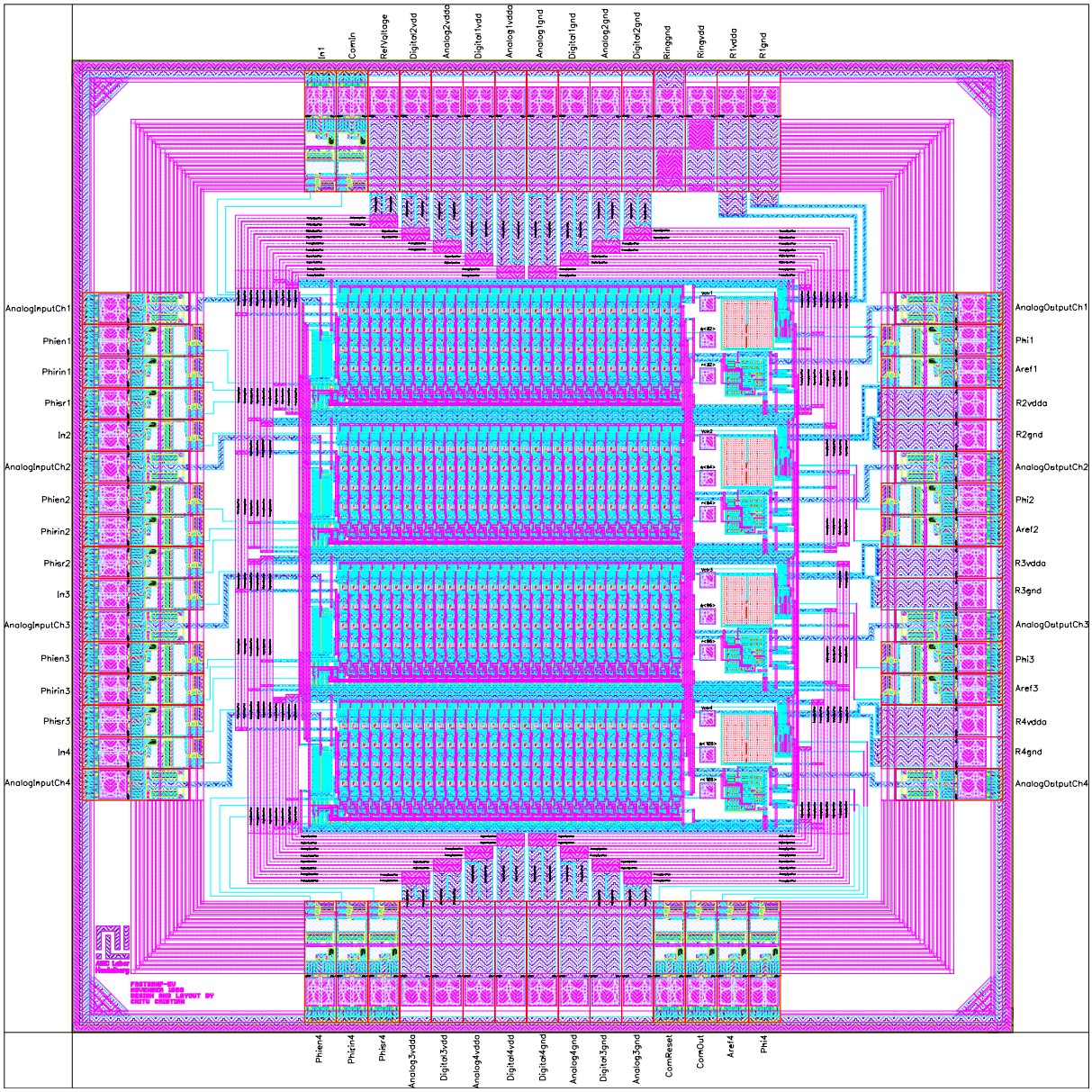

Figure 7.1: Layout view (3.26 mm × 3.37 mm) of the FASTSAMP-EV chip.

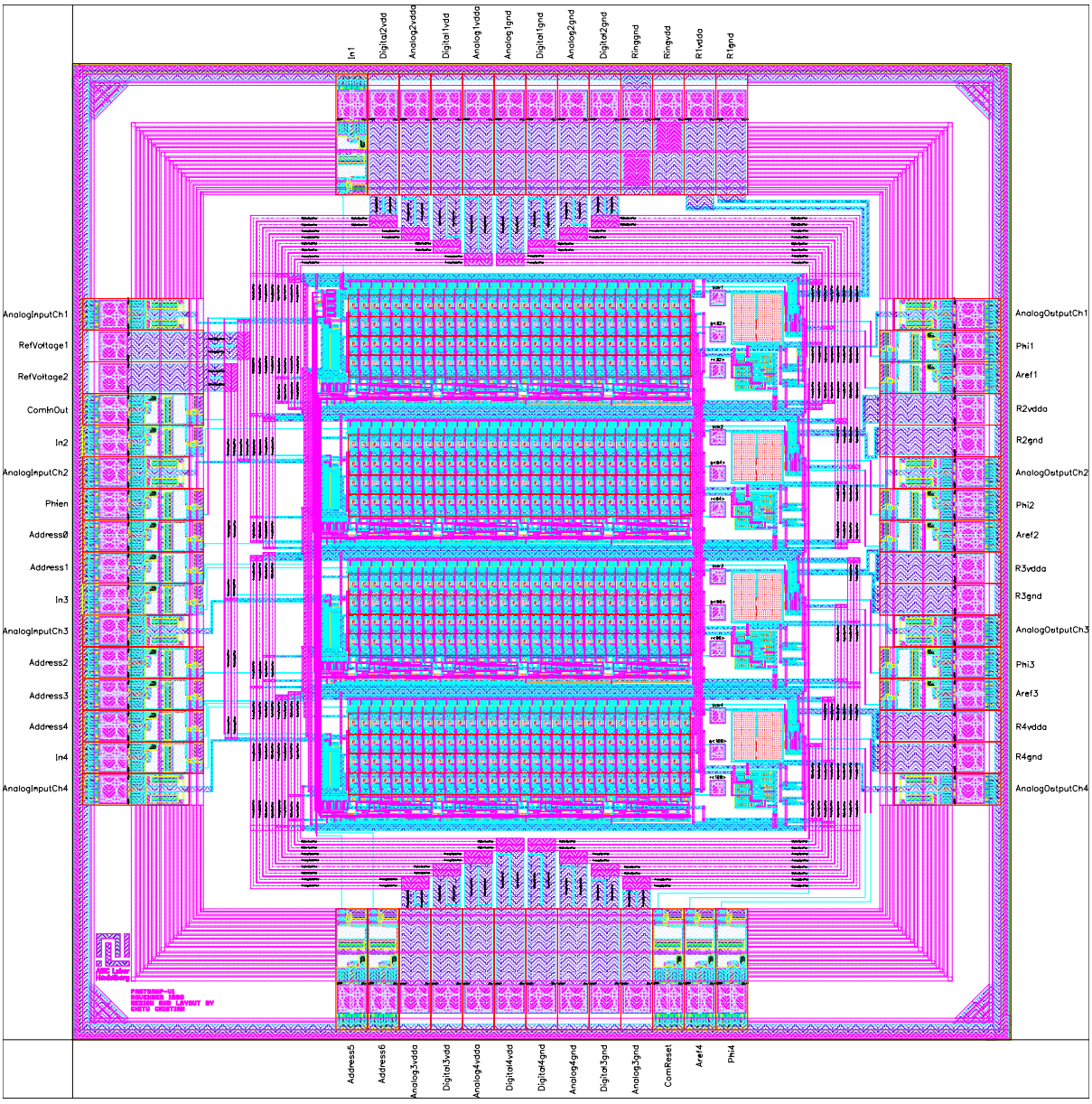

Figure 7.2: Layout view (3.26 mm × 3.39 mm) of the FASTSAMP-V1 chip.

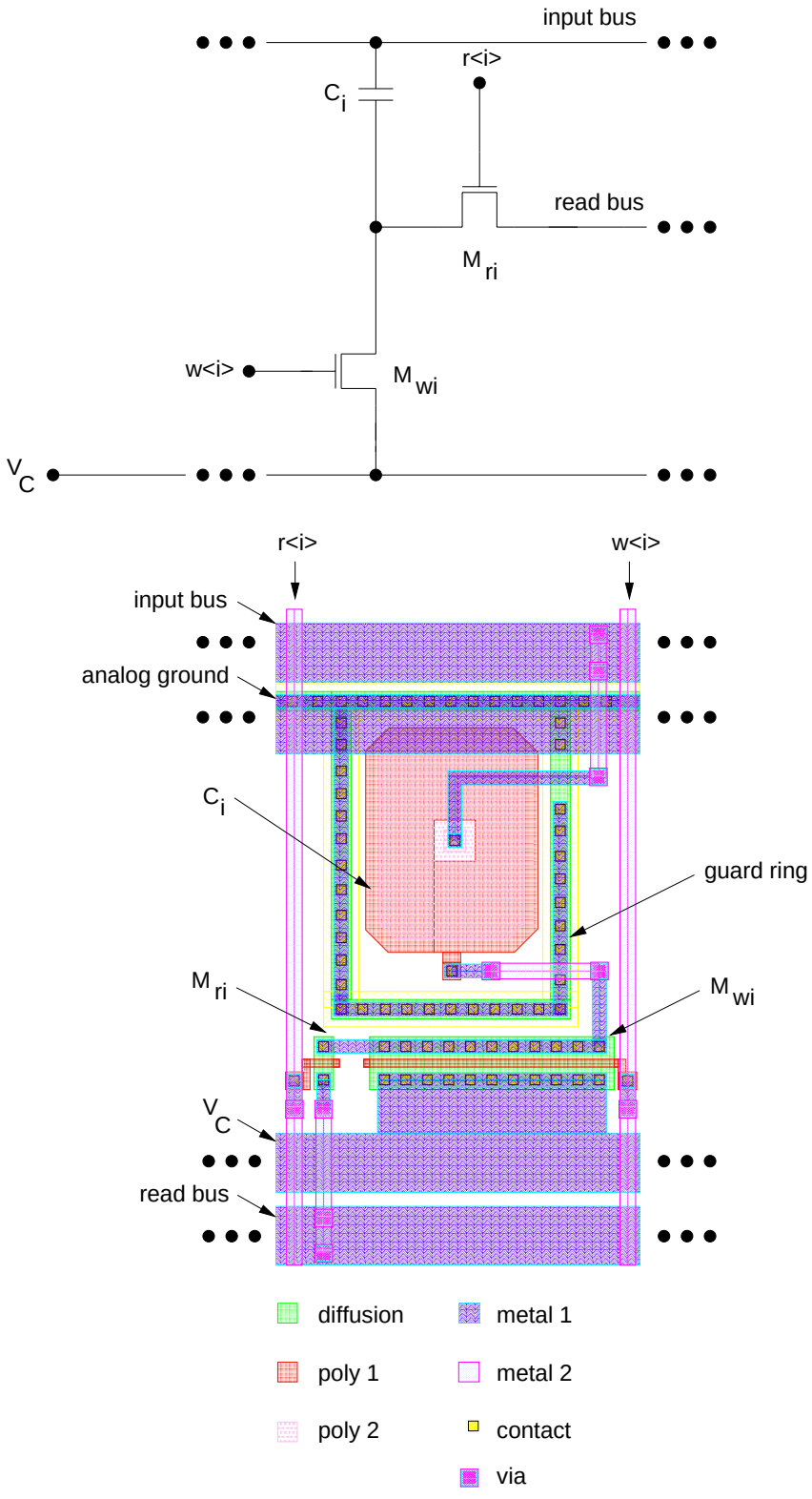

Figure 7.3: Schematic (upper) and layout (lower) of an analog memory cell.

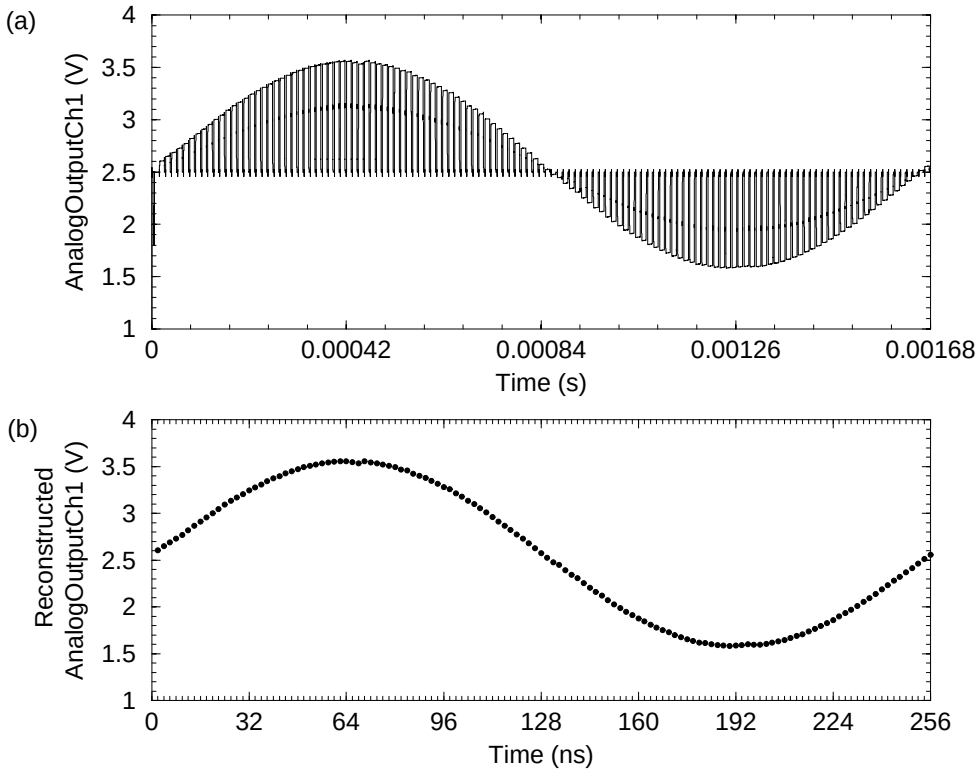

Figure 7.4: Response after simulations of one channel to a 2 V peak-to-peak, 3.906250 MHz sine wave sampled at 500 MHz. The pulse is plotted on the (a) read and the (b) write time scale.

*Digital*4*gnd*, respectively. The delay chains, feedback delay control circuits, amplifiers are connected to the analog power supply while the switches and read control circuits to the digital power supply. All analog and digital pads are protected electrostatically to avoid discharge and destruction of the chips. *Ringvdd* and *Ringgnd* are the power supply connections to all digital and analog pads around the chips.

The layout of each chip is divided on four blocks of 32 cells. Each block consists of an inverter delay chain, an analog memory and a read control circuit. One block of 32 cells is connected to an analog power supply *Analog*k*vdda* and to a digital power supply *Digital*k*vdd*, where $1 \leq k \leq 4$.

The schematic and layout of an analog memory cell are shown in Figure 7.3. As was mentioned in Chapter 3, an analog memory cell consists of a write transistor M_{wi}, a read transistor M_{ri}, and a sampling capacitor C_i. The layout area occupied by one analog memory cell is 37 μm $\times$ 66 μm. Since the AMS 0.8 μm CMOS process provides two polysilicon layers (poly 1 and poly 2), the storage capacitor C_i is implemented as a poly-to-poly capacitance. The capacitance is surrounded by a guard ring connected to the analog ground. Two metal layers (metal 1 and metal 2) were used for routing. Connections to the input bus, read bus, analog ground and V_C are done with metal 1 while for $w < i >$ and $r < i >$ with metal 2. The M_{wi} and M_{ri} transistors can be

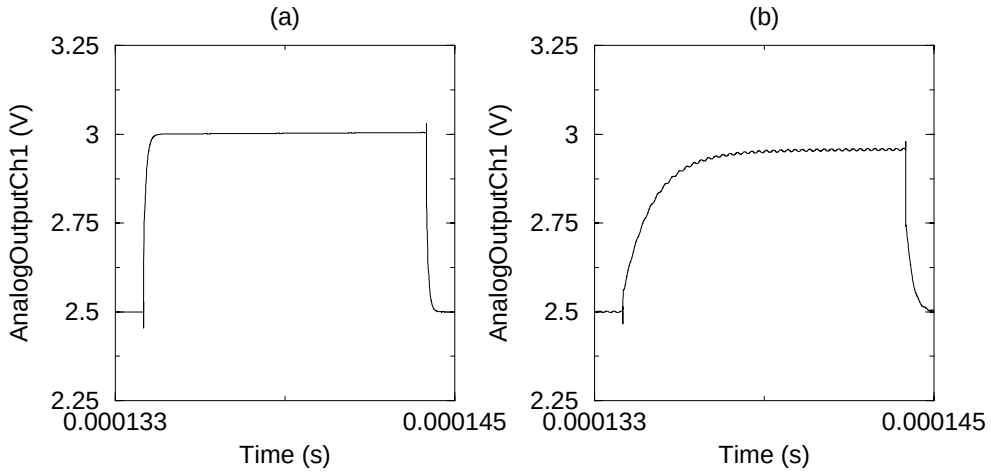

Figure 7.5: Response after simulations of one analog memory cell to a 2 V peak-to-peak, 3.906250 MHz sine wave sampled at 500 MHz after (a) ideal and (b) parasitic simulations. The pulse is plotted on the read time scale.

recognised in the layout by the intersection of diffusion and poly 1 layer representing the gate area. Contacts connect diffusion or polysilicon with the routing layer metal 1, whereas metal 1 and metal 2 are connected by vias. This layout configuration of an analog memory cell minimises the parasitic capacitance of the input bus.

7.3 Simulation Results

FASTSAMP-EV and FASTSAMP-V1 were simulated with SPICE [43]–[46]. Ideal and parasitic simulations were performed and the simulation setup was identically for both chips. The response after ideal simulations of one channel to a 2 V peak-to-peak (from 1.5 V up to 3.5 V) input sine waveform is shown in Figure 7.4(a) and illustrates the operation of the circuit with V_C and V_B set to 2.5 V. The output signal levels of the 128 memory cells are alternated with the amplifier reset level, V_B, as illustrated in the timing diagram in Figure 3.4(b). The readout time for each cell was set to 10 μs and reset time to 1 μs. In Figure 7.4(b) the output pulse is plotted as a function of input time, and the results agree with the input pulse. The input signal range of 2 V has been chosen according with (3.14) and (3.15) to avoid the subthreshold leakage.

The parasitic simulations included all parasitic capacitances extracted from layouts. The results after ideal and parasitic simulations for one memory cell are shown in Figure 7.5(a) and (b), respectively. It should be noted the effect of the parasitic capacitances on the raising edge of the pulse represented in Figure 7.5(b).

Both ideal and parasitic simulations were performed without using load capacitances at the outputs of the operational amplifiers. As was discussed in Section 4.3, 10 pF load capacitances must be considered for real applications.

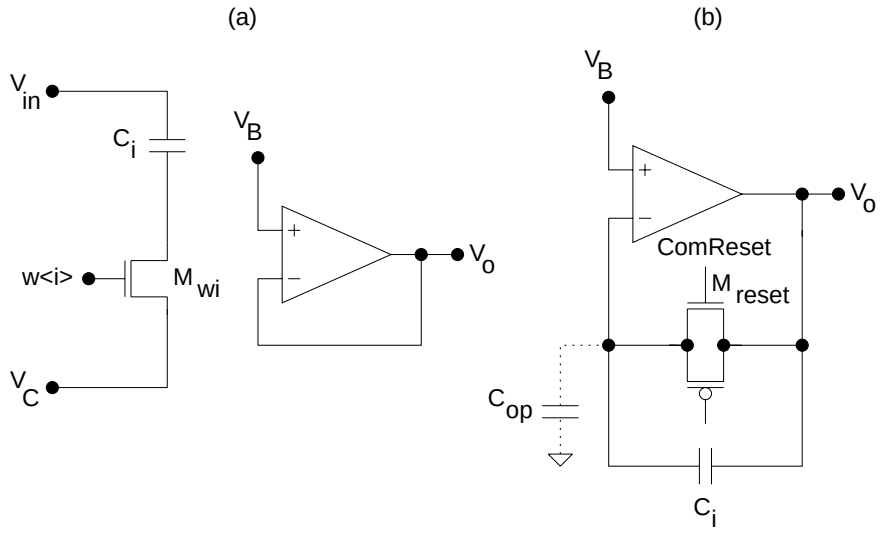

Figure 7.6: Circuit for analysis of analog memory noise during the (a) write and (b) read phase.

7.4 Analog Memory Noise

The output voltage of the analog memory circuit is contaminated by noise. The main sources of noise are thermal and flicker noise generated in the switches and in the operational amplifiers, and noise coupled directly or capacitively through the power, ground, clock lines, and through the substrate. The power supply lines must be bypassed to ground sufficiently to attenuate potential noise sources. Noise injected from clock lines into circuit nodes and into the substrate may contribute to the pedestal voltage of a memory cell.

In order to investigate the noise performance of the analog memories, the simplified circuits shown in Figure 7.6 are considered, which correspond to the write and read configuration, respectively. C_{op} is the parasitic capacitance at the inverting amplifier input and is dominated by the capacitance of the read bus to ground C_{rdb}. The value of C_{rdb} has been extracted from the layout of the analog memory core and listed in Table A.2 of Appendix A. In the write phase when the write switch is turned off the thermal noise voltage is given by kT/C_i [31], where $k = 1.38 \times 10^{-23}$ [J/K] is the Boltzmann's constant and T is the absolute temperature. During the read phase the capacitor C_i is switched across the amplifier, and the square of the total noise voltage for the analog memory is given by

$$\overline{v_n^2} = \frac{kT}{C_i} + \left(\frac{C_i + C_{op}}{C_i}\right)^2 \overline{v_{op}^2} \tag{7.1}$$

where $\overline{v_{op}^2}$ is the input referred noise from the amplifier. In order to obtain the amplifier noise voltage, $\overline{v_{op}^2}$, the amplifier noise power density $S_{op}(f)$ in (4.10) must be multiplied by a noise transfer function and integrated over the unity-gain bandwidth f_u (1.92 MHz) of the amplifier. Since the reset switch, M_{reset}, across the amplifier in Figure 7.6(b) is closed

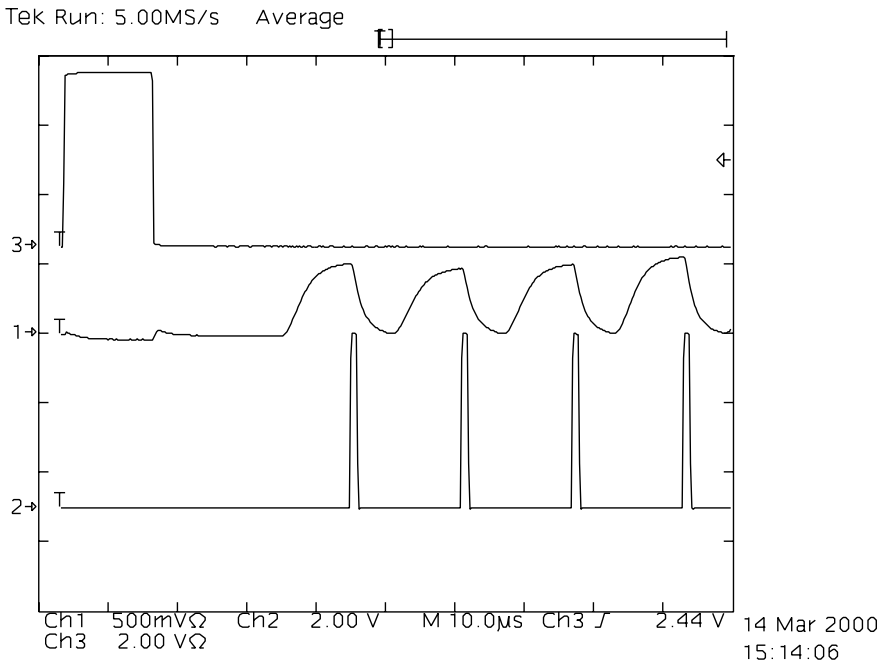

Figure 7.7: Picture taken from the oscilloscope representing three channels Ch1: $AnalogOutputCh1$, Ch2: $TriggerScope$ and Ch3: $ComIn$ or $ComInOut$ depending of the chip version.

and opened before the memory cell is addressed for readout, the circuit forms a correlated double sampling (CDS) system [32]. It is known that the noise transfer function of a CDS system is given by

$$H(f) = 2sin\left(\frac{2\pi f T_s}{2}\right), \tag{7.2}$$

where T_s is the interval from the time when the reset switch is turned off until the time when the analog memory cell is addressed for readout. The time interval T_s was 9 μs during measurements. The noise contributed from the amplifier in Figure 7.6(b) is given by

$$\overline{v_{op}^2} = \int_0^{f_u} S_{op}(f)H^2(f)df. \tag{7.3}$$

The total circuit noise in the system, expressed by (7.1), is theoretically

$$\overline{v_n} = \sqrt{(8280\ \mu V^2) + (7.6)^2(3974\ \mu V^2)} = 488\ \mu V. \tag{7.4}$$

It is therefore concluded that the total circuit noise is limited by the noise in the amplifier.

Device Name			FASTSAMP-EV	FASTSAMP-V1
Parameter	Symbol	Calculation	Measurement	Measurement
Cell gain	A_i	0.979	0.982	0.972
Cell offset voltage	V_{offi}	141 mV	147 mV	136 mV

Table 7.1: Calculation and measurement results for both devices.

7.5 Experimental Results

The experimental test setups used to evaluate the performance of the analog memory circuits are described in detail in Appendix C and Appendix D. The dc and ac results presented in this section are thus representative for the performance of both devices. The dc power dissipations for FASTSAMP-EV and FASTSAMP-V1, when operated from +5 V analog and +5 V digital supplies, were measured to be 50 mW and 35 mW, respectively, and were dominated by dissipation of the output amplifiers, delay chains and servo feedback circuits.

In order to measure the dc or ac voltages stored in analog memory cells in one analog memory channel a signal *TriggerScope* was created, as illustrated in Figure 7.7. Depending of the chip version, the signal *ComIn* or *ComInOut* was applied to the third channel of the oscilloscope as a trigger signal. The waveforms were transfered via GPIB [52] interface from the oscilloscope to a Hewlett Packard workstation. At each edge of signal *TriggerScope* a dc or ac voltage stored in a memory cell is read out. This was possible by programming in C and C++ programming languages [35, 36].

The dc and ac measurements for FASTSAMP-EV device were performed for 128 cells in one channel. Unfortunately for FASTSAMP-V1 device was only possible to perform measurements over 32 cells (instead of 128 cells), because the rest of the cells were not working properly. After investigation of this problem it was assumed that its cause is a technology failure. Due to limitation in time a new submission in fabrication was not possible.

7.5.1 DC Transfer Characteristic

The input voltage range of 1.5 V (from 2 V up to 3.5 V) has been chosen for measurements according with the nonlinearities of the output amplifiers and with (3.14) and (3.15) to avoid the subthreshold leakage. This input signal range was set for both devices.

The measured pedestal voltages uncorrected for the 32 cells of FASTSAMP-V1 device are plotted in Figure 7.9 as a function of the input voltage. The cell-to-cell pedestal variations result in a deviation from the average of 50 mV. This deviation is determined by the control signal feedthrough on-chip and on printed circuit board (PCB) and by the fabrication process used. The deviation for the 128 cells in one channel of FASTSAMP-EV device was of 150 mV. This improvement of the deviation in FASTSAMP-V1 device was determined through a carefully layout of the PCB. The cell-to-cell pedestal variations are not accepted for the Cherenkov application and therefore dc and ac calibrations must be performed. As dc calibration the multiplication and addition method with two calibration

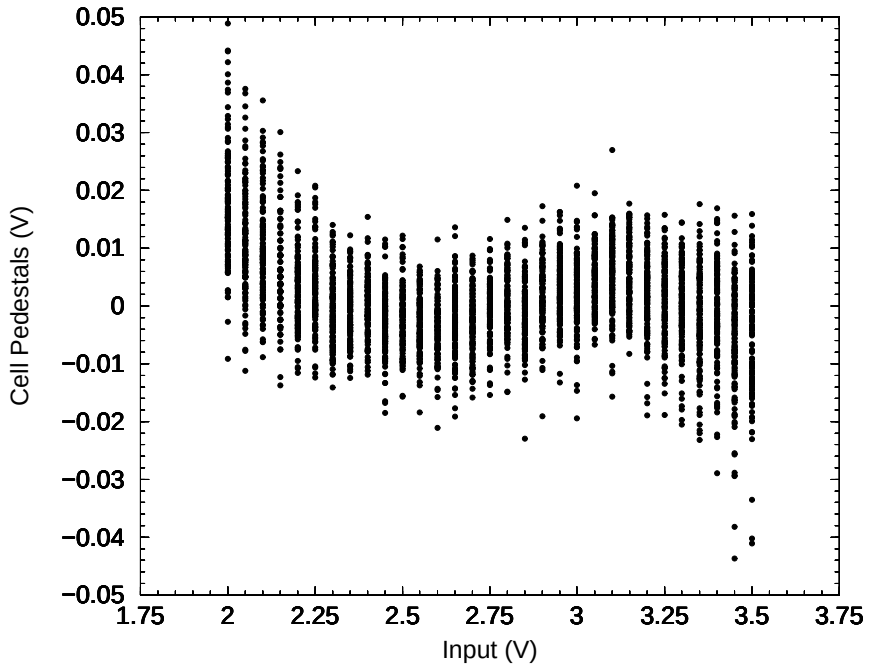

Figure 7.8: Cell pedestals after calibration as a function of input voltage for the 128 memory cells. Dc measurements for FASTSAMP-EV device.

voltages ($V_{cal1} = 2$ V and $V_{cal2} = 3.5$ V) was used to correct both cell-to-cell gain and offset voltage errors for dc input signals.

In order to investigate whether the cell pedestals depend on the input signal, the responses to various dc input levels were recorded, and the responses after dc calibration using a multiplication and addition method are plotted in Figure 7.8 and Figure 7.10, respectively, as a function of the input voltage. The rms cell response variation across the full input range is 10 mV for both devices, demonstrating that the sampling switch charge injection is independent of the dc input level and can be reduced by a simple calibration procedure.

The cell gain and offset voltage variations for devices are plotted as a function of cell number, as illustrated in Figure 7.11 and Figure 7.12, respectively. The average gains were measured to be 0.982 and 0.972, with an rms gain variation of 0.01, as indicated by Figure 7.11 and Figure 7.12. The average offsets were measured to be 147 mV and 136 mV, respectively. The values calculated for gain A_i and offset V_{offi} from (3.12) and (3.13) approximately agree with the measured values, as listed in Table 7.1.

The nonlinearity of each device was measured by applying 31 equally spaced input voltages and plotting the output levels as a function of input levels. Figure 7.13 and Figure 7.14 show the output of a typical cell and the deviations plotted as a function of input voltage over a range of 1.5 V. The maximum deviation in each case is 20 mV, or 1.3 %

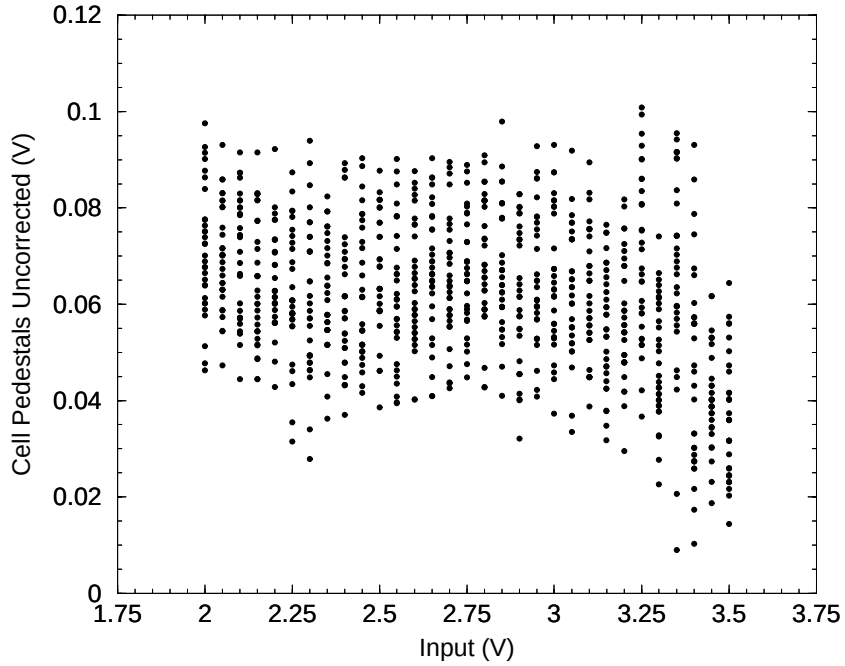

Figure 7.9: Cell pedestals before calibration as a function of input voltage for the 32 memory cells. Dc measurements for FASTSAMP-V1 device.

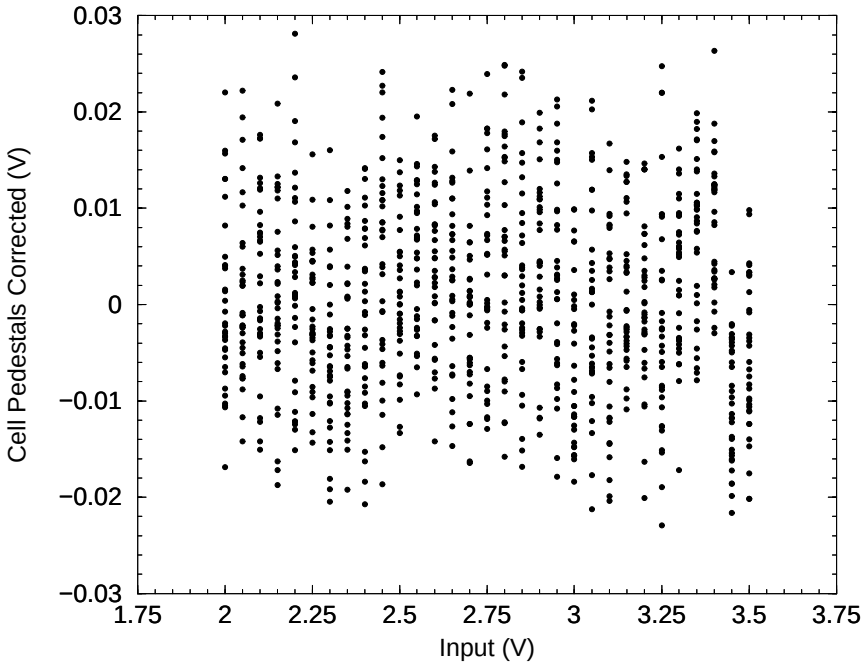

Figure 7.10: Cell pedestals after calibration as a function of input voltage for the 32 memory cells. Dc measurements for FASTSAMP-V1 device.

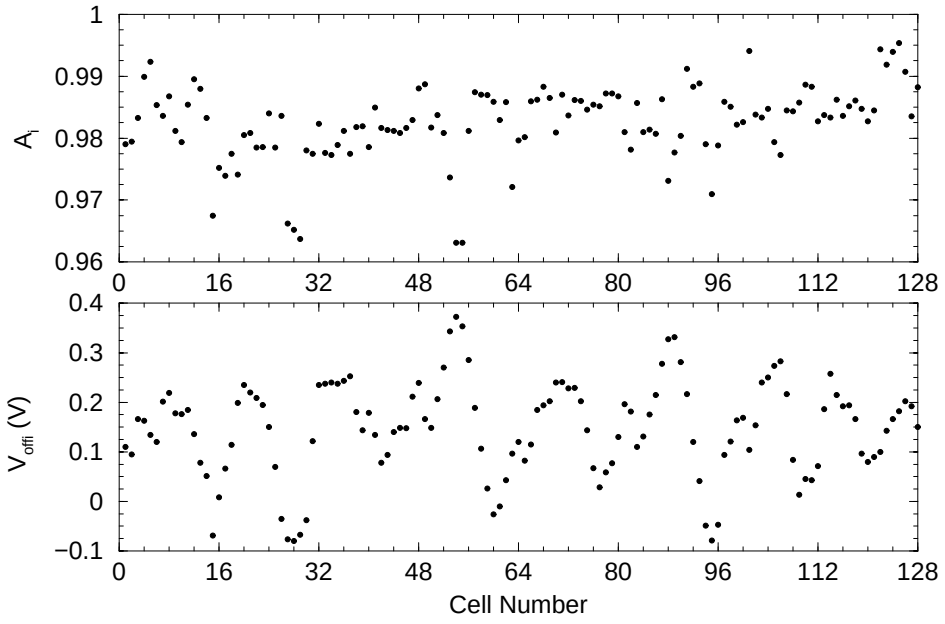

Figure 7.11: Cell gain (upper) and cell offset voltage (lower) as a function of cell number for FASTSAMP-EV device.

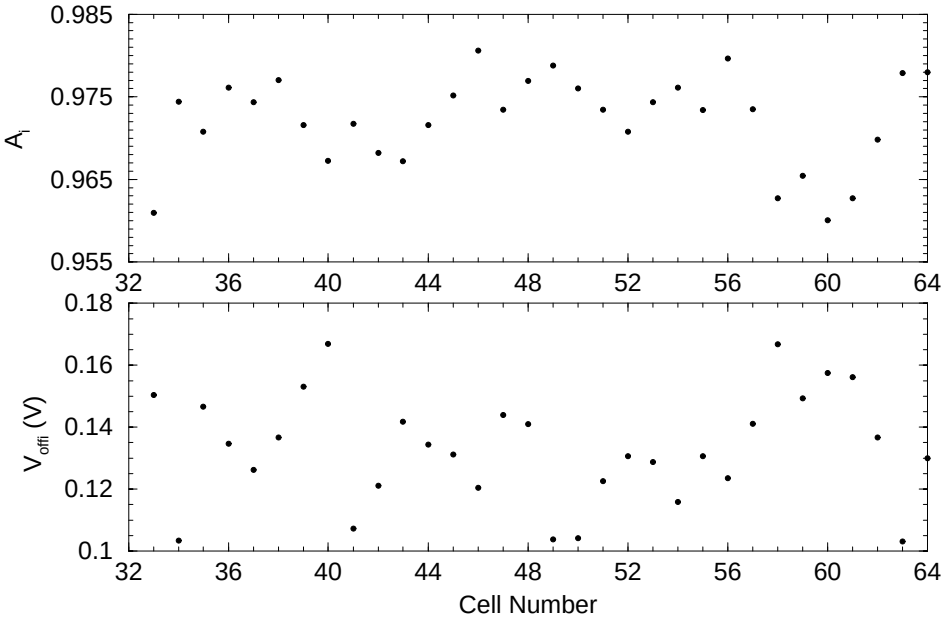

Figure 7.12: Cell gain (upper) and cell offset voltage (lower) as a function of cell number for FASTSAMP-V1 device.

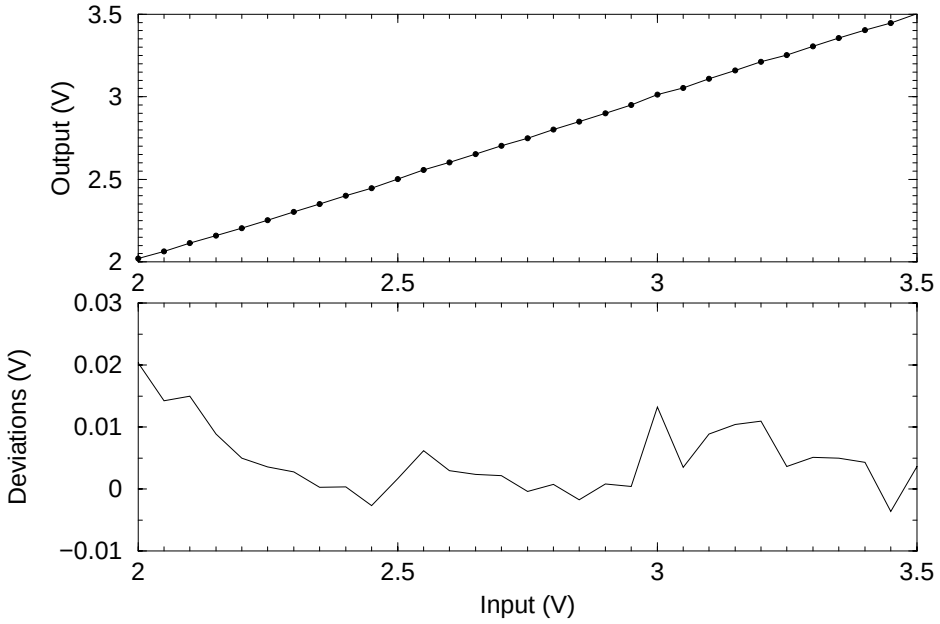

Figure 7.13: Upper: Output plotted as a function of input voltage. Lower: Deviations for the selected 1.5 V input signal range. Dc measurements for FASTSAMP-EV device.

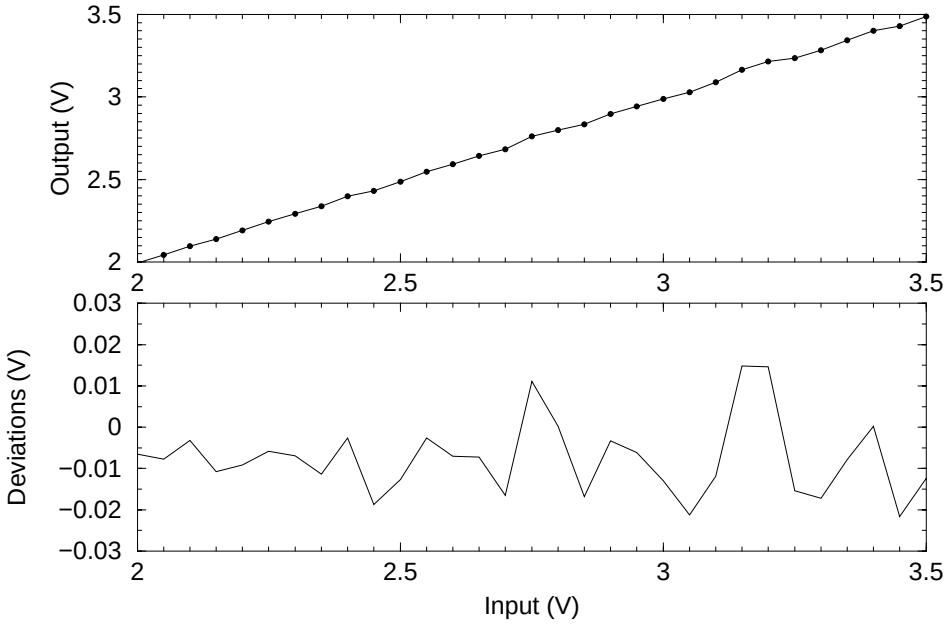

Figure 7.14: Upper: Output plotted as a function of input voltage. Lower: Deviations for the selected 1.5 V input signal range. Dc measurements for FASTSAMP-V1 device.

of the chosen input voltage range of 1.5 V.

7.5.2 Dynamic Range

The dynamic range of an analog memory circuit [26] is commonly defined as the maximum recordable signal divided by the baseline noise. The baseline noise of these analog memories was determined by recording the response of the devices to repeated measurements [33, 34] with a constant input voltage level and by calculating the mean square rms voltage error

$$\overline{v_{rms}} = \frac{\sqrt{\sum_{i=1}^{M}(V_{oi} - V_{avg})^2}}{\sqrt{M-1}}, \tag{7.5}$$

where V_{oi} is the output voltage of cell i and V_{avg} is the average of M measurements,

$$V_{avg} = \frac{1}{M}\sum_{i=1}^{M} V_{oi}. \tag{7.6}$$

An rms error voltage of 10 mV for each device was obtained from sets of 100 repeated measurements. The dynamic range is therefore better than 150/1, or 8 bits, for a 1.5 V input voltage range.

7.5.3 AC Response

Figure 7.15 shows the response of FASTSAMP-V1 device to a 1.5 V peak-to-peak gaussian pulse sampled at 500 MHz. At 3 V amplitude of the input signal the width of the gaussian pulse is 10 ns. On the reconstructed output signal can be seen five samples which corresponds to 10 ns, as illustrated in Figure 7.15(c). This proves that the sampling frequency is stable in time. It should be noted that the response of the device to a gaussian pulse is shown without using a calibration procedure.

The response of FASTSAMP-V1 device to a rectangle pulse with a 6 ns rise time is shown in Figure 7.16. In Figure 7.16(c) the output pulse is plotted as a function of input time, and the results agree with the input pulse, as monitored on an oscilloscope, with respect to rise time, fall time and pulse width.

The ac performances of the devices were evaluated applying sine waves at the analog inputs. The pedestal subtracted responses of 20 separate sets of measurements are shown in Figure 7.17 and Figure 7.18, respectively. The deviations of the measured data from the ideal sine waves are plotted and a rms error voltage of 10 mV was calculated for each device. The errors can be attributed to a variety of sources, including errors in sampling time, variations in the ac response of different cells, nonlinearities, and electronic noise.

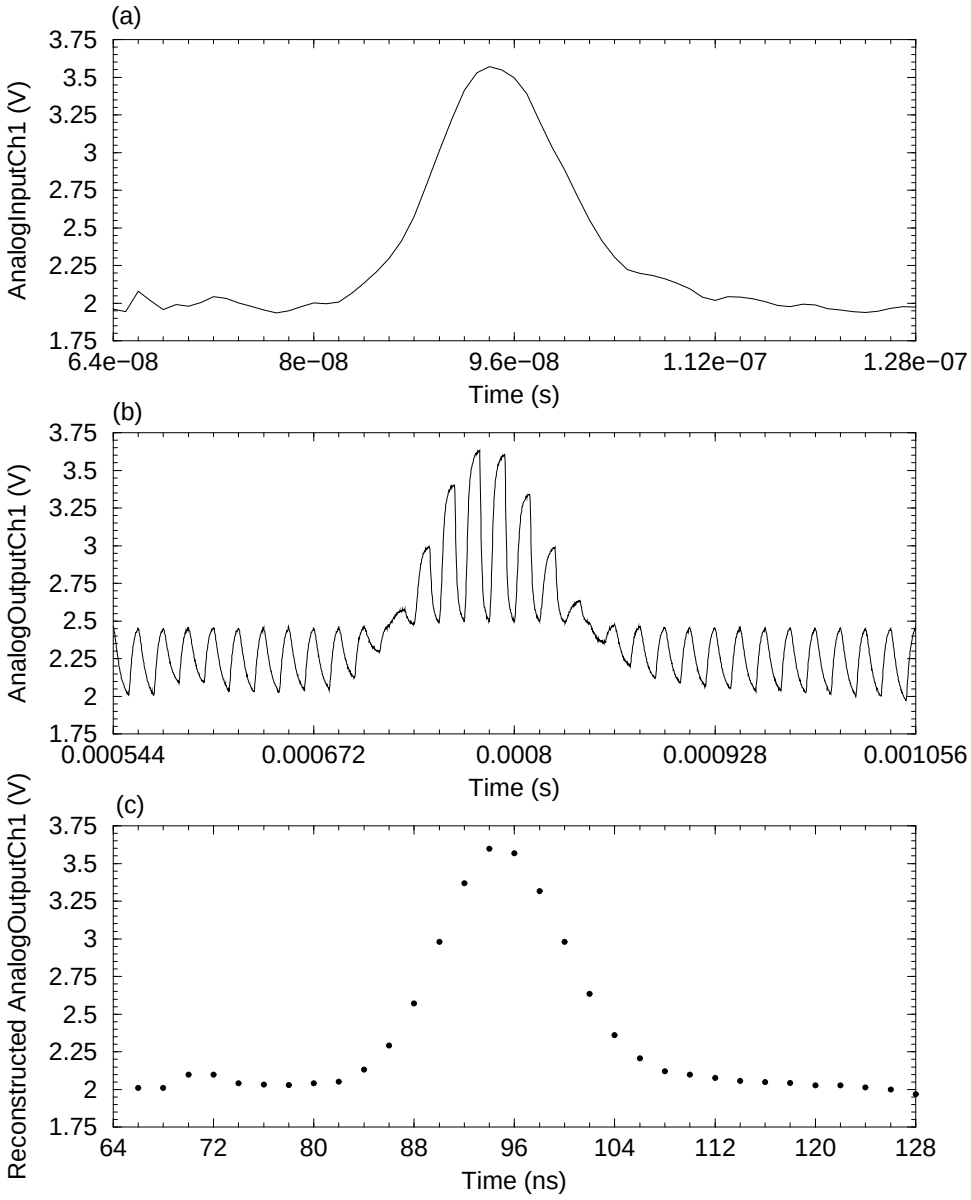

Figure 7.15: Response after measurements of 32 cells to a 1.5 V peak-to-peak (a) gaussian pulse sampled at 500 MHz. The pulse is plotted on the (b) read and the (c) write time scale. Ac measurements for FASTSAMP-V1 device.

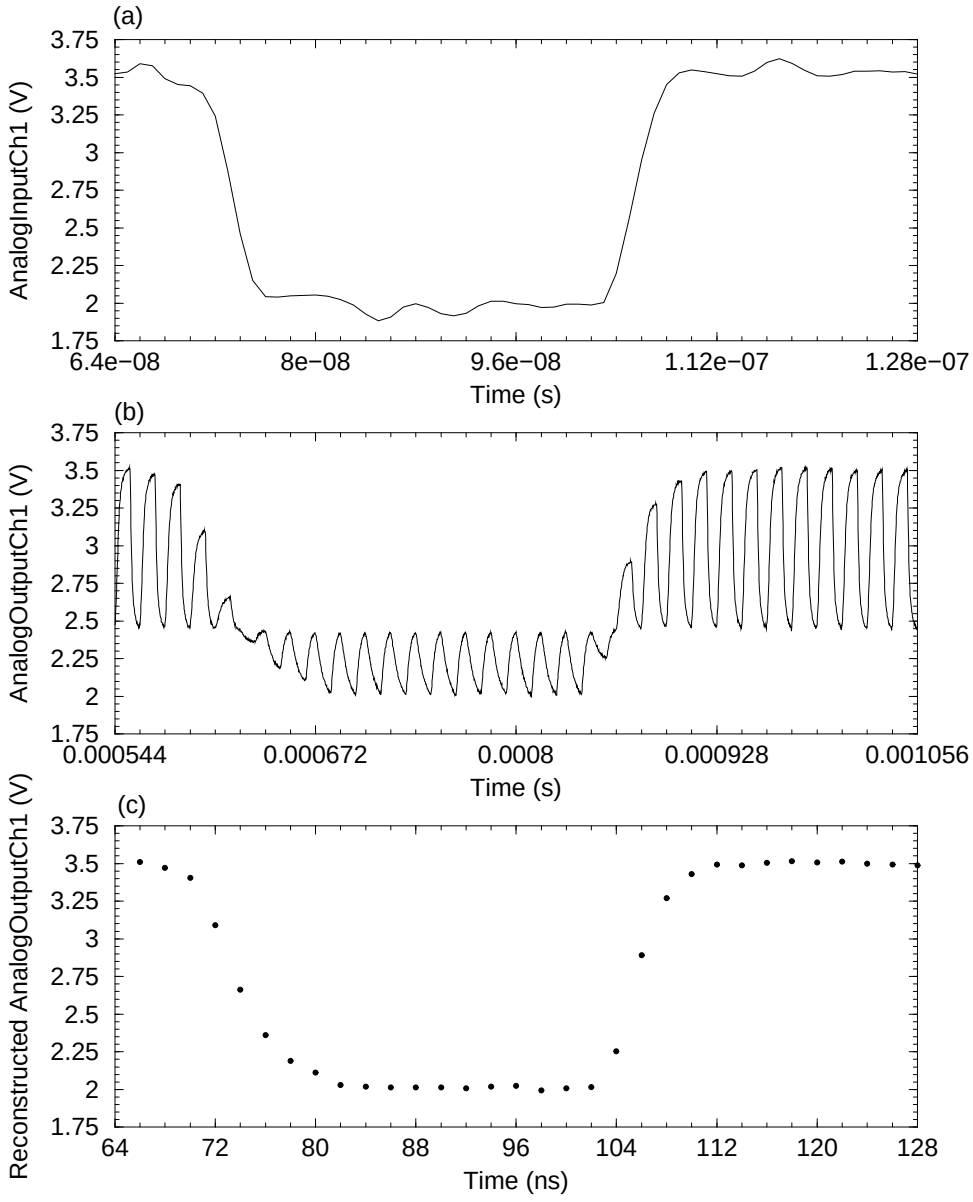

Figure 7.16: Response after measurements of 32 cells to a 1.5 V peak-to-peak (a) rectangle pulse sampled at 500 MHz. The pulse is plotted on the (b) read and the (c) write time scale. Ac measurements for FASTSAMP-V1 device.

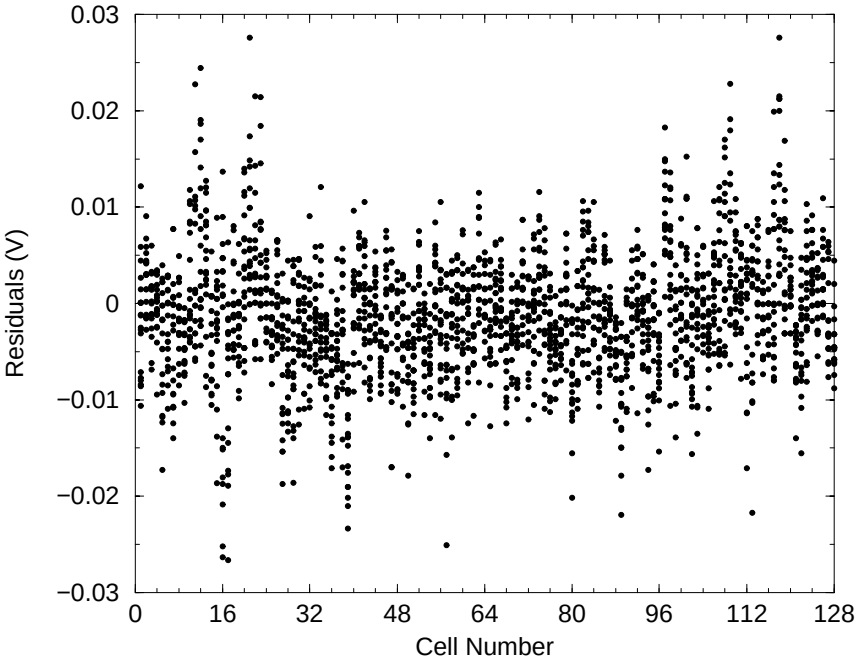

Figure 7.17: Results of 20 measurement sets from a 1.5 V peak-to-peak, 3.906250 MHz sine wave sampled at 500 MHz. Residuals are plotted as a function of cell number for FASTSAMP-EV device.

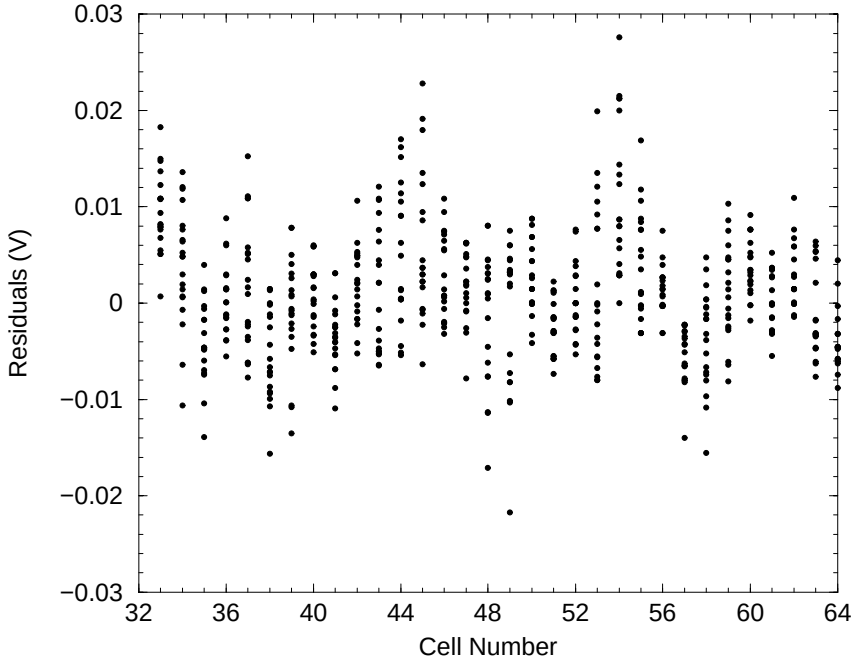

Figure 7.18: Results of 20 measurement sets from a 1.5 V peak-to-peak, 15.625 MHz sine wave sampled at 500 MHz. Residuals are plotted as a function of cell number for FASTSAMP-V1 device.

Device Name	FASTSAMP-EV	FASTSAMP-V1
Cell pedestal variations across full input range of 1.5 V		
uncorrected	150 mV	50 mV
corrected	10 mV	10 mV
Nonlinearity (for 1.5 V full scale)	1.3 %	1.3 %
Cell gain non-uniformity	1 % (mean gain: 0.982)	1 % (mean gain: 0.972)
Dynamic range	8 bits	8 bits
Acquisition time	< 500 ps	< 500 ps
RMS timing error in one delay chain	160 ps	160 ps
Sampling frequency	500 MHz	500 MHz
Readout frequency	100 kHz	100 kHz
Power dissipation on		
device	50 mW	35 mW
PCB	100 mW	555 mW

Table 7.2: Performances for both devices.

7.6 Summary

The implementation of two analog memory circuits have been described in this chapter. Two chip versions were fabricated; a first experimental chip FASTSAMP-EV followed by FASTSAMP-V1 which is more approached to the camera electronics. Measurement results at sampling rate of 500 MHz were presented. The dc and ac results of the performance tests are summarised in Table 7.2.

It was shown that the baseline noise that was measured for the fabricated analog memory circuits is limited by the noise in the amplifier. Theoretically, the value of the total noise calculated by (7.4) of 488 μV should agree with the rms error voltage of 10 mV from (7.5) after measurements. This difference between the two noise values may be due to perturbations caused by the power supply (e.g. ringing), ground, control signals, routed on board traces to the chip packages.

Chapter 8

Conclusions and Suggestions

8.1 Conclusions

Many acquisition systems require the recording of analog waveforms at a high rate and with high resolution. In applications such pulse echo phenomena (radar, ultrasonics), pulse shape recording (high energy physics experiments), and laboratory instrumentation (oscilloscopes, transient digitisers), the analog waveforms need only to be captured for a limited period of time and a continuous digitisation is not required.

This research has concentrated on switched capacitor analog memories. The goal of this research was to investigate analog memories for waveform sampling at several hundred MHz. An effort was devoted to optimise the analog memory architecture and circuit implementation for uniformity of memory cell responses within a channel. This is especially important in Cherenkov application, where analog waveforms of hundreds of channels are recorded. In this application it is also important to minimise the complexity of dc and ac calibration, as well as the number of calibration constants needed to correct the data.

After an examination of the characteristics of MOS switches and capacitors, this work has analysed their performance in a number of sample and hold configurations wherein the switch can be inserted in the signal or signal return paths. Expressions for the error voltages from switch charge injection and clock feedthrough effect were derived for circuits wherein the sampling capacitance is not large compared to the parasitic capacitances associated with the sampling switch. It was analytically shown that the sampling switch must be inserted in the signal return path to eliminate cell specific gain and sampling time errors that are dependent on the input signal level.

Based on the results from the investigation of the sample and hold circuits, an analog memory architecture was proposed. The transfer function of this memory was derived and then verified by measurement results obtained from two devices. It was shown that the memory cell pedestal voltages are independent of the input signal voltage and that the cell specific voltages can be cancelled by a simple multiplication and addition procedure.

Each channel of the analog memory incorporates an on-chip operational amplifier for readout. The amplifier provides sufficient gain, bandwidth, and low power dissipation.

The results from simulations and calculations show that the folded cascode amplifier circuit is well suited for use in this application.

At high sampling speeds, the variations in cell-to-cell sampling times due to the sensitivity of on-chip delays to the fabrication process, the temperature, and the power supply levels are considerable, and extensive dc and ac timing timing correction procedures are required. In addition, a high speed sampling clock must be provided to the circuit. This thesis proposed the use of inverter chains for write control, which avoid the need for a high speed external clock. This write control circuit is insensitive to variations in the fabrication process, temperature, and supply levels because servo feedback circuits are used to adjust the sampling rate. Furthermore, the high speed write signals are confined to a small area on the dies, and perturbations from external clocks that otherwise must be distributed across the chips are avoided.

Two 4 channel $\times$ 128 cell analog memories for use in Cherenkov application were fabricated in a AMS 0.8 μm CMOS technology with poly-to-poly capacitors, and operated at sampling rate of 500 MHz. The cell-to-cell sampling time variation is 160 ps rms. The acquisition time of the analog memories for a given accuracy is less than 500 ps. The measured nonlinearity is 1.3 % for a 1.5 V input range, and the cell to cell gain matching is 1 % rms. The uniformity of the individual memory cell responses across the whole input voltage range is 10 mV rms after a simple multiplication and addition procedure. The dynamic range of the circuits is 8 bits and the power dissipation for devices, when operated from +5 V analog and +5 V digital supply levels, is 50 mW and 35 mW, respectively.

The proposed analog memories are an alternative for the camera electronics of the Cherenkov telescope where continuous data acquisition is not required.

8.2 Suggestions for Future Work

A number of suggestions merits to be taken in consideration for further investigation.

- A new circuit board smaller than the previous boards would be necessary to be implemented. This board must be carefully designed to minimise the perturbations caused by routed on board traces , reflections on cables, ringing of power supply, and control signals. The experimental device should be bounded directly on board and not by using a chip package and socket (68 pin CLCC). This configuration minimises the parasitic and cross-coupling capacitances and may increase the dynamic range and the readout speed.

- An analog calibration was used to correct data. The output voltages were measured with high impedance FET probes and their values displayed on the digital oscilloscope. Errors can occur due to the probe and oscilloscope measurements. Therefore a digital calibration would be suitable for the analog memories. The waveforms applied at the analog inputs are stored in the analog memories and then digitised by analog-to-digital converters. The digitised output voltage levels are transferred into static digital memories. These digital memories can also store the calibration constants.

- It would be possible the integration of analog-to-digital converters on a single die. This would enable an implementation of an on-chip digital correction circuit.

- The maximum sampling rate of the analog memories is limited by the delays of the inverters in the write control circuit, as explained in Section 5.2. In AMS 0.8 μm CMOS technology the sampling rate can be increased to 1 GHz by modifying the drawn dimensions of MOS transistors in the delay chains. In more advanced CMOS submicron technologies it should be possible to attain sampling speeds of 2 GHz.

Appendix A

Parameters

	Parameter	Symbol	Value	Units
NMOS Electrical Parameters	electron mobility	μ_n	4.63×10^{-2}	m^2/Vs
	threshold voltage	V_{Tn}	0.72	V
	flicker noise coefficient	K_{fn}	2.33×10^{-26}	–
	flicker noise exponent	A_{fn}	1.451	–
PMOS Electrical Parameters	hole mobility	μ_p	1.67×10^{-2}	m^2/Vs
	threshold voltage	V_{Tp}	-0.72	V
	flicker noise coefficient	K_{fp}	6.314×10^{-29}	–
	flicker noise exponent	A_{fp}	1.279	–
Capacitance	oxide capacitance per unit area	C_{ox}	2.16×10^{-3}	F/m^2

Table A.1: AMS 0.8 μm CMOS Process Parameters [40].

	Parameter	Symbol	Value	Units
Capacitances	write transistor gate overlap capacitance	C_{wi}	8.5	fF
	read transistor gate overlap capacitance	C_{ri}	2.5	fF
	parasitic capacitance to ground at node x_i	C_{pi}	41	fF
	capacitance between the inverting input and the output of the amplifier	C_{pp}	10.6	fF
	capacitance of the input bus to ground	C_{inb}	4.6	pF
	capacitance of the read bus to ground	C_{rdb}	3.3	pF
	drain capacitance of the input switch	C_{is}	116	fF
Resistances	write switch on resistance	R_{wi}	180	Ω
	input switch on resistance	R_{is}	7	Ω

Table A.2: Analog Memory Core Parameters.

Appendix B

Analysis of Charge Injection in MOS Analog Switches

The error voltage induced by the turning off of a MOS switch is one of the fundamental factors that limit the accuracy of the switched capacitor circuits. A MOS transistor holds mobile charges in its channel when it is on. When the transistor turns off, some portion of the mobile charges is transferred to the storage capacitor and causes an error in the sampled voltage. The clock voltage feedthrough through the gate-drain overlap capacitance also contributes to the error. The turn off of an MOS switch consists of two distinct phases [22]–[25]. During the first phase, the transistor is on and a conduction channel extends from the source to the drain of the transistor. When the gate voltage reaches the threshold voltage, the conduction channel disappears and the transistor enters the second phase of turn off. During this phase, only the clock feedthrough through the gate-drain overlap capacitance continues to increase the error voltage.

In Figure B.1 is shown a schematic of the NMOS switch placed in signal return path together with parasitic capacitances associated and with sampling capacitance C_S. C_o is the gate oxide capacitance excluding overlap capacitance, C_p is the parasitic capacitance to ground, and C_{ov} is the gate overlap capacitance. The input voltage V_{in} and the dc reference voltage V_C are supposed to be constant during this analysis.

The transistor is turned off by changing the gate voltage V_G from the high voltage level V_H to the low level V_L, as represented by the PR segment in Figure B.1. The gate voltage is assumed to be a ramp function which begins to fall at time 0 from the high value V_H toward the low value V_L at a falling slope U,

$$V_G = V_H - Ut. \tag{B.1}$$

As long as the transistor is in the ohmic region ($V_H \geq V_G \geq V_C + V_T$), which corresponds to the PQ segment in Figure B.1, the drain-to-source current can be described as

$$I_{DS} = \beta \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} \tag{B.2}$$

where $V_{DS} = V_D - V_C$ is the transistor drain-to-source voltage, $V_{GS} = V_G - V_C$ is the transistor gate-to-source voltage, V_T is the threshold voltage, $\beta = \mu_n C_{ox} W/L$, μ_n is the

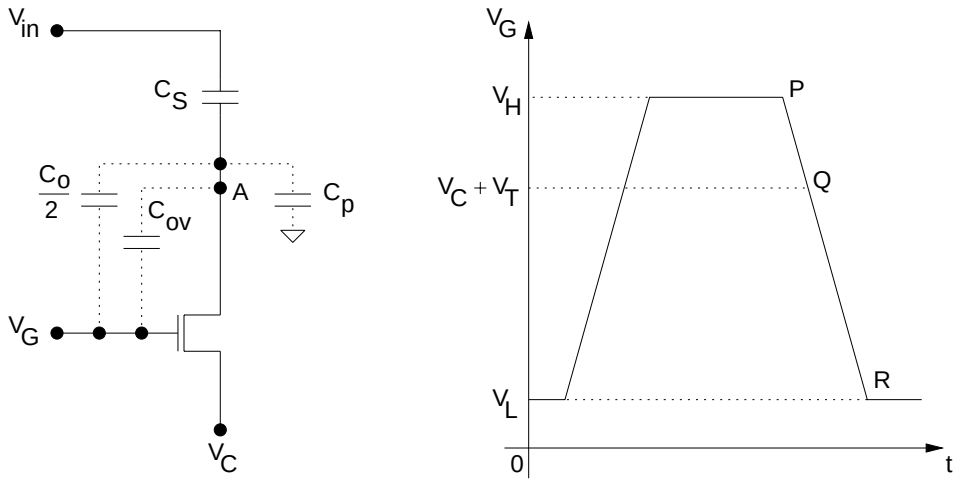

Figure B.1: Schematic of the NMOS switch placed in signal return path.

electron mobility in the channel, C_{ox} is the oxide capacitance per unit area, and W and L are the channel width and length of the transistor, respectively. For small drain-to-source voltages (B.2) can be approximated by

$$I_{DS} = \beta \left(V_{GS} - V_T\right) V_{DS}. \tag{B.3}$$

If (B.1) is inserted into (B.3),

$$I_{DS} = \beta \left(V_{HT} - Ut\right) V_{DS} \tag{B.4}$$

where $V_{HT} = V_H - V_C - V_T$.

From the Kirchhoff's Current Law applied at node A in Figure B.1,

$$C_{eq}\frac{dV_{DS}}{dt} = -\beta \left(V_{HT} - Ut\right) V_{DS} - \left(C_{ov} + \frac{C_o}{2}\right) U \tag{B.5}$$

where

$$C_{eq} = C_p + C_{ov} + \frac{C_o}{2} + C_S. \tag{B.6}$$

The solution of the differential equation [37, 38] with the boundary condition $V_{DS}(0) = 0$ is

$$\begin{aligned} V_{DS}(t) = &-\frac{C_{ov} + \frac{C_o}{2}}{C_{eq}}\sqrt{\frac{\pi U C_{eq}}{2\beta}} exp\left[\frac{\beta U}{2C_{eq}}\left(t - \frac{V_{HT}}{U}\right)^2\right] \times \\ &\times \left\{erf\left(\sqrt{\frac{\beta}{2UC_{eq}}} V_{HT}\right) - erf\left[\sqrt{\frac{\beta}{2UC_{eq}}}(V_{HT} - Ut)\right]\right\}. \end{aligned} \tag{B.7}$$

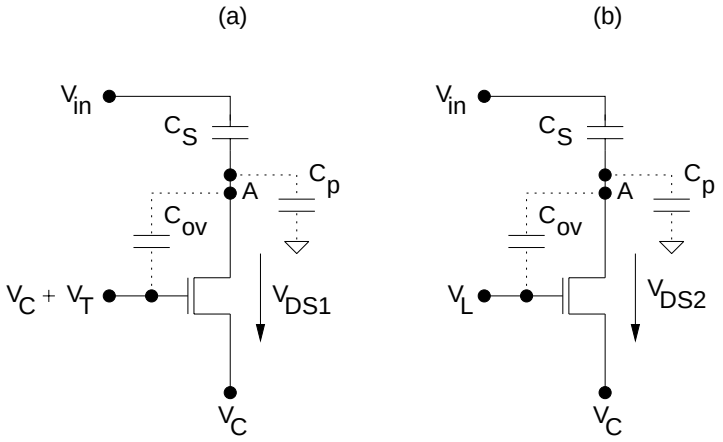

Figure B.2: Analysis of clock feedthrough effect for NMOS switch placed in signal return path when (a) $V_G = V_C + V_T$ and (b) $V_G = V_L$.

At $t_Q = V_{HT}/U$ which corresponds to the Q point in Figure B.1, the threshold condition is reached ($V_G = V_C + V_T$) and the first phase ends. The error voltage at this time is

$$V_{DS}(t_Q) = -\frac{C_{ov} + \frac{C_o}{2}}{C_{eq}} \sqrt{\frac{\pi U C_{eq}}{2\beta}} erf\left(\sqrt{\frac{\beta}{2UC_{eq}}} V_{HT}\right). \tag{B.8}$$

It is well known that

$$erf(x) \approx \begin{cases} 1 & \text{if } x \gg 1 \\ \frac{2x}{\sqrt{\pi}} & \text{if } x \ll 1 \end{cases} \tag{B.9}$$

therefore, (B.8) can be simplified for fast switching-off

$$\frac{\beta V_{HT}^2}{2C_{eq}} \ll U$$

$$V_{p1} = -\frac{C_{ov} + \frac{C_o}{2}}{C_{eq}} (V_H - V_C - V_T) \tag{B.10}$$

where V_{p1} is the pedestal voltage due to the charge injection. Assuming that α is a coefficient ($0 < \alpha < 1$), $C_o = C_{ox} WL$ where C_{ox} is the oxide capacitance per unit area, then (B.10) can be written as follows

$$V_{p1} = -\frac{\alpha C_{ox} WL}{2C_S} (V_H - V_C - V_T). \tag{B.11}$$

After the transistor turns off ($V_G \leq V_C + V_T$), only the gate overlap capacitance contributes to the pedestal voltage. In order to calculate the pedestal voltage due to

the clock feedthrough effect, two configurations were proposed in Figure B.2. The total charge at node A in Figure B.2(a) is

$$Q_A^{(a)} = C_p(V_{DS1} + V_C) + C_S(V_{DS1} + V_C - V_{in}) + C_{ov}(V_{DS1} - V_T) \tag{B.12}$$

and in Figure B.2(b) is

$$Q_A^{(b)} = C_p(V_{DS2} + V_C) + C_S(V_{DS2} + V_C - V_{in}) + C_{ov}(V_{DS2} + V_C - V_L). \tag{B.13}$$

The charge conservation ($Q_A^{(a)} = Q_A^{(b)}$) and the voltage difference ($V_{DS2} - V_{DS1}$) defined as the pedestal voltage due to the clock feedthrough effect V_{p2} yield

$$V_{p2} = -\frac{C_{ov}}{C_{ov} + C_S + C_p}(V_C - V_L + V_T). \tag{B.14}$$

The total pedestal voltage V_p after turn off of the sampling switch is then

$$V_p = V_{p1} + V_{p2}. \tag{B.15}$$

Appendix C

FASTSAMP-EV Chip Test Setup

The test setup used to evaluate the performance of the FASTSAMP-EV chip is described in detail in this appendix. Figure C.1 illustrates the configuration of the instruments for the performance tests, while the instruments are identified in Table C.1. The chip was mounted on a printed circuit board (PCB) together with the supporting circuitry such as commercial amplifiers, resistors and capacitors. Only low speed digital input and output ports are required to control the circuit and to read out the measured data. The board can thus be operated without an elaborate high speed data acquisition system.

The test board was mounted in an aluminium box and the digital control signals were transmitted on LEMO cables to minimise the noise pick-up. The acquisition of the measured data was controlled by a Hewlett Packard workstation via GPIB [52] interface connected to the digitising oscilloscope TDS 420A [53, 55], as indicated in Figure C.1. A digital test equipment HP 82000 [56] was used to generate external signals necessary for the chip. The analog input waveforms were generated by a waveform generator AWG 2041 [57] and the supply voltages, +5 V analog and digital, were provided by a triple linear dc power supply IC-TRIPLE-100. The software used for control and data processing was written in C and C++ programming languages [35, 36]. The graphical HP VEE [58] data acquisition software was used to control the instruments and process the data.

The schematic for the PCB was entered on a workstation using CONCEPT [49, 50] schematic design software, and the board was laid out using the ALLEGRO [51] layout editor. A gerber file was then created, and the board was fabricated at ASIC laboratory in Heidelberg. The board measures 12 cm $\times$ 24 cm and consists of two layers.

Shown in Figure C.2 is the schematic of the board including the chip and the power supply connections. The chip was mounted on board in a socket (68 pin CLCC). The power for the analog and digital components is separated on PCB, as is the ground, to minimise feedthrough from the digital signals to the analog circuits. Outside the PCB, the analog ground and digital ground are connected together to ensure the functionality of the circuit. The power supplies $P_1 - P_3$ together with filter capacitances $C_{11} - C_{16}$ provide +5 V analog, +5 V digital, and +2.5 V reference voltage. Each chip power supply pin has its own ceramic decoupling capacitor as identified by $C_1 - C_{10}$.

In Figure C.3 are shown the connections between the chip and other components such as commercial amplifiers, resistors and capacitors. All input digital signals around

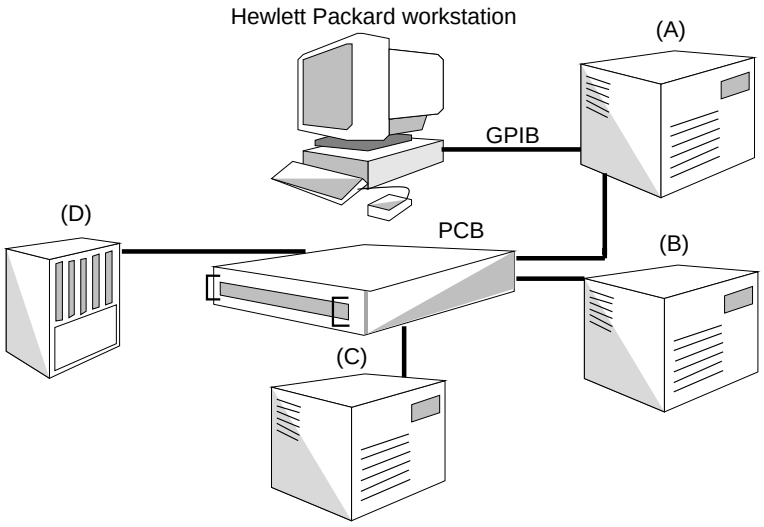

Figure C.1: Experimental setup for FASTSAMP-EV chip.

(A) Tektronix TDS 420A Digitising Oscilloscope
(B) Sony/Tektronix AWG 2041 Arbitrary Waveform Generator
(C) IC-TRIPLE-100 Linear Triple Power Supply
(D) Hewlett Packard HP 82000 Test Equipment

Table C.1: Test setup equipment list for FASTSAMP-EV chip.

the chip are connected by LEMO coaxial cables to the HP 82000 test equipment. The LEMO cables are transmission lines and have a characteristic impedance of 50 Ω. To avoid reflections on cables, every transmission line is terminated in a 50 Ω resistor on PCB, as represented by the resistors $R_1 - R_{27}$ and $R_{36} - R_{39}$, respectively. The analog signals applied at the inputs of the test board are ac coupled to the chip by the capacitors $C_{17} - C_{20}$ of 1 μF value and the dc voltages generated by the power supplies $P_4 - P_7$ are superimposed via 10 kΩ resistors $R_{40} - R_{43}$. Since these dc voltages can be changed, they can be used to generate the dc calibration voltage levels during the calibration phase. The outputs are buffered by the AD645 [59] operational amplifiers $U_{33} - U_{36}$. The AD645 is a low noise, high input impedance (FET) commercial amplifier, an excellent choice for high impedance applications where stability is of prime concern. $C_{21} - C_{28}$ serve for decoupling and are ceramic capacitors. In order to ensure a speed in the four servo feedback circuits of the chip, four resistors $R_{28} - R_{31}$ are connected to power supply and other four resistors $R_{32} - R_{35}$ to ground, respectively.

The operation of the circuit can be described into write and read phases. For testing the chip , 50 write cycles and one read cycle were sufficient. One sequence of 65000 vectors including 50 write cycles and one read cycle was repeated at infinite and each vector of the sequence was set to 32 ns. Figure C.4 and Figure C.5 show the vector diagrams for write and read phases.

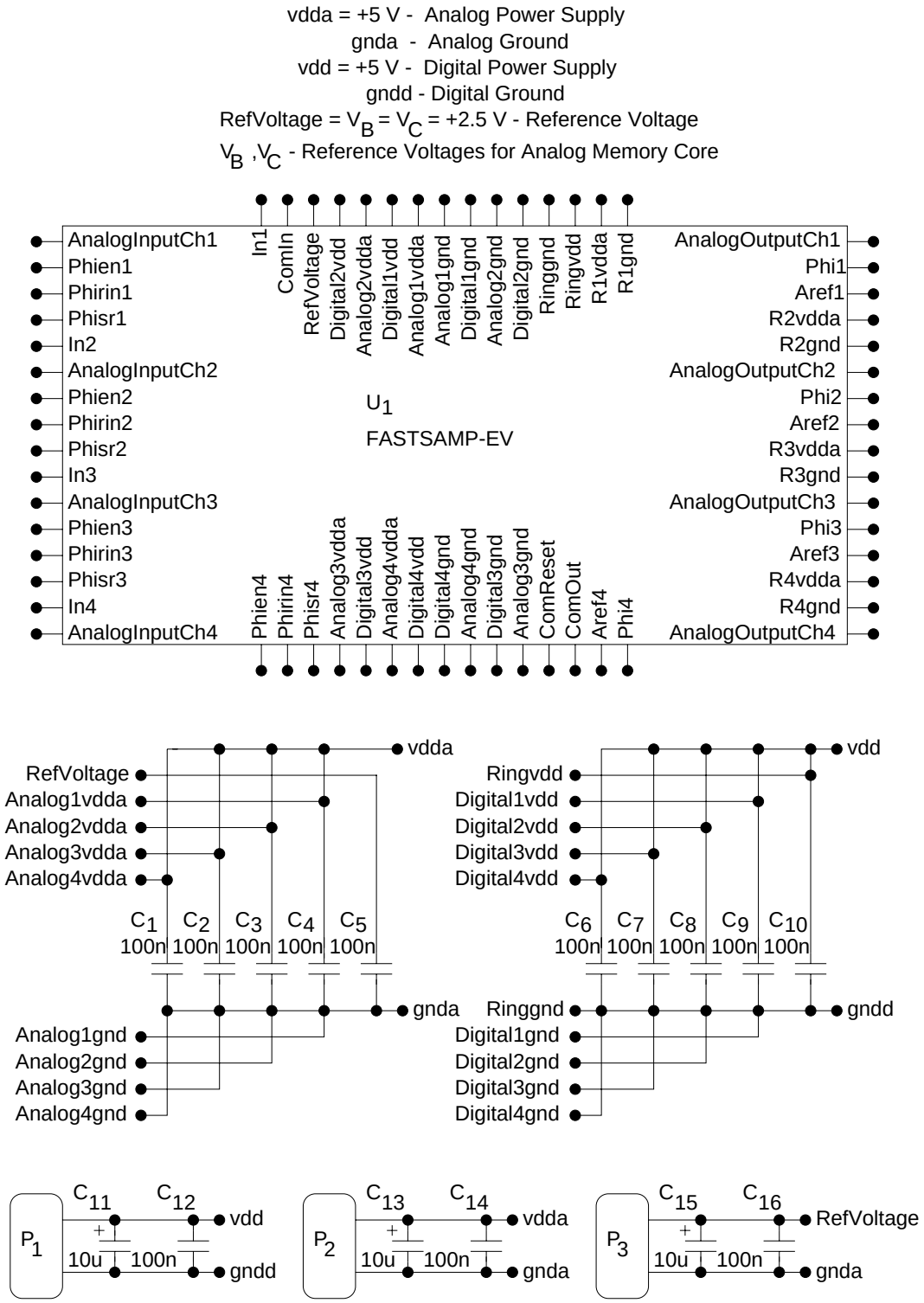

Figure C.2: Schematic of the Printed Circuit Board of FASTSAMP-EV chip. Power supply connections.

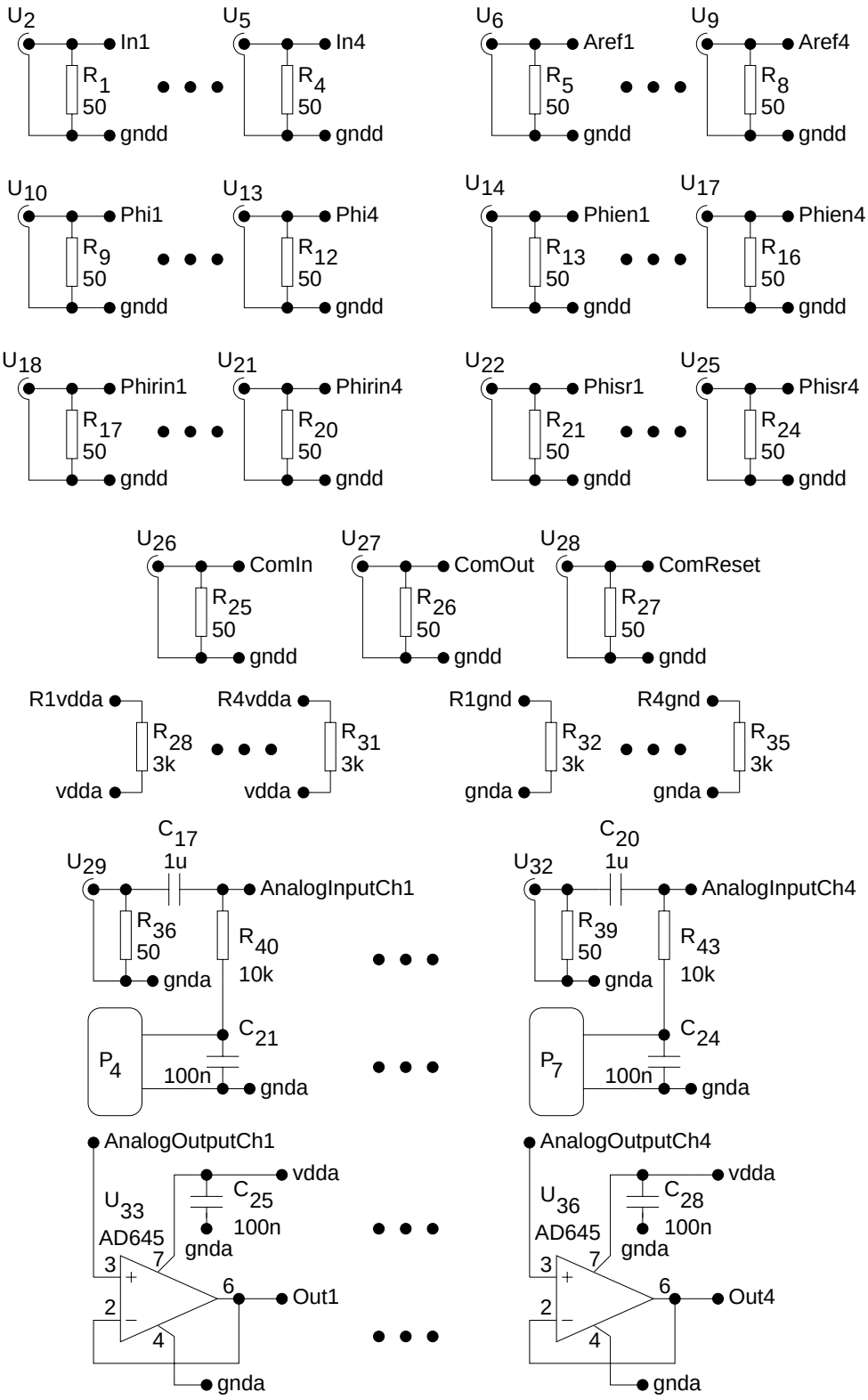

Figure C.3: Schematic of the Printed Circuit Board of FASTSAMP-EV chip. Connections between the chip and other components.

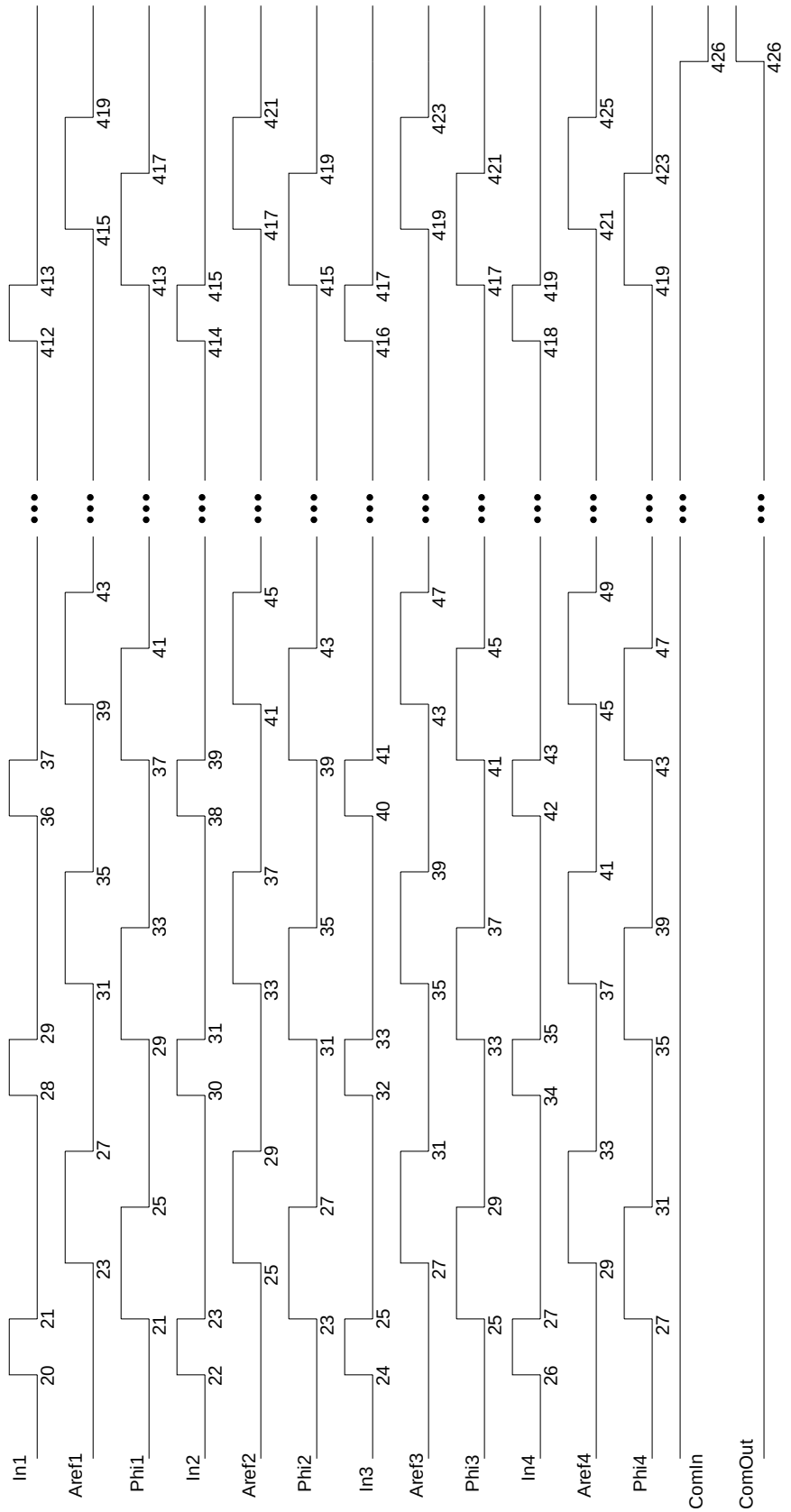

Figure C.4: Vector diagram for write phase of FASTSAMP-EV chip.

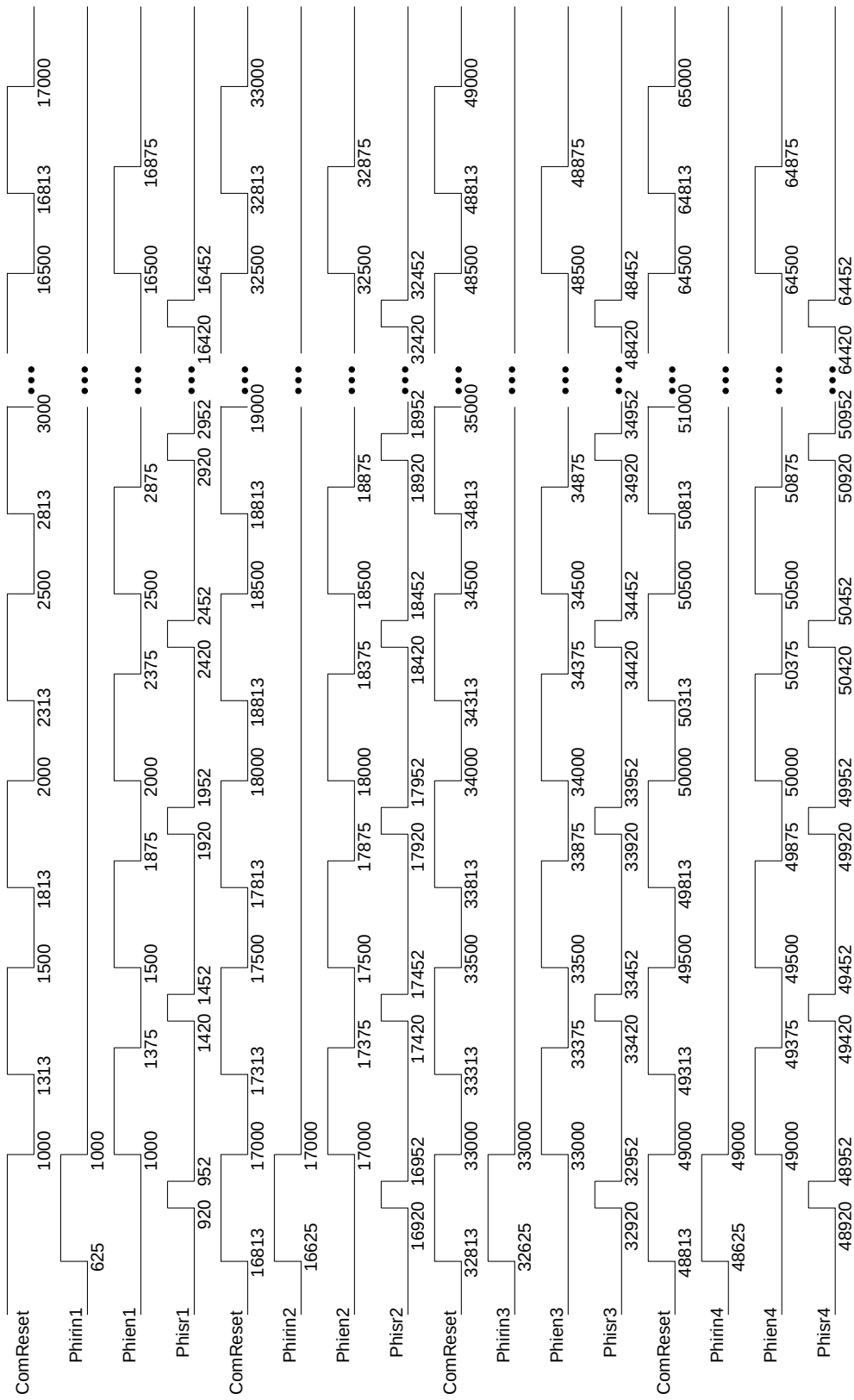

Figure C.5: Vector diagram for read phase of FASTSAMP-EV chip.

Appendix D

FASTSAMP-V1 Chip Test Setup

This appendix describes the test setup for FASTSAMP-V1 chip. The configuration of the instruments is shown in Figure D.1 and the instruments are identified in Table D.1. The steps for the acquisition data are explained in detail in Appendix C. To reduce the ground noise in this configuration the digital test equipment HP 82000 has been replaced by the data generator DG 2020A [60].

The printed circuit board (PCB) measures 14 cm $\times$ 14 cm and was mounted in an aluminium box. The board has two layers and was fabricated at ASIC laboratory in Heidelberg. The test board was laid out using the same software as for the PCB of FASTSAMP-EV chip.

The schematic of the board including the chip and the power supply connections is shown in Figure D.2. The connections of the power supply are similar as for the previous chip FASTSAMP-EV.

Figure D.3 shows the connections of the chip with a Generic Array Logic (GAL), counters, commercial amplifiers, resistors and capacitors. The digital input signals are connected to the DG 2020A data generator by LEMO coaxial cables and are terminated on PCB by 50 Ω resistors. The configurations for the analog inputs as well as for the analog outputs are the same as in the test board of FASTSAMP-EV chip. A clock signal *Clock* of 15.625 MHz is connected to the counters $U_2 - U_3$ and to the GAL.

Two 4-bit binary counters 74AS163 [61] were used to provide the address signals $a0$ through $a7$ necessary for the GAL device. The counters are on 8-bit cascading configuration and each of them has an internal look ahead circuitry for fast counting. The clear function for both counters is synchronous. Setting up a high level at the load enables the counters to be in the counting mode for all time. All unused inputs are connected to the ground to improve noise immunity and reduce the current for the devices. Each power supply pin of the counters is decoupled to ground by ceramic capacitors C_{17} and C_{18}.

A programmable device GAL is employed to produce the control signals necessary for the chip. The GAL26CV12 [62], at 4.5 ns maximum delay time from clock input to data output, combines a high performance CMOS process with Electrically Erasable (E^2) floating gate technology. This technology offers high speed erase times, providing the ability to re-program or reconfigure the device quickly and efficiently. The code for the GAL was written using ABEL-HDL [63] design software and the device was programmed

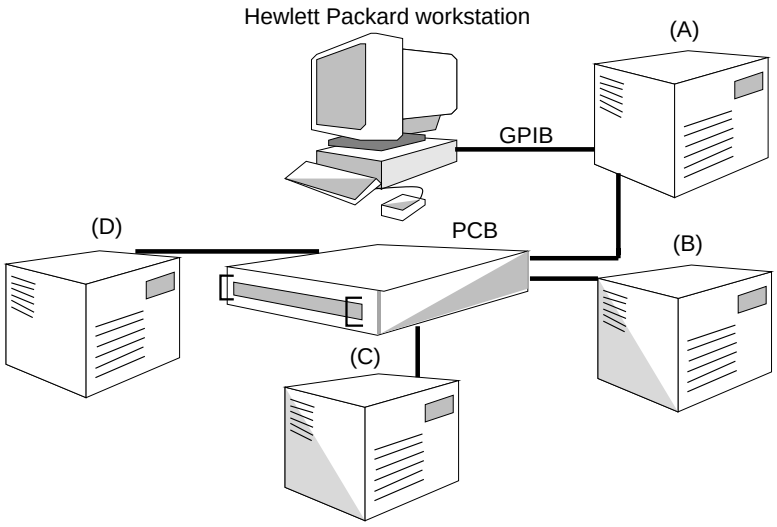

Figure D.1: Experimental setup for FASTSAMP-V1 chip.

(A) Tektronix TDS 784A [54, 55] Digitising Oscilloscope
(B) Sony/Tektronix AWG 2041 Arbitrary Waveform Generator
(C) IC-TRIPLE-100 Linear Triple Power Supply
(D) Sony/Tektronix DG 2020A Data Generator

Table D.1: Test setup equipment list for FASTSAMP-V1 chip.

in registered mode by ISP SYNARIO [64] programming system. Unused inputs are connected to ground to reduce the power consumption on device and to reduce the noise. A ceramic capacitor C_{19} serves for decoupling the power supply of the device.

To test the chip, one sequence of 65000 vectors which covers the write and read phases was repeated at infinite. One sequence consists of 50 write cycles and one read cycle. In figure D.4 is shown the vector diagram for the write phase including also the signals which are provided by GAL. One read cycle is represented in Figure D.5. For both phases each vector of the sequence was set to 32 ns.

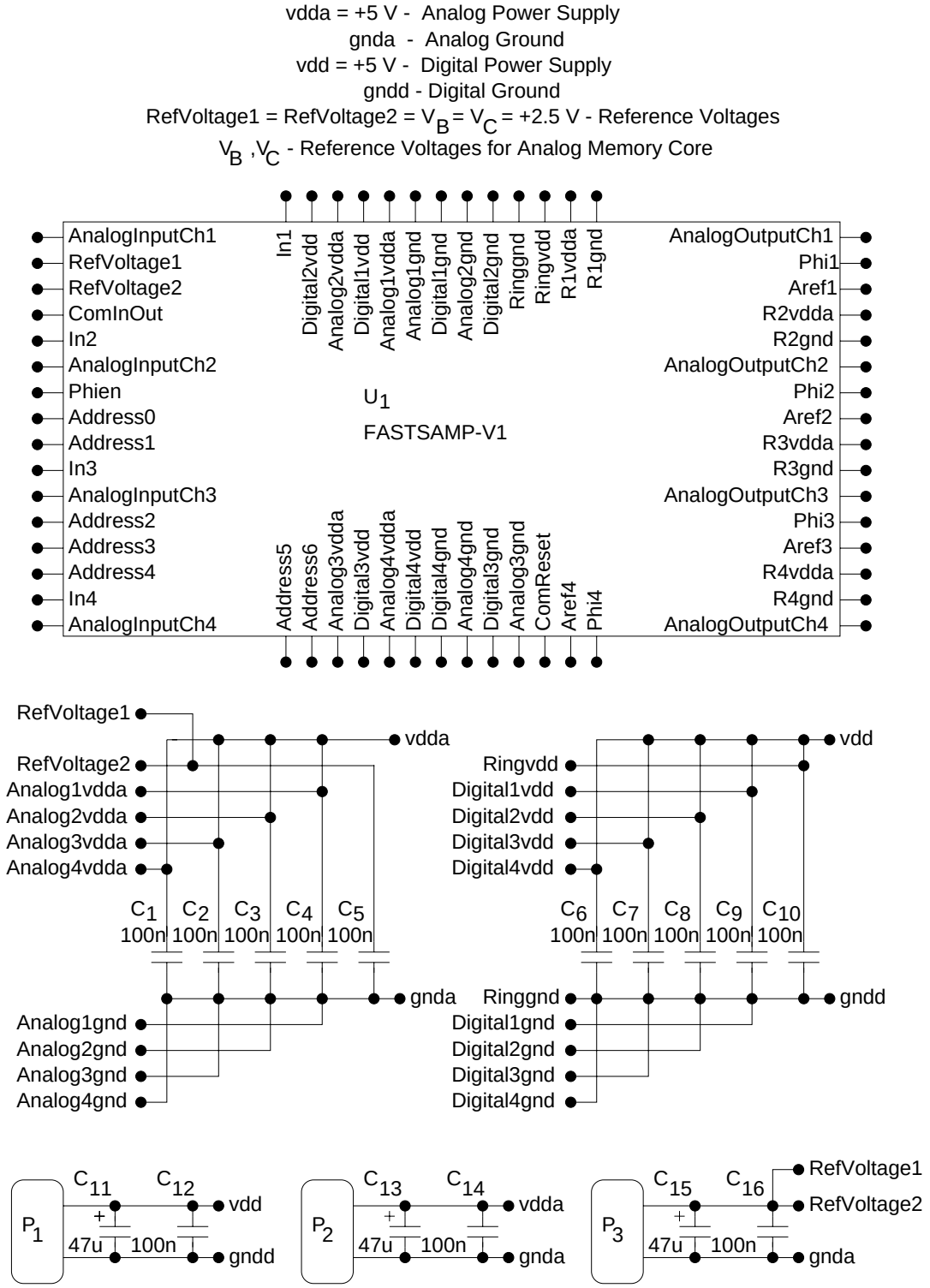

Figure D.2: Schematic of the Printed Circuit Board of FASTSAMP-V1 chip. Power supply connections.

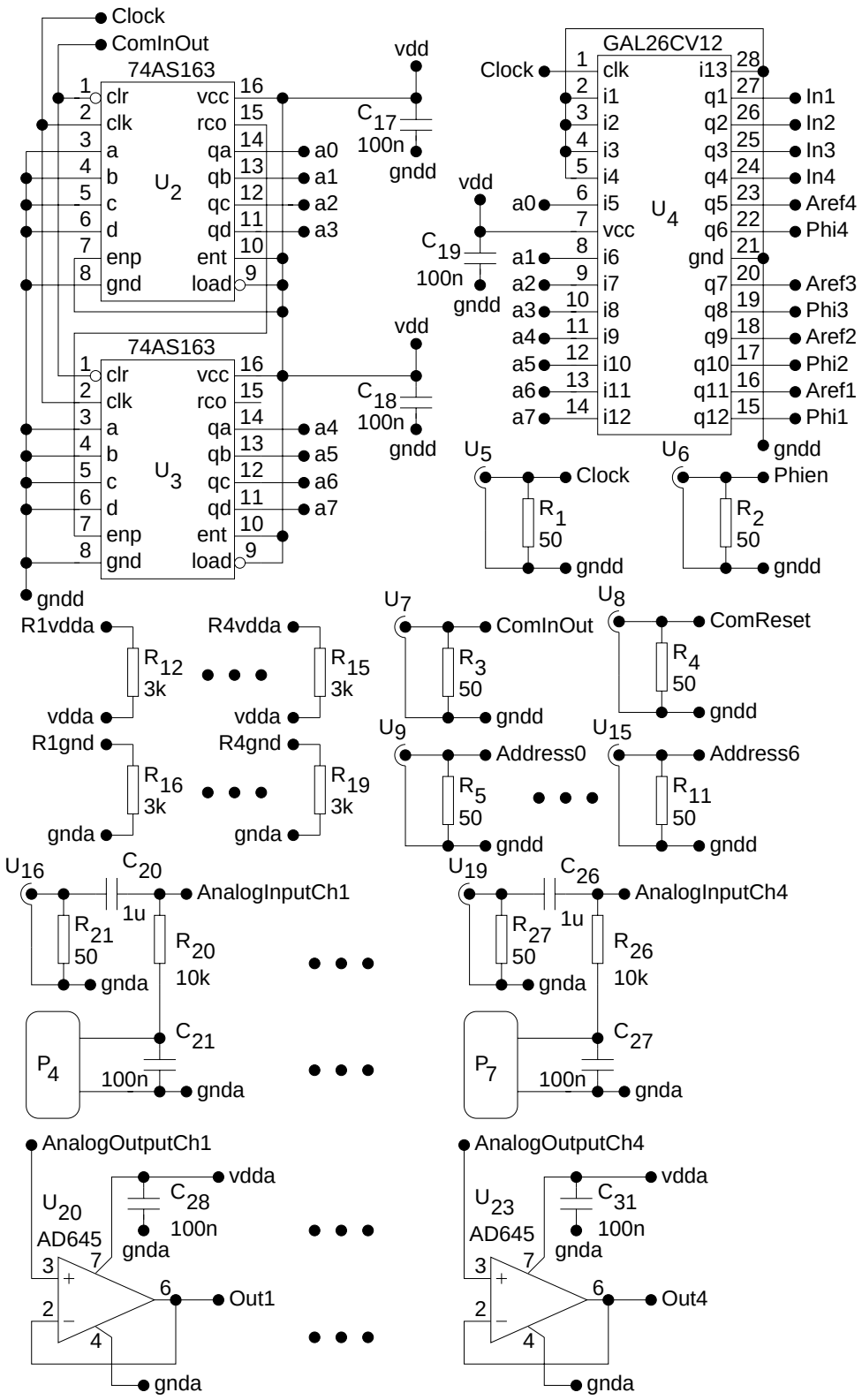

Figure D.3: Schematic of the Printed Circuit Board of FASTSAMP-V1 chip. Connections between the chip and other components.

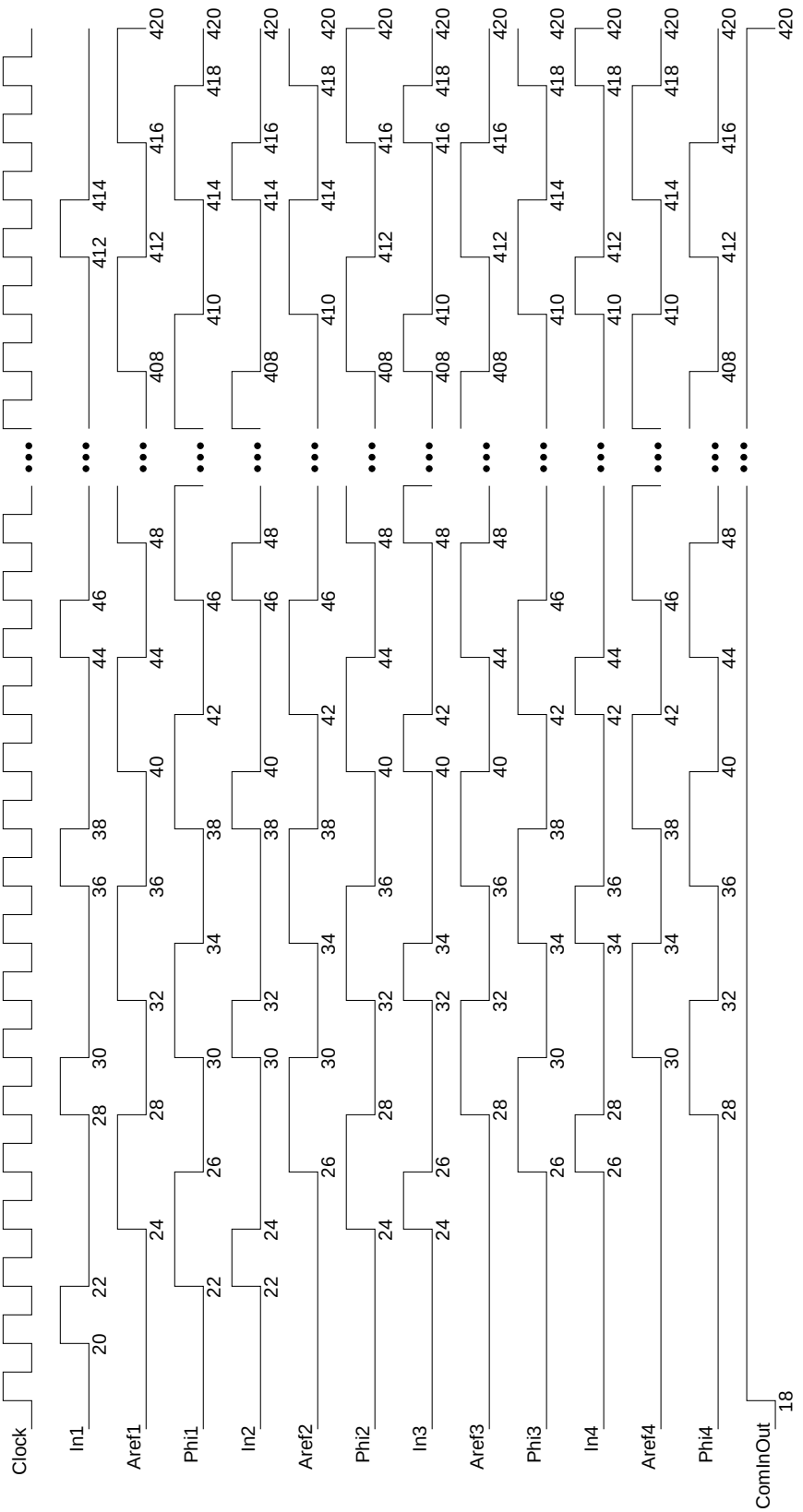

Figure D.4: Vector diagram for write phase of FASTSAMP-V1 chip.

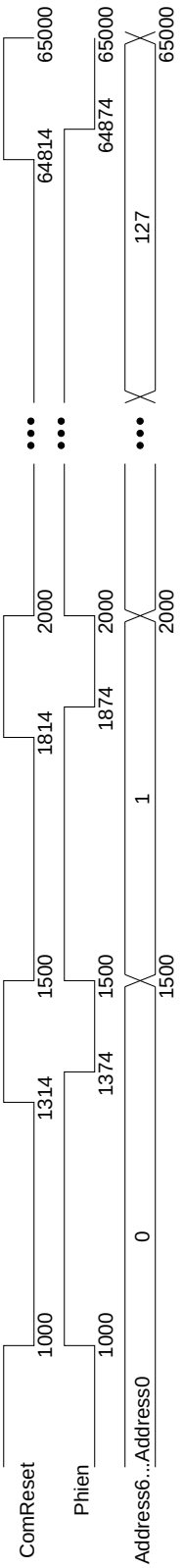

Figure D.5: Vector diagram for read phase of FASTSAMP-V1 chip.

Bibliography

[1] W. Hofmann, N. Bulian, T. Kihm, A. Kohnle, and M. Stein, "Design of Camera Electronics for HESS", Max-Planck-Institut für Kernphysik, Heidelberg, Germany, November 1998.

[2] W. Hofmann et al., "An Array of Imaging Atmospheric Cherenkov Telescopes for Stereoscopic Observation of Air Showers from Cosmic Gamma Rays in the 100 GeV Energy Range", Max-Planck-Institut für Kernphysik, Heidelberg, Germany, March 1997.

[3] R. Larsen, "Overview of the Data Acquisition Electronics System Design for the SLAC Linear Collider Detector (SLD)", *IEEE Transactions on Nuclear Science*, vol. NS-33, No. 1, pp. 65-72, February 1986.

[4] M. Pelgrom, A. Duinmaijer, and A. Welbers, "Matching Properties of MOS Transistors", *IEEE Journal of Solid State Circuits*, vol. SC-24, pp. 1433-1440, October 1989.

[5] K. Lakshmikumar, R. Hadaway, and M. Copeland, "Characterization and Modeling of Mismatch in MOS Transistors for Precision Analog Design", *IEEE Journal of Solid State Circuits*, vol. SC-21, pp. 1057-1064, December 1986.

[6] J. McCreary, "Matching Properties, and Voltage and Temperature Dependence of MOS Capacitors", *IEEE Journal of Solid State Circuits*, vol. SC-16, pp. 608-616, December 1981.

[7] J. Walker, S. Chae, S. Shapiro, and R. Larsen, "Microstore-The Stanford Analog Memory Unit", *IEEE Transactions on Nuclear Science*, vol. NS-32, No. 1, pp. 616-621, February 1985.

[8] D. Freytag and J. Walker, "Performance Report for Stanford/SLAC Microstore Analog Memory Unit", *IEEE Transactions on Nuclear Science*, vol. NS-32, No. 1, pp. 622-625, February 1985.

[9] G. Haller, D. Freytag, J. Walker, and S. Chae, "Performance Report for Stanford/SLAC Multichannel Sample and Hold Device", *IEEE Transactions on Nuclear Science*, vol. NS-33, No. 1, pp. 221-225, February 1986.

[10] E. Franchi, M. Tartagni, R. Guerrieri, and G. Baccaranie, "Random Access Analog Memory for Early Vision", *IEEE Journal of Solid State Circuits*, vol. 27, pp. 1105-1109, July 1992.

[11] K. Matsui, T. Matsuura, S. Fukasawa, Y. Izawa, Y. Toba, N. Miyake, and K. Nagasawa, "CMOS Video Filters using Switched Capacitor 14-MHz Circuits", *IEEE Journal of Solid State Circuits*, vol. SC-20, pp. 1096-1101, December 1985.

[12] D. Munday, et. al., "A 66-MHz, 32-channel Analog Memory Circuit with Data Selection for Fast Silicon Detectors", *Nuclear Instruments and Methods in Physics Research*, vol. A-326, pp. 100-111, 1993.

[13] R. Horisberger and D. Pitzl, "A Novel Readout Chip for Silicon Strip Detectors with Analog Pipeline and Digitally Controled Analog Signal Processing", *Nuclear Instruments and Methods in Physics Research*, vol. A-326, pp. 92-99, 1993.

[14] S. Kleinfelder, "Development of a Switched Capacitor Based Multi-Channel Transient Waveform Recording Integrated Circuit", *IEEE Transactions on Nuclear Science*, vol. NS-35, pp. 151-154, February 1988.

[15] S. Kleinfelder, "A 4096 Cell Switched Capacitor Analog Waveform Storage Integrated Circuit", *IEEE Transactions on Nuclear Science*, vol. NS-37, pp. 1230-1236, June 1990.

[16] W. Sippach, A. Caldwell, H. Cunitz, U. Kötz, and J. Möschen, "Development of the Front End Electronics for the ZEUS High Resolution Calorimeter", *IEEE Transactions on Nuclear Science*, vol. NS-36, pp. 465-470, February 1989.

[17] J. Möschen, A. Caldwell, L Hervas, B. Hosticka, U. Kötz, and B. Sippach, "High-Speed Analog CMOS Pipeline System", *Nuclear Instruments and Methods in Physics Research*, vol. A-288, pp. 180-186, 1990.

[18] Phillip E. Allen and Douglas R. Holberg, "CMOS Analog Circuit Design", Saunders College Publishing, 1987.

[19] Randall R. Geiger, Phillip E. Allen, and Noel R. Strader, "VLSI Design Techniques for Analog and Digital Circuits", McGraw-Hill, 1990.

[20] Kenneth R. Laker and Willy M. C. Sansen, "Design of Analog Integrated Circuits and Systems", McGraw-Hill, 1994.

[21] David A. Johns and Ken Martin, "Analog Integrated Circuit Design", John Wiley & Sons, 1997.

[22] B. Sheu and C. Hu, "Switch-Induced Error Voltage on a Switched Capacitor", *IEEE Journal of Solid State Circuits*, vol. SC-19, pp. 519-525, August 1984.

[23] G. Wegerman, E. Vittoz, and F. Rahali, "Charge Injection in Analog MOS Switches", *IEEE Journal of Solid State Circuits*, vol. SC-22, pp. 1091-1097, December 1987.

[24] J. Shieh, M. Patil, and B. Sheu, "Measurement and Analysis of Charge Injection in MOS Analog Switches", *IEEE Journal of Solid State Circuits*, vol. SC-22, pp. 277-281, April 1987.

[25] J. Kuo, R. Dutton, and B. Wooley, "MOS Pass Tranasistor Turn-Off Transient Analysis", *IEEE Transactions on Electron Devices*, vol. ED-33, pp. 1545-1555, October 1986.

[26] Gunther M. Haller, "High-speed, High Resolution Analog Waveform Sampling in VLSI Technology", Ph.D. dissertation, Stanford University, U.S.A., March 1994.

[27] Cristian Chiţu and Werner Hofmann, "High Speed Analog Memory Integrated Circuit for Cherenkov Telescopes", *Proceedings of the first IEEE Asia Pacific Conference on ASICs*, Seoul, Korea, pp. 336-339, August 1999.

[28] Cristian Chiţu and Werner Hofmann, "High Speed Analog CMOS Pipeline System for the Recording of Fast Signals from Cherenkov Telescopes", published twice in *−CD-ROM Proceedings of the 4th World Multiconference on Circuits, Systems, Communications and Computers (CSCC 2000)* , Vouliagmeni, Greece, July 2000, *−Advances in Physics, Electronics and Signal Processing Applications*, Electrical and Computer Engineering International Post-Conference Book of the World Scientific and Engineering Society Press, pp. 98-103, July 2000.

[29] P. Gray and R. Meyer, "MOS Operational Amplifier Design - A Tutorial Overview", *IEEE Journal of Solid State Circuits*, vol. SC-17, pp. 969-982, December 1982.

[30] Paul R. Gray and Robert G. Meyer, "Analysis and Design of Analog Integrated Circuits", John Wiley & Sons, 1984.

[31] R. Brodersen, P. Gray, and D. Hodges, "MOS Switched-Capacitor Filters", *Proceedings of the IEEE*, vol. 67, pp. 61-75, January 1979.

[32] W. Buttler, B. Hosticka, and G. Lutz, "Noise Filtering for Readout Electronics", *Nuclear Instruments and Methods in Physics Research*, vol. A-288, pp. 187-190, 1990.

[33] Philip R. Bevington, "Data Reduction And Error Analysis for the Phisical Sciences", McGraw-Hill, 1969.

[34] Steven W. Smith, "The Scientist and Engineer's Guide to Digital Signal Processing", California Technical Publishing, San Diego, California, U.S.A., 1999.

[35] Samuel P. Harbison and Guy L. Steele, "C a Reference Manual", Prentice Hall, 1991.

[36] B. Stroustrup, "The C++ Programming Language", Addison-Wesley, 1997.

[37] Waterloo Maple, "Maple V Release 4", Version 4.00h, Waterloo Maple, 1997.

[38] Wolfram Research, "Mathematica 4", Version Number 4.0.1.0, Wolfram Research, 1999.

[39] Austria Mikro Systeme International, "2.0-Micron, 1.2-Micron, 1.0-Micron and 0.8-Micron Standard Cell Databook", Austria Mikro Systeme International AG, Austria, 1995.

[40] Austria Mikro Systeme International, "0.8 μm CMOS Process Parameters", Document No. 9933006, Revision B, Austria Mikro Systeme International AG, Austria, 1997.

[41] Austria Mikro Systeme International, "0.8 μm CMOS Design Rules", Document No. 9931015, Revision B, Austria Mikro Systeme International AG, Austria, 1997.

[42] Austria Mikro Systeme International, "0.8 μm Analogue Standard Cells (CYE Datasheets), OP01B operational amplifier", Hit-Kit version 3.01, Austria Mikro Systeme International AG, Austria, 1997.

[43] Cadence Design Systems, "Analog Artist Simulation Help - Release 4.4.1", Cadence Design Systems, San Jose, CA 95134, U.S.A., 1997.

[44] Cadence Design Systems, "Cadence SPICE^{TM} Reference Manual", Product Version 4.4, Cadence Design Systems, San Jose, CA 95134, U.S.A., 1995.

[45] Cadence Design Systems, "Spectre Reference", Product Version 4.4.1, Cadence Design Systems, San Jose, CA 95134, U.S.A., 1997.

[46] Cadence Design Systems, "HSPICE/SPICE^{TM} Interface & SPICE^{TM}2G6 Reference Manual", Product Version 4.1, Cadence Design Systems, San Jose, CA 95134, U.S.A., 1990.

[47] Cadence Design Systems, "Composer Tutorial 4.4", Cadence Design Systems, San Jose, CA 95134, U.S.A., 1997.

[48] Cadence Design Systems, "Virtuoso Layout Editor Help - Release 4.4.1", Cadence Design Systems, San Jose, CA 95134, U.S.A., 1997.

[49] Cadence Design Systems, "Concept Schematic User Guide 3.0", Cadence Design Systems, San Jose, CA 95134, U.S.A., 1997.

[50] Cadence Design Systems, "RapidPart User Guide 2.2", Cadence Design Systems, San Jose, CA 95134, U.S.A., 1997.

[51] Cadence Design Systems, "Allegro Designer User Guide 12.0", Cadence Design Systems, San Jose, CA 95134, U.S.A., 1997.

[52] IEEE, "GPIB, ANSI/IEEE 488 Codes, Formats and Protocols", IEEE, New York, U.S.A..

[53] Tektronix, "Tektronix TDS 420A, TDS 430A, TDS 460A and TDS 510A, Digitizing Oscilloscopes", 070-9758-00, Tektronix Corporation, U.S.A., 1995.

[54] Tektronix, "Tektronix TDS 620B, TDS 644B, TDS 680B, TDS 684B, TDS 744A, & TDS 784A, Digitizing Oscilloscopes", 070-9382-00, Tektronix Corporation, U.S.A., 1995.

[55] Tektronix, "Programmer Manual for TDS Family Digitizing Oscilloscopes (TDS 410A, 420A, 460A, 520A, 524A, 540A, 544A, 620B, 644B, 680B, 684B, 744A & 784A)", 070-9385-00, Tektronix Corporation, U.S.A., 1995.

[56] Hewlett Packard, "HP 82000 IC Evaluation System, Standard Test Function Reference", HP Part No. E180-90205, Hewlett-Packard Company, U.S.A., November 1993.

[57] Sony/Tektronix, "User Manual for AWG 2041 Arbitrary Waveform Generator", Sony Tektronix Corporation, U.S.A., 1995.

[58] Robert Helsel, "Visual Programming with HP VEE", Hewlett-Packard Company, Prentice Hall PTR, U.S.A., 1997.

[59] Analog Devices, "Low Noise, Low Drift FET Op Amp AD645", Analog Devices Corporation, U.S.A., 1996.

[60] Sony/Tektronix, "User Manual for DG 2020A Data Generator with P3410 & P3420 Pods", Sony Tektronix Corporation, U.S.A., 1994.

[61] Texas Instruments, "SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163, SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163 Synchronous 4-Bit Decade and Binary Counters", Texas Instruments Corporation, U.S.A., 1994.

[62] Lattice Semiconductor Corporation, "GAL26CV12 High Performance E^2CMOS PLD Generic Array Logic™", Lattice Semiconductor Corporation, U.S.A., 1997.

[63] Lattice Semiconductor Corporation, "ABEL-HDL Reference Manual", Version 7.0, Lattice Semiconductor Corporation, U.S.A., 1998.

[64] Data I/O Corporation, "ISP™ Synario System", 1993-1994 Data I/O Corporation, Redmont, Washington, U.S.A..