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Investigations in radiation hard electronics

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Untersuchung an strahlenharter Elektronik: Es wurden Bestrahlungstests an Teststrukturen (einzelnen Transistoren von verschiedener Größe und Form) durchgeführt, die im 0,6µm-Prozeß von AMS hergestellt wurden, um die Strahlenhärte dieses Prozesses, insbesondere im Hinblick auf die Anforderungen der LHC*b* und HERA-B Detektoren sowie den Einfluß des geschlossenen (*edgeless*) Transistor-Designs auf die Strahlenhärte zu untersuchen. Die Teststrukturen wurden bis 10 kGy in Schritten von 900 Gy bestrahlt. Die Parameter, die gemessen wurden, waren die Schwellenspannung V_{T0}, der Verstärkungsfaktor KP und der Leckstrom. Die Meßverfahren wurden nach den Angaben von AMS [1, Kap. 3.1] durchgeführt. Die Ergebnisse lassen den Schluß zu, daß der AMS-Prozeß eine wesentlich geringere Strahlenhärte als moderne 0,25 µm-Prozesse besitzt und nicht den maximalen Anforderungen von 2 Mrad pro Jahr von LHC*b* genügen würde. Allerdings ist er generell für mittlere Anforderungen an Strahlenhärte geeignet, wie z. B. denjenigen von HERA-B von 200 krad pro Jahr. Das geschlossene Transistordesign reduziert den Leckstrom deutlich, wie vorhergesagt (siehe die Abschnitte 3.2 und 3.5). Ein Einfluß der Verpackungsmethode auf den Leckstrom wurde festgestellt. Schließlich wurden Teststrukturen im 0.25 µm-Prozeß von IBM entworfen und submittiert.

Abstract. Irradiation tests were performed on teststructures (single transistors of different size and type) in the 0.6 µm-process from AMS, to investigate the radiation hardness of this process, in particular with respect to the requirements of the LHC*b* and HERA-B detectors, and the impact of the edgeless design on radiation hardness. The teststructures were irradiated up to 10 kGy, in steps of 900 Gy. The values measured were the threshold voltage V_{T0}, the slope—of which the gain factor K' was computed—and the leakage current. Setup of the measurements for V_{T0} and the gain factor were as given by AMS [1, Note 3.1]. The results indicate that the AMS process is clearly inferior to modern deep submicron processes in terms of radiation hardness, and would not stand the maximum requirement of 2 Mrad per year at LHC*b*. However, the overall performance seems adequate for lower radiation hardness requirements, e. g., those of HERA-B (200 krad per year). The edgeless design does reduce the leakage current as supposed (see Sects. 3.2 and 3.5). The method of packaging was found to influence the leakage current. Another set of teststructures was designed in the IBM 0.25 µm-process and submitted.

Contents

Chapter 1

High energy physics experiments

To show the motivation for irradiation tests and radiation hard integrated circuits, a modern experiment will be discussed in detail. Then comparisons to earlier experiments will be made to show general trends in integrating electronics for high energy physics (HEP) experiments.

1.1 The LHC*b* experiment

LHC*b* is an experiment to precisely measure CP-violation and rare decays in the B-meson system [17, 18] (see Fig. 1.1). It is conducted at the large hadron collider (LHC) at CERN, Geneva. Elements of the detector include the *vertex detector*, the *ring-imaging Cherenkov (RICH) detector*, the *tracking system* and the *calorimeter*. Of these, the vertex detector and the tracking system will be described in more detail, since they pose the strictest requirements regarding radiation hardness. Data coming from the detectors are filtered by a set of triggers, Level-0–Level-3, to reduce the data rate and storage requirements. Level-0 is the foremost trigger level, integrated in the frontend electronics (FEE). The projected luminosity of LHC is $2 \cdot 10^{32}\ \mathrm{cm}^{-2}\,\mathrm{s}^{-1}$. The minimum distance of the FEE to the beam interaction point of approx. 6 cm, leads to an expected radiation dose of 2 Mrad per year.

The vertex detector is used to measure the tracks (vertices) of produced and decayed B-hadrons; it comprises the actual silicon vertex detector and a pile-up veto counter. The silicon vertex detector consists of several discs of silicon strip detectors in which ionizing particles create charges on the strips. Each disc is fitted with both circular and radial strips, on which the FEE for the Level-0 buffer is mounted at a distance of approx. 6 cm from the beam axis. The strips of the detector are directly bonded to the readout electronics. The veto counter data are evaluated by the trigger to decide for each event if data transmit should be triggered, while the event data are stored in a pipeline on the readout chip for a time equal to the latency of the trigger algorithm. Data are released upon receiving the trigger signal.

The tracking system provides data for the reconstruction and momentum measurement of charged particle tracks, as well as directional data for the RICH detector and trigger data for the Level-1 trigger. It consists of the inner and outer tracker, the distinction being made because of the different technologies used, since particle fluxes are higher for the inner tracker. The inner tracker consists of microstrip cathode chambers

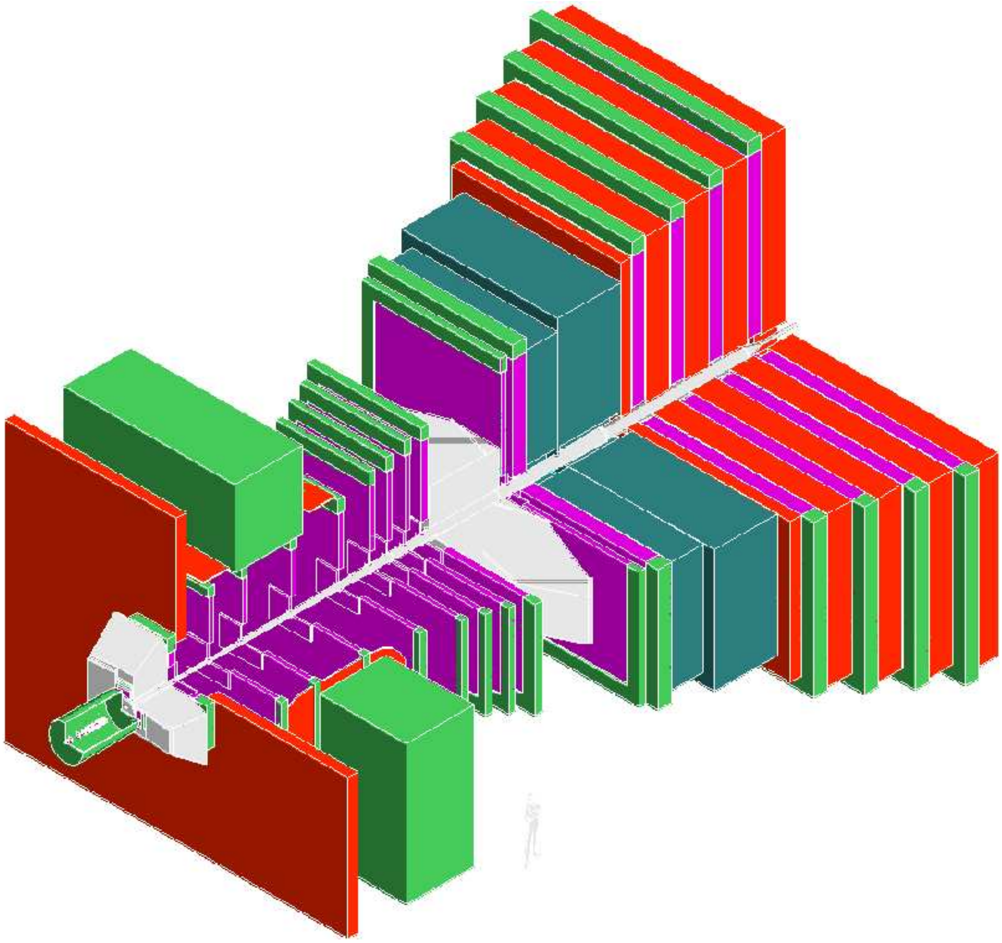


Figure 1.1: A 3D view of the LHCb detector, taken from [18]

(MSCC), with readout electronic chips mounted on the modules. The outer tracker consists of honeycomb-chambers, also equipped with readout electronics.

1.2 Comparison to earlier experiments

An earlier experiment for particle physics in the b-system is HERA-B, conducted at the Hadron-Elektron-Ringanlage* (HERA) at DESY, Hamburg. While LHCb will do precision measurements of CP violation, HERA-B was designed to search for CP violation and to investigate other physics topics. It has elements similar to the LHCb. However, there is a difference concerning the integration of electronics into the detector. In HERA-B, the nearest distance of FEE to the beam is approx. 31 cm, which leads to an expected radiation dose of approx. 200 krad per year, assuming a luminosity of approx. $6 \cdot 10^{30}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$.

One can see from these numbers that there is a tendency for electronics in HEP experiments to be moved nearer to the actual detectors (to the point of being integrated on

*Hadron electron ring unit

the detector) and thus, nearer to the interaction region, with an accompanying higher radiation rate. Since the particles to be investigated become heavier and their production cross sections smaller, one needs to have high energy and luminosity to obtain good statistics on the processes. The increased luminosity leads to a higher data rate, which means that data from the detector have to be read out faster, so the latency for the first trigger levels decreases (first-level trigger latency in HERA-B 10 µs, Level-0 trigger latency in LHC*b* 4 µs). Additionally, the bunch crossing frequency increases (HERA-B 10 MHz, LHC*b* 40 MHz), again imposing limits on the latency of the triggers. The data cannot be transmitted to an outside trigger because of cable length delays, so the trigger must be located in the detector. Another problem is that the resolution of detectors increases, which leads to an increase in the number of channels (HERA-B vertex detector 175 000, LHC*b* vertex detector 222 000). The number of channels would require the same number of cables to be routed outside (which is not possible for lack of space), so there has to be a trigger electronic on or near the detector, to reduce the number of channels routed outside. The nearer the FEE to the detector, however, the higher the total dose accumulated over time, so there is an increasing requirement on the radiation hardness of the electronics.

Chapter 2

MOSFET fabrication and functionality

2.1 The CMOS process

The most widely used process for fabricating integrated circuits today is the *CMOS process* for digital and analogue circuits. It derives its name from the requirement to integrate both N- and PMOS on the same wafer to be able to produce *combined N- and PMOS* (CMOS) circuits. Advantages of the CMOS technology include compact size, low power dissipation and good linearity. Most microprocessors used in computers are produced in the CMOS process.

The fabrication of an integrated circuit starts with a single crystal of ultra-high-purity silicon, a cylinder with a diameter of approx. 200 mm and a length of approx. 1 m. Depending on the exact process specifications desired, the silicon cylinder can also be *doped*, i. e., impurities of donor- or acceptor-like nature can be added to the silicon to change its electrical properties, especially resistivity. One distinguishes between n- (e. g., Phosphorus or Arsen) and p-doping (e. g., Boron), corresponding to electron-donors and -acceptors, respectively. The cylinder is then sawed to get thin discs called *wafers*.

In the process that follows, the wafers can be subjected to six different fabrication steps, described below (see also [19, 20]).

Oxidation: The wafer is exposed to an atmosphere of either high-purity oxygen or water vapor, at a temperature of approx. 1000 °C, so that an isolating layer of SiO_2 grows on the surface. This layer can be used for the field oxide, the gate oxide, as a dielectric for capacitors, for isolation of the whole chip or for masking of underlying structures from following process steps.

Diffusion: Impurities are being introduced into the silicon to change its doping. This is done by first exposing the wafer to an atmosphere containing the desired impurity, thus depositing a layer of the impurity on the wafer; this is called pre-deposition. Then, the wafer is heated to a certain temperature (normally around 1000 °C) to let the impurities diffuse into the wafer; this is called drive-in. The resulting density profile of impurities in the bulk is strongly dependent on both the temperature and duration of the drive-in.

Ion implantation: This is another method of introducing impurities into the silicon. The desired impurities are, as ions, accelerated towards the surface by an electric field, and become embedded into the silicon. The depth of penetration and the number of ions can be accurately controlled via the field and current of the ion source, respectively. This process is much more precise than diffusion, and can be done at room temperature. Also, it can deposit an impurity profile under a surface. However, the impurities introduce defects in the crystal lattice, which must be healed out by heating the wafer.

Deposition: With this process, materials are deposited on the surface of the wafer. There are different types of this process: *Chemical vapor deposition* (CVD) is used to deposit polycristalline silicon (polysilicon), Si_3N_4 or SiO_2 on the surface, by exposing the wafer to an atmosphere of silane (SiH_4), ammonium (NH_3) or a mixture of oxygen and silane, respectively. A chemical reaction takes place in the gas phase. *Epitaxy* is similar to CVD, but the wafer is exposed to silane at a temperature of approx. $1000\,^{\circ}C$. This way, a singlecrystalline layer of silicon grows on the surface. *Vacuum deposition* involves heating a solid above the cooler wafer, so that hot vapor is deposited on the surface. This is mostly used for metallisation. *Sputtering* is done by shooting with positive ions at a cathode coated with the material to be deposited, so that the material is released from the surface and deposited on the wafer, which is connected to the anode.

Etching: This process is used to etch away material on certain areas. To this end, the wafer is exposed to acidic fluid chemicals such as HF or H_3PO_4 for wet etching, or to ionized gases for plasma etching. Etching is strongly connected to photolithography, to define areas to be processed in another step.

Photolithography: To define the areas to be etched and processed, the wafer is coated with a photosensitive layer and then exposed to light through a mask with the layout for the areas. This leaves the layer on either the exposed (negative lacquer) or unexposed (positive lacquer) areas after development, and prepares the wafer for subsequent etching of the areas not protected by the lacquer.

The actual fabrication process is a combination of these steps in sequence, with as many as fifty steps required for a modern chip. The process steps themselves being quite difficult to control, there are a lot of factors (unknown to or uncontrollable by the designer) introduced into the design of electronic circuits. Another important consideration is the limited precision of the fabrication process. Etching always etches away more than defined by the mask, and the layers produced by deposition or oxidation do not fall off sharply at the edges, but with a finite slope, which causes noticeable effects on the behaviour of the devices. For example, the leakage current described in Sect. 3.5 is caused solely by the blurred edges of the field oxide growing partly over the diffusion area, and those of the diffusion partly extending under the field oxide.

2.2 MOSFET operation

The metal–oxide–silicon field effect transistor (MOSFET) is the basic component of the CMOS technology, and will now be described in more detail.

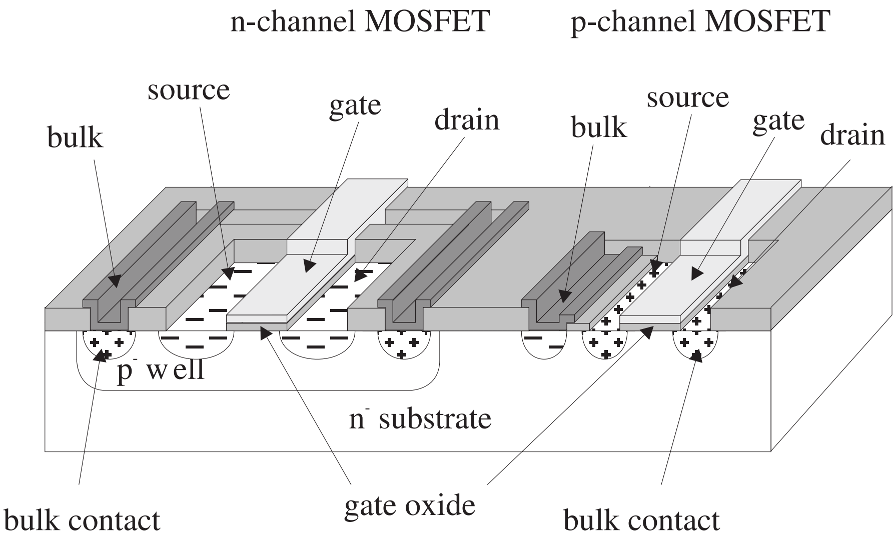


Figure 2.1: NMOS and PMOS in an n-well technology. Taken from [20]

As its name implies, the MOSFET consists of a metal contact* called *gate* over a thin (12 nm for an 0.8 µm-process) oxide layer called *gate oxide*, which rests on the silicon wafer itself (the *bulk* or *substrate*). To both sides of the gate, heavily doped regions called *drain* and *source* lie in the bulk which are also contacts (cf. Fig. 2.1). The region between drain and source is called *channel region* for reasons explained below. There are two types of MOSFETS, dependent on the type of majority charge carrier. An NMOS has a p-doped channel, with drain and source being n^+-doped, while a PMOS has an n-doped channel, with drain and source being p^+-doped. The upper index $^+$ denotes heavy doping of the given type. Since the bulk is either n- or p-doped, one type of MOSFET has to be put into a well of a doping opposite to the bulk's to allow for both types on one chip. Because of the thin gate oxide, MOSFETs are very sensitive to high gate voltages from, e. g., electrostatic discharge (ESD), so the gate inputs need to be shielded with protection diodes. W/L, the ratio of the width W of the channel region against its length L when looked at from above, is the single most important layout parameter for integrated circuits, since it determines the conductivity of the transistor and is the only parameter normally controllable by the designer. An important process dependent parameter is the gain factor K', which also determines the conductivity (see Eq. 2.1).

In the following, the behaviour of an NMOS with different applied voltages will be described. If all contacts of the NMOS (gate, source, drain, bulk) are on the same potential, the pn-junctions of both drain and source to bulk build up a depletion region. This leads to a very high drain–source resistivity, and no current flows (besides the leakage current). Increasing the gate–source voltage v_{GS} leads to the accumulation of positive charges on the gate, with corresponding accumulation of negative charges in the region under the gate, which neutralize the holes in the p-doped bulk; this effect is called *weak inversion*. (Since the gate oxide is an isolator, gate, oxide and bulk act as a capacitance.) If v_{GS} is further increased over a certain value called *threshold voltage*

*Nowadays, the gate contact consists of polysilicon rather than metal

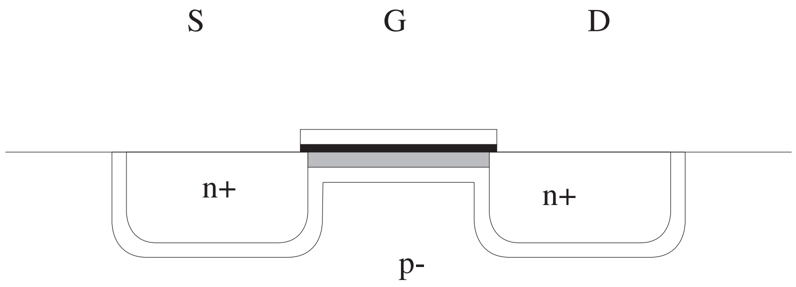


Figure 2.2: NMOS with gate voltage greater than the threshold voltage. Note the channel under the gate. Taken from [20]

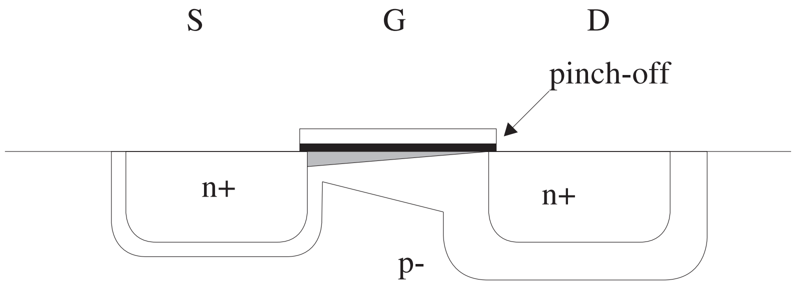


Figure 2.3: NMOS with the drain–source voltage greater than the pinch-off voltage. Taken from [20]

V_{T0}, there are free electrons in the region under the gate, as all holes have already been neutralized; this effect is called *strong inversion* (cf. Fig. 2.2). The electrons now form a channel from source to drain, so that a drain–source current i_{DS} can flow:

$$i_d = \beta[v_{GS} - V_{T0}]^2 , \quad \text{where } \beta = K' \left(\frac{W}{L}\right)_{\text{eff}} = \frac{\mu C_{OX}}{2} \left(\frac{W}{L}\right)_{\text{eff}} , \tag{2.1}$$

where μ is the mobility of the majority charge carriers and C_{OX} is the capacitance of the gate. $(W/L)_{\text{eff}}$ denotes the *effective* W/L. It takes into account influences of the process on the geometry of the transistor. See also Sects. 2.1, 4.4.1 and 4.4.2.

This channel is not uniform, but gets thinner in direction of the drain region, depending on the drain–source voltage v_{DS}. If v_{DS} is increased over a certain value called *pinch-off voltage* $V_P = v_{GS} - V_T$, the channel is pinched off before reaching the drain region. The region between the end of the channel and the drain region is devoid of charge carriers of any kind, and the current i_{DS} becomes independent of the drain–source voltage (cf. Fig. 2.3).

Chapter 3

Effects of ionizing radiation

3.1 Introduction

In the LHCb experiment, some parts of the electronics are very near to the beam channel (as close as 6 cm), which gives rise to a high buildup of radiation dose, mainly due to γ-rays; the total dose on the electronic components is expected to be as high as 2 Mrad (= 20 kGy) accumulated over one year. This poses new problems for designing integrated circuits, since total doses in this order of magnitude have never before been a practical issue. (Consider, e.g., that the military calls a device "radiation hard" if it continues to function up to 100 krad.)

The observable effects of ionizing electromagnetic (EM) radiation on MOSFETs include (see [4, 5, 6]):

Single event upset (SEU): A spontaneous change in the state of a transistor due to additional charge-carriers created by the ionizing radiation leads to a wrong output, which can be reset.

Single event latchup (SEL): A spontaneous change in the state of a transistor leads to the emergence of parasitic currents, which destroy the circuit.

Threshold voltage shift: Charge-carriers trapped in the gate oxide lead to a negative shift in the threshold voltage, while interface traps at the gate–channel interface (the Si/SiO_2 junction below the gate oxide) cause a positive or negative shift of the threshold voltage in N- or PMOS, respectively.

Gain factor/mobility shift: Interface traps at the Si/SiO_2 junction below the gate oxide cause a degradation of the mobility of charge-carriers in the channel, and thus a shift in the gain factor K'.

Leakage current increase: Ionizing radiation also produces charge carriers in the field oxide beside the gate oxide, which increase the conductivity of the path from source to drain alongside the gate for an NMOS, thereby increasing the leakage current.

Of these effects, only threshold voltage shift, gain factor shift and leakage current increase are considered in this thesis and will be discussed in more detail, since SEU and SEL are more a problem of complete circuits. These effects apply mainly to EM

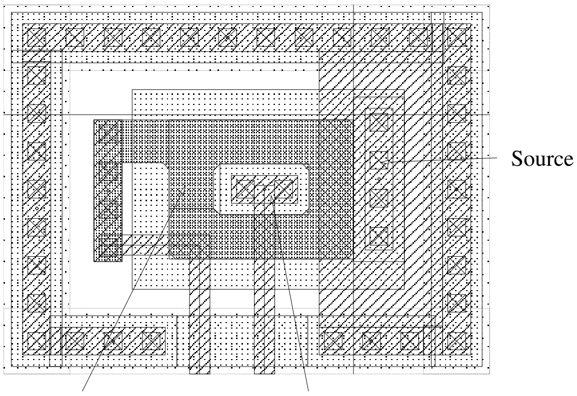


Figure 3.1: Layout of an edgeless transistor. Drain is encircled by gate

radiation, and will only be discussed with respect to such radiation. There are other effects for other types of radiation, which will not be discussed here.

3.2 Radiation hard design

Some, but not all, effects of ionizing radiation can be dealt with by obeying certain rules in the design process. On the other hand, there are already production processes available which are intrinsically radiation hard, e.g., the DMILL process or the various deep sub-micron processes. Since these processes are expensive and pose other problems, one would prefer to be able to design radiation hard electronics in a standard, well-defined (from an analogue point of view) process like the 0.6 µm-process from AMS. Radiation hardness must then be achieved on the design level.

One proposal to obtain a radiation hard design is the enclosed structure, or *edgeless*, transistor. In this design, the gate forms a doughnut shape, encircling the drain and itself being encircled by the source, as shown in Fig. 3.1. This prevents the buildup of a path from source to drain alongside the gate and thus the increase in leakage current that would otherwise result.

3.3 Gate oxide trapped charges

Ionizing radiation passing through the oxide region creates electron/hole pairs. Since the electrons created are much more mobile than the holes (by a factor of approx. 10^{11} [6]), they are swept out of the oxide region in a short time (in the order of ps), while the holes drift more slowly. Is is possible for electrons and holes to recombine before the electrons are swept out. The amount of recombination depends on the applied field (viz. the gate voltage) as well as the energy of the radiation. Due to the small time scale, recombination is of minor importance in the gate oxide. Since the electrons are swept out in a short time, and their trapping rate in SiO_2 is several orders of magnitude lower than the holes', their contribution to trapped charge radiation effects can be neglected.

After recombination has taken place, the holes drift in the direction of the applied field (either to the gate surface or to the gate–channel border, for negative or positive bias, respectively) until they are captured in oxide traps or drift out of the gate oxide and recombine in the silicon or the polysilicon (see Fig. 3.2). The holes are trapped very near the respective surface, in the order of a few nm, since the trap precursors themselves are concentrated near the surfaces. The cause for the location of the traps at the surfaces lies in their nature as strained chemical bonds, as described in the following.

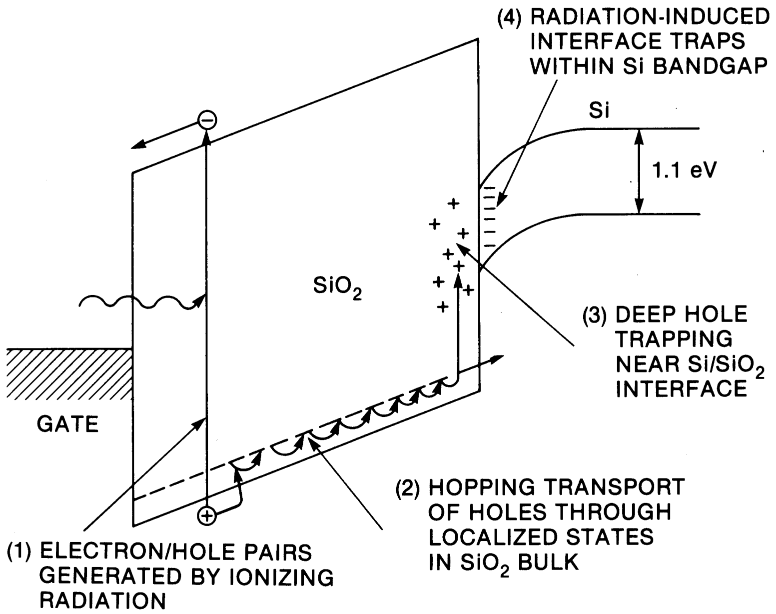


Figure 3.2: Microscopic view on the processes involved in effects of ionizing radiation in the gate oxide. Taken from [6]

The transition from Si to SiO_2 at the interface occurs within one atom layer. However, on both sides of the transition layer, there is a thin (1–4 nm [6]) region where atomic bonds are strained because the crystal lattice has to reorientate itself from the oxide to the channel. This leads, e. g., to a reduction of the normal 144° angle of the SiO_2 network to just 120°, and thus to a weakening of the Si–O bonds in the gate oxide, as well as to the formation of strained Si−Si bonds without oxygen in between, called *oxygen vacancies*. These vacancies serve as traps for the holes diffusing to the surfaces. This also explains the decreased radiation hardness of devices exposed to high temperature annealing after gate oxidation which allows the defects in the lattice to heal, but increases the number of oxygen vacancies [16].

Before irradiation, one has two $Si{\equiv}O_3$ (trivalent silicons) bonded symmetrically by one Si sp^3 orbital each, with both $Si{\equiv}$ stretched out of the plane of the oxygens. The trapping of a hole leads to its recombination with one of the electrons (breaking the bond) and the relaxation of the corresponding Si into the plane of its oxygens, while the other retains its now unpaired electron (see Fig. 3.3). The relaxed structure is positively charged, and so accounts for the effect of the threshold voltage shift. This asymmetrically relaxed oxygen vacancy is called an E'_γ *center* (see Fig. 3.4a). It is the dominant form of the E' centers responsible for the radiation effects on MOSFETs. Other forms include the E'_δ center, which is not stable, and subject to either annihilation (by recombination with tunneling electrons) or transfer of its trapped hole to an E'_γ precursor (a strained Si$-$Si bond), since the potential well of the E'_δ center is less deep than that of the E'_γ [16]. The cross section for recombination is much larger for the E'_δ than for the E'_γ center, so most of the E'_δ centers are annihilated in an ionizing radiation experiment (as opposed to a hole injection experiment, where no electrons are created).

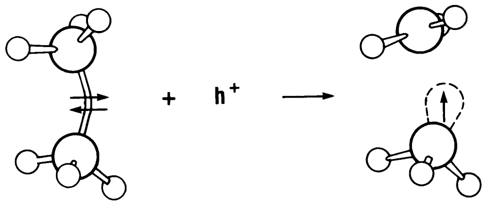


Figure 3.3: Conversion of an oxygen vacancy to an E'_γ center

For very thin gate oxides ($< 10\,\mathrm{nm}$), the number of trapped holes becomes negligible, because electrons have a reasonable probability to tunnel from the channel into the oxide, recombining with the trapped holes and thus eliminating the E' centers. This is the reason why modern deep sub-micron processes are expected to be intrinsically radiation hard; threshold voltage shifts are small even for high doses [10].

The effect of the trapped holes on the behaviour of a transistor is that they act as a positive applied voltage. Since this makes NMOS "easier to turn on" and PMOS "harder to turn on", it can effectively be described as a negative shift of the threshold voltage (the voltage required to build up a conducting channel under the gate oxide) for both N- and PMOS. Since the number of trapped holes increases with the total dose, the threshold voltage decreases with total dose. For the NMOS, this means that it may even reach a negative threshold voltage (and thus, be permanently turned on), while for the PMOS that the threshold voltage gets even more negative. The buildup of hole traps reaches saturation for high doses, dependent on the process characteristics and irradiation conditions [6].

3.4 Gate–channel interface traps

While the structure and creation of gate oxide traps is fairly well understood, there is still some uncertainty about the stucture and creation of interface traps. Thus, the following explanation of interface trap generation and their structure is to be taken *cum grano salis*, since there are different, even contradictory, models, and no theory exists that sufficiently describes all phenomena related to interface traps; neither do the models.

The interface traps are located directly at the transition region from Si to SiO_2 mentioned before, also related to the existence of strained bonds. In their creation,

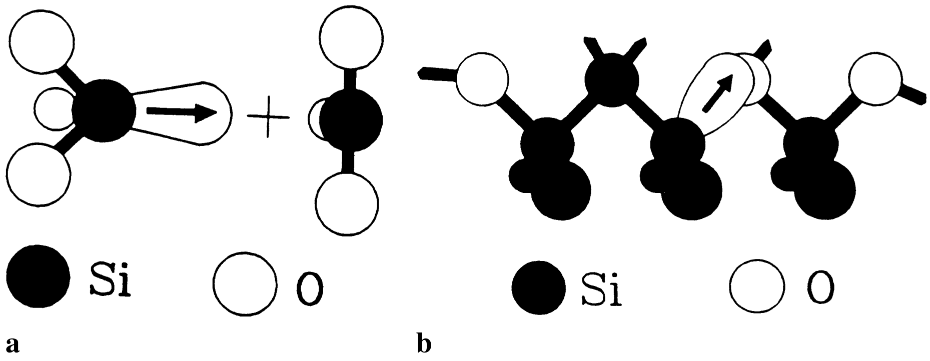


Figure 3.4: **a** E'_γ center and **b** P_{b0} center. Taken from [13]

there seems to be a link to the E' centers; according to Conley and Lenehan [12], it was discovered that ionizing radiation creates atomic hydrogen (thus called *radiolytic* atomic hydrogen), which dimerizes quickly to molecular hydrogen H_2. In their model, this molecular H_2 then reacts with E'-center-like defects to either a 74 G center (a silicon bonded to two oxygens and one hydrogen, as $\mathrm{Si}\equiv\mathrm{O}_2\mathrm{H}$) or a 10.4 G center (a silicon bonded to three oxygens, of which one is in turn bonded to a hydrogen), both of which have been experimentally verified. This releases a form of hydrogen which moves to the surface, where it breaks weak Si−Si bonds, creating Si−H bonds, which are generally assumed to be the precursors to P_b centers. The "dangling bonds" of the E' centers (i. e., the unpaired electrons) then react with the P_bH to create the P_b centers [13]. They do not, however, specify what the intermediate hydrogen exactly looks like, nor in what way the "dangling bonds" and the P_b centers interact. They claim a good agreement between their model and results from their own as well as others experiments'. In another model from Warren et al. [16], both E' and P_b precursors are created by the diffusion of oxygen from SiO_2 to the Si layer, leaving behind strained Si−Si bonds, which directly serve as the precursors to E' and P_b centers if they are located in the oxide or at the interface, respectively. Note that in this model, strained Si−Si bonds are assumed to be the direct precursors to the P_b centers, not Si−H bonds, so there is no difference between E' and P_b centers save the location. Additionally, their model takes into account a distinction between two components of interface trap buildup. *Fast buildup* is the generation of interface traps from strained Si−Si bonds immediately after irradiation, while *slow buildup* is a proposed reaction of radiolytic hydrogen with Si−H bonds. These different types of buildup have also been observed in experiments and are described in the literature [6].

Concerning the structure, there is a consensus that generally the interface trap is an interface silicon with an unpaired electron, called P_b center. There are two variants of the interface trap (see Fig. 3.5):

- The P_{b0} center, known to be a silicon bonded to three other silicons [13], as $\dot{\mathrm{Si}}\equiv\mathrm{Si}_3$ (see Fig. 3.4b).
- The P_{b1} center, whose structure is not exactly known, but which is presumed to be a silicon bonded to two other silicons and an oxygen [11], as $\dot{\mathrm{Si}}\equiv\mathrm{Si}_2\mathrm{O}$.

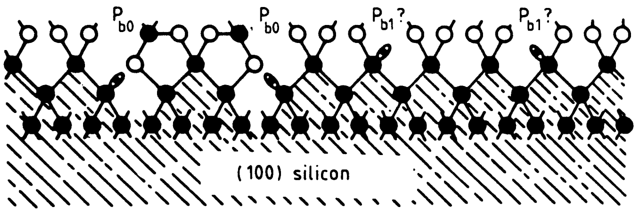


Figure 3.5: Si/SiO_2 interface with P_{b0} and P_{b1} centers. *Hollow circles* ◦ are oxygen, *filled circles* • are silicon. Taken from [11]

Both of these variants are observed in two chemically equivalent orientations [11].

Interface traps have an effect on both the threshold voltage and the channel mobility. The effect on the threshold voltage is dependent on the type of transistor, with a positive or negative shift for NMOS or PMOS, respectively, in addition to the negative shift caused by trapped oxide holes. This may, for the NMOS, lead to the phenomenon known as *rebound*, where the negative threshold voltage shift is compensated and the threshold voltage even rises above its initial value, because the number of interface traps saturates at a higher dose than the number of trapped holes [6]. The reason for the different effect on N- and PMOS lies in the structure of the energy levels of the P_b centers in the Si bandgap. The P_b center has two broad levels above and below midgap [13], which correspond to the existence of both acceptor- and donor-like traps, respectively. For PMOS, the Fermi-level ε_F is below midgap, so that the acceptor-like traps are neutral and the donor-like positive; so one has an additional positive charge at the interface. For NMOS, ε_F is above midgap, so the acceptor-like traps are negative and the donor-like neutral; this results in a negative charge at the interface. Obviously, the neutral traps do not contribute to the threshold voltage shift in either case.

Interface traps exhibit the same effect as trapped holes for thin oxides, in that transistors fabricated in a deep sub-micron process show only a very small threshold voltage shift, even for high doses [10]. This might be explained with the model of Conley and Lenehan [12], which proposes a strong correlation between interface traps and E' centers.

The effect on channel mobility is due to increased lattice and Coulomb scattering of electrons in the channel. The interface traps pose additional obstacles, i. e., scattering centers, for the charge carriers in the channel. The mobility μ is proportional to the inverse of the density of interface traps, so

$$\mu = \frac{\mu_0}{1 + \alpha(\Delta N_{\mathrm{it}})}\,, \tag{3.1}$$

where α is a parameter to reflect process variations. μ does not (in first order) depend on the density of trapped holes.

3.5 Charges trapped in the field oxide

In principle, charges are trapped in the field oxide in the same way as in the gate oxide. That the trapped charges have any affect at all on the behaviour of the transistor

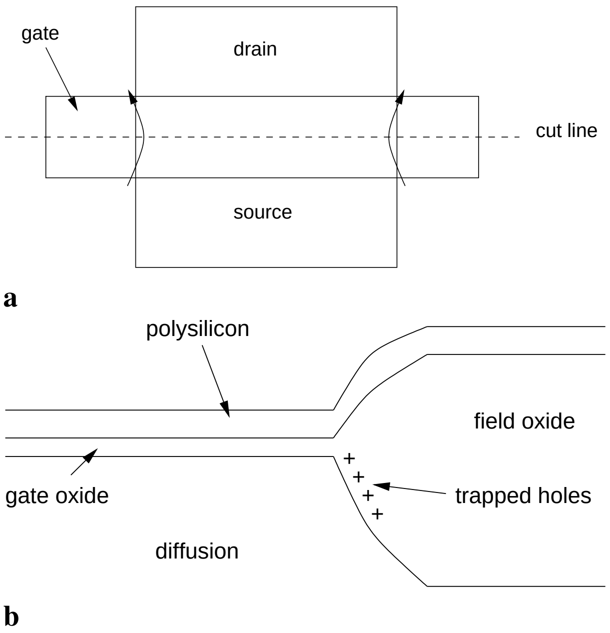


Figure 3.6: The leakage path alongside the gate. **a** Top view. The arrows indicate the path. **b** Cut view along the cut line (*dashed line* in **a**)

comes from the geometric structure of the MOSFET device and the associated depth profile. For a linear NMOS, i. e., an NMOS with an open gate structure, as opposed to the enclosed structure shown in Fig. 3.1, there is a possible path for charge carriers—and thus a current (called *leakage current*)—from drain to source alongside the gate, independent of the gate–source voltage. Due to limited precision of the fabrication process, this path is in the diffusion region of the channel, but not under the gate oxide, but the field oxide (cf. Fig. 3.6). While this path is normally only marginally conductive, and thus the current very low (in the order of pA), trapping of holes in the field oxide leads to effects similar to those in the gate oxide. The trapped holes over the leakage path region act as an applied gate voltage, building up a channel along the the leakage path. One effectively has a parasitic MOS transistor, which gets turned on more and more with increasing total dose, resulting in the leakage current increasing with total dose.

Recombination is important in the field oxide as opposed to the gate oxide. Travel times of holes can be in the order of thousands of seconds and those of electrons can also be higher than in the gate oxide. The higher travel times are due to the greater thickness of the field oxide and the weaker field.

The increase of leakage current cannot be observed for the PMOS. The holes trapped in the field oxide repel the holes in the diffusion, so there is no buildup of a channel. Thus, there is no increase in conductivity of the path, so there is no increase of leakage current.

3.6 Effects of the applied field

All radiation effects are in some way dependent on the strength of the applied gate field, the *bias*. Concerning the effect of trapped holes in the oxide, the hole-trapping fraction f_T is smaller for a stronger field ($\propto E^{-1/2}$), so there are less trapped holes, which leads to a smaller shift of the threshold voltage. On the other hand, the cross section for recombination of electrons at hole traps is smaller for a stronger field ($\propto E^{-3/2}$–E^{-3}), so there is less recombination and thus, less annihilation of E' centers, which leads to a greater threshold voltage and delays the saturation of hole trapping at higher doses [6]. The buildup of interface traps depends on the sign of the applied field; it is greater for a positive bias. The slow buildup* of interface traps becomes faster with a stronger field, while the fast buildup does not [6].

*For an explanation of slow and fast buildup, see Sect. 3.4

Chapter 4

The measurement setup

The general procedure for the measurements was as follows: First, the chips were inserted into their respective sockets on the irradiation board. Second, the board was put into a frame and connected to its battery power supply. Third, the frame with the board were irradiated in the γ-ray source at the Blutbank in steps of 30 Gy up to the desired dose. Fourth, back at the ASIC lab the chips were—one at a time—inserted into the socket on the measurement board. Fifth, the measurement board was connected to the parameter analyser, and measurements began.

4.1 The chips

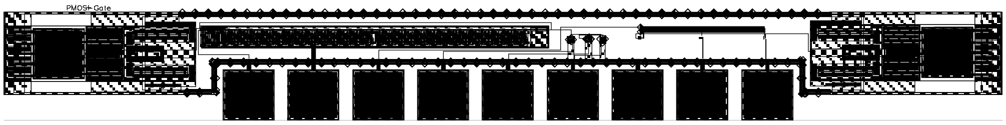
The teststructures are part of the OASYS chip produced in the 0.6 µm-process from AMS, designed and submitted by M. Feuerstack-Raible, M. Keller, J. Langeheine and M. Loose. They consist of a minimum size transistor* and both an edgeless and a "normal" (linear) transistor with the same drawn W/L of approx. 6.8/0.7. The real W/L of the edgeless transistor differs from this value, because a correct formula for the extraction of W/L for an edgeless transistor (as, e. g., presented in [9]) was not available at the time. Each of the transistors is available as both PMOS and NMOS. Also included is the input-transistor of the HELIX chip (a readout chip for HERA-B and other HERA experiments), a waffle-shaped PMOS transistor which, however, did not function and thus was not tested. The layout and schematic of the part of the chip with the teststructures are shown in Fig. 4.1. Note that there is just one gate contact for N- and PMOS, respectively, because the transistors were measured one after the other. The gates are protected from ESD by protection diodes connected after the gate pads. The dies coming from the fabrication site (*fab*) were glued into PGA68-packages and then bonded. The pads of the chips and their corresponding contacts on the package are shown in Table 4.1.

Other teststructures have been designed in the Blue Logic™ CMOS6SF 0.25 µm-process from IBM. They were included in another chip, the BeetleBG 1.0 designed by N. Smale. It was planned to compare the two processes with regard to radiation hardness and explore the possibilities for designing radiation hard devices in a modern deep sub-micron process. The schematic for the teststructures was very similar to the

*A transistor with the minimum allowed W and L (AMS 0.6 µm-process: $(W/L)_{\min} = 0.8/0.6$)

Table 4.1: Contact layout of the chips

Pad	Contact no.	Pad	Contact no.
NMOSGate	68	minPMOSDrain	62
minNMOSDrain	67	gnd	61
NMOSDrain	66	vnd	60
elNMOSDrain	65	HelixInDrain	59
PMOSDrain	64	PMOSGate	58
elPMOSDrain	63		



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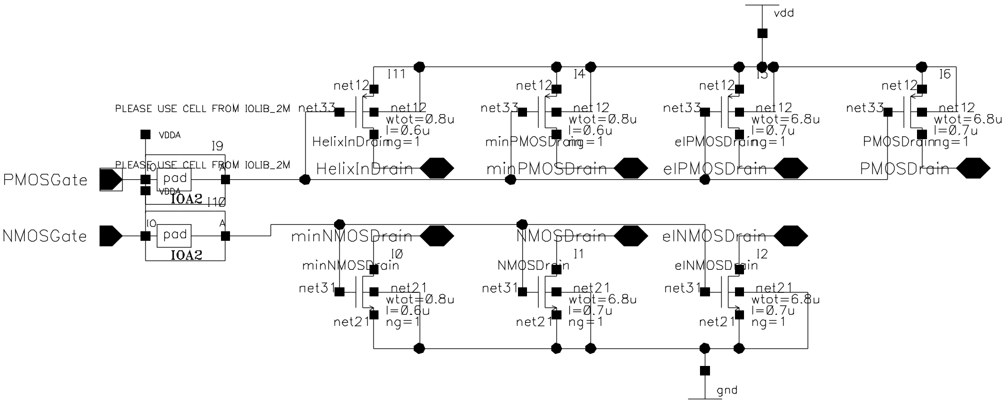

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Figure 4.1: **a** Layout and **b** schematic of the teststructures on the OASYS chip

one used for the AMS teststructures, to be able to compare transistors in different processes. The W/L of the linear and edgeless transistors was chosen as close as possible to the W/L of the corresponding transistors on the teststructures on the OASYS chip, with the exception of the minimum size transistor. Additionally, there was a prototype of an input-transistor for the Beetle chip (a proposed readout chip for the LHCb vertex detector, inner tracker and RICH detector) among the transistors, to gain a first insight into the irradiation behaviour of the Beetle chip, as well as to compare drawn W/L values to measured ones for transistors with extremely large W/L. This transistor consists of several parallel edgeless NMOS transistors, surrounded by guardrings. The design of the teststructures is shown in Fig. 4.2. Note the extremely large guardring structure around the teststructures as a whole and the NMOS transistors, to shield them from electrical interference, prevent parasitic coupling between them and provide as large a ground contact as possible. The transistor shown in Fig. 3.1 is the edgeless NMOS transistor of the teststructures. Its shape is compatible to the one used by the RD49 collaboration at CERN for their model of an enclosed transistor and their formula to calculate the W/L of the transistor [9, 10]. All the transistors are designed to

Table 4.2: List of the chips of the third series. All of the chips are glued with epoxy glue

No.	Designation	Hardened at [°C]	Notes
1	Perseus	80	Minimum size transistor broken after 2195 Gy
2	Jason	80	
3	Orion	80	
4	Theseus	80	
5	Odysseus	80	Broken after 2195 Gy
6	Herakles	50	Introduced at 5490 Gy
	Ref	80	Not irradiated

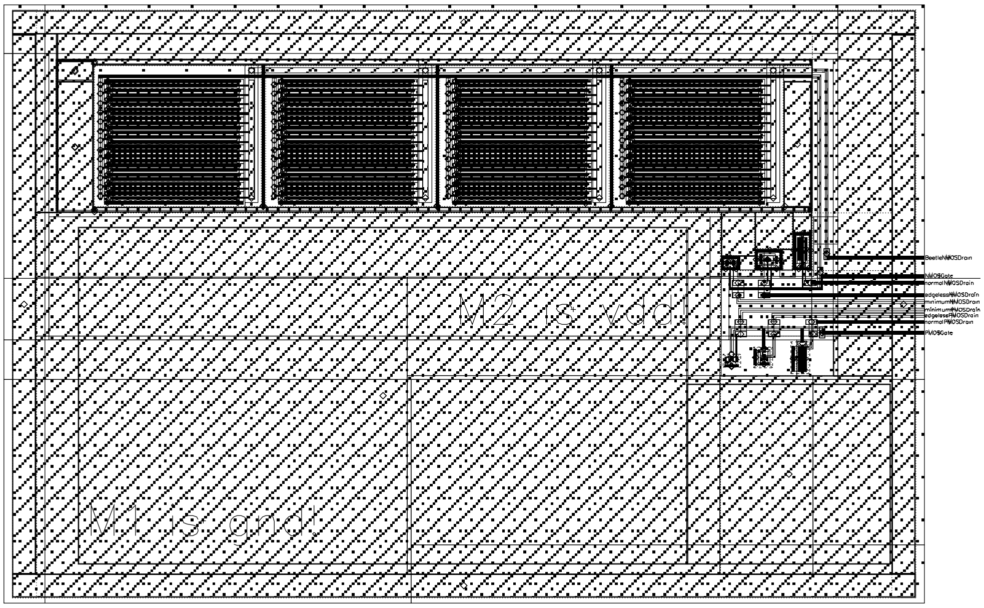
take up as little space as possible, to effectively model real-life conditions, where chip area is at a premium. Since the submitted chip was not returned in time, it was not tested.

There were several problems concerning the measurement of the leakage current and the threshold voltage, which might have been due to the glue used (see [2]). *Silver conductive paint* is not a glue, but can be used as such. It is, however, known to fade away under radiation, and may not be as durable as normal glue. *Epoxy glue* is a two-component-glue, which needs to be hardened for some time at a certain temperature as recommended by the manufacturer (e. g., 90 min at 80 °C). If epoxy glue is used, the dies seem to be put under mechanical stress during the hardening process. This might be the cause for the anomalies observed in the measurements of the leakage current (see Sect. 5.5). The chips glued with silver conductive paint generally showed a lower leakage current than the ones glued with epoxy glue (see Fig. 4.3).

In the first series of chips, epoxy glue and silver conductive paint were used. In the final series presented here, only epoxy glue was used. One chip (no. 6, called *Herakles*) was hardened at a lower temperature (50 °C) than the other five (80 °C). It was bonded after chip 5 (called *Odysseus*) was destroyed (during re-bonding after one bondwire was broken). Another chip (called *Ref*) was hardened at 80 °C and bonded. It was not irradiated, but measured along with the others as a reference to detect possible problems in the setup (e. g., temperature changes, calibration). The minimum size transistor on chip no. 1 (called *Perseus*) was destroyed due to ESD (see Fig. 4.4). A list of the chips is given in Table 4.2.

4.2 The boards

Two boards were used for the measurements: the irradiation board during irradiation and the measurement board for the measurements at the ASIC lab. The irradiation board includes five sockets to be able to irradiate all chips simultaneously. The irradiation board was necessary to bias the transistors during irradiation, because the total dose effect depends on the charge-carrier density in the channel region, which in turn is a function of the applied bias voltage (see Sect. 3.6). To have equal conditions for all transistors with regard to the charge-carrier density, their geometry (minimum size, normal and edgeless) and type (N- or PMOS) had to be taken into account, as shown



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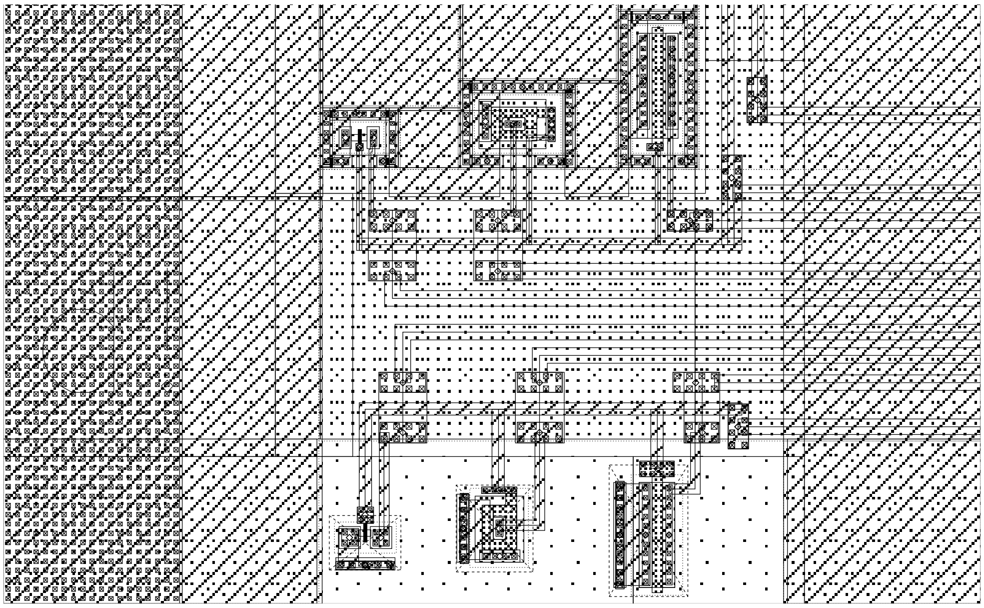

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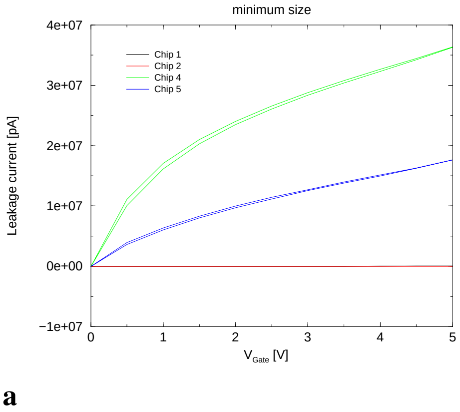
Figure 4.2: **a** Layout of the teststructures designed in the IBM 0.25 µm process on the BeetleBG 1.0 chip. **b** Zoom-in view on the smaller transistors



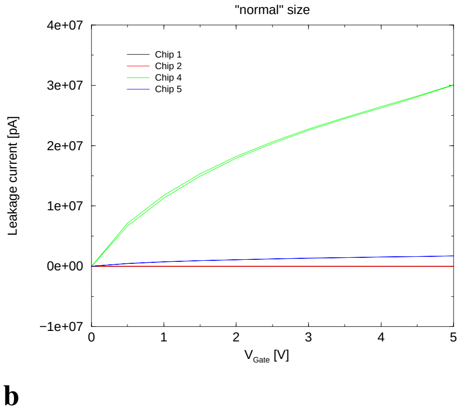


Figure 4.3: The leakage currents of chips 1 and 2 (glued with silver conductive paint) compared to chips 4 and 5 (glued with epoxy glue). **a** Minimum size transistors; **b** "Normal" size linear transistors. Leakage currents of chips 4 and 5 are approx. 10^4 times greater than of chips 1 and 2. The chips belong to the first series

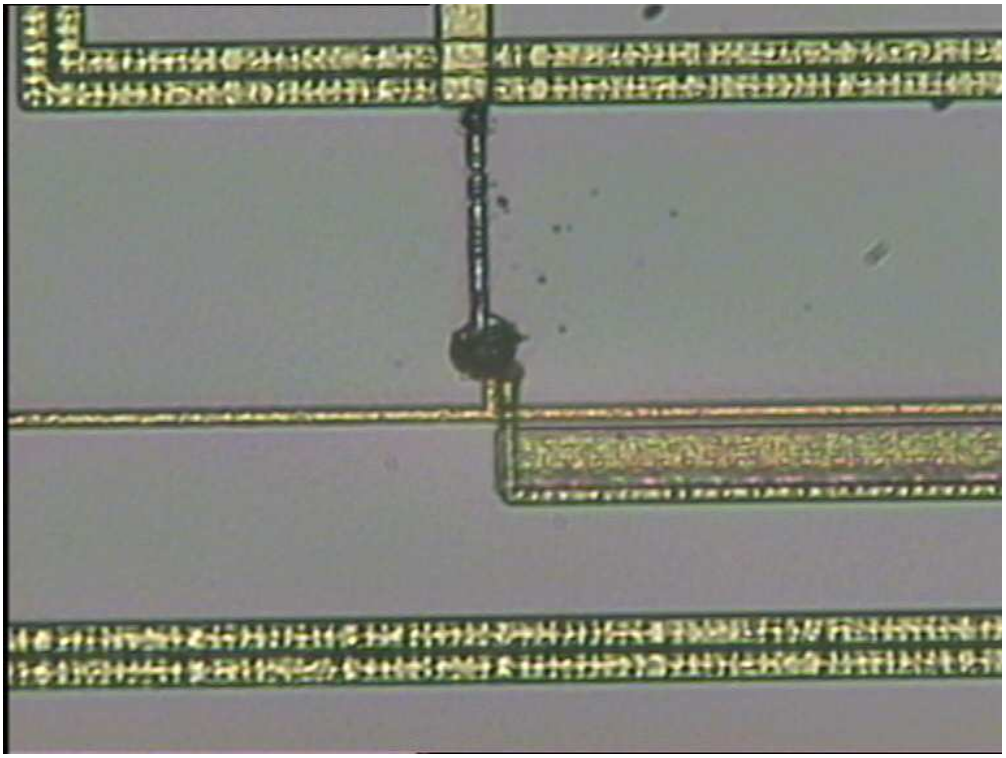


Figure 4.4: Photograph of the minimum size transistor on *Perseus* after ESD

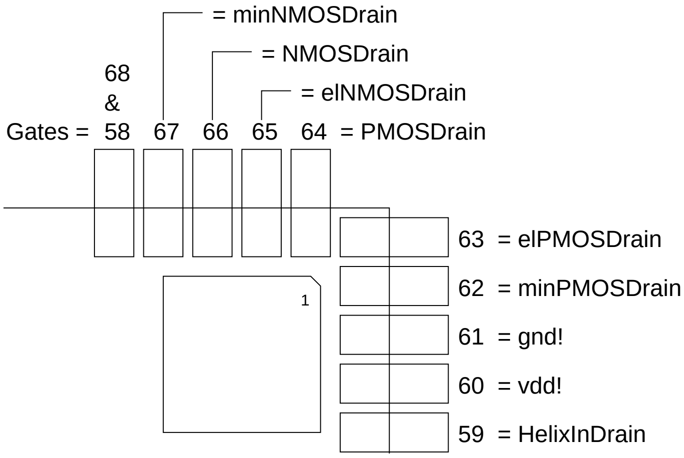


Figure 4.5: Schematic view of the measurement board

by

$$I_d = (W/L)H\varrho\mu V_{DS}\,, \tag{4.1}$$

where H is the height of the gate oxide, ϱ is the charge-carrier density, μ is the mobility of the charge-carriers and V_{DS} is the drain–source voltage. The correct voltage was achieved with a resistance R_t connected serially before the source of each transistor t. The desired drain current I_d for the "normal" linear transistor was arbitrarily set to $0.5\,\mathrm{mA}$. R_t was then calculated from

$$R_t = \frac{V_{GS} - V_{T0}}{I_d} \cdot \frac{W_{\mathrm{linear}}}{W_t} \quad \text{for the NMOS,} \tag{4.2}$$

$$R_t = \frac{V_{GS} - V_{T0}}{I_d} \cdot \frac{W_{\mathrm{linear}}}{W_t} \cdot \frac{\mu_n}{\mu_p} \quad \text{for the PMOS,} \tag{4.3}$$

where V_{GS} is the gate–source voltage, W_{linear} is the width of the "normal" linear transistor and W_t is the width of the transistor t. This calculation was made with the assumption that the supply voltage was $+4.5\,\mathrm{V}$ during irradiation.

Power was supplied by four mono-cell batteries mounted into the frame. The frame had connectors for $+3$, 0 and $-3\,\mathrm{V}$. The voltage was brought to $\pm 2.26\,\mathrm{V}$ by connecting diodes serially in the voltage path, so vdd was connected to $+2.26\,\mathrm{V}$, gnd to $-2.26\,\mathrm{V}$ and the gates to $0\,\mathrm{V}$. The frame was also necessary to fix the board in the correct position, so that the chips were irradiated equally in all sessions.

The measurement board was connected to the analyser to perform the measurements. There is one socket on the board. The board provides individual plugs for each pin of the teststructures. The plugs are connected to the pins of the chip-package via copperwire. Figure 4.5 shows a schematic view of the measurement board.

4.3 The radiation source at the Blutbank

The chips were irradiated using the Cs137 γ-ray source of the Blutbank. This source is normally used to irradiate blood plasma to prevent the graft-vs.-host-reaction. Radiation is provided in doses of 30 Gy over a 10-min period. The total dose was checked with an alanin dosimeter mounted onto the board. After evaluation of the dosimeters by Dr. Regulla, München, the actual dose was found to be 36.6 Gy per 10-min-period. The dose given by Dr. Regulla is the energy dose in water.

4.4 Measurement procedures on the analyser

The HP 4155A semiconductor parameter analyser can be programmed to perform a measurement and automatically analyse the results. It has four source/monitor units (SMUs) which were connected to the plugs on the measurement board. Measurement and analysis results are shown on a graphic colour screen. Data are saved as multi-column lists.

4.4.1 Threshold voltage

The method specified by AMS [1, Note 3.1] is as follows: source and substrate are connected to ground ("zero substrate bias"), while the gate–source voltage v_{GS}[†] and the drain–source voltage v_{DS} are swept synchronously[‡]. From the formula for the drain current with the transistor in saturation (Eq. 2.1), one gets

$$\sqrt{i_D} = \sqrt{\beta}\,(v_{GS} - V_{T0}) \tag{4.4}$$

as a linear curve (theoretically), where $\beta = K'\frac{W}{L} = \frac{\mu C_{OX}}{2}\frac{W}{L}$. The cross point with the x-axis is the threshold voltage V_{T0}. However, the curve of $\sqrt{i_D}$ measured is not linear, so one fits a tangent to the curve at the point of maximum slope

$$\frac{\partial\sqrt{i_D}}{\partial v_{GS}} = \max \tag{4.5}$$

and takes its cross point with the x-axis as V_{T0}.

4.4.2 Gain factor

The method to measure the gain factor is given by AMS [1, Note 3.1] as follows. Source and substrate are connected to ground ("zero substrate bias"). The drain–source voltage V_{DS} is set to 0.2 V or -0.2 V for N- and PMOS, respectively (so that measurements are taken in the ohmic region), and the gate–source voltage v_{GS} is swept. Based on Eq. 2.1, a linear regression is performed around the point of maximum slope of the drain current i_D:

$$i_D = K'\left(\frac{W}{L}\right)_{\text{eff}} V_{DS}(v_{GS} - V_{T0} - V_{DS}/2) \tag{4.6}$$

K' is calculated from the slope of the linear regression (Eq. 4.6) by

$$K' = \frac{\text{SLOPE}}{(W/L)_{\text{eff}}V_{DS}}\,. \tag{4.7}$$

[†]Lowercase letters indicate variable parameters, uppercase letters indicate constant parameters
[‡]All sweeps were done forwards and backwards

There is the problem that $(W/L)_{\text{eff}}$ is measured by AMS only for the minimum size transistor. It has a variation of 13% over the wafer, compared to 1% for K'. For the first, unirradiated measurement, $(W/L)_{\text{eff}}$ is calculated from Eq. 4.7. The average of K' over the wafer is given by AMS and is assumed to be very precise. As $(W/L)_{\text{eff}}$ does not change with the total dose (since it is a function of the geometry of the transistor and the production process), K' can be calculated in the following measurements from the now known $(W/L)_{\text{eff}}$ and Eq. 4.7 (see the appendix, Sect. A.2).

4.4.3 Leakage current

The leakage current was measured with gate, source and substrate connected to ground. The drain–source voltage v_{DS} was swept. For the diagrams (Figs. 5.6 and 5.7), the leakage current at $v_{DS} = 3\,\text{V}$ was taken. For this measurement, the measurement board was put into a special wooden box to isolate the setup. As the leakage currents measured were of the order of pA, the lower end of the measuring range of the analyser, even sound of footsteps influenced the data. For more precise measurements of the leakage current, one should also isolate the setup against interference of electronic devices and optimize the layout of the chip with regard to current flow (see Sect. 4.1).

Chapter 5

Measurement results and discussion

5.1 General issues

There were some problems regarding the gate diodes that were on the chip to protect the gates from ESD. Beginning with approx. 500 Gy, the diodes started to breakdown earlier than specified. (They were designed to take on all voltages exceeding 5 V.) This resulted in the analyser limiting the applied gate voltage so that the current would not go beyond the compliance, the maximum allowed current for the measuring unit (see the appendix, Sect. A.1). This effect was not discovered until the end of the second series of chips. The analyser gives no indication when it limits the voltage, and even falsely plots the progress of the sweep of the gate voltage. One had to manually measure the gate voltage to detect this effect. Not only the gate voltage path, but also the VDD-path was limited by the analyser (since the diodes connect to both VDD and GND). This was more difficult to detect, since it only resulted in a general decrease of measured currents due to the decreased VDD.

The diode-effect was fully taken into account in the last of three series of chips, presented in this paper. In the first series, the effect was not recognized as a lowering of the breakdown voltage, but was thought to be a complete breakthrough of the gate, so the chips that showed this effect were taken out of the measurements. In the following series, the effect was taken into consideration. The compliance was increased only slightly from one measurement to the next, for fear of destroying the chip through ohmic heat, so measurements were not performed under identical conditions. The compliance on VDD was raised even later in the run, so the measurements before were performed with a lower VDD than at the beginning. All this led to the start of a new series of chips, which is presented here. In this series, compliance was set to 60 mA, high enough to prevent an influence on the measurements—as increasing it further did not change the results—but low enough to avoid the danger of overheating the chip.

Another problem was chip 1, which exhibited different behaviour than the other chips in several curves. In Fig. 5.1, it shows a sudden rise at 4390 Gy, and decreases slower than the other chips, while in Fig. 5.3, it decreases much faster than the other chips. In Fig. 5.6a, it drops to nearly zero at 3290 Gy, while in Fig. 5.6b, it rises from nearly zero to approx. $9 \cdot 10^6$ pA and remains constant thereafter. Since these effects are not understood and do not seem to be effects of the irradiation, chip 1 has been taken out of the discussion of the results.

5.2 Error estimation

The parameter analyser has a measurement accuracy of 0.5% in the nA-range and 0.1% in the mA-range, as given by HP [3]. Additionally, to get an estimate for the measurement error of the setup, one measurement was repeated several times, and the highest deviation of the mean taken as the error. This resulted in an error estimate of 0.01%. Dr. Regulla gives a total error of 2.3% for the evaluation of the total dose.

5.3 Threshold voltage

The results from the measurement of the threshold voltage V_{T0} for n- and p-type transistors are shown in Figs. 5.1 and 5.2, respectively. One can see that for both N- and PMOS, the threshold voltage decreases with total dose as expected (see Sect. 3.3). The PMOS decreases slower than the NMOS.

There is no sign that the threshold voltage of the NMOS is going to show the rebound effect (see Sect. 3.4 and [5, 6]). However, after falling off rapidly at the beginning of irradiation, the curves start to flatten. This may be an indication that they are going to rise again due to negative interface trap charges. The behaviour of flattening curves was also observed in other experiments [7], though the absolute changes were much smaller there (approx. 50 mV). According to Saks et al. [8], the densities of both trapped oxide charges and interface states decrease with decreasing oxide thickness. One might expect both the resulting negative threshold voltage shift (due to trapped oxide holes) as well as the positive shift (due to interface traps) to be smaller than in the older literature, where structures with thicker oxides were investigated. Measurements of deep sub-micron minimum size structures irradiated up to 30 Mrad show no negative shift and only a small positive shift in the order of tens of mV (see [9, 10]).

Mekkaoui and Yarema [7] mention generally lower threshold voltage shifts for enclosed than for linear devices. They give values for the edgeless transistor which are approx. 33% higher than those for a linear transistor, both with a W/L of 8/0.6. This could not be verified here. The shifts in threshold voltage differ by approx. 3% for the linear and the enclosed transistors with a W/L of 6.8/0.7. It is, however, difficult to compare transistors in different processes, since one does not know the exact specifications of the other processes—like, e. g., doping profile—that might influence the results. In [10], for instance, the threshold voltage shift of the enclosed transistors is higher than that of the linear transistors.

The V_{T0}-measurements for the linear NMOS were heavily disturbed by high leakage currents. Since the leakage current increases with irradiation, there was an offset to the measured i_D-curves increasing with the total dose. This altered the results for V_{T0}. Another problem was that the computation of the threshold voltage required a derivative and a square root of the measured curves (see Sect. 4.4.1), which were computed by the analyser. As shown in Sect. 5.5, the measured curves of the leakage current have a negative offset for NMOS, so one measured a negative current for small v_{DS}.

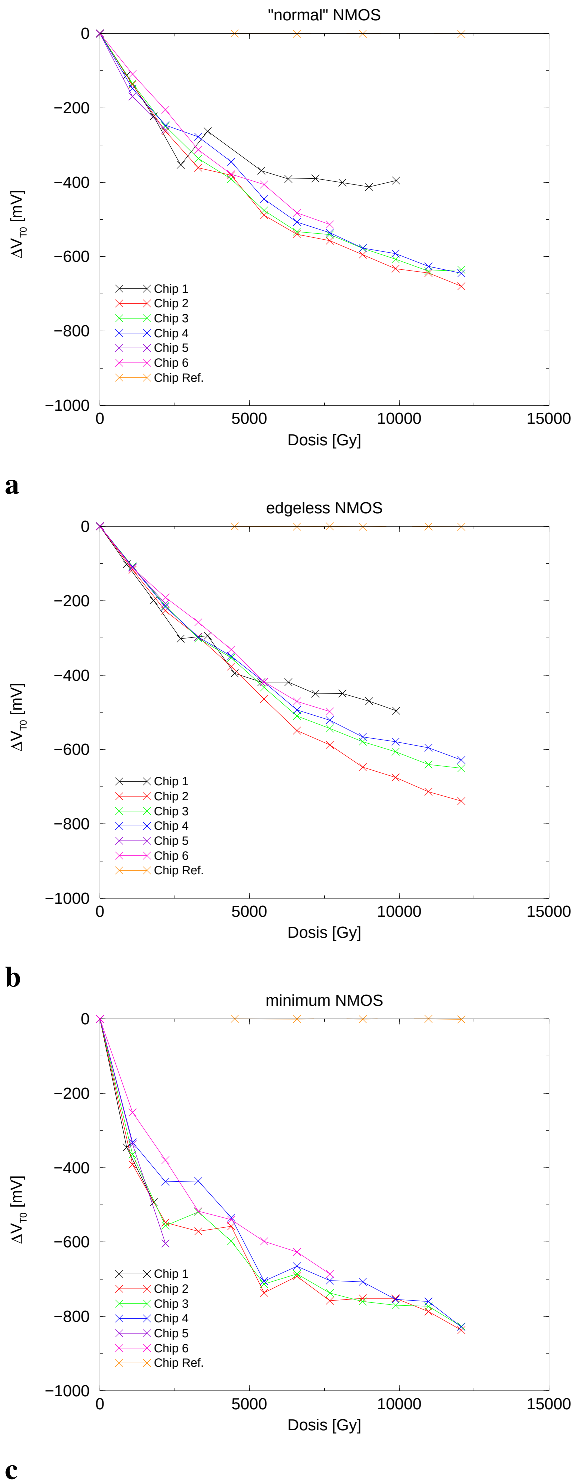
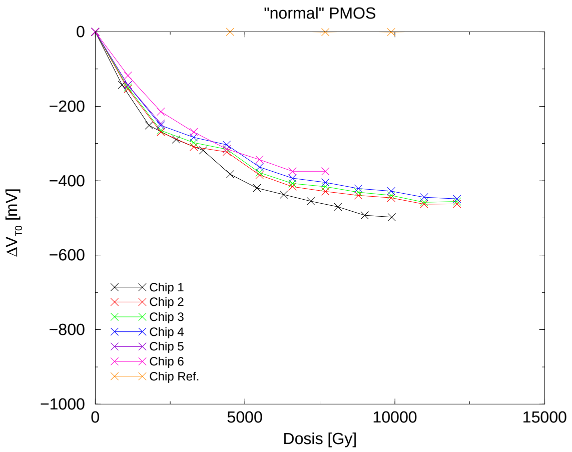


Figure 5.1: The measured threshold voltage shifts plotted against the total dose. **a** normal NMOS; **b** edgeless NMOS; **c** minimum size NMOS



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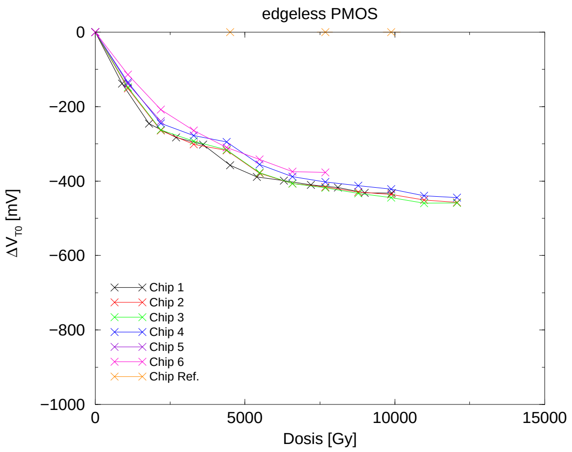

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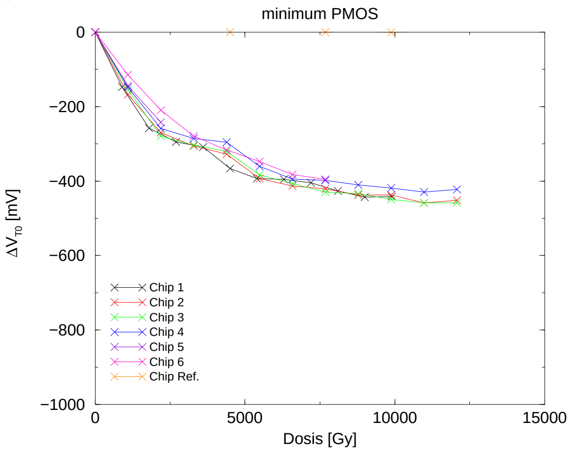

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Figure 5.2: The measured threshold voltage shifts plotted against the total dose. **a** normal PMOS; **b** edgeless PMOS; **c** minimum size PMOS

The parameter analyser computed the square root of the absolute of the curve. This led to a point of discontinuity where the curve intersected the v_{GS}-axis. (v_{GS} is swept along with v_{DS} in this measurement, so low v_{GS} also means low v_{DS}.) This point resulted in a peak after derivation of the curve, so that the tangent was not fitted to the curve at the actual point of maximum slope (see Eq. 4.5) but at the peak, resulting in erroneous results.

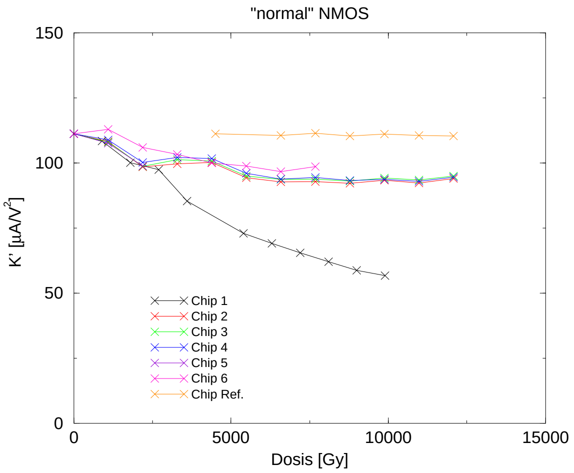
This effect was reduced by "calibrating" the measurement curves before the analysis and computation. To this end, a separate measurement was performed. Every parameter was chosen as in the threshold voltage measurement except v_{GS}, which was set to 0 V, so it was effectively a measurement of the leakage current, adapted to suit the need of the calibration. The results of this measurement were subtracted from the results for the threshold voltage, so that one had the curves without the offset from the leakage current. These curves were then analysed after the measurement session with the Perl-scripts described in the appendix, Sect. A.2. The effect was not entirely ruled out with this scheme, since the curves for the leakage current were not completely identical to the offset of the measured i_D-curves, so the peak was only diminished, not negated. This had to be accounted for in the Perl-scripts.

5.4 Gain factor

The results from the measurement of the gain factor K' for n- and p-type transistors are shown in Figs. 5.3 and 5.4, respectively. There is a problem with a dip in the curves, as was the case with the leakage current (see Sect. 5.5), at 4390 Gy. This dip occurs only in the PMOS measurements and does not show for chip 6, so it might be regarded as an artifact from the measurements.

One can see that, for the PMOS, after a steep decline in the beginning, K' does not decrease any longer, but begins to rise again slowly. For the NMOS, there is a less steep decline in the beginning, but K' also rises with higher total doses, albeit slower than for the PMOS. This is partly in agreement with curves given in the literature [4, 6] as well as theory. There are, however, curves in the literature showing contrary data [5]. Dressendorfer [6, Sect. 5] describes how the mobility (on which K' depends) relates to the buildup of interface traps, whose density increases with total dose, but reaches saturation after a certain amount of irradiation. Following this, the curve for mobility vs. interface trap density should rapidly decline in the beginning (low density), but should gradually flatten for increasing densities (see Eq. 3.1). So, the saturation can be understood, but not an increase in mobility resp. K'. Following Sect. 5.2, the increase in K' is well outside the error margin, and happens for all chips, so it cannot be attributed to a defect in the measurement setup.

Mekkaoui and Yarema [7] and the RD49 collaboration [10] report a decrease of transconductance g_m (which depends linearly on K') for all types of transistors. This is in agreement with the results presented here. A lower decrease is reported in [7, 10] for the edgeless NMOS than is observed here ("very little" [7] and 6% [10] compared to 18%). Mekkaoui and Yarema [7] give a decrease for the PMOS transistor of 13% compared to 29% measured here. They don't give curves for the dependency of transconductance on the total dose, so the behaviour of rising curves for higher doses cannot be compared.



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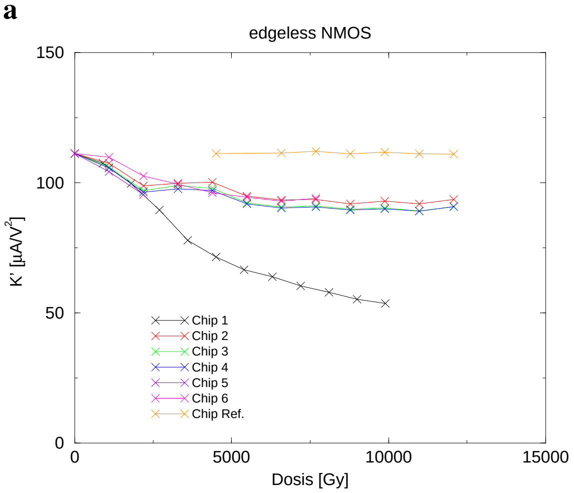

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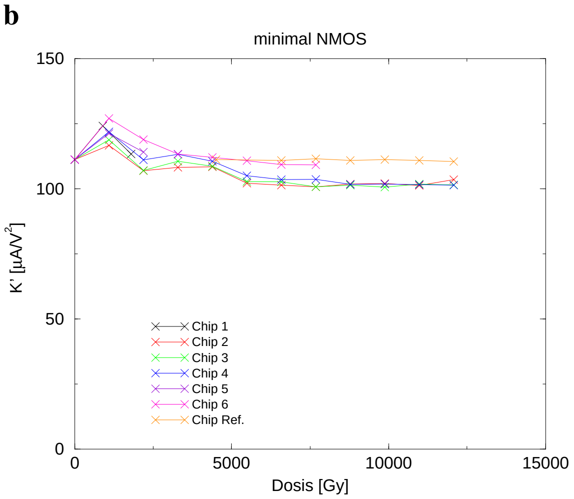
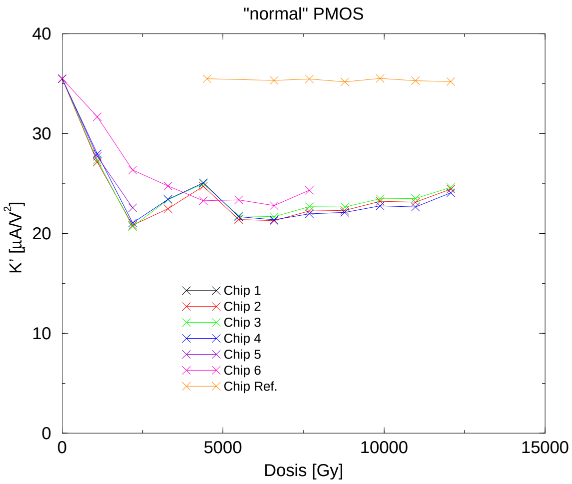
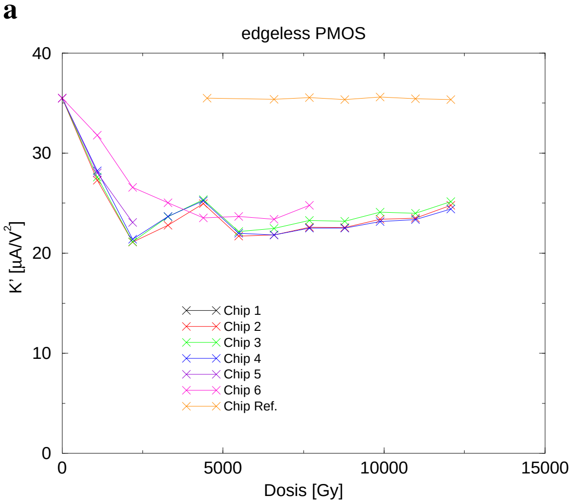


c

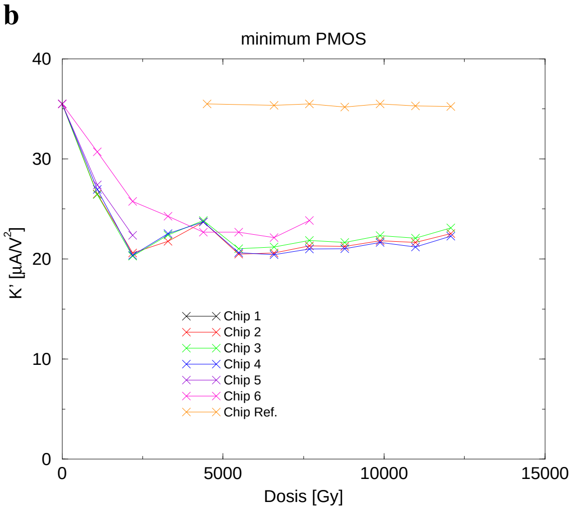
Figure 5.3: The measured gain factors plotted against the total dose. **a** normal NMOS; **b** edgeless NMOS; **c** minimum size NMOS



a



b



c

Figure 5.4: The measured gain factors plotted against the total dose. **a** normal PMOS; **b** edgeless PMOS; **c** minimum size PMOS

5.5 Leakage current

The results from the measurement of the leakage current for n- and p-type transistors are shown in Figs. 5.6 and 5.7, respectively. One can see that the linear NMOS show an increase, while the PMOS and edgeless NMOS do not. This is in agreement with theory (see Sect. 3.5). There are, however, some differences to what was expected:

1. There is a dip in the NMOS measurements at two consecutive points, approx. 3290 Gy and 4390 Gy.
2. The leakage current of the edgeless NMOS does increase, beginning with approx. 5000 Gy.
3. For high total doses, the leakage current for the NMOS reaches saturation and even starts to decrease slightly.

1: This dip does not seem to come from a physical property of the leakage current under irradiation. Only the transistors on chips 1–5 show the dip, while the transistors on chip 6, which joined the irradiation process later at 5490 Gy, do not. Also, except for the dip, the points seem to lie on one curve, where a physical phenomenon would be expected to influence later parts of the curve. Rather, there seems to have been an error in the two measurement sessions corresponding to the two points of the dip. Chip 6, for which the measurement sessions corresponding to these total doses were done at a different time, was not influenced by the problem. What exactly was wrong is not known. In theory, the leakage current should increase steadily with total dose, since the path from source to drain should become more conductive with additional trapped holes generated by irradiation. The measurement setup was not found to be defective on any of the respective days. The uncertainty about the cause of the dips led to the introduction of chip *Ref* to have a comparison.

2: This is not an actual leakage current starting to build up, but rather seems to be the effect of trapped holes in the gate oxide which also cause the V_{T0}-shift. The holes act as a voltage applied to the gate, so the transistor effectively progresses to the strong inversion region. This effect should also apply to linear NMOS, but cannot be seen in the diagrams because of the different orders of magnitude. The effect is in the order of 10^5 pA, compared to an order of 10^7 pA for the leakage current of the linear NMOS. Its effect on the measurements of threshold voltage and gain factor should be negligible, again due to differences in order of magnitude (10^5 pA compared to 10^8 pA). Note that in another experiment performed by Mekkaoui and Yarema [7] for teststructures in a 0.5 µm process with a W/L of $8/0.6$, they get different results for the enclosed (edgeless) transistor. In their experiment, the leakage current changes by less than an order of mangitude.

It is interesting to note that the plot of the edgeless NMOS' leakage current versus total dose (Fig. 5.6b) looks like a standard i_{DS} vs. v_{GS}-plot. If plotted logarithmically against the dose as in Fig. 5.5, one can see that for low to medium total doses, the leakage current goes exponentially with the total dose, whereas for high total doses, the slope decreases. This can be explained by trapped holes accumulating in the gate oxide. The exponential behaviour at low to medium total doses would mean that the transistor is operating in weak inversion, while for higher doses, it begins the progress

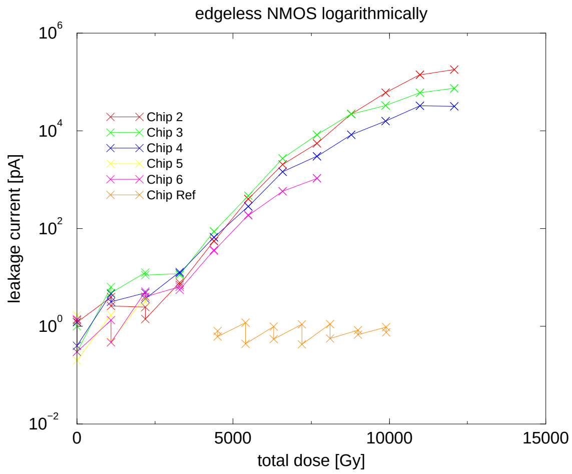


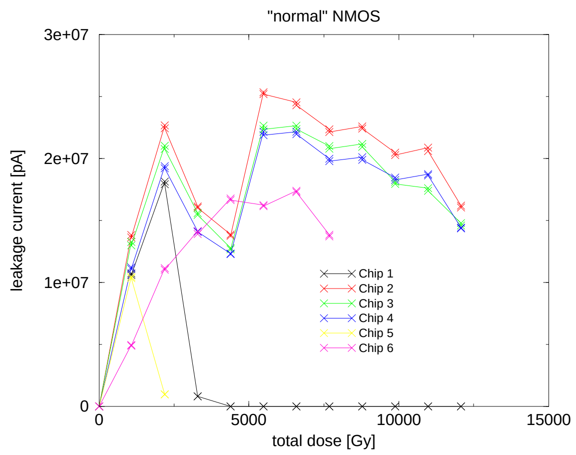
Figure 5.5: The measured leakage current of the edgeless NMOS plotted logarithmically against the total dose

to strong inversion, i. e., operation with gate voltages greater than V_{T0}, with a quadratic dependency on v_{GS} (see Sect. 2.2). Strong inversion is not reached in this measurements, since the threshold voltage never gets below 0 V (see Fig. 5.1).

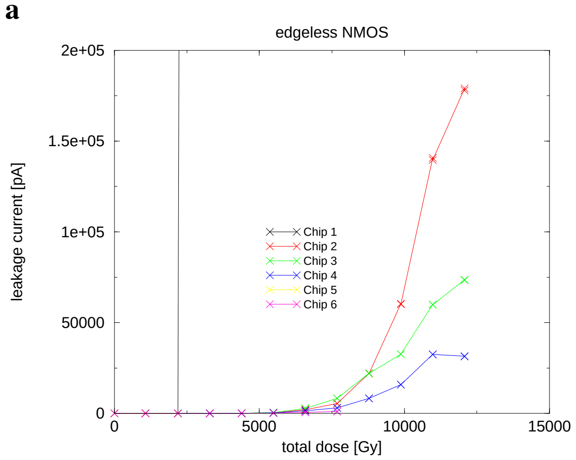
3: This has also been observed by Mekkaoui and Yarema [7]. Their results for the linear transistors resemble the ones presented here. There does not, however, seem to be a theoretical explanation for this phenomenon. There is no mention of saturation of the leakage current with high total doses in the literature. There is also a steeper drop at the end of the measurements, for both chip 6 and the rest. This might be a dip similar to the one described under 1, since it happens at different total doses at the same measurement session. It is, however, also present in [7], so it may also be a physical phenomenon.

There are also irregularities in the curves for the PMOS, but these may be attributed to the parameter analyser, which was unable to handle currents in the order of pA—although the manual gives a resolution of 10 fA [3]—as it had not been calibrated in a while. Another reason was the measurement setup, which was not built for the measurement of low currents. The measurement of leakage currents was introduced after the first chips of the first series, when the setup was already installed.

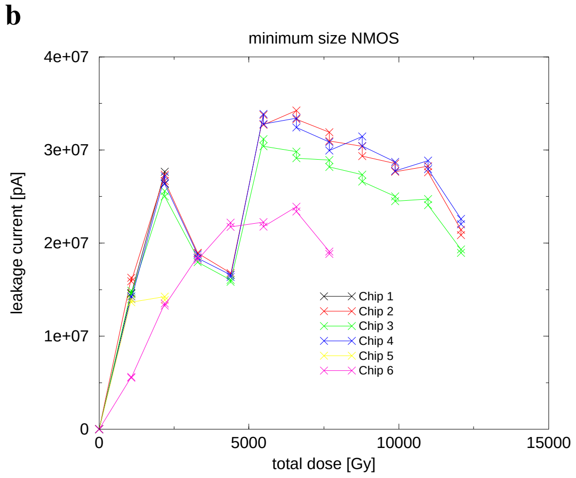
There are two problems observed in the curves of each single measurement (leakage current vs. drain–source voltage curves). First, while the curves generally look as one would expect, i.e., like the typical current–voltage-plots of a transistor with a small gate-voltage applied, they always have a certain current-offset—negative for n-, positive for p-type FETs—in the order of pA. This effect cannot stem from a physical property of the transistors, since it would mean a current flowing with no voltage applied. Additionally, it was already present when there was no irradiation applied, and does not show any dependency on the total dose, but only non-continuous fluctuations. This might also be a problem of the parameter analyser resp. the measurement setup, as described above.



a

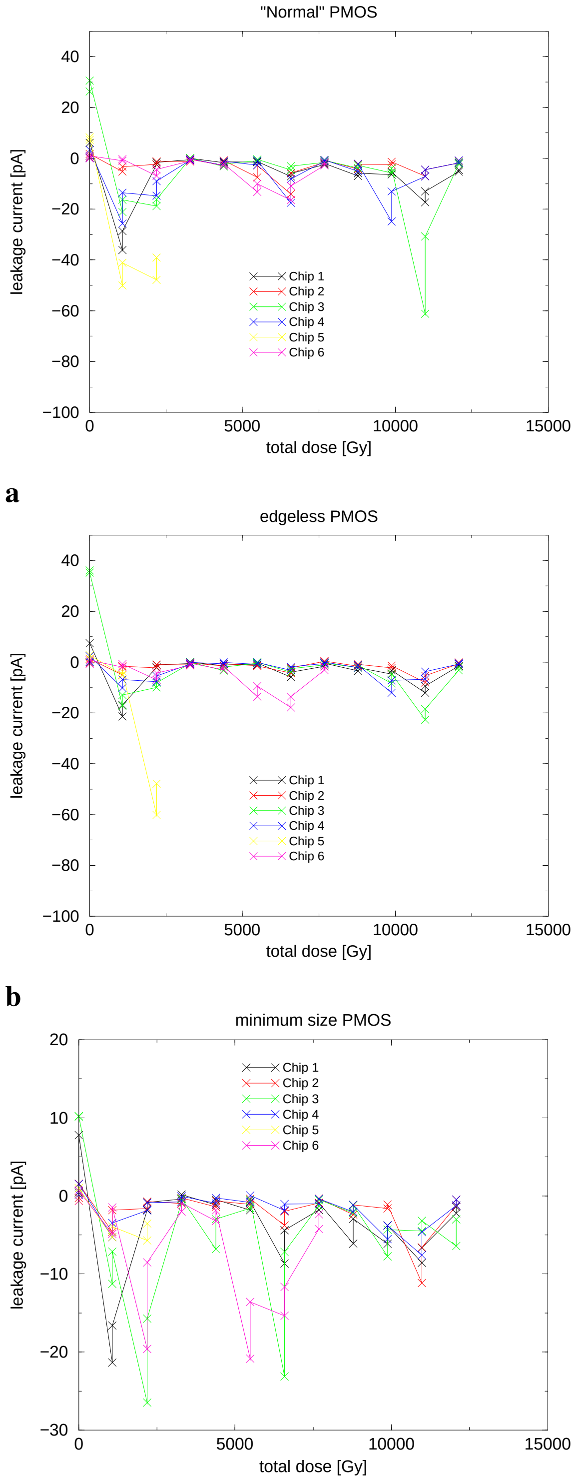


b



c

Figure 5.6: The measured leakage current at $v_{DS} = 3\,\mathrm{V}$ plotted against the total dose. **a** normal NMOS; **b** edgeless NMOS; **c** minimum size NMOS



a

b

c

Figure 5.7: The measured leakage current at $v_{DS} = 3\,\mathrm{V}$ plotted against the total dose. **a** normal PMOS; **b** edgeless PMOS; **c** minimum size PMOS

Second, the curves take the form of a hysteresis, where the relative difference between the "forward" and "backward" parts of the curves remains nearly constant for increasing total dose. This may again be a problem of the measuring procedure. The analyser waits for a certain delay time before it measures the data at the value of the swept variable that has been set before the delay (see [3] for further details). The delay time was set to 100 ms in all measurements. It seems possible that the leakage current did not settle fast enough from its higher value (or rose from its lower value) from the preceding measurement. So for the "forward" sweep from 0 to 5 V, it would be systematically too low, and for the "backward" sweep from 5 to 0 V, it would be too high, compared to a supposed real value of the leakage current at the respective point (which one might get setting the delay time to a higher value).

Chapter 6

Conclusions

One should keep in mind that on one hand, the process size generally influences the radiation tolerance (the smaller the size, the more radiation hard the process), and on the other hand, the processes themselves introduce a number of unknown factors into the analysis. Comparisons between different processes should therefore be made only very cautiously. In the following, it is tried to investigate differences in the measurements which can not be traced back to differences in the process parameters, as well as similarities of a general nature in the results.

The differences between the results for the leakage current of the enclosed transistors and the ones of Mekkaoui and Yarema [7] and Faccio et al. [9] might be explained by an additional factor. The design of their chip and its glueing to the package may differ. As seen in Sect. 4.1 and [2], the type of glue used to glue the die to the package can have a great influence on the leakage current. Also, the design of, e. g., ground contacts, guard rings or metal lines can influence the results in a way that even the same process may yield different results.

The threshold voltage shifts were much larger in this experiment than in the ones presented in [7, 9, 10]. Again, this might be due to differences in the design of the test-structures. Threshold voltage is, however, a complicated function of various process parameters, so it might more than other parameters depend on the process. The overall look of the results is in good agreement with the other experiments' results. For the NMOS, the curves of the deep sub-micron designs do not go down, but instead rise at high total doses ($> 10\,\mathrm{Mrad}$). This is due to the thin gate oxide which enables the trapped holes to leave via quantum effects, and thus leaves interface traps as the only source of trapped charge carriers. Since the effect of interface traps does not show until high doses, and is positive for NMOS, this leads to results like in [9, 10]. For larger process sizes like the HP-process discussed in [7] or the AMS $0.6\,\mu\mathrm{m}$-process, the thicker gate oxide does not allow for quantum effects. So, both N- and PMOS curves go down because of trapped holes in the oxide.

The results for the gain factor are in agreement with theory (see Sect. 3.4 and [6]) and results presented in the literature [7, 10]. The behaviour of rising curves is, however, not understood and should be investigated further to prove it as either a measurement error or a physical effect.

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Appendix

A.1 Implementation on the parameter analyser

A.1.1 Threshold voltage measurement

Here, the setup for the NMOS is given, with the corresponding values for the PMOS given in square brackets. The implementation on the analyser was like this: first, the voltages (VDD for vdd, VS for gnd, VD for the drain and VG for the gate voltage) were defined in the screen CHANNELS: CHANNEL DEFINITION and set in MEASURE: SWEEP SETUP:

- VG and VD as sweep sources VAR1 and VAR1′, respectively, swept from 0 to 2 V and back in steps of 20 mV [from 0 to -2 V and back in steps of -20 mV] with a compliance of 60 mA and 1 mA, respectively,
- VS as COMMON [VS = -5 V with a compliance of 60 mA], and
- VDD = 5 V with a compliance of 60 mA [VDD as COMMON].

The compliance is the maximum allowed current for the SMU. Then, in CHANNELS: USER FUNCTION DEFINITION, the user functions were defined for the subsequent analysis.

- SQID = SQRT(ID), the square root of the drain current ID.
- DSQID = DIFF(SQID,VG), the derivative of SQID with respect to the gate voltage VG.
- VT0 = @L1X, the cross point of LINE1 in the graphic display with the x-axis.
- BETA = @L1G, the slope of LINE1 in the graphic display.

In DISPLAY: DISPLAY SETUP, the voltages and user functions were assigned to the X-, Y1- and Y2axis.

- VG to the Xaxis,
- DSQID to the Y1axis and
- SQID to the Y2axis.

VT0 and BETA were defined as DATA VARIABLES, which means that they would be shown on the graphic display along with the curves.

The setup for the analysis is done in DISPLAY: ANALYSIS SETUP. First, a MARKER is defined to point at the maximum of the curve DSQID, so DSQID = MAX(DSQID). Then LINE1 was defined as a TANGENT on Y2 (which is SQID) at a point where VG = @MX, the x-value of the MARKER.

A.1.2 Slope measurement

The setup on the analyser is given for the NMOS, with the corresponding values for the PMOS given in square brackets. The voltages are defined in CHANNELS: CHANNEL DEFINITION and set in MEASURE: SWEEP SETUP to the following:

- VG as the sweep source VAR1, swept from 0 to 2 V and back in steps of 20 mV [from 0 to -2 V and back in steps of -20 mV] with a compliance of 60 mA,
- VS as COMMON [VS = -5 V with a compliance of 60 mA]
- VD = 200 mV [VD = -200 mV] with a compliance of 2 mA
- VDD = 5 V with a compliance of 60 mA [VDD as COMMON].

In CHANNELS: USER FUNCTIONS, the user functions for the analysis were defined:

- SLOPE = @L1G, the slope of LINE1 in the graphic display.
- DID = DIFF(ID,VG), the derivative of ID with respect to the gate voltage VG.
- VT0 = @L1X, the cross point of LINE1 in the graphic display with the x-axis.

In DISPLAY: DISPLAY SETUP, the voltages and user functions were assigned to the X-, Y1- and Y2axis:

- VG to the Xaxis,
- ID to the Y1axis and
- DID to the Y2axis.

SLOPE and VT0 were defined as DATA VARIABLES, to let them be shown on the graphic display.

The analysis setup in DISPLAY: ANALYSIS SETUP was like this: First, a MARKER was defined to point at the maximum of the curve DID, so DID = MAX(DID). Then LINE1 was defined as a TANGENT on Y1 at a point where VG = @MX, the x-value of the MARKER.

A.1.3 Leakage current measurement

For this measurement, the voltages were defined and set as follows in CHANNELS: CHANNEL DEFINITION and MEASURE: SWEEP SETUP for the NMOS (values for PMOS in square brackets):

- VS and VG as COMMON [VDD and VG as COMMON],
- VD as sweep source VAR1, swept from 0 to 5 V and back in steps of 500 mV [from 0 to -5 V and back in steps of -500 mV] with a compliance of 100 µA,
- VDD = 5 V [VS = -5 V] with a compliance of 1 mA.

In DISPLAY: DISPLAY SETUP, the axes were assigned as follows:

- VD to the Xaxis and
- ID to the Y1axis.

There were no user functions defined.

A.1.4 Offset measurement

This measurement was done to get the offset curves for the threshold voltage measurement. The voltages were defined and set as follows:

- VS as COMMON,
- VDD = 5 V with a compliance of 60 mA,
- VG = 0 V with a compliance of 60 mA and
- VD as sweep source VAR1, swept from 0 to 2 V and back in steps of 20 mV with a compliance of 60 mA.

In DISPLAY: DISPLAY SETUP, the axes were assigned as follows:

- VD to the Xaxis and
- ID to the Y1axis.

There were no user functions defined. Since no offset values had to be taken for the PMOS, there was no PMOS setup defined.

A.2 Implementation of the scripts in Perl

There were some Perl-scripts needed to do the the offset calculations for the measurement of the threshold voltage, and to process the data for visualisation with Xmgr.

First, the script to compute the threshold voltage from the corrected files, Compute_VT0_from_corrected_data.pl. The algorithm is programmed after the setup given in Sect. 4.4.1. Note that in the `maximum` and `maxindex` subroutines, the `for`-loop does not include the first 13 and last 11 measurement points. This was done to prevent the inclusion of the peak in the computation of the maximum (see Sect. 5.3).

```
#! /usr/local/bin/perl

unlink <~tippel/messkurven/FETs/?N*.svbv>;

@TYP = ("", "MIN", "EL");
@typ = ("", "min", "el");
@dosen = ("unbestrahlt", "900Gy", "1800Gy",
"2700Gy", "3600Gy", "4500Gy", "5400Gy",
"6300Gy", "7200Gy", "8100Gy", "9000Gy", "9900Gy");

sub maximum     {      # from Perl-book
 my $max = shift (@_);
 my $f = 0;
 foreach $foo (@_)
       {
       if ( $f < 190 and $f > 13 )
        {
        $max = $foo if $max < $foo;
        }
       $f++;
       }
 return $max;
}

sub maxindex    {  # as sub maximum; index of maximum
 my $max = shift (@_);
 my $maxi = 0;
 my $g = 0;
 foreach $foo (@_)       {
       if ( $g < 190 and $g > 13 )
        {
        if ($max < $foo)
         {
         $max = $foo;
         $maxind = $maxi;
         }
        $maxi++;
        }
       $g++;
       }
 return $maxind;
}

$n = 1;
CHIP: for $n (1 .. 6)   # all chips
{
$d = 0;
```

```
$s = 0;
$t = 0;
$z = 0;
for $t (0 .. 2) # from array TYP
 {
 for $d (0 .. 11) # all doses
 {
 $readname = $dosen[$d] . "/" . $n . "N" . $TYP[$t] . "VT0.ribit";
 $svbvname = "FETs/" . $n . "n" . $typ[$t] . ".svbv";
 $writename = ">>" . "FETs/" . $n . "N" . $TYP[$t] . ".svbv";

# Several cases being handled by this if
  if (-e $readname)      # the "normal case"
   {
   open(BLOCK, $readname); # open .ribit
   open(SVBV, $svbvname);
   open(WRITE, $writename);
   while (not eof SVBV)
       {
       $svbvzeile = "svbvzeile" . $n;
       ${$svbvzeile}[$s] = [split ' ', <SVBV>];
       $s++;
       }
   }
  elsif ($d == 0) # for the unirradiated (no .ribit-file)
      {
      open(SVBV, $svbvname);
      open(WRITE, $writename);
      while(not eof SVBV)
          {
          $svbvzeile = "svbvzeile" . $n;
          ${$svbvzeile}[$s] = [split ' ', <SVBV>];
          $s++;
          }
  ${$svbvzeile}[$d][0] = 0;
  print WRITE "@{${$svbvzeile}[$d]}\n";
  print "$svbvname @{${$svbvzeile}[$d]}\n";
  close WRITE;
  close SVBV;
  next;
  }
  elsif ($t == 2) # edgeless w/o .off/.ribit-files
      {
      # Check for chip 5 and over 1800Gy, or
      # chip 6 and over 6300Gy ist
      if (($n == 6) and ($d > 7))
       {
```

```
         next;   # stop...
         }
       elsif (($n == 5) and ($d > 2))
           {
           next CHIP;      # next chip...
           }
       else # all other edgeless-cases...
           {
           open(SVBV, $svbvname);
           open(WRITE, $writename);
           while (not eof SVBV)
               {
               $svbvzeile = "svbvzeile" . $n;
               ${$svbvzeile}[$s] = [split ' ', <SVBV>];
               $s++;
               }
           print WRITE "@{${$svbvzeile}[$d]}\n";
           print "$svbvname @{${$svbvzeile}[$d]}\n";
           # edgeless will be written as they were read,
           # no offset-correction necessary
           close WRITE;
           close SVBV;
           next;
           }
       }
   else
      {
      warn "Skipping $readname...\n";
      next;
      }
 # done with the cases...

   print "File $readname... ";

 # ...now to the actual computation
   while (not eof BLOCK)
       {
       $zeile = "zeile" . $n;
       ${$zeile}[$z] = [ split ' ', <BLOCK> ];
       $vgate[$z] = ${$zeile}[$z][1];
       $sqrt[$z] = ${$zeile}[$z][4];
       $diffsqrt[$z] = ${$zeile}[$z][5];
       $z++;
       }
   # now get the variables for computation out of
   # the arrays, then ($tangentnull) the computation
   $maxdiff = maximum (@diffsqrt);
```

```
  $indmaxdiff = maxindex (@diffsqrt);
  $maxsqrtdrain = $sqrt[$indmaxdiff];
  $tangentnull = 1000 * ($vgate[$indmaxdiff] -
  (($maxdiff)**(-1)) * $maxsqrtdrain);
  $beta = $maxsqrtdrain**2 * 10**6;
  # 1000 *, to get mV
  print "VT0 = $tangentnull mV\n"; # just for control
  ${$svbvzeile}[$d][4] = $tangentnull;
  ${$svbvzeile}[$d][3] = $beta;
  print WRITE "@{${$svbvzeile}[$d]}\n";
  close BLOCK;
  close SVBV;
  close WRITE;
  $z = 0; # Highly important!
  $s = 0;
  }
  }
}
```

Next, the script threshold.pl. This script computed the offset corrections which the script Compute_VT0_from_corrected_data.pl used for computation of the threshold voltage.

```
#! /usr/local/bin/perl

@typ = ("", "EL", "MIN");

MAIN: for $n (1 .. 6)
 {
 TYPEN: for $t (0 .. 2)
 {
 $z = 0;
 $b = 0;
 $vtname = $n . "N" . $typ[$t] . "VT0.TXT";
 $offname = $n . "N" . $typ[$t] . "OFF.TXT";
 $writename = ">" . $n . "N" . $typ[$t] . "VT0.ribit";
 if (-e $vtname and -e $offname)
  {
  open(VT, $vtname);
  open(OFF, $offname);
  open(DATA, $writename);
  }
 else
    {
    warn "File not found: skipping $vtname\n";
    next;
    }
```

```
print "Working on file $vtname...";
while (not eof VT)
     {
     $tempvt = <VT>;
     $tempvt =~ s/(^\S+) (\S+) (\S+) (\S+) (\S+)/$1 $2 $3/s;
     $vtzeile = "vtzeile" . $n;
     @{$vtzeile}[$z] = [ split ' ', $tempvt ];
     $z++;
     }

$z = 0;
$b = 0;
$i = 0;

while (not eof OFF)
     {
     $tempoff = <OFF>;
     $offzeile = "offzeile" . $n;
     @{$offzeile}[$z] = [ split ' ', $tempoff ];
     $z++;
     }

NZEILEN: for $i (4 .. $#{$vtzeile})
{
${$vtzeile}[$i][3] = ${$vtzeile}[$i][2] - ${$offzeile}[$i][2];
${$vtzeile}[$i][4] = sqrt(abs(${$vtzeile}[$i][3]));
$i++;
}

for $b (4 .. $#{$vtzeile})
  {
#########
  if (${$vtzeile}[$b][0] == 1)
   {
   ${$vtzeile}[$b][5] = 0;
   }
  elsif (${$vtzeile}[$b][0] == 202)
       {
       ${$vtzeile}[$b][5] = 0;
       }
  else
      {
      ${$vtzeile}[$b][5] =
      (abs(${$vtzeile}[$b+1][4]-${$vtzeile}[$b-1][4])) /
      (abs(${$vtzeile}[$b+1][1]-${$vtzeile}[$b-1][1]));
      }
#########
```

```
    if (${$vtzeile}[$b][0] == 1)
     {
     ${$vtzeile}[$b][6] = 0;
     }
    elsif (${$vtzeile}[$b][0] == 202)
        {
        ${$vtzeile}[$b][6] = 0;
        }
    else
       {
       ${$vtzeile}[$b][6] =
       (abs(${$offzeile}[$b+1][3]-${$offzeile}[$b-1][3])) /
       (abs(${$offzeile}[$b+1][1]-${$offzeile}[$b-1][1]));
       }
#########
    ${$vtzeile}[$b][7] = ${$vtzeile}[$b][5] - ${$vtzeile}[$b][6];
    print DATA "@{${$vtzeile}[$b]}\n"; # data written to file
    }
 print " ready!\n";
 close VT;
 close OFF;
 close DATA;
}
}
```

The follwing is the script Compute_KP_from_slope.pl. It reads in the data files and computes K' out of the measured slope, after Eq. 4.7 and the method given in Sect. 4.4.2.

```
#! /usr/local/bin/perl

$n = 0;
$t = 0;
$m = 0;
$w = 0;
@num = ("1", "2", "3", "4", "5", "6", "ref");
@typ = ("", "el", "min");
@mos = ("n", "p");

for $m (0 .. 1)
{
for $n (1 .. 6)
{
for $t (0 .. 2)
  {
  $readname = $num[$n] . $mos[$m] . $typ[$t] . ".svbd";
  $writename = ">" . $num[$n] . $mos[$m] . $typ[$t] . ".kvbd";
```

```
  if (-e $readname)
   {
   open(READ, $readname);
   open(WRITE, $writename);
   $w = 0;
   while (not eof READ)
       {
       @readzeile[$w] = [ split ' ', <READ> ];
       for $s (0 .. 4)
         {
         $writezeile[$w][$s] = $readzeile[$w][$s];
         }
       if ($w == 0)
        {
        if ($m == 0)    # ... hier fuer NMOS
         {
         $writezeile[0][1] = 111.23;
         $wleff = ($readzeile[0][1] / (111.23 * 0.2));
         }
        else
           {
           $writezeile[0][1] = 35.494;
           $wleff = ($readzeile[0][1] / (35.494 * 0.2));
           }
        }
       else
          {
          $writezeile[$w][0] = ($readzeile[$w][0] * 1.21975);
          $writezeile[$w][1] = ($readzeile[$w][1] / ($wleff * 0.2));
          }
       print WRITE "@{$writezeile[$w]}\n";
       $w++;
       }
   }
  else
     {
     warn "Skipping $readname...\n";
     next;
     }
  close READ;
  close WRITE;
  }
}
}
```

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Erklärung:

Ich versichere, daß ich diese Arbeit selbständig verfaßt und keine anderen als die angegebenen Quellen und Hilfsmittel benutzt habe.

Heidelberg, den ___________

____

(Till Tippel)