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# R27 Self-calibrating logarithmic CMOS image sensor with single chip camera functionality

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## Abstract

*CMOS photoreceptors with logarithmic response offer a high dynamic range but suffer from large device-to-device variations. We describe a CMOS image sensor that has an automatic analog calibration on chip to correct the resulting fixed pattern noise. In principle one single photoreceptor includes a photodiode and two transistors converting the incident light into a logarithmic voltage and a capacitor for storing the offset correction voltage. The calibrated image sensor (96 × 72 pixels) shows a dynamic range of 6 decades and a fixed pattern noise of 3.3 % of a decade. The sensor has a video output and special readout features like digital zoom and averaging of adjacent pixels making it suitable for image processing applications and single chip cameras.*

## 1. Introduction

The high dynamic range of logarithmic photoreceptors allows to cover nearly the complete intensity range of natural scenes. A tactile vision aid system for blind people [1] which is the motivation for our camera development has to manage these conditions. Together with additional requirements coming from the image processing unit of the system (e.g. random access to any picture part, averaging of neighbouring pixels) the usage of logarithmic CMOS receptors is a suitable solution.

CMOS image sensors always have to cope with the problem of mismatch between individual pixels (fixed pattern noise). In the case of linear integrating receptors the *correlated double sampling* technique [2] can be used to get rid of these non-uniformities. For logarithmic receptors off-chip methods with digital calibration have been established [3]. We have presented an integrated analog calibration method in [4] which brings the standard deviation of the pixel-to-pixel variations down to 2.3 % of a decade for one column. For the complete 64 × 64 array this value increased to 6 % of a decade due to larger column mismatch. This paper describes an improved version with reduced fixed pattern noise, higher resolution and additional features.

## 2. Sensor Concept and Implementation

The calibration concept is based on the fact that the sensor circuit can be stimulated not only by the photodiode but also by a reference current. The output signal corresponding to this reference current is ideally the same for all pixels but in reality differs from pixel to pixel caused by device-to-device variations. A differential amplifier compares the real pixel output to a reference voltage and adjusts the pixel until both voltages are equal. The calibrated pixel state is finally stored on a capacitor working as an analog memory cell.

### 2.1. Photoreceptor circuit

Figure 1 shows the schematic diagram of one offset-correcting pixel. The switches $S_1$ to $S_5$ are realized by single MOS transistors. During readout mode the switch $S_2$ is closed leading to a current path from the photodiode through the transistors $M_1$ and $M_2$ to $V_{dd}$. $M_1$ and $M_2$ work in weak inversion and convert the photocurrent into a logarithmic voltage. The pixel output voltage, buffered by transistor $M_3$, can be read out through the $V_{out2}$ line by closing the selection switch $S_4$. By opening $S_2$ and

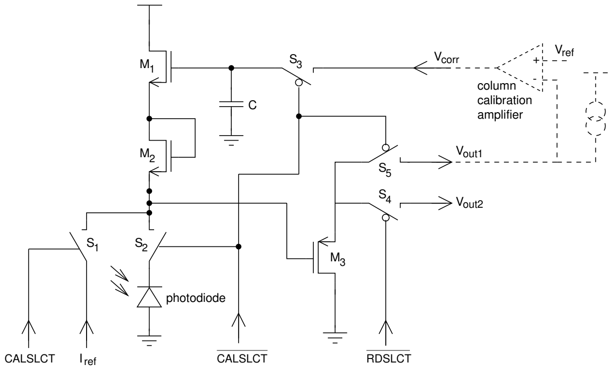


Figure 1. Photoreceptor circuit

closing $S_1$, $S_3$ and $S_5$ the receptor circuit changes to calibration mode. It is now stimulated by the reference current $I_{ref}$. The output signal is guided through $V_{out1}$ to the input of the calibrating operational amplifier at the end of each column. This autozeroing amplifier [4] compares $V_{out1}$ to a voltage $V_{ref}$ and produces the correction voltage $V_{corr}$. Since $V_{corr}$ is connected to the gate of $M_1$ a change of this voltage leads to a change in the pixel output voltage. The calibration amplifier moves $V_{corr}$ until the difference between $V_{out1}$ and $V_{ref}$ becomes zero. Finally the correction voltage is stored on the capacitor C by opening $S_3$.

## 2.2. Sensor architecture

The complete image sensor (block diagram in figure 2) consists of 96 × 72 pixels. It has 96 differential amplifiers allowing to calibrate all pixels of one row at the same time. The reference current $I_{ref}$ is mirrored into each column by well-matched transistors. It can be adjusted to a fixed value or generated by additional small photodiodes (one per pixel) leading to an automatic exposure control. The output multiplexer produces (with a maximum pixel rate of 8 Mhz) a single analog output which can be additionally amplified and mixed with the video synchronisation signal in the subsequent amp/mixer stage. The result is either a composite video signal (CCIR) or an analog signal with an arbitrarily chosen timing.

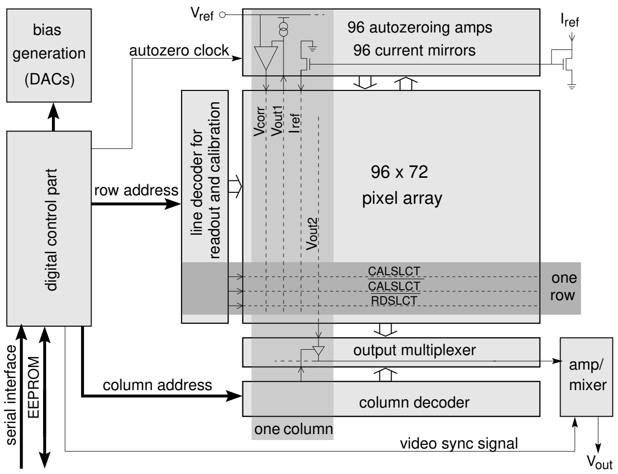


Figure 2. Block diagram of the image sensor

A number of digital to analog converters (DACs) generate the necessary bias and control voltages. They are realized as sample&hold stages that are updated in regular intervals. The appropriate voltages come from one single integrating DAC. It collects charge from a constant current source over a specific time and, depending on the integration time, delivers the according voltage. The complete image sensor is controlled by a digital part that produces the row and column addresses and all timing signals. A serial interface as well as a three button interface with on-screen display allow to select different operation modes and to change parameters. All chip settings can be stored in an external EEPROM and are automatically loaded after a system reset. The major sensor properties are summarized in table 1.

Table 1. Sensor properties

| | |
|---|---|
| Technology | 0.6 $\mu$m single-poly triple-metal CMOS Process |
| Die size | 5 × 2.5 mm$^2$ |
| Pixel size | 24 × 24 $\mu$m$^2$ |
| Resolution | selectable, max. 96 × 72 pixels |
| Output | analog, either video timing (CCIR) or self-defined timing |
| Features | random pixel access |
| | digital zoom (video mode) |
| | averaging of up to 8 × 8 adjacent pixels |
| | automatic exposure control |
| | programmable gain of output signal |
| | on-screen display (video mode) |

## 2.3. CMOS implementation

The chip layout is shown in figure 3 with the sensor array on the right half and the digital control part on the left half. Results from earlier designs (see in [4]) have shown that the layout of calibration amplifier and mirror transistor for $I_{ref}$ have to be done very carefully to avoid column to column variations. In the case of the reference current mirror the column transistors have been divided into 5 parts and spread over 4 neighbouring columns. Thus the high spatial frequencies of the process parameter variations are reduced by averaging.

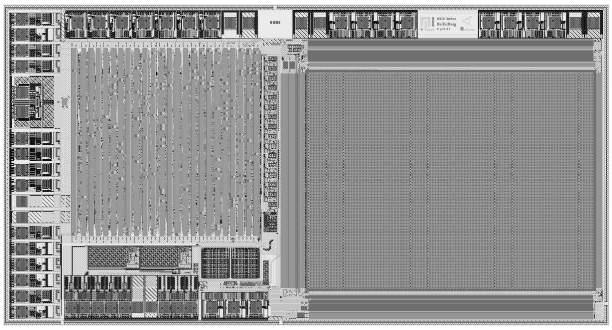

Figure 3. Layout of the image sensor

To prevent the pixel storage capacitors from fast discharging by parasitic photocurrents all structures except for the diodes are covered by a light shielding metal layer. Nevertheless the capacitors lose their charge with time (fractions of ms to many s depending on the light intensity) and the receptors have to be recalibrated. For image processing applications it is often useful to take the complete image first in a lower, time-saving resolution and then examine only the interesting image parts with a higher resolution. Therefore the photodiodes of adjacent pixels can be interconnected by transistor switches to build a larger receptor averaging the photocurrents of the individual diodes.

# 3. Measured results

## 3.1. Photoreceptor response

Figure 4 shows the averaged response of all 96 $\times$ 72 photoreceptors. Over a dynamic range of 6 decades the sensor has the expected logarithmic behaviour. The absolute voltage values given on the ordinate depend on different parameters controling the bias and control voltages. For the following measurements one specific set of parameters has been used. The curve shows a slope of about 105 mV per decade. To determine the fixed pattern noise the next results have to be compared to this value.

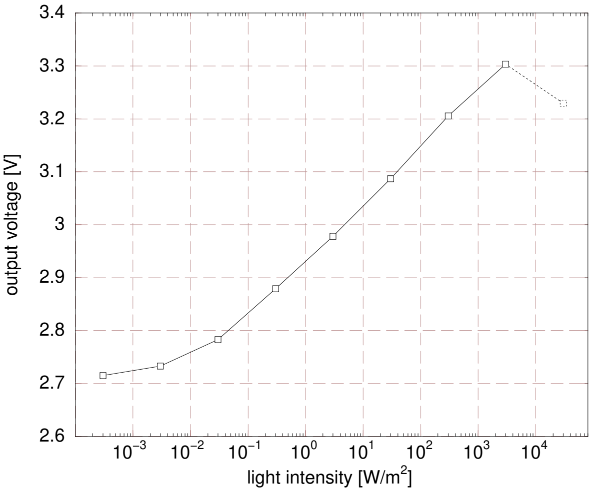


Figure 4. Pixel response measured over 8 decades of incident light intensity. The dashed line at high illumination results from the discharge of the storage capacitors by parasitic photocurrents.

## 3.2. Fixed pattern noise

A comparison between a calibrated and an uncalibrated image in figure 5 makes the importance of a fixed pattern noise correction clear. The contrast between background and ring symbol amounts to about 80 % of a decade. Since the sensor itself is not able to produce an uncalibrated image, the right picture shows a simulation. It is obtained by taking the measured offset distribution of a separately manufactured pixel column (different run of the same CMOS process) that has no calibration mechanism (and half the size of the calibrated pixel) and adding this distribution to the calibrated image. The two histograms in figure 5 show the grey level distribution. On the left two narrow peaks represent background and ring symbol, whereas on the right only one wide peak can be seen.

To get a quantitative value for the remaining fixed pattern noise after calibration the sensor was uniformly illuminated at an intensity of 3 W/m$^2$. The individual pixel output voltages were filled into a histogram shown in figure 6. The standard deviation (RMS) of 3.5 mV corresponds to 3.3 % of a decade in light intensity due to the slope of 105 mV per decade. Since the uncalibrated RMS value amounts to nearly 100 % of a decade, this means a non-uniformity reduction by a factor of 30. The RMS value for one column goes down to 2.5 %, and the column-to-column variations show a standard deviation of 2.2 %.

Figure 7 represents an example of a high dynamic range scene. It shows a bright bulb in front of a black symbol printed on white paper. The left picture is taken with the self-calibrating CMOS sensor which is able to see both, the structure of the bulb and the background symbol. The middle and the right picture stem from a CCD camera with an opened (middle) and closed (right) optical aperture respectively. The CCD sees either the background symbol but a bright blurred spot for the bulb, or the distinct bulb structure but no background at all. The CMOS sensor image looks a bit coarse due to the much smaller pixel number compared to the high resolution CCD camera.

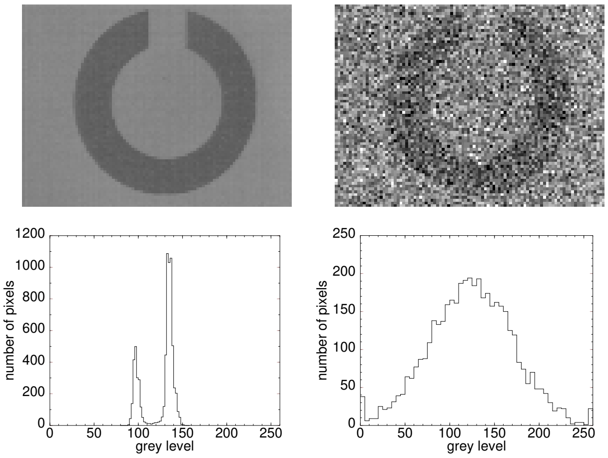


Figure 5. Comparison between a calibrated (left picture, measured data) and an uncalibrated image (right picture, simulated on the basis of measurements).

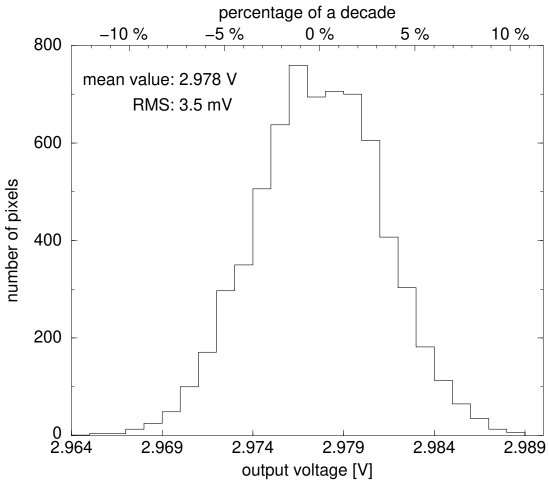


Figure 6. Distribution of pixel offsets at a light intensity of 3 W/m$^2$.

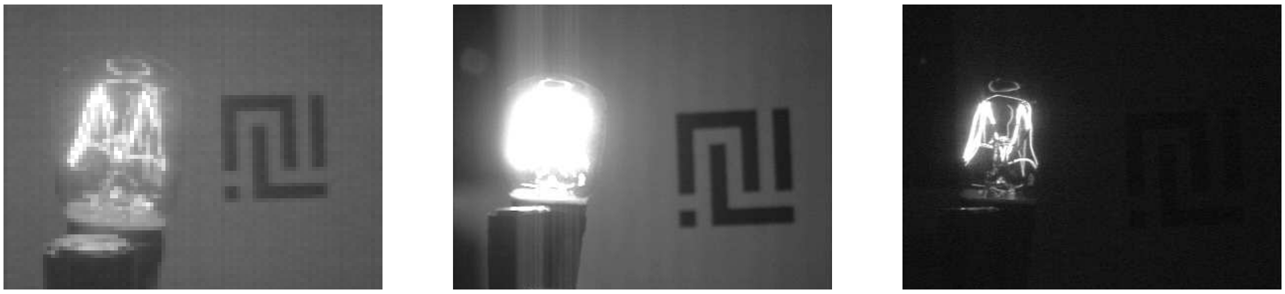

Figure 7. Images of a high dynamic range scene. The left one is taken with the presented logarithmic image sensor, the middle and the right one with a high resolution CCD camera.

### 3.3. Slope variations

The reference current $I_{ref}$ used for calibration corresponds to a specific intensity. Since the image intensities are normally spread over a large range, slope variations become important. They are calculated for each pixel by taking the response curve (cf. figure 4) and averaging the slope over 5 decades. The result, shown in figure 8, is a RMS value of 0.69 mV/decade or 0.65 % with respect to the mean slope of 105.6 mV/decade. If the calibration point is located in the middle of the response curve, intensities can vary by three decades up or down. For that reason the slope variations have to be tripled leading to 1.95 % which is a little more than the half of 3.3 %, the standard deviation of the fixed offsets. Table 2 again summarizes the sensor performance.

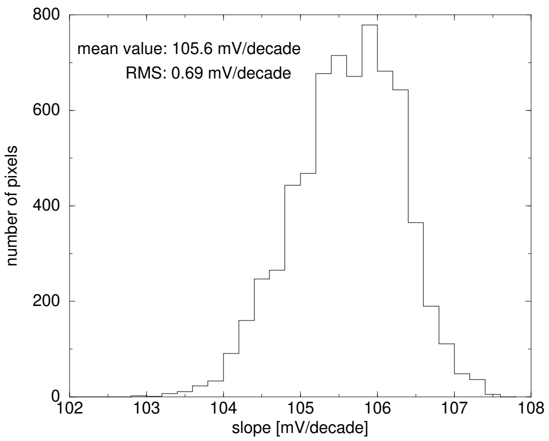


Figure 8. Histogram of pixel slopes

## 4. Conclusion

The on-chip calibration concept results in a logarithmic image sensor with significantly less fixed pattern noise in comparison to uncalibrated sensor arrays. The problem with remaining column-to-column variations of former solutions [4] has been reduced to a level below the pixel non-uniformity in one column. The pixel size of $24 \times 24\ \mu m^2$ allows to integrate about 200000 pixels on the area of an 1 inch CCD chip which should be enough for many applications.

Table 2. Sensor performance summary

| | |
|---|---|
| dynamic range | 6 decades, from 3 mW/m$^2$ to 3 kW/m$^2$ |
| fixed pattern noise | 2.5 % of a decade (RMS) for one column |
| | 3.3 % of a decade (RMS) for the complete array |
| slope variations | 0.65 % (RMS) per decade |

In contrast to external calibration methods with fixed offset values for the individual pixels, the presented concept has the advantage of also correcting temperature and aging effects [3]. During each calibration cycle the according offset values are determined again taking into account any possible change in the pixel-to-pixel variations. The influence of different pixel slopes remains small as long as the calibration point is not too far from the image intensities.

## 5. Acknowledgements

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[1] M. Loose, K. Meier, J. Schemmel, “A camera with adaptive photoreceptors for a tactile vision aid”, *Intelligent Robots and Computer Vision XV: Algorithms, Techniques, Active Vision and Materials Handling*, David P. Casaent, ed., Proc. SPIE 2904, 1996, pp. 528-537

[2] B. Diericks, G. Meynants, D. Scheffer, “Offset-free offset calibration for APS”, *IEEE CCD & AIS workshop*, Brugge, Belgium, 1997; Proceedings p. R13

[3] G. F. Marshall, S. Collins, “A high dynamic range front end for automatic image processing applications”, *Advanced Focal Plane Arrays and Electonic Cameras*, Thierry M. Bernard, ed., Proc. SPIE 3410, 1998, pp. 176-185

[4] M. Loose, K. Meier, J. Schemmel, “CMOS image sensor with logarithmic response and self calibrating fixed pattern noise correction”, *Advanced Focal Plane Arrays and Electonic Cameras*, Thierry M. Bernard, ed., Proc. SPIE 3410, 1998, pp. 117-127