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A Self-Calibrating CMOS Image Sensor with Logarithmic Response

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DISSERTATION

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A Self-Calibrating CMOS Image Sensor with Logarithmic Response

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Zusammenfassung

Ein CMOS Bildsensor mit automatischer Kalibrierung und logarithmischem Antwortverhalten - Im Rahmen dieser Dissertation wurde ein Bildsensor entwickelt und getestet, der einen hohen dynamischen Bereich und eine eingebaute analoge Korrektur der Pixel-zu-Pixel Variationen besitzt. Der endgültige Sensorchip besteht aus 384×288 automatisch kalibrierten Photorezeptoren, die den durch einfallendes Licht generierten Photostrom in eine logarithmische Spannung umwandeln. Der Sensor besitzt einen dynamischen Bereich von 6 Dekaden zwischen den Intensitäten 3 mW/m^2 und 3 kW/m^2. Im Vergleich zu nicht-kalibrierten logarithmischen CMOS-Sensoren führt das Konzept der eingebauten automatischen Kalibrierung zu deutlich verringerten Unterschieden zwischen den Ausgangsspannungen gleichförmig beleuchteter Pixel. Die Standardabweichung der verbleibenden Pixel-zu-Pixel Variationen beträgt 3.8 % einer Intensitätsdekade bei einer Beleuchtungsintensität von 1 W/m^2. Der Sensor beinhaltet alle Strukturen, die für den Einsatz als Ein-Chip-Kamera erforderlich sind, wie beispielsweise digitale Kontrolllogik, Auslesemultiplexer und Ausleseverstärker. Die Bilddaten können wahlweise über eine einzelne analoge Leitung (Videosignal) oder über eine digitale Schnittstelle (seriell oder parallel) ausgelesen werden. Dazu werden die analogen Signale direkt auf dem Chip mit Hilfe eines analog/digital Wandlers in digitale Daten konvertiert. Zusätzlich wurden weitere Funktionen wie eine automatische Blendenregelung, die Mittelung von benachbarten Pixeln und eine digitale Zoomfunktion eingebaut. Der Sensor wurde für den Einsatz in einem Sehersatzsystem für Blinde entwickelt und erfüllt die gegebenen Anforderungen.

Abstract

A self-calibrating CMOS image sensor with logarithmic response - Within the scope of this thesis, a high dynamic range image sensor with an integrated analog non-uniformity (fixed pattern noise) correction has been developed and tested. The final sensor chip includes 384×288 self-calibrating photoreceptors converting the photocurrent, generated by the incident light, into a logarithmic voltage. It provides a dynamic range of 6 decades in the intensity region from 3 mW/m^2 to 3 kW/m^2. Compared to uncalibrated logarithmic CMOS sensors, the self-calibration concept leads to a significantly reduced fixed pattern noise. The standard deviation of the remaining pixel-to-pixel variations amounts to 3.8 % of an intensity decade at a uniform illumination of 1 W/m^2. The sensor contains all components required for operating as a single chip camera like digital control part, readout multiplexer and readout amplifier. The image data can be read out either via a single analog line (video signal) or via a digital interface (serial or parallel) after undergoing an analog-to-digital conversion which is integrated on the chip. Additional features like automatic exposure control, averaging of adjacent pixels and digital zoom have been implemented. The sensor has been designed for use in a vision substitution system for the blind and fulfills the given requirements.

Contents

Introduction

The intrinsic photoelectric effect of standard CMOS devices allows integrating electronic circuits and optical sensors on the same microchip. For this reason, in recent years more and more CMOS image sensors partly consisting of up to several million pixels have been developed. They often represent single chip solutions or offer a high dynamic range (up to 6 decades in light intensity). These are two important advantages compared to commonly used CCDs. A major drawback exists in the mismatch of identical structures due to process variations. Different methods to reduce the influence of mismatching devices have been proposed or realized (some examples are given in chapter 2).

The image sensor developed within the scope of this thesis is based on a typical high dynamic range CMOS photoreceptor. It logarithmically converts the incident light intensity into a voltage. By this signal compression it becomes possible to handle wide intensity ranges with electrical signals that have a much lower dynamic range. However, this sensor concept is very sensitive to device mismatch leading to large pixel-to-pixel variations (*fixed pattern noise*). In most cases these pixel offsets are digitally corrected. To achieve a completely analog solution, an on-chip self-calibration method has been developed. It is presented in chapter 3.

On the basis of this method prototypes of image sensors with 64×64 and 96×72 pixels have been built and tested. Finally, a camera chip with about 110000 pixels (384×288) has been realized in a 0.6 μm CMOS process. It combines the high dynamic range of about 6 decades with significantly reduced fixed pattern noise and represents a complete *camera on a chip*. Chapter 4 describes the sensor design including all circuits for the different readout modes (analog or digital, video timing) and for the digital control. Finally, chapter 5 contains the measured results and some image demonstrations of the camera sensor.

The self-calibrating image sensor is embedded in a larger project dealing with the development of a tactile vision substitution system (TVSS) for blind people ([MAU98] and [LOO96-2]). The goal is to give these handicapped persons a new kind of visual sense as a replacement for their missing ability to see. The system should enable them to orientate in their environment, to avoid obstacles and endangerments and to recognize important hints like traffic signs or street names. Natural scenes can cover large dynamic ranges of even more than 6 decades which is a major reason for the use of CMOS sensors. Since it is currently not possible to contact the optical nerve in a way that any useful information can be transported to the brain, other transmission channels have to be found.

The TVSS uses the sense of touch which is often excellently trained in the case of blind persons. So far three different tactile displays have been developed: a pneumatic system for the abdomen described in [JES96], following the ideas of P. Bach-y-Rita and C. C. Collins in [BAC71], another pneumatic system for examinations in a functional magnetic resonance imaging device (fMRI), and a piezo-electric driven display for the fingers (see [MAU98]). However, the bandwidth of the tactile sense is much lower than the bandwidth of the visual sense. The human eye contains about 100 million photoreceptors. Their information is reduced in the retina by a factor of 100 and then transmitted to the visual cortex where further interpretation takes place. It does not seem to be possible to transfer such an amount of information via the skin. The fingertips or the tongue have a high density of tactile receptors but only a small surface, abdomen or back cover a large area but have a poor resolution of about one receptor per cm^2. Therefore, a strong but intelligent reduction of optical data has to be carried out in such a way that most of the essential information is preserved.

Consequently, the complete TVSS consists of three parts: image sensor, image processing unit and tactile display. An effective and common image processing method for extracting information out of a grey level image is edge detection. Different digital edge detection algorithms are known (some examples are given in [JAE93]), but they are either slow due to complex calculations or generate insufficient results. To overcome this problem an analog edge detection chip has been developed. It is able to process an image of 64×64 pixels in a few microseconds with a power consumption of about 1 μJ per frame. Realisation and performance are presented in [SCH99]. The resulting edges representing the object outlines can be either transferred directly to the tactile display or interpreted in further image processing steps with a computer.

To simplify the communication between camera and edge detection chip, additional features have been implemented in the image sensor. Because the camera resolution is higher than the edge detection resolution, only a part of the sensor frame can be processed at the same time. Random access to all pixels makes it possible to read out any subpart of the picture. Averaging of up to 8×8 pixels allows to obtain the image in a lower resolution which is useful for getting a first and fast impression of the whole scene. Adjustable offset and gain of the analog output signal enable an optimal adaptation to the input range of the processing chip. Other properties like digital output or video output with on-screen display are not required for the TVSS-project but strongly increase the number of possible applications especially in the field of image processing.

Chapter 1

Opto-Electronic CMOS Properties

This chapter describes the principal opto-electronic behaviour of devices in the standard CMOS process. The first part introduces the basic concepts of optical absorption, charge carrier diffusion and quantum efficiency and their relations to each other. The second part explains the different types of photodiodes and phototransistors which can be used for light detection. Simulated and measured quantum efficiencies are presented. Finally, the shielding of non-sensor circuits against light by the process metal layers is discussed.

Integrating optical sensors and processing electronics on the same chip offers attractive possibilities for smart sensor solutions. The CMOS[1] process uses silicon as base material which has a high absorption coefficient for electromagnetic radiation in the range of visible light. Consequently, incident light influences the behaviour of integrated electronic devices. To take advantage of this fact for realizing optical sensors and to minimize parasitic opto-electronic effects on the non-sensor electronics, an understanding of the principal interaction between light and silicon is important.

1.1 Photoelectric effect and charge carrier diffusion

Generally, the inner photoelectric effect of a semiconductor describes the absorption of electromagnetic radiation by transferring the photon's energy to an electron and lifting the electron to the conduction band. Depending on the material this interaction occurs in different wavelength ranges. In the following only the spectrum of visible light, slightly extended to the near infrared and the near ultraviolet, will be regarded. The corresponding wavelengths of 1000 nm $> \lambda >$ 300 nm result in photon energies of 1.24 eV $< E_{ph} <$ 4.1 eV due to the relation $E_{ph} = h\nu = hc/\lambda$ (h: Planck constant, c: speed of light).

1.1.1 Absorption

The absorption of radiation in semiconductors is based on the fact that incident photons can generate electron-hole pairs by raising electrons from the valence band to the conduction band. Assume that

[1] Complementary Metal Oxide Silicon

a semiconductor is illuminated from a light source with the intensity J_0. The number of photons dJ absorbed along the distance dx is proportional to the local intensity $J(x)$:

$$dJ = -\alpha\, J(x)\, dx \quad \text{or} \quad \frac{dJ}{dx} = -\alpha\, J(x). \tag{1.1}$$

The proportionality constant α is defined as the *absorption coefficient*. The negative sign indicates the decreasing intensity. The solution of this differential equation with the boundary condition $J(x) = J_0$ at $x = 0$ results in *Lambert's law of absorption* [BER93-1]:

$$J(x) = J_0 e^{-\alpha x}. \tag{1.2}$$

The absorption coefficient α depends on the photon energy and varies over several orders of magnitude. Figure 1.1 shows the wavelength dependency of α for silicon (Si) and gallium arsenide (GaAs).

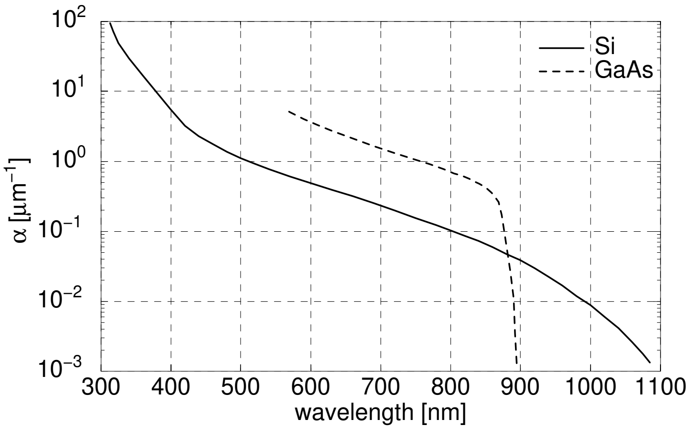


Figure 1.1: Absorption coefficient α for silicon (Si) and gallium arsenide (GaAs) [SZE85-1].

For energies below the bandgap E_g which is the difference between the energy levels of valence band and conduction band, photons do not possess enough energy to lift electrons to the conduction band. Therefore, silicon has a very low α and is nearly transparent for wavelengths larger than 1100 nm corresponding to the silicon bandgap of $E_g = 1.12$ eV [HUN93]. Nevertheless, a weak absorption even occurs in this region. The reasons are states in the bandgap due to crystal defects and absorption by free electrons brought to the conduction band by thermal excitation.

For energies exceeding E_g, α increases significantly. This is caused by a rising number of possible energy states for the excited electrons. The *density of states* can be calculated by taking into account that only standing electron waves in the semiconductor material are allowed. The wavelength λ of a standing wave is related to the length of the semiconductor L by

$$\frac{2L}{\lambda} = n \tag{1.3}$$

where n is an integer. Introducing the wave vector $k = \frac{2\pi}{\lambda}$ and substituting λ from equation 1.3 yields

$$k_x = \frac{\pi}{L} n_x \qquad k_y = \frac{\pi}{L} n_y \qquad k_z = \frac{\pi}{L} n_z \tag{1.4}$$

for the 3-dimensional case. Accordingly, all possible vectors in the k-space can be expressed by a cubical lattice with a distance of π/L between the lattice points. The volume of each individual electron state is thus equal to

$$V_{es} = \frac{1}{2} \left(\frac{\pi}{L}\right)^3. \tag{1.5}$$

The factor $1/2$ results from the electron spin. It allows to occupy each state with two electrons of opposite spin direction. The total number of states with $k \leq k_{max}$, where k_{max} is any given value, can be calculated by dividing the volume of a sphere with radius k_{max} by the volume V_{es} of a single electron state. Since k has to be positive, only one eighth of the sphere volume V_{sp} must be regarded, and the number of states amounts to

$$N = \frac{\frac{1}{8}V_{sp}}{V_{es}} = \frac{\frac{1}{8}\cdot\frac{4}{3}\pi k_{max}^3}{\frac{1}{2}\left(\frac{\pi}{L}\right)^3} = \frac{L^3 k_{max}^3}{3\pi^2}. \tag{1.6}$$

To express this equation as a function of energy we describe the electron energy E_n as a sum of the bandgap energy E_g and the kinetic electron energy E_{kin}

$$E_n = E_g + E_{kin} = E_g + \frac{p^2}{2m_n^*}, \tag{1.7}$$

where m_n^* is the *effective mass* of the electron. The momentum p is related to the wave vector k due to the equivalence of particles and waves: $k = 2\pi p/h$ with h as the Planck constant. Using this relation and substituting equation 1.7 into equation 1.6 we obtain the number of states per volume as

$$\frac{N}{L^3} = \frac{8\pi}{3h^3}(2m_n^*)^{3/2}(E_n - E_g)^{3/2}. \tag{1.8}$$

The density of states, which is the partial derivative of equation 1.8 with respect to the energy E_n [JON92], results in

$$\rho(E_n) = \frac{\partial(N/L^3)}{\partial E_n} = \frac{4\pi}{h^3}(2m_n^*)^{3/2}\sqrt{E_n - E_g}. \tag{1.9}$$

The density of states describes the density of allowed energy states in the conduction band per unit volume.

For GaAs and Si the band structures and the process of absorption are demonstrated in figure 1.2. In the case of GaAs the maximum energy level of the valence band and the minimum energy level of the conduction band are located at the same wave vector k. This is called a *direct* semiconductor since no change of the electron momentum is required for a transition with the bandgap energy E_g. A photon, which has a negligible momentum compared to the electron, can transfer its energy directly to the electron and raise it to the conduction band.

In silicon, which is an *indirect* semiconductor, the process of absorption becomes slightly more complicated. Since the minimum energy level of the conduction band has a different k-vector than the maximum of that of the valence band, a change of the electron momentum is necessary for a transition with the minimum energy E_g. This additional momentum is delivered by a phonon[2] of the semiconductor crystal. Thus, the electron has to interact simultaneously with the photon and the phonon. The probability of this indirect process is smaller than the probability of the direct process. Therefore, the absorption coefficient α of silicon (figure 1.1) rises slower with increasing energy than that of GaAs. At an energy of 3.1 eV ($\lambda = 400$ nm) the transition without momentum change also becomes possible in silicon (dashed arrow in figure 1.2). The transition probability increases and leads to a steeper rise of α.

The spectral variation of α has consequences for the spectral sensitivity of silicon photodetectors. Due to the weak absorption infrared and red light penetrates deeply into the semiconductor crystal whereas ultraviolet radiation is absorbed directly below the surface. Therefore, infrared receptors

[2]Oscillations of the crystal lattice can also be treated as particles and are called phonons.

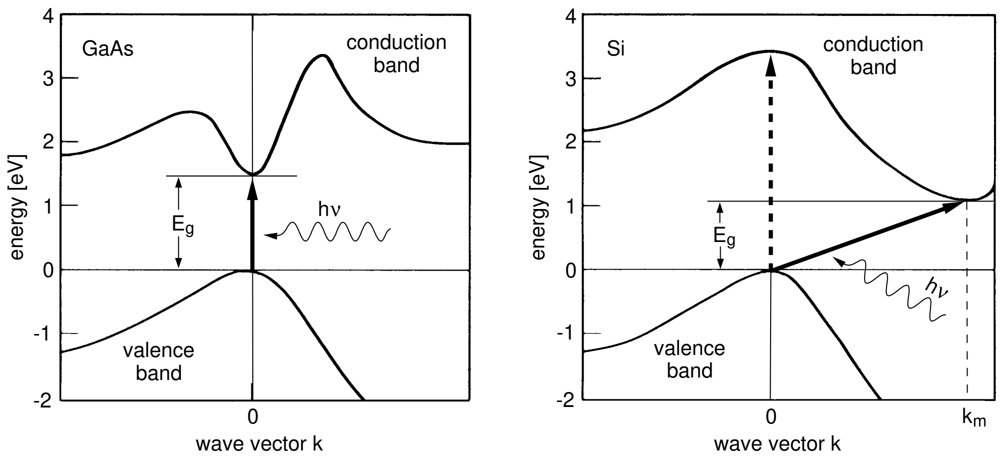


Figure 1.2: Energy band structures and optical absorption of the direct semiconductor GaAs and the indirect semiconductor Si (band structures taken from [SZE85-2]).

have to be largely extended into the substrate. Ultraviolet detectors, which are very inefficient in silicon, must be located near the surface. Table 1.1 gives three examples of the absorption length[3] at a temperature of 300 K.

wavelength (nm)	photon energy (eV)	absorption length (μm)
400	3.10	0.76
700	1.77	4.5
1000	1.24	110

Table 1.1: Absorption length in silicon at three different wavelengths.

1.1.2 Diffusivity and mobility

If there is a spatial variation of carrier concentration in the semiconductor material, for instance due to optical absorption, the carriers tend to move from a region of high concentration to a region of low concentration. This current is called *diffusion current*. Assuming that the number of electrons $n(x)$ varies in the x-direction we can consider the current density J_n flowing from left and right through the plane at $x=0$. Because of the finite temperature, the electrons show random thermal motions with a thermal velocity $v_{th}=l/\tau_c$ (l is the mean free path, τ_c the mean free time). In the mean free time τ_c, half of the electrons starting at $x=-l$ will move from the left across the plane $x=0$ and half of the electrons at $x=l$ will move from the right across $x=0$. Thus the resulting current density is

$$
\begin{aligned}
J_n = J_{left} - J_{right} &= \frac{1}{2}(-q)\cdot n(-l)\frac{l}{\tau_c} - \frac{1}{2}(-q)\cdot n(l)\frac{l}{\tau_c} \\
&= -\frac{1}{2}q\cdot v_{th}\cdot[n(-l)-n(l)] \qquad (1.10)
\end{aligned}
$$

[3] after covering the *absorption length* the incident intensity has decreased by a factor of e.

with the electron charge $-q$. Approximating the electron densities at $x=\pm l$ by the first two terms of a Taylor series expansion, we obtain

$$\begin{aligned} J_n &= -\frac{1}{2} q v_{th} \left[\left(n(0) - l\frac{dn}{dx} \right) - \left(n(0) + l\frac{dn}{dx} \right) \right] \\ &= q v_{th} l \frac{dn}{dx} = q D_n \frac{dn}{dx} \end{aligned} \tag{1.11}$$

where $D_n = v_{th} l$ is called the *diffusivity*. The theorem for the equipartition of energy, which means for this one-dimensional case

$$\frac{1}{2} m_n^* v_{th}^2 = \frac{1}{2} kT, \tag{1.12}$$

with the electron effective mass m_n^*, the Boltzmann constant k and the temperature T, can be substituted into equation 1.11 using the relation $l = v_{th}\tau_c$:

$$J_n = q D_n \frac{dn}{dx} = q \left(\frac{kT}{m_n^*} \tau_c \right) \frac{dn}{dx}. \tag{1.13}$$

Introducing the mobility $\mu_n = q\tau_c / m_n^*$ which describes the carrier velocity v_n in an electric field $\mathcal{E}$ ($v_n = \mu_n \mathcal{E}$) leads to a relation between diffusivity and mobility:

$$D_n = \frac{kT}{m_n^*} \tau_c = \frac{kT}{q} \mu_n. \tag{1.14}$$

This is known as the *Einstein relation*. It also applies between D_p and μ_p, the corresponding quantities for holes. At room temperature, $kT/q \approx 25\,\text{mV}$.

Figure 1.3 shows the measured mobility and diffusivity for Si as a function of the impurity concentration. The mobility of electrons is higher than that of holes due to the smaller effective mass

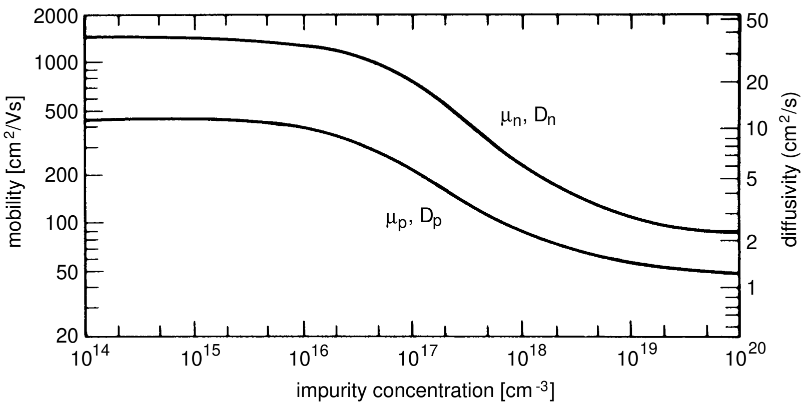


Figure 1.3: Mobility and diffusivity of electrons and holes in Si at 300 K [SZE85-2].

of electrons. The two major mechanisms determining the mobility are lattice scattering and impurity scattering. Lattice scattering which dominates at impurity concentrations below 10^{17} cm^{-3} (in this region μ_n and μ_p are almost independent of the impurity concentration) results from thermal vibrations of the lattice atoms. Since these vibrations become larger with increasing temperature the mobility decreases with temperature. The impurity scattering dominates at high doping concentrations (decreasing mobility in the right half of figure 1.3). It results from Coulomb force interaction between the charge carriers and ionized impurities. At higher temperatures it becomes less significant. The carriers move faster, remain near the impurity atom for a shorter time and are therefore less effectively scattered.

1.1.3 Diffusion length

The *diffusion length* describes the distance at which the number of charge carriers in the diffusion current has decreased by a factor of e. It plays an important role to determine the dimensions of the sensitive area of a photodetector. Carriers diffusing from outside into the photodetector influence the total receptor sensitivity and the crosstalk between adjacent receptors.

Assuming an electron injection at the left side of a semiconductor crystal (position $x=0$), the electron concentration decreases in the x-direction from the left to the right. The steady state can be described using the *continuity equation* for electrons [SZE85-2]

$$\frac{\partial n_p}{\partial t} = \frac{1}{q}\frac{\partial J_n}{\partial x} + (G_n - R_n). \tag{1.15}$$

G_n and R_n are the generation and recombination rate, respectively. The subscript p at the electron concentration n_p indicates that the electrons are minority carriers in a p-doped substrate. Because all electrons are injected from outside, the generation rate G_n inside the crystal is zero. The recombination rate R_n is proportional to the excess of electrons $\Delta n_p = n_p - n_{po}$ (n_{po} is the concentration without additional electron injection) and inversely proportional to the electron *lifetime* τ_n:

$$R_n = \frac{\Delta n_p}{\tau_n} = \frac{n_p - n_{po}}{\tau_n}. \tag{1.16}$$

Substituting eq. 1.13 and eq. 1.16 into eq. 1.15 and setting $\frac{\partial n_p}{\partial t}=0$ due to equilibrium gives

$$\frac{\partial n_p}{\partial t} = 0 = D_n\frac{\partial^2 n_p}{\partial^2 x} - \frac{n_p - n_{p0}}{\tau_n}. \tag{1.17}$$

The boundary conditions for this differential equation are $n_p(x=0) = n_p(0) =$ *constant value* and $n_p(x\to\infty)=n_{po}$. The solution for n_p is an exponential decay

$$n_p(x) = n_{po} + (n_p(0) - n_{po})\, e^{\frac{-x}{\sqrt{D_n\tau_n}}} = n_{po} + (n_p(0) - n_{po})\, e^{\frac{-x}{L_n}} \tag{1.18}$$

with the *diffusion length* of electrons as minority charge carriers

$$L_n = \sqrt{D_n\tau_n}. \tag{1.19}$$

The same relation holds for holes with the diffusion length $L_p = \sqrt{D_p\tau_p}$.

The electron lifetime τ_n in direct semiconductors is proportional to the reciprocal value of the hole concentration p_{po}, because a larger number of holes leads to a higher recombination probability. In indirect semiconductors like silicon the direct recombination process is very unlikely due to the additionally needed momentum exchange with the lattice. Therefore, the dominant process is indirect transition via localized energy states (or recombination centres) in the forbidden energy gap. The lifetime τ_n is significantly influenced by the density of recombination centres N_t. It can be proven that $\tau_n \propto 1/N_t$. Doping silicon with gold atoms increases N_t and decreases the lifetime. Typical lifetime is about $0.3\,\mu$s for τ_p in n-type silicon and about $1.0\,\mu$s for τ_n in p-type silicon at room temperature. Table 1.2 gives an example for the diffusion lengths calculated from the lifetime and the diffusivity.

carrier type	substrate doping (cm^{-3})	lifetime τ (μs)	diffusivity D (cm^2/s)	diffusion length $L = \sqrt{D\tau}$ (μm)	diff. length L (μm) measured [LAN98]
electrons	$1.45 \cdot 10^{17}$ (p_{po})	1.0	19	43.6	49.6
holes	$5.2 \cdot 10^{16}$ (n_{no})	0.3	7	14.4	

Table 1.2: Diffusion length in typical p-type and n-type silicon.

1.1.4 Quantum efficiency

The *quantum efficiency* is a measure for the spectral sensitivity of a photoreceptor. It is defined as the ratio of the number of measured electron-hole pairs N_q per time generated by the absorption process to the number of incident photons N_{ph} per time:

$$\eta = \frac{N_q/t}{N_{ph}/t} = \frac{I_{ph}/q}{P_{ph}/E_{ph}}. \tag{1.20}$$

I_{ph} describes the measured photocurrent, q the elementary charge, P_{ph} the power of the electromagnetic radiation and E_{ph} the energy of a single photon. Basically, the quantum efficiency η depends on the following three factors. Firstly, a part of the incident light intensity is reflected at the crystal surface or at different layers on top of the semiconductor in the CMOS-process. Only transmitted photons can contribute to the charge carrier generation. Secondly, the absorption behaviour of the detector material determines the spatially distributed generation of electron-hole pairs. It is described by the absorption coefficient α. Finally, the effectiveness of the charge carrier separation specifies the number of detected carrier pairs before recombination.

If a complete charge carrier separation is assumed and light reflection is neglected, the quantum efficiency can be calculated. The number of generated charge pairs N_q along the distance Δx is equal to the number of absorbed photons N_{abs}. Regarding the interval from x_0 to $x_0 + \Delta x$, N_q/t results in

$$\frac{N_q}{t} = \frac{N_{abs}}{t} = \frac{P_{ph}(x_0) - P_{ph}(x_0 + \Delta x)}{E_{ph}} = \frac{A\lambda}{hc}\left(J_{ph}(x_0) - J_{ph}(x_0 + \Delta x)\right) \tag{1.21}$$

with the photon energy $E_{ph} = hv = hc/\lambda$. A is the illuminated area and $J_{ph} = P_{ph}/A$ the radiation intensity. Expressing $J_{ph}(x)$ by Lambert's law (equation 1.2) yields

$$\frac{N_q}{t} = \frac{A\lambda}{hc} \cdot J_0 \cdot e^{-\alpha x_0}\left(1 - e^{-\alpha \Delta x}\right). \tag{1.22}$$

J_0 describes the total incident intensity. By substituting equation 1.22 into equation 1.20 and using $P_{ph} = J_0 A$, the quantum efficiency η can be written as

$$\eta = e^{-\alpha x_0}\left(1 - e^{-\alpha \Delta x}\right). \tag{1.23}$$

This relation shows that efficient photodetectors need a small value of x_0 and a large value of Δx. They should be located near the surface and deeply extended into the substrate.

The quantum efficiency in equation 1.20 leads to the photocurrent I_{ph} that can be generated by the absorbed photons

$$I_{ph} = \frac{\lambda}{hc} q \eta A J_0. \tag{1.24}$$

The resulting photocurrent of a receptor with an active area of $10 \times 10\ \mu m^2$ (typical size of a pixel photodiode in CMOS image sensors) is relatively low. With an intensity of $J_0 = 1$ W/m^2, a wavelength of $\lambda = 600$ nm and a quantum efficiency of 0.5 the photocurrent amounts to $I_{ph} = 24$ pA. This is three to six decades below the typical working current in MOSFETs[4]. Therefore specially adapted circuits are necessary that use transistors in the so-called *subthreshold region*. In this region the transistors are almost switched off and therefore work with low currents.

1.2 Photosensitive CMOS devices

Two types of devices can be used for photodetection in the standard CMOS process: photodiodes and phototransistors. Because most of today's CMOS applications have no requirements for photoreceptors, diodes and transistors are not optimized with regard to quantum efficiency or response time. Besides additional layers on top of the semiconductor for isolation or passivation reduce the incident light intensity. Consequently, they are somewhat less efficient than semiconductor devices specially built for photodetection. In the following, the properties of CMOS photodiodes and phototransistors will be described and discussed.

1.2.1 Photodiodes

Semiconductor diodes represent the connection of two layers with opposite doping (pn-junction). One layer, which is called n-type, is obtained by implanting donor atoms (atoms with 5 valence electrons like phosphorus or arsenic) during the production process. The other layer, called p-type, is fabricated by doping with acceptor atoms (3 valence electrons like boron). The doping concentration and the doping profile determine the electrical properties of the two layers and of the pn-junction.

In thermal equilibrium there is a depletion region between the two doped layers. Due to the concentration gradient of electrons and holes, respectively, a diffusion current arises trying to equalize the concentrations on both sides. The resulting electrical field generates a current in the opposite direction. In thermal equilibrium both currents compensate for each other. The magnitude of the electrical field depends on the concentration profiles. The diffusion potential or built-in potential V_{bi} caused by the diffusion current can be written as [SZE81]

$$V_{bi} = \frac{kT}{q} \ln \left(\frac{N_A N_D}{n_i^2} \right). \tag{1.25}$$

Here, N_A and N_D are the doping concentrations of acceptors and donors and n_i the intrinsic concentration of charge carriers at room temperature. The electric field in the depletion region leads to a separation of electron-hole pairs generated by absorption. Separated charge carriers can be measured as photocurrent. Therefore, the quantum efficiency of a photodiode is influenced by the width W_d of the depletion layer, which, in the case of an abrupt junction, can be approximated by [SZE81]

$$W_d = \sqrt{\frac{2\epsilon_{si}}{q} \left(\frac{1}{N_A} + \frac{1}{N_D} \right) (V_{bi} - V)} \tag{1.26}$$

where ϵ_{si} is the permittivity of silicon and V an externally applied voltage. Consequently, W_d is large for low doping concentrations and small for high doping concentrations. It can be additionally extended by increasing the external voltage V in reverse direction (negative sign).

[4] Metal Oxide Silicon Field Effect Transistor, the most important device in the CMOS process

In real semiconductor diodes there is no abrupt junction between n-layer and p-layer as assumed in equation 1.26. Instead, the doping concentrations show a gradient that varies with the position in the semiconductor. In the CMOS process the differently doped layers are produced by implantation or diffusion mechanisms that allow no sharp borders. Besides, during the successive steps of the production process, the doping profile changes due to thermal diffusion of the donor and acceptor atoms. The final doping concentration N of the three usable pn-junctions in the AMS[5] 0.8 μm CMOS process is shown in figure 1.4 as a functions of the depth z. The profiles are based on process simulation data of AMS and are taken from [DRO99]. Additionally, cross sections of the corresponding diodes can be seen in the lower part of the figure.

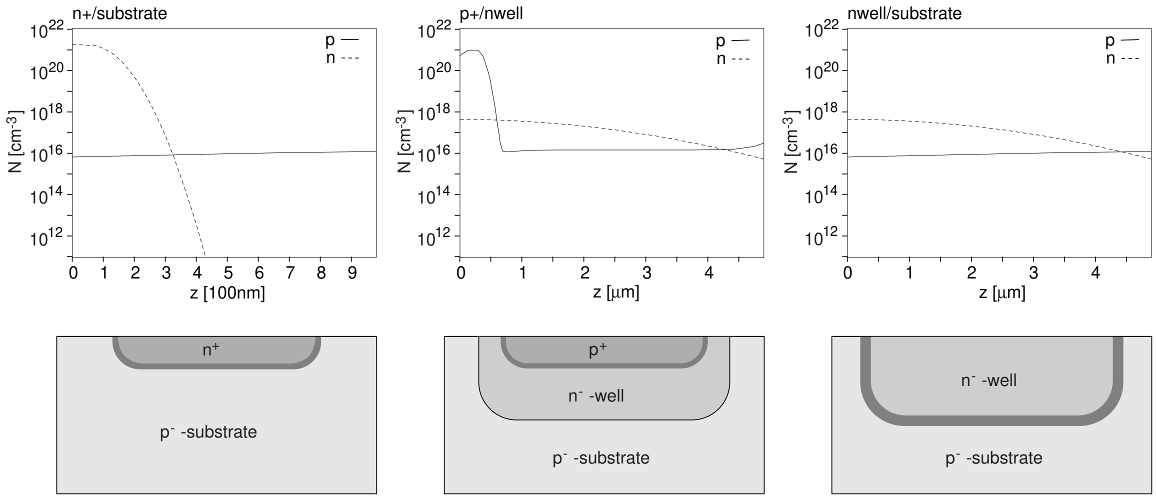


Figure 1.4: Doping profiles and cross sections of the three CMOS pn-junctions usable as photodiodes: n^+-substrate-diode, p^+-nwell-diode and nwell-substrate-diode.

On the basis of the given concentration profiles, simulations of the photodiodes were carried out in [SCH98] with the device simulator *ATLAS* [SIL95]. Figure 1.5 (taken from [DRO99]) shows the simulated quantum efficiencies of the 0.8 μm CMOS diodes as a function of the wavelength λ with an applied reverse voltage of $V = -2$ V. The data points drawn at a wavelength of 675 nm were measured in [LOO96-1] with photodiodes of the AMS 1.2 μm CMOS process. They confirm the simulation data with an error of less than 15%. The measured spectral quantum efficiency for the 0.8 μm n^+-substrate-diode can be seen in figure 1.6. The oscillation of η stems from interference effects in the passivation and oxide layers on top of the silicon wafer. The thickness l of the interference layer can be calculated by regarding the wavelengths of two neighbouring sensitivity maximums λ_1 and λ_2 with $\lambda_1 > \lambda_2$. These peaks result from constructional interference, that means for vertical illumination

$$2l = n_1 \frac{\lambda_1}{n_{SiO_2}} \quad \text{and} \quad 2l = n_2 \frac{\lambda_2}{n_{SiO_2}} \tag{1.27}$$

where n_1 and n_2 are integers and n_{SiO_2} is the refractive index of SiO_2. Due to the shorter wavelength λ_2 one additional wave cycle fits into the length l in comparison to the wavelength λ_1: $n_2 = n_1 + 1$. Substituting this relation into equation 1.27 and solving for n_1 yields

$$n_1 = \frac{\lambda_2}{\lambda_1 - \lambda_2}. \tag{1.28}$$

[5] Austria Mikro Systeme International AG

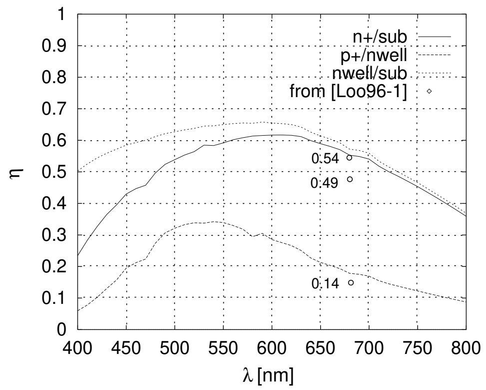


Figure 1.5: Simulated spectral quantum efficiency and three measured data points of the CMOS photodiodes [DRO99].

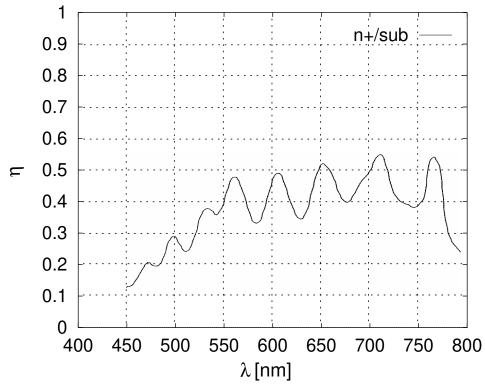


Figure 1.6: Measured spectral quantum efficiency of the n^+-substrate-diode [TEO97].

Taking the two peaks at $\lambda_1 = 710$ nm and $\lambda_2 = 652$ nm gives a number of wave cycles of $n_1 \simeq 11$. Thus, using equation 1.27 and $n_{SiO_2} = 1.46$ from literature, the thickness of the interference layer results in

$$l = \frac{n_1 \lambda_1}{2 n_{SiO_2}} = \frac{11 \cdot 710\,\mathrm{nm}}{2 \cdot 1.46} = 2.67\,\mu\mathrm{m} \tag{1.29}$$

Comparing this value to the AMS process parameters [AMS95-2] for the sum of oxide thickness and passivation thickness of about 2.69 μm proves that in fact the interference process occurs in these layers.

The different spectral quantum efficiencies shown in figure 1.5 are related to the different structure of the three types of photodiodes. Two effects influence the total sensitivity. On the one hand the width of the depletion layer determines the region where generated charge pairs are immediately separated and measured as photocurrent. On the other hand charge carriers generated somewhere else in the substrate can diffuse to the pn-junction. Hence, diodes with a large diffusion area show high quantum efficiencies. However, since diffusion is a slow process, these diodes suffer from long response times.

The p^+-nwell-diode is relatively inefficient due to the narrow depletion layer and mainly due to the small diffusion area. Charge carriers arising outside the nwell-layer are shielded by the nwell-substrate-junction and have no chance to be detected by the diode inside. In return, this leads to a very fast behaviour with short response time. The maximum of the sensitivity is located in the lower wavelength range at about $\lambda = 530$ nm. The reason is the location of the junction near the surface where most of the short-wave light is absorbed. The n^+-substrate-diode is more sensitive due to the wider depletion layer and the larger diffusion area which reaches deeply into the substrate. Therefore, also long-wave light can be efficiently detected, and the maximum of quantum efficiency occurs at about $\lambda = 620\,\mathrm{nm}$. However, the response time is increased compared to the p^+-nwell-diode owing to the slow diffusion process. Finally, the nwell-substrate-diode shows a similar behaviour. It is slightly more sensitive because the depletion zone is still larger and located deeper in the substrate.

Figure 1.7 shows the equivalent circuit of a photodiode used in reverse direction. It includes the current sources I_d and I_{ph} which represent the reverse saturation current (or dark current) and the photocurrent, respectively. The component C_j is the junction capacitance

$$C_j = A \sqrt{\frac{\epsilon_{si} q N_A N_D}{2(N_A + N_D)(V_{bi} - V)}} \tag{1.30}$$

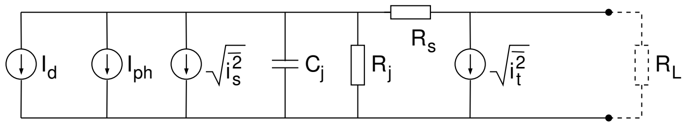


Figure 1.7: Equivalent circuit of a photodiode.

where A is the area of the pn-junction and N_A (N_D) the acceptor (donor) density [DRO99]. The junction resistance R_j is very high and can be neglected in most cases. The series resistance R_s can also be neglected because it is usually much smaller than the other resistances. R_L symbolizes an external load resistor. The dark current I_d caused by thermal generation of electron-hole pairs can be expressed as a function of the diffusion lengths L_n and L_p and the diffusivities D_n and D_p of the minority carriers

$$I_d = qAn_i^2 \left(\frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A} \right). \tag{1.31}$$

The absorption of photons and the generation of thermal charge pairs are statistical processes. Due to the randomness of these events, photocurrent and dark current contribute *shot noise* which is represented by the current source $\sqrt{\overline{i_s^2}}$. It can be written as

$$\overline{i_s^2} = 2q(I_{ph} + I_d)\Delta f \tag{1.32}$$

where Δf is the bandwidth of the system. Additionally, the thermal noise generally existing in resistors increases the total noise. It is given by the current source $\sqrt{\overline{i_t^2}}$ and amounts to

$$\overline{i_t^2} = 4kT \frac{1}{R_{eq}} \Delta f \tag{1.33}$$

with the equivalent resistance $R_{eq} = R_L \| (R_j + R_s)$. An important quantity describing the dynamic range of a system is the *signal-to-noise ratio* S/N. It is defined by the ratio of the usable signal to the system noise. Since the square roots of equation 1.32 and 1.33 give the rms[6] noise, the signal to be compared to this noise also needs to be a rms value (e.g. for a sinusoidal signal: amplitude/$\sqrt{2}$). Assuming that P_{ph} is the rms incident light power, the rms photocurrent yields $I_{ph} = q\eta P_{ph}\lambda/hc$ due to equation 1.24. If R_s is neglected, the ratio of signal power to noise power results in

$$\begin{aligned} \left(\frac{S}{N}\right)_{power} &= \frac{I_{ph}^2 (R_L \| R_j)}{(\overline{i_s^2} + \overline{i_t^2})(R_L \| R_j)} \\ &= \frac{\left(q\eta P_{ph} \frac{\lambda}{hc}\right)^2}{2q\left(q\eta P_{ph} \frac{\lambda}{hc} + I_d\right) + 4kT/(R_L \| R_j)} \cdot \frac{1}{\Delta f}. \end{aligned} \tag{1.34}$$

For a given photodiode (I_d, R_j and η fixed) and a given light power P_{ph}, the signal-to-noise ratio can be improved by increasing the load resistance R_L and decreasing the system bandwidth Δf within the specification limits.

1.2.2 Phototransistors

For the sake of completeness the properties of phototransistors are shortly described in this section, although no phototransistors are used in the developed image sensors. Basically bipolar transistors in normal operation mode show an amplification of the base-emitter current. When the base is floating,

[6] root mean square

the photo-generated carriers arising in the base-collector junction contribute a photocurrent in the collector. In addition, majority carriers generated in the base or swept into the base from the collector are compensated by the injection of minority carriers from the emitter into the base. The resulting base-emitter potential causes the transistor to work in active region. The total collector current can be written as

$$I_C = I_{ph} + h_{FE} I_{ph} = (1 + h_{FE}) I_{ph} \tag{1.35}$$

where I_{ph} is the photocurrent of the base-collector diode and h_{FE} the current gain of the transistor. Consequently the effective quantum efficiency of a phototransistor is $(1 + h_{FE})$ times larger than that of a photodiode and can be much larger than unity.

In the CMOS process two bipolar transistors (vertical and lateral pnp) exist. Usually, the vertical pnp-transistor is called a parasitic device because it always appears when p-channel MOSFETs are implemented. Doping profile [DRO99] and cross section of this pnp-transistor are shown in figure 1.8. Emitter (p^+-diffusion), base (nwell) and collector (p^--substrate) are vertically arranged. Figure 1.9 shows the effective spectral quantum efficiency simulated in the same way as the photodiodes in figure 1.5. The curve resembles that of the nwell-substrate diode since most of the amplified photocurrent is generated in the base-collector junction (= nwell-substrate diode). The sensitivity maximum is at about $\lambda = 630$ nm. The current gain, calculated by comparing the quantum efficiencies of photodiode and phototransistor, amounts to about $h_{FE} = 5.5$. Higher current gains can only be achieved by using special bipolar processes (BiCMOS) which offer an additional so-called *buried* layer deep in the substrate and an additional base sheet layer to form a high gain vertical npn-transistor.

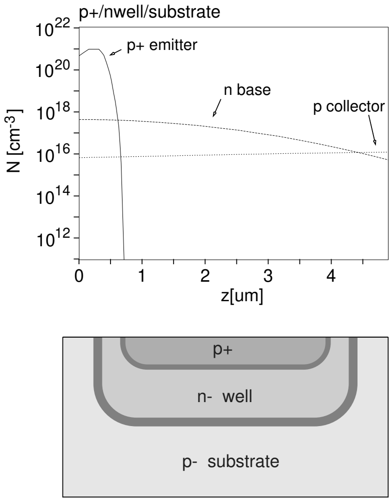


Figure 1.8: Doping profile and cross section of the vertical parasitic pnp-transistor.

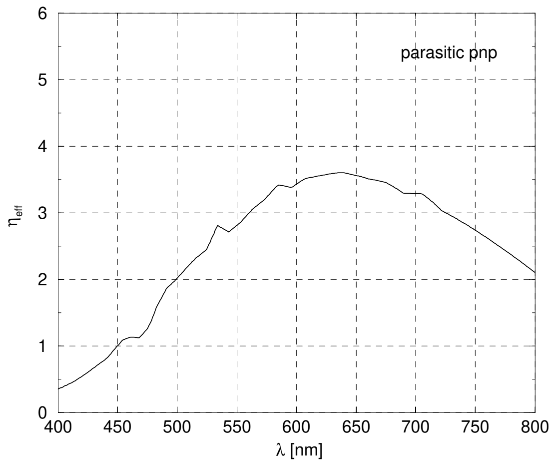


Figure 1.9: Simulated effective quantum efficiency of the parasitic pnp-transistor.

Despite the higher effective quantum efficiency, the use of transistors as photosensitive devices has two major drawbacks. At first, the dynamic range is lower than that of photodiodes. Since the noise increases by the factor h_{FE} as well, phototransistors have the same sensitivity at weak light intensities. At higher radiation power the current gain h_{FE} decreases and leads to a reduced quantum efficiency. The overall dynamic range is therefore reduced by about one decade. The second disadvantage is the response time of phototransistors. It is significantly reduced (factor of 100 or even more) in comparison to photodiodes due to the large base-collector capacitance which is additionally increased by the gain (feedback effect). Hence, photodiodes should be used for high dynamic range or high frequency photoreceptors.

1.2.3 Efficiency of metal shielding

All transistors that can be integrated in the CMOS process consist of the photosensitive pn-junctions described in section 1.2.1. For that reason, parasitic photocurrents influence the normal circuit properties when the chip is exposed to light. A reduction of this undesirable behaviour can be achieved by shielding the non-sensor devices against illumination. The easiest way is to use the metal layers always available in the CMOS process (usually for the electrical interconnection of the devices). No further processing steps are necessary because these layers are directly implemented during the normal production process (in contrast to lacquer layers that have to be applied afterwards). However, the possibilities for wiring are restricted since holes and isolation channels in the shielding metal layer should be avoided.

The efficiency of metal shielding was measured by [TEO97] for the AMS 0.8 μm CMOS process. This process provides two metal layers (aluminium, in the following called metal 1 and metal 2) which can be used for shielding. Figure 1.10 shows the remaining quantum efficiency of the n^+-substrate diode covered with metal 1. The interference pattern known from the diode in figure 1.6 basically remains, but the absolute values are reduced by more than three decades. To get an impression of the variation of the shielding effect as a function of the wavelength, the spectral attenuation which means $\eta_{shielded}/\eta_{unshielded}$ can be seen in figure 1.11. In the measured frequency range it is nearly constant, but shows slight remaining oscillations. These oscillations on the one hand result from the different interference structure on top of the shielded diode in comparison to the unshielded one. On the other hand the wavelength scales of the shielded and unshielded curve could be shifted a little toward each other due to measurement inaccuracies (see [TEO97]). The table on the right of each diagram contains the attenuation factor at 575 nm and the mean value, averaged from 450 nm to 800 nm.

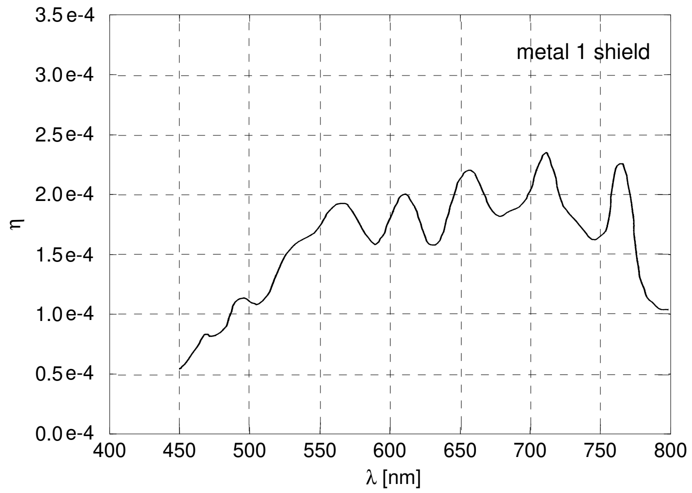
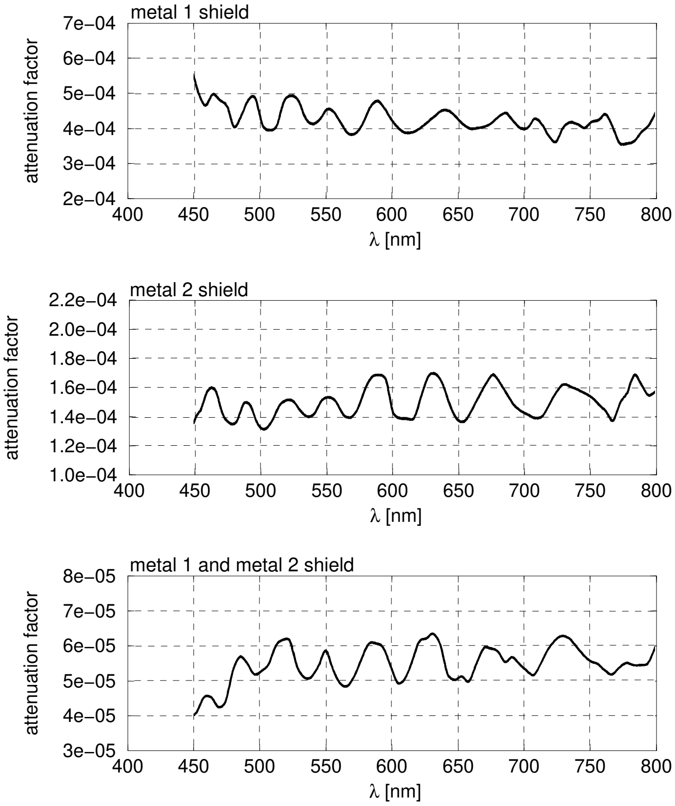


Figure 1.10: Measured spectral quantum efficiency of the n^+-substrate diode shielded by metal 1 [TEO97].

The shielding effect is caused by the light reflection on the metal surface and by the absorption in the metal layer. Both effects are, in first approximation, independent of the intensity. Due to the reflection only a fraction of the incident radiation which is called the transmittance $\mathcal{T}$ penetrates into the metal layer. The absorption of photons follows the same exponential law as in semiconductors (equation 1.2). Using the absorption coefficient α, the attenuation ratio of the remaining intensity J



metal 1 thickness: 0.6 μm

λ [nm]	attenuation
575	$3.9 \cdot 10^{-4}$
mean	$4.26 \cdot 10^{-4}$

metal 2 thickness: 1.1 μm

λ [nm]	attenuation
575	$1.6 \cdot 10^{-4}$
mean	$1.48 \cdot 10^{-4}$

metal 1+2 thickness: 1.7 μm

λ [nm]	attenuation
575	$5.2 \cdot 10^{-5}$
mean	$5.53 \cdot 10^{-5}$

Figure 1.11: Spectral attenuation factors of metal 1, metal 2, and metal 1+2 [TEO97].

to the incident intensity J_0 can be written as

$$\frac{J}{J_0} = \mathcal{T} \cdot e^{-\alpha l} \tag{1.36}$$

where l is the thickness of the shielding layer. The magnitudes $\mathcal{T}$ and α can be determined by using the measured attenuation values and the given thicknesses (AMS process parameters [AMS95-2]) of the two different metal layers. Solving equation 1.36 for $\mathcal{T}$ and α and substituting attenuation (at 575 nm) and thickness from figure 1.11 gives

$$\alpha = \frac{1}{l_2 - l_1} \ln \frac{(J/J_0)_1}{(J/J_0)_2} = \frac{1}{(1.1-0.6)\,\mu\mathrm{m}} \ln \frac{3.9 \cdot 10^{-4}}{1.6 \cdot 10^{-4}} = 1.78\,\mu\mathrm{m}^{-1} \tag{1.37}$$

$$\mathcal{T} = \left(\frac{J}{J_0}\right)_1^{\frac{l_2}{l_2-l_1}} \cdot \left(\frac{J}{J_0}\right)_2^{\frac{l_1}{l_1-l_2}} = (3.9 \cdot 10^{-4})^{\frac{1.1}{1.1-0.6}} \cdot (1.6 \cdot 10^{-4})^{\frac{0.6}{0.6-1.1}} = 1.14 \cdot 10^{-3} \tag{1.38}$$

where the subscripts 1 and 2 indicate metal 1 and metal 2, respectively. The very low value of $\mathcal{T}$ shows that most of the light is reflected and does not penetrate into the metal layer. This explains, why the attenuation of both metal layers combined is not the product of the individual ones as expected from the exponential law of absorption. The total attenuation of two shielding layers with an oxide layer in between yields

$$\frac{J}{J_0} = \underbrace{\mathcal{T} \cdot e^{-\alpha l_1}}_{\text{metal 1}} \cdot \underbrace{1/2 \cdot e^{-\alpha l_2}}_{\text{metal 2}}. \tag{1.39}$$

The factor 1/2 results from reflections inside the oxide layer. Once the light has passed the first metal layer, it is reflected many times between the two metal layers due to the low transmittance $\mathcal{T}$. Consequently, half of the photons leave the oxide through the upper layer and half through the lower layer. Using the values for $\mathcal{T}$ and α from eq. 1.37 and eq. 1.38, the theoretical attenuation of both metal layers can be calculated with eq. 1.39

$$\frac{J}{J_0} = 1.14 \cdot 10^{-3} \cdot e^{-1.78 \cdot 0.6} \cdot 1/2 \cdot e^{-1.78 \cdot 1.1} = 2.8 \cdot 10^{-5} \tag{1.40}$$

The result is a good confirmation of the measured value which is $5.2 \cdot 10^{-5}$ (from figure 1.11). The difference between both value amounts to merely 50 % on a scale of 5 decades. The remaining error can be caused by process variations or by slightly different reflection coefficients of metal 1 and metal 2.

The measurement results show that an effective shielding with the help of the process metal layers can be achieved. The attenuation of one layer nearly reaches 4 decades. However, to build sensor chips with a dynamic range of 6 or more decades, it has to be ensured that the remaining parasitic photocurrent does not affect the circuit's functionality.

Chapter 2

Fixed Pattern Noise and Existing Sensor Concepts

The problem of mismatch between individual identical CMOS devices, which represents a major difficulty in the design of image sensors, is presented and discussed. Some formulas describing the matching behaviour of MOS-transistors in strong and weak inversion are derived and compared to experimental data. In addition, specially designed test structures are examined to obtain information about the non-uniformity behaviour of the CMOS process used for the developed camera chip. Finally, a short summary of today's CMOS image sensor concepts including mismatch correction possibilities is given at the end of the chapter.

2.1 Device matching properties

Many integrated circuits rely on the assumption that devices identically drawn in the layout also show an identical behaviour in reality. If this is nearly the case, they are called *well-matched* devices. However, transistors, resistors or capacitors with the same geometrical extensions usually differ from each other due to a spatial variation of the process parameters. The consequences of this *mismatch* are improper current mirrors, operational amplifiers with high offset voltages and, in the case of image sensors, non-uniform output signals of the individual sensor pixels. Since the pixel variations are fixed but randomly distributed, the image shows the so-called *fixed pattern noise*. For practical use the fixed pattern noise has to be reduced to a value that is below the minimum intensity difference to be detected.

The observed distribution of the mismatches between two supposedly identical CMOS devices is primarily the result of two factors: 1. Variations in the location of the transistor, resistor or capacitor edges resulting from the limited imaging quality of the photolithographic process itself. This causes mismatches in length and width and thus different electrical behaviour. 2. Variations of the process parameters like gate oxide[1] thickness and doping concentration across the wafer resulting from non-uniform conditions during the predeposition and diffusion of the impurities. This causes the sheet

[1] thin layer between gate and channel of a MOS transistor

resistances and the threshold voltages[2] of the transistors to vary with distance across the die[3].

A large amount of additional mismatch is introduced by rotating or mirroring CMOS structures. This is caused by process parameters depending on the geometrical direction. The mismatch considerations in the following paragraphs refer to equal devices, that are neither mirrored nor rotated.

2.1.1 Transistor mismatch in strong inversion

To quantify the mismatch of MOS transistors, the variation of the drain current I_D is regarded. In the case of saturation, i.e. the gate-source-voltage V_{GS} is higher than the threshold voltage V_T and the drain-source-voltage V_{DS} is higher than $V_{GS} - V_T$, I_D can be expressed as

$$I_D = \frac{\beta}{2}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \quad \text{with} \quad \beta = \mu C_{ox}\frac{W_{eff}}{L_{eff}} \tag{2.1}$$

where λ is the channel length modulation parameter, μ the channel mobility and C_{ox} the gate oxide capacitance. The effective width W_{eff} and effective length L_{eff} of the transistor channel are smaller than the drawn parameter W and L due to lateral diffusion of the source and drain diffusions and due to blurred transition from the gate oxide to the field oxide[4]. The variation of the drain current I_D is caused by the variation of the two parameter β and V_T. Therefore, the standard deviation of the drain current $\sigma(I_D)$, which can be written as a quadratic summation of the individual errors caused by $\sigma(\beta)$ and $\sigma(V_T)$, yields

$$\begin{aligned}\sigma(I_D) &= \sqrt{\left(\frac{\partial I_D}{\partial \beta}\right)^2 \sigma^2(\beta) + \left(\frac{\partial I_D}{\partial V_T}\right)^2 \sigma^2(V_T)} \\ &= \sqrt{\left(\frac{(V_{GS} - V_T)^2(1 + \lambda V_{DS})}{2}\right)^2 \sigma^2(\beta) + \Big(\beta(V_{GS} - V_T)(1 + \lambda V_{DS})\Big)^2 \sigma^2(V_T)}. \end{aligned}\tag{2.2}$$

This relation describes the absolute error of I_D. To get the relative error, which in most cases is the more important information, equation 2.2 has to be divided by the drain current I_D from equation 2.1:

$$\frac{\sigma(I_D)}{I_D} = \sqrt{\frac{\sigma^2(\beta)}{\beta^2} + 4\frac{\sigma^2(V_T)}{(V_{GS} - V_T)^2}}. \tag{2.3}$$

Due to the second term on the right hand side (contribution of $\sigma(V_T)$) the mismatch of I_D should decrease for increasing gate voltages V_{GS}. On the other hand a decrease of V_{GS} worsens the mismatch of the drain current. If V_{GS} gets close to V_T, the variation of I_D strongly increases because the denominator becomes almost zero. Figure 2.1 shows some measurements confirming the expected behaviour. They were carried out in [LOV98] for NMOS devices in a 0.8 μm process. The significant increase near $V_T \simeq 0.8$ V and the decrease with higher gate voltages can be seen. The mismatch, however, does not totally become zero even at very high values of V_{GS} owing to the constant offset resulting from the first term in equation 2.3. The two curves correspond to two transistors possessing the same area but different W/L. The devices with shorter channel length and wider channel width show a poorer matching than those with longer channel length and narrower channel width. This is

[2]Gate voltage which represents the transition from weak inversion (subthreshold region, very low currents, exponential I-V_{GS}-behaviour) to strong inversion (linear and saturation region, medium to high currents, square I-V_{GS}-behaviour). Typical values of V_T are 0.7 - 0.8 V.

[3]The piece of silicon which includes all structures on its surface is called a *die* (or a *bar*).

[4]Field oxide is much thicker than gate oxide and covers the complete die beyond the area below the gate.

due to a higher threshold voltage mismatch $\sigma(V_T)$ and a higher $\sigma(\beta)$ for devices with large W/L ratios. Both influences are discussed in more detail in the following paragraphs.

The variation of the threshold voltage V_T depends on the effective transistor area $W_{eff} \cdot L_{eff}$. The expression

$$\sigma(V_T) = \frac{A_{VT0}}{\sqrt{W_{eff} L_{eff}}}, \tag{2.4}$$

derived in [PEL89], predicts the standard deviation σ of the threshold voltage mismatch for adjacent devices with equal effective area. In first approximation A_{VT0} is a constant. Equation 2.4 is confirmed by measurements shown in figure 2.2. The threshold voltage mismatch $\sigma(V_T)$ was determined in [LOV98] for PMOS devices in a 0.8 μm process. The drawn channel lengths varied from 0.8 to 6.66 μm and the drawn channel widths from 1.66 to 8.33 μm. Generally, the difference between drawn and effective length is higher than the difference between drawn and effective width. For a given drawn area short channel transistors (small L) thus have a smaller effective area than narrow channel transistors (small W). Hence short channel devices show a higher threshold voltage mismatch than narrow channel devices.

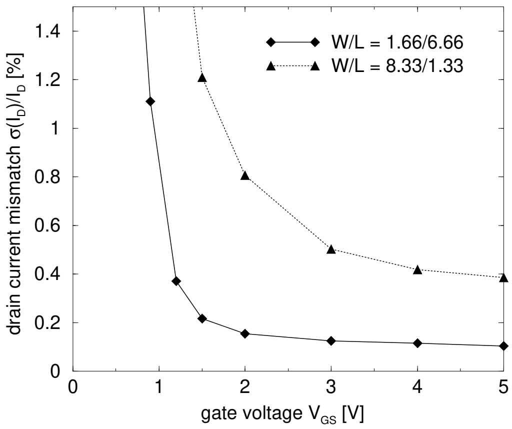


Figure 2.1: Drain current mismatch of NMOS transistors as a function of the gate voltage (data from [LOV98]).

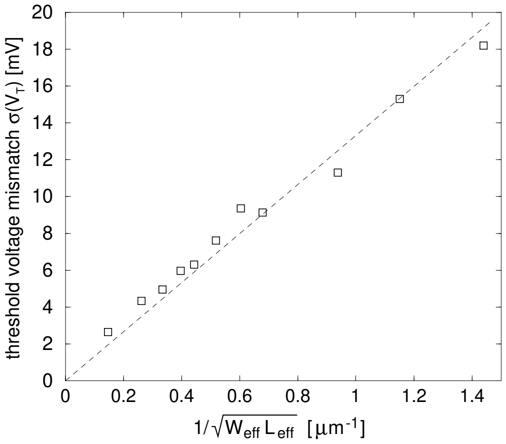


Figure 2.2: Threshold voltage mismatch of PMOS transistors plotted against $1/\sqrt{W_{eff} L_{eff}}$. A linear relationship is apparent (data from [LOV98]).

The second parameter variation that influences the overall drain variation in equation 2.3 is the mismatch of β. As shown is equation 2.1, β is a function of the channel mobility μ, the gate oxide capacitance C_{ox} and the ratio W_{eff}/L_{eff}. Since the gate oxide thickness is nearly constant for adjacent structures, C_{ox} variations only give a contribution to long range mismatch. The dominant source of short range mismatch of β is, besides the geometrical mismatch of W and L, the variation of the mobility [LAK86]. By considering β as a function of four random variables the following expression can be derived [LOV98]:

$$\frac{\sigma^2(\beta)}{\beta^2} = \frac{B_{W^2}^2}{W^2 L} + \frac{B_{L^2}^2}{L^2 W} + \frac{A_{\beta^2}^2}{WL} \tag{2.5}$$

where W and L refer to the drawn channel dimensions and B_{W^2}, B_{L^2}, A_{β^2} are constants. The first two terms on the right hand side are responsible for the difference in β mismatch between equal (small) area devices. When W and L are relatively large, both terms can be neglected due to their small influence on the complete sum. For a short channel device, however, the term $B_{L^2}^2/L^2 W$ becomes significant and inflates the β mismatch. The term $B_{W^2}^2/W^2 L$ is increased for a narrow width device, but not to the same extent as the short channel term owing to the smaller constant B_{W^2}. The general behaviour is described by the third term which follows the same trend as V_T mismatch (which means $\propto 1/\sqrt{WL}$). Substituting the V_T mismatch (equation 2.4) and the β mismatch (equation 2.5) into equation 2.3 gives the total theoretical drain current mismatch of transistors in strong inversion.

To determine the different behaviour of NMOS and PMOS devices, mismatch evaluations of the company AMS are regarded [AMS94]. Measured data of the drain current of different sized transistors leads to a simple empirical model for the relation between current mismatch and channel width and length. The relative error of I_D can be written as

$$\frac{\sigma(I_D)}{I_D} = \frac{A_W}{W} + \frac{A_L}{L} \tag{2.6}$$

where W and L describe the drawn channel dimensions and A_W, A_L are constants. This relation is similar to the previously derived equation 2.3 concerning the dependence on W and L. For $W/L = 1$ the $1/\sqrt{WL}$ behaviour can be easily seen by expanding the left fraction with $\sqrt{L/W}$ and the right fraction with $\sqrt{W/L}$. Using transistors of a 2.0 μm CMOS process in the range of $L = 2 \ldots 25\,\mu$m and $W = 2.4 \ldots 100\,\mu$m, the drain current mismatch was measured in strong inversion. The derived values for A_L and A_W are shown in table 2.1. To demonstrate the $1/L$ and $1/W$ behaviour with the steep rise at lower dimensions, the mismatch $\sigma(I_d)/I_d$ is drawn in figure 2.3 as a function of L and W, respectively.

NMOS	$A_W = 5.02 \cdot 10^{-2}\,\mu$m	$A_L = 3.94 \cdot 10^{-2}\,\mu$m
PMOS	$A_W = 13.45 \cdot 10^{-2}\,\mu$m	$A_L = 3.61 \cdot 10^{-2}\,\mu$m

Table 2.1: NMOS and PMOS drain current mismatch parameters [AMS94].

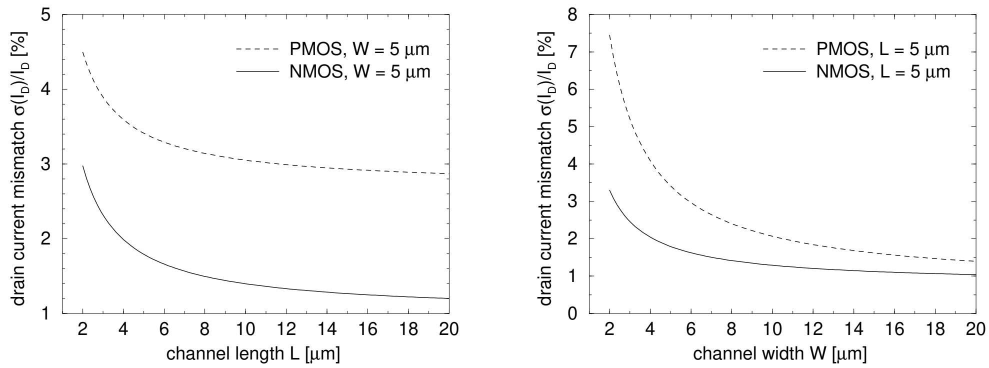


Figure 2.3: Drain current mismatch of NMOS and PMOS transistors as a function of the channel length (on the left) and the channel width (on the right) referring to the mismatch parameters in table 2.1.

Although the qualitative behaviour of PMOS and NMOS devices is the same, a difference exists in the mismatch magnitude. The PMOS parameter A_W is significantly increased compared to that of the NMOS, whereas A_L is more or less the same for both transistor types. Consequently the mismatch of PMOS devices is higher, especially for narrow channel transistors (diagram on the right in figure 2.3). The reason for the inferior PMOS matching properties could be related to three different circumstances. The first point is the different diffusion type which could be better controlled in the case of n-type diffusion. Secondly, in the p-substrate process the PMOS transistor is surrounded by the n-well. This layer, which is implanted in a special process step, could also introduce a larger mismatch. Finally, the PMOS devices usually would show a relatively high intrinsic conductivity even when they are completely switched off. To compensate for that additional ions are implanted in the gate oxide or the channel surface [LAK94-2]. They shift the threshold voltage and lead to a symmetric behaviour between both transistor types. This additional implantation step could be another reason for the increased mismatch of PMOS devices.

2.1.2 Transistor mismatch in weak inversion

So far mismatch has been regarded in the case of strong inversion where the drain current is a quadratic function of the gate voltage. In the case of weak inversion, which is also called the subthreshold region, a different current-voltage law applies. Assuming the bulk-source potential V_{BS} to be zero and $V_{DS} \gg V_t$, the drain current I_D can be expressed as [GEI90-1]

$$I_D = I_{D0} \frac{W}{L} e^{\frac{V_{GS}-V_T}{nV_t}} \quad \text{with} \quad I_{D0} \simeq \beta \frac{L}{W} \frac{2(nV_t)^2}{e^2} \tag{2.7}$$

where β is given in equation 2.1 and n is a process parameter (subthreshold slope factor) with typically $n = 1 \ldots 2$. The *temperature potential* V_t is equal to kT/q and must not be mistaken for the threshold voltage V_T. The parameter k is Boltzmann's constant, T is the device temperature and q is the elementary charge. At room temperature, $V_t \approx 25$ mV.

Due to the exponential relation between drain current and gate-source voltage, I_D varies over a large dynamic range of several decades (fA to nA) when V_{GS} varies from 0 V to V_T. Therefore, a high mismatch sensitivity, especially for variations of V_T, may be expected. The standard deviation of the I_D mismatch can be derived from equation 2.7 in the same way as carried out in equation 2.2

$$\begin{aligned} \sigma(I_D) &= \sqrt{\left(\frac{\partial I_D}{\partial \beta}\right)^2 \sigma^2(\beta) + \left(\frac{\partial I_D}{\partial V_T}\right)^2 \sigma^2(V_T)} \\ &= \sqrt{\left(\frac{2(nV_t)^2}{e^2} e^{\frac{V_{GS}-V_T}{nV_t}}\right)^2 \sigma^2(\beta) + \left(\beta \frac{2nV_t}{e^2} e^{\frac{V_{GS}-V_T}{nV_t}}\right)^2 \sigma^2(V_T)} \end{aligned} \tag{2.8}$$

To obtain the relative error of current mismatch, the absolute error from equation 2.8 is divided by the expression for I_D in equation 2.7:

$$\frac{\sigma(I_D)}{I_D} = \sqrt{\frac{\sigma^2(\beta)}{\beta^2} + \frac{\sigma^2(V_T)}{(nV_t)^2}}. \tag{2.9}$$

Two major differences with respect to the strong inversion mismatch can be deduced from the above relation. On the one hand $\sigma(I_D)/I_D$ is not any longer a function of V_{GS}. Hence it is constant in the complete subthreshold region[5]. On the other hand the contribution of the V_T mismatch is much higher. Since $\sigma(V_T)$ is only divided by nV_t which is in the region of 25 mV, measured threshold voltage variations of about 20 mV (cf. figure 2.2 for small transistors) can lead to a drain current mismatch of nearly 100 %. Therefore subthreshold devices have to be designed very carefully to reduce the mismatch itself or at least its influence on the circuit behaviour.

Additional measurements of the mismatch behaviour in weak inversion are described in [DRO99]. Here relatively large transistors ($W/L = 10/6$) are regarded in a 0.6 μm CMOS process. They are

[5] This is only valid in first approximation because the used equations and assumptions are approximations in many respects, too. For example the parameter n also shows a slight mismatch destroying the independence of V_{GS}.

arranged in pairs with a spacing of 70 μm. Table 2.2 lists the measured drain current mismatch $\sigma(I_D)/I_D$ for PMOS and NMOS devices. The values are obtained by averaging the standard deviations measured at different gate-source and drain-source voltages. The first row refers to structures on the same die. The second row is based on measurements of the same transistors on different dies (but corresponding to the same production run). Again, the higher mismatch of PMOS in comparison to NMOS transistors is apparent. Besides, a significant mismatch increase arises by considering devices that are far away from each other during the production process. In the case of different dies, i.e. large transistor-transistor spacing, the matching gets worse by a factor of 3 to 4. The reason is that process parameters show larger variations over the complete wafer than in small parts of it.

measured transistors	$\sigma(I_D)/I_D$ NMOS	$\sigma(I_D)/I_D$ PMOS
devices on the same die	0.09	0.11
devices on different dies	0.23	0.44

Table 2.2: Drain current mismatch in weak inversion with the channel dimensions of $W/L = 10/6$ (data taken from [DRO99]).

Particularly in the case of image sensors, the subthreshold devices are frequently used as logarithmic compressors. This means that the exponential current-voltage law is reversed into a logarithmic voltage-current law. Solving equation 2.7 for the gate voltage V_{GS} gives

$$V_{GS} = V_T + 2nV_t - nV_t \ln \frac{2\beta(nV_t)^2}{I_D}. \tag{2.10}$$

Since V_{GS} is a function of the logarithm of I_D, current ratios are converted into voltage differences. Hence not the relative but the absolute error $\sigma(V_{GS})$ is the interesting magnitude for mismatch considerations. Using equation 2.10 and following the derivation in equation 2.8 yields

$$\sigma(V_{GS}) = \sqrt{\sigma^2(V_T) + \left(\frac{nV_t}{\beta}\right)^2 \sigma^2(\beta)}. \tag{2.11}$$

Here, the mismatch of V_{GS} directly depends on the threshold voltage variations $\sigma(V_T)$. Besides, it is independent of the drain current I_D and therefore constant in the complete subthreshold region[6]. Some measurements concerning the V_{GS} mismatch are presented in the next section.

2.2 Evaluation of test structures

2.2.1 Design and layout

For the development of the image sensor, the AMS 0.6 μm CMOS process was best suited among the available processes. To examine the matching behaviour of transistor devices in this process special test structures were designed and measured. They should help to understand the fixed pattern noise problem and to evaluate the quality of subthreshold current mirrors. Measurements focused on two aspects: 1. V_{GS} mismatch of small transistors leading to the fixed pattern noise of logarithmic photoreceptors (a more detailed description of this kind of receptor is given in the next section).

[6] Assuming again, that n is constant.

2. I_D mismatch of relatively large transistors which is important for the self-calibration concept of the developed image sensor.

The test structure consists of one column of 64 identical elementary cells. The circuit diagram of one cell is shown in figure 2.4. It includes a photoreceptor and a large NMOS transistor. Using this elementary cell, the test column is continued in the upward and downward direction. To select an individual cell, a shift register consisting of one flip-flop per cell has been implemented. A high level at the output Q of the flip-flop switches on the transistors M_3 and M_4 and enables the corresponding photoreceptor and test transistor. The shift register is initialized by storing a logical one in the first cell and resetting all others. Subsequently, every clock cycle shifts the selection bit from one cell to the next. In this way every elementary cell can be selected by applying the corresponding number of clock cycles to the shift register.

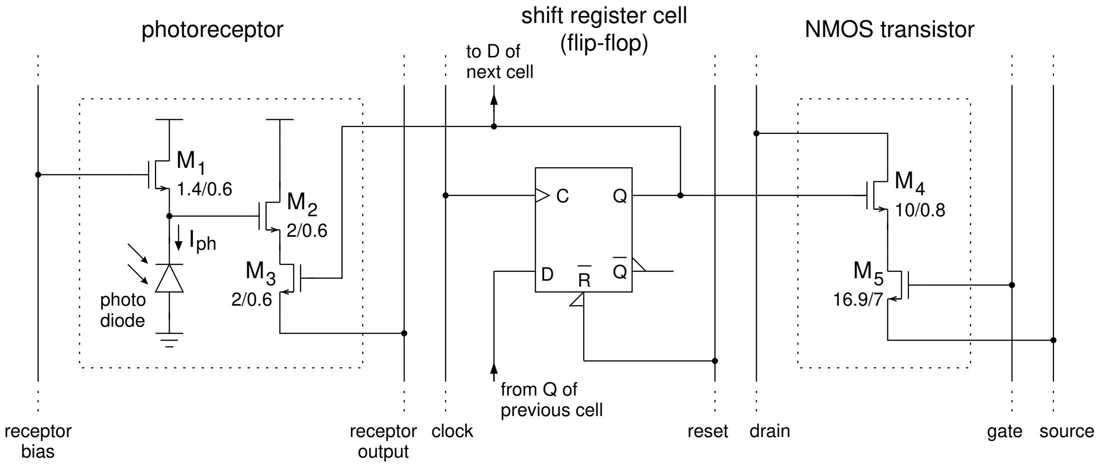


Figure 2.4: Circuit diagram of one elementary cell of the test column including photoreceptor, flip-flop and large NMOS transistor.

The channel dimensions of every transistor are given by the W/L ratio written below the transistor identifier M. The photoreceptor circuit implemented in the test column basically consists of the photodiode and the transistor M_1. The photocurrent generated by optical absorption in the diode flows through M_1. Due to the low photocurrent I_{ph} (cf. section 1.1.4) M_1 works in weak inversion. Therefore, the gate-source voltage V_{GS} is a function of the logarithm of I_{ph}. Since the gate voltage is fixed by the receptor bias line, the source potential (node between diode and transistor) shows a logarithmic dependence on the photocurrent. For readout this source potential is buffered by the transistor M_2 working as a source follower. The necessary bias current is provided for all buffers by one additional transistor at the end of the column. By buffering with the help of a source follower circuit, the signal amplitude of the photoreceptor is slightly reduced since the voltage gain is less than one. However, this signal reduction has no influence on the mismatch measurements since the mismatch is decreased by the same factor.

Mismatch of the individual photoreceptors in the test column mainly results from V_{GS} mismatch of the subthreshold transistor M_1. The photodiodes match well due to their large area of $13 \times 18\ \mu\text{m}^2$. Besides, the buffer transistor M_2 only produces a small mismatch contribution because it is driven in the saturation region. Therefore the photoreceptor mismatch, or in other words fixed pattern noise, can be described by equation 2.11. A relatively large fixed pattern noise is expected owing to the small size of M_1. However, larger channel dimensions would significantly increase the transistor capacitance. Since the low photocurrent has to charge this capacitance, the receptor circuit would become slow in the case of large transistor dimensions.

The other test circuit in the elementary cell, which is the single NMOS transistor M_5, has been implemented with large W and L values. Therefore, a good matching of these devices can be expected. To minimize the influence of the switch transistor M_4 its W/L ratio is higher than that of M_5. Consequently, the mismatch contribution of M_4 can be neglected due to its relatively low resistance. The drain current mismatch is described by equation 2.3 (strong inversion) or equation 2.9 (weak inversion) depending on the applied gate-source voltage. To reduce the number of switching devices only the drain node can be selected, whereas the gate as well as the source nodes of all transistors are permanently connected to the same gate and source line, respectively.

Figure 2.5 shows the layout of one elementary cell of the test column. Additionally, the upper part of the previous and the lower part of the subsequent cell can be seen at the bottom and top border. Generally, MOS transistors in the layout can be recognized by the intersection of diffusion and polysilicon layer representing the gate area. The diffusion type is determined by the surrounding nplus layer for n^+-diffusion and the surrounding pplus layer for p^+-diffusion. Contacts connect diffusion or polysilicon with the routing layer metal 1, whereas metal 1 and metal 2 are connected by vias. The dominant structure on the left side is the large diffusion area representing the n^+-substrate photodiode of the photoreceptor. The small subthreshold transistor responsible for the logarithmic behaviour is directly connected to the diode by using the diode diffusion as source node of the transistor. In the middle part the complex structure of the shift register flip-flop can be seen. It is taken from the digital standard cell library[7] provided by AMS. The right part contains the large NMOS-FET and the corresponding selection transistor. All vertical readout and control lines going through the complete column are indicated.

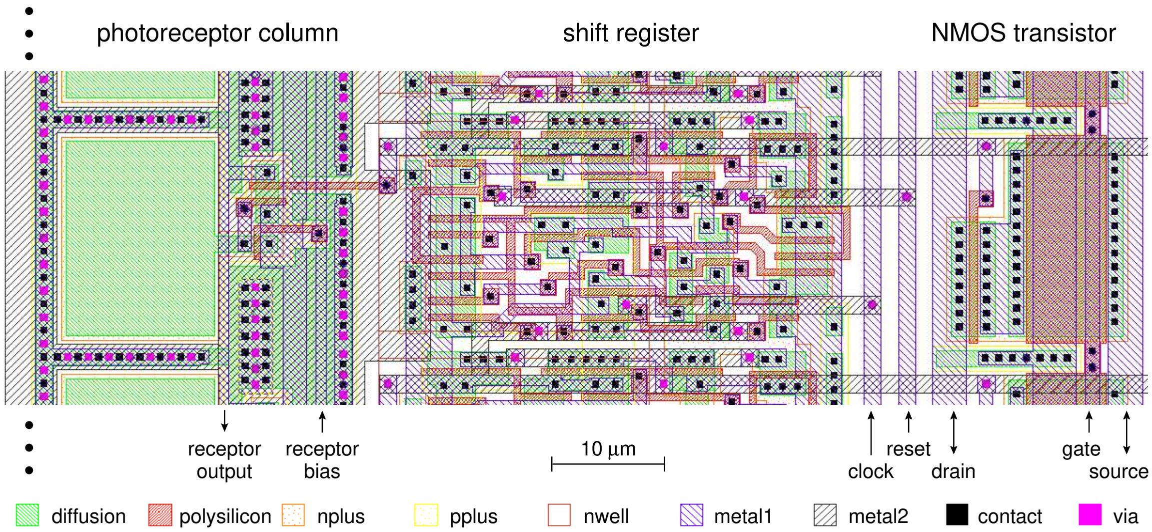


Figure 2.5: Cutout of the test structure layout. It shows one column cell consisting of logarithmic photoreceptor, selection shift register (flip-flop) and NMOS transistor.

2.2.2 Measurement results

Both the photoreceptor and the single MOSFET were examined on two individual chips. Firstly, the results of the photoreceptor obtained by optical measurements are presented. In the following the

[7] Layouts of basic digital components are usually provided by the production company for automatic generation of digital logic blocks.

expression *pixel* (from *pic*ture *el*ement) is equivalently used in place of photoreceptor. The offset distribution of the individual pixel signals were measured by illuminating the complete test structure with white light of a xenon arc lamp. With the help of neutral density filters different intensities covering a large dynamic range could be achieved. Since each filter decreases the intensity by a factor of 10, the total reduction amounts to $(10\%)^n$, where n is the number of used filters. The receptor bias potential was adjusted to 3.5 V for all measurements.

Figure 2.6 shows the measurement results. The diagrams are labelled with chip 1 and chip 2, respectively, according to the two examined dies. Part a) represents the offset distribution as a function of the pixel number at three different intensities. The variations are more or less random, no systematic behaviour is apparent. However, as expected, the mismatch magnitude is very high. Although the curves correspond to light intensities which differ from each other by two decades in each case, they show peak-peak-variations larger than the output voltage difference between two curves.

Part b) of figure 2.6 contains the averaged response curve measured at 6 illumination intensities in a dynamic range of 5 decades. The almost linear behaviour results from the logarithmic scale on the intensity axis. The negative slope is a property of the receptor architecture. Due to the linear relation between light power and generated photocurrent, the intensity is proportional to the receptor current. Therefore, a higher intensity (which means a higher photocurrent) leads to a higher gate-source voltage V_{GS}. Since the pixel output is the difference between the fixed gate potential and V_{GS},

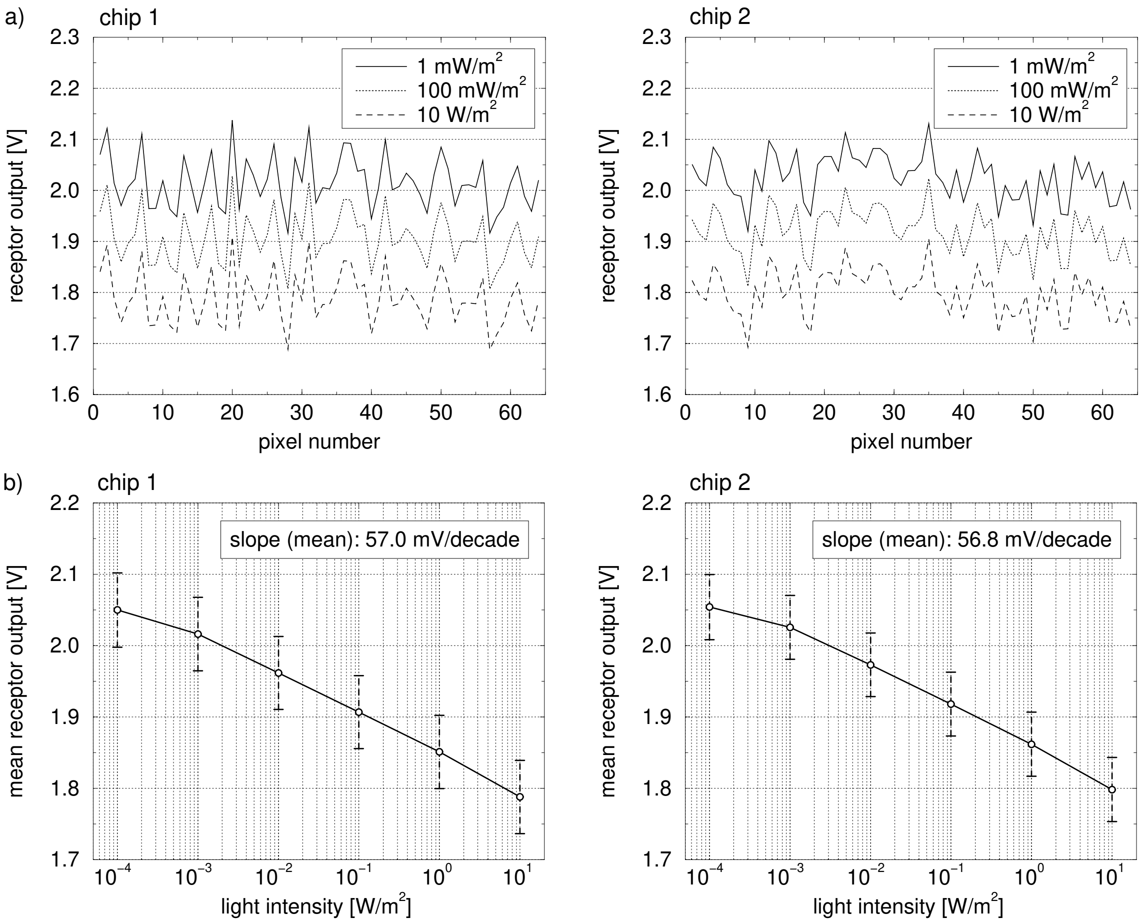


Figure 2.6: Measured offset distributions and response curves of all photoreceptors included in the test column at different illumination intensities.

it decreases with increasing V_{GS}. The slope averaged over 4 decades is about -57 mV/decade. For the sake of simplicity, the negative sign is disregarded in further considerations. The error bars represent the standard deviation of the pixel offset variations (fixed pattern noise). The measured mean and mismatch values of the receptor output V_{out} are given in table 2.3. Additionally, the last table row contains a kind of relative mismatch error obtained by dividing the absolute error by the averaged slope. The result is independent of the slope and is comparable to the relative error $\sigma(V)/V$ of linear systems.

chip 1

intensity [W/m^2]	10^{-4}	10^{-3}	10^{-2}	10^{-1}	10^{0}	10^{1}
$\overline{V_{out}}$ [V]	2.050	2.016	1.962	1.907	1.851	1.788
$\sigma(V_{out})$ [mV]	52.0	51.4	51.2	51.2	51.2	51.3
$\sigma(V_{out})/slope$ [% of a decade]	91.2	90.2	89.8	89.8	89.8	90.0

chip 2

intensity [W/m^2]	10^{-4}	10^{-3}	10^{-2}	10^{-1}	10^{0}	10^{1}
$\overline{V_{out}}$ [V]	2.054	2.026	1.973	1.918	1.862	1.798
$\sigma(V_{out})$ [mV]	45.7	44.8	44.7	44.8	44.9	45.0
$\sigma(V_{out})/slope$ [% of a decade]	80.5	78.9	78.7	78.9	79.0	79.2

Table 2.3: Mean value and mismatch of the photoreceptor column at different intensities.

Regarding the large mismatch which nearly reaches values corresponding to one intensity decade, it is obvious that image sensors consisting of these photoreceptors need some kind of mismatch correction. Otherwise, the image information of common scenes (e.g. contrast of dark script on white paper is less than one decade) would disappear in the sensor's fixed pattern noise. To decide, if a simple offset subtraction is sufficient or a higher dimensional correction has to be carried out, the slope variations have to be considered. The distribution of all pixel slopes averaged over 4 decades can be seen in figure 2.7. The slope variations are below 0.5 mV/decade which corresponds to a maximum relative error of $\sigma(slope)/slope \leq 0.85$ % for one decade. This small magnitude is a good confirmation of the fact that the subthreshold slope factor n in equation 2.7 is relatively constant. Assuming a dynamic range of 6 decades and a one point correction in the middle of this dynamic range, intensity signals can differ at most by 3 decades from the calibration point. Hence, the maximum contribution of slope variations to the overall fixed pattern noise is 3×0.85 % $= 2.6$ % of a decade. Consequently, no correction of the slope mismatch is required as long as the applied offset correction leads to a remaining fixed pattern noise higher than 2.6 %. However, for a further decrease of the fixed pattern noise not only the offset but also the slope variations have to be regarded. This at least means a two point correction concept.

The slope factor n of the used CMOS process can be calculated by using equation 2.7. It should be noted, that this is only an approximation, since the bulk effect is completely neglected. To obtain the real receptor voltage V_{GS}, the measured output signal has to be multiplied by the reciprocal gain factor of the pixel source follower. The gain of this buffer stage amounts to about $\nu = 0.8$. Solving the ratio of two photocurrents I_{D1}/I_{D2} for n and substituting the measured averaged slope divided by ν yields

$$n = \frac{V_{GS1}/\nu - V_{GS2}/\nu}{V_t \ln(I_{D1}/I_{D2})} = \frac{slope}{\nu V_t \ln 10} = \frac{56.9\,\text{mV}}{0.8 \cdot 25\,\text{mV} \cdot \ln 10} = 1.24 \tag{2.12}$$

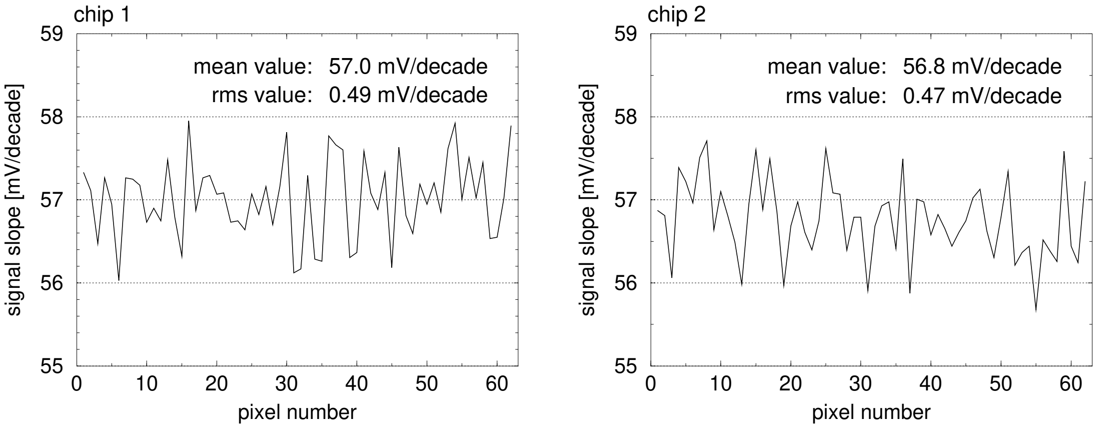


Figure 2.7: Slope distribution of the photoreceptors.

The mismatch of n can be determined by substituting the slope variations of 0.5 mV into equation 2.12. The standard deviation results to $\sigma(n) = 1.09 \cdot 10^{-2}$ corresponding to a relative error of $\sigma(n)/n = 0.88$ %.

The focus of the second measurements is on the 64 individual large MOS transistors located on the right in figure 2.5. They were examined with the help of a parameter analyser. It is able to measure the characteristic transistor curves down to drain currents in the sub-pA region. To determine the device mismatch, the individual drain currents were measured at 4 different gate-source voltages. Two of them lead to a biasing in strong inversion ($V_{GS} = 1\,\text{V}$, 2 V), the other ones make the MOSFETs to work in weak inversion ($V_{GS} = 0.5\,\text{V}$, $0.6\,\text{V}$). During all measurements the drain-source voltage was adjusted to $V_{DS} = 3\,\text{V}$. Figure 2.8 shows the drain current distributions as a function of the transistor number. The corresponding mean values, rms values and the relative errors in percent are summarized in table 2.4.

Due to the large transistor dimensions the overall mismatch is relatively small. As predicted from theory the variations increase with decreasing V_{GS} in strong inversion (cf. equation 2.3) and remain constant at a high level in weak inversion (cf. equation 2.9). The maximum mismatch in the subthreshold region amounts to about 3 %. Using these transistors in place of the small ones for the logarithmic photoreceptors, the fixed pattern noise would decrease to only a few % of a decade. However, the capacitance of the large transistors is about 150 times higher than that of the small devices used for the measured receptors. Therefore, the receptor circuit would be significantly slowed down. Besides, the pixel size is increased, which is an important argument in the case of 2-dimensional sensor arrays.

chip no.	chip 1				chip 2			
V_{GS} [V]	2.0	1.0	0.6	0.5	2.0	1.0	0.6	0.5
$\overline{I_D}$ [A]	116.1 μ	1.76 μ	573 p	50.5 p	116.6 μ	1.83 μ	620 p	55.0 p
$\sigma(I_D)$ [A]	0.36 μ	27 n	19 p	1.5 p	0.52 μ	27 n	19 p	1.5 p
$\sigma(I_D)/I_D$ [%]	0.31	1.5	3.3	3.0	0.45	1.5	3.0	2.7

Table 2.4: Mean value and standard deviation of the NMOS transistor current ($W/L = 16.9/7$).

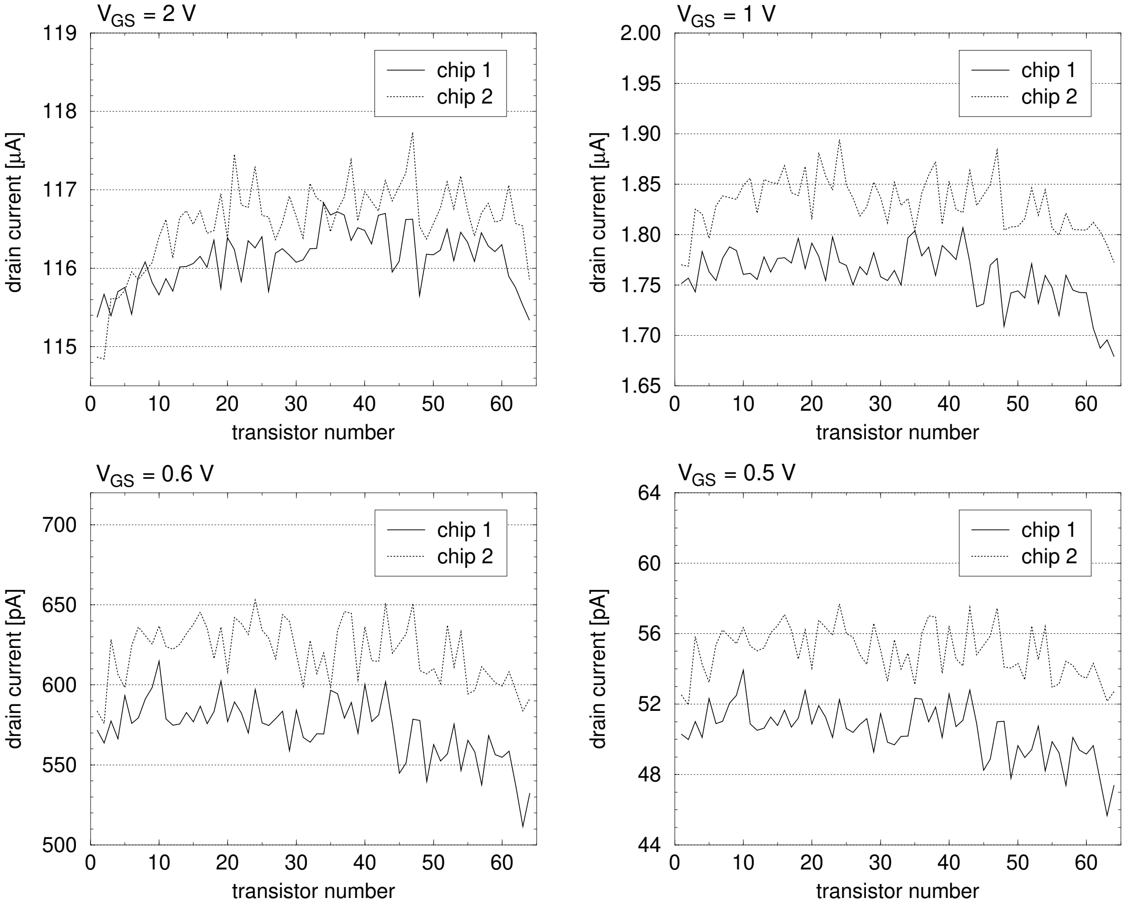


Figure 2.8: Drain current distribution of the 64 NMOS transistors at different gate-source voltages.

Although their capacitance makes the large devices inapplicable for logarithmic photoreceptors, their small mismatch can be of advantage for other subthreshold circuits. In the case of the self-calibration concept, which will be presented in the next two chapters, well matching current mirrors are required. They have to generate the same reference current for every sensor column. Since the current stays constant with time, here the large transistor capacitances show a negligible influence on the circuit behaviour.

2.3 Common CMOS image sensor concepts

The integration of photodetectors together with processing electronics leads to a complete vision system on a chip. The photosensitive array of these so-called *vision chips* can consist of very different pixel types. If the pixel circuit only includes the sensing element and a readout amplifier, it is called an active pixel and the complete chip an *active pixel sensor* (APS). Its capabilities are limited on transformation of light into electrical signals and signal amplification. By integrating more and more additional electronics in the receptor circuit, the vision chip becomes able to perform certain image processing tasks directly in the pixel. These so-called *smart pixels* can include up to several hundred transistors. However, the transition from active pixel sensors to smart sensors is not exactly determined. Some APSs possess additional circuitry in the pixel that makes them not really, but kind of smart.

The basic circuits most frequently used in CMOS photoreceptors are shortly presented in the following sections. The description concentrates on APS circuits, but also one example of a smart pixel is given. Generally, the pixel concepts can be divided in two groups: integration based photoreceptors and continuously working photoreceptors. Properties of both are discussed, especially with respect to their mismatch behaviour and possible fixed pattern noise reduction methods. An excellent overview of today's vision chip concepts and realizations with the focus on smart sensing can be found in [MOI97].

2.3.1 Integration based photoreceptors

The concept of integrating CMOS photoreceptors, which is similar to that of CCDs[8], is used in most of the commercially available imagers. The basic circuit diagram consisting of charge integration and a sample-and-hold stage is shown in figure 2.9. Initially, the reset transistor is turned on and the voltage at the input node V_{in} is set to the reset value V_{dd}. Then, this transistor is turned off and the photocurrent charges up the input capacitance at the input node. The capacitance is usually comprised of the parasitic capacitances C_p of the devices connected to this node. The major contribution results from the photodiode which covers a large area for high sensitivity. To obtain longer storage times and to reduce the voltage swing, the load capacitance can be increased by an additional capacitor.

The sample-and-hold stage can often be removed since the readout time is usually very short in comparison to the integration time. Therefore, the output voltage V_{out} only changes a little during readout, although the pixel is still integrating. Besides, in the case of no sample-and-hold stage, some of the photodetectors are integrating while others are being read out. Thus, an appropriate timing control has to ensure that the integration time is the same for all pixels. An example of an APS photodetector without sample-and-hold stage is shown is figure 2.10. It uses a source follower circuit for buffering the pixel voltage V_{in}. The row select signal enables the individual buffers of one row, and the corresponding column line can be read out at the border of the sensor array.

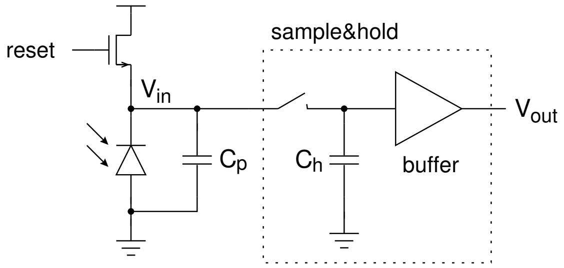


Figure 2.9: Basic circuit of an integration based photoreceptor.

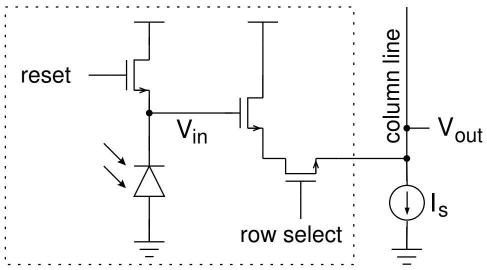


Figure 2.10: APS photoreceptor circuit with source follower as output buffer.

The charge integration method provides several advantages. It shows a linear transfer characteristic and a controllable sensitivity range by changing the integration time. Additionally, the fixed pattern noise (at least up to the sample-and-hold stage or the buffer) is low because the output signal depends on the input capacitance which has less mismatch than other device parameters. Another important advantage is the principal low-pass filter behaviour of the integration concept. The signal noise is reduced since high frequency components are removed. However, although the sensitivity range can be easily shifted by changing the integration time, the dynamic range in one frame is limited to about three decades. This property results from the fact, that the integration time is the

[8] charge coupled devices

same for all pixels and can not be locally adapted. In order to achieve higher dynamic ranges recent progress in the design of smart sensors allows to control the integration time of individual pixels at the expense of some area [LUL99]. Another disadvantage of the integrating sensor concept is the limitation concerning random pixel access. After the readout of one pixel the next readout can not be carried out until the integration time has passed.

Figure 2.11 shows an improved integration based photoreceptor with a dynamic range increased by nearly 30 dB [DEC98]. At the beginning of the integration interval the circuit is reset by pulling the potential $b(t)$ high. Then $b(t)$ is abruptly lowered by a small amount. Charge begins to accumulate on the capacitor C_d at a rate proportional to the illumination. Over the integration period, $b(t)$ continuously decreases as an exponential-like function of time with increasing slope. First, when the slope of $b(t)$ is relatively low, the amount of charge that can be integrated is limited to a certain value. High illumination produces too much charge which flows through the transistor M_b into V_{dd}. Later on, when the slope of $b(t)$ gets high enough, also high illumination charges can be integrated. Consequently the integration time for high level signals is shorter than that for low level signals. The dynamic range is extended and the response curve is compressed in a non-linear way.

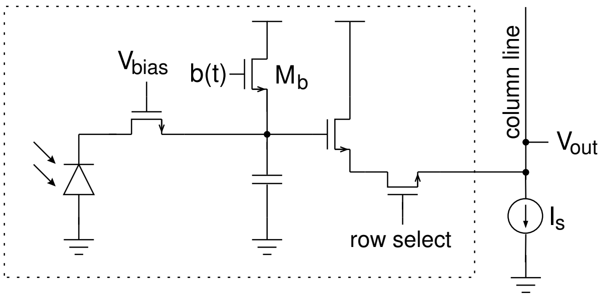


Figure 2.11: Example of an integration based photoreceptor with increased dynamic range.

2.3.2 Offset correction for integration based photoreceptors

Fixed pattern noise is one of the main disadvantages of CMOS imagers in comparison with CCD imagers. In a CCD imager charge is transferred between neighbouring CCD elements with a high charge transfer efficiency. The amount of the charge collected by a CCD pixel does also not heavily depend on the parameters of the device. However, in CMOS imagers the charge at a pixel passes through CMOS circuits which in addition to adding some systematic nonlinearity possess a high mismatch.

A technique commonly used for correcting the resulting fixed pattern noise is the correlated double sampling (CDS) method [DIE97]. Two samples of the pixel signal are taken during the readout cycle. One when the pixel is still in the reset state, and one when the charge integration has been completed. The two values are then subtracted or used as differential signals in further stages. The principal CDS circuit is shown is figure 2.12. It consists of two sample-and-hold stages which can be selected for storing the reset and the signal value, respectively. There is one such circuit for every column.

Mismatch in the CDS circuits introduces a new component contributing to the fixed pattern noise. These column-to-column variations can be reduced by applying a similar concept to the column CDS circuits. Due to the differential signals, this method is called delta double sampling (DDS). It is often directly implemented in the output buffer pad. The described CDS circuit can only be completely effective, if the fixed pattern noise is intensity independent, the circuits (e.g. the source follower stage in each pixel) are linear and the mismatch merely consists of an offset component. In reality, these assumptions are only valid in first approximation. Hence, more elaborate correction methods, which

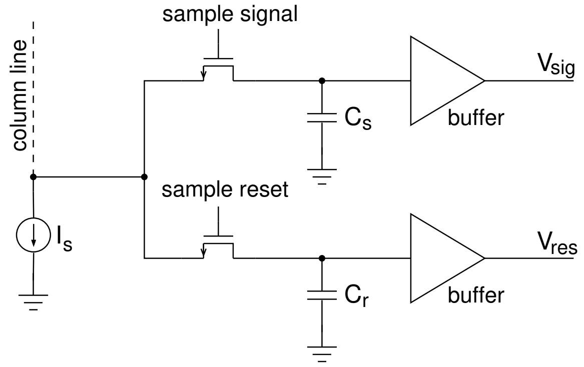


Figure 2.12: Schematic diagram of the correlated double sampling circuit.

can compensate for gain mismatch and nonlinearity in the circuits, are required. Today's CDS circuits achieve a remaining fixed pattern noise of 0.3 % (peak-peak) of the full scale signal [SMI98].

2.3.3 Continuously working photoreceptors

In contrast to integration based photoreceptors, continuously working receptors directly transform the photocurrent into a corresponding voltage. The output signal always represents the actual illumination as long as the circuit bandwidth is higher than the input frequency of the light stimulus. A simple continuously working sensor is shown in figure 2.13. It mainly consists of the photodiode and the transistor M_1 working in the subthreshold region (cf. test structures in 2.2.1). In order to drive the readout column line a buffer realized as a source follower is usually implemented (M_2). The pixel output can be selected by enabling the switch transistor M_3.

Due to the exponential current-voltage characteristic in weak inversion, the output voltage V_{out} logarithmically depends on the photocurrent I_{ph}. Since the drain current of weak inversion transistors can cover many orders of magnitude without leaving the exponential region, dynamic ranges of more than 6 decades can easily be achieved. However, the circuit becomes significantly slow at low intensities, because the photocurrent has to charge the capacitive load at the input of the photodetector. If the transistors M_1 and M_2 are small, the major contribution to this capacitance results from the photodiode.

A common solution to overcome the capacitive load problem is shown in figure 2.14. A high gain inverting amplifier, whose input is connected to the normal sensor output (now V_{in}), controls the gate voltage of the subthreshold transistor M_1. When V_{in} slightly increases due to a lower photocurrent, this voltage change is amplified by $-A$ and leads to a lower gate voltage at M_1. Since V_{GS} keeps constant, also V_{in} has to decrease according to the reduced gate voltage. Therefore the initial rise of V_{in} is reduced to a large extent due to the feedback amplifier. The same behaviour in opposite direction is valid for a decreasing input voltage. Consequently the input node V_{in} shows more or less the same potential at any illumination. The parasitic capacitance of the photodiode no longer slows down the frequency response of the circuit. Usually, an additional buffer for driving the column line is not required due to the already existing amplifier.

Unfortunately the contrast sensitivity of the standard logarithmic receptor is low due to the logarithmic compression. A biologically motivated solution which imitates the behaviour of the cones in the retina is presented in figure 2.15 [DEL94]. It shows the normal logarithmic behaviour for steady state (or long term) intensity variations while having a high gain for transient (or short term) variations. After an abrupt change in the incident intensity the circuit responds with its high transient

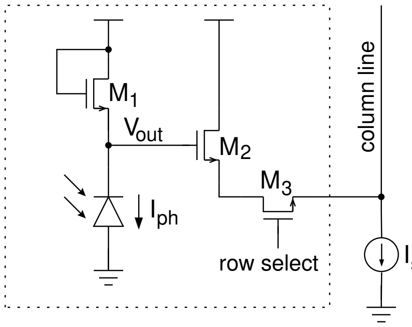


Figure 2.13: Circuit diagram of a continuously working photoreceptor with logarithmic response. The output line is driven by a source follower.

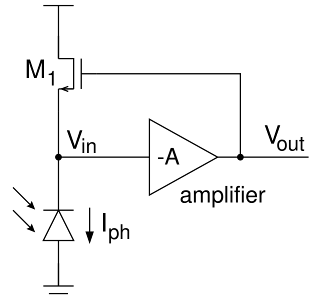


Figure 2.14: Logarithmic photoreceptor with feedback amplifier to enhance the frequency response.

gain and subsequently adapts to the steady state response within several seconds. Thus it is called an *adaptive* photoreceptor.

The adaptive circuit is principally based on the photocircuit with feedback amplifier already presented in figure 2.14. However, in the feedback loop from the output of the amplifier consisting of M_2 and M_3 to the gate of M_1, an adaptive element and a capacitive voltage divider have been introduced. Assuming that the adaptive element is just an extremely large resistor, the circuit at low frequencies operates similar to the photoreceptor with normal feedback amplifier in figure 2.14. At higher frequencies the gain of the circuit is boosted by the capacitive division of C_1 and C_2. The time constant for the adaptation process after an intensity change is determined by the adaptive element and the capacitor C_1 on which the actual adaptation state is stored. Very high ohmic adaptive elements for long adaptation times are achieved by using special transistor circuits operating in the deep subthreshold region.

The measured response curves are shown in figure 2.16. The steady-state response is obtained by stimulating the receptor with a definite intensity and measuring the output voltage after 5 minutes of adaptation. Providing an abrupt intensity change and measuring the resulting peak voltage gives the transient response. Due to the larger gain of short term variations a much higher contrast sensitivity for changing intensities is obtained. Therefore, this photoreceptor is well suited for motion detection vision chips. Moving objects cause abrupt intensity changes and can be detected with the transient receptor response.

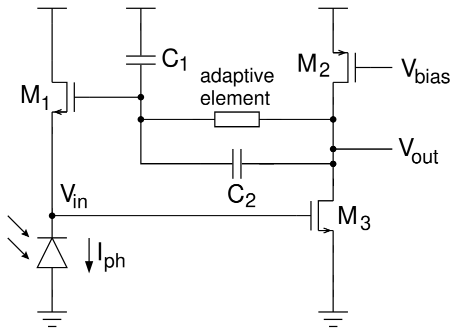


Figure 2.15: Circuit diagram of the adaptive photoreceptor.

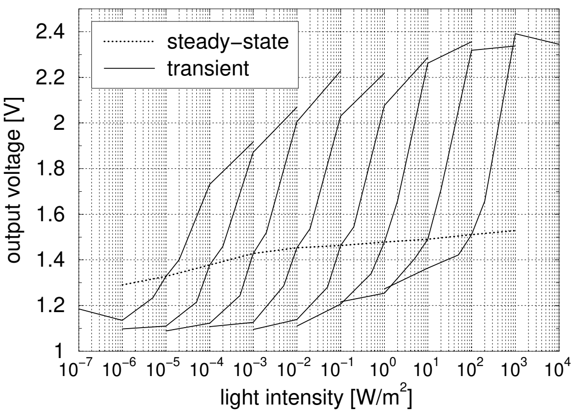


Figure 2.16: Steady-state and transient response of the adaptive photoreceptor [LOO96-1].

2.3.4 Fixed pattern noise correction in logarithmic image sensors

As measured in section 2.2.2, logarithmic photodetectors show an extremely high fixed pattern noise due to the weak inversion mismatch. The large offset variations resulting in peak-peak values, which correspond to 3 decades of light intensity, are also confirmed in [RIC95]. Unfortunately, it turns out that any effective kind of offset correction on the chip is much more complicated than in the case of integration based image sensors. The reason is the missing reset state of all continuously working receptors. There is no defined reference state whose corresponding pixel signal could be subtracted from the intensity-dependent output signal. Thus, other calibration concepts have to be applied.

The most common way of correcting the non-uniformities of logarithmic image sensors is to carry out a digital correction method. Initially, the pixel errors are measured by illuminating the sensor array homogeneously and stored in a digital memory. During readout operation, the actual pixel signals are converted into digital values and then digitally corrected according to the stored pixel errors. A one point (only offset), two point (offset and slope) or even higher order calibration algorithm can be utilised. The digital fixed pattern noise correction is usually carried out outside the chip although there is no principal problem to directly perform it on the sensor itself. However, an on-chip solution would require a large area for digital memory and additional control logic leading to larger chips and worse yield. Therefore, in case of a digital correction, the off-chip method is preferred. An example of a logarithmic camera with off-chip fixed pattern noise correction is given in [IMS97].

The digital solution, however, has some disadvantages. It consumes much power, usually disregards aging or temperature effects and needs the analog-to-digital conversion even if an analog signal is finally required. These drawbacks could be overcome by implementing an analog calibration method directly on chip, similar to the concept for integration based sensors. However, it is difficult to bring the pixel into the required reference state.

A possibility that has been recently proposed in [KAV99] realizes the calibration by stimulating the receptor with a very high current in addition to the photocurrent. In this case, the pixel output is nearly independent of the actual illumination, as the varying photocurrent only amounts to a small fraction of the total current. Then, the receptor output corresponding to this reference state can be subtracted from the output signal corresponding to the actual illumination by using the correlated double sampling method (cf. section 2.3.2). This calibration concept leads to a small photoreceptor size because only one additional transistor per pixel is required. However, the remaining fixed pattern noise is relatively high. This non-uniformity mainly results from the slope variations. Since the calibration current is much higher than the photocurrent, the calibration point is far away from the operating point. Besides, the readout frequency is limited, because after calibration the pixel potential needs some time to reach its original level again.

The image sensor developed within the scope of this work also includes an analog offset correction method. The applied concept, which is mainly based on the self-calibrating photoreceptor presented in the next chapter, differs from the one described in the previous paragraph. It uses very low calibration currents of the same magnitude as the photocurrents. Therefore, slope variations only have a subordinate impact on the fixed pattern noise, and the remaining offset variations are further reduced.

Chapter 3

Self-Calibrating Photoreceptor

In order to overcome the fixed pattern noise problem of logarithmic photoreceptors, a self-calibrating pixel concept is presented. At first, the corresponding pixel circuit and its functionality are described. Possible timing and stability problems arising from the implemented feedback loop are discussed. Subsequently, improvements and alternatives as well as complementing structures required for the use in a sensor array are explained. These circuit extensions include the auto-exposure mechanism, averaging of adjacent pixels, reducing of charge injection variations and a concept to compensate for the calibration amplifier offsets. Finally, different layouts of the realized photoreceptor circuits and measured results of the implementation using mirrored pixels are shown.

As shown in the last chapter, the high dynamic range required for the vision substitution system TVSS (cf. introduction) can be achieved by using photoreceptors with logarithmic response. In addition, these logarithmic receptors provide further advantages. Firstly, contrasts, in linear systems represented by intensity ratios, are converted into signal differences. This means a simplification for the subsequent image processing stage, as it is easier to calculate with sums than with products. Secondly, due to the continuous photodetector concept, a real random pixel access can be implemented. It is possible to read out any pixel at any time without taking care of fixed integration times.

However, the dominant problem of fixed pattern noise has to be solved before the usage of logarithmic sensors becomes feasible. Since further image processing is carried out in an analog manner (edge detection with an analog switched capacitor network), the method including analog-to-digital conversion, digital correction and digital-to-analog conversion should be avoided. Therefore, an analog self-calibrating photoreceptor has been developed that reduces the non-uniformities to an uncritical level directly on the chip. The according pixel circuit and its functionality are presented in this chapter. A summary of the self-calibrating image sensor including circuit description and measurement results can be found in [LOO98] and [LOO99].

3.1 Calibration concept

The signal to fixed pattern noise ratio in a sensor system can be improved by either increasing the sensor signal or decreasing the pixel variations. Both possibilities have been implemented. Before explaining the self-calibration to reduce the fixed pattern noise, the enhancement of the logarithmic signal slope with the help of one additional transistor is described.

3.1.1 Enhancement of the logarithmic response

The principal photoreceptor with logarithmic response shown in part a) of figure 3.1 consists of the photodiode and the MOS-transistor M_1 working in weak inversion. The slope of the logarithmic voltage (i.e. voltage change per current decade), which is also called the gain of the circuit, is determined by the subthreshold slope factor n. Since the source node of M_1 is not fixed, the bulk effect gives an additional term compared to the current-voltage relation in equation 2.7. For the sake of clarity, the bulk node of transistor M_1 is also drawn and connected to ground. A common model which is derived in [ALL87-1] leads to the following relationship between the drain current I_D, the gate-source-voltage V_{GS} and the source-bulk-voltage V_{SB}:

$$I_D = I_{DO}\frac{W}{L}e^{\frac{V_{GS}}{nV_t}}\,e^{\frac{V_{SB}}{V_t}\left(\frac{1}{n}-1\right)} \tag{3.1}$$

The current I_{D0} already includes the constant term corresponding to the threshold voltage V_T to simplify the equation. For a given V_{GS}, the voltage V_{SB} influences the drain current in a way that a higher V_{SB} leads to a lower I_D as the term $(\frac{1}{n}-1)$ is negative. Solving for V_{GS} to obtain the logarithmic voltage-current law yields

$$V_{GS} = nV_t \ln\frac{I_D}{I_{D0}\frac{W}{L}} + V_{SB}(n-1). \tag{3.2}$$

This equation can be used to express the behaviour of the receptor output V_{out} in terms of the photocurrent I_{ph} which is equal to the drain current I_D. Regarding the circuit in part a) of figure 3.1 and using $V_{out} = V_b - V_{GS}$ and $V_{SB} = V_{out}$ gives

$$V_{out} = V_b - V_{GS} = V_b - nV_t \ln\frac{I_{ph}}{I_{D0}\frac{W}{L}} - V_{out}(n-1) \tag{3.3}$$

where V_b is a constant bias voltage. Solving this equation for V_{out} results in

$$V_{out} = \frac{V_b}{n} - V_t \ln\frac{I_{ph}}{I_{D0}\frac{W}{L}}. \tag{3.4}$$

Compared to the considerations without bulk effect, the gain of the logarithmic compression is reduced from nV_t to V_t (cf. equation 2.10). This means a difference of about 20 %, because $n \simeq 1.2$. Besides, the offset voltage V_b is decreased by a factor of n. It should be noted, that the slope still shows a slight dependence on the factor n. The total independence obtained in equation 3.4 is a consequence of the applied model. The simulated behaviour of the receptor output as a function of the photocurrent is plotted in figure 3.2 (upper curve). The logarithmic decrease in the subthreshold region as well as the transition to the square root function in strong inversion can be seen. The channel dimensions of the simulated transistors are $W = 3\,\mu$m and $L = 1\,\mu$m.

In order to increase the slope factor, an additional transistor M_2 has been inserted in the current path. Part b) of figure 3.1 shows the corresponding circuit diagram. Since the photocurrent has to flow through two weak inversion transistors, it produces the voltage drop V_{GS} twice. Therefore, a doubling of the subthreshold slope can be expected. However, due to the different source-bulk-voltage of M_1 and M_2, the bulk effect leads to a gain which is not exactly twice the gain of the one transistor solution.

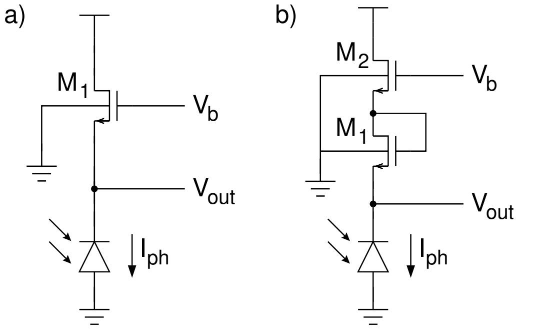


Figure 3.1: Circuit diagram of a logarithmic photoreceptor with one or two subthreshold transistors.

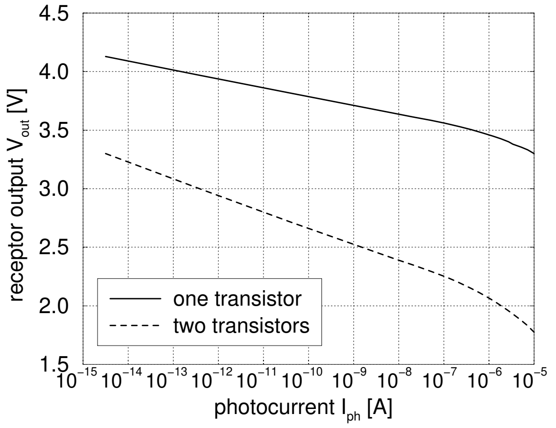


Figure 3.2: Logarithmic response of photoreceptors with one or two subthreshold transistor.

The receptor output can be calculated by determining the gate-source-voltages V_{GS1} and V_{GS2} according to equation 3.2. The corresponding source-bulk-voltages which have to be substituted into the V_{GS} relation can also be expressed in terms of the photocurrent I_{ph} and the output voltage V_{out}. The circuit is described by the following equations:

$$V_{out} = V_b - V_{GS1} - V_{GS2} \tag{3.5}$$

$$V_{GS1} = nV_t \ln \frac{I_D}{I_{D0}\frac{W}{L}} + V_{SB1}(n-1) \tag{3.6}$$

$$V_{GS2} = nV_t \ln \frac{I_D}{I_{D0}\frac{W}{L}} + V_{SB2}(n-1) \tag{3.7}$$

$$V_{SB1} = V_{out} \tag{3.8}$$

$$V_{SB2} = V_{out} + V_{GS1} \tag{3.9}$$

Substituting these equations into each other and solving for V_{out} yields

$$V_{out} = \frac{V_b}{n^2} - \left(1 + \frac{1}{n}\right) V_t \ln \frac{I_{ph}}{I_{D0}\frac{W}{L}}. \tag{3.10}$$

Comparing this relation to the photoreceptor with one transistor (equation 3.4) shows, that the logarithmic gain is increased by a factor of $(1+\frac{1}{n})$. This is somewhat less than 2. In case that $n=1.2$, the gain enhancement amounts to a factor of 1.83. Besides, the offset voltage given by the bias voltage V_b is divided by n^2 which means a further decrease compared to the receptor with one transistor. The lower curve in figure 3.2 shows the simulated output signal behaviour as a function of the photocurrent. The increased slope as well as the lower offset is apparent. The simulations were carried out with a bias voltage of $V_b = 5\,\mathrm{V}$.

Replacing the NMOS transistor M_1 by a PMOS-FET, whose gate node is connected to V_{out} (drain and source are exchanged), would result in an even higher signal gain. The bulk is not connected to ground but to V_{dd}, which means that the bulk effect now works in the opposite direction and enhances the logarithmic slope. Unfortunately, it is very space-consuming to integrate small NMOS and PMOS transistors near to each other, because the PMOS-FET is embedded in a n-well leading to large spacing between the two device types. Besides, PMOS devices show a worse matching behaviour (cf. section 2.1). For that reason, the pure NMOS solution has been preferred.

The slope factor could be further increased by using more than two transistors. However, this would lead to a deterioration of other circuit parameters. First of all, the parasitic capacitance at the output node has to be charged by the small photocurrent. A higher voltage swing as obtained by a higher gain thus leads to a reduced dynamic response of the circuit. Besides, the offset of the output voltage decreases by one V_{GS} per additional transistor. Particularly at higher photocurrents the receptor output could saturate by reaching the ground level. Finally, every additional transistor increases the pixel size which is an important factor concerning high resolution image sensors.

Therefore, using two transistors is an acceptable tradeoff between gain enhancement on the one hand and worse dynamic response as well as increased pixel size on the other hand. Since the threshold voltage variations of both transistors are statistically independent, the resulting offset distribution is given by the square root of the quadratically summed individual offset variations. This means, that the absolute fixed pattern noise is increased by $\sqrt{2}$, whereas the signal slope is increased by a factor of nearly 2. Hence, the signal to fixed pattern noise ratio is improved by about 30 % compared to the photoreceptor with one transistor.

3.1.2 Photoreceptor circuit

The other way to improve the signal to fixed pattern noise ratio is to reduce the transistor non-uniformities. Since the passive solution by using large transistor dimensions is not reasonable (large capacitances), an active solution by applying a self-calibration mechanism is used. Before describing the corresponding pixel circuit including additional devices compared to the standard logarithmic photoreceptor, the basic functionality of the calibration concept is explained.

To calibrate any sensor system, it is required to bring the system into a reference state that corresponds to a definite sensor input. In the case of continuously working photoreceptors, the circuit is usually stimulated by the photocurrent which is generated in the photodiode by the photoelectric effect. For calibration it is either necessary to set the light intensity for all pixels to a definite level or to stimulate the receptor circuit by a reference current instead of the photocurrent. Since the first possibility needs specific environmental conditions (uniform illumination of all pixels), this solution is unpractical (but not impossible, see [MAR98]), if the calibration should be carried out under the normal sensor operating conditions. Consequently, the second solution is used in the following concept.

During the calibration cycle all photoreceptors are stimulated by the same reference current. Without fixed pattern noise, all pixel outputs would show an identical signal. In reality, however, these signals differ from each other due to the device-to-device variations. A differential amplifier now compares the individual output voltages to a reference voltage and adjusts each pixel until both voltages are equal. Then, the calibrated pixel state is stored on an analog memory present in every photoreceptor. Because the differential amplifier is very space-consuming it is not included in the pixel itself, but is located at the border of the sensor array. One amplifier is responsible for all pixels of one array column and calibrates them sequentially.

The concrete CMOS implementation of the self-calibration concept is shown in figure 3.3. The pixel circuit consists of 8 transistors, one capacitor and the photodiode. For the sake of clarity the transistors selecting between different operation modes are drawn as switches. PMOS switches in contrast to NMOS switches are indicated with a circle. NMOS devices are switched on with a high signal level, whereas PMOS switches need a low signal level to be enabled. Devices located outside the pixel are plotted with dashed lines.

During the normal operation mode (image acquisition) the control line CALSLCT (calibration select) is set to low and the inverted line $\overline{\text{CALSLCT}}$ to high. This means that the switch S_2 is closed,

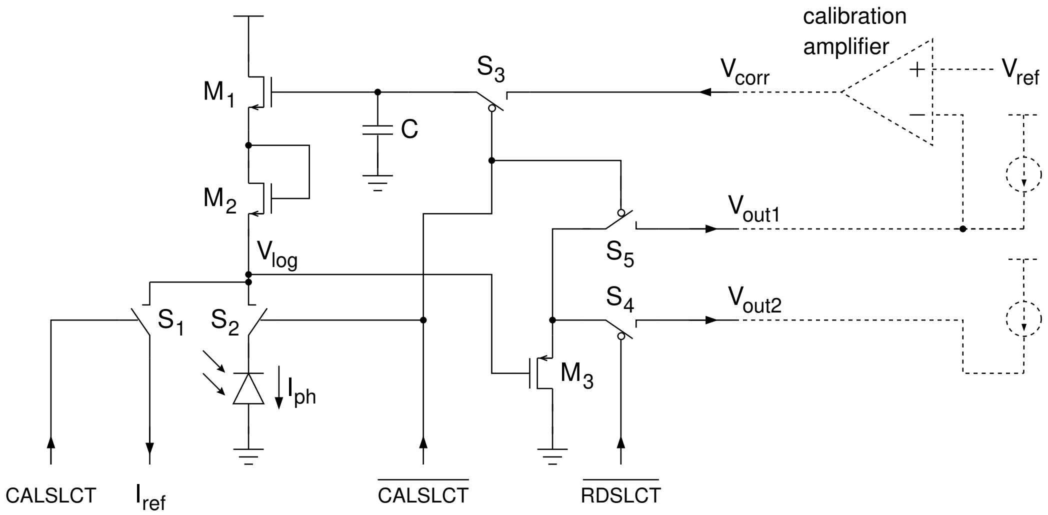


Figure 3.3: Circuit diagram of the self-calibrating photoreceptor.

whereas the switches S_1, S_3 and S_5 are open. The transistors M_1 and M_2, together with the photodiode representing the main part of the receptor, convert the photocurrent I_{ph} into the logarithmic voltage V_{log}. The reason for the use of two transistors in series has been explained in section 3.1.1. The main advantage in contrast to a single transistor consists in the nearly doubled signal slope. The sensor signal V_{log} is buffered by the transistor M_3 which operates as a source follower with a voltage gain of somewhat less than 1. That way, the circuit is able to drive large capacitive loads at the readout lines V_{out1} and V_{out2}. The current required for the operation of the buffer transistor is provided by a current source located outside the pixel. It can be shared with all pixels of one column as long as only one receptor is activated for readout at the same time. In order to select one pixel, the control signal $\overline{\text{RDSLCT}}$ (read select) switches on S_4 and connects the buffer transistor M_3 to the V_{out2} line. The logarithmic sensor signal V_{log} has a relatively low absolute level due to the two transistors M_1 and M_2 in series. Therefore, the readout buffer is realized with a PMOS transistor, because it is able, in contrast to an NMOS source follower, to operate at low input voltages.

When CALSLCT goes high and $\overline{\text{CALSLCT}}$ goes down, the switches S_1, S_3 and S_5 are closed and S_2 is open. The receptor circuit changes to calibration mode and is no longer stimulated by the photocurrent but by the reference current I_{ref}. The sensor signal V_{log} is guided to the V_{out1} line which is connected to the input of the calibrating operational amplifier. This amplifier compares V_{out1} to a voltage V_{ref} and generates the correction voltage V_{corr} which is the difference between the two input signals multiplied by the amplifier gain A. V_{corr} controls the gate node of transistor M_1. It corresponds to the bias voltage V_b in figure 3.1 and therefore influences the signal V_{log} due to equation 3.10. A change of V_{corr} directly shifts V_{log} in the same direction. Consequently, the receptor circuit in calibration mode represents a feedback loop consisting of the logarithmic sensor and the differential amplifier.

After calibration, CALSLCT goes low again and the pixel returns to normal operation mode. As S_3 is switched off, the correction voltage V_{corr} is stored on the capacitor C. The pixel offset is reduced by the gain factor A of the calibration amplifier. Hence, a high gain is required to obtain a low remaining fixed pattern noise. Since the amplifier is located outside the pixel, the number of transistors (= chip area) plays a subordinate role. For this reason, a differential amplifier with at least two stages providing a high gain should be used.

By applying this self-calibration concept, all mismatch sources are eliminated besides the photodiode itself. It is switched off and thus disregarded during the complete calibration process. However, due to the large dimensions and the relatively low sensitivity to process parameter variations, photodiodes show very small non-uniformities. They can be completely neglected compared to the mismatch of active devices. A very important contribution to the remaining fixed pattern noise results from the mismatch of switch S_3. When it is switched off, it generates a charge injection onto the capacitor C leading to a shifted correction potential V_{corr}. Variations in the amount of the injected charge produce variations of V_{corr} and therefore influence the receptor signal. A proper implementation of S_3 is essential to achieve a low fixed pattern noise.

3.1.3 Small signal behaviour

The equations describing the electrical behaviour of transistors mainly consist of non-linear functions. As a consequence, exact calculations of electrical circuits with more than one device are complicated or even not feasible at all. A common method to simplify the problem is the small signal analysis. Here, only small variations of current and voltage signals are regarded, whereas the circuit on a larger scale stays at a fixed operating point. Then, all functions can be approximated by linear relations and the resulting system of equations is easier to solve.

The properties of the logarithmic photoreceptor with photodiode and subthreshold transistors have already been described in section 3.1.1 using the exact weak inversion equations. However, only the static operation without caring for any timing behaviour has been regarded. To determine the dynamic response a small signal analysis of the receptor is carried out taking into account all important parasitic capacitances. For the following calculations the simplified circuit drawn in part a) of figure 3.4 is used. It mainly shows the same behaviour as the original one with two transistors in series, but leads to shorter equations. In order to analyse the timing behaviour, the gate-source-capacitance C_{gs} and the parasitic capacitance C_p taking into account the capacitances of photodiode, switches and buffer transistor (cf. figure 3.3) are added to the diagram. Besides their capacitances, all influences of the switches and the buffer transistor are ignored.

The corresponding equivalent circuit is shown in part b) of figure 3.4. As the bias voltage V_b ($= V_{corr}$ in the self-calibrating circuit) is constant, the gate-source-voltage $V_{GS} = V_b - V_{out}$ of transistor M_1 can simply be expressed by $-v_{out}$. The voltage-controlled current source describing the transistor in the case of small signals is thus given by $-g_m v_{out}$, where g_m is the transconductance in weak inversion. The resistor R_{ds} represents the drain-source-resistance leading to a higher current for increasing drain-source-voltages. Because $R_{ds} \gg 1/g_m$, R_{ds} is neglected in the following considerations. The photocurrent i_{ph} is replaced by the input current i_{in} since the circuit behaviour will be examined as a function of the stimulating current.

Regarding the output node v_{out}, the sum of all contributing currents has to be zero. This can be written as

$$g_m v_{out} + sC_{gs} v_{out} + sC_p v_{out} + i_{in} = 0 \tag{3.11}$$

where s includes the frequency dependence of the capacitor currents according to the Laplace-transformation. The transfer characteristics given by the ratio of output signal to input signal results in

$$\frac{v_{out}}{i_{in}} = \frac{-1}{(C_{gs} + C_p)\left(s + \frac{g_m}{C_{gs}+C_p}\right)}. \tag{3.12}$$

Using the Laplace-transformation, the timing behaviour of the output signal can be calculated. Assuming an abrupt rise (or fall) of the input current, i_{in} can be expressed with the help of the Heaviside-

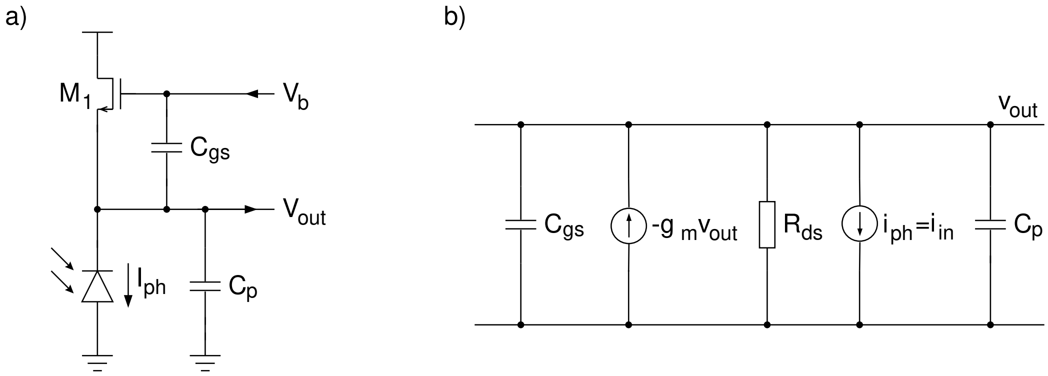


Figure 3.4: Simplified circuit diagram and corresponding small signal model of the logarithmic photoreceptor. Calibration and readout switches as well as the buffer transistor are neglected.

step-function $U(t)$[1]

$$i_{in}(t) = I_0 U(t) \tag{3.13}$$

Substituting the Laplace-transform of equation 3.13 into the transfer characteristics in equation 3.12 and transforming back into the time domain yields

$$v_{out}(t) = -\frac{I_0}{g_m}\left(1 - e^{-\frac{g_m}{C_{gs}+C_p}t}\right) = -\frac{I_0}{g_m}\left(1 - e^{-\frac{t}{\tau}}\right). \tag{3.14}$$

As shown, the voltage level corresponding to the increased input current is reached by an exponential decrease with the time constant $\tau = (C_{gs} + C_p)/g_m$. This time constant, however, is not fixed since g_m depends on the input current level. In the subthreshold region the current-voltage-law is given by equation 3.1. Using this relation and neglecting the bulk effect, g_m results in

$$g_m = \frac{\partial i_D}{\partial v_{GS}} = \frac{I_{in}}{nV_t} \tag{3.15}$$

which means, that $g_m \propto I_{in}$. Consequently, the dynamic response becomes slower at low currents and faster at high currents.

Typical values of the dynamic behaviour of a logarithmic receptor with a parasitic capacitance of $C_{gs} + C_p = 100$ fF and a subthreshold slope factor of $n = 1.2$ are presented in table 3.1. Here, the

intensity [W/m^2]	$I_{ph} = I_{in}$ [A]	g_m [1/Ω]	τ [s]
1000	2.4×10^{-8}	5.2×10^{-7}	1.9×10^{-7}
1	2.4×10^{-11}	5.2×10^{-10}	1.9×10^{-4}
0.001	2.4×10^{-14}	5.2×10^{-13}	1.9×10^{-1}

Table 3.1: Time constants describing the dynamic behaviour of the photoreceptor.

influence of the second transistor enhancing the slope in the receptor circuit (cf. figure 3.3) and the bulk effect are also taken into consideration by calculating g_m on the basis of equation 3.10

$$g_m = \frac{I_{in}}{\left(1 + \frac{1}{n}\right) V_t}. \tag{3.16}$$

[1]The Heaviside-function is defined by $U(t) = \begin{cases} 0 & : \quad t < 0 \\ 1 & : \quad t \geq 0 \end{cases}$.

It can be seen, that the circuit becomes significantly slow at photocurrents corresponding to light intensities below 100 mW/m^2. As one consequence fast movements in the image leading to fast changes of the pixel illumination can not be detected at very low intensities. The more important consequence, however, results from the fact, that the pixel circuit has to adapt in a short time to a completely new input current when it is switched from readout to calibration mode or vice versa. In order to calibrate the circuit in a fraction of a millisecond, reference currents of more than 100 pA lying in the upper half of the dynamic range of the receptor are required. After applying the self-calibration and switching back to normal operation mode at low intensities, the receptor voltage needs a relatively long time to reach its working level again. Therefore, the time between calibration and next readout cycle should be as long as possible.

It should be mentioned, that the small signal analysis only delivers results with respect to small changes in the signal levels. The difference between reference current (for calibration) and photocurrent (for readout), however, can reach several decades. For that reason, a more exact analysis of the circuit behaviour when switching between the two operation modes is necessary.

3.1.4 Large signal behaviour

To determine the photoreceptor behaviour in the case of large changes in the input current, the pixel again is reduced to the simplified model drawn in part a) of figure 3.4. In the following calculations, the capacitances C_{gs} and C_p are combined to the total capacitance $C_{tot} = C_{gs} + C_p$. Also the influence of the second transistor in series which is not shown in the simplified circuit is taken into account by using the voltage-current relation given in equation 3.10. Thereby the offset contribution V_b/n^2 is neglected and the ratio W/L is included in the current I_{D0}. Regarding the output node of the circuit, the sum of all contributing currents has to be zero

$$\underbrace{-I_{D0}\, e^{-\frac{V_{out}}{\tilde{n}V_t}}}_{\text{transistor current}} + \underbrace{C_{tot}\frac{\partial V_{out}}{\partial t}}_{\text{capacitor current}} + I_{in} = 0 \tag{3.17}$$

where $\tilde{n} = (1 + \frac{1}{n})$. This is a first order non-linear differential equation with respect to the variable V_{out}. The trivial solution, which describes the equilibrium state, is given by

$$V_{out}(t) = V_{out0} = \text{const.} \qquad \text{with} \qquad V_{out0} = \tilde{n}V_t \ln\frac{I_{D0}}{I_{in}}. \tag{3.18}$$

In the dynamic case, the differential equation is still exactly solvable. Assuming the initial condition $V_{out}(t = 0\,\text{s}) = V_0 = \text{const.}$, the following solution is obtained

$$V_{out}(t) = \tilde{n}V_t \ln\left[\frac{I_{D0}}{I_{in}}\left(e^{\frac{I_{in}}{\tilde{n}V_t C_{tot}}t} - 1\right) + e^{\frac{V_0}{\tilde{n}V_t}}\right] - \frac{I_{in}}{C_{tot}}t. \tag{3.19}$$

The behaviour of this solution significantly depends on the initial value of V_0. Two cases have to be distinguished: 1. $V_0 > V_{out0}$ and 2. $V_0 < V_{out0}$. In the first case, which corresponds to an abrupt increase of I_{in}, the voltage V_{out} shows a monotonous decrease which approaches more and more the equilibrium $V_{out} = V_{out0}$. It is plotted in figure 3.5 for 3 different input currents. The initial condition has been set to $V_0 = 0.3$V which corresponds to somewhat more than 2 decades in the input current due to the subthreshold slope factor of $n = 1.2$. The equilibrium voltage is $V_{out0} = 0$V and the capacitance $C_{tot} = 100$ fF. The second case of the solution in equation 3.19 includes a monotonous rise of V_{out} which also nears the equilibrium state $V_{out} = V_{out0}$. It corresponds to a sudden decrease of I_{in} and is shown in figure 3.6 with the same parameters used for the plot of the first case.

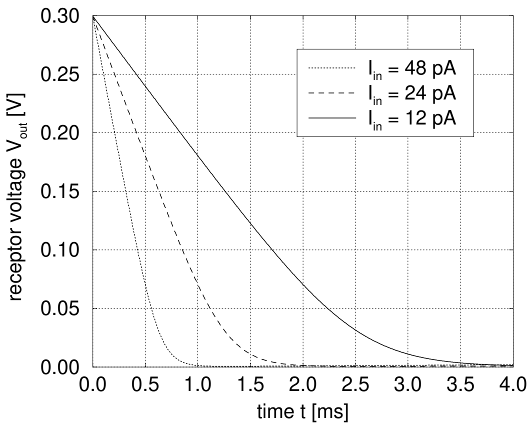


Figure 3.5: Circuit behaviour after an increase of the input current.

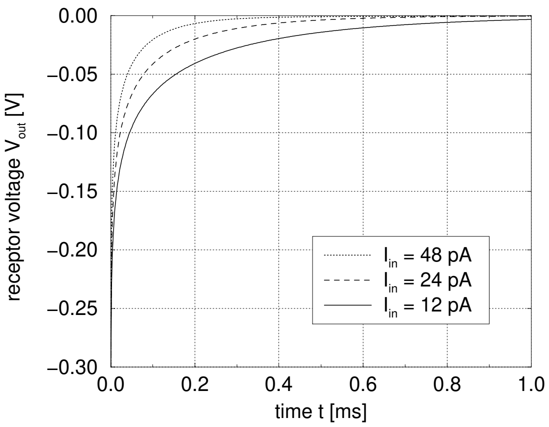


Figure 3.6: Circuit behaviour after a decrease of the input current.

The difference between the two solutions is not only given by the opposite sign of the slope, but also by a different quantitative behaviour. Regarding the decreasing curves of the first case in figure 3.5, it is apparent that down to about $V_{out} = 50$ mV a linear relation between time and voltage is valid. Below this limit, a more exponential-like behaviour occurs. These two different properties result from the two terms of equation 3.19. The second term gives the linear decrease which is dominant as long as the output voltage is far away from V_{out0}. The more V_{out} approaches V_{out0}, the more the behaviour of the first term becomes important. The linear term only depends on the current I_{in} and the capacitance C_{tot}. This means, that the complete current required to change the potential by discharging C_{tot} is given by I_{in}. This current is independant of the voltage difference $V_{out} - V_{out0}$. Therefore, C_{tot} is discharged at most with I_{in}, and it takes a relatively long time to reach the equilibrium level.

In the case that V_{out} starts at a value below V_{out0} (figure 3.6), no linear behaviour can be observed. Here the first term dominates especially at a large distance from V_{out0}. The consequence is a very fast rise at the beginning which slows down more and more when approaching the equilibrium level. This level is reached 3-4 times earlier than in the opposite case of figure 3.5 (different time scales in both diagrams!). Hence, if possible, only abrupt signal changes leading to an increasing output voltage should be initiated.

However, switching the photoreceptor from readout mode to calibration mode could cause an increase of the input current resulting in the slow decrease of the output voltage. In addition, the parasitic capacitance of the line, which delivers the reference current, has to be added to C_{tot} and leads to a further slowdown of the circuit. Since the self-calibration has to be carried out relatively fast compared to the recovery time between calibration and readout (where the pixel output goes back to its operation point), a long transition time can be critical.

In order to reduce this problem a mechanism to precharge the reference current line to a given voltage has been implemented. The operation principle is simple. Before switching to calibration mode, the reference current line is connected for a short time to a voltage which is a definite amount below the pixel voltage in calibration mode. Afterwards, when changing to calibration mode, the charge-sharing between the receptor capacitance C_{tot} and the higher line capacitance results in an averaged potential. This potential can be still lower than the pixel voltage during calibration, if the precharge voltage has been chosen low enough. Consequently, to reach the equilibrium state in the calibration mode, the pixel voltage has to increase in any case. This means a faster transition from readout to calibration mode, since the voltage increase occurs with the fast rise of figure 3.6.

3.1.5 Stability and timing considerations

Feedback stability

During the calibration cycle the photoreceptor and the calibration amplifier form a feedback loop. It is thus necessery to make a comment on the stability of the circuit. The question is: Is there any danger of getting oscillations that would destroy the calibration mechanism?

The photoreceptor can be treated as an additional stage of the differential amplifier. Hence, the stability arguments are the same as in the case of an individual, multi-stage operational amplifier. To obtain a stable behaviour, the phase margin has to be high enough, in the optimal case 90°. Since the amplifier already causes a phase shift of at least 90°, the pixel stage should introduce no further phase shift. This can be avoided by slowing down the first amplifier stage (frequency compensation) in a way that the subsequent photoreceptor is always fast enough to follow the amplifier output V_{corr}.

A phase shift of 90° always occurs at a pole of the transfer function. After crossing the first pole on the frequency axis, the open loop gain goes down with $1/\omega$ and the phase shift amounts to 90°. Crossing the next pole results in a higher decrease of the gain and in a phase shift of 180°. For a stable feedback, the second pole (and also the third, fourth etc.) has to be located at a frequency high enough for the open loop gain to be already below the closed loop gain. This can always be achieved by shifting the first pole introduced by the calibration amplifier towards lower frequencies which means a slowdown of the first stage.

The transfer characteristics of the pixel circuit is given by equation 3.12. Unfortunately, the pole located at $g_m/(C_{gs} + C_p)$ is not fixed but strongly dependent on the input current I_{in} because $g_m \propto I_{in}$ (cf. equation 3.16). Therefore, the frequency compensation of the calibration amplifier should be adjustable to adapt it to the actual conditions. A fast calibration can be achieved using a high reference current and a fast amplifier, whereas at low reference currents the calibration has to be carried out with slow amplifier settings.

Photodiode behaviour during calibration

When changing to calibration mode, the photodiode is completely separated from the current path through the two transistors M_1 and M_2. Nevertheless, incident photons are still converted into electron-hole pairs. The holes flow into the ground node whereas the electrons are collected in the photodiode. As a consequence, the diode's capacitance is charged up leading to a decreasing potential. When reaching the substrate level (ground), the charges are no longer bound to the diode but spread out into the substrate. This overflow results in a crosstalk between adjacent pixels, if it is not prevented by guard structures surrounding the photodiode. Besides, when switching back to readout mode the charged diode capacitance has to be discharged to get back to the actual operating level.

In order to keep the influence of these effects as small as possible, a slightly extended pixel circuit can be used. It is shown in figure 3.7. Compared to the normal self-calibrating photoreceptor in figure 3.3, the two transistors M_4 and M_5 and the switch S_6 have been added (grey area). In principle, they represent a second current path with the same behaviour as the main path consisting of the transistors M_1 and M_2. Now, the photodiode is no longer isolated during the calibration cycle but is connected to the additional current path. This means that the generated photocurrent can flow through M_4 and M_5. The photodiode stays at its normal operating level and is not charged. Consequently no overflow can occur and the diode potential keeps constant when switching back to readout mode.

However, the proposed implementation is not ideal. The major drawback consists in the additional space which is occupied by the extended pixel circuit. Besides, the mismatch of the transistors

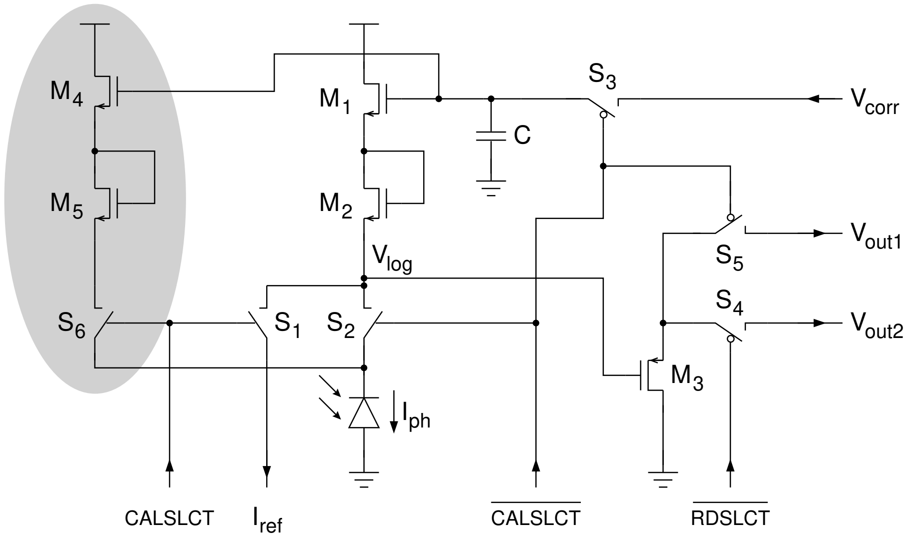


Figure 3.7: Photoreceptor circuit with additional devices to avoid charge accumulation in the photodiode during calibration.

M_4 and M_5 compared to M_1 and M_2 still leads to a different diode potential depending on the operation mode (calibration or readout). On the other hand, after a decrease of the potential due to charge accumulation in the isolated photodiode, it is recovered relatively fast due to the steep rise of the voltage in figure 3.6. Hence, keeping the diode potential constant plays a subordinate role.

The other argument concerns the crosstalk between neighbouring pixels due to a charge overflow in the photodiode. The bounding conditions required to obtain this overflow can be calculated using the typical diode capacitance of $C = 100$ fF. The saturation time, which the potential needs to reach the ground level, is given by

$$t_s = \frac{Q}{I_{ph}} = \frac{V_{out}C}{I_{ph}} \approx \frac{100\,\mathrm{fC}\cdot\mathrm{V}}{I_{ph}} \tag{3.20}$$

where the typical pixel voltage is set to $V_{out} = 1$ V. In the medium intensity range of 1 W/m^2 the photocurrent amounts to about 10 pA and the saturation time results in $t_s = 10$ ms. Since the calibration time is much shorter (about 100 μs), the photodiode does not overflow. Changing to higher intensities, however, significantly shortens the saturation time. At an intensity of 1 kW/m^2, t_s is reduced to 10 μs. In this case, a massive charge overflow occurs. Therefore, to avoid crosstalk at high illuminations, either the second current path shown in figure 3.7 or efficient guard structures have to be implemented.

During the development of the complete image sensor, both types of pixel circuits (with and without second current path) have been implemented. In the final version of the photoreceptor, the simple concept without the additional current path has been chosen. The advantage of the smaller pixel size is more important in the case of the high resolution image sensor than the suppression of crosstalk. Finally, measurements have shown, that crosstalk is not a big problem. It can be overcome by reading out pixels which are far away from the pixels currently calibrated.

3.2 Complementing structures

This section describes additional concepts and structures, that either have been integrated in the self-calibrating photoreceptor or significantly influence the performance of the calibration mechanism.

The first subsection includes an automatic exposure control that adapts the receptor output to the actual illumination. The second subsection deals with the reduction of the sensor resolution by averaging neighbouring pixels. That way, a coarse but fast impression of the complete scene is obtained. Then, the problem of charge injection variations is regarded which causes most of the remaining fixed pattern noise. Finally, an autozeroing concept for the calibration amplifier is presented which reduces the remaining column-to-column variations.

3.2.1 Auto-exposure control

During the calibration cycle the output signal of the photoreceptor is forced to be the same as the reference voltage V_{ref}. On the other hand, the applied reference current I_{ref} corresponds to a definite light intensity at which the generated photocurrent I_{ph} shows the same magnitude. Consequently, the pixel voltage also amounts to V_{ref} in readout mode, if the pixel is illuminated with the intensity corresponding to I_{ref}. In other words, for a given definite intensity the signal level of the pixel output can be shifted by changing the reference current.

This relationship between reference current and output voltage is demonstrated in figure 3.8. Here, a fixed illumination with a corresponding photocurrent I_{ph} and a fixed reference voltage V_{ref} are assumed. The figure is divided in three parts each containing the input current and the pixel voltage in calibration and readout mode. From left to right the reference current increases which can be seen in the lower diagrams. In part a) I_{ref} is far below I_{ph}. Part b) shows the situation that both currents are relatively close to each other. Finally, in part c) I_{ref} is much higher than I_{ph}. These currents are plotted on a logarithmic scale. The according output voltage is shown in the upper diagrams. In the calibration mode, it always equals the reference voltage V_{ref}. When switching to the readout mode it changes to the voltage V_{ph} that corresponds to the photocurrent I_{ph}. However, as can be seen in the three different parts, V_{ph} depends on the reference current I_{ref}. A higher I_{ref} results in a higher V_{ph} and vice versa. Accordingly, the general offset level of the output signal can be controlled by the magnitude of the reference current.

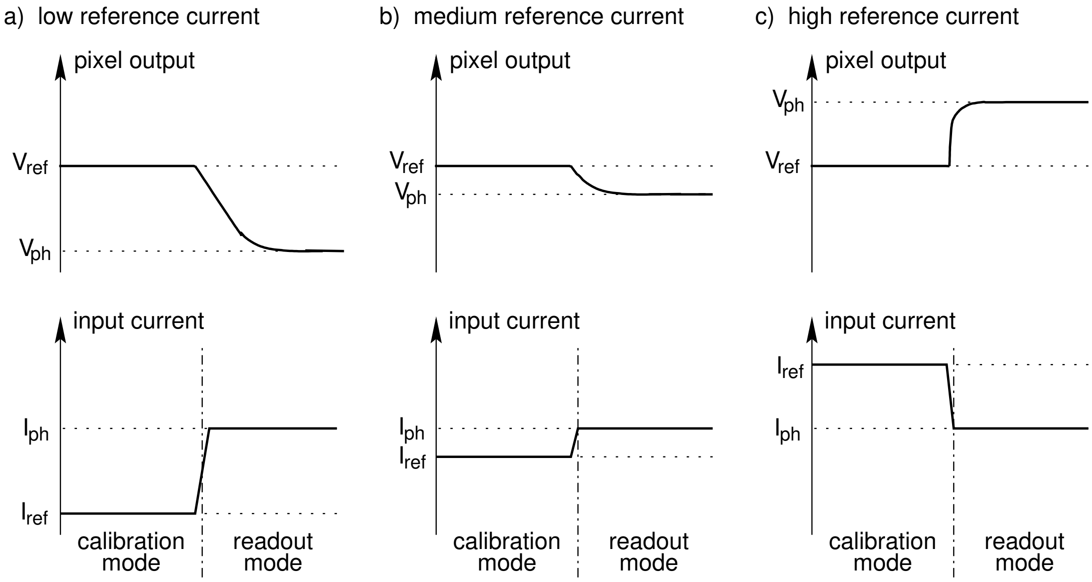


Figure 3.8: Qualitative behaviour of the pixel output voltage for 3 different reference currents. Illumination (i.e. photocurrent I_{ph}) and reference voltage V_{ref} are fixed.

This situation can be used to implement a mechanism whose effect resembles that of an automatic exposure control in an integration based sensor system. Here, the auto-exposure control usually determines the integration time depending on the actual illumination conditions. Shorter integration times result in a dynamic range shift towards high intensities, whereas longer integration times improve the sensitivity for low intensities. Regarding a constant illumination, the variation of the integration time leads to a corresponding variation of the output signal.

In case of the logarithmic sensor, there is no integration time as it is a continuously working circuit. Since it already has an intrinsic high dynamic range, it is not necessary to shift the sensitivity range according to the illumination. However, it is possible to control the offset of the output voltage depending on the actual light conditions by changing the reference current. Choosing the reference current proportional to the averaged illumination results in a constant mean output value (averaged over all pixels) independent of the illumination. Because this behaviour represents the same effect as in the case of integration-based sensors with automatic exposure, it is also called auto-exposure control.

An essential point of the auto-exposure concept is the generation of the reference current which has to be proportional to the averaged illumination. For that reason each pixel includes one additional small photodiode. The current of all these diodes is summed by connecting them together. Dividing this current by a fixed value to adjust the optimal global range and then using it as the reference current gives the required proportional behaviour.

Two major advantages can be gained from the auto-exposure control. At first, it represents a compensation method for the light flicker due to artificial illumination. Because every receptor shows a signal corresponding to the actual intensity, the signal varies with the 100 or 120 Hz frequency of the room light. At a typical frame rate of 50 Hz or less, some pixels are read out at high and some at low illumination leading to a stripe pattern in the picture. Applying the exposure control shifts the output voltage according to the illumination and thus compensates for the original signal variation.

The second advantage results from the fact that the exposure control forces the averaged output signal to stay in the middle of the output signal range. It is now possible to increase the contrast by mapping only the middle part of the signal range to the complete input range of the following system (ADC or video screen). The averaged output voltage will never leave this subrange. However, the dynamic range is reduced since intensities that are far away from the mean value can generate output signals outside the selected subrange. Therefore, a tradeoff between contrast and dynamic range has to be chosen.

3.2.2 Averaging of neighbouring pixels

Image processing algorithms can require many floating point operations per pixel. In the case of high resolutions ($>$ 100k pixels), even a very fast computer often fails to process the image data in real time and consumes much power. One method to reduce the number of calculations is to first regard the image with a decreased resolution. In the second step, only regions that seem to be interesting in the coarse image are processed in the higher resolution. Besides, in the tactile vision aid system the developed sensor will be connected to an integrated analog edge detection array which has a resolution of only 66×66 cells. To process a complete frame which normally has more than 100k pixels, a reduced image resolution is required. Hence, the possibility of a fast readout of the complete image in a reduced resolution should be implemented in the sensor.

A lower resolution is obtained by averaging adjacent pixels and reading out only the mean value. The desired averaging, which simply corresponds to a larger extended photodiode, is represented by averaging the photocurrents themselves. This can be achieved by electrically connecting the diodes.

However, this would require additional switches in the receptor circuit to decide, if two pixels are averaged or not. Another possibility is the averaging of the logarithmic output voltages which could be easily carried out at the end of one column. But, the result can significantly differ from the photocurrent averaging leading to a disproportional weighting of individual pixels.

The quantitative analysis of the different ways of averaging is described in appendix C. The results referring to linear averaging (photocurrent averaging), ideal logarithmic averaging (voltage averaging) and modified logarithmic averaging due to the source follower properties (simplified voltage averaging) of two pixels in each case are shown in figure 3.9. In addition, the signal of the non-averaged pixels stimulated by a fixed current (1. pixel: $I_{ph} = 100$ pA) and a varying current (2. pixel: $I_{ph} = 100$ fA ... 100 nA) are represented by the top and bottom curve. The output voltages are plotted as a function of the varying photocurrent of the second pixel on a logarithmic scale. A higher photocurrent results in a lower voltage due to the inverting behaviour of the logarithmic photoreceptor.

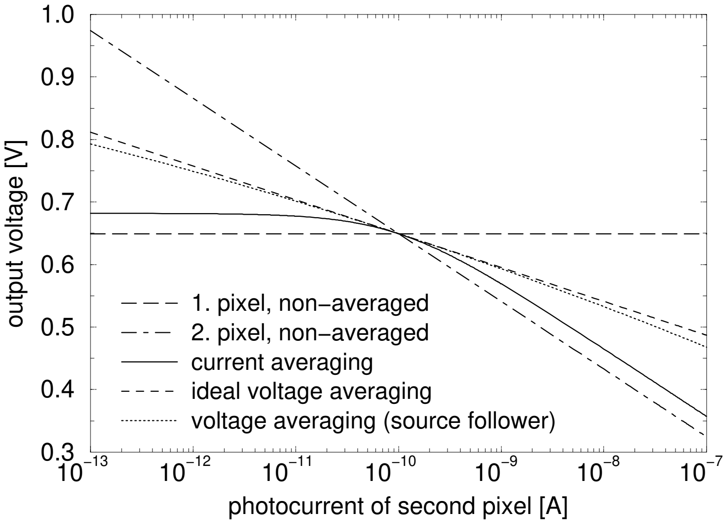


Figure 3.9: Averaging behaviour of two logarithmic pixels. The photocurrent of the first pixel is constant, the second one is given by the current on the abscissa. The averaged output voltage is shown in case of current averaging, ideal voltage averaging and simplified voltage averaging due to the readout amplifier (source follower).

In the case of current averaging, the pixel stimulated by the higher photocurrent dominates the behaviour of the averaged signal. The corresponding voltage always follows the signal of the receptor with the higher current. The reason is the small influence of a small current when added to a much higher current. The ideal voltage averaging gives a linear behaviour due to the logarithmic current scale. Particularly at large current differences between the two pixels (left and right border), the voltage averaging significantly differs from the current averaging. When averaging the voltages, smaller currents get more weight due to the logarithmic compression. Regarding the simplified averaging of the source follower voltages, only a small deviation from the ideal voltage averaging is obtained. The curve is somewhat shifted towards the current averaging curve.

Since the method of averaging the output voltages differs very much from the photocurrent averaging, carrying out the photocurrent averaging in the pixel is the preferred solution. The required switches are added to the receptor circuit shown in figure 3.10 (grey area). Assuming, that the pixels are arranged in rows and columns, the connections to the neighbouring photodiodes are indicated

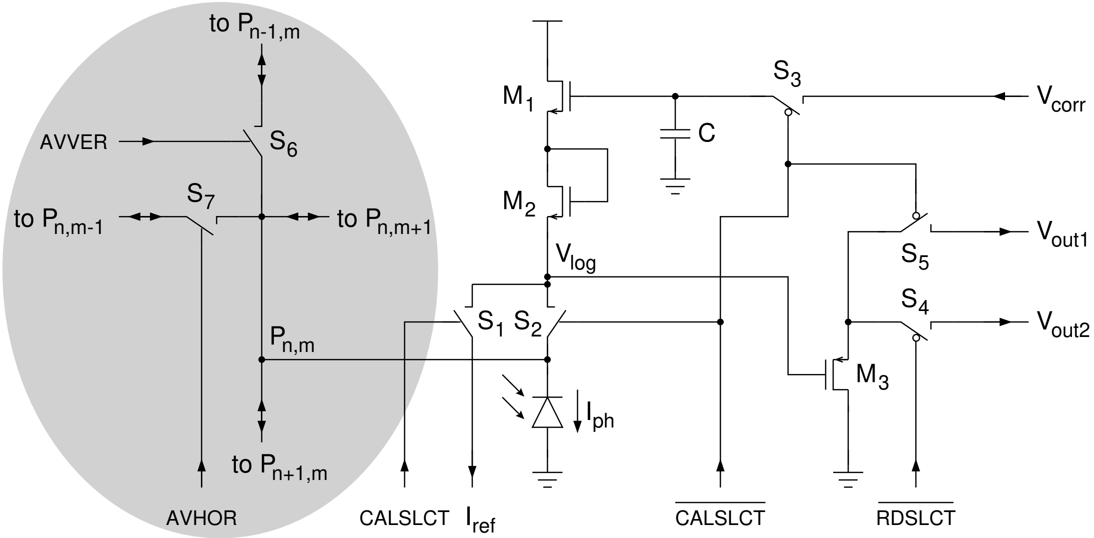


Figure 3.10: Photoreceptor circuit with additional switches to average the photocurrent of adjacent pixels.

with $P_{n,m}$, where n and m represent the corresponding row and column, respectively. The digital lines AVVER and AVHOR (AVeraging in VERtical or HORizontal direction) control the switches S_6 and S_7 which enable the averaging of the according photodiodes. This concept is very flexible as it allows averaging any number of pixels in horizontal and vertical direction. In the final image sensor, the possible averaging patterns have been restricted to a maximum of 8×8 pixel clusters due to the logic circuits controlling the AVVER and AVHOR lines.

3.2.3 Reduction of charge injection mismatch

Charge injection always occurs when using a MOS transistor for switching. It is caused by the parasitic capacitances between gate and channel and between gate and source or drain diffusion. These capacitances lead to a coupling of the digital control signal switching the transistor on or off to the analog signal line to be switched. If one node of this signal line is isolated after switching off the transistor, the injected charge is stored and shifts the voltage at that node. The voltage shift depends on the ratio of the switch capacitance to the isolated node capacitance: the higher the node capacitance and the smaller the switch capacitance, the smaller the influence of the injected charge.

In the case of the self-calibrating pixel (figure 3.3) the switch S_3 represents the critical device. When it is switched off, it injects charge onto the storage capacitor C. In this case the problem does not consist in the absolute amount of the injected charge. Due to the voltage shift at the input node of transistor M_1, the pixel output is just shifted by a definite global value. If, however, the charge injection varies from pixel to pixel, an additional contribution to the fixed pattern noise is introduced. The corresponding voltage shifts on the capacitor C lead to an individual pixel offset at the output node. Therefore, it is important to reduce the charge injection variations as much as possible.

In order to determine the magnitude of the voltage shift caused by charge injection, the circuit diagram of a NMOS-switch shown in figure 3.11 is regarded. C_{gs} is the gate-source-capacitance and C_{gc} the contributing gate-channel-capacitance which is half the total capacitance between channel and gate. If the transistor M_1 is switched on by pulling V_{sw} high, the storage capacitor C_{st} is charged to the input voltage V_{in}. When V_{sw} goes low again, M_1 is switched off and C_{st} stores the voltage V_{in}, however somewhat reduced by the charge injection through C_{gc} and C_{gs}.

Figure 3.12 shows the timing behaviour of the switch voltage V_{sw} (upper diagram) and the stored voltage V_{st} (lower diagram) when switching off M_1. As long as V_{sw} is higher than $V_{in} + V_T$ (V_T = threshold voltage), C_{gc} and C_{gs} both contribute to the charge injection leading to a fast decrease of V_{st}. When V_{sw} becomes lower than $V_{in} + V_T$ the gate-channel-capacitance C_{gc} nearly disappears since the transistor is almost switched off and charges can no longer flow through the channel. At this point, charge injection mainly occurs due to the gate-source overlap C_{gs} leading to a reduced decrease of V_{st}.

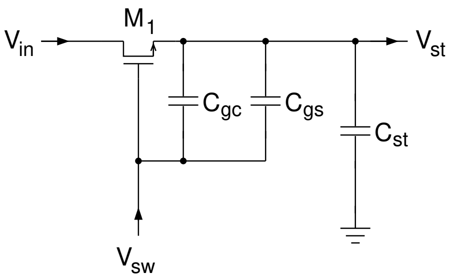


Figure 3.11: NMOS-switch with parasitic capacitances and additional storage capacitor.

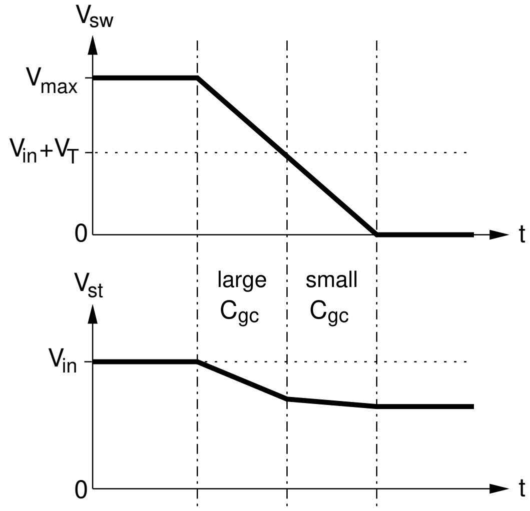


Figure 3.12: Behaviour of the stored voltage V_{st} during the switching-off process.

The voltage shift $V_{shift} = V_{in} - V_{st}$ is given by the amount of injected charge Q_{inj} divided by the capacitance C_{st}

$$V_{shift} = \frac{Q_{inj}}{C_{st}} = \frac{C_{gc}(V_{max} - V_{in} - V_T) + C_{gs}V_{max}}{C_{st}} \tag{3.21}$$

where V_{max} is the maximum level of V_{sw}. Regarding this equation two methods of reducing the absolute voltage shift are straight forward: Increasing the storage capacitance C_{st} and decreasing the voltage swing of the digital control line V_{max}. These methods would also reduce the absolute voltage shift variations from pixel to pixel caused by mismatch of the concerned capacitances because the relative variations with respect to the absolute shift are constant. However, both methods are limited: The first one by the required space, the second one by the fact, that a reduced maximum switch voltage V_{max} also reduces the range of the switched analog signal V_{in}. In order to keep the transistor M_1 conductive, V_{max} has to be higher than $V_{in} + V_T$. Thus, an acceptable tradeoff has to be realized.

Besides the device parameter mismatch there is another effect leading to shift voltage variations. It is given by the dependence of V_{shift} on the signal voltage V_{in} shown in equation 3.21. This means, that different voltages V_{in} result in different charge injections. In case of the self-calibrating photoreceptor V_{in} corresponds to the correction voltage V_{corr} which indeed differs from pixel to pixel. Therefore an additional transistor can be implemented in the receptor circuit to compensate for the dependence on the correction voltage. The corresponding diagram of the switch is shown in figure 3.13. The additional device M_2 is controlled by the inverse voltage $\overline{V_{sw}}$. The voltage shift is now given by

$$V_{shift} = \frac{(C_{gc} - C'_{gc})(V_{max} - V_{in} - V_T) + (C_{gs} - C'_{gsd})V_{max}}{C_{st}}. \tag{3.22}$$

A complete compensation of the charge injection (i.e. $V_{shift} = 0$) is achieved if

$$C_{gc} = C'_{gc} \qquad \text{and} \qquad C_{gs} = C'_{gsd} \tag{3.23}$$

but only the first condition is necessary to eliminate the dependence on V_{in}. C'_{gc} now means the total gate-channel-capacitance since source and drain are connected to the storage node. Accordingly, the capacitance C'_{gds} represents the gate-source- and the gate-drain-overlap. Hence, the size of transistor M_2 has to be half the size of M_1 to comply with equation 3.23. Figure 3.14 shows the behaviour of the voltage V_{sw} in case of total charge injection compensation.

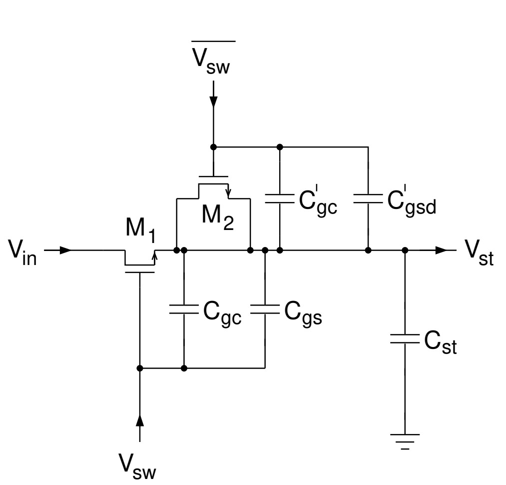


Figure 3.13: NMOS-switch with additional transistor to compensate the charge injection.

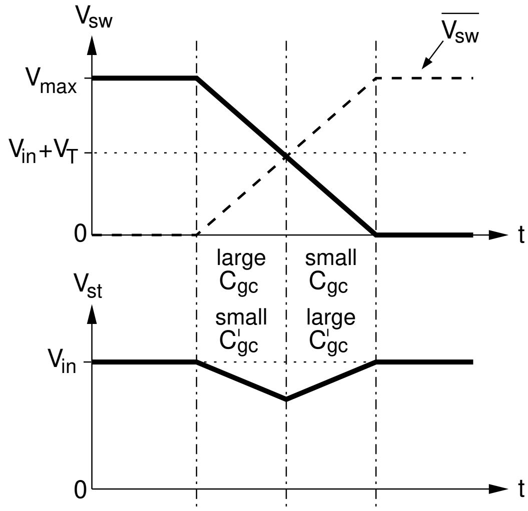


Figure 3.14: Behaviour of the stored voltage V_{st} during the switching-off process in the case of a compensation transistor.

3.2.4 Autozeroing calibration amplifier

In order to calibrate all pixels during the readout of one frame, the calibration of one complete pixel row has to be carried out at the same time. This means that as many calibration amplifiers as sensor columns are needed. Due to transistor mismatch in the input stage of the amplifiers, an offset voltage varying from column to column is obtained. To eliminate this offset variation, which would introduce additional column fixed pattern noise, an autozeroing concept has been implemented [GEI90-2].

The principal circuit is shown in figure 3.15. The inner triangle (solid lines) represents an ideal, offset-free amplifier. A realistic version indicated by the dashed triangle is obtained by adding the offset voltage source V_{off}. The autozeroing mode is enabled by closing the switches S_2 and S_3 and opening S_1. The amplifier output is fed back to the negative input forcing this node to show the same voltage as the positive input, namely $V_p + V_{off}$. The capacitor C_{off} connected to this negative input is charged to a voltage of $V_p + V_{off} - V_{cal}$. Switching to normal operation mode by opening S_2 and S_3 and closing S_1 stores this voltage on C_{off}. Hence, on the one hand the intrinsic offset voltage V_{off} is compensated. On the other hand any desired global offset can be added by controlling V_{cal} to adapt the input range of the amplifier to the signal V_n.

To ensure, that the switches S_2 and S_3 are completely off when S_1 is switched on, a non-overlapping clocking scheme is used for ϕ_1 and ϕ_2. It can be seen in figure 3.16. ϕ_1 has to be

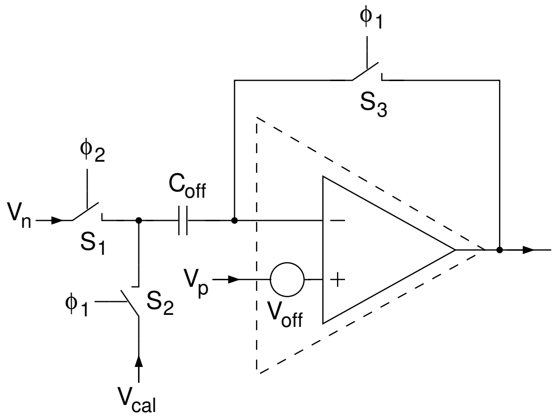


Figure 3.15: Circuit diagram of the autozeroing operational amplifier.

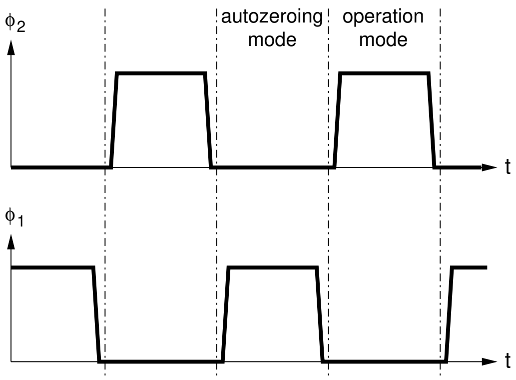


Figure 3.16: Non-overlapping two-phase clock.

totally down before ϕ_2 starts to rise and vice versa. Since all amplifiers can be switched to autozeroing mode at the same time, the non-overlapping clocks have to be generated only once. The concrete implementation of the autozeroing calibration amplifier as well as the non-overlapping clock generation are described in chapter 4 where the complete image sensor is presented.

3.3 Receptor layout implementation

The described concept of the self-calibrating photoreceptor has been implemented in three different layout versions using 0.8 μm and 0.6 μm CMOS processes. At first, the most space saving version is presented which, however, introduces a regular fixed pattern noise due to rotated and mirrored pixels. The other two layouts, which do not show this regular pattern and thus represent the preferred solution, are described subsequently.

3.3.1 Layout and performance using mirrored devices

Placing, designing and connecting CMOS devices like transistors or capacitors have to follow the so-called *design rules* which give definite limits for minimum structure spacings or minimum device dimensions (for details see [AMS95-1] and [AMS98-1]). Usually, equal devices can be placed closer to each other than different device types. Therefore, mirroring of the complete receptor layout which brings equal structures near to each other results in smaller pixels if the device dimensions remain constant.

Layout of the four-pixel-cluster

In order to implement the concept of mirrored pixels, a geometry leading to clusters of four pixels each has been chosen. It is realized in the AMS 0.6 μm process using two metal and one polysilicon layer. On the left side of figure 3.17 one cluster including four pixels is shown. The photodiodes occupy about one third of the pixel area and represent the dominant part. They are integrated as n^+-substrate-diodes, which show a high quantum efficiency and can be directly used as the drain node of the subsequent NMOS switch. The pixel pitch amounts to 24 μm resulting in a cluster size of 48×48 μm^2. The storage capacitors consist of NMOS transistors because no second polysilicon layer is available in the used process to build a more linear double poly capacitor. The transistor capacitance (150 fF) is slightly voltage-dependent which, however, only influences the storage time but not the stored voltage.

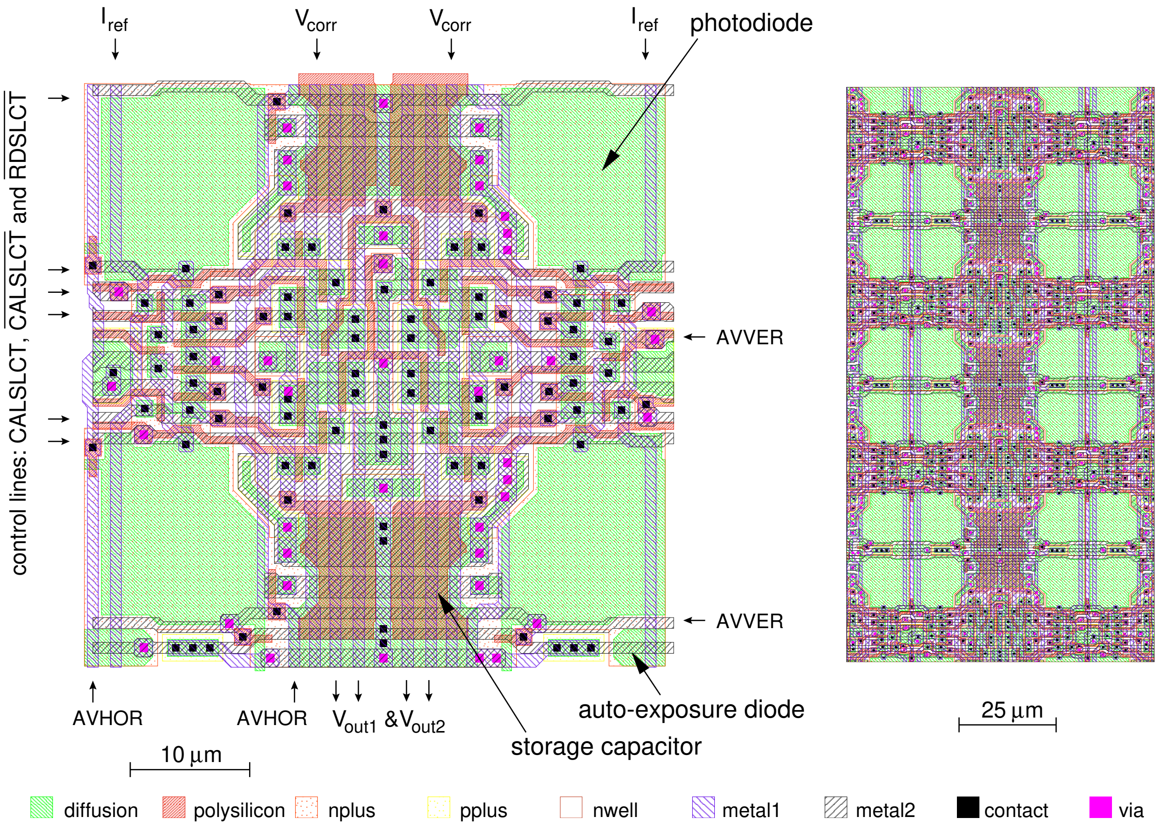


Figure 3.17: Layout of one pixel cluster consisting of 4 photoreceptors (on the left) and larger cutout of the complete sensor array (on the right).

The residual structures represent the transistors M_1 to M_3 (cf. pixel circuit in figure 3.3) and the switches for calibration, readout and averaging. The switches are realized by minimum size transistors ($W = 0.8\,\mu$m and $L = 0.6\,\mu$m) besides the readout selection switches having a larger width. The dimensions of the transistors M_1 and M_2 performing the logarithmic current to voltage conversion are $W = 2\,\mu$m and $L = 0.6\,\mu$m. The buffer transistor M_3 is still wider ($W = 3.3\,\mu$m) to get a higher transconductance g_m. In addition, a small photodiode can be seen at the bottom of the cluster generating the reference current for the auto-exposure control. All readout and control lines horizontally and vertically going through the complete sensor array are indicated by the corresponding signal names.

Using the four-pixel-clusters a complete chip including a sensor array of 96×72 pixels and a digital control part has been designed and manufactured. The right part of figure 3.17 shows a larger cutout of the sensor array. Due to the mirrored pixels a cloverleaf-like structure is obtained consisting of the photodiodes of four different clusters.

Measured performance

Mirrored or rotated devices show a large mismatch because the CMOS process parameters are direction-dependent due to the manufacturing process. The idea to mirror the pixels despite the higher intrinsic fixed pattern noise was, that the self-calibrating mechanism would compensate for the additional mismatch. Unfortunately, the measurement results differ from that theory. In order to examine the remaining non-uniformities of the individual pixels, the sensor array was uniformly illuminated at different intensities in a dynamic range of 6 decades.

Figure 3.18 shows the averaged output voltage as a function of the incident light intensity, separately drawn for the four different pixel types in one cluster. In contrast to the direct receptor output, the voltage rises with increasing intensity. This inverting behaviour results from the output amplifier driving the analog chip output line. It can be seen that the two upper pixels have more or less the same behaviour whereas the output voltage of the lower pixels differs from that. The lower right pixel shows a higher output signal and a smaller slope compared to the upper pixels. The curve of the lower left receptor is located in between. At low intensities the four corresponding output values are far away from each other. At higher intensities, the curves get closer to each other due to the different slopes.

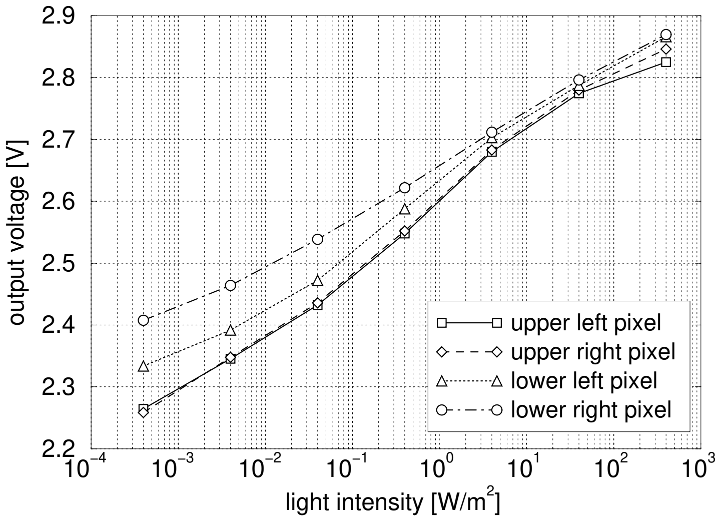


Figure 3.18: Output voltage of the four different pixels types as a function of the light intensity.

A sample image taken with the 96×72 sensor array and representing the offset distribution at an intensity of 0.4 W/m^2 (uniformly illuminated) is shown in figure 3.19. The regular fixed pattern caused by the different response curves of the four cluster pixels is apparent. If images taken at lower intensities are regarded this effect would be intensified due to the results in figure 3.18. Every second row as well as every second column differs from the previous one. In each cluster the lower right pixel generates the highest signal. The corresponding bright spots surrounded by the three darker pixels can be easily found in the image.

The pixel values of figure 3.19 are filled into a histogram and shown in figure 3.20. Again, the different mean values of the four pixel types can be seen. In addition, the variations within the individual offset distributions are represented by the width of the according peaks. The corresponding simulated and measured mean values as well as the measured standard deviations (rms) and averaged slopes are summarized in table 3.2. The simulated results were obtained by carrying out a parasitic simulation of a 3×3 cluster array. All capacitive couplings between the devices and the routing lines were taken into consideration. The stimulating current was adjusted to a value leading to almost the same mean value as the measured mean value of the upper two pixel types. Since the digital control lines are differently placed in the upper and lower pixel types, a different parasitic coupling occurs.

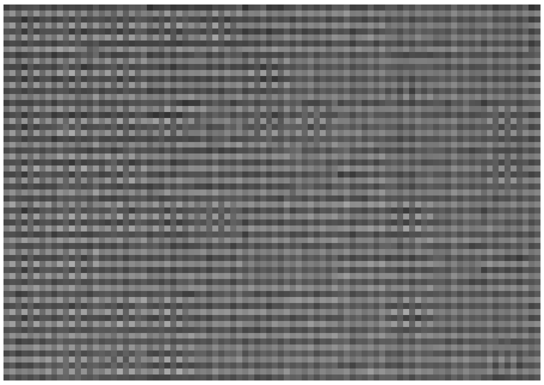


Figure 3.19: Image of the uniformly illuminated sensor array at an intensity of 0.4 W/m^2.

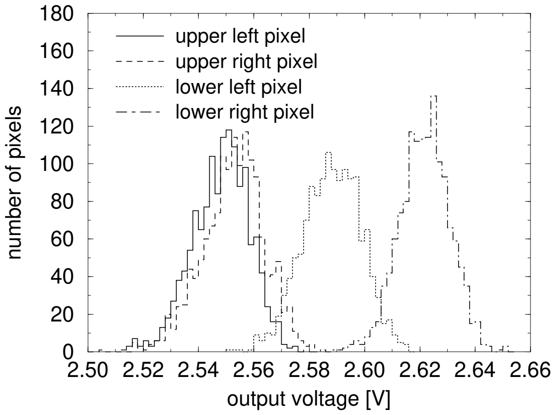


Figure 3.20: Histogram of the four different pixel types at an intensity of 0.4 W/m^2.

As a result, the simulated values of upper and lower pixel types vary from each other by about 30 mV. This is a good confirmation of the measured value for the difference between the upper pixels and the lower left pixel. However, the additional offset of the lower right pixel can not be explained by the simulation. It is a result of the different pixel slopes. As the slope behaviour is not influenced by parasitic capacitances, the slope variations can not be simulated.

Taking into account that the reference current used for the self-calibration corresponds to a high intensity ($\approx$ 100 W/m^2), the low difference between output voltages of the individual pixel types at high illumination becomes clear. The self-calibration compensates for the different offsets. Since the pixel slopes are not influenced by the calibration mechanism, they can not be corrected. Therefore, they lead to the observed different offset values at low intensities.

pixel type	simulated mean [V]	measured mean [V]	measured rms [mV]	measured slope [mV/decade]
upper left	2.550	2.548	10.3	102
upper right	2.550	2.553	11.1	104
lower left	2.581	2.588	10.4	91
lower right	2.581	2.622	9.2	78

Table 3.2: Simulated and measured results of the four different pixel types.

The measurement results have shown, that mirroring devices or complete pixels can lead to different slopes of the response curve. This behaviour cannot be compensated by the implemented self-calibration. Consequently, as the slope variations contribute to the total fixed pattern noise, the self-calibration is not able to sufficiently correct the mismatch error in case of using mirrored or rotated devices. The advantage of getting smaller pixels comes along with the severe disadvantage of a higher fixed pattern noise. The main contribution leading to the chessboard pattern seen in 3.19 is no longer statistically distributed but correlated to the individual pixel types. Therefore the sensor is unsuitable for most applications and a different pixel layout without mirrored devices has to be used. Two possible implementations are presented in the next section.

3.3.2 Pixel layout without mirrored devices

Apart from the layout described in the last section, the photoreceptor circuit has been implemented in two other versions without using mirrored or rotated devices. The first version is realized in a 0.8 μm CMOS process whereas the second one uses the smaller 0.6 μm CMOS process. On the basis of these pixel types complete camera chips with different resolutions have been built.

Layout in the 0.8 μm CMOS process

The photoreceptor version realized in the AMS 0.8 μm CMOS process includes the extended concept shown in figure 3.7. Accordingly, two additional transistors make sure that the photocurrent does not accumulate in the photodiode but flows to V_{dd}. Besides, a PMOS transistor instead of the NMOS transistor M_2 is used resulting in a higher subthreshold slope factor n (cf. section 3.1.1). The averaging of adjacent pixels by connecting the photodiodes has not been implemented in this version.

Figure 3.21 shows the layout of the photoreceptor embedded in a sensor array. The cutout includes two complete pixels and parts of the adjacent ones. All control and readout lines as well as the most important structures are indicated. The area occupied by one pixel is $33 \times 33\,\mu\text{m}^2$. The dominant structure is given by the photodiode whose size amounts to about 20 % of the pixel area. It is integrated as a n^+-substrate-diode to take advantage of the high quantum efficiency. Besides, the diode can be used as the drain of the switch transistors which select the according current path for readout and calibration.

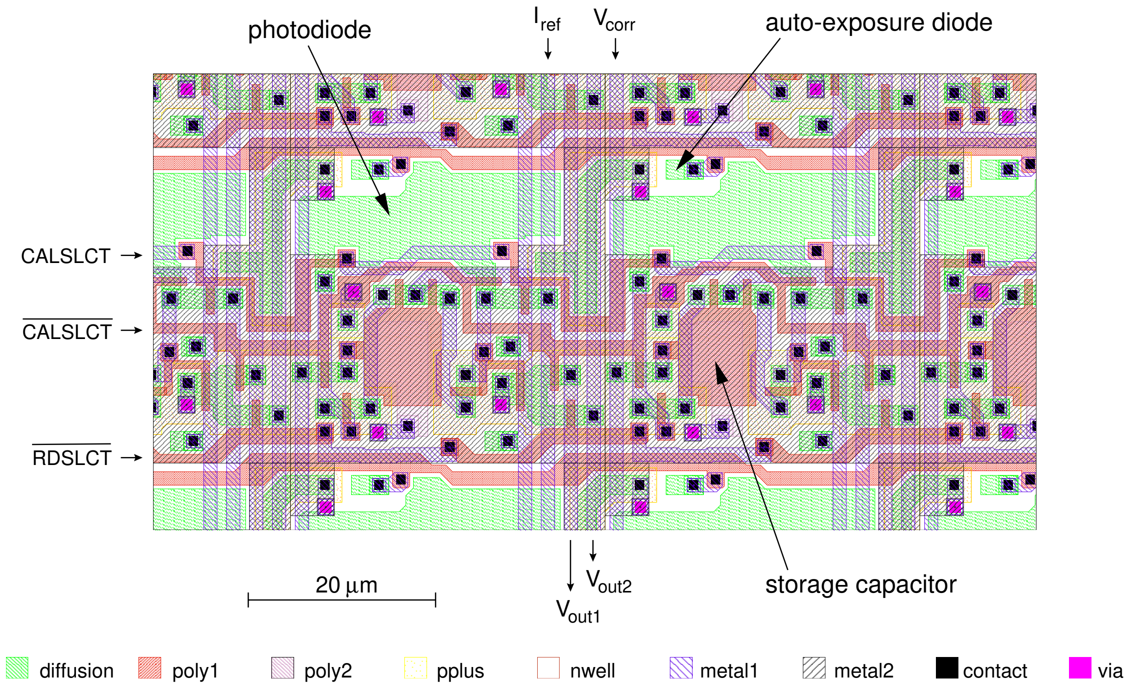


Figure 3.21: Cutout of a sensor array containing the self-calibrating photoreceptor in a 0.8 μm CMOS process. The size of one pixel is $33 \times 33\,\mu\text{m}^2$.

Since the CMOS process provides two polysilicon layers, the storage capacitor is implemented as a poly-poly capacitance. It shows a linear behaviour, good matching properties and possesses a high capacitance per area. The magnitude of the integrated capacitor amounts to about 100 fF. In order to realize the auto-exposure control, the reference current required for the self-calibration is extracted from small photodiodes (indicated as auto-exposure diode) in the pixels (cf. section 3.2.1). The dimensions of all transistors beside the wider readout source follower are $W = 2\,\mu$m and $L = 0.8\,\mu$m. Metal 2 shields the complete circuit except for the photodiode and provides the ground potential. Therefore, only one metal layer (metal 1) can be used for routing. For this reason the horizontal control lines consist of poly 1, which is only possible in the case of small sensor arrays ($< 100 \times 100$ pixels). In larger arrays the high resistance of the poly layer would result in too slow selection signals.

Layout in the 0.6 μm CMOS process

The last version of the photoreceptor layout has been realized in the AMS 0.6 μm CMOS process which provides three metal layers and one polysilicon layer. The corresponding circuit diagram including the averaging of neighbouring pixels is shown in figure 3.10. The subthreshold transistors M_1 and M_2 are implemented with the channel dimensions of $W = 2.9\,\mu$m and $L = 1\,\mu$m. The buffer transistor M_3 has a higher W/L ratio ($W = 3.5\,\mu$m, $L = 0.6\mu$m) to increase the transconductance g_m. The switch S_3 consists of a NMOS transistor with $W/L = 1.6/0.6$ and a transistor with half the size to compensate for the absolute charge injection (cf. section 3.2.3) and the variations. The residual switches are designed as minimum size transistors with $W/L = 0.8/0.6$.

The layout of the photoreceptor embedded in a larger sensor array is shown in figure 3.22. Two complete pixels as well as the adjacent structures can be seen. The size of the pixel layout amounts to $24 \times 24\,\mu\text{m}^2$. Nearly 30 % of the pixel area are occupied by the photodiode and about 10 % by the storage capacitance. Again, the diode is integrated as a n^+-substrate-junction. Because the second poly layer was only available with definite restrictions and to keep the design portable to other processes, it is not used. Instead the storage capacitor ($\approx$ 150 fF) consists of an NMOS transistor whose gate-channel-capacitance stores the correction voltage.

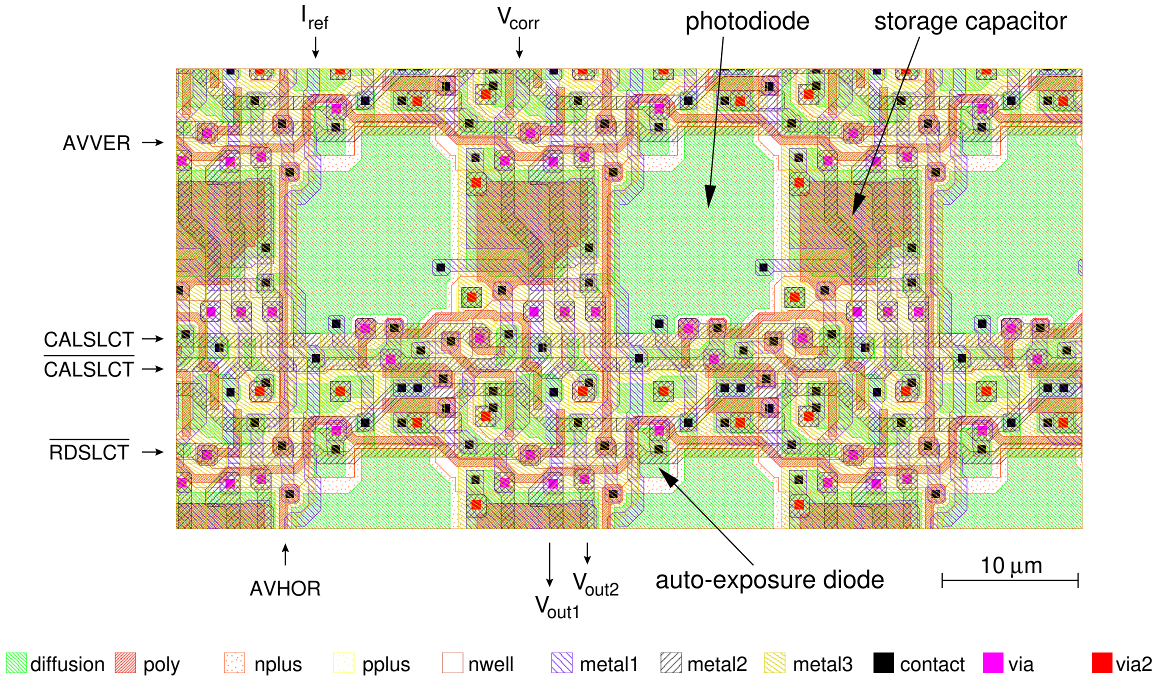


Figure 3.22: Cutout of a sensor array containing the self-calibrating photoreceptor in a 0.6 μm CMOS process. The size of one pixel is $24 \times 24\,\mu\text{m}^2$.

Due to the three metal layer process, two metal layers remain for routing if metal 3 is completely used for light shielding. The usage of the third metal layer is also the main reason why the pixel size is not increased in comparison with the mirrored layout in figure 3.17. The pixel pitch is still 24 μm although the storage capacitor and the photodiode occupy almost the same area. In order to save area the control lines for horizontal and vertical averaging are routed with poly. Here, the high resistance of poly lines only plays a subordinate role, because the signal changes can be very slow without influencing the performance.

On the basis of the presented pixel layouts, camera chips with different resolutions of the integrated sensor array have been realized. The design of the final image sensor is described in the next chapter, whereas the measurement results are presented in chapter 5.

Chapter 4

Image Sensor Design

The following chapter describes the design of the image sensors developed within the scope of this thesis. The main focus is on the final implementation, a camera chip with over 100k pixels. The general sensor architecture and the structure of the individual components are presented and explained. A few results of former chips as well as some simulations are shown to clarify special problems and their solutions. The first part of the chapter includes the analog building blocks like calibration circuits, readout multiplexer and operational amplifiers. The second part describes the digital control logic required for the calibration and the readout timing. Finally, a complete camera system containing the developed image sensor is presented.

The self-calibrating photoreceptor concept described in the last chapter should result in logarithmic image sensors with significantly reduced fixed pattern noise in comparison to uncalibrated sensor arrays. In order to demonstrate the principal functionality and to measure the real performance, image sensors on the basis of the self-calibrating pixels have been designed and manufactured. Besides the pixel array itself, they mainly include the control circuits for row and column selection, the signal amplifiers and the digital control part. Depending on the chip additional structures are implemented to obtain a camera chip more or less representing a single chip solution.

The final version, whose description makes up the main part of this chapter, includes a sensor array of 384×288 self-calibrating pixels and all additional components to allow the image sensor to work as a *camera on a chip*. A complete camera can be realized by combining the sensor chip with a small fixed focus, fixed aperture lens. Due to its high dynamic range, its flexible readout options and its compactness, this camera fulfills the given requirements of the tactile vision substitution system (TVSS).

4.1 Sensor architecture

Before explaining the individual components of the image sensor, a principal overview containing the basic building blocks and their connections to each other is presented. At first, a short summary of the different designed camera chips and the global architecture, which in principal applies for all developed image sensors, is given. Afterwards, a more detailed scheme of the final vision chip is described.

4.1.1 Realized image sensors

During the development of the self-calibrating image sensor, four chips including different pixel numbers and diverse pixel types have been realized. The first three designs represent test versions to examine the quality of the calibration concept and to test the main additional components. The fourth development consists of the final image sensor with over 100k pixels. The characteristic properties of the individual chips including design name, pixel type, pixel number, CMOS process and additionally implemented features are summarized in the following:

Vichi[1] 64×64 pixels, pixel type presented in the first part of section 3.3.2, 0.8 μm CMOS process with two metal and two poly layers, 33 μm pixel pitch, 3.5×2.5 mm^2 chip size, auto-exposure control, single analog output.

Oasys_vichi[2] 96×72 pixels, pixel type presented in section 3.3.1 (mirrored pixels), 0.6 μm CMOS process with two metal and one poly layer, 24 μm pixel pitch, 4.5×2.5 mm^2 image sensor size, auto-exposure control, single analog output, video timing selectable, pixel averaging, random pixel access and digital zoom.

Vichideo[3] 96×72 pixels, pixel type presented in the second part of section 3.3.2, 0.6 μm CMOS process with three metal and one poly layer, 24 μm pixel pitch, 5×2.65 mm^2 chip size, bias generation on chip (DACs), auto-exposure control, single analog output, video timing selectable, pixel averaging, random pixel access, digital zoom, on-screen display and EEPROM interface.

Divichi[4] 384×288 pixels, pixel type presented in the second part of section 3.3.2, 0.6 μm CMOS process with three metal and one poly layer, 24 μm pixel pitch, 11.5×7.7 mm^2 chip size, bias generation on chip (DACs), auto-exposure control, single analog output, video timing selectable, pixel averaging, random pixel access, digital zoom, on-screen display and EEPROM interface, analog-to-digital conversion (ADC).

The final implementation includes most of the building blocks already used in the previous designs. Therefore, a detailed description of the last sensor version, which will follow in the next sections, is sufficient to understand the functionality of all manufactured chips. However, problems with parts of the test chips which caused a redesign of the corresponding structures are mentioned at any rate. One example is the mirroring of devices, which results in an uncorrectable fixed pattern noise. Measurements of the sensor Oasys_vichi composed of mirrored pixels are already presented in section 3.3.1. Additional information about the first image sensor (Vichi) can be found in [LOO98], the third one (Vichideo) is presented in [LOO99].

The principal architecture, which is mainly the same for all four developed image sensors, is shown in figure 4.1. The sensor array composed of the self-calibrating pixels represents the main part. One row and one column are highlighted. The calibration amplifiers, responsible for comparing the pixel output voltages V_{out1} to the reference voltage V_{ref} and controlling the correction voltage V_{corr} as well as the current mirrors generating the column reference current, are located above the sensor array. There are as many amplifiers as array columns in order to calibrate one complete row at the same time. On the left side, the decoders for the readout and calibration row can be seen. They also include the corresponding digital drivers to control the selection lines (CALSLCT, $\overline{\text{CALSLCT}}$ and

[1] Vichi = <u>vi</u>sion <u>chi</u>p

[2] Oasys_vichi = <u>vi</u>sion <u>chi</u>p together with other designs integrated on a chip called OASYS.

[3] Vichideo = <u>vi</u>sion <u>chi</u>p with vi<u>deo</u> output

[4] Divichi = <u>vi</u>sion <u>chi</u>p with analog-to-<u>di</u>gital conversion on-chip.

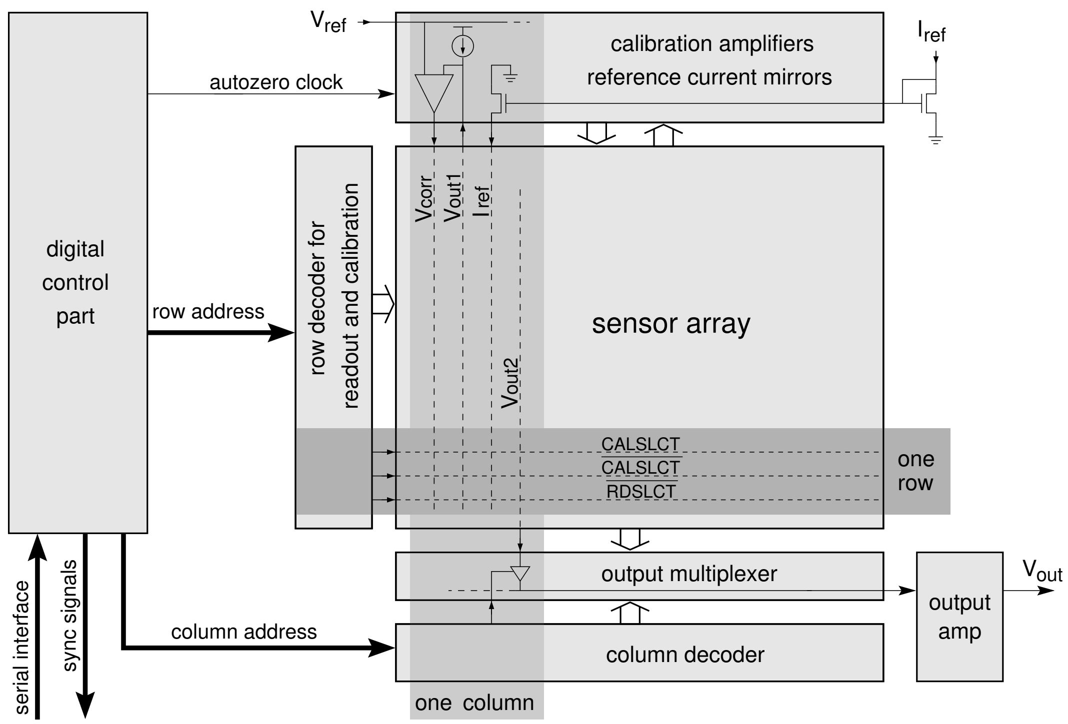


Figure 4.1: Principal architecture of the four designed image sensors.

$\overline{\text{RDSLCT}}$). For the readout, the pixel signals are guided to the bottom of the array. Then, the analog output multiplexer selects the individual columns in turn and generates one single output signal. The current column is selected by the column decoder below. Finally, the multiplexed signal is buffered or amplified to drive the off-chip load and to adapt the signal range to the subsequent input device.

The left block in the diagram represents the digital part responsible for the overall control of the chip. It produces the row and column addresses and the autozero clock for the calibration amplifiers. A serial interface allows to select different operation modes and to change parameters like calibration or readout timing. In addition, synchronisation signals indicating the start of a new frame or a new row and the availability of a new pixel value are generated to obtain the option of synchronizing the sensor with external processing electronics.

4.1.2 Final implementation with 110k pixels

The complete architecture of the high resolution vision chip with 384×288 pixels (Divichi, fourth item in the previous list) includes some additional building blocks compared to the general overview in figure 4.1. The extended architecture of this sensor chip can be seen in figure 4.2.

In reality, the sensor array consists of 386×290 pixels. The outer pixel rows and columns, however, can not be selected for readout. They represent dummy structures to avoid variations in the outer visible pixels due to border effects. The self-calibration occurs with the help of the autozeroing calibration amplifiers located above the receptor array. They are controlled by a clock circuit providing the required non-overlapping clocks switching between autozeroing and normal operation mode. The reference current mirrors generating the calibration currents are biased by a mirror circuit with adjustable gain. By this means, the reference current can be adapted to the averaged photocurrent $I_{auto-expo}$ of the small pixel diodes to realize the auto-exposure control. The current sources respon-

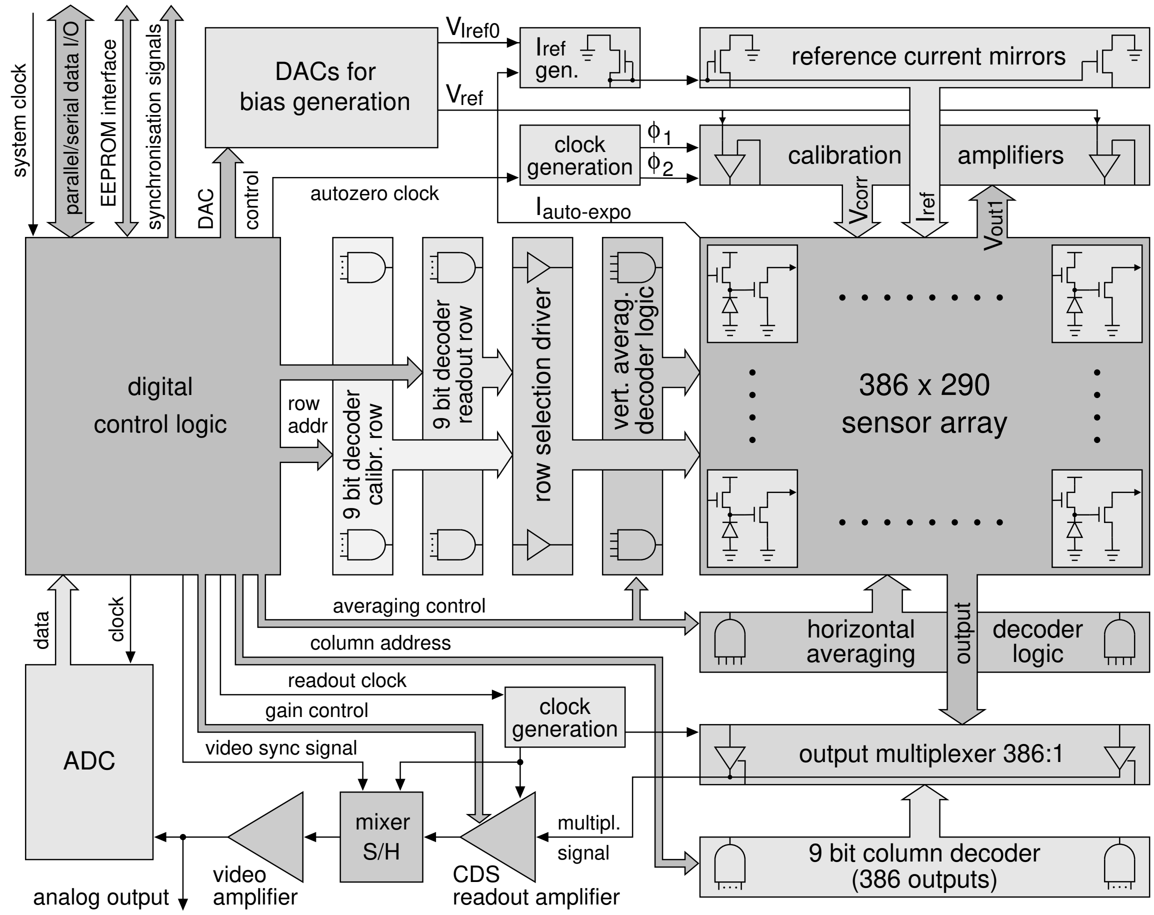


Figure 4.2: Extended architecture of the final image sensor divichi.

sible for the pixel readout source followers are omitted in the diagram. They are needed twice per column due to the separated output lines for calibration and readout.

The 9 bit decoders for selecting the calibration and readout row are located to the left of the photoreceptor array. They control the corresponding row drivers which are connected to the array selection lines. Additionally, there are decoders on the left of and below the sensor array to adjust the size of the averaged pixel clusters. During readout, the pixel signals are guided to the analog multiplexer controlled by the 9 bit column decoder below. The multiplexed output signal goes to the CDS (correlated double sampling, cf. 2.3.2) amplifier. Subsequently, a mixer with sample-and-hold stage combining the sensor output with the video synchronisation signal and the final video amplifier follow.

The analog output signal can be used to directly drive any video or other analog input devices. In addition, it can be converted into a digital signal on-chip. The corresponding ADC[5] generates a 10-bit digital value which can be read out via a parallel interface or a high speed serial link. Design and performance of the on-chip ADC are described in appendix A.

The overall number of required analog bias and control voltages on the image sensor amounts to 19. These voltages are provided by the bias generation block. It includes 19 DACs[6] converting 8-bit digital values into their corresponding bias voltages in the range of 0 V - 5 V. Only two examples

[5]analog-to-digital converter

[6]digital-to-analog converter

for the used bias signals are shown in the diagram: V_{ref} and V_{Iref0}. All other voltages will be mentioned when the according circuitry is described more in detail.

The large rectangle on the left side of the architecture diagram represents the digital logic responsible for the overall control of the chip. It generates the decoder addresses for calibration row, readout row, readout column and the clock signals for the calibration amplifiers, multiplexer, readout amplifier, mixer stage and the ADC and DAC circuits. Three interfaces (slow serial, fast serial and parallel) allow the chip to be programmed by changing internal register values. That way, different operation modes like zooming or averaging and all timing paramters can be selected. The fast serial and the parallel interface are bidirectional allowing to read out the ADC values as well as the complete internal register set. An additional EEPROM[7] interface offers the possibility to save the chip parameter values in an external EEPROM. The parameters are automatically recovered after a system reset. Finally, the digital part provides additional signals for the synchronisation with external electronics.

The next sections present the design and the functionality of the individual image sensor components. They are grouped into calibration circuits, selection circuits, readout circuits, bias generation and digital control logic. As mentionend above, the ADC description can be found in appendix A since it represents a stand-alone development which is not only dedicated to the image sensor but also for other applications.

4.2 Calibration circuits

The image sensor part responsible for carrying out the self-calibration method consists of the autozeroing calibration amplifiers and the reference current sources. Besides, an adjustable current mirror and a clock generation circuit are implemented. Before describing these components some measurement results of the first image sensor (Vichi) are presented because they led to a redesign of the calibration building blocks.

4.2.1 Measurement results of the first sensor implementation

The image sensor *Vichi* was the first one with self-calibrating logarithmic photoreceptors. The measurements carried out with this chip confirm the principal feasibility of the self-calibration. Besides, they give hints which sensor parts have to be improved to obtain better results, i.e. less remaining fixed pattern noise. To understand the applied improvements, these measurements are presented before the description of the calibration circuits.

Measurements were carried out with a frame rate of about 20 Hz using a white light source (xenon arc lamp). Since the sensor output voltage can be shifted to any level by changing the reference voltage V_{ref}, the absolute voltage in the following figures has no meaning. Only voltage differences describe the essential chip behaviour. Figure 4.3 shows the response of one photoreceptor of the 64×64 pixel matrix measured over 8 decades of incident intensity. From 10^{-3} W/m^2 to 10^3 W/m^2 the receptor has the expected logarithmic behaviour. The slope in this logarithmic region amounts to 110 mV per decade. This is an important value because the other measurements have to be compared to it in order to get a normalized fixed pattern noise value.

At very low intensities the signal slope decreases. The reason is the small photocurrent which on one hand needs a long time for charging parasitic capacitances and on the other hand reaches the region of the diode's dark current. At illumination levels higher than about 10^3 W/m^2 the slope

[7] electrically erasable programmable read only memory

suddenly changes its direction (dashed line). This effect is caused by the imperfect shielding of the switch transistor normally forcing the electric charges to stay on the storage capacitor. Parasitic photocurrents rapidly discharge the capacitor after calibration in a way that the correction voltage V_{corr} has noticeably moved before the pixel is read out.

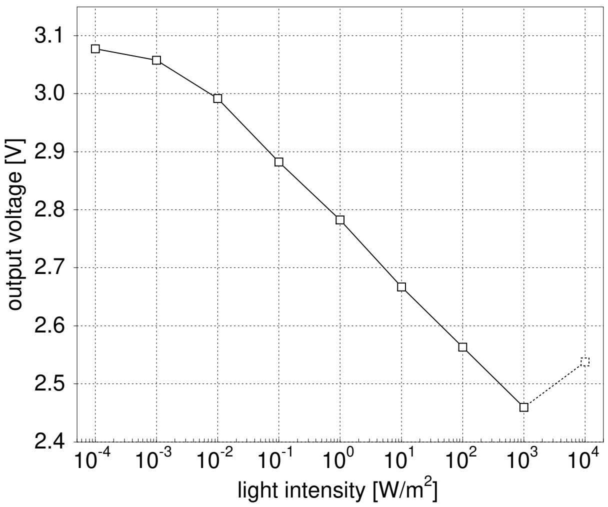


Figure 4.3: Pixel response measured over 8 decades of incident light intensity. The dashed line at high illumination results from the discharge of the storage capacitor by parasitic photocurrents.

The remaining offset distribution of the individual pixel voltages after applying the self-calibration is shown in figure 4.4 with respect to one column and in figure 4.5 with respect to the complete array. The data is taken at a uniform illumination of 4 W/m^2. The rms value of the variations in one column amounts to 2.58 mV. This corresponds to 2.3 % of one decade in light intensity when weighting with the slope of 110 mV/decade. Compared to the uncalibrated pixel column presented in section 2.2.2 which shows a rms value of about 90 % of a decade, this means a fixed pattern noise reduction by a factor of 40.

Regarding the complete array (figure 4.5) the rms value increases by a factor of almost 3 to 6.1 mV. This value corresponds to 5.5 % of a decade. The reason for the larger fixed pattern noise

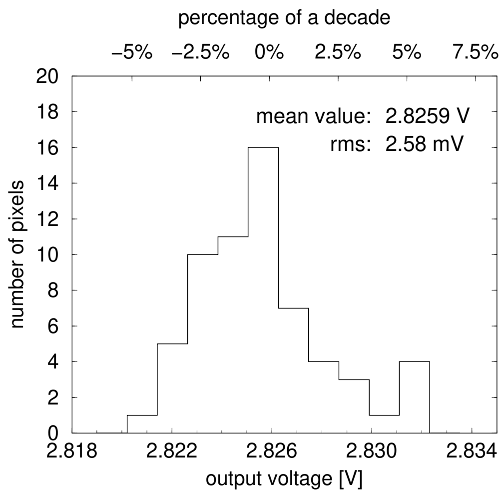


Figure 4.4: Offset distribution of one array column at an intensity of 4 W/m^2.

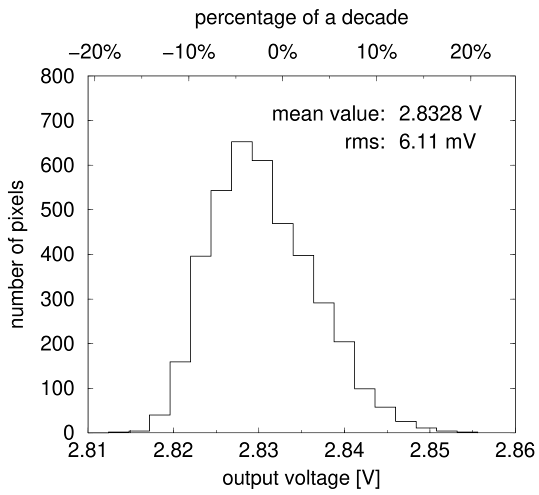


Figure 4.5: Offset distribution of the complete sensor array at an intensity of 4 W/m^2.

of all pixels in comparison to one column is given by additional column-to-column variations. In order to get an impression of the geometric distribution of the remaining photoreceptor offsets, a three-dimensional view is shown in figure 4.6. The variation from column to column can be seen, particularly at the region around column 25 which is elevated against the residual pixels.

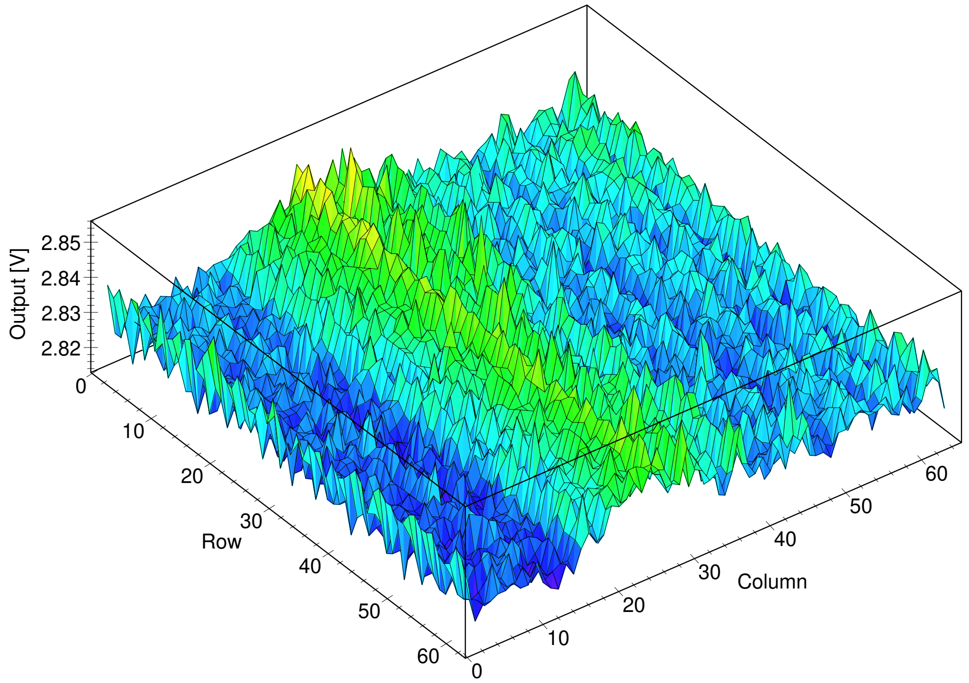


Figure 4.6: Geometric offset distribution of all 4096 calibrated pixels at an intensity of 4 W/m^2. The large column-to-column variations are apparent.

As a consequence of the increased non-uniformity between the array columns, pictures taken with this sensor chip show a slight stripe pattern. An example of this effect is given in figure 4.7. It shows two images of the letter A. The contrast between background and letter is about 80 % of an intensity decade. The left image represents the original data. Vertical stripes corresponding to the different column mean values are apparent. The image shown on the right in part b) is corrected for the column variations by calculating the individual column mean values and subtracting them from the pixel values (by software).

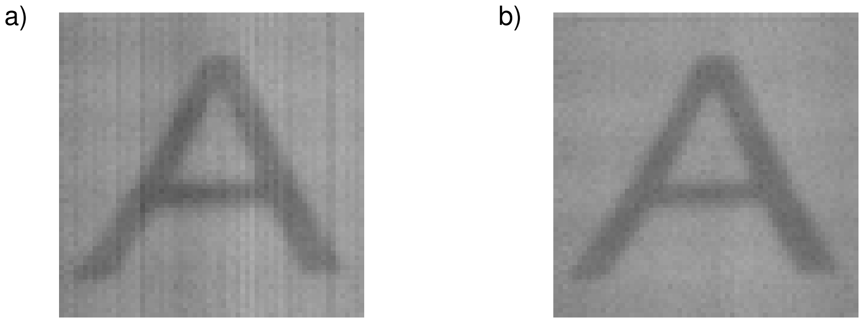


Figure 4.7: Two images of the letter A, taken with the 64×64 image sensor. The left one shows the original data, whereas the right one is corrected with regard to the column-to-column variations.

Before applying the self-calibration concept to larger image sensors, the problem of the remaining column fixed pattern noise should be solved. The reason for the column variations coheres with the reference current generation and the input offset of the calibration amplifiers. The output multiplexer does not contribute since it includes no active amplifiers but only switches. The pixel signal is completely driven down to the single output amplifier by the source follower included in every receptor.

The matching of the reference current is determined by the matching of the mirror transistors. To reduce the mismatch, they have to be implemented using wide and long channel geometries (cf. the measurements in section 2.2.2). Besides, a proper layout including dummy structures and splitting one transistor into several parts can reduce the non-uniformity of the reference current. Therefore, an improved design of the mirror transistors has been realized in the image sensors Vichideo and Divichi.

The influence of the input offset variations in case of the calibration amplifiers should be cancelled by the autozeroing mechanism (cf. section 3.2.4). However, due to some side effects, the offset compensation does not work perfectly. On the one hand, the magnitude of the remaining non-uniformities depends on the intial input offset variations since they are only reduced by the gain of the amplifier. Larger initial mismatch means larger remaining variations. On the other hand, the charge injection of the MOS switches shifts the voltage stored on the compensation capacitor. Hence, a large capacitor should be used to reduce the charge injection influence.

4.2.2 Autozeroing calibration amplifier

Design and functionality

The calibration amplifier, which is implemented in the final image sensor, represents an improved version compared to the first implementation. The circuit diagram is shown in figure 4.8. It mainly consists of a typical two-stage operational amplifier with Miller compensation and the additional autozeroing circuitry. The channel dimensions (W/L) of the individual transistors are written below the transistor identifier M. The switches selecting the operation mode (normal or autozeroing) are realized as single MOS transistors. Transmission gates (two complementary transistors) are not required because the voltage swing is limited to a range which, in any case, can be covered by one switch transistor. Depending on the absolute voltage level, NMOS or PMOS devices are used. The

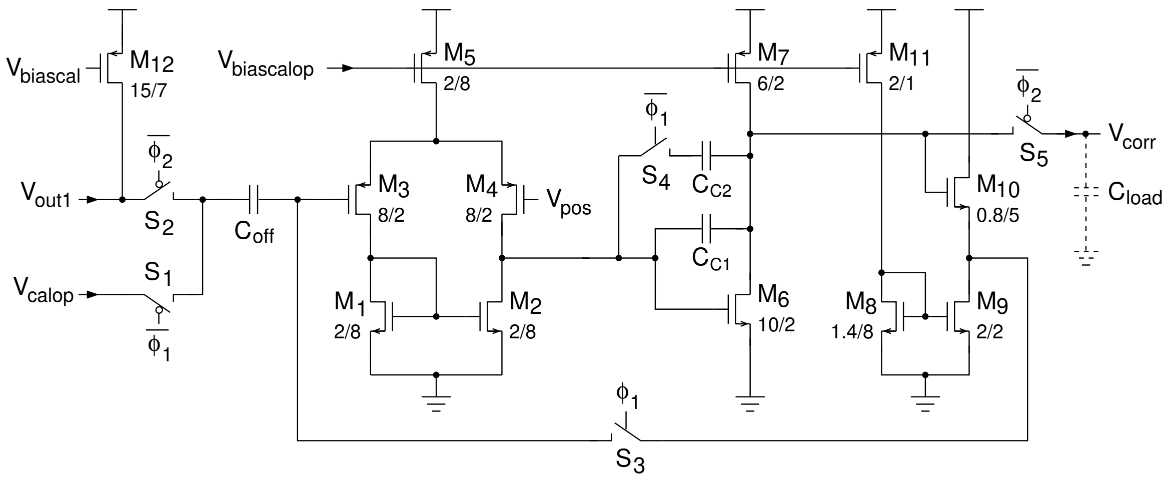


Figure 4.8: Circuit diagram of the autozeroing calibration amplifier.

transistor M_{12} works as current source for the pixel readout source follower. It has a wide and long channel to reduce the column-to-column mismatch.

The differential input stage is composed of the transistors M_1 to M_5. The source-coupled pair M_3 and M_4 is controlled by the two input signal V_{pos} and V_{out1}. Together with the current mirror transistors M_1 and M_2 which are used to form the active load devices, a gain of more than 100 is achieved. The working current is provided by M_5 and can be adjusted by changing the bias voltage $V_{biascalop}$. A detailed description of differential input stages in general can be found in [LAK94-1]. A good matching of the two transistor pairs M_1, M_2 and M_3, M_4 is essential to obtain a low intrinsic offset. Therefore, they should have large dimensions. Unfortunately, this would result in a high input capacitance. Consequently, the actual size has to be a tradeoff. Due to the self-calibrating amplifier concept, a medium transistor size is sufficient leading to a relatively small input capacitance.

The transistors M_6 and M_7 form the second stage which is an inverting amplifier with a gain of more than 100. It directly drives the output line V_{corr} since no third buffer stage is implemented. The Miller capacitances C_{C1} and C_{C2} perform the frequency compensation by slowing down the first stage. Due to the Miller effect the capacitance is increased by the gain of the second stage and thus results in a high load of the differential stage. The capacitor C_{C2} can be switched off to increase the amplifier speed during the autozeroing cycle. In this case, only a weak compensation is required as the switch S_5 interrupts the connection to the amplifier output. The capacitance C_{C1} is 80 fF, whereas C_{C2} is significantly larger and amounts to 1.7 pF.

Pulling ϕ_1 up and ϕ_2 down changes from normal operation to autozeroing mode. $\overline{\phi_1}$ and $\overline{\phi_2}$ correspond to the inverse clock signals. Thereby, the switches S_1 and S_3 are closed, whereas the residual ones are off. The amplifier output is separated from the column line and fed back to the negative input. The source follower stage consisting of M_9 and M_{10} is used to shift the absolute voltage level. This is necessary because only MOS capacitors can be implemented due to the single poly process. They need a minimum voltage of at least V_T (threshold voltage) between their nodes to show a reasonable capacitance. The voltage drop at C_{C1} and C_{C2} would become too small if the unshifted output voltage is directly fed back. The offset capacitor C_{off} also needs this minimum voltage difference between its two nodes. Therefore the positive input signal has to be V_T lower than the autozeroing reference V_{calop}.

After charging C_{off} to the appropriate offset correction voltage, ϕ_1 goes low and ϕ_2 goes high. Thus, the switches S_2, S_4 and S_5 are closed, S_1 and S_3 are opened and the amplifier returns to normal operation. Remaining offset variations between the individual amplifiers are caused by the charge injection of switch S_3. It can be reduced by using a large capacitor C_{off}. The implemented value of C_{off} amounts to about 1 pF which results in a low charge injection influence and in storage times of at least several 100 μs even at very high light intensities. The autozeroing cycle takes only a few microseconds and can be carried out each time before a new sensor row has to be calibrated.

Simulations of the transfer characteristics

The different behaviour of the calibration amplifier in case of weak and strong compensation, respectively, has been simulated. The results with respect to the frequency transfer function are shown in figure 4.9 for the small load capacitance of 10 fF and in figure 4.10 for the larger capacitance of 10 pF. The latter one corresponds to the correction line capacitance in one column of the complete sensor area and therefore represents a realistic value. The bias voltage $V_{biascalop}$ was set to 3.8 V resulting in a current of 170 nA for the first differential stage and about 2 μA for the second stage. Using these settings, the maximum open loop gain is 103 dB. The -3 dB decrease is reached at a frequency of 26 Hz for the small compensation capacitance and at a frequency of 1.1 Hz for the large one. The unity gain bandwidth depends on the compensation as well as on the load capacitance. Regarding the output load of 10 fF, it results in 2.88 MHz (C_{C2} disabled) and 162 kHz (C_{C2} enabled), respectively. Increasing the load to 10 pF, the unity gain bandwidth decreases to 1.07 MHz in case of the weak compensation (C_{C2} disabled), whereas it amounts to 156 kHz (almost equal to the value corresponding to the small output load) if C_{C2} is enabled.

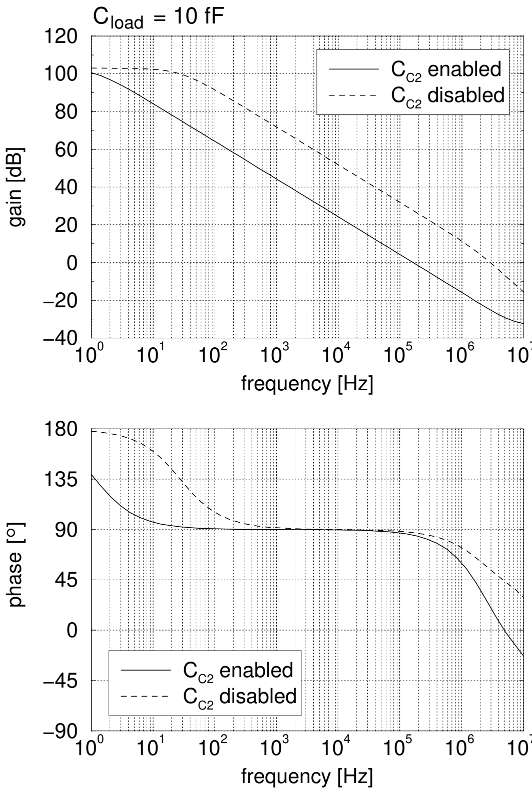


Figure 4.9: Simulated frequency response (Bode-plot) of the calibration amplifier with a small load capacitance of 10 fF.

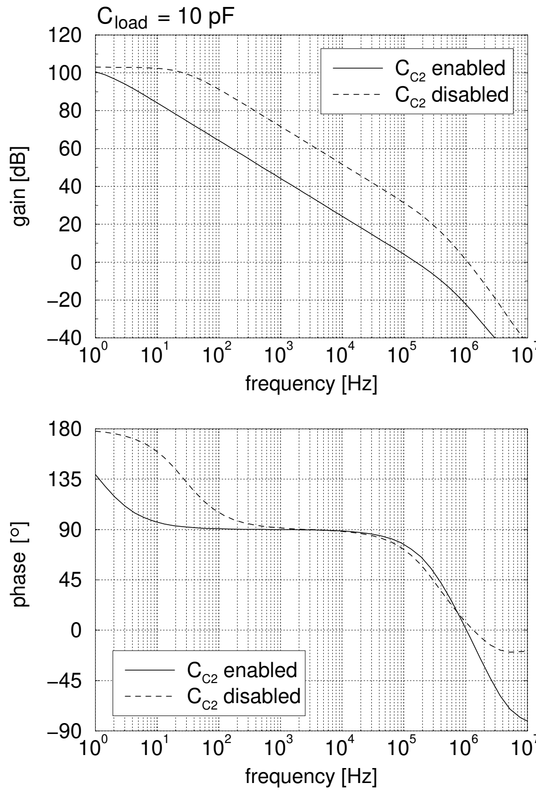


Figure 4.10: Simulated frequency response (Bode-plot) of the calibration amplifier with a large load capacitance of 10 pF.

The phase behaviour, which is plotted in the lower diagrams of the frequency response, allows to predict the stability. The phase margin at the unity gain frequency always exceeds 65° except for the case using the large output load and the uncompensated amplifier (figure 4.10). This means that apart from the latter case a stable behaviour is obtained independently of the compensation method. Therefore, the faster operation mode can be used to calibrate the amplifier which results in a shorter autozeroing cycle. Large load capacitances like the correction line going to the individual pixels of one column require the better compensation by the additional capacitor C_{C2}.

Layout implementation

Figure 4.11 shows the layout of the calibration amplifier. It is rotated by 90° to better fit on the page. Hence, the sensor array is located on the right side. The readout line V_{out1} and the correction line V_{corr} going into the pixel array can be seen. The width is equal to the pixel pitch of 24 μm. The length including the bias transistor M_{12} is 175 μm. Metal 3 shielding the complete design against light has been omitted in the plot in order to achieve a better recognizability of the individual structures. It can be seen, that the three capacitors take up the most space. However, they would be more than ten times larger if no MOS capacitors but so-called metal-metal-poly sandwich capacitors were used. For this reason, it is the better choice to cope with the drawbacks of the MOS transistors by adding the above mentioned circuitry than implementing the much larger sandwich devices.

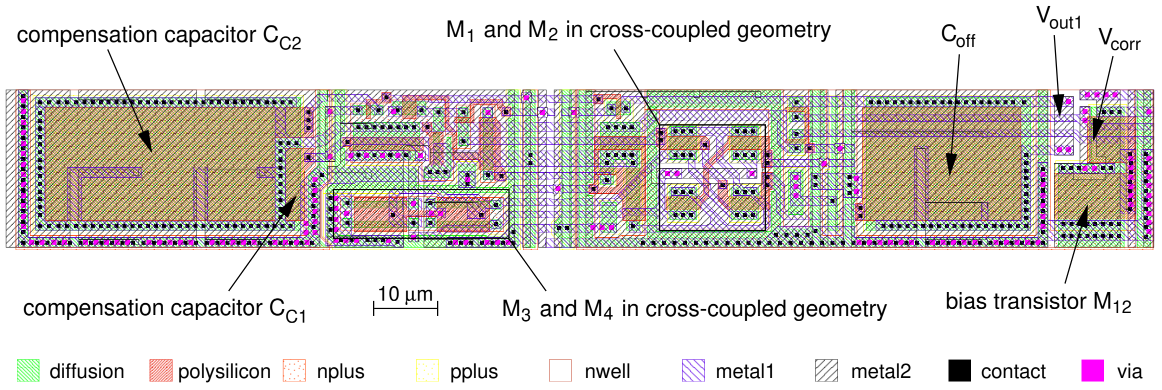


Figure 4.11: Layout of the autozeroing calibration amplifier.

Both the transistor pairs M_1, M_2 and M_3, M_4 have been layed out in a cross-coupled geometry to achieve a better matching behaviour. That way, most of the influence caused by process parameter gradients is eliminated by averaging. However, mismatch due to local parameter fluctuations still exists. It is reduced to a large extent by applying the autozeroing mechanism.

4.2.3 Non-overlapping two phase clock

The actual operation mode of the calibration amplifier is controlled by the two clock signals ϕ_1 and ϕ_2. They are not allowed to be active at the same time because this would cause a short circuit between the input signals V_{out1} and V_{calop}. The required non-overlapping clocking scheme, which avoids this forbidden state, is shown in figure 3.16 of section 3.2.4 (explanation of the autozeroing concept). In addition, the inverted clocks $\overline{\phi_1}$ and $\overline{\phi_2}$ have to be generated. In case of the second clock ϕ_2 only the inverted signal $\overline{\phi_2}$ is used for the amplifier control.

The circuit diagram performing the non-overlapping clock generation is shown in figure 4.12. It consists of 2 nand-gates and some inverters. ϕ_{az} represents the main clock selecting between autozeroing and normal operation mode. The circuit functionality is explained with respect to the inverted clock signals $\overline{\phi_1}$ and $\overline{\phi_2}$. This means, that both signals are not allowed to be low at the same time. Regarding the case ϕ_{az} = low results in a high $\overline{\phi_1}$ and a low $\overline{\phi_2}$. When ϕ_{az} goes high, the

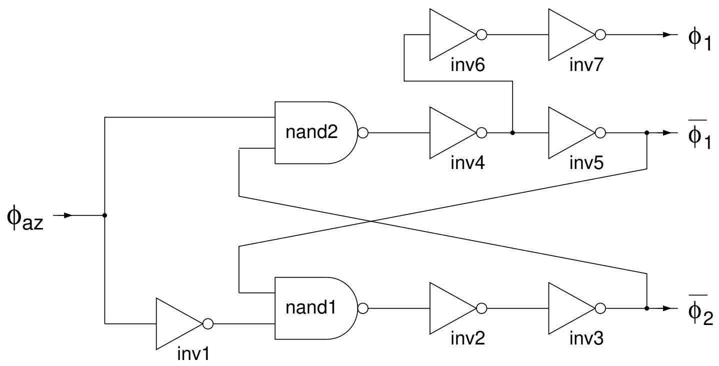


Figure 4.12: Diagram of the logic circuit generating the non-overlapping two phase clock.

input signal of the lower nand-gate (nand1) goes low. Consequently it changes its state leading to a high $\overline{\phi_2}$. The upper nand-gate (nand2), however, is switched off as long as $\overline{\phi_2}$ is low. Hence, a change in the signal $\overline{\phi_1}$, which is still high, can only happen when $\overline{\phi_2}$ has gone high.

Switching back by pulling ϕ_{az} low gives the same behaviour in the opposite direction. The clock signal $\overline{\phi_2}$ can only go low if $\overline{\phi_1}$ is already high. For this reason, the case that both clocks are low at the same time never occurs. The non-inverted clock ϕ_1 also required for the amplifier control is obtained by inverting the $\overline{\phi_1}$ signal before passing the last inverter. One clock circuit is used to drive the complete row of 386 calibration amplifiers. Therefore, the last inverter stages have to drive a high capacitive load. They are implemented with a medium driver strength ($W = 6\,\mu$m for the PMOS) in order to achieve slow switching times in the region of 100 ns. This reduces the crosstalk between clocks and analog signals.

4.2.4 Reference current generation

In order to calibrate one complete pixel row at the same time, not only the calibration amplifier but also the reference current is required individually for each column. The generation of a number of equal currents can be achieved by using the corresponding number of transistors and biasing them with the same voltage. Due to device mismatch, however, the resulting currents differ from each other. The typical magnitude of the current variations has been measured in the case of large transistors driven in weak inversion and is presented in section 2.2.2. The current non-uniformities can be further reduced by applying a special layout implementation: dividing one transistor in several parts and spreading them over a large area. By this means, higher spatial frequencies of the process parameter variations are averaged.

Figure 4.13 shows the circuit diagram of one complete current source transistor and parts of the adjacent ones. They are implemented as NMOS devices, which means, that they actually represent current sinks. Nevertheless, they are usually called sources if the sign of the current is not important. The transistor belonging to the n-th column is highlighted. It is composed of five smaller transistors in parallel which are spread over five neighbouring columns. On the other hand, one column includes five sub-transistors corresponding to the adjacent columns. The absolute current magnitude is controlled by the bias voltage V_b, which is generated by a current mirror outside the transistor row.

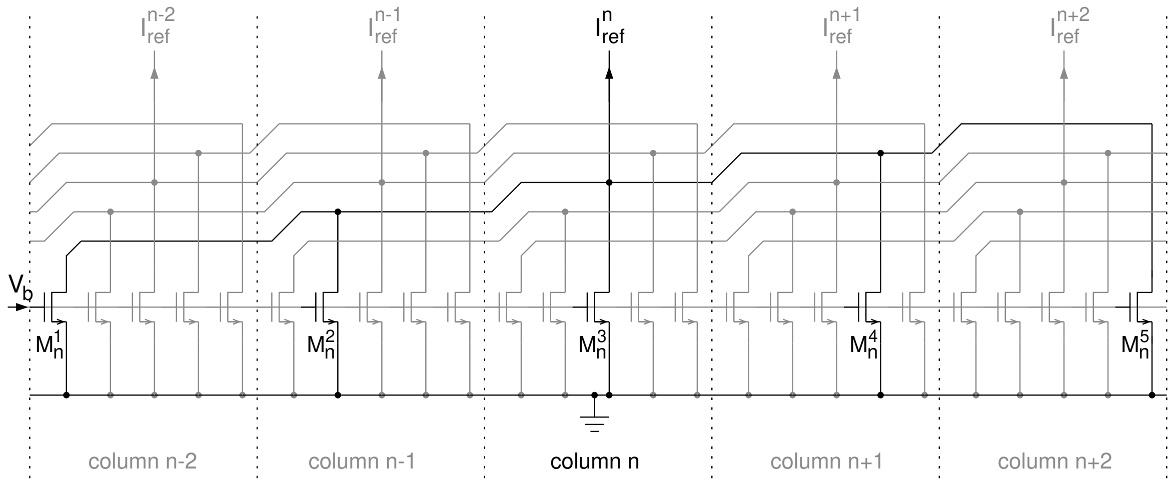


Figure 4.13: Circuit diagram of the spread current source transistors to reduce the column-to-column variations. The five parts corresponding to the middle current source (column n) are highlighted.

The channel dimensions of one sub-device are $W = 4\,\mu$m and $L = 12\,\mu$m. The total width of the current source transistor hence amounts to $W = 5 \cdot 4\,\mu\text{m} = 20\,\mu$m. Consequently, process parameter fluctuations locally arising in the region of one column only influence one sub-transistor. Besides, the neighbouring reference currents are affected in the same way due to their transistor part located in the actual column.

The layout of the well-matched current source transistors is shown in figure 4.14. Compared to the circuit diagram it is vertically mirrored. The sensor array starts below the drawn layout, the previously described calibration amplifiers are located above. The five transistors generating the reference current for the middle column (column n) are indicated by black frames. In addition, small precharge transistors (one per column) can be seen. When activated, they pull down the reference line potential to a definite level. This is done before each calibration cycle to obtain the fast signal rise demonstrated in figure 3.6. By this means, a shorter calibration time particularly at low reference currents is achieved.

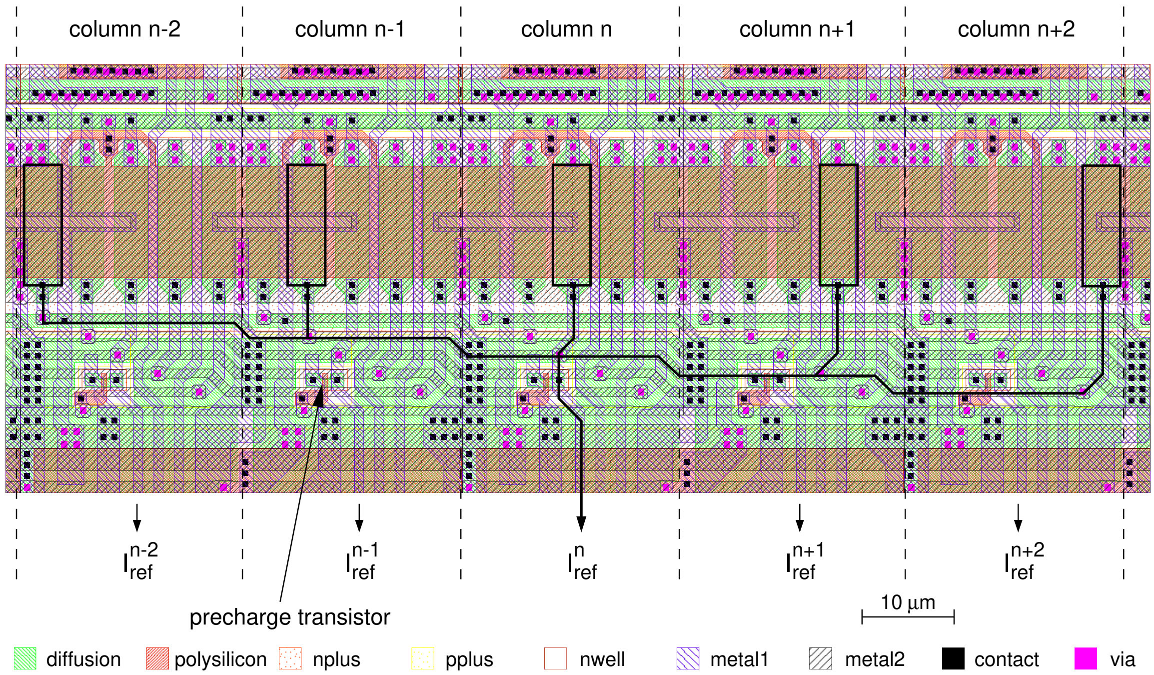


Figure 4.14: Layout corresponding to the circuit diagram in figure 4.13. The five transistors of the middle current source (column n) are indicated.

4.2.5 Current mirror with selectable gain

The reference current generated by the well-matched NMOS-FETs can be adjusted by changing the bias voltage V_b. A high current leads to shorter calibration times but higher remaining fixed pattern noise at low intensities due to the slope variations. A low current improves the fixed pattern noise but worsens the calibration time. Furthermore, a coupling between V_b and the summed current of all auto-exposure diodes in the pixels results in an automatic adapation of the output signal to the current illumination (automatic exposure control).

In order to enable all described options, a current mirror with selectable input signal and selectable current gain has been implemented in the image sensor. The according schematic diagram is shown in figure 4.15. Again, the drawn switches are realized as single MOS transistors. In principal, the circuit includes two different possibilities for generating the voltage V_b. The first one is chosen when S_3 is switched off by pulling down the digital signal AEN (auto-exposure enable). In that case, transistor M_{18} delivers a current I_{ref1} according to the applied bias voltage $V_{refcurr}$. The current flows into the drain node of the NMOS transistor M_{19}. It is converted into the voltage V_b and finally mirrored into the individual columns by the reference current transistors. That way, the reference current can be set to any value by changing $V_{refcurr}$.

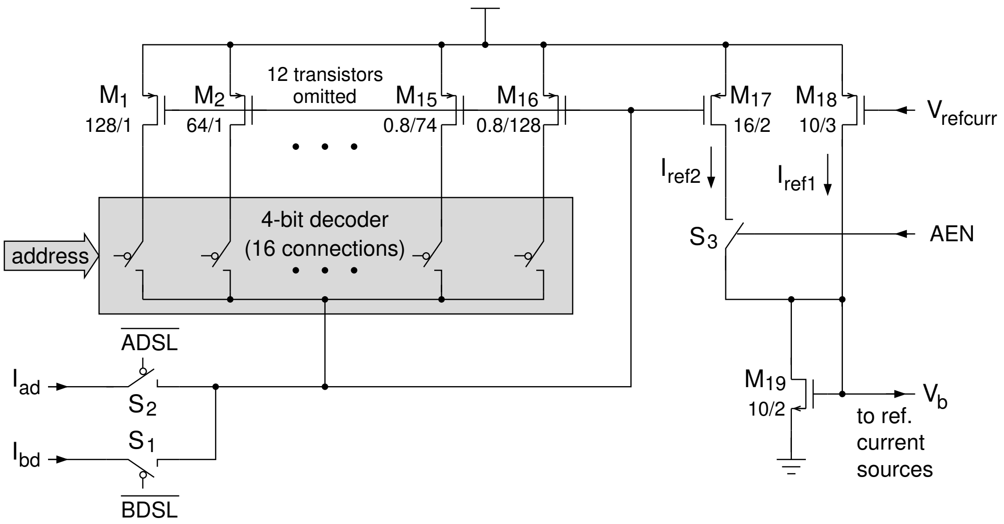


Figure 4.15: Schematic diagram of the bias voltage generation for the reference current sources.

The second possibility for controlling the bias voltage V_b is enabled by pulling AEN high. Switch S_3 is closed and adds the current I_{ref2} to the total current through M_{19}. It is produced by the current mirror consisting of M_{17} and one transistor out of M_1 to M_{16}. Therefore, I_{ref2} corresponds to the input currents I_{ad} and I_{bd}, respectively, depending on the state of the switches S_1 and S_2. I_{ad} means the total current of the auto-exposure diodes in the pixels, whereas I_{bd} stems from photodiodes located around the sensor array (border diodes). The latter ones show a lower relative capacitance (with respect to the generated photocurrent) due to the shorter connection lines and consequently react faster to intensity changes. On the other hand, they only represent the average of the image border which differs from the total averaged illumination. For a proper auto-exposure control, the array diodes should be used. The active-low signals $\overline{\mathrm{ADSL}}$ and $\overline{\mathrm{BDSL}}$ control S_1 and S_2 selecting the corresponding photodiodes.

In order to adapt the current I_{ref2} to the photocurrents I_{ad} or I_{bd}, the gain of the current mirror can be adjusted in a wide range from 0.1 to 2000. The actual gain factor is selected by enabling one of the 16 possible mirror transistors M_1 to M_{16} with the help of a 4-bit address decoder. The step size between the gain of two adjacent transistors is always a factor of two resulting in a logarithmic distribution of the different gain values. The active transistor can be selected by programming the corresponding register value in the digital logic.

As the sum of I_{ref1} and I_{ref2} determines the reference current, the minimum current is given by I_{ref1}. This is important to keep the self-calibration in a stable state if the sensor chip is used in a dark environment. Here, the photocurrent of the auto-exposure diodes can nearly disappear (or saturate due to dark currents) leading to a negligible current I_{ref2}. Thus, $V_{refcurr}$ has to be set to a voltage which always holds the reference current high enough for calibrating the photoreceptors.

4.3 Row and column selection circuits

Basically, two different implementations are commonly used to select a specific column or row of an array: shift register selection and address decoder selection. The former one merely requires a number of identical flip-flops which are connected in series. During initalization, the first flip-flop is loaded with a logical one selecting the first array row. Every clock cycle, the bit is shifted by one cell and successively selects all rows. An example of the shift register selection method is given in section 2.2.1. In contrast to this method, the decoder implementation directly converts a binary address into the selection signal for the corresponding row. It has the advantage that a very fast access to any part of the array is possible.

4.3.1 Address decoder

Since the image sensor has to be able to quickly read out subframes, the decoder instead of the shift register solution is used. The principal operation will be explained by means of a 2-bit decoder which can be seen in figure 4.16. The two address signals coming from the left first go through an inverter stage to get the inverse signals. Then, the decoding logic composed of and-gates with two inputs each follows. Depending on the address of the output line, the corresponding gate inputs are connected to the normal or the inverse address line. By this means, exactly one output line is active for every applied address.

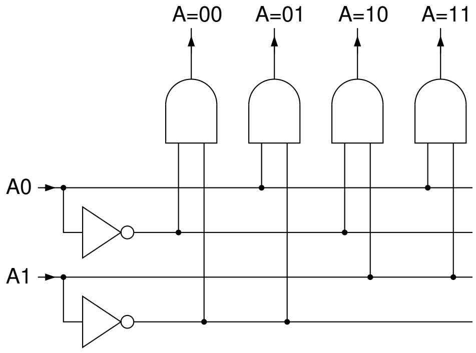


Figure 4.16: 2-bit address decoder using and-gates.

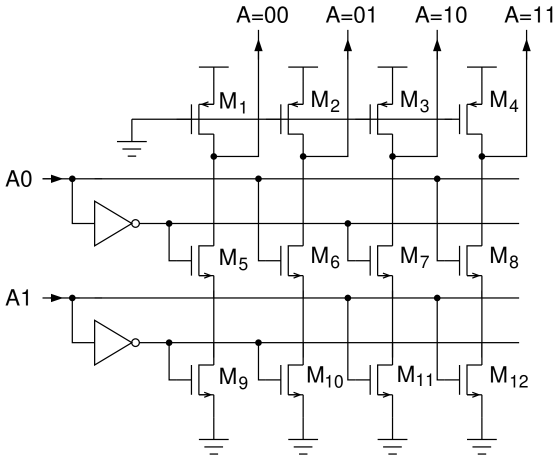


Figure 4.17: 2-bit address decoder using pull-up transistors.

The typical implementation of and-gates (or better nand-gates) requires as many NMOS-PMOS-pairs as input lines. Regarding a 9-bit decoder which is integrated in the developed image sensor, 18 transistors per cell are needed. The solution shown in figure 4.17 uses only one PMOS device per output line as a pull-up transistor (M_1 to M_4). It therefore manages the desired functionality with $n+1$ transistors if n is the number of address bits. However, since the pull-up resistor is always active, a current flows in the selected decoder column. Consequently, the dimensions of the PMOS pull-up transistors determining the current magnitude represent a tradeoff between power consumption and rise time.

In the case of a decoder with many address bits, the described implementation causes an additional difficulty. The selection transistors (M_5 to M_{12} in figure 4.17) are connected in series leading to a high resistance. This limits the fall time of the output signal. Using or- instead of and-gates or the according version with one pull-down NMOS transistor offers the possibility to control the fall time with the help of the pull-down current. However, this current flows in all decoder columns besides the selected one and therefore results in a high power consumption. Regarding the required 9-bit decoder for the sensor array, the first implementation shown in figure 4.17 is used because it is still fast enough for the sensor application and additionally saves current.

The 9-bit address decoder has been designed in two different versions. The first one converting the input address into 290 output lines is used twice: for the calibration row selection and for the readout row selection. Both decoders are located on the left of the sensor array. The second version situated below the array possesses 386 outputs and controls the column multiplexer. The principal interconnections of the decoders with the residual circuitry can be seen in the architecture diagram in figure 4.2. The pitch between two decoder outputs is equal to the pixel pitch of 24 μm. Since the selection transistor size is much smaller, additional area exists in each cell. To take advantage of this unused space, power blocking capacitors have been integrated to reduce the switching noise. They are realized as MOS transistors and amount to about 500 pF for one complete decoder.

4.3.2 Speed controllable line drivers

In order to keep the transistor size and the pull-up current small, the decoder outputs only have a low driver strength. Consequently, an additional line driver is inserted between the decoder and the calibration as well as the readout row selection lines. In case of the readout row selection the driver simply consists of two sequent CMOS inverters with increasing driver strength. It is shown in part a) of figure 4.18. The channel dimensions of the included NMOS and PMOS transistor are written above and below the inverter symbols. The input signal $\overline{\text{DO}}$ comes from one of the decoder outputs and results in the selection signal $\overline{\text{RDSLCT}}$.

Regarding the calibration row selection shown in part b) of figure 4.18, a slightly more complicated circuit is used. The first inverter stage (INV1) is equal to the readout line driver. Then, the signal is split into a normal and an inverted path. The current through the second inverter stages INV3 and INV4 generating the CALSLCT signal and the inverse $\overline{\text{CALSLCT}}$ signal can be controlled by the transistors M_1 and M_2. By this means, the rise and fall times of the selection signals become adjustable and an optimal setting can be found during the normal operation of the image sensor.

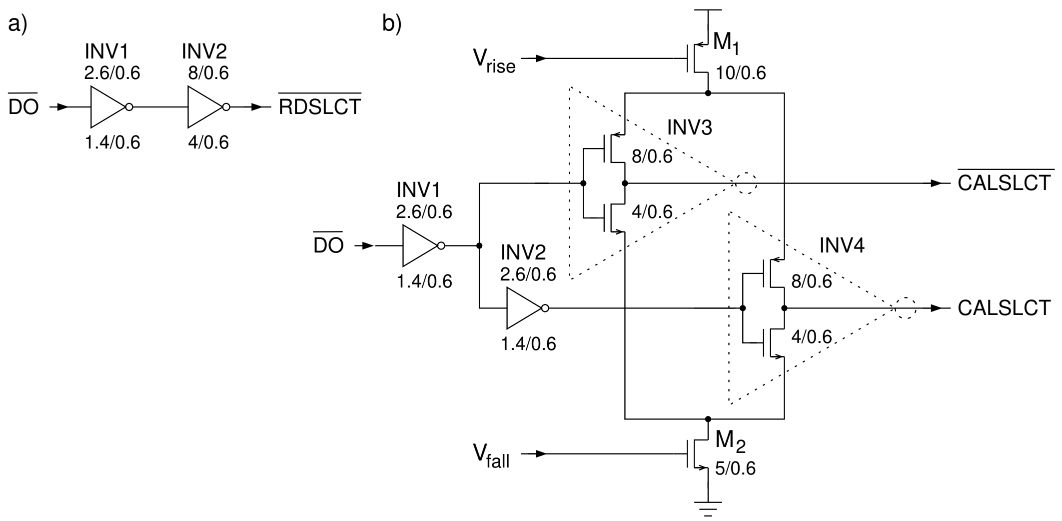


Figure 4.18: Circuit diagram of the selection line drivers for the readout and calibration rows.

Two reasons cause the requirement of selection signals with slowed rise and fall times. On one hand, the charge injection onto the storage capacitor in the photoreceptor circuit is reduced. As the switch transistor separating the capacitor from the correction line is conductive as long as the gate-source-voltage is above the threshold voltage V_T, a current compensating for the charge injection can flow through the switch. Due to the finite conductance of the switch, the current is limited to a certain value. Therefore, if using selection signals with longer rise times, the compensation current is flowing for a longer time resulting in a better charge injection cancellation.

The other effect leading to the need of slowly rising switching signals stems from the decoder. Due to the generation of the address input signals in the digital logic part, the timing of the individual address lines differs from each other. When changing to another address, several invalid states occur until the new address is valid. In the worst case, this can take a few nanoseconds. By slowing down the rise time of the line driver, the invalid states represent faster signals than the bandwidth of the driver allows to process. Consequently, the slow drivers hinder the decoder to select wrong rows and, by this means, avoid disturbing the self-calibration.

4.3.3 Averaging control

Beside the address decoders for sensor row and column, an additional decoder for selecting the number of averaged pixels is required. It has to control the horizontal and vertical averaging signals AVHOR and AVVER introduced in figure 3.10. Figure 4.19 shows the first eleven cells of the implemented averaging decoder. It is explained by means of the horizontal version which in prinicpal is the same as the vertical one except for the higher number of output lines.

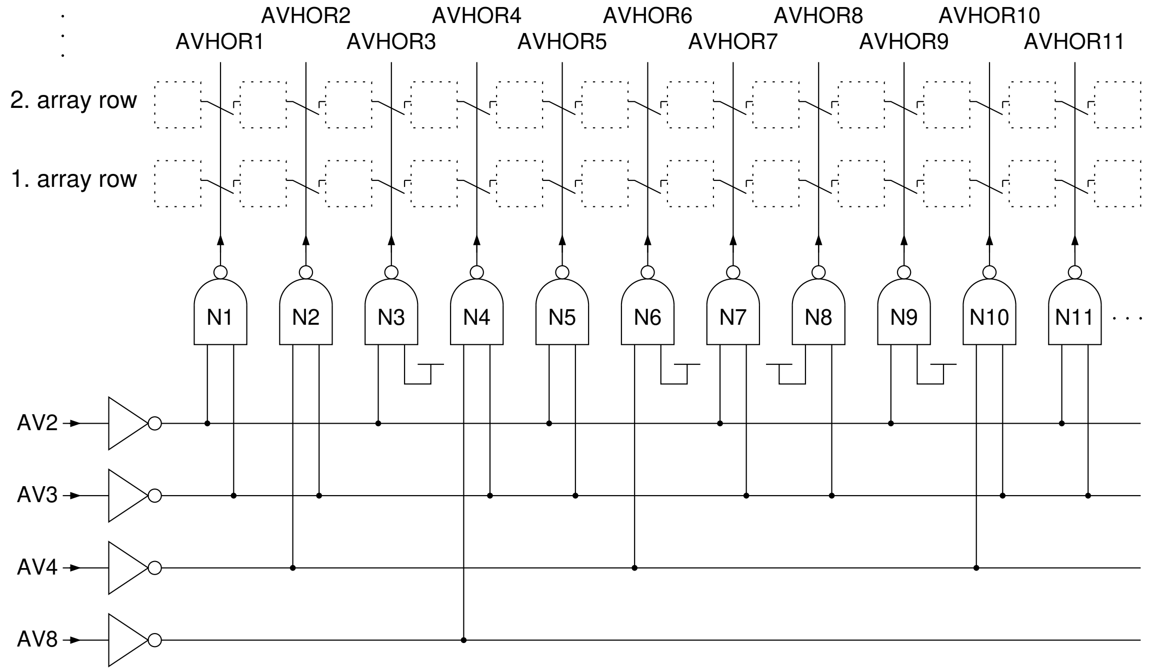


Figure 4.19: Part of the circuit diagram showing the horizontal averaging decoder. Two rows of the sensor array are additionally indicated at the upper border.

Each output line is driven by a nand-gate with two inputs. As long as both inputs are high (i.e. the four control lines AV2, AV3, AV4 and AV8 are set to low), the output is low and the averaging switches between the pixel diodes are open. By applying different combinations of high and low input signals, the nand-gates connected to the according control lines change their state. To keep the symmetric structure, a nand-gate is used even in the case that only one control line determines the output level. If so (e.g. gate N3), the second input of the gate is fixed to V_{dd}. Altogether, six different output patterns can be generated corresponding to the averaging of 1, 2, 3, 4, 6 and 8 pixels. They are summarized in table 4.1. The complete decoder is composed of smaller blocks of 24 cells each. Since 24 is the least common multiple of the possible numbers of averaged pixels, the output pattern repeats every 24 cells.

number of averaged pixels	AV2	AV3	AV4	AV8	nand-gates corresponding to the activated outputs
1	L	L	L	L	-
2	H	L	L	L	N1, N3, N5, ... N23
3	L	H	L	L	N1, N2, N4, N5, ... N22, N23
4	H	L	H	L	N1 - N3, N5 - N7, ... N21 - N23
6	H	H	L	L	N1 - N5, N7 - N11, ... N19 - N23
8	H	L	H	H	N1 - N7, N9 - N15, N17 - N23

Table 4.1: Required levels of the decoder input signals to obtain the six different averaging modes.

The control lines for the vertical and horizontal averaging decoder can be set independantly. Therefore, it is possible to choose a different vertical averaging pattern than the horizontal one. During the horizontal averaging, not only the photoreceptor diodes but also the vertical readout lines are connected. This results in a smaller remaining fixed pattern noise because the individual output offsets are reduced by averaging. Unfortunately, the connecting of the output lines is not possible in the case of vertical averaging. Here, two or more buffer transistors would have to share the same bias current leading to a significant shift of the voltage level. Hence, vertical averaged pixels show a higher fixed pattern noise than horizontally averaged ones.

4.4 Signal multiplexing and amplification

When selecting one pixel row for readout, all photoreceptor outputs of this row are guided to the lower array border at the same time. Since it makes little sense to drive about 400 lines off-chip, the individual column signals have to be multiplexed to a lower number of output lines. The presented image sensor provides one single analog output. For a short time each pixel output determines the level of the output line. The time corresponding to one pixel is calculated by dividing the time of one frame by the total number of pixels. Assuming a frame rate of 50 Hz (European video standard) and a number of 100k pixels results in 200 ns per pixel. This is equal to a pixel rate of 5 MHz. However, due to the video synchronisation signals, only a definite percentage of the frame time can be used for pixel readout. The final pixel rate therefore amounts to 7.4 MHz.

4.4.1 Multiplexing concept to avoid column fixed pattern noise

Unfortunately, the pixel source follower is not strong enough to charge the parasitic capacitance of the analog output line in the required time of less than 200 ns. In order to achieve such a performance, wider transistors (i.e. higher transconductance g_m) and higher currents would have to be used resulting in larger pixels and a very high power consumption. Therefore, the simple multiplexing concept of using one switch per column and connecting all column outputs to one horizontal readout line one after another does not work. Instead, the pixel outputs have to be buffered again at the end of each column. Then, the amplified signals are multiplexed to the single readout line.

Using one additional amplifier per column, however, will introduce a further contribution to the column fixed pattern noise. Due to the transistor mismatch each amplifier shows a different offset. To avoid the resulting column-to-column variations an offset cancellation method has to be applied. The developed and implemented solution, which in principal carries out a kind of correlated double sampling, can be seen in figure 4.20. It includes the multiplexing circuits of two array columns (column n and m, where n and m are integers out of 0 ... 385) and the offset-correcting readout amplifier.

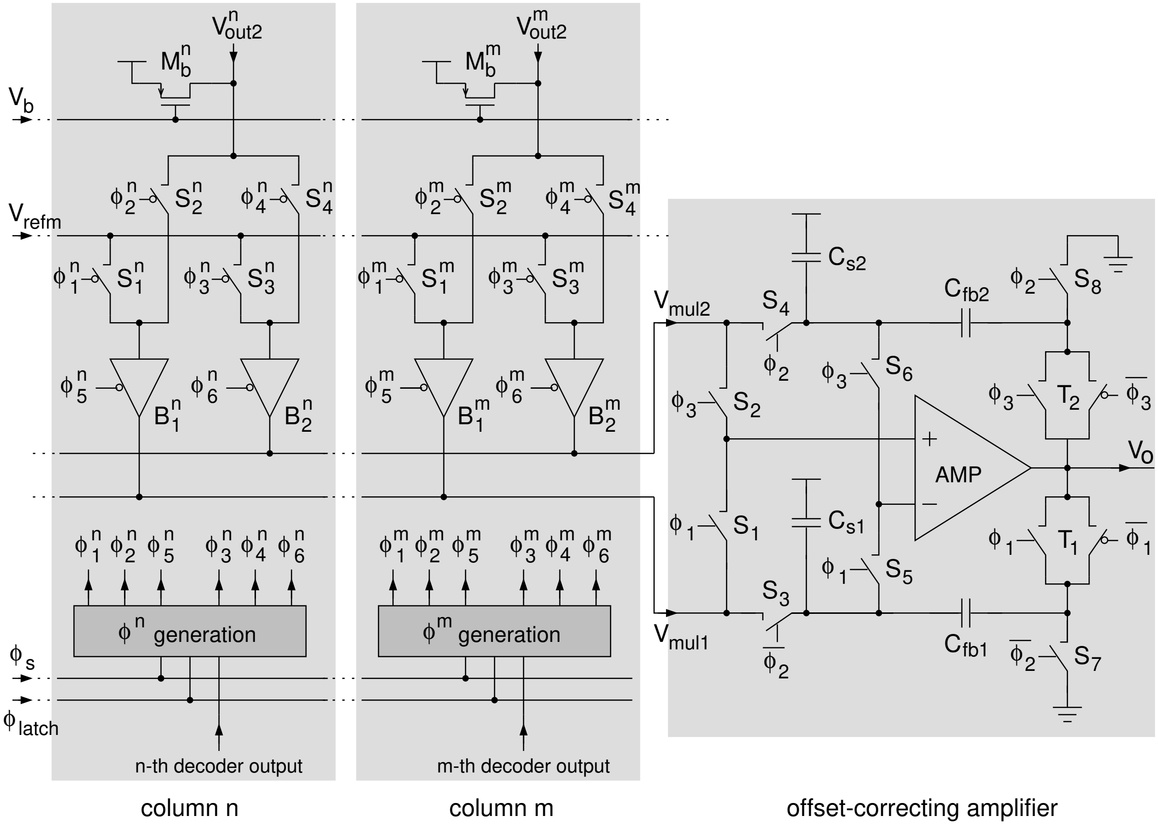


Figure 4.20: Column multiplexing concept including column signal buffering and offset cancellation.

Basically, the readout circuit operates as follows: At first, the n-th column output V^n_{out2} is buffered by the amplifier B^n_1 and guided to the horizontal readout line V_{mul1}. The voltage level of this line is stored on the capacitors C_{s1} and C_{fb1}. The next step enables the reference voltage V_{refm} (which must not be mistaken for the pixel reference voltage V_{ref}). It is also buffered by B^n_1 determining the potential V_{mul1}. Finally the previously stored column voltage V^n_{out2} is substracted from the reference voltage by the readout amplifier AMP annihilating any possible offset of the column buffer B^n_1. At the same time another pixel can be read out via the second multiplexer line V_{mul2}. This is done using the second buffer B^m_2 (in case of the m-th column) and the upper capacitances C_{s2} and C_{fb2}. By this means the multiplexer frequency is halfed resulting in less power consumption due to reduced transistor geometries (less parasitic capacitance) and smaller currents. In addition, the required readout amplifier bandwidth is reduced. The transistors M_b^n and M_b^m represent the load resistances for the buffer transistors in each pixel. They have the large channel dimensions of $W = 20\,\mu$m and $L = 5\,\mu$m leading to a low contribution to the column fixed pattern noise. All switches shown in the diagram represent single MOS transistors. The NMOS devices are drawn as active-high switches (no circle), the PMOS devices as active-low switches (small circle at the control input).

The exacting functionality of the multiplexer is explained with the help of figure 4.21. It shows the clocking scheme for the amplifier clocks ϕ_1, ϕ_2, $\overline{\phi_2}$ and ϕ_3 and for the clocks ϕ^n and ϕ^m of column n and m, respectively. Assume, that the two columns n and m have to be read out. The readout cycle starts by pulling ϕ_1 low and $\overline{\phi_2}$ high. This closes the switches S_3 and S_7 and opens the switches S_1, S_5 and the transmission gate[8] T_1. The transmission gate is used so as not to be restricted by the voltage range of a single switch but to take advantage of the full amplifier output swing.

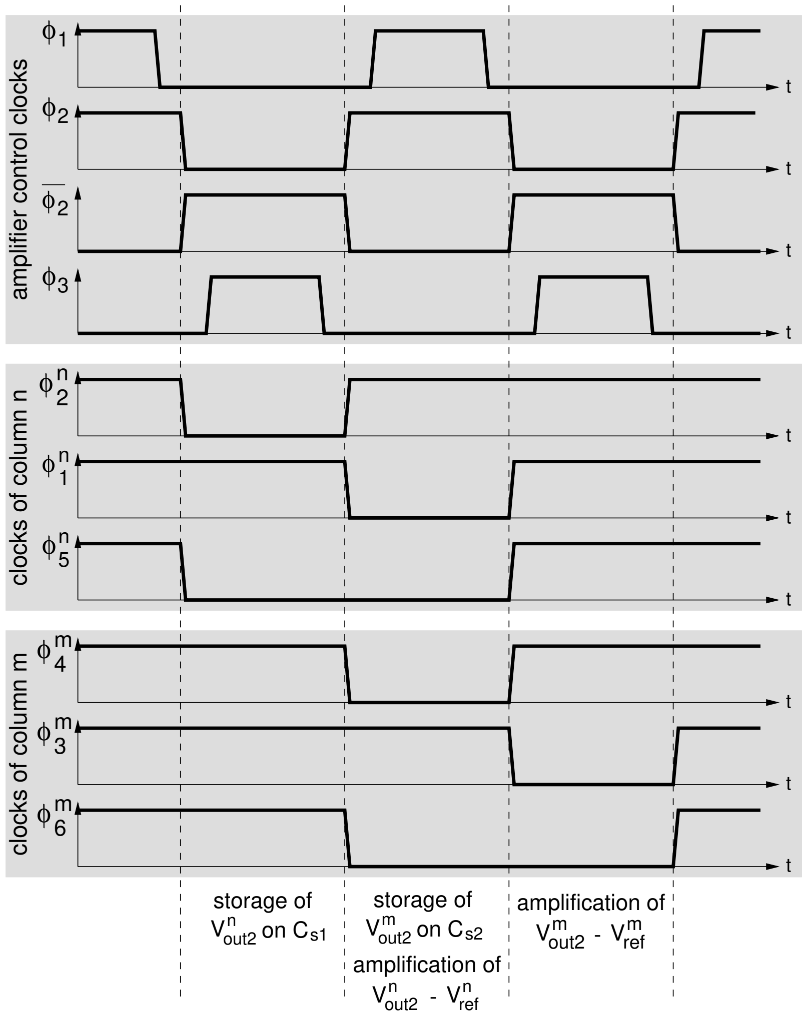


Figure 4.21: Clocking scheme for the readout of the two columns n and m.

[8] A transmission gate consists of two complementary MOS transistors to allow the switched voltage signals to cover the whole range from V_{dd} to ground.

At the same time S_2^n is switched on by the column clock ϕ_2^n going low (active-low switch!) and the output signal of the n-th column V_{out2}^n is connected to the buffer B_1^n. In addition, B_1^n is enabled by pulling ϕ_5^n low. The output of B_1^n determines the potential V_{mul1} of the first horizontal readout line. It is connected by S_3 to the storage capacitor C_{s1} and the feedback capacitor C_{fb1}. The other node of C_{fb1} is fixed to ground by the switch S_7. After a definite time given by the product of the buffer output resistance including all switches and the storage capacitance, C_{s1} and C_{fb1} are charged to the voltage V_{mul1}.

Next, $\overline{\phi_2}$ goes low and switches off S_3 and S_7. This means that the voltage V_{mul1} is held on C_{s1}. Besides, the input of the buffer B_1^n changes to the reference voltage V_{refm} due to a high ϕ_2^n and a low ϕ_1^n. At the same time, the next column m is prepared for readout. The column output V_{out2}^m is connected to the buffer B_2^m due to a low ϕ_4^m. As ϕ_2 goes high, the switches S_4 and S_8 are closed and B_2^m charges the capacitors C_{s2} and C_{fb2} to the voltage V_{mul2}.

In order to avoid that T_1 and S_7 both are switched on resulting in a short circuit between the amplifier output and ground, ϕ_1 is pulled up a little later to enable S_1, S_5 and T_1. Now, the voltage V_{mul1}, corresponding to the reference voltage V_{refm} buffered by B_1^n, is fed to the positive input of the readout amplifier. The amplifier's negative input is determined by the common node of C_{s1} and C_{fb1}. Since the other node of C_{fb1} is now driven by the amplifier output V_o, a feedback loop through the capacitive divider composed of C_{s1} and C_{fb1} is obtained. The closed loop gain of this configuration is given by

$$A_f = \frac{V_o}{V_i} = 1 + \frac{C_{s1}}{C_{fb1}} \tag{4.1}$$

where V_i is the input signal difference [ISM94]. Assuming that the reference voltage V_{refm} is higher than the photoreceptor voltage, V_{out2}^n results in a positive voltage between the positive and the negative amplifier input. Because an amplifier with negative feedback always tries to minimize the input difference, the output V_o increases until both inputs are more or less equal. If the initial difference between V_{refm} and V_{out2}^n is large, the output has to increase by a higher magnitude compared to a smaller initial difference. Consequently, using equation 4.1 the amplifier output V_o can be written as

$$V_o = \left(1 + \frac{C_{s1}}{C_{fb1}}\right) V_i = \left(1 + \frac{C_{s1}}{C_{fb1}}\right) (V_{refm} - V_{out2}^n)\,. \tag{4.2}$$

Two remarks should be mentioned concerning this result. The first comment refers to the negative sign of V_{out2}^n. Since the output voltage is inversely proportional to the input voltage, the intrinsic negative slope of the photoreceptor signal is converted into a positive slope. Brighter pixels are now represented by higher voltages which corresponds to the common video standards. The second comment is on the possibility to influence the output signal by changing V_{refm} or one of the capacitors C_{s1} or C_{fb1}. V_{refm} determines the offset and C_{fb1} the gain. By adjusting these parameters any voltage range can be covered by the output signal.

At the end of this cycle the buffer B_1^n is disabled by pulling ϕ_5^n high and the multiplexer line V_{mul1} can be used by another column buffer. Besides, the second readout part of the m-th column starts. The voltage V_{mul2}, corresponding to the receptor output V_{out2}^m, is stored on C_{s2} and C_{fb2} by opening the switches S_4 and S_8. The reference voltage V_{refm} is buffered by B_2^m and fed to the positive amplifier input, whereas the negative input is determined by the common node of the two capacitors C_{s2} and C_{fb2}. This represents the same situation as the previous readout of column n and thus ends up with the same relation between input and output voltage (equation 4.2). However, a good matching between the corresponding capacitances is required to avoid additional gain variations in every second column.

The method of taking the difference between the actual signal and a reference signal both amplified by the same buffer results in an elimination of any offset introduced by the buffer itself. However, the design and layout of all complementing structures, the switches in particular, has to be done very carefully to avoid other mismatch sources like charge injection variations. The two main building blocks of the diagram in figure 4.20 (column part and readout amplifier) are explained more in detail in the next two sections. Besides, the way how to generate the three non-overlapping clocks ϕ_1, ϕ_2 and ϕ_3 will be presented.

4.4.2 Column readout cell

Figure 4.22 shows the column part of the output multiplexer. One cell including the clock generation and the two output buffers are presented. The upper index n or m of the clock and switch identifiers indicating the column number is omitted as only one column is regarded. The buffers are implemented as source followers being composed of the transistors M_1 and M_2 in the column cell and the bias transistors M_{bs1} and M_{bs2} outside the cell at the end of the multiplexer row. The latter transistors are required only once since they are shared with all column cells.

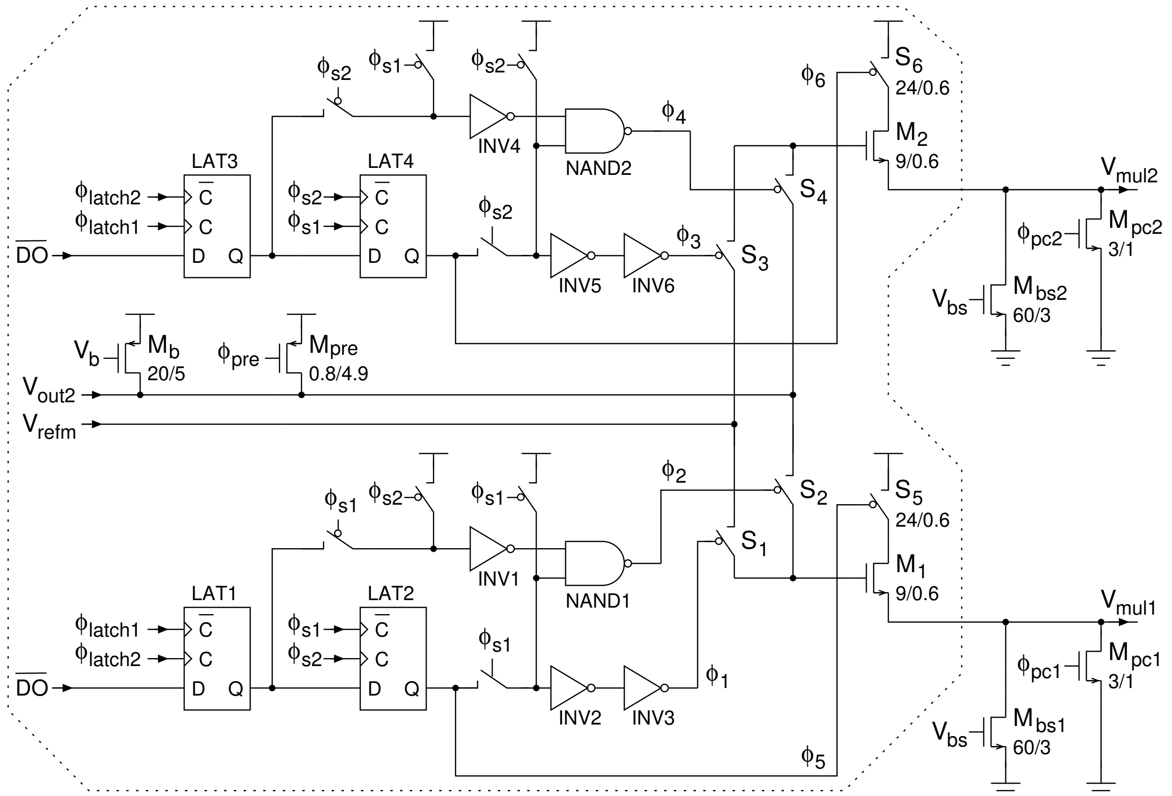


Figure 4.22: Circuit diagram of the column readout cell for the horizontal signal multiplexing.

The transistors M_{pc1} and M_{pc2} are responsible for the precharge of the multiplexer readout lines. When activated, they pull the corresponding line potential down to reach a level below the lowest readout value. In principle, the reason for precharging is the same as in the case of the reference current line for the photoreceptor calibration (cf. section 3.1.4). Due to the fixed current of the bias transistors M_{bs}, the decrease of the line potential occurs with a constant speed of $\frac{dV}{dt} = I/C$. The increase, however, is determined by the transconductance g_m of the buffer transistors M_1 and

M_2 resulting in a varying current depending on the gate-source-voltage. Since higher gate-source-voltages lead to increased currents, the settling time is shortened. Hence, the principal behaviour shown in the figures 3.5 and 3.6 with a long settling time for decreasing and a short settling time for increasing voltages also applies, if strong inversion source followers are used. Consequently, the precharge mechanism speeds up the buffer stage. It is carried out by pulling high ϕ_{pc1} and ϕ_{pc2} for a short time before every new readout cycle. The required clock pulses are generated by a monoflop. It uses the logic nor-operation to compare a clock signal with its inverse signal delayed by a cascade of inverters. Every falling edge, the two nor-inputs both are low for the time of the signal delay and the output produces a corresponding active-high clock pulse. The chosen pulse width of the integrated monoflop is about 6 ns.

The same precharge method is also applied to the pixel readout source follower. The according transistor M_{pre} as well as the bias transistor M_b providing the buffer current are located in the multiplexer column cell. Here, the precharge time determined by the clock ϕ_{pre} is not fixed but can be adjusted in the digital control part. The switches S_1 to S_6 shown in the right part of figure 4.22 are identical with the switches S_1 to S_4 and the switches of the two controllable buffers B_1 and B_2 of one column in figure 4.20.

In the following, the clock generation of ϕ_1, ϕ_2 and ϕ_5 controlling the lower readout line V_{mul1} is explained. The upper clock generator responsible for the line V_{mul2} shows the same functionality but is triggered by the opposite input clock edges of ϕ_{latch} and ϕ_s. This results from the permutation of ϕ_{latch1} and ϕ_{latch2} and the permutation of ϕ_{s1} and ϕ_{s2} in the upper and lower clock circuits. As a consequence, the first or second readout line, respectively, is selected by applying a rising or a falling clock edge of ϕ_{latch} and ϕ_s.

At first, the active-low decoder output $\overline{\text{DO}}$ is fed to the data input node D of the latch LAT1. As long as ϕ_{latch1} is low, the latch output Q follows the input signal. The latch is in the *transparent* mode. When ϕ_{latch1} goes high, the latch changes to the *storage* mode keeping the current output level independent of input signal behaviour. The implemented latch circuit consisting of six MOS transistors is shown in figure 4.23. The transistors M_1 and M_2 represent switches whereas the residual four transistors form the inverters INV1 and INV2. The non-overlapping clocking-scheme which is required for the latch control can be seen in figure 4.24. It prevents M_1 and M_2 from being switched on at the same time in order to avoid a short circuit between the input signal IN and the output signal OUT of the second inverter stage. The active-low clocks ϕ_c and $\phi_{\overline{c}}$ are generated in the same way as the non-overlapping calibration amplifier clocks $\overline{\phi_1}$ and $\overline{\phi_2}$ in figure 4.12. If ϕ_c is high and $\phi_{\overline{c}}$ is low, the PMOS switch M_2 is open and M_1 is closed. The input signal is connected to the first inverter and

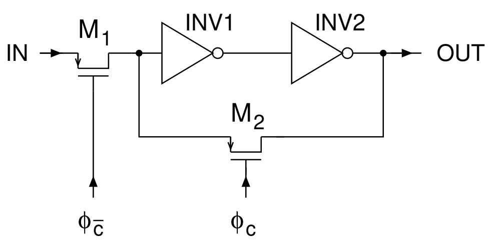


Figure 4.23: Static CMOS latch composed of two inverters and two switch transistors.

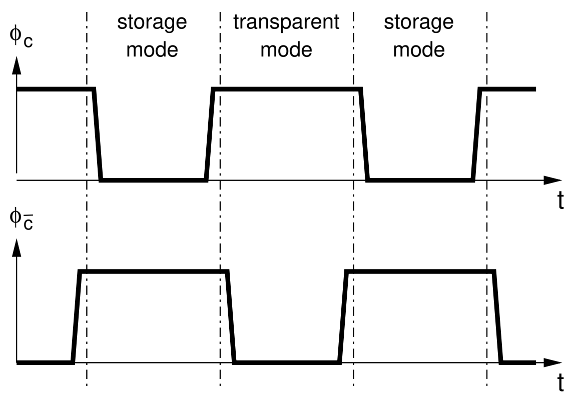


Figure 4.24: Non-overlapping active-low two phase clocks controlling the latch.

the output signal after two inverters equals the input level (transparent mode). Closing switch M_2 and switching off M_1 feeds back the output signal to the first inverter input and fixes the latch in its current state (storage mode).

Assuming that the shown column cell in figure 4.22 is selected by a low decoder output $\overline{\text{DO}}$ gives a low level at the latch output Q. As soon as the clock ϕ_{s1} goes low, the latch LAT2 becomes transparent. The clock signal ϕ_5 goes low and enables the readout buffer by closing switch S_5. Besides, the output signal of LAT1 is fed to the inverter INV1 converting it into a high signal level at the input of NAND1. Since the second nand input is also pulled up during this clock phase, the output ϕ_2 goes low. It switches on S_2 and connects the column output voltage V_{out2} to the buffer transistor M_1. When ϕ_{s1} goes high again (and ϕ_{s2} low), the low output signal level of LAT1 is stored in latch LAT2. Buffered by the two inverters INV1 and INV2, it closes the switch S_1 by pulling ϕ_1 low and connects V_{refm} to the buffer transistor M_1. At the same time the input of INV1 is pulled up resulting in a high level at the output of NAND1. This means that S_2 is switched off. The readout buffer is still active due to a high ϕ_5.

Before ϕ_{s1} changes its level again, the column decoder has selected the next column. Therefore, $\overline{\text{DO}}$ is back at the high signal level. When LAT2 becomes transparent by a low ϕ_{s1}, ϕ_5 as well as ϕ_1 are pulled up switching off S_5 and S_1. This corresponds to the initial state where all switches are off. The readout cycle is finished.

4.4.3 Multiplexer readout amplifier and gain adjustment

Amplifier description

The differential readout amplifier indicated as AMP in figure 4.20 has been designed as a two-stage operational amplifier with additional output stage. Figure 4.25 shows the corresponding circuit diagram. Again, the transistor dimensions are written below every identifier M. The input stage consisting of the differential PMOS-transistor pair M_3 and M_4 and the NMOS current mirror M_1 and M_2 amplifies the difference between the positive input INP and the negative input INN. The use of a PMOS input stage makes it possible to handle input voltages down to the ground level and up to about 3.5 V (with a 5 V voltage supply). The lower voltage margin is more important because the column buffers of the multiplexer shift the output voltage by more than V_T towards ground. The current of the first stage is provided by the transistor M_5. It is controlled by the bias voltage V_{b1} allowing to change the amplifier speed.

The second stage represents an inverting amplifier composed of the load transistor M_7 and the amplifying transistor M_6. For frequency compensation the capacitor C_c has been implemented. Due to the Miller effect, its capacitance is multiplied by the gain of the second stage resulting in a high output load of the first stage. The resistor R_c compensates for the feed forward path through C_c [ALL87-2] essentially influencing the stability behaviour. C_c is integrated as a metal-metal-poly sandwich capacitor with 700 fF leading to a linear charge-voltage relation over the whole voltage range. Besides, no minimum voltage between the two capacitor nodes is required in contrast to the use of a MOS capacitor. R_c amounts to 7 kΩ and is realized as a poly resistor.

In order to drive large output loads, an output buffer is added to the amplifier. The main transistors M_{13} and M_{14} form a class AB[9] push-pull amplifier which is driven by the two source follower stages M_8, M_9 and M_{11} and M_{12}. The source followers perform a voltage shift which goes in the upper

[9] The class of an output stage defines the ratio of the usable output power to the total power consumption of the stage. Class AB represents a tradeoff between class A (high quiescent current = high power consumption) and class B (very small quiescent current, but high signal distortions) with a reasonable intrinsic power consumption and small signal distortions [HIN95-1, TIE93].

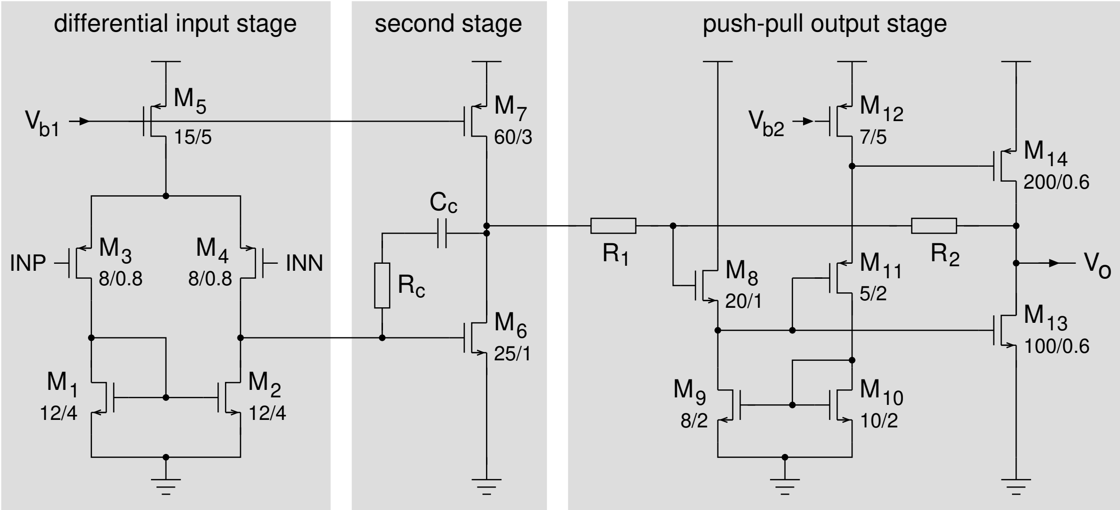


Figure 4.25: Circuit diagram of the readout amplifier carrying out the offset cancellation of the multiplexer column buffers (cf. figure 4.20).

direction in case of the PMOS stage and in the lower direction for the NMOS stage. The result is a gate voltage difference of about two times the threshold voltage V_T between the gates of M_{13} and M_{14} limiting the quiescent current. Transistor M_{12} which is controlled by the bias voltage V_{b2} generates the current for the PMOS source follower. It is mirrored by M_{10} and M_9 into the neighbouring path to provide the NMOS source follower. Changing the current by adjusting the voltage V_{b2} also results in a change of the quiescent current in the output stage. A higher source follower current increases the voltage difference between the two output gates and thus decreases the output quiescent current. A lower source follower current causes the opposite effect.

The resistors R_1 and R_2 represent a feedback between output and input of the third stage. This causes a decrease of the output resistance making the amplifier capable of driving higher loads. R_1 and R_2 are implemented as nwell-resistors with 72 and 111 kΩ, respectively. In contrast to poly-resistors, nwell-devices have a much higher resistance per square allowing to build relatively small sized, high ohmic resistors [AMS98-2].

Adjustable gain

As seen in equation 4.1, the closed loop gain of the readout amplifier integrated in the capacitive feedback of figure 4.20 is determined by the capacitances C_s and C_{fb}. The numbers 1 and 2, indicating the lower and upper signal path, are omitted since the following remarks apply to both cases. The storage capacitor C_s consists of a PMOS transistor with a gate-channel-capacitance of 2 pF. Its size is fixed. The feedback capacitor C_{fb} cannot be realized as transistor since the required voltage difference of V_T between channel and gate is not guaranteed. It therefore consists of a metal-metal-poly sandwich capacitance.

In order to obtain the possibility of adjusting the gain during the image sensor operation, the capacitor C_{fb} is composed of several subparts. By enabling or disabling these individual parts, the overall capacitance of C_{fb} can be controlled. The total number of sub-capacitors is eight whereof seven are selectable and one is fixed (offset value). Since the magnitude of the selectable devices increases from one capacitor to the next by a factor of two, $2^7 = 128$ different values can be chosen. The individual subparts of C_{fb} and the resulting gain with respect to equation 4.1 are summarized in table 4.2. Although C_{fb} can be linearly adjusted, the corresponding gain varies in a hyperbolic way. This is caused by the fact that the capacitance C_{fb} belongs to the denominator of equation 4.1. Because all the sub-capacitors of C_{fb} are needed twice (upper and lower signal path), a good matching of the individual devices is required. It can be achieved by a proper layout of the corresponding structures.

subpart	C_{off}	C_1	C_2	C_3	C_4	C_5	C_6	C_7
capacitance [fF]	250	25	50	100	200	400	800	1600
gain ($C_{fb} = C_{off} + C_n$)	9.0	8.27	7.67	6.71	5.44	4.08	2.90	2.08

Table 4.2: The resulting amplifier gain in case of activating only one of the seven selectable sub-capacitors at a time. Additional gain factors can be achieved by using any combination of the seven subparts. The total capacitance of C_{fb} is always given by the sum of the offset capacitance C_{off} and the additionally selected capacitors.

4.4.4 Output mixer with sample-and-hold stage

The analog signal coming from the multiplexer amplifier output needs some time for settling after being connected to a new column. Therefore, a sample and hold stage follows the amplifier. It samples the signal after the settling time has passed and holds it during the settling time of the next pixel. By this means, a continuous analog output signal is obtained. The circuit diagram of the sample-and-hold stage and the output mixer and limiter for generating the composite video signal are shown in figure 4.26. In addition, the video output amplifier, which is capable of directly driving a 75 Ω video input, can be seen.

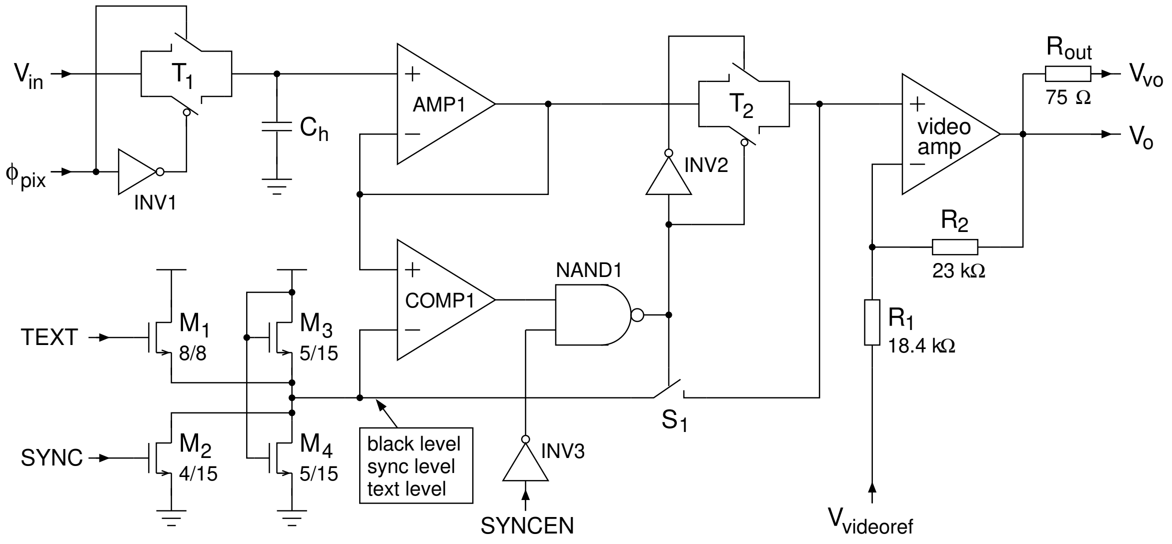


Figure 4.26: Circuit diagram of the output sample-and-hold stage and the mixer combining video synchronisation, on-screen text and analog pixel output.

The sample-and-hold stage consists of the transmission gate T_1, the hold capacitor C_h and the buffer AMP1. As long as the pixel clock ϕ_{pix} is high, T_1 is enabled and the buffer output follows the input signal V_{in}. When ϕ_{pix} goes low, the transmission gate isolates the positive buffer input and the current voltage level is held on C_h. To reduce the charge injection effect of T_1, C_h has been implemented with the relatively large capacitance of 5 pF. The amplifier AMP1 belongs to the analog standard cell library provided by the company AMS. The datasheet can be found in [AMS98-3]. Slight changes of the design have been carried out in order to adapt the circuit to the given requirements. Since no second poly layer should be used, the poly-poly compensation capacitor has been replaced by a metal-metal-poly sandwich capacitor. Also the frequency behaviour has been tuned by adjusting the amplifier current.

Leaving the first amplifier, the analog signal next passes the transmission gate T_2 and is finally amplified by the video buffer. This buffer is integrated with a resistive feedback (resistors R_1 and R_2) leading to a gain of $1 + R_2/R_1 = 2.25$. The video amplifier output can be used with or without 75 Ω termination. The latter case provides the low output resistance of the amplifier and the full output voltage but no adaptation of the output impedance to the input impedance of the following device (cable, ADC, etc.). The former case allows adapting the chip output to a 75 Ω coaxial cable and thus prevents signal reflections at the chip-cable-connection. Since the other end of the cable is also terminated with 75 Ω, the voltage level of the output signal is halved. The absolute level of the output voltage can be adjusted by the reference voltage $V_{videoref}$.

The remaining parts of figure 4.26 are responsible for mixing the analog pixel values and the synchronisation signals required for the composite video signal. Besides, a limiter (COMP1) to prevent the image sensor signal from falling below the black level is implemented. Otherwise, dark pixels could disturb the synchronisation as they are regarded as negative synchronisation pulses. Figure 4.27 shows the behaviour of the analog output signal behind the video amplifier. It corresponds to the CCIR[10] video standard which is wide spread in Europe. The digital control signals SYNCEN, SYNC and TEXT as well as the output COMPOUT of the limiting comparator COMP1 are plotted

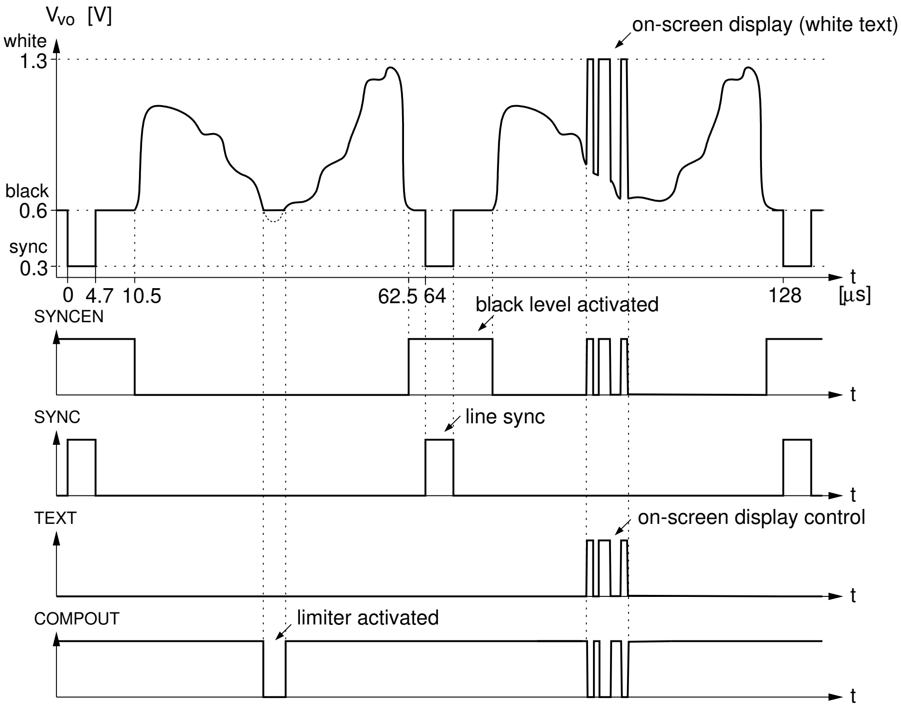


Figure 4.27: Timing of the composite video signal (CCIR) and control signals of the output mixer stage. Two complete video lines are shown.

[10] CCIR means Consultative Committee of International Radio

below the analog signal. Except for COMPOUT, they are generated by the digital control logic which has to take care of the right timing.

As long as SYNC and TEXT are low, the transistors M_1 and M_2 are deactivated. Due to the voltage divider of M_3 and M_4 a definite potential arises at the common node corresponding to the black level of the video signal. When SYNCEN goes high, the nand-gate NAND1 pulls high its output. This closes the switch S_1 and opens the transmission gate T_2. The input of the video amplifier is now determined by the black level of M_3 and M_4. The sync-signal to indicate the start of a new line is generated by pulling SYNC high. Transistor M_2 is enabled resulting in a lower total resistance to ground, and the voltage drops to the sync level. Afterwards, SYNC goes low again and the black level is recovered.

During the readout of the pixel values, SYNCEN is low and allows the output signal of AMP1 to determine the input of the video amplifier through the transmission gate T_2. At one spot of the first video line in figure 4.27, this output voltage drops below the black level. This behaviour is detected by the comparator COMP1 which immediately forces its output to go low. As a consequence, the gate NAND1 opens T_2 and activates switch S_1 fixing the output voltage to the black level. By this means, no output level lower than the black reference can be reached beside the specially controlled sync level. The comparator consists of a differential input stage and a second inverting stage. Apart from the compensation path including C_c and R_c, the principal design is very similar to the first two stages of the readout amplifier in figure 4.25.

In order to be able to adjust some of the image sensor parameters without using an external digital control device (PC, microcontroller), a three button interface has been implemented. The buttons choose the desired parameter and allow increasing or decreasing the according value. The name of the selected parameter is displayed in the video image to simplify the orientation. This on-screen display requires a possibility to set the output voltage to a fixed bright value (white level). During the sensor readout, this level is enabled and disabled in a way, that the resulting pattern of bright (white level) and dark (pixel level) spots appears as the name of the selected parameter. The activation of the white level is controlled by the signal TEXT which switches the transistor M_1. The second video line in figure 4.27 gives an example of the on-screen display. Every time TEXT is high, the output signal rises to the white level. When TEXT goes low, the output returns to the image signal level.

4.4.5 Video amplifier

The amplifier indicated as video amp in figure 4.26 has to drive the video impedance of 75 Ω at a frequency of nearly 10 MHz. In order to obtain a reasonable settling time the unity gain bandwidth needs to be higher than 20 MHz. This means, that a high speed operational amplifier with a low output resistance is required. The developed design, whose circuit diagram is shown is figure 4.28, mainly follows the concept described in [MIL85]. It consists of an unbuffered amplifier with two stages and a push-pull output buffer. A power-down mode has been added allowing to completely switch off the amplifier. However, for the sake of simplification, the eight power-down transistors are omitted in the diagram.

The unbuffered first two stages (input part) are essentially a cascade of a differential-transconductance input stage and a current-amplifier second stage. The voltage gain is achieved by the high resistance node at the junction of M_8, M_{12}, M_{17} and M_{18}. All other nodes have a low impedance resulting in a good frequency response. The amplifier current is generated by the transistor M_{15}. It can be adjusted by the video bias voltage V_{vb} to influence the frequency behaviour and the power consumption.

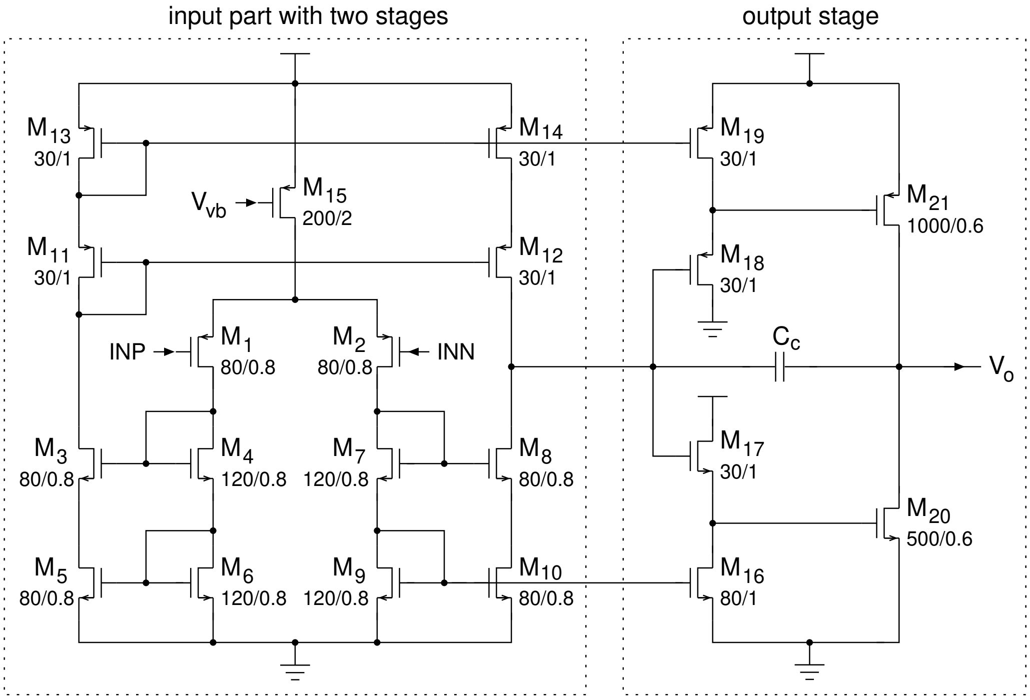


Figure 4.28: Circuit diagram of the video amplifier.

The output stage represents a class AB push-pull-buffer composed of the two source followers M_{16}, M_{17} and M_{18}, M_{19} and the output transistors M_{20} and M_{21}. The source followers are used to shift the input voltage in order to reduce the current through the output transistors. The capacitance C_c compensates the amplifier by introducing a dominant pole in the transfer function. It is integrated as a metal-metal-poly sandwich capacitor with about 2 pF. The small-signal output resistance of the buffer stage is mainly given by

$$r_{out} = \frac{1}{g_{m20} + g_{m21}} \tag{4.3}$$

where g_{m20} and g_{m21} are the transconductances of M_{20} and M_{21}. To reduce r_{out}, the output transistors have a large W/L ratio leading to a high g_m. The chosen channel dimensions result in an output resistance of less than 10 Ω.

The frequency response has been simulated for different output loads and different bias voltages V_{vb}. Figure 4.29 shows the results (Bode-plot) in case of $V_{vb} = 3.5$ V. The total amplifier current (disregarding the current required for the output load) amounts to 4 mA which means a power consumption of 20 mW due to the supply voltage of 5 V. The upper diagram includes the gain as a function of the frequency. It can be seen that the open loop gain at low frequencies is reduced if driving high resistive loads. The unity gain bandwidth is 45 MHz for resistive loads and 60 MHz for the pure capacitive load. The phase behaviour shown in the lower diagram gives a phase margin of more than 60° in case of the 75 Ω load, but only about 50° for the capacitive load of 50 pF.

A higher stability can be achieved by increasing the bias voltage V_{vb}. This leads to a smaller current in the first stage slowing it down and a higher current in the output path through M_{20} and M_{21}. Consequently, the unity gain bandwidth is reduced but the phase margin is increased. The simulation of the frequency response in figure 4.30 confirms the expected behaviour. The overall current is risen to 9 mA corresponding to a power consumption of 45 mW. The unity gain bandwidth has decreased to 21 and 29 MHz, respectively, but the phase margin in any case is above 70°. Depending on the application a faster, more unstable or a slower, more stable adjustment can be chosen. In the image sensor, the video amplifier has to manage two tasks: driving the video output line and driving the on-chip analog-to-digital converter. Since the first one represents a resistive load and the second one a capacitive load, both amplifier capabilities are required.

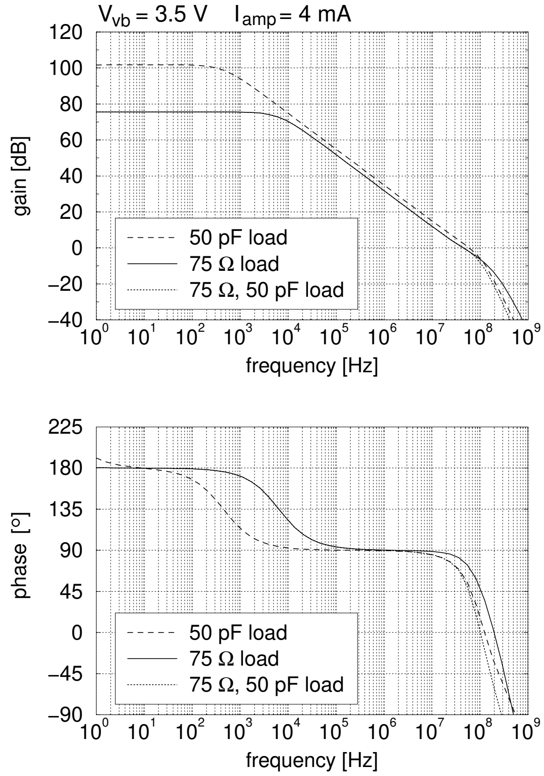


Figure 4.29: Simulated frequency response (Bode-plot) of the video amplifier with a bias voltage of $V_{vb} = 3.5$ V. The amplifier current without load is 4 mA resulting in a power consumption of 20 mW.

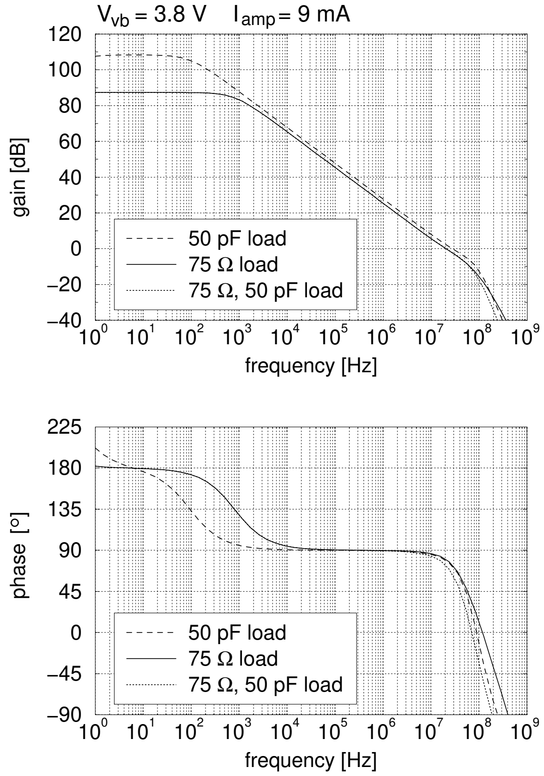


Figure 4.30: Simulated frequency response (Bode-plot) of the video amplifier with a bias voltage of $V_{vb} = 3.8$ V. The amplifier current without load is 9 mA resulting in a power consumption of 45 mW.

The layout of the video amplifier is shown in figure 4.31. The input and output lines as well as the main building blocks are indicated. Two properties are apparent: the large dimensions of all transistors and the dominating compensation capacitor which occupies nearly half of the area. The size of the amplifier layout is $314 \times 100\,\mu\text{m}^2$. The output line consists of a wide metal path in order to conduct the high output current of up to 30 mA (2 V at 75 Ω).

Two other output amplifiers are implemented in the image sensor providing additional possibilities. If only a lower buffer strength is needed, the overall power consumption can be reduced by deactivating the video amplifier. The analog output signal is then driven either by a simple source follower or by a weaker operational amplifier of the same type already applied for the sample-and-hold stage in figure 4.26. Both outputs are fed to separated pads and can be used in parallel.

4.4.6 Clock generation

The readout components (multiplexer, readout amplifier, mixer) described in the last sections need a number of different timing signals. Most of them are directly controlled by the digital logic part

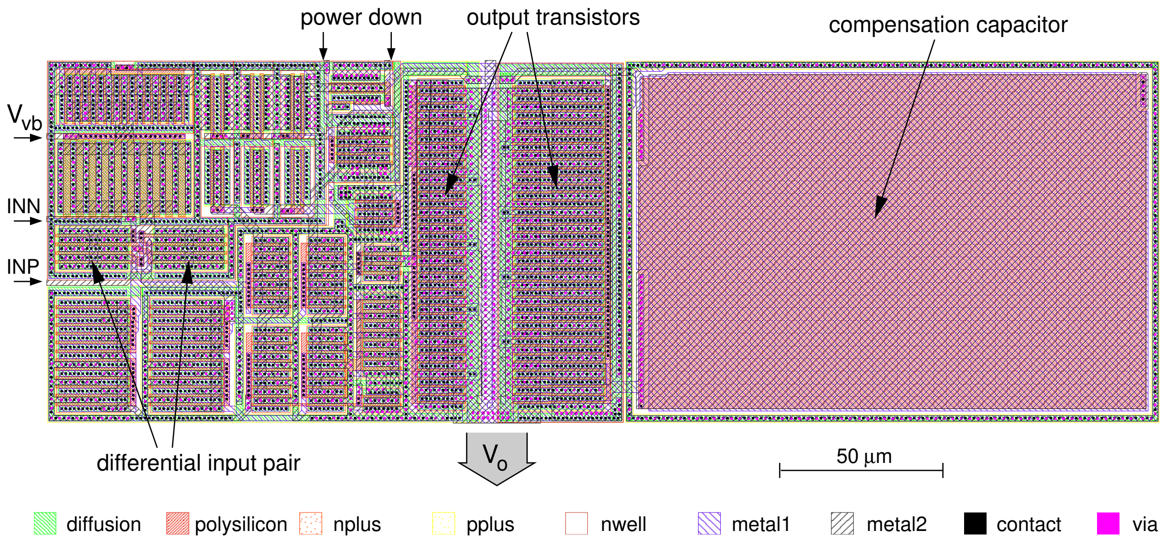


Figure 4.31: Layout of the video amplifier.

providing a high flexibility of changing the timing during operation. However, the non-overlapping three-phase clock required for the readout amplifier in figure 4.20 could not be realized with the synchronous digital design used for the control logic. Therefore an extra circuit generates the clock pattern shown in figure 4.21 for ϕ_1, ϕ_2, $\overline{\phi_2}$ and ϕ_3.

This clock generator, whose circuit diagram can be seen in figure 4.32, is stimulated by the single clock ϕ_{read}. Depending on the level of ϕ_{read} the first or second readout path (V_{mul1} or V_{mul2}) is used. Initially assuming a low ϕ_{read}, the clocks ϕ_1 and ϕ_2 also show a low, $\overline{\phi_2}$ and ϕ_3 a high level. When ϕ_{read} goes high, the gate NOR3 gets a high input and pulls its output down. At this point of time, NOR1 and NOR2 are not affected because they are kept in its state by the high signals $\overline{\phi_2}$ and ϕ_3. After a few moments, ϕ_3 goes down due to the change in NOR3. Now, NOR2 sees two low inputs and thus raises its output. This leads to a change of the clock signals ϕ_2 and $\overline{\phi_2}$. After $\overline{\phi_2}$ has gone low, NOR1 switches and pulls up ϕ_1. The described clock transition corresponds to the change from the first complete cycle to the second one in figure 4.21.

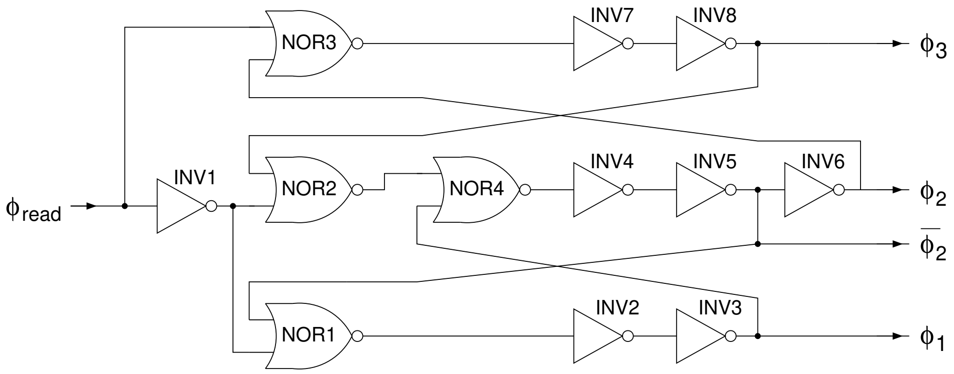


Figure 4.32: Generation of the 3-phase non-overlapping clock required for the multiplexing readout amplifier.

When ϕ_{read} goes low again, the transition repeats in the opposite direction. At first, ϕ_1 is pulled down. Next, ϕ_2 and $\overline{\phi_2}$ change their state and allow ϕ_3 to finally go high. The realization of the clock generator consists of a full custom design, i.e. all structures are designed according to the concrete requirements (timing, power consumption) without using digital standard cells.

4.5 Digital-to-analog converter for bias generation

The complete image sensor requires 19 different bias and control voltages. They are generated on the chip with the help of a DAC (digital-to-analog converter) and 19 sample-and-hold stages. By this means the chip performance can be individually tuned to either adapt it to the actual conditions or to compensate for the chip-to-chip variations of the process parameters. The DAC has a resolution of 8 bits allowing to adjust the output voltage in steps of 20 mV over a total range of 0 - 5 V.

4.5.1 Operation principle

The architecture of the bias generator is shown in figure 4.33. It is composed of the integrator stage converting a digital value into the corresponding analog voltage and the sample-and-hold output buffers. The output voltage of the integrator is determined by the integration current I_{int}, the capacitors C_{int} (integration capacitance) and C_{fb} (feedback capacitance) and the integration time. The current I_{int} is not generated on-chip, but has to be provided externally. This allows adjusting the resulting voltage range by selecting the corresponding integration current.

The operation principle works as follows: At first, the transmission gate T_0 is disabled and the RESET signal closes the switches S_{r1} and S_{r2}. The input node of C_{int} is fixed to ground, whereas the negative input node of AMP1 is pulled to the upper supply voltage V_{dd} (as long as S_{r2} is closed, the amplifier works as voltage follower forcing the negative input to show the same value as the positive input). When RESET goes low again, S_{r1} and S_{r2} are opened and the integration cycle starts by closing T_0. Charges accumulate on C_{int} according to the current I_{ref} and increase the potential at the input node. Due to the connection between C_{int} and C_{fb}, the potential of the common node (negative amplifier input) is also influenced and tries to rise. This, however, is prevented by the amplifier reducing its output voltage to compensate for the increasing input. Consequently, the longer the integration time, the lower the resulting output voltage.

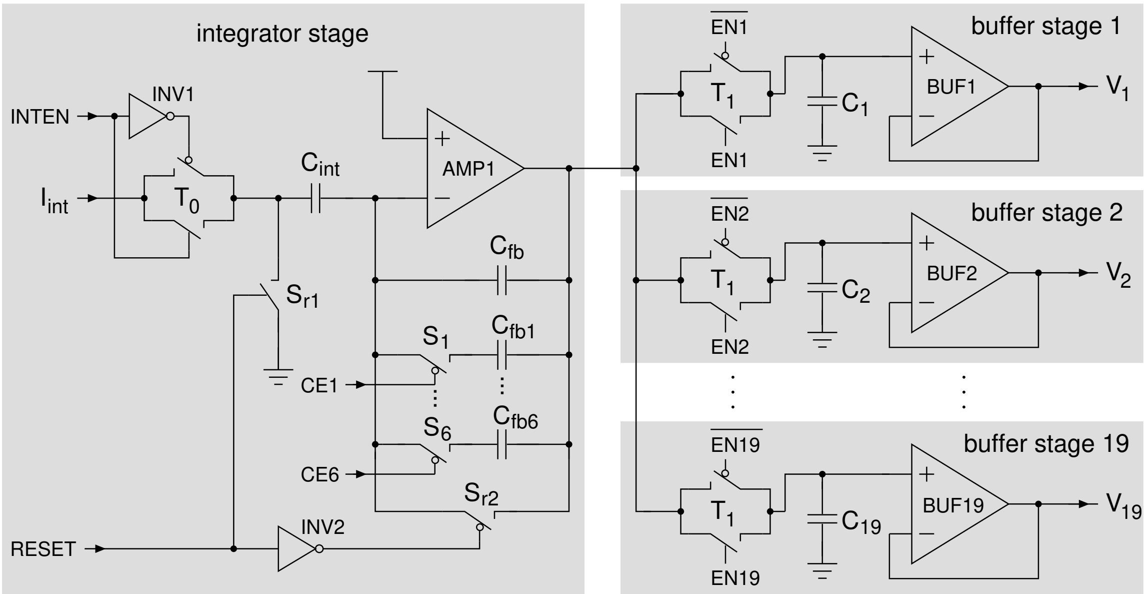


Figure 4.33: Architecture of the bias generator. It consists of the integrating stage working as digital-to-analog converter and 19 sample-and-hold output buffers.

The integration time is determined by the signal INTEN (integration enable) which controls the transmission gate T_0. A digital counter in the main control part simultaneously starts with INTEN going high and pulls INTEN low as soon as the digitally stored value for the corresponding bias voltage is reached. Afterwards, the integrator output is stored on the appropriate sample-and-hold stage by enabling one of the EN1 to EN19 signals. By this means, all 19 bias voltages are generated one after another. They are held in the storage capacitors C_1 - C_{19} until the next update occurs. Depending on the voltage values, the time between two updates amounts to some hundred microseconds to two milliseconds. Besides, the DAC control logic can be set to a mode in which the update is carried out only once per readout frame. This means an update rate of 50 Hz in video mode.

The capacitors C_{int} and C_{fb} determine the closed loop gain A_f of the integration amplifier AMP1. Since the input signal is coupled to the negative amplifier input, a negative voltage gain is achieved. Solving the voltage equations describing the feedback loop results in a gain of

$$A_f = -\frac{C_{int}}{C_{fb}}. \tag{4.4}$$

The dependence of the output voltage on the input current, the capacitances and the integration time therefore can be expressed as

$$V_o = V_{dd} - A_f V_i = V_{dd} - \frac{C_{int}}{C_{fb}} \frac{I_{int} T_{int}}{C_{int}} = V_{dd} - \frac{I_{int} T_{int}}{C_{fb}} \tag{4.5}$$

where $V_i = (I_{int} T_{int})/(C_{int})$ is the integration voltage corresponding to the integration time T_{int}. The output shows an offset of V_{dd} because it is charged to that value during the reset cycle. It is interesting that the output voltage does not depend on the integration capacitance C_{int}. The effect of a higher integration voltage if using a smaller C_{int} is completely cancelled by the lower gain of the subsequent amplifier and vice versa.

In order to get a possibility of adjusting the output range even if the external integration current is fixed, the capacitance C_{fb} can be varied by adding up to six capacitors C_{fb1} to C_{fb6}. Since the size always increases by a factor of two from one to the next, 32 different combinations are possible and can be selected by the signal CE1 to CE6 (capacitor enable). All capacitances of the integrator stage are realized as metal-metal-poly capacitors. The individual capacitor values are $C_{int} = 860$ fF, $C_{fb} = 215$ fF and $C_{fb1} \ldots C_{fb6} = 2.5, 5, 10, 20, 40, 80$ fF. Thus, the gain can be set to a number between 2.3 and 4. The integration capacitor therefore has to be maximally charged to less than half of the supply voltage. The obtained smaller voltage swing gives a better linearity since the current source generating I_{ref} is not ideal but shows a slight voltage dependence.

The hold capacitors C_1 to C_{19} are implemented as MOS transistors which offer a much higher capacitance per unit area. However, they need a voltage higher than the threshold voltage V_t to work properly. For this reason, a PMOS and an NMOS transistor with a capacitance of 1.7 pF each are used together in order to cover the full voltage range. Beside the capacitances, two amplifiers are required: one for the integrator (AMP1) and one as output buffer of the sample-and-hold stage (BUF1 ... BUF19). In both cases, the same operational amplifier design is used. It is described in the next section.

4.5.2 Rail-to-rail buffer

The buffer used for the bias generator outputs in figure 4.33 needs to have rail-to-rail[11] inputs and outputs in order to get bias voltages in the full supply range from ground to V_{dd}. Typical operational amplifiers like the calibration amplifier in figure 4.8 or the video amplifier in figure 4.28 usually

[11] Rail-to-rail means, that the signal (input or output) can cover the complete range from the lower supply voltage to the upper supply voltage.

possess a limited input range and therefore cannot be used. The input transistors require a minimum gate-source-voltage of V_T to be turned on. An NMOS differential stage operates only above an input voltage of 1 V, whereas a PMOS stage needs a voltage below $V_{dd} - 1$ V.

The solution implemented in the bias generator uses an NMOS and a PMOS differential input stage in parallel to overcome the limited input range of a single differential stage. Figure 4.34 shows the circuit diagram which basically follows the idea of [FER98]. The NMOS and PMOS stages are built up identically except for the mirrored potentials and opposite device types. Their functionality corresponds to that of the video amplifier input stage in figure 4.28. A difference exists in the integrated current mirrors which are cascode mirrors (two transistors in series per current path) in the case of the video amplifier and normal mirrors (only one transistor per current path) in the case of the currently described buffer. The consequence is a higher gain of the video amplifier due to the increased output resistance of the current mirror. In addition to the input stages, the described sample-and-hold buffer contains a class AB push-pull output buffer and three transistors for generating the bias currents.

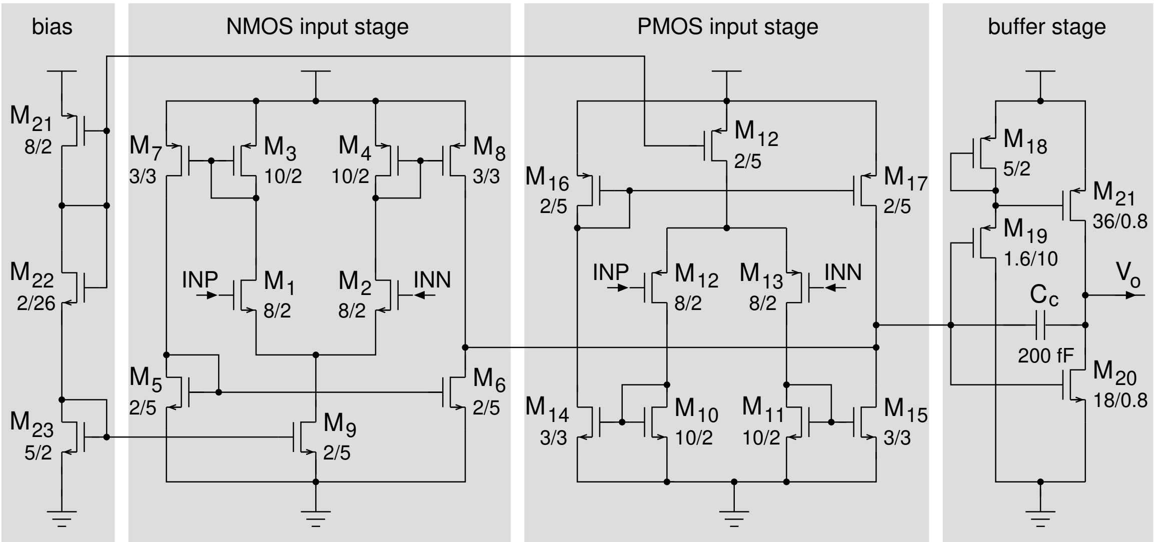


Figure 4.34: Circuit diagram of the rail-to-rail input and output operational amplifier used as integrator and as output buffer.

The behaviour of the input stages is explained by means of the NMOS version. It consists of the differential transistor pair M_1 and M_2 representing a transconductance amplifier. The currents are mirrored by the transistors M_3 to M_8 and converted back into a voltage at the common node of M_6 and M_8. Due to the high output resistances of these two transistors working as current sources, a high voltage gain is achieved. The same happens to the output node (common node of M_{15} and M_{17}) of the PMOS stage.

Both outputs are connected to each other to get one output voltage controlling the following buffer stage. In the middle range of the input voltages, the two differential stages work together determining the voltage at the common output node. If the input voltage drops below V_T, the transistors M_1 and M_2 are switched off and limit the current through M_6 and M_8 to a very low level. Therefore, the total amplification is carried out by the PMOS. If the input voltage becomes too high ($> V_{dd} - V_T$), the transistors M_{12} and M_{13} are switched off. In this case, the NMOS stage amplifies the input signal. Consequently, the complete buffer can process input signals in the range from the lower to the upper supply voltage.

The output stage includes the buffering transistors M_{20} and M_{21} and the source follower transistors M_{18} and M_{19}. The latter ones shift the gate voltage of M_{21} towards the upper supply voltage in order to reduce the quiescent current. The capacitance C_c enlarged by the Miller effect is responsible for the frequency compensation. It is implemented as a sandwich capacitor with about 200 fF. The layout of the complete amplifier occupies an area of $80 \times 80\ \mu\text{m}^2$. In addition to the circuit shown in figure 4.34, an output-disable mode is integrated. It can be used to switch off the output buffers in order to overwrite the DAC voltages by externally generated voltages.

The amplifier circuit has been simulated for typical process parameters with a capacitive output load of 5 pF. This load value corresponds to most of the input capacitances of the components provided with voltages from the bias generator. To examine the rail-to-rail behaviour, the absolute input voltage level has been set to three different values covering nearly the full range from ground to V_{dd}. The simulation results are presented in table 4.3.

input voltage [V]	quiescent current [μA]	open loop gain [dB]	unity gain bandw. [kHz]	phase margin
2.5	58	92	990	69°
0.4	64	91	250	81°
4.6	49	88	810	74°

Table 4.3: Simulated performance of the rail-to-rail amplifier at three different absolute input voltages.

It can be seen that the amplifier mainly keeps its high gain of 90 dB when reaching the border of the input range (input voltage 0.4 and 4.6 V). The unity gain bandwidth decreases from about 1 MHz for a medium voltage to 250 kHz for an input signal of 0.4 V. On the other hand, the phase margin increases resulting in a more stable system. The performance in any case is sufficient for the application as a static voltage buffer.

4.6 Digital control part

The largest building block beside the sensor array in the image sensor architecture of figure 4.2 is represented by the digital part. It is responsible for the control of all sensor components necessary to make the chip a completely autonomous system (camera on a chip). The logic has been realized by describing the abstract behaviour in the hardware description language *Verilog* [THO91] and subsequently converting the design into an electronical circuit consisting of digital standard cells. The latter step is done by the automatic synthesis tool *synergy* which is included in the *cadence design software* [CAD97]. The used standard cells belong to the library installation of the AMS 0.6 μm CMOS process and contain the basic digital functions like inverters, buffers, and-, or- and xor-gates, multiplexers, flip-flops and so on [AMS97].

The layout of the design is carried out by the automatic place-and-route tool of the cadence software. It arranges the individual cells in rows which are separated from each other by the routing channels for the interconnection lines. The applied routing software is capable of using all three metal layers resulting in relatively narrow and space-saving channels. In addition to the automatic routing, some lines are connected by hand. Especially the clock routing is very important to make sure that the clock signal always arrives before the data changes (i.e. low clock skew between individual cells). The complete digital design includes nearly 4000 standard cells corresponding to about 50000 transistors and occupies an area of $3.5 \times 1.1\ \text{mm}^2$.

4.6.1 Overview

The logic part of the image sensor is composed of several subparts. They are responsible for different controlling tasks but have to exchange data and clock signals. Figure 4.35 shows an overview of the complete digital part including the basic building blocks and their interconnections. Signals going outside (either off-chip or into the analog structures of the chip) are labelled. The whole design is synchronous to the main system clock of 14.7 MHz except for the interface logic. Slower clock signals required for the generation of the DAC signals and the EEPROM control part are derived from the main clock and thus keep the design synchronous.

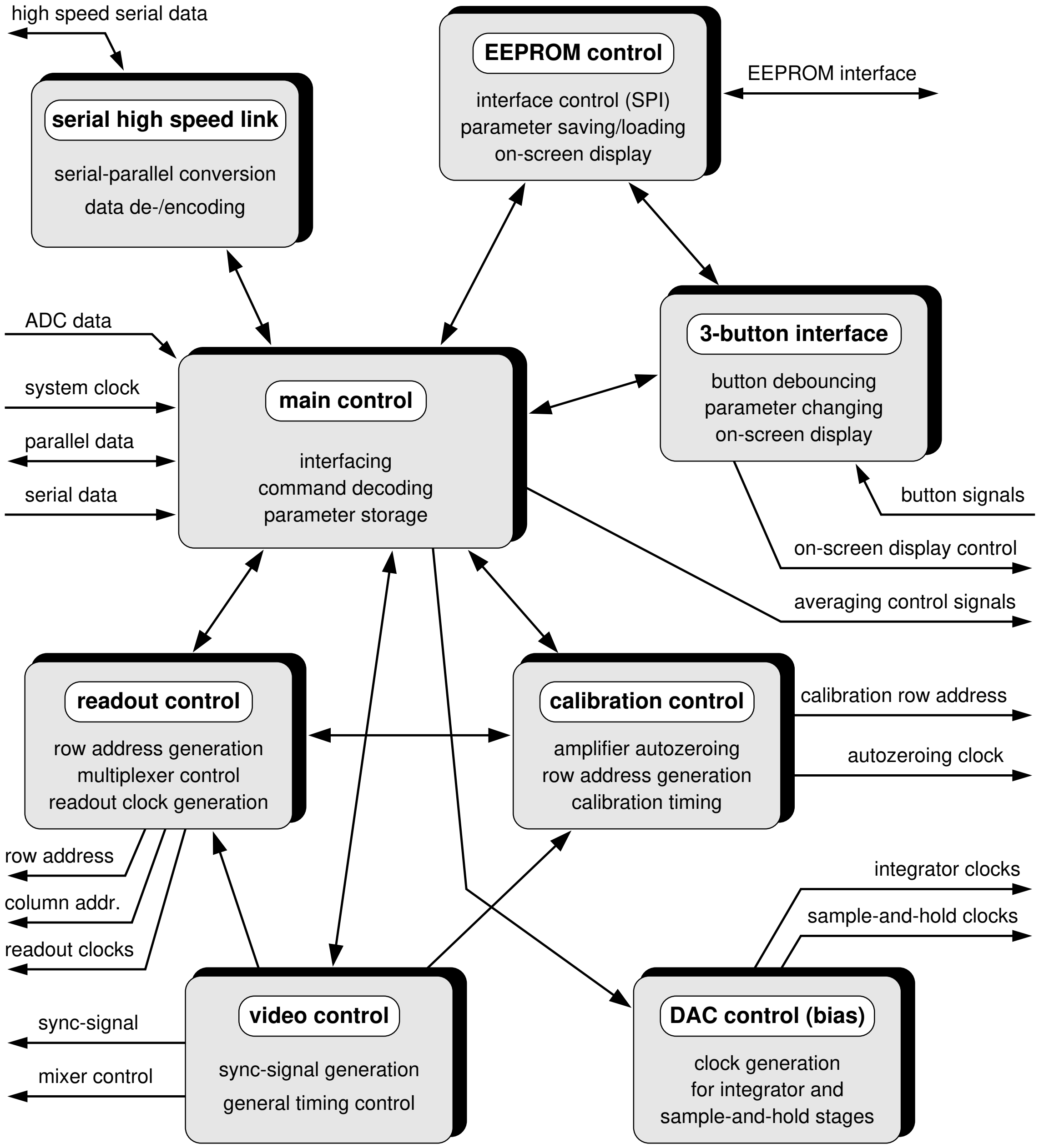


Figure 4.35: Block diagram of the control logic divided into the main subparts.

The properties of the individual building-blocks shown in figure 4.35 are shortly summarized in the following list. The principal behaviour is explained without going too much into detail. By this means a basic overview of the functionality of the control logic is given.

Main control: This part is responsible for the overall control and the communication between all other logic components. It includes the command interpreter for decoding the programming commands and the memory registers for storing the sensor parameter. A unidirectional serial interface using one clock and one data line is implemented to transfer the different commands to the image sensor. The integrated bidirectional parallel interface can also be used for programming the chip but basically allows to read out the on-chip ADC and the sensor parameters. Besides, the main control part provides the signals for adjusting the pixel averaging and for setting the gain of the output amplifier and the auto-exposure current mirror, respectively.

Serial high speed link: In addition to the parallel interface, a bidirectional serial interface is integrated in the image sensor. It can be used to read out the internal 10-bit ADC via two low voltage differential line pairs significantly reducing the number of lines in comparison to the parallel readout. Also, the sensor parameters can be adjusted or checked by this serial link. The maximum data rate is given by the pixel rate of 7.5 MHz multiplied by the bits per pixel which is 16 (data + control bits). Hence, the interface has to transmit 120 Mbit/s. The corresponding module contains the serial-to-parallel converter (and vice versa) and the required data encoding and decoding logic.

EEPROM control: In order to work properly, the image sensor has to be programmed with the appropriate parameters after every power outage. This could be done using one of the three implemented interfaces but would require some intelligent external device (computer, microcontroller, etc.). For this reason, all parameters can be stored in a small EEPROM outside the chip and are automatically loaded back into the sensor after a system reset. The EEPROM control module generates the required control commands and the SPI[12] protocol for writing into and reading from the EEPROM. Besides, it is responsible for controlling the on-screen display by reading the corresponding bitmaps from the EEPROM.

3-button interface: Due to the possibility of storing parameters in the external EEPROM, the sensor becomes independent of other control systems. Sometimes, however, it is required to change parameters in order to adapt the performance to the actual conditions. Therefore, a 3-button interface has been implemented. The control signals can be provided by any buttons mounted outside the chip (e.g. at the back of the camera housing). The first button changes the selected parameter, whereas the other two buttons increase or decrease the corresponding value. The name of the selected parameter is shown on the video screen (on-screen display) using the bitmaps stored in the EEPROM.

Readout control: This module is responsible for generating the readout row and column addresses. It has to check which part of the array needs to be read out (random pixel access) and which sensor mode is selected (video mode or arbitrarily chosen timing). If the digital zoom is enabled, the pixel timing is changed in order to map a subpart of the image to the complete screen. Additionally, the control clocks for the analog column multiplexer and the readout amplifier are generated in the readout control block. Every time before selecting a new row, it has to be checked if this row is currently selected for calibration. Otherwise a collision between readout and calibration row could occur.

[12] Serial Peripheral Interface

Calibration control: Every pixel row has to be calibrated for a definite time in regular intervals. The calibration control module has to take care of the self-calibration to ensure that these conditions are fulfilled. Poorly calibrated rows could result in images with annoying side effects. After checking that the current row is not selected for readout, the calibration row is set to the corresponding address. When the chosen calibration time has passed, the address switches to the next row. If a collision between readout and calibration row occurs, the logic either waits until the readout is finished or selects a different row for calibration. Besides, the clock signal for the autozeroing amplifiers and the precharge clock for the reference current lines are generated in this module.

Video control: The composite video signal corresponding to the CCIR standard needs a specific timing of the vertical and horizontal synchronisation signals. The video control block generates these sync-signals using different counters determining the required time steps by counting the number of passed clock cycles. It also gives the trigger signal for starting the on-screen display and provides some other timing signals used for the video signal generation.

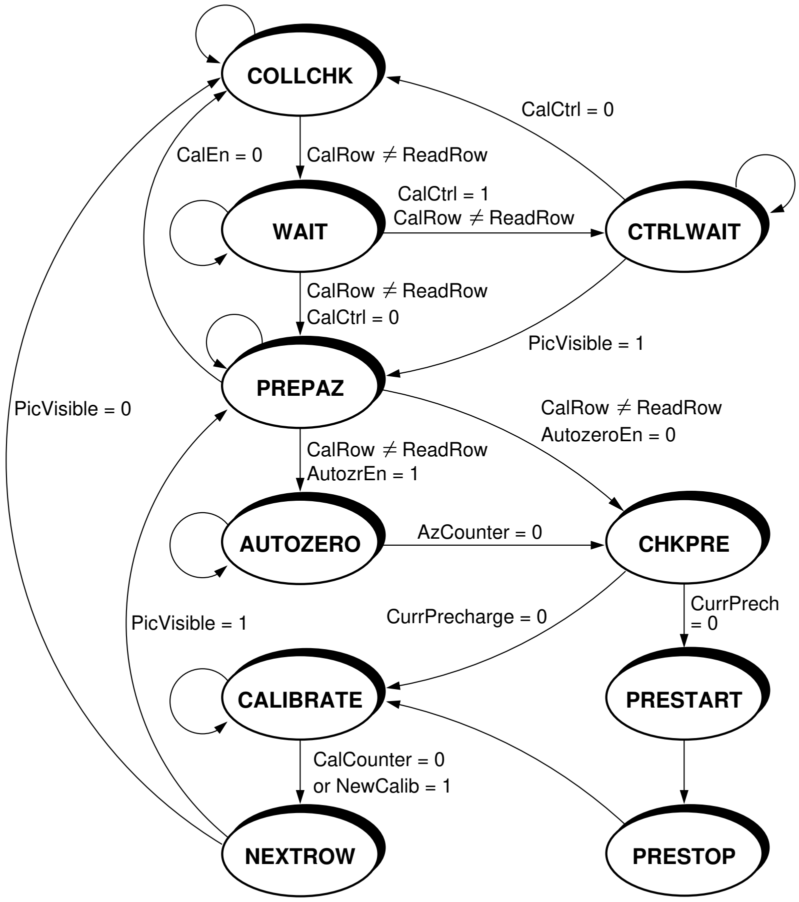
DAC control: The generation of the 19 bias voltages for the different sensor components is carried out by using one DAC and storing the output voltages on 19 sample-and-hold stages (cf. section 4.5). The digital-to-analog converter realized as an integrator stage needs a reset and another control clock determining the integration interval. The individual sample-and-hold stages require signals for enabling or disabling the corresponding transmission gates. All clock signals for the bias generator are produced in the DAC control module. The length of the integration interval depends on the parameter values of the voltages stored in the main control block.

Some of the modules described above are explained more in detail in the next sections in order to better understand the integrated algorithms and functionality. However, the following comments will stay on an abstract level and will not introduce the concrete verilog implementation. Otherwise, the explanations would go far beyond the scope of this thesis.

4.6.2 Calibration control

The calibration module generates the calibration row address and the control clocks for the autozeroing calibration amplifiers and for the precharging of the reference current lines. The state diagram corresponding to the calibration state machine is shown in figure 4.36. For the sake of clarity, it is simplified and includes only the essential signals. All possible transitions from one state to another are indicated by arrows. A transition occurs if the condition written beneath the corresponding arrow is true. Transitions without any indicated condition are always carried out if no other condition belonging to the current state is fulfilled. In case of two conditions for the same transition, both have to be true at the same time. A short explanation of the most important states and of the individual signals is given on the right side of the diagram.

After a system reset, the state machine is in the COLLCHK state to compare the address of the readout row with the address of the next calibration row. In the case, that no collision is detected, it changes to the WAIT state. Here, the collision is checked again. Then a transition to either CTRLWAIT or PREPAZ occurs depending on the value of CalCtrl. This signal selects, if the calibration is triggered externally by the readout control module (required for video mode) or if the internal counter determines the length of the calibration interval. CalCtrl = TRUE means external calibration control and causes a transition to the CTRLWAIT state, whereas CalCtrl = FALSE directly leads to the autozeroing preparation state PREPAZ. The start address for the first calibration row is loaded from



State explanations

CTRLWAIT	load calibr. address with first row number
PREPAZ	load AzCounter with autozeroing time
AUTOZERO	decrease AzCounter, autozeroing activated
CHKPRE	load CalCounter with calibration time
CALIBRATE	decrease CalCounter, calibration activated
NEXTROW	increase calibration row address

Signal declarations

CalRow:	calibr. row address
ReadRow:	readout row address
CalCtrl:	if TRUE, calibr. time = row readout time
PicVisible:	readout of visible pixels is going on
CalEn:	calibration enable
AutozrEn:	autozeroing of calibr. amplifier enable
AzCounter:	autozeroing counter
CurrPrech:	precharge of ref. current line enable
CalCounter:	counter for calibr. time
NewCalib:	start new calibration

Figure 4.36: Principal state diagram of the calibration control module. Some conditions and control lines are omitted for the sake of clarity.

the corresponding memory register. As soon as the trigger signal PicVisible indicating the beginning of the pixel readout becomes true the state machine also changes to PREPAZ.

Depending on the level of the AutozeroEn signal, which enables or disables the autozeroing cycle of the calibration amplifiers, a transition to AUTOZERO (if autozeroing is enabled) or CHKPRE occurs. Besides, the counter register AzCounter is loaded with the number of clock cycles corresponding to the selected autozeroing time. In the AUTOZERO state, the control clock switching the calibration amplifiers to autozeroing mode is activated. AzCounter is decreased until 0 is reached. The autozeroing control signal is deactivated and the module changes to the CHKPRE state. Here, the calibration counter CalCounter is loaded with the number of clock cycles selected for the calibration time. If the precharge of the reference current lines is selected (CurrPrech = TRUE), a change to the PRESTART and PRESTOP states occurs before the most important state CALIBRATE is reached. In this case, the precharge control line is activated for the duration of one clock cycle. In the other case, a direct transition to the calibrating state CALIBRATE is carried out.

Every clock cycle, CalCounter is decreased by one. When 0 is reached or the external signal NewCalib from the readout control module becomes true, the calibration state machine changes to NEXTROW. The calibration row address is increased (or set to 1 if the last array row is reached) and the system starts the calibration of a new pixel row. Therefore, it either switches to the COLLCHK state if the readout of the current frame is finished or to the PREPAZ state if the frame readout is still going on (PicVisible = TRUE).

The two different calibration modes determined by the CalCtrl signal result in a different relationship between the calibration row address and the readout row address. If CalCtrl = TRUE, the length of the calibration interval is equal to the time required for the readout of one pixel row. Consequently, the distance between the calibration and the readout row is constant, a collision of the two addresses should never occur. In the opposite case, the calibration time differs from the readout time leading to a varying distance between calibration and readout address. Although the latter case could cause address collisions and different pixel relaxation times (time between calibration and readout of one pixel), it should be applied when only subframes are read out. In contrast to the first mode, which starts from the beginning when finishing the readout of a frame even if some rows are not yet calibrated, the second one always calibrates all array rows.

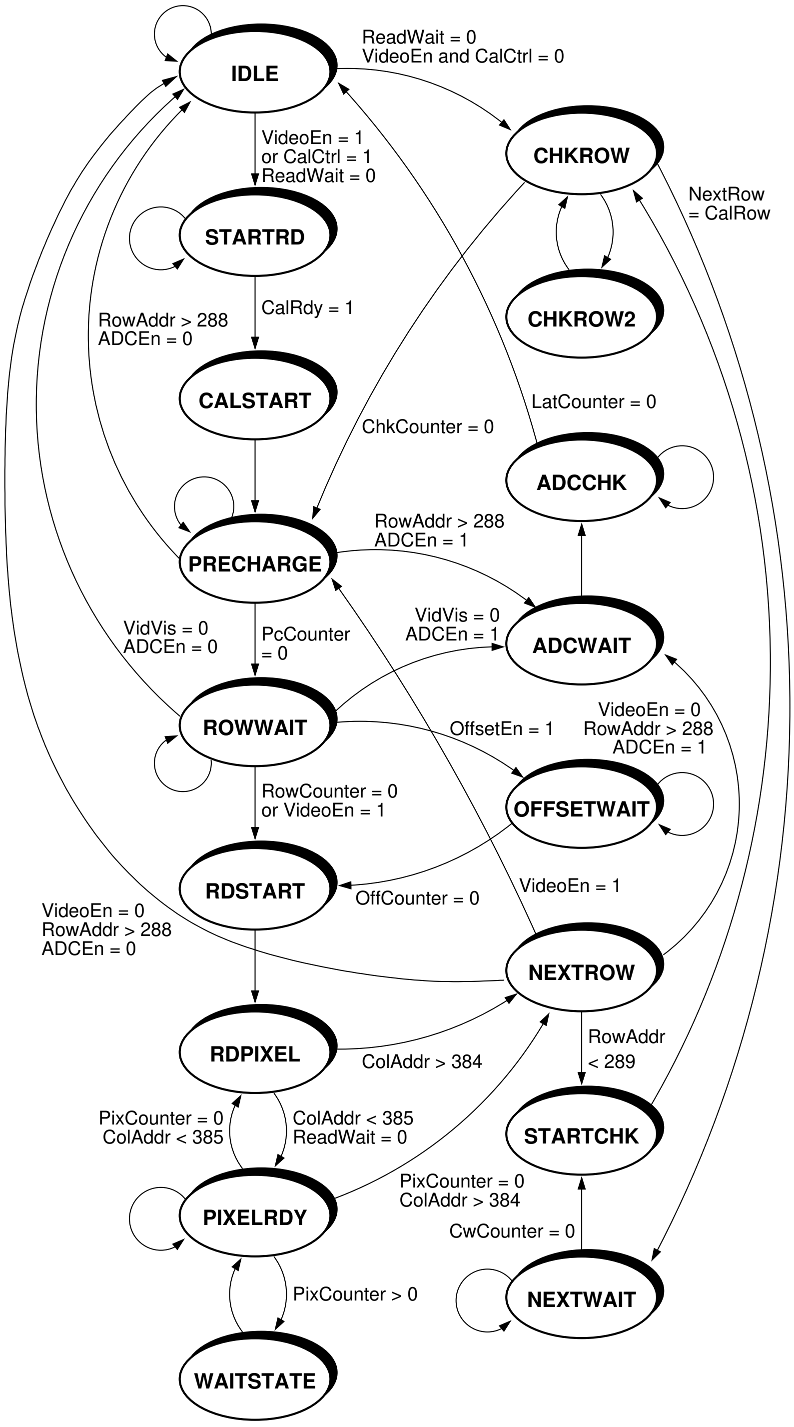
4.6.3 Readout control

Except for the main control part including all memory registers and the command decoding, the readout control module represents the largest building block. Since it is responsible for the readout timing, it has to communicate with most of the analog components and to generate the required timing signals. In addition, the different readout options like video or non-video mode, digital zoom, random pixel access, readout of averaged pixels, selectable precharge and readout times etc., have to be managed. Another important task is to avoid any collision between the calibration and the readout row. Otherwise a number of useless pixel values would result.

Figure 4.37 contains a simplified state diagram of the readout module. It is still relatively complicated although all states and signals referring to random pixel access, digital zoom, pixel averaging and exact readout clock generation have been omitted. The presented diagram shows the principle state machine for realizing the basic readout functionality. The conditions for a transition from one state to another are written beneath the corresponding arrow. Arrows without condition are always carried out, if no other condition belonging to the current state is true. The two tables on the right shortly explain the most important states and the used signal names.

After a system reset or a readout reset, the module is in the IDLE state. If the ReadWait signal, which can either be programmed or externally controlled by a separate line, goes low, the readout process starts. Depending on the level of VideoEn (video mode enable) and CalCtrl (calibration time controlled by the readout module, i.e. calibration time equals readout time of one row) a transition to STARTRD or CHKROW occurs. If arriving in the STARTRD state, the system waits until a possible calibration cycle is finished (CalRdy = 1) and subsequently changes to CALSTART. Here, the precharge counter register PcCounter is initialized with the corresponding precharge time. In the next clock cycle the PRECHARGE state is reached.

If neither the video mode is enabled nor the CalCtrl signal is high, the distance between the readout and the calibration row is not fixed but varies with time. Therefore, a collision check has to be carried out to ensure that the next readout row is not being currently calibrated. This is done in the CHKROW state considering up to 15 rows which will be selected next. By this means, a minimum time distance between calibration and readout of the same pixel can be guaranteed. It is ensured that the pixel has already reached its normal operation level before being read out. If a collision is detected the state machine switches to NEXTWAIT and waits for a pre-defined time before returning via STARTCHK to CHKROW. When the collision check has finished, the precharge counter PcCounter is loaded and a transition to the PRECHARGE state occurs. During the next steps, the behaviour is equal for all different readout modes.



State explanations

STARTRD	load RowAddr with first row number
CALSTART	load PcCounter with precharge time
CHKROW	check for collision load CwCounter decrease ChkCounter
PRECHARGE	load RowCounter, precharge clock activ. decrease PcCounter
ROWWAIT	load OffCounter decrease RowCounter
OFFSETWAIT	decrease OffCounter
RDSTART	load first col. address
RDPIXEL	load PixCounter enable readout clock
PIXELRDY	increase column addr. disable readout clock
NEXTROW	increase row address
STARTCHK	load ChkCounter
NEXTWAIT	decrease CwCounter
ADCWAIT	ADC-latency cycles load LatCounter
ADCCHK	decrease LatCounter

Signal declarations

ReadWait:	if TRUE, readout starts
VideoEn:	video timing enabled
CalCtrl:	if TRUE, calibr. time = row readout time
CalRdy:	no calibration is going on
RowAddr:	readout row address
ADCEn:	ADC enabled
NextRow:	readout row which will be selected next
CalRow:	calibr. row address
ChkCounter:	collision check counter
VidVis:	visible video image
PcCounter:	precharge counter
OffsetEn:	image border shifted into visible frame
OffCounter:	offset counter for OffsetEn:
RowCounter:	counter for initial row waiting time
ColAddr:	readout column addr.
PixCounter:	counter determining the pixel rate
CwCounter:	collision wait counter
LatCounter:	ADC latency counter

Figure 4.37: Principal state diagram of the readout control module. Some states, conditions and control lines (which, for instance, refer to the digital zoom, random pixel access or pixel averaging) have been omitted in order to simplify the diagram.

In the PRECHARGE state, the precharge clock of the column source followers is activated and the PcCounter decreases every clock cycle until it becomes 0. Assuming a row address below 288, a change to the ROWWAIT state is carried out after the RowCounter has been loaded with the row waiting time. Now, the RowCounter decreases and the OffCounter is initialized with the number corresponding to the shifted image (only video mode, upper left corner is shifted into the visible screen area). If the image shifting is enabled (OffsetEn = 1), the module changes to OFFSETWAIT and subsequently, when the OffCounter reaches 0, to RDSTART. If the image shifting is disabled, a direct transition to RDSTART occurs. Here, the address of the first readout column is loaded into the address register, followed by a change to the RDPIXEL state.

Here, some additional states are required to generate the different readout and multiplexer clocks. In the diagram they are combined in the two states RDSTART and RDPIXEL. In the latter state, the main readout clock is enabled and the counter PixCounter, responsible for the pixel timing, is loaded with the appropriate number of clock cycles. As long as the column address is below 385, the system changes to the PIXELRDY state. Here, the column address is increased and the readout clock is disabled. If the PixCounter shows a value higher than 0, it is decreased in WAITSTATE and again checked in PIXELRDY. Finally, when PixCounter = 0, the next pixel is read out by going back to RDPIXEL.

This cycle is interrupted as soon as the column address exceeds 384. The readout module switches to the NEXTROW state where the readout row address is increased. If the video mode is enabled, the system goes back to the PRECHARGE state and the readout of the next pixel row starts. Otherwise, a new collision check has to be carried out. Therefore, a transition to the STARTCHK state and subsequently to the CHKROW state occurs before a new array row can be selected for readout.

When the row address reaches the end of the sensor array, i.e. 288, the readout of one frame is completed. The system either directly goes back to the IDLE state or, if the on-chip ADC is enabled, changes to the ADCWAIT state. Together with the ADCCHK state, two further clock pulses for the ADC clock are generated in order to compensate for the ADC latency (cf. appendix A). After the last analog-to-digital conversion, the ADC requires two more clock cycles until the last pixel value appears at the output. Finally, the module also switches to the IDLE state and the readout of a new frame can begin.

It should be noted that the different counters required for the readout control module are composed of only a few main counters which are used several times. Since the maximum number of counters working in parallel is four, only four separate counters have to be implemented. This saves flip-flops and additional logic circuitry resulting in a reduced size of the overall digital part.

4.6.4 Video timing generation

The composite video signal in any standard requires a specific pattern of voltage pulses to synchronize the internal vertical and horizontal oscillators of the video device with the incoming video signal. These synchronisation pulses are generated in the video control module. The resulting analog output signal of the image sensor complies with the European CCIR standard. It uses an interlaced method which shows the even lines in the first frame field and the odd lines in the second frame field. That means, that the synchronisation pattern has to change slightly between the first and the second field. Since the resolution of the developed image sensor corresponds to the resolution of one field, it shows the same pixel data in both frame fields. Therefore, it is also possible to use a non-interlaced video signal which only act on the even video lines. Both, the interlaced and the non-interlaced mode, are integrated in the sensor chip.

The state diagram of the sync signal generator is shown in figure 4.38. In contrast to the previous two state diagrams of the calibration and the readout part, additional information beside the transition conditions is given. A change of the current state always occurs if the non-framed equations written beneath the transition arrow are true. At the same time the framed assignments are carried out changing the values of the concerned variables. The circle transitions which have no condition are carried out as long as no other condition of the current state becomes true. The states resulting in

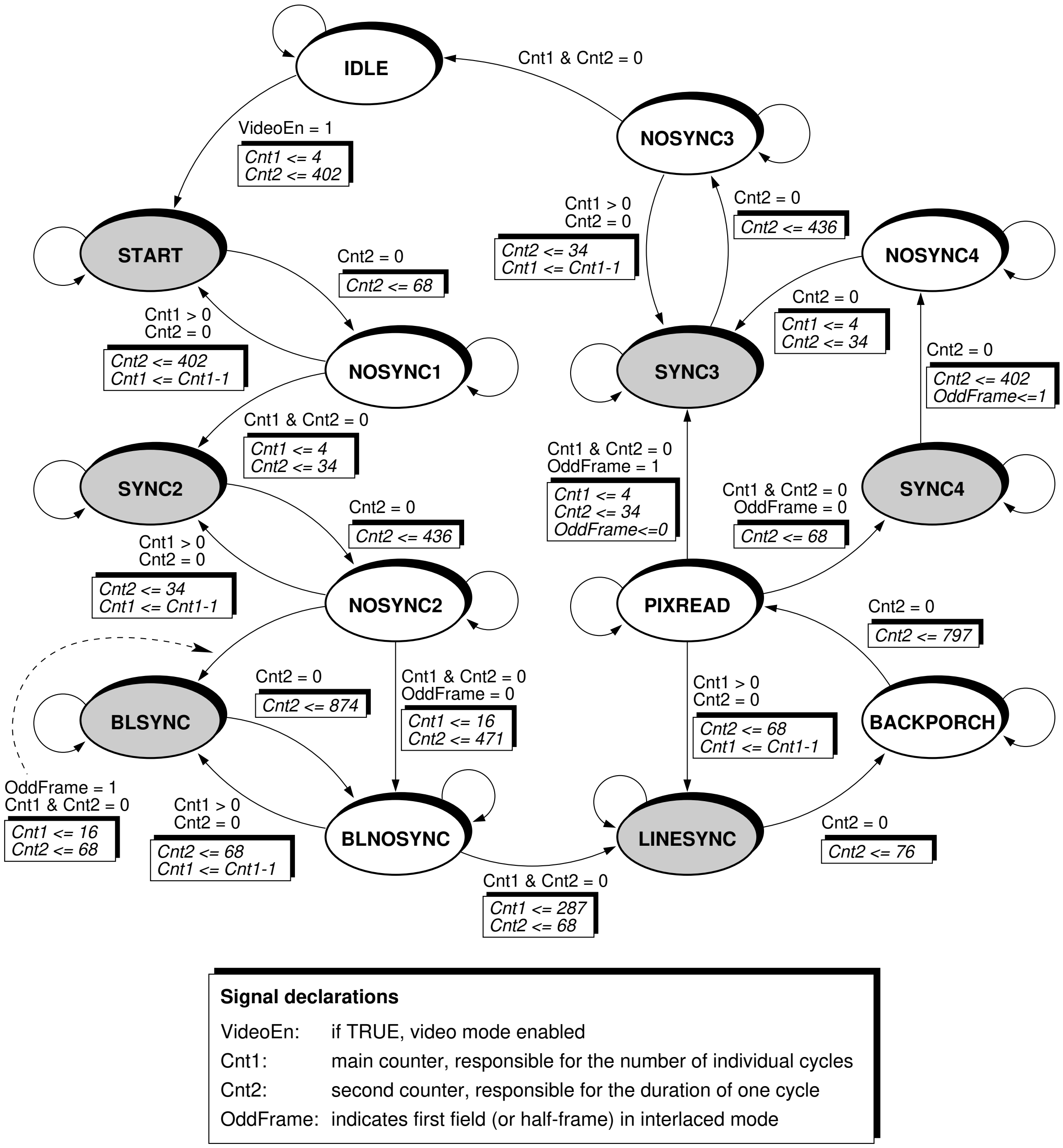


Figure 4.38: State diagram of the video control module generating the video synchronisation signal. The transition conditions are written without frame beneath the corresponding arrow, whereas new signal assignments are surrounded by a black frame. The synchronisation control signal SYNC is active in all states having a grey background.

a high level of the synchronisation control signal SYNC are indicated with a grey background. In all other states, the SYNC signal is low. This signal controls the output mixer which is presented in section 4.4.4.

The full functionality is managed with two counters. The first one, Cnt1, is responsible for counting the number of individual active or non-active pulses. The second one, Cnt2, determines the duration of one pulse by counting the number of passed clock cycles. The second counter is always decreased with every clock cycle (independent of the current state), whereas the first counter only decreases when the assignment Cnt1 $<=$ Cnt1 $-$ 1 is noted at the corresponding transition arrow. The resulting timing diagram showing the vertical synchronisation pattern for the first and second frame field (interlaced) is given in figure 4.39. When the video state machine changes from IDLE state to START, the sync signal generation begins at the point indicated with *frame start* in the upper timing diagram. The system clock oscillates at a frequency of 14.7456 MHz corresponding to 67.8168 ns per clock cycle. Therefore, the pulse lengths can be specified in microseconds or in the number of clock cycles. The timing diagram includes both values.

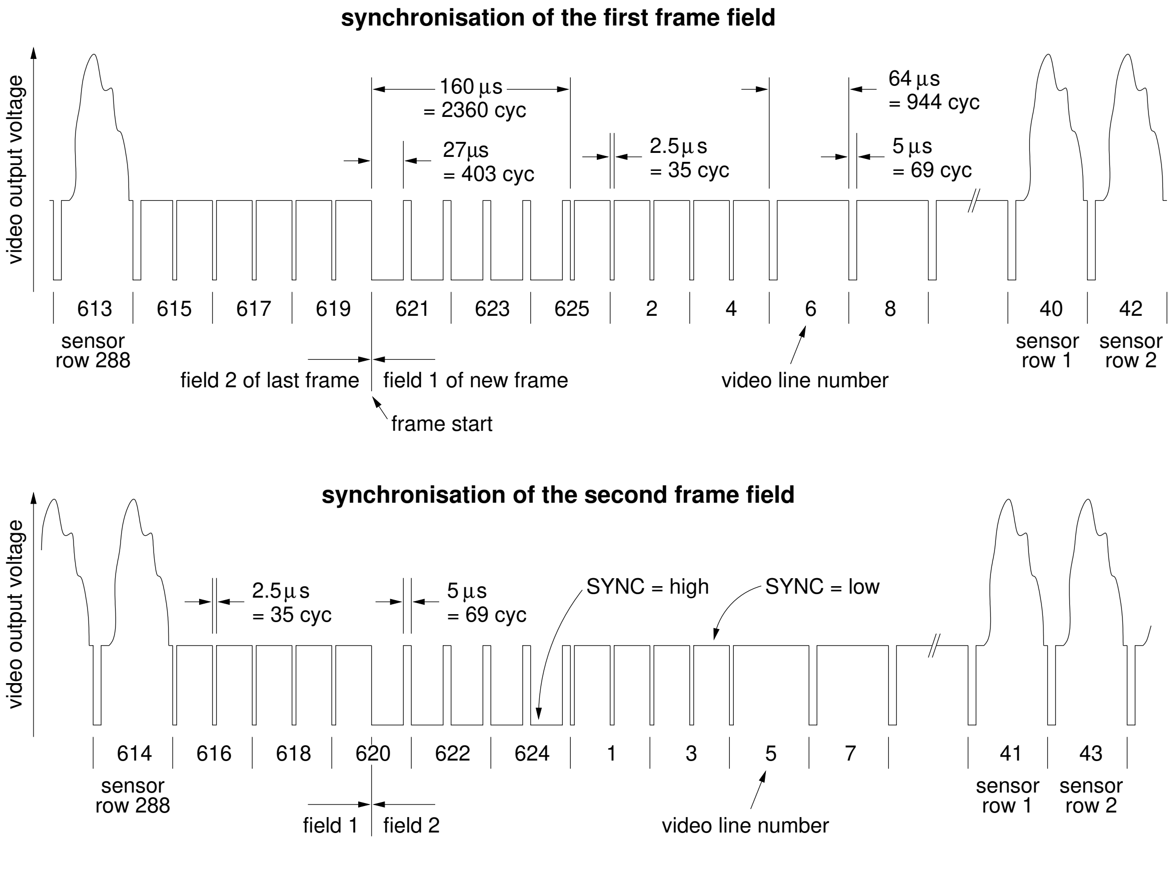


Figure 4.39: Timing diagram of the synchronisation pulses required in interlaced mode (CCIR timing). An active SYNC signal (high) results in a low voltage level and vice versa, because the video synchronisation signals have to be negative.

After starting the video timing by activating the signal VideoEn and changing to the START state, five pulses with a length of 27 μs or 403 cycles each are generated first, separated from each other by intervals of 5 μs or 69 cycles. This is carried out by 5 transitions between START and NOSYNC1. Next, five pulses with a length of 2.5 μs (= 35 cycles) produced by the states SYNC2 and NOSYNC2 follow. Subsequently, the normal line synchronisation starts with an initial pulse of 5 μs and a pause of 59 μs. This ends up in 64 μs or 944 cycles per line. The first 17 lines generated by the BLSYNC and BLNOSYNC states are completely black. They are located in the invisible part of the video screen. Then, the sensor readout begins. The sync pulse for each new line is determined by the LINESYNC state. The BACKPORCH state causes another delay of about 5.2 μs before the pixel readout of one row occurs in PIXREAD.

When reaching the last video line, five compensation pulses are generated with the help of the SYNC3 and NOSYNC3 states. If the system is currently in the second half-frame (field2), another pulse is inserted using the states SYNC4 and NOSYNC4. Finally, the state machine returns to the IDLE state and a new frame can start. One frame field includes 312.5 lines and takes 20 ms. Regarding both fields of a complete frame, 625 lines are generated in a time of 40 ms. This corresponds to $625 \times 944 = 590000$ cycles of the system clock.

4.7 Digital I/O interfaces

The developed camera chip *Divichi* possesses five diverse communication interfaces designed for different requirements and applications. The unidirectional serial interface and the bidirectional parallel interface include the standard functionality commonly provided by such communication ports. They are shortly explained in the next two sections. The high speed bidirectional serial interface represents a more sophisticated solution. It is therefore presented in a more detailed manner. Finally, the EEPROM interface control, used for parameter storage and for the on-screen display, and the manual 3-button interface are described.

4.7.1 Unidirectional serial interface

The unidirectional serial interface is designed for easily programming the sensor parameters without using complex protocols or special signal conditions. The interface consists of the four signals $\overline{\text{CHIPSLCT}}$ (select chip for writing), SERCLK (serial clock), DATAIN and DATAOUT. The former three ones are input lines whereas the latter one is an output signal. The required timing is shown in figure 4.40. If no data is transferred, the clock line and the chip select line have to be high in order not to influence the functionality of the other two programming interfaces (parallel and high speed serial). To write a command into the chip, the $\overline{\text{CHIPSLCT}}$ signal has to go low. Each command is composed of 14 bits and is transmitted via the DATAIN line. The serial clock (SERCLK) controls an internal shift register which performs a data transfer every rising edge. Hence, 14 clock cycles have

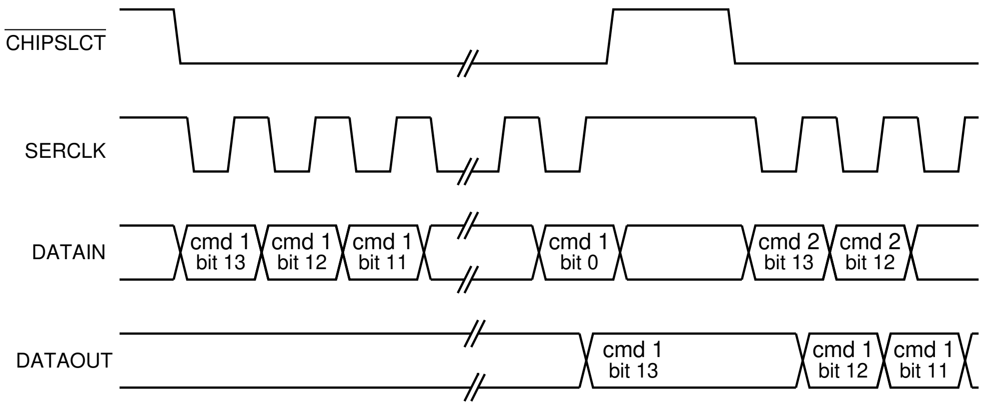


Figure 4.40: Timing diagram of the serial input interface.

to be provided until one command completely fills the shift register. The following rising edge of $\overline{\text{CHIPSLCT}}$ initializes the command decoding and prepares the chip for getting a new command.

The DATAOUT line is connected to the last storage cell of the shift register. By this means, the DATAIN line of other programmable devices, for instance further image sensors or an optical motor zoom controller, can be connected to this output. They can be programmed by firstly shifting the data through the first image sensor and then into the following device. This interfacing architecture is called a *daisy chain* because the output of one device clings to the input of the next.

4.7.2 Bidirectional parallel interface

The parallel chip interface is integrated not only to write commands to the sensor but also to read out the digital pixel values generated by the on-chip ADC. Besides, all sensor parameters can be read back to verify them in case of any malfunction. The interface consists of 10 data lines and three control lines. The upper eight data bits (DATA[9] - DATA[2]) are bidirectional signals whereas the lower two bits are only used as output lines. The $\text{W}/\overline{\text{R}}$ signal represents an input line and selects between write (high) and read (low) mode. ACK/CLK, also an input signal, clocks command data into the chip or operates as handshake signal during the readout. The $\overline{\text{VALRDY}}$ signal is an output line and indicates, that a new data value is ready for reading.

Figure 4.41 shows the interface timing in the case of command writing, data reading without and data reading with a handshake protocol. Since one command consists of 14 bits, it has to be divided into two parts in order to be transmitted via an 8 bit interface. The first part includes two address bits (to select one of up to four sensor chips connected to the same physical interface) and the upper 6 command bits. The second part contains the residual lower 8 command bits. Data is clocked into the chip with the rising edge of ACK/CLK. If no transfer is going on, this signal has to be high so it will not interfere with the other chip interfaces.

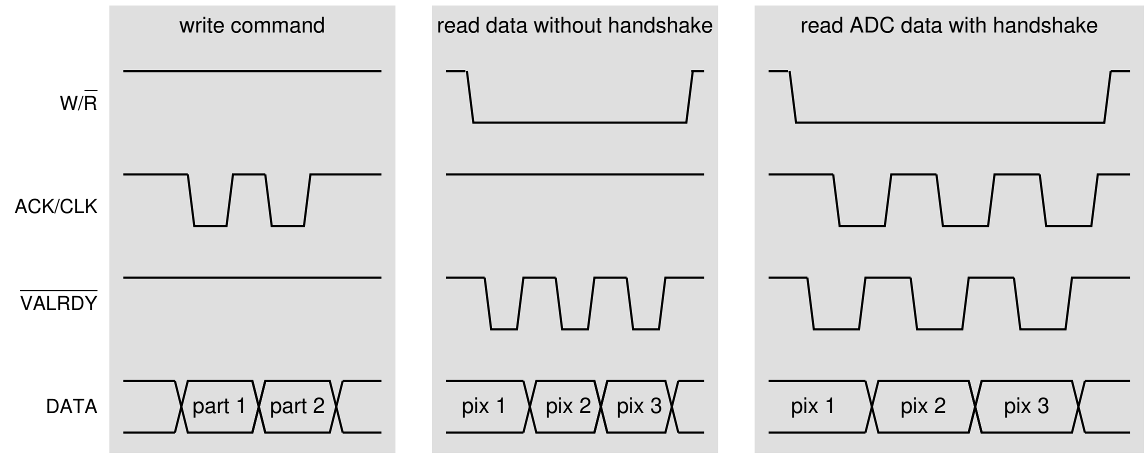


Figure 4.41: Timing diagram of the parallel interface. The three different cases referring to command writing, data reading without handshake and data reading with handshake are shown.

The data readout can be carried out in two ways: either with or without feedback from the receiving device. If switched to non-handshake mode, the chip generates the pixel data according to the internal timing adjustments and indicates every new value by the falling edge of $\overline{\text{VALRDY}}$. Changing to handshake mode allows to control the readout timing by the external acknowledge signal ACK/CLK. Every time $\overline{\text{VALRDY}}$ goes low due to a new pixel value, ACK/CLK has to confirm the successful reading by also going low. After $\overline{\text{VALRDY}}$ has returned to the high level, a new value is not presented at the data output before ACK/CLK is also pulled up again. The readout of the internal parameter settings can only be carried out in the non-handshake mode as it is coupled to the EEPROM timing.

4.7.3 High speed bidirectional serial interface

The bidirectional serial interface has been implemented to obtain a power-saving digital connection with as few lines as possible. Within the scope of the tactile vision aid system, the camera chip will be mounted close to the eyes (e.g. on the glasses). Since the other system parts are separated from the image sensor, a thin and flexible cable for the interconnection should be used. The applied solution requires two signal connections realized as shielded low voltage differential signal pairs (twisted pair line) each. The first line transmits the interface clock, the second one the digital data. The physical implementation with respect to the signal voltage levels follows the IEEE 1394 standard, which is also known as *firewire* [IEE96]. This provides the possibility of using commercial transceiver chips for the counterpart outside the image sensor.

The principal serial connection between the sensor chip and the external transceiver is shown in figure 4.42. The diagram refers to the data line which in contrast to the clock line has to be bidirectional. The connection lines are terminated on both sides with a 110 Ω resistor corresponding to the cable impedance. Thus, each driver sees an output load of 55 Ω. The left transceiver integrated on the image sensor consists of a differential line driver and a differential input amplifier. The latter device is built up in the same way as the PMOS input stage of the operational amplifier for buffering the bias voltages in figure 4.34. The driver circuit is shown in figure 4.43. It is composed of six transistors forming, together with the output load of 55 Ω, a switchable resistive divider.

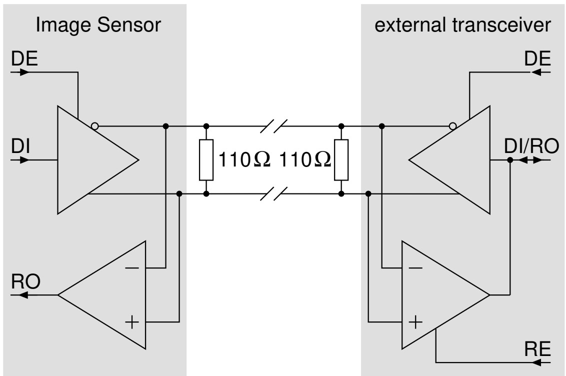


Figure 4.42: Differential interface connection between the image sensor and an external transceiver.

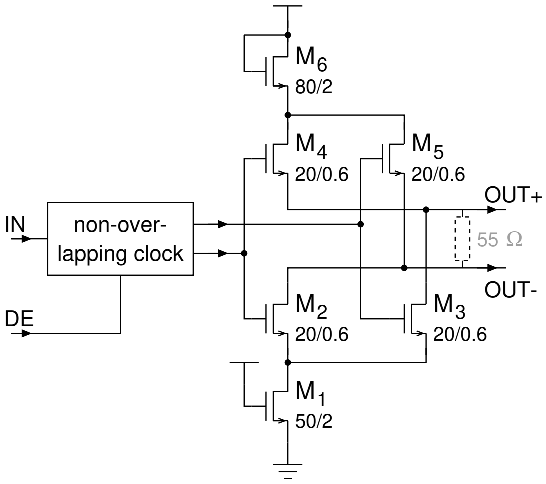


Figure 4.43: Circuit diagram of the differential line driver implemented in the image sensor.

If the transistors M_2 and M_4 are enabled and M_3 and M_5 are disabled, the output voltage OUT+ is higher than OUT-. The opposite situation results, if M_3 and M_5 are enabled and M_2 and M_4 are disabled. The voltage difference between the two output signals amounts to about 200 mV. The switching transistors are controlled by non-overlapping clock signals which are generated in the same way as shown in figure 4.12 for the calibration amplifier. In addition, a driver enable input (DE) is included. If low, it switches off all four transistors and forces the driver to go into a high ohmic state. This is required if the transceiver is in receiving mode in order to ensure that the on-chip driver outputs do not interfere with the data coming from the external line driver.

The external transceiver can be any bidirectional device which physically converts standard digital signals (TTL or CMOS) into the low voltage differential values corresponding to the IEEE 1394 norm. In the test setup for the sensor evaluation, the transceiver chip DS36C200 from National Semiconductor [NAT98] has been used. Although data can be transmitted in both directions, the interface clock in any case (reading or writing) is generated externally. It therefore needs only a unidirectional connection. By this means, no high frequency oscillator with PLL[13] to synchronize external data and internal clock is required on the sensor chip. The internal shift register used for data reading and writing is always controlled by the external clock.

Figure 4.44 contains the timing diagram showing the command writing into the chip. The first row includes the data bits with respect to CMOS voltage levels going into the external transceiver. The second and third row represent the converted low voltage signals being transmitted through the twisted pair cable to the image sensor. The lowest row finally shows the interface clock before also being converted into differential signals.

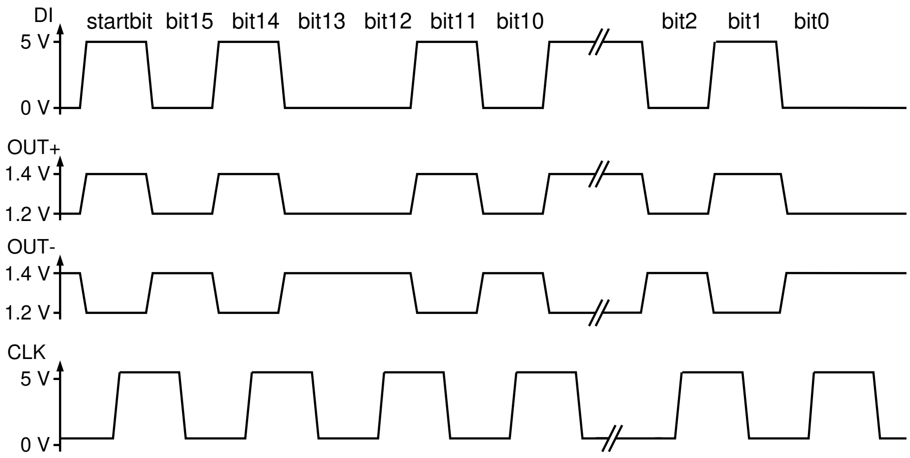


Figure 4.44: Timing diagram of the high speed serial interface. The writing cycle of one single command is shown.

As can be seen, a new data bit becomes valid with every edge (rising and falling) of the clock signal. Consequently, the clock frequency is halved compared to the case that data is only transmitted every rising or every falling edge, respectively. One command word consists of 17 bits: 1 start bit, 2 address bits and 14 data bits describing the actual command. The start bit is required to indicate that a new data block is received. The two address bits allow to connect up to four image sensors to the same bus lines (e.g. applicable for stereo vision). If the digital pixel data or the internal parameters should be read out, the sensor has to be switched over to the sending mode by a specific control command. Then, data is transmitted in the opposite direction to the external receiver with every new clock cycle. In this case, one data word is composed of 16 bits: 1 startbit, 2 address bits, 3 status bits, 10 data bits. Again, the start bit indicates a new data block and the address corresponds to the currently sending chip. The status bits refer to the pixel position and readout mode as follows: first pixel of a new frame, first pixel of a new line, other pixel position or parameter readout.

The complete interface has been designed to reach a transfer rate of 120 MHz leading to a clock frequency of 60 MHz. This value results from the video pixel rate of nearly 7.5 MHz multiplied

[13]phase locked loop

by the 16 bits per pixel. If the interface is in readout mode, it can be reset to the command writing mode by holding the clock signal high for a few microseconds. This, however, is only required, if the readout has to be interrupted before it is completed. Depending on the selected readout mode, the sensor automatically returns to the writing mode after sending one pixel or one complete frame. A more detailed description concerning the interface protocol and the sensor commands can be found in the Divichi user manual in appendix E.

4.7.4 EEPROM parameter storage

The digital control part of Divichi contains 285 memory bits determining the sensor parameter adjustments. They should be tuned individually for each chip in order to achieve the optimal performance. Since the on-chip registers lose their information in case of a power failure, it has to be stored externally. Therefore, a standard EEPROM interface is included in the sensor chip which allows transfer of the parameter settings from the image sensor to the external memory and vice versa. The stored data is read by the camera chip either in case of a system or power-on reset or when initiated by the corresponding command.

Besides the sensor parameters, the bitmaps belonging to individual commands of the on-screen display are saved in the EEPROM. When the 3 button interface is activated, the bitmap data is read out according to the selected command. It controls the TEXT signal of the output mixer stage (cf. section 4.4.4) generating the brightness level of the on-screen script. Every command bitmap consists of 512 bits arranged in 8 lines of 64 dots each. Since 13 different commands can be selected by the camera buttons, an 8 kbit EEPROM is sufficient for storing the sensor parameters and the on-screen bitmaps. In the realized camera system, a *microchip 25C080* device providing 8192 memory bits and a Serial Peripheral Interface (SPI) is used [MIC98].

The SPI interface is very similar to the unidirectional programming interface of the image sensor (see section 4.7.1). The timing diagram in figure 4.40 also applies except for the fact that the EEPROM does not have a serial output for building a daisy-chained setup. On the other hand, it provides an output line which is required to read out the stored data. The connection lines between sensor chip and EEPROM are shown in figure 4.45. The signals SI (EDO), $\overline{\text{CS}}$ ($\overline{\text{ECS}}$) and SCK (ESCK) correspond to the interface signals DATAIN, $\overline{\text{CHIPSLCT}}$ and SERCLK in figure 4.40. This figure describes the timing of the data transfer from the sensor to the external memory. However, the command length is not 14 but 8 bits. The letter E in the signal names on the sensor side in figure 4.45 refers to the word EEPROM, i.e. EDI means EEPROM Data Input. The SO (EDI) line goes in the opposite direction and represents the EEPROM output line. The timing for the readout is similar to the timing for the data writing. The clock signal is still provided by the sensor chip, whereas the data is produced by the EEPROM on the SO line.

The internal memory organisation is given in table 4.46. The EEPROM contains 1024 memory cells with 8 bits each. The given addresses refer to the memory cells and not to the individual bits. The sensor parameters are divided into 3 parts. The first part includes the values which can be changed by the button interface. To save the altered values, only the first block has to be transferred to the memory. This guarantees, that the information of the other two parts cannot be destroyed by a possible error during the data transmission. Starting from address 040h, the command bitmaps are stored. Each bitmap occupies 64 memory cells. Hence, the second one begins at the address 080h which is 64 cells away from 040h.

The used EEPROM is capable of accepting clock frequencies of up to 3 MHz. Since the system clock of the image sensor is much higher (nearly 15 MHz), a clock signal with only a third of the main clock frequency is applied to the digital EEPROM control part. Every cycle, the serial EEPROM

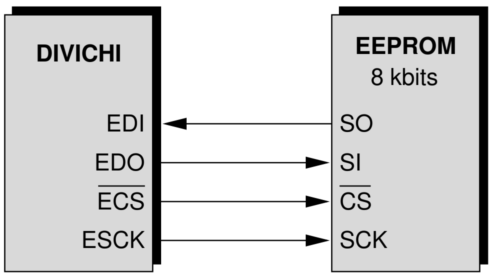


Figure 4.45: Schematic interconnection diagram between the sensor chip Divichi and an external EEPROM.

address	data
000h	parameter block 1
010h	parameter block 2
020h	parameter block 3
040h	command bitmap 1
080h	command bitmap 2
0c0h	command bitmap 3
⋮	⋮
340h	command bitmap 13

Figure 4.46: Data organization in the EEPROM.

clock changes its level. This means that two internal clock cycles are required to get one external serial clock cycle. Consequently, the data rate to the external memory is $15/(3 \cdot 2)$ MHz $= 2.5$ MHz. Because one data bit corresponds to the time of three pixels (pixel rate 7.5 MHz), one bitmap pixel occupies the size of 3×3 sensor pixels on the video screen.

4.7.5 Three button interface with on-screen display

The image sensor provides three input pads connectable to buttons mounted on the camera housing. When pushing a button, the corresponding input pin is pulled up to the positive supply voltage V_{dd} leading to a level change of the digital signal which otherwise is connected to ground. Unfortunately, mechanical switches are not ideal digital signal sources but introduce a lot of switching noise. This means, that the voltage level of the button output shows an unsmooth transition from one voltage to the other but toggles several times between both levels until the final and stable state is reached. This behaviour can be seen in figure 4.47. Part a) contains the ideal switching process, part b) the realistic one. The switching process of a mechanical device can take up to several milliseconds. Thus, the subsequent digital logic, operating with much faster signals, would detect many level changes instead of just one.

The easiest way to overcome the switching problem is to insert a RC-delay slowing down the level transition. However, this would require one additional capacitor per button resulting in a higher

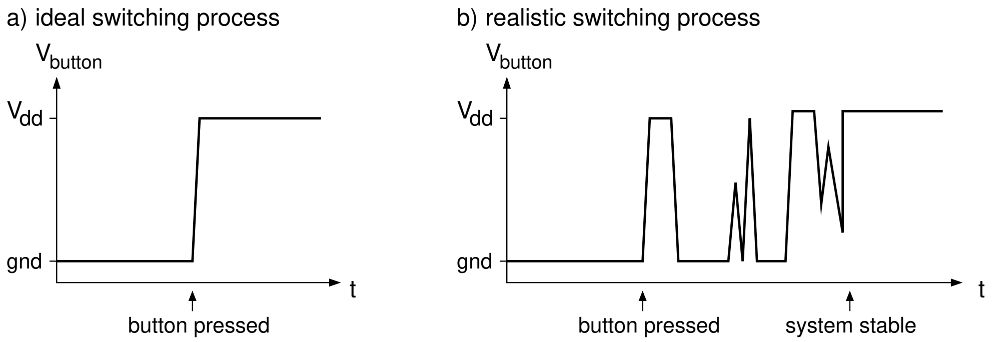


Figure 4.47: Ideal and realistic switching process when closing a mechanical switch. The realistic transition shown in part b) can take up to several milliseconds.

number of external components. The other possibility is to digitally eliminate the transition flicker. This solution is implemented in the camera chip. It uses a counter measuring the time between one and the next signal change. If this time is too short, the transition is ignored. A new level is only accepted, if the signal is stable for more than 40 ms.

As soon as one of the three buttons is pressed, the currently selected command appears on the video screen. When all buttons are released, the display disappears after a few seconds. The first button steps through the 13 selectable commands including digital zoom, image size, averaging, brightness, contrast and a few more adjustments. The other two switches increase or decrease the corresponding parameter value. The concrete implementation of the on-screen display has been realized with the help of the EEPROM interface and is described in the previous section. More detailed information about the handling and the functionality of the 3-button interface is given in the Divichi user manual in appendix E.

4.8 Chip layout

All structures described in the previous sections of this chapter are realized in the AMS 0.6 μm CMOS process. As already mentioned, this process provides one polysilicon and three metal layers. The third metal layer is used for shielding all devices beside the photodiodes against incident light. In most cases, only the wide power lines are routed with metal 3 in order to cause as few discontinuities in the shielding layer as possible. The final layout, including the sensor array and all complementing components, occupies an area of 11.5 mm $\times$ 7.7 mm $=$ 89 mm^2. The sensor array itself represents the largest part. Its size amounts to 386×290 pixels times the size of one pixel ($24 \times 24\,\mu\text{m}^2$) which equals 65 mm^2.

A micro-photograph of the camera chip is shown in figure 4.48. The large and homogeneously appearing area represents the actual sensor array. Since one pixel contains 10 transistors, the whole array includes more than 1 million transistors. This large number led to some severe problems during the design process of the chip because the applied software tools were unable to cope with so many active devices. Therefore, the final checks before submitting the layout to production were carried out with a modified design. It only includes all structures beside the sensor array and additionally the first and last array row and column. In other words, the main part of the array was omitted to reduce the number of transistors. Since all pixels are identical, no error should be overseen if checking only the outer pixel line of the array.

The calibration amplifiers and the reference current sources are located above the pixel matrix. Below the sensor array, the column multiplexer including column buffers and address decoder can be seen. On the right side of the chip, no active structures beside some power and analog input pads exist. The left part finally contains the digital part, the analog-to-digital converter and the analog readout structures like amplifiers and mixer stage. On most of the pads having a size of nearly $100 \times 100\,\mu\text{m}^2$, the bond wires connecting the chip to the outside can be seen. They consist of a thin aluminium wire with a diameter of 25 μm.

In order to protect the sensor array from sudden fluctuations of the power supply, a ring of blocking capacitors surrounds the pixel matrix. They are realized as NMOS transistors using the gate-channel capacitance and show an overall value of 2.2 nF. The total number of active devices including all transistors, resistors and capacitors amounts to about 1.4 million. Apart from the sensor array and its bounding structures, the main contributions are given by the digital part (50000 transistors) and the ADC (12000 transistors).

The most interesting layout part which is the left border of the camera chip, is shown again is figure 4.49 in an enlarged representation. The arrangement of the individual components is explained

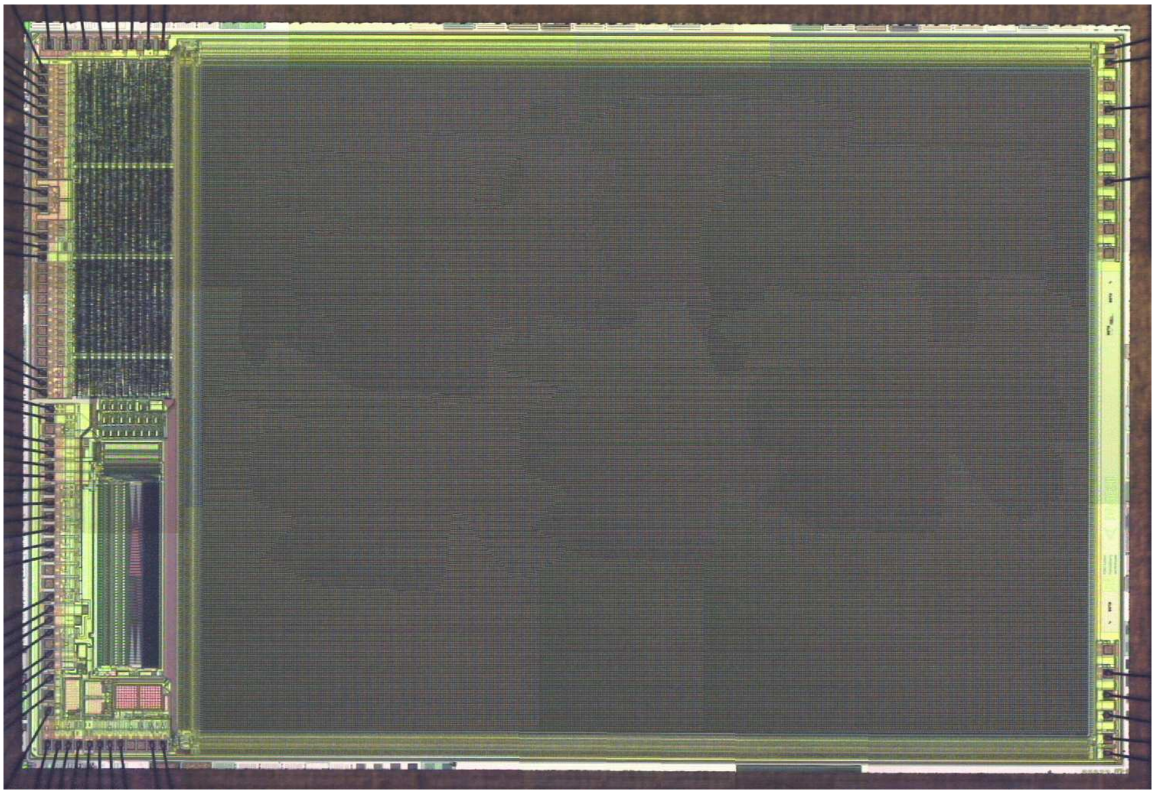


Figure 4.48: Micro-photograph of the image sensor Divichi. It is scaled by a factor of 13. The true chip dimensions are 11.5 mm × 7.7 mm.

by means of the schematic floor plan at the right of the layout plot. The digital control part occupies about one half of the left border structure and includes all the modules described in section 4.6. It can be seen, that the digital standard cells are arranged in vertical columns separated by the routing channels. This part is surrounded by the digital input/output pads which are mainly realized by AMS standard I/O cells. They provide ESD[14] protection and, in case of output pads, CMOS and TTL drivers with diverse strengths. However, a few pads have been modified: The low voltage differential transceiver of the high speed serial interface, a power-on reset and additional pull-up or pull-down resistors are included in the pad structures.

The bias generation block with 19 output buffers for the individual voltages is directly attached to the digital part. By this means, the required control signals for the integrating DAC and the sample and hold stages can be realized with short connecting lines. The next large building block is given by the ADC which is described in appendix A. It provides a resolution of 10 bit and a sample frequency of 8 MHz corresponding to the maximum pixel rate. Below the ADC, the readout components with a number of operational amplifiers and the output mixing stage can be seen. These analog structures are surrounded by the analog input/output pads which also include the ESD protection circuits.

The sensor array itself, which is partly shown on the right border of the layout in figure 4.49, is enclosed by the row selection circuits at the left, the calibration circuits at the top and the readout multiplexer at the bottom. The corners include complementing structures like clock generators or the adjustable reference current mirror.

[14]ESD means electro-static discharge, which could cause unrecoverable damage of the internal chip structure (gate oxide breakdown).

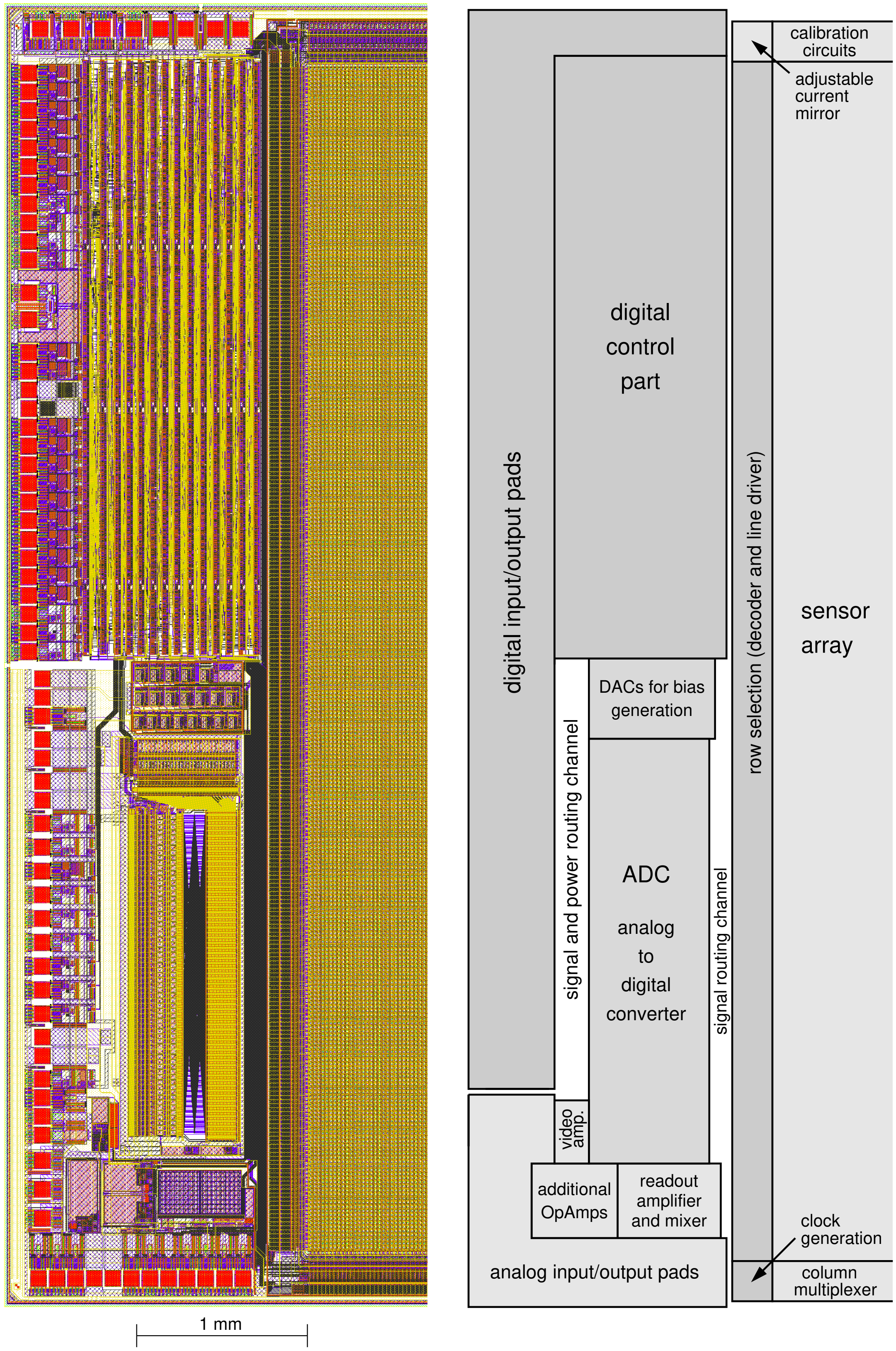


Figure 4.49: Layout and floor plan of the left sensor part including all structures besides the sensor array.

The indicated routing channels are required to assimilate either the digital control lines of the column multiplexer and the video mixer or the signal lines to the separated digital input/output pads. The total number of digital pads amounts to 57, the number of analog pads to 34. It should be mentioned, however, that only a fraction of these signals have to be connected depending on the actual application. The minimum number of bond wires required for video mode operation is 22, composed of 16 power lines, 2 clock oscillator inputs, 3 control lines for the serial interface and the analog output signal.

4.9 Camera system

To demonstrate and to measure the functionality of the developed image sensor, a complete camera system including the sensor, a few external electronic components, a small lens and a camera housing has been built. It provides a 10-pin jack for connecting the camera to the power supply and to the readout system which can use either the analog output signal (e.g. video device or edge detection chip) or the digital output signal (e.g. digital image processing). In addition, three buttons for controlling the corresponding interface are implemented and can be operated from the backside of the camera.

Figure 4.50 shows the schematic diagram of the external (i.e. off-chip) camera electronics. The supply voltages of the analog and the digital part are separately generated by 5 V voltage regulators in order to avoid noise coupling through the power lines. An additional RC-delay eliminates possible fluctuations on the supply cable and leads to a further decoupling of the two supply voltages. Blocking capacitors are used to compensate for sudden variations of the consumed sensor current.

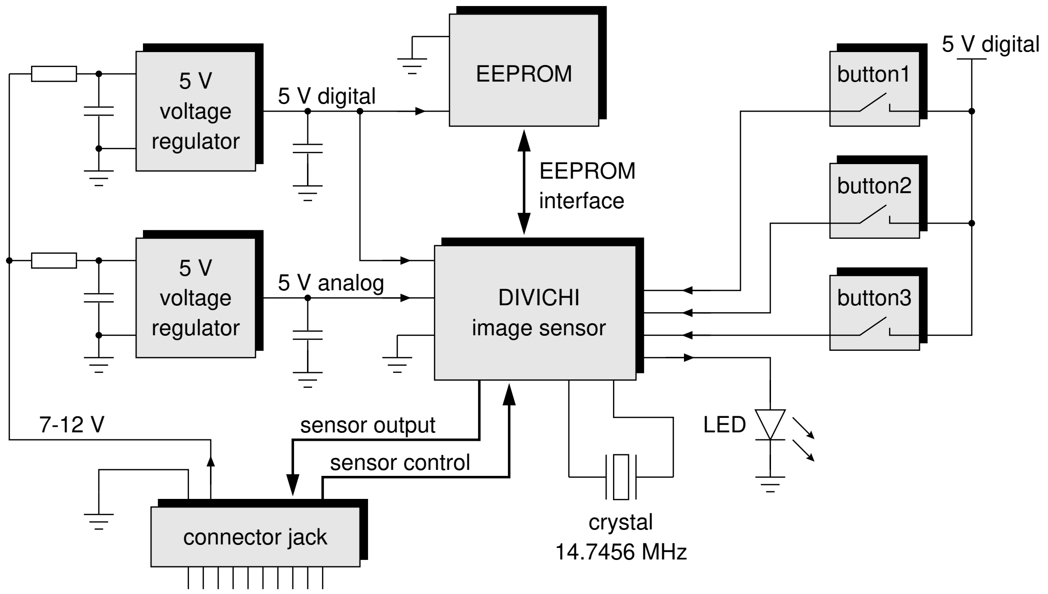


Figure 4.50: Schematic diagram of the camera board including voltage regulation, EEPROM, quartz crystal and the control buttons.

For generating the main clock signal with a frequency of 14.7456 MHz, an external quartz crystal is used. The oscillator circuit additionally required for the clock generation is realized by an analog standard cell of the AMS library [AMS98-3]. It is located at the clock input/output pins on the chip. The three control buttons are supported by one light emitting diode (LED) which indicates the currently selected sensor command. It is only switched on, if the first command, namely *digital zoom*, is selected. The connector jack allows to change between two operation modes: either providing the analog output line and the unidirectional serial interface for programming the chip or enabling the low voltage, bidirectional serial interface with digital readout. Both modes are selected by using small jumpers for connecting the corresponding signal lines on the camera board.

All components are placed on a 23×23 mm^2 PCB[15] shown in figure 4.51. On the frontside (left image) two connectors with 21 pins each can be seen. They are used to connect the camera board to the sensor chip which is bonded on a separate PCB. By this means, different chips can be tested with the same main board. The quartz crystal and some tantalum capacitors and resistors represent the residual components on the frontside. The backside contains the connector jack (black cube) and the control buttons. The EEPROM and the voltage regulators are not visible since they are located between the board and the jack due to their flat package.

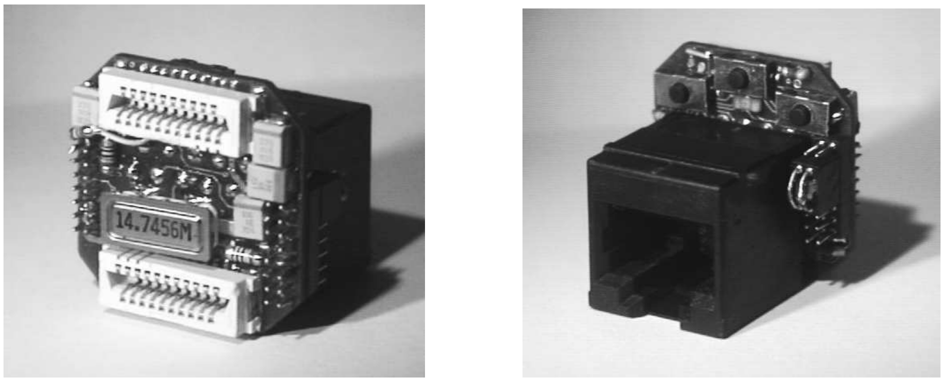


Figure 4.51: Camera board containing the external electronics. The black cube in the right picture represents the jack for connecting the camera cable.

Figure 4.52 contains a photograph of the sensor board which has to be plugged into the camera board. It includes the image sensor on the frontside (left picture) and a few ceramic capacitors together with the board connectors on the backside (right picture). The sensor PCB as well as the

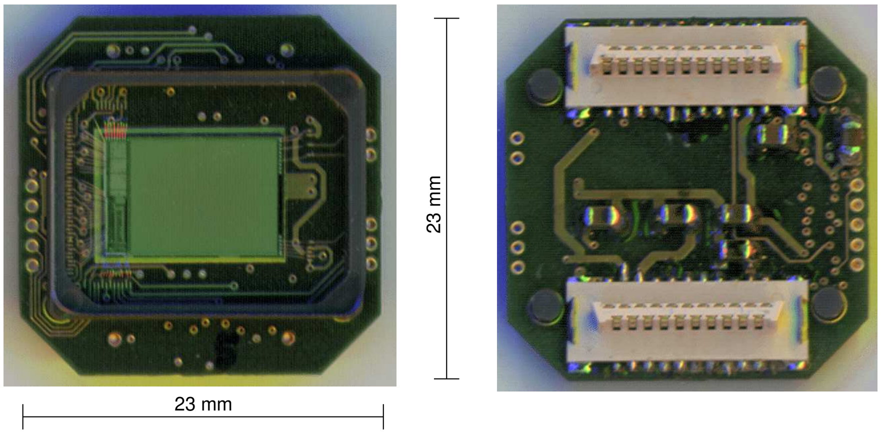


Figure 4.52: Image sensor board with the camera chip directly bonded on the PCB. On the back side, the contact rows for connecting the sensor board to the camera board can be seen.

[15] printed circuit board

main camera PCB are realized as a four layer board. Only the top and the bottom layer are visible since the middle layers are shielded by the outer ones. In order to protect the camera chip and the bond wires, a glass lid is mounted above the sensor and its surroundings. A plastic frame, which has been glued to the little plate of glass, guarantees a minimum distance between chip surface and lid. It can be seen in the left picture of figure 4.52.

Using the camera board, the sensor board and a lens, the camera would be complete. However, a stable housing for the electronics and the lens should be added, on the one hand to shield the sensor against light coming from other directions than the lens and, on the other hand, to protect the whole system from other environmental influences. Therefore, a matching housing has been designed providing a thread with a diameter of 17 mm (M17) for the lens and three holes on the backside for the control buttons. It is made of aluminium and consequently has a relatively low weight. A mechanical adapter allows to connect any standard C-mount lens to the camera.

The complete camera is shown in figure 4.53. It is 25 mm wide and 35 mm long. The applied lens possesses a focal length of 14 mm resulting in a viewing angle of about 40°. The aperture number (focal length divided by the aperture diameter) is 3.5 corresponding to a diameter of 4 mm. The backside of the camera shows the connector jack and the buttons for controlling the selectable parameters. The middle button is made of Plexiglas and transports the light of the LED mounted on the camera board to the outside.

Figure 4.53: The complete camera housing including lens and control buttons. Without lens, the length is 35 mm. The diameter amounts to 25 mm.

All components forming the image sensor system can be seen in the photograph of the disassembled camera in figure 4.54. The middle part shows the two boards containing the camera electronics and the image sensor. The right part contains the lens and the aluminium housing with the lens thread. A small additional thread (3 mm diameter, M3) on the top side and the bottom side allow to fix the camera on an external mounting. The left part of the picture includes the back cap of the housing and the pins for controlling the buttons on the camera board. It is apparent, that the right pin is made of a transparent material. It consists of polished Plexiglas. The light penetrating into this pin at one side is totally reflected at the inside of the pin border. At the opposite end, the angle between surface and light beam is higher than the angle required for total reflection. Here, the light leaves the pin and can be observed. In the camera, the Plexiglas pin is used for the middle button transferring the light of the corresponding LED indicating the currently selected command.

Due to the implemented EEPROM, whose values are automatically loaded after a power-on reset, the camera is ready for operation as soon as the power cable is connected to the integrated jack. This allows to use it as an independent device without any need for an external control device like

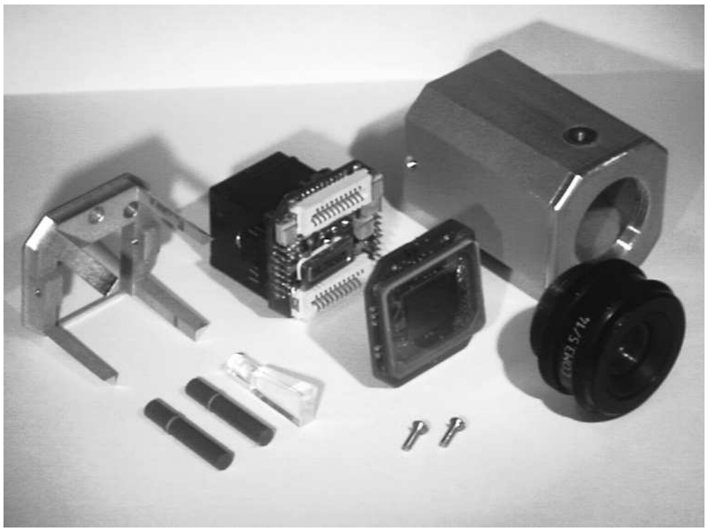


Figure 4.54: The completely disassembled camera.

a microcontroller or a computer. The mechanical length of the camera could be shortened by about 1 cm by not using the 10-pin connector and fixing the cable directly on the camera board. By this means, however, the flexibility would be limited since different cables are required for analog and digital readout. This solution can only be applied, if the camera will be operating either in the digital or in the analog mode all the time.

Chapter 5

Measurements

The final chapter refers to the measurement setup and to the results obtained by the realized image sensors. At first, the test hardware and software as well as the optical setup is described. Then, the measurements of the response curve and the remaining fixed pattern noise are presented. The individual contributions to the total fixed pattern noise like column-to-column variations are separately examined. Additional results concerning temporal noise, crosstalk and discharge of the storage capacitors by parasitic photocurrents subsequently follow. Finally, a few camera images of Divichi illustrating the properties like high dynamic range, pixel averaging and digital zoom are shown.

Most of the measurement results presented within the scope of this chapter correspond to the image sensors Vichideo and Divichi. Both vision chips contain the same pixel types but provide different resolutions. Results of the prototype sensors Vichi and Oasys_vichi were already presented in the previous chapters 3 and 4. Therefore, only a few additional measurements will follow on some of the next pages. However, before describing the image sensor performance, some comments on the measurement setup concerning test hardware, test software and optical equipment are necessary.

5.1 Measurement setup

The test setup for the image sensors in all considered case consists of a PC with integrated data acquisition system, individually adapted control software written in C++ and optical components like light sources, neutral density filters and diverse focusing and defocusing lenses. The PC works as the control device allowing to program the camera, to present the acquired image data on the computer display and to save the data on a harddisk for further analysis. However, sensitive analog measurements have to be carried out very carefully due to the possible distortions caused by the computer.

5.1.1 Test hardware

Except for the last sensor Divichi, all measurements were realized with a data acquisition card of National Instruments [NAT97]. It provides 16 analog input channels with a maximum sampling rate of 1.25 MHz and a resolution of 12 bit. In addition, two analog 12 bit outputs with a maximum update rate of 1 MHz and 8 digital, free-programmable I/O lines are available. The card is connected to the internal PCI[1]-bus. All functions can be controlled in the programming language C using special library functions belonging to the standard installation of this data acquisition system. A lot of different routing and trigger options concerning the individual signals on the PC card result in a high flexibility.

The readout of the image sensors is realized by configuring the 12-bit ADC in a way that it starts operating at the rising edge of the FRAMESTART signal and takes a sample every falling edge of $\overline{\text{VALDRY}}$ (new pixel value ready). The generated digital data is automatically transferred to the PC memory by the corresponding C-function. When reaching the end of the current frame, the readout function returns to the main program. Subsequently, the acquired data can be processed or saved on the harddisk. The internal sensor parameters are changed with the help of the serial interface. The corresponding signals are connected either to the digital I/O lines of the PC card or to the data lines of the parallel PC port. In any case, the different signals can be individually controlled by the software in order to produce the correct timing.

Test board architecture

Regarding the final image sensor, the pixel rate of 7.5 MHz is too high for being sampled with the 1.25 MHz ADC. Furthermore, the counterpart of the low voltage differential serial interface has to be integrated in the computer to be able to read out the digital pixel data. Since the data rate of this interface amounts to 120 Mbits/s, the digital I/O lines of the data acquisition card providing several 100 kbits/s are much too slow. For this reason, a new control and data acquisition system has been developed. It is composed of a commercial PCI card including an FPGA[2], additional RAM and some extension connectors for further electronics and a self-designed PCB with ADC, DAC, low voltage differential transceivers and a number of disposable digital I/O lines.

The PCI card is produced by the company *Silicon Software* and is called *microEnable* [MIC99-1]. It contains a PCI bridge chip converting the PCI protocol into a simpler local bus protocol. The FPGA is implemented as a Xilinx XC4036 [XIL99] including 1296 configurable logic blocks (CLB). This chip provides a high flexibility since it can perform any logic function fitting into the gate array. 64 I/O lines of the FPGA are fed to two CMC[3] connectors and can be used for controlling external electronics. The microEnable additionally includes 2 MB RAM and supporting clock generators. Two independent clock signals are available adjustable in the range of 1 to 40 MHz and 1 to 120 MHz, respectively.

The required additional components like differential transceivers and ADC are integrated on a separate board. It contains the counterpart of the CMC connectors and can be plugged onto the microEnable board. Figure 5.1 shows the corresponding block diagram. Three different connectors accessible on the backside of the computer (extension slots) allow to connect the digital or analog camera signals (6-pin or 10-pin jack) or to control further electronics via the 30-pin jack. The 6-pin jack provides two power lines and the two differential signal pairs corresponding to the high speed serial interface. The differential signals go to the transceiver chips (DS36C200 [NAT98]) converting them into TTL signals. In order to determine the phase between data and clock, two adjustable delays are inserted in the data signal path. The upper one influences the incoming data, the lower one is responsible for the outgoing bitstream. Finally, the signals reach the CMC connectors guiding them to the microEnable board. The 10-pin jack provides the power supply, the unidirectional serial interface and some additional control lines (e.g. FRAMESTART, RESET).

[1]Peripheral Component Interconnect
[2]Field Programmable Gate Array
[3]Common Mezzanine Card

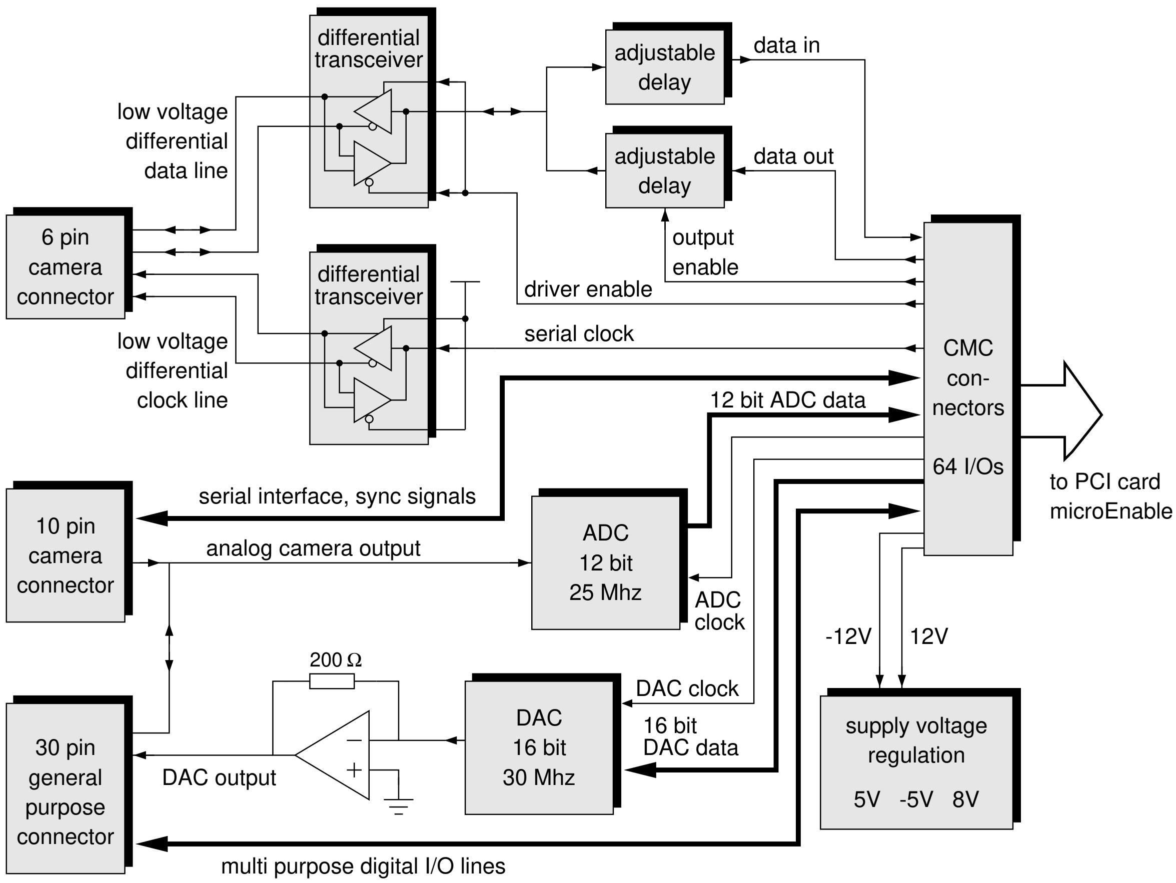


Figure 5.1: Block diagram of the test board, realized as a common mezzanine card (CMC) connected to the microEnable FPGA card.

The ADC has been implemented as a device with 12 bit resolution and 25 MSamples/s [BUR96]. Its input is connected to the analog camera output. The digital ADC data is fed to the FPGA for being stored in the microEnable RAM or being directly transferred to the PC. The digital-to-analog converter is integrated for generating a precise analog output voltage. It provides 16 bit resolution and an update rate of 30 Msamples/s [ANA96]. As it produces an output current, a subsequent transimpedance amplifier converts the current into a corresponding voltage available at the 30-pin general purpose connector. The DAC is controlled by the FPGA together forming an arbitrary waveform generator. A possible application is given by the evaluation of the ADC integrated on the image sensor requiring specific analog input patterns.

In addition, diverse voltage regulators and blocking capacitors for generating the analog supply voltages 5 V, -5 V and 8 V can be found on the test board. The PCB has been realized using four routing layers. The two middle layers include large ground planes shielding the sensitive analog electronics against the noisy computer environment.

FPGA programming

The FPGA integrated on the microEnable represents the main control component in the signal path between camera and PC. It is responsible for serving the different interface protocols (e.g. local bus to PCI chip, low voltage differential camera interface, RAM) and for controlling the ADC and DAC on the test board. The principal block diagram of the functionality implemented in the FPGA is shown in figure 5.2. It consists of the main control part and six sub-modules. Thick lines refer to signal paths containing more than one bit, whereas thin lines always correspond to a single signal line. The complete design is written in the hardware description language VHDL[4] [VHD97] and subsequently converted into a digital circuit (gate level equivalent) by the synthesizer program *synopsys* [SYN98]. Finally, a software tool corresponding to the applied Xilinx FPGA maps the circuit to the internal FPGA structure. It generates a bitstream which has to be transmitted to the Xilinx chip in order to configure the internal logic blocks and their connections to each other.

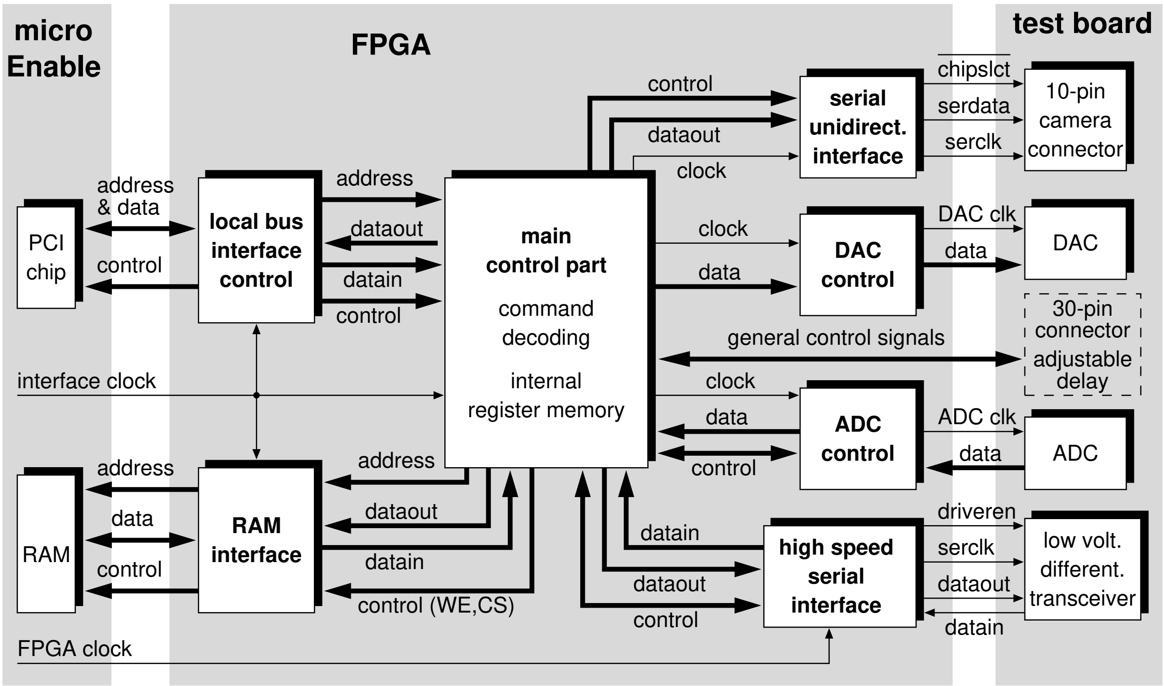


Figure 5.2: Block diagram of the control logic implemented in the FPGA.

The main control part performs the communication between the residual modules and decodes the commands coming from the PC for setting different operation modes or writing data to the camera. The interface modules controlling the RAM and the local bus between the PCI chip and the FPGA are provided by the microEnable VHDL library [MIC99-2]. The RAM module converts the external asynchronous protocol into a synchronous protocol with one or two waitstates. The local bus module splits address and data signals, which are transmitted from the PCI chip via the same physical lines, into separated address, datain and dataout signals.

The serial interface part is responsible for controlling the unidirectional serial link to the camera chip. It gets 14 bits of parallel data and, using a 14 bit shift register, transforms them into a serial bitstream. Additionally, the corresponding clock and chipselect signals are generated in order to comply with the required interface protocol. The DAC and ADC modules determine the sample rates and transfer the sampled data values from the ADC to the main module or from the main module to the DAC. The ADC values can be either stored in the microEnable RAM or directly transmitted to the PC memory.

[4]VHDL: VHSIC (very high speed integrated circuit) hardware description language

The final sub-module refers to the bidirectional, low voltage differential camera interface. It also contains a shift register for converting serial into parallel data and vice versa. Since a new data bit is valid at every edge of the serial clock, two shift registers are used. The first one shifts the register bits at the rising edge, the second one at the falling edge of the clock signal. Finally, the values of both register types are combined to obtain the parallel data. As the microEnable provides two independent clocks, different clocks are used for the control module of the bidirectional serial interface and for the other parts. By this means, the transmission rate can be adjusted independently of the general system clock.

5.1.2 Test software

The software for controlling and measuring the different image sensors is included in a larger program system called Visor which is used for all tasks within the tactile vision project (image acquisition, image processing and control of the tactile displays). It is written in C++, runs under windows 95/98 or windows NT and shows a high flexibility concerning any additional extensions. The Visor routines providing the basic functionality like general image processing algorithms and real-time image presentation on the computer display were written by J. Schemmel [SCH97]. By and by, the complementing functions for controlling special hardware or for performing more complex image processing tasks have been added by the different members of the vision project.

Figure 5.3 shows the graphical user interface of the Divichi control software implemented in the Visor program. The upper right window in the background represents the main program window,

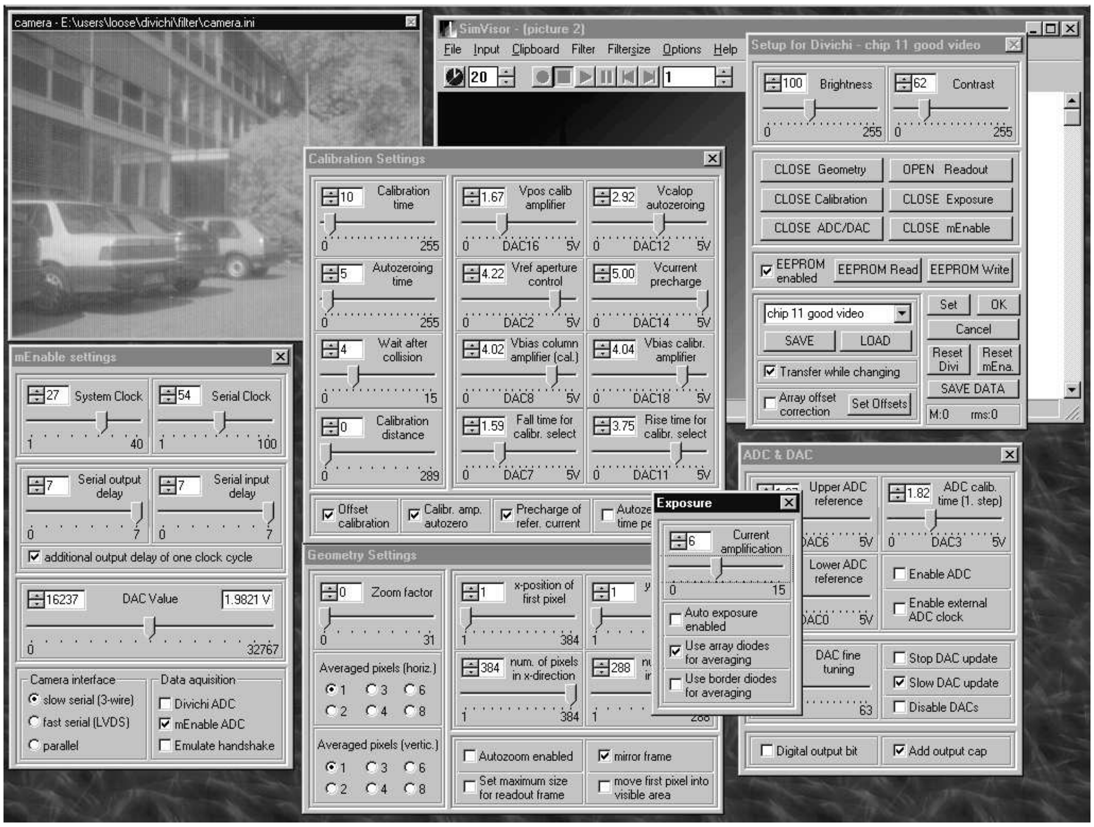


Figure 5.3: Control software for the Divichi camera. The main window, the camera image and some control windows for adjusting the sensor parameters are shown.

the upper left window contains the acquired camera image. The other windows correspond to the special camera control part linked to the Visor main program. It allows to adjust the individual sensor parameters and to control the FPGA behaviour. The diverse input elements are arranged in different windows depending on their functionality. The windows corresponding to the calibration, geometry, auto-exposure, ADC & DAC and microEnable settings can be seen, whereas the window for the readout settings is not shown. The complete parameter sets can be saved in order to allow different reproducible test setups.

The camera control part of the Visor software has to communicate with the hardware components controlling the analog sensor readout and the diverse digital interfaces. This hardware can be either the data acquisition card applied for the first three sensor evaluations or the microEnable board in the case of the Divichi camera chip. Both systems provide C functions for configuring the individual components and for transferring data from the acquisition system to the PC memory and back. These functions make it possible to easily communicate with the corresponding hardware components. For the measurements, the analog sensor values are converted by any of the ADCs (depending on the acquisition system and the image sensor), transmitted to the PC and finally stored on the harddisk for further analysis. Besides, a few calculations like determining the mean and rms values are directly performed in the control software in order to reduce the size of the data files.

5.1.3 Optical setup

The camera chips represent a sensor system converting optical into electrical information. Therefore, most of the sensor measurements require a possibility to optically stimulate the image sensors. For this reason, the measurements were carried out in an optical laboratory providing different kinds of light sources like monochromatic laser light or white light from arc or halogen lamps. To achieve the high dynamic range necessary for evaluating the logarithmic photoreceptors, a number of neutral density filters were used. Each of them attenuates the light intensity by a definite factor. By applying more than one filter, the attenuation factor should correspond to the product of the individual factors. However, this has to be verified because a part of the incident light is reflected instead of being absorbed. Regarding two filters, a fraction of the photons penetrating the first filter is reflected at the second one. A part of these photons is reflected again at the first filter and subsequently reaches the second filter again. Consequently, more light than expected will go through the filter system. This effect can be reduced by turning the filters a little resulting in a smaller angle than 90° between the filter surface and the optical axis.

The properties of the applied neutral density filters have been examined in [TEO97]. The incident light was generated by a 675 nm diode laser whose absolute intensity was measured by a calibrated photometer. The attenuation factors given by the ratio of transmitted intensity J_{trans} to incident intensity J_{inc} are shown in figure 5.4. The scale of the y-axis refers to the percentage of the attenuation ratio. The values correspond to eight different neutral density filters each reducing the intensity by a factor of about 10. The individual deviations from this ideal factor are relatively low and in any case stay below $\pm 3\,\%$.

Figure 5.5 shows the behaviour of a light beam attenuated by maximal 4 filters in series. The incident intensity amounts to 505 W/m^2 going down 0.054 W/m^2 after passing the filter system. This means, that the difference between the ideal value (i.e. 0.0505 W/m^2) and the measured value is about $7\,\%$. Since most of the individual filters show an attenuation ratio of less than 10 %, a total reduction of somewhat more than 10^4 in the case of 4 filters may be expected. However, the measured value is smaller than the ideal one. As mentioned above, this behaviour comes from the multiple reflections in the space between the different filters. It should be mentioned that the overall attenuation factor is very sensitive to the measurement setup. It has to be guaranteed that the filter system is not aligned exactly in the same direction as the light beam in order to suppress multiple reflections.

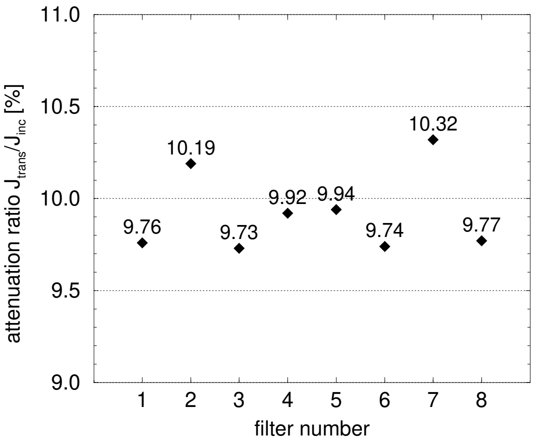


Figure 5.4: Attenuation factors of the eight neutral density filters used for the sensor measurements [TEO97].

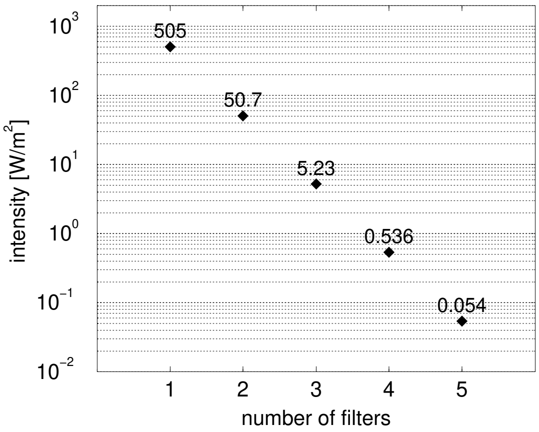


Figure 5.5: Intensity attenuation of five neutral density filters in series [TEO97].

The neutral density filters presented in the previous paragraph were used for measuring the image sensor properties in a dynamic intensity range of 8 decades. Due to the error of 7 % with respect to 4 filters, an error of less than 15 % can be expected in the case of using 8 filters. Since the response curves are always calibrated to an absolute value (photometer) lying in the middle of the applied intensity range, the error at the upper and lower end of the intensity scale should not exceed 8 %. In the following measurement, this error has to be kept in mind when estimating the overall errors of the acquired results.

Two different light sources were used for stimulating the image sensor chips: a red diode laser ($\lambda = 675$ nm) with a maximum power of 10 mW and a xenon arc lamp emitting a relatively homogeneous white spectrum with a few peaks in the near infrared [ORI94]. The laser can be focussed to a very small light spot (diameter $\approx 5\,\mu$m) allowing to stimulate individual photodiodes. Before focusing the laser beam onto the chip, it goes through a spatial filter eliminating all disturbing border effects around the laser beam. For this purpose, the beam is focused by a lens and passes a small aperture with a diameter of $5\,\mu$m. Afterwards, it is transformed back into a parallel beam finally being focused onto the sensor chip.

The arc lamp was used to measure the homogeneity of the complete pixel array. It is able to generate a large light spot covering the whole sensor area. In order to guarantee a homogeneous illumination, the fixed pattern noise measurements were carried out in most cases not by using the arc lamp's direct light but by inserting a diffuse reflector and using the reflected light.

5.2 Photoreceptor response and fixed pattern noise

The following sections describe the measured behaviour of the self-calibrating photoreceptors with respect to the incident light intensity J. In the field of electronic cameras, a different quantity for expressing the actual light power is often used: the illuminance with the unit *lux*. The illuminance represents a photometric quantity corresponding to the spectral sensitivity of the human eye, whereas the light intensity (or irradiance) is a more physical quantity. The exact correlation between physical and photometric quantities is given in appendix D.

Most of the following measurement results describe the output voltage of the sensor chips as a function of the incident intensity. It should be mentioned that the absolute value of the output voltage has no meaning as it can be shifted to any value by changing either the pixel reference voltage or the multiplexer reference voltage. Only differences of the voltage signals correspond to the receptor sensitivity. They have to be regarded for the comparison of the photoreceptor response with the sensor fixed pattern noise.

5.2.1 Response curves

The photoreceptor response as a function of the light intensity was measured in a dynamic range of 8 decades. The pixels were illuminated by the white light of the xenon arc lamp. Figure 5.6 shows the response curves corresponding to two different single photoreceptors of the image sensor Vichideo. This chip contains the same pixel types as the larger sensor Divichi, but provides a resolution of only 96×72 pixels. In a dynamic range of six decades, the photoreceptors show the expected logarithmic behaviour. The output voltages of both pixels differ somewhat from each other due to the remaining offset variations. However, it is apparent, that both curves are nearly parallel. This confirms the low slope variations already measured with the test chip in figure 2.7.

The averaged response curve of all 6912 pixels can be seen in figure 5.7. It is obtained by illuminating the sensor array homogeneously at a definite intensity and plotting the mean value of all pixel outputs. As expected, the averaged curve shows the same behaviour as the individual pixels with a usable dynamic range of 6 decades. The slope, i.e. the voltage increase per intensity decade, amounts to 105 mV/decade. This value, however, is not a fixed property of the sensor chip, but can be varied in a wide range by changing the gain of the readout amplifier.

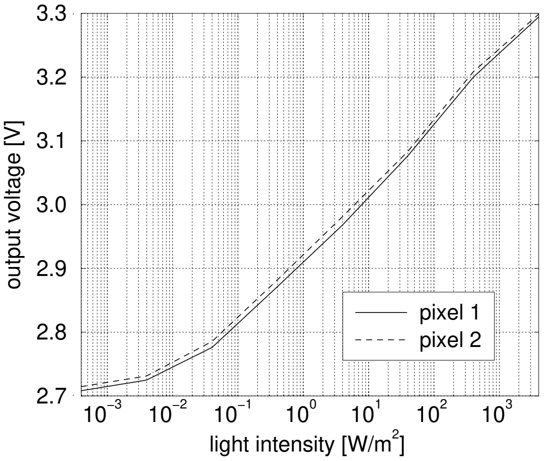


Figure 5.6: Response curves of two single pixels of the image sensor Vichideo.

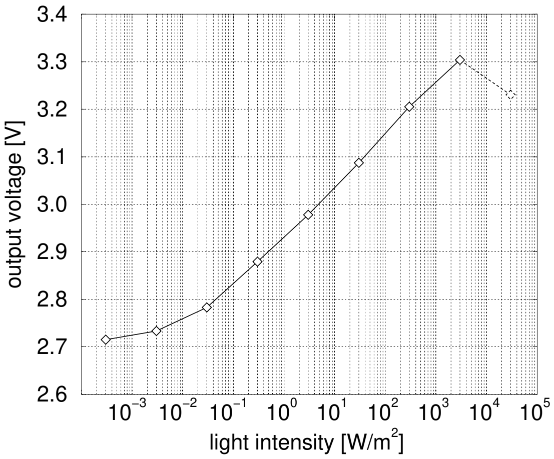


Figure 5.7: Averaged photoreceptor response with respect to all 6912 pixels of the image sensor Vichideo.

The decreasing slope at very low intensities results from the low photocurrents in this region. They reach the value of the diode's dark current representing a fixed offset in the response curve. In addition, due to the low current, the photoreceptor needs more time to charge the parasitic capacitances. Therefore, the pixel has not yet recovered the normal operation level after applying the calibration cycle. The decrease at very high intensities (dashed line) stems from the discharge of the storage capacitors. The metal shielding of the switch transistor isolating the capacitor node, is not perfect. Thus, a parasitic photocurrent arises in this transistor making the capacitor significantly change its voltage before reading out the corresponding photoreceptor. This effect can be reduced by shortening the time between calibration and readout. On the other hand, in this case the relaxation time at low intensities would also be shortened resulting in a limited dynamic range at the lower end of the response curve. The overall dynamic range remains constant, but can be shifted somewhat upwards or downwards.

The sensor response has also been measured for the final camera chip Divichi. The averaged curve of all 100k pixels is shown in figure 5.8. Again, the dynamic range of six decades with the characteristic drop at high intensities and the saturation at low illuminations can be observed. In order to examine the transition region from the positive to the negative slope at about 5000 W/m^2, more measurement points than available with the neutral density filters were required. Therefore, the intensity of the arc lamp was changed by varying the supply current. Every new intensity corresponding to a new adjustment of the lamp was calibrated with the help of the photometer. By this means, four additional points were measured in the decade from 2 kW/m^2 to 20 kW/m^2. The slope of the response curve, averaged in a range of five decades, amounts to 250 mV per decade.

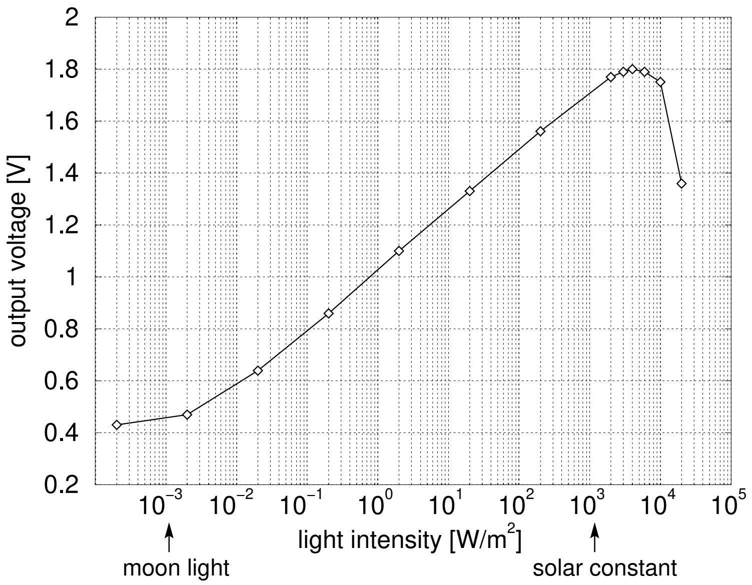


Figure 5.8: Averaged photoreceptor response with respect to all 100k pixels of the image sensor Divichi. The decreasing signal at high intensities results from the discharge of the storage capacitors by parasitic photocurrents.

When regarding the remaining fixed pattern noise in the next section, the results have to be referred to the corresponding slope. This is important in order to obtain a fixed pattern noise value which is independent of the actual slope and can be compared to other results (e.g. from the test chip in section 2.2.2 including one column of uncalibrated logarithmic photoreceptors). Some measurements of Divichi correspond to a different slope than shown in figure 5.8 due to a varied readout amplifier gain. Therefore, the actual slope is always mentioned if it is important for the interpretation of the results.

5.2.2 Remaining fixed pattern noise

The remaining fixed pattern noise was measured using the xenon arc lamp. In each case, the sensor chip was homogeneously illuminated at a definite intensity. The results are presented in two steps: At first, the overall fixed pattern noise is shown corresponding to all pixels of the image sensor. The second step includes the individual contributions like column-to-column variations and non-uniformities within one single column.

Vichideo results

The following figures show the results of the image sensor Vichideo providing a resolution of 96×72 pixels. The fixed pattern noise, i.e. the distribution of the individual pixel offsets at a uniform illumination, has been measured at 3 different light intensities: 30 mW/m^2, 3 W/m^2 and 300 W/m^2. The frame rate was 20 Hz. Figure 5.9 contains the output voltages of all photoreceptors at an intensity of 3 W/m^2. The values are filled into a histogram in order to examine the shape of the distribution. In addition, a Gaussian curve fitted to the acquired data using the least square fit method is shown. The diagram in part a) has a linear ordinate scale, whereas the diagram in part b) presents the same data on a logarithmic scale. The latter graph allows to compare more precisely the behaviour of the very low histogram bins to the Gaussian fit.

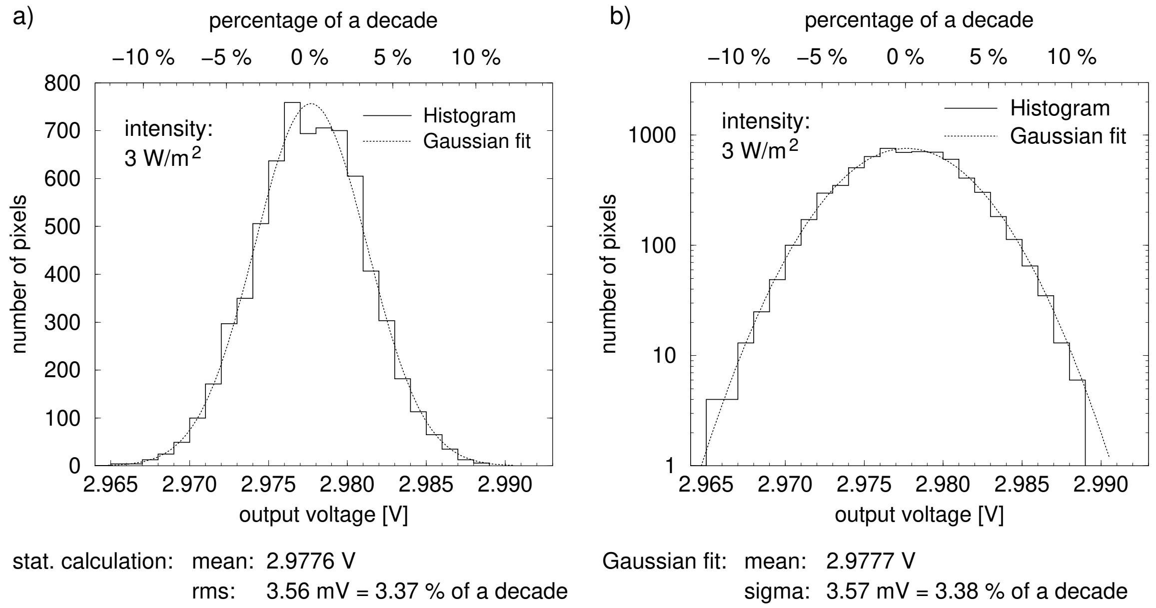


Figure 5.9: Offset distribution of Vichideo at an intensity of 3 W/m^2. A Gaussian function has been fitted to the histogram values to verify the normal distribution of the measurement results. Both diagrams contain the same data with a linear y-axis (left diagram) and a logarithmic y-axis (right diagram), respectively.

It is apparent that the distribution of the pixel offsets resembles the curve of the Gaussian fit. Even at very low values, there is a relatively good matching between the ideal normal distribution and the measured values. This is also confirmed by the characteristic parameters written below the diagrams: the width and the mean value of the offset distribution. The left values (stat. calculations) are calculated applying the statistical mean and rms formulas to the measured data. The right values are gained from the fitted Gaussian function. The mean values as well as the rms value (or sigma) show nearly the same results. The rms values are not only given in mV but also as the percentage of one intensity decade. This percentage is obtained by dividing the rms value by the slope of the response curve which is 105.6 mV/decade.

The width of the offset distribution is relatively small compared to an uncalibrated logarithmic image sensor. The results of the uncalibrated test column in section 2.2.2 show an rms value of 90 % of a decade. Therefore, the remaining variations with a sigma of 3.37 % of a decade represent a reduction of the fixed pattern noise by a factor of 27. Regarding the peak-peak values, the variations increase to about $\pm 10\,\%$. This number, however, is not only a property of the distribution itself, but additionally depends on the total number of pixels. The more pixels which are regarded the higher the probability of getting large peak-peak values. Therefore, it is important that the $\pm 10\,\%$ correspond to a resolution of about 7000 pixels.

Figure 5.10 shows the offset distributions measured at an intensity of 300 W/m^2 (left diagram) and at an intensity of 30 mW/m^2, respectively. The rms values of 3.94 % and 3.22 % are similar to the results of the medium intensity of 3 W/m^2 (figure 5.9). The small difference can be explained with the help of the slope variations. If the sensor is calibrated with a reference current corresponding to a definite intensity, the fixed pattern noise increases towards higher and lower intensities. This property stems from the slightly different slopes of the individual pixels. The measurement results dealing with the slope non-uniformities will be presented in section 5.2.4.

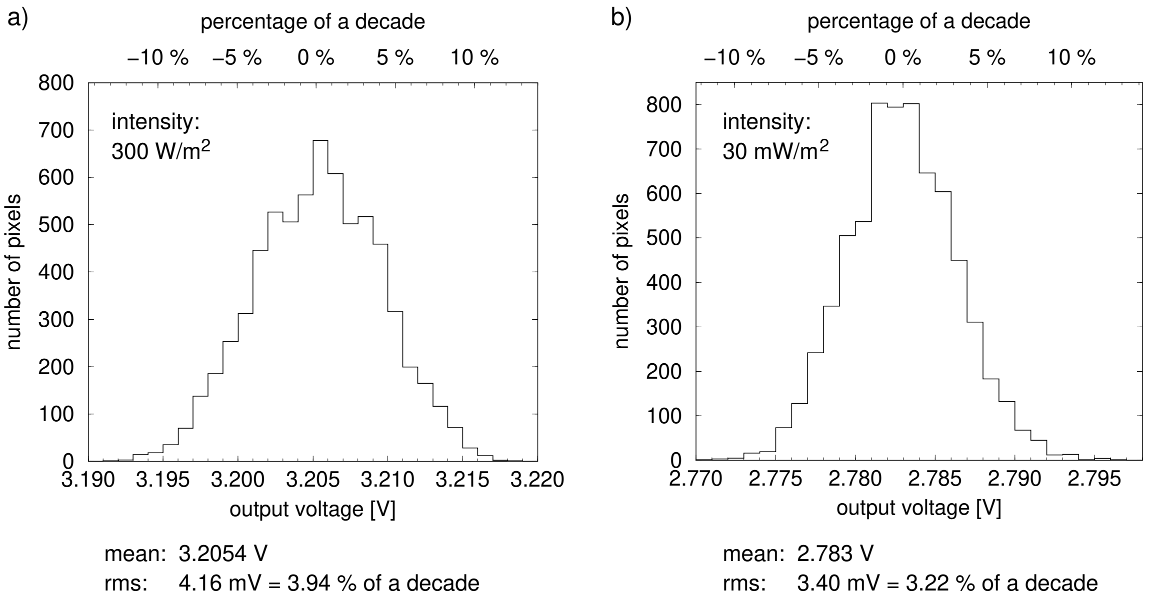
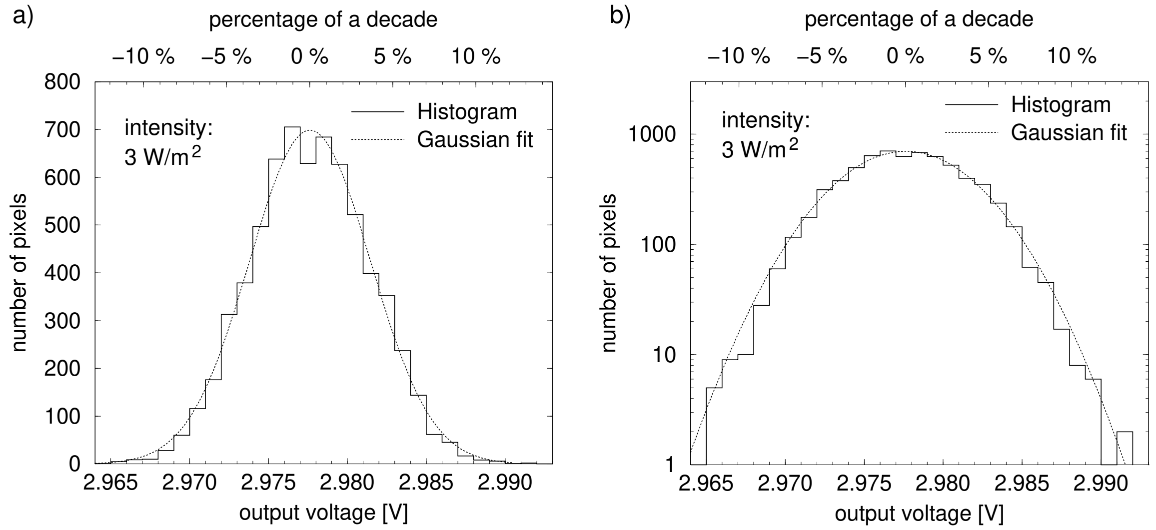


Figure 5.10: Offset distribution of Vichideo at an intensity of 300 W/m^2 (left diagram) and at an intensity of 30 mW/m^2 (right diagram).

So far, only measurement results of one die have been regarded. In order to ascertain if the observed behaviour is typical, another Vichideo chip was examined. The measured offset distribution as well as the corresponding Gaussian fit can be seen in figure 5.11. The left diagram shows a linear ordinate scale, the right diagram a logarithmic one. Again, the histogram values match the fitted curve well. The mean value of the statistical calculation is almost the same as the Gaussian mean value, and the two sigmas also differ only a little from each other. Compared to the first die in figure 5.9, the rms value of 3.54 % of a decade is slightly higher. The peak-peak values are also somewhat increased and amount to $\pm 12\,\%$ of a decade. Summarizing the results, two properties can be concluded: The offset distribution of Vichideo shows a Gaussian shape and the remaining fixed pattern noise stays below 4 % of a decade.



stat. calculation: mean: 2.9777 V
rms: 3.73 mV = 3.54 % of a decade

Gaussian fit: mean: 2.9776 V
sigma: 3.84 mV = 3.65 % of a decade

Figure 5.11: Offset distribution of a different Vichideo die at an intensity of 3 W/m^2. The data is shown together with a Gaussian fit on a linear and a logarithmic y-axis.

Finally, in order to illustrate the importance of a fixed pattern noise correction, a comparison between a calibrated and an uncalibrated image is given in figure 5.12. The contrast between background and the shown ring symbol amounts to about 80 % of an intensity decade. The picture is taken with the camera chip Vichideo. The left image contains the unmodified sensor data. Unfortunately, the self-calibrating pixel concept does not allow to produce an uncalibrated image. Therefore, the

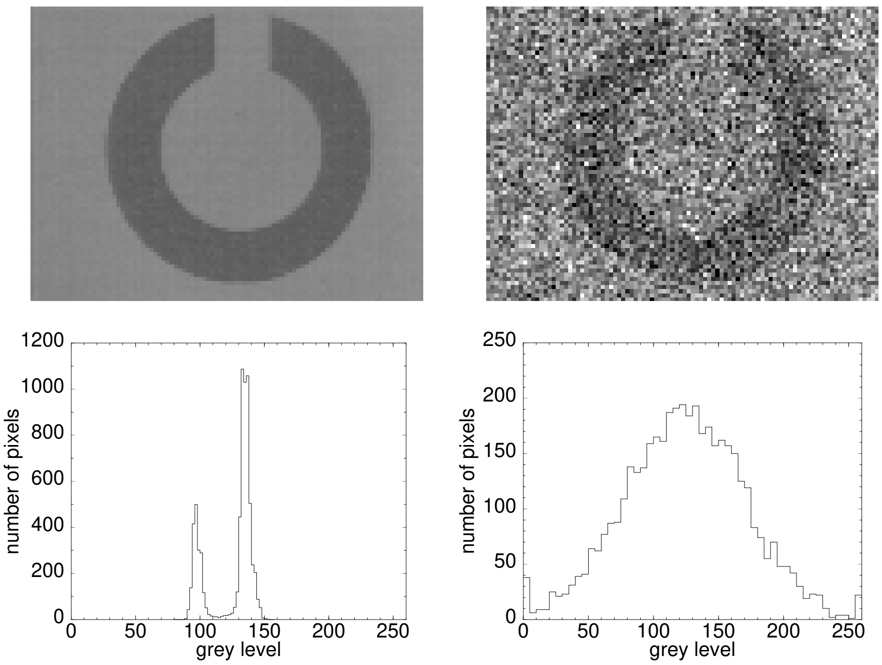


Figure 5.12: Comparison between a calibrated and an uncalibrated image. The left one was measured with the image sensor Vichideo, the right one is simulated on the basis of the test results in section 2.2.2.

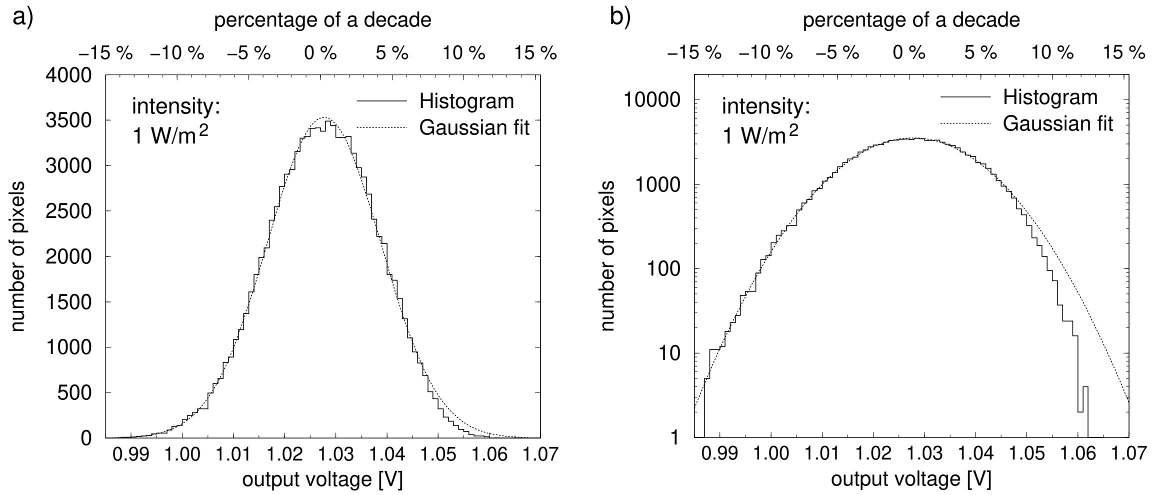
right picture includes additional noise gained from a simulation on the basis of measurements. The simulation assumes a normal distribution with a sigma of 90 % corresponding to the measured values of the test column in section 2.2.2.

The two histograms below the images contain the according grey level distributions. The left one shows two narrow peaks referring to the background and the darker ring symbol. The right histogram only includes one single wide peak which means that the background and the symbol disappear in the fixed pattern noise. The small peaks at the left and right side of the right histogram correspond to overflowing values. Due to the spatial correlation of the pixels belonging to the symbol, the human eye is still capable of detecting the ring structure in the corresponding image. Image processing algorithms, however, would run into severe problems when analysing this picture. Therefore, a fixed pattern noise reduction is essential, particularly if regarding even smaller contrasts.

Divichi results

The image sensor Divichi is composed of the same pixel type as Vichideo, but provides a higher resolution of more than 100k pixels. For this reason, the remaining fixed pattern noise after applying the self-calibration should lead to similar results. However, a slightly increased rms value of the corresponding offset distribution can be assumed, since the process parameters show larger variations when regarding larger chip sizes. All measurements were carried out at a frame rate of 50 Hz.

The fixed pattern noise distribution at a medium intensity of 1 W/m^2 can be seen in figure 5.13. The diagram contains the corresponding histograms as well as a Gaussian curve fitted to the measured values. On the linear scale (left diagram) the data seems to be in good accordance with the fitted function. Regarding the same curves on a logarithmic scale (right diagram), a discrepancy at the low histogram bins on the right border becomes apparent. Consequently, the offsets are not exactly normally distributed. The reason for this behaviour is not completely understood and can only be assumed. On the one hand, the process parameters could vary over large distances in a way which does not correspond to a statistical normal distribution. On the other hand, the homogeneous illumination could show slight non-uniformities adulterating the Gaussian shape.



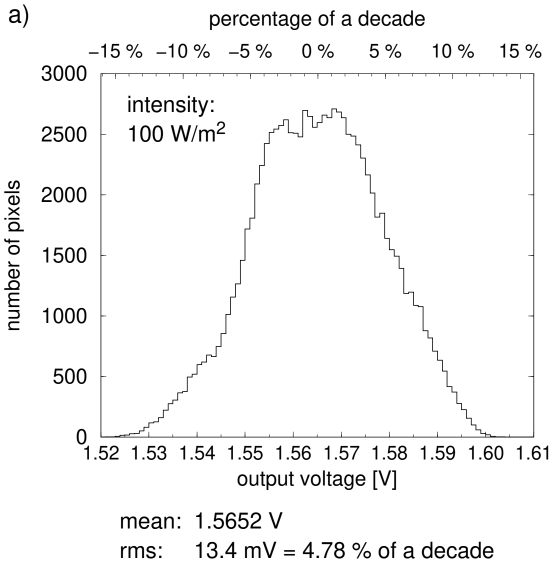
stat. calculation: mean: 1.0270 V
rms: 10.7 mV = 3.82 % of a decade

Gaussian fit: mean: 1.0272 V
sigma: 11.1 mV = 3.96 % of a decade

Figure 5.13: Offset distribution of Divichi at an intensity of 1 W/m^2. A Gaussian function has been fitted to the histogram values to test whether the distribution of the measurement results is normal or not. Both diagrams contain the same data with a linear y-axis (left diagram) and a logarithmic y-axis (right diagram), respectively.

The mean value of both, the statistical calculation and the Gaussian fit, amounts to 1.027 V. The offset distribution is somewhat wider (about 4 %) for the fit than for the direct calculation. This can be attributed to the discrepancy mentioned above. The sigma (or rms) percentages refer to a slope of 280 mV/decade adjusted by selecting the corresponding gain factor of the readout amplifier. As expected, the rms value of 3.82 % of a decade means a slight increase compared to the Vichideo rms value of 3.37 % of a decade (at 3 W/m^2, figure 5.9).

Figure 5.14 shows the fixed pattern noise distribution at an intensity of 100 W/m^2 in part a) and at an intensity of 10 mW/m^2 in part b). In both cases, the rms value is increased compared to the one measured at 1 mW/m^2 in figure 5.13. Hence, the calibration point (intensity corresponding to the applied reference current) is somewhere in between. Due to the slope variations, the offset variations become larger with decreasing or increasing intensities. Again, the rms percentages correspond to a slope of 280 mV/decade. The rms value of 4.78 % of a decade (left diagram) at an intensity of 100 W/m^2 is comparable with the fixed pattern noise increase of Vichideo at 300 W/m^2 in figure 5.10. The relatively high rms value of 8.5 % of a decade in the right diagram can be explained with the high slope variations in the lower intensity range (cf. slope variations in section 5.2.4).



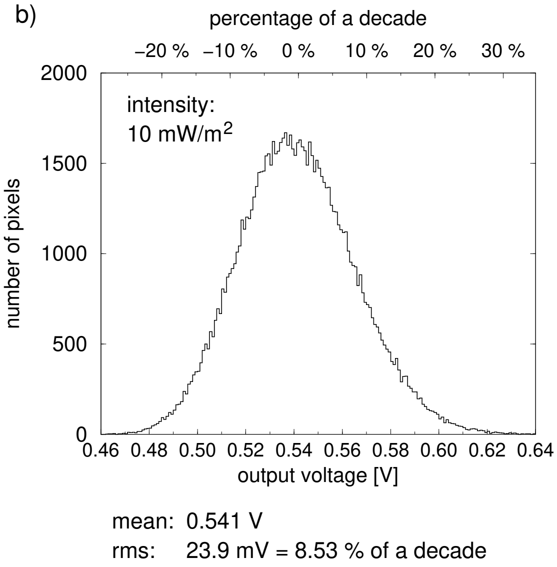


Figure 5.14: Offset distribution of Divichi at an intensity of 100 W/m^2 (left diagram) and at an intensity of 10 mW/m^2 (right diagram).

In order to separate the long range variations from the short range variations, the rms values have been calculated for different subparts of the sensor array. Starting from the total pixel number, more and more rows and columns are omitted until the size of 100×75 pixels is reached. This final resolution is similar to the resolution of the smaller image sensor Vichideo. Here, the fixed pattern noise of both sensor chips should be more or less equal.

The rms values corresponding to the three intensities 10 mW/m^2, 1 W/m^2 and 100 W/m^2 are plotted in figure 5.15 as a function of the number of regarded columns. The number of considered rows can be calculated by multiplying the number of columns with 3/4 due the aspect ratio of 4:3 of all applied subparts. The regarded parts are always concentric to the whole array, only border columns and rows are omitted.

As expected, the fixed pattern noise decreases when reducing the array size. In the case of the two higher intensities, the values corresponding to the 100×75 resolution are very similar to the Vichideo results and amount to values below 4 % of a decade. This confirms the existence of long

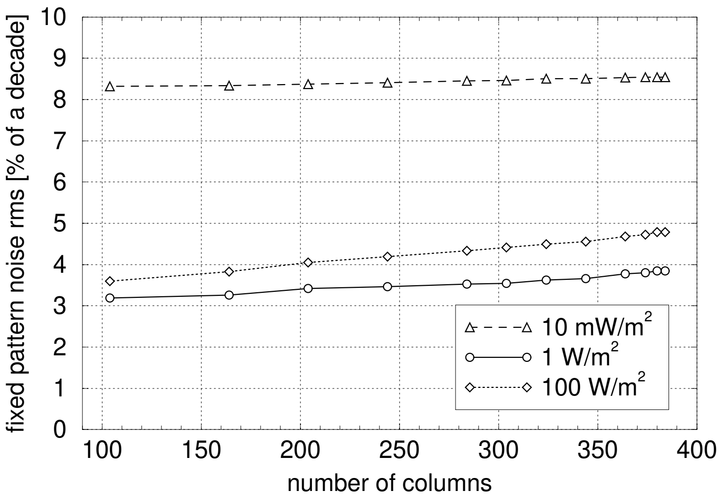


Figure 5.15: Remaining fixed pattern noise as a function of the image size.

range process parameter variations. The rms values of the lowest intensity (10 mW/m^2), however, only show a slight decrease. They always stay above the high level of 8 % of a decade. Again, the high slope variations at low intensities are responsible (cf. section 5.2.4). They are obviously less determined by the long range than by the short range variations of the process parameters.

5.2.3 Composition of the fixed pattern noise

The total fixed pattern noise presented in the last section can be interpreted as a superposition of the pixel-to-pixel variations within one column and the column-to-column variations of the individual column mean values. The latter contribution should be statistically independent[5] of the former one because it is not influenced by the individual pixel offsets but by the column structures like reference current source, calibration amplifier and readout buffer. Therefore, the total fixed pattern noise σ_{tot} should be given by

$$\sigma_{tot} = \sqrt{\sigma^2_{c\leftrightarrow c} + \overline{\sigma}^2_{col}} \tag{5.1}$$

corresponding to the column-to-column variations $\sigma_{c\leftrightarrow c}$ and the mean offset distribution within one column $\overline{\sigma}_{col}$.

Vichideo results

The measurement results already presented in the last section are analysed with respect to the column mean values and the column-to-column non-uniformities. Part a) of figure 5.16 contains the column-to-column variations as a function of the column number (intensity 3 W/m^2). Each value corresponds to the mean value of all pixels belonging to the considered column. Part b) shows the same values filled into a histogram. The width of the distribution, which roughly shows a Gaussian shape, amounts to 2.24 % of a decade with respect to the slope of 105.6 mV/decade.

Regarding the left diagram, two properties can be observed: a large variation on the scale of the whole sensor and a short range variation between odd and even column numbers. The first

[5] A statistical correlation would occur if the individual column rms values vary from column to column. Hence, statistical independence means, that every column shows almost the same standard deviation.

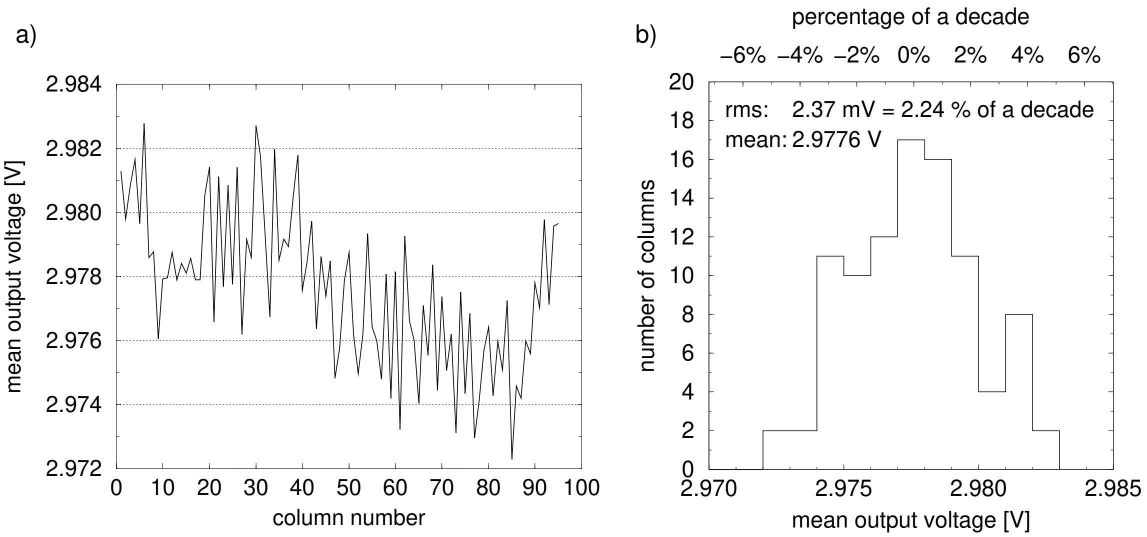


Figure 5.16: Mean of all pixel values within one column as a function of the column number (left diagram) and the corresponding histogram (right diagram). The results refer to the image sensor Vichideo and are measured at an intensity of 3 W/m^2.

behaviour results from the process parameter variations across the die. They influence the performance of the reference current sources, the readout buffers and the calibration amplifier. The second non-uniformity is caused by the readout amplifier of the column multiplexer. As described in section 4.4.1, two different readout lines are used. The feedback loop of the readout amplifier consists of different capacitors for the first and the second line. Since all even columns are read out via the first and all odd columns via the second line, a possible mismatch between the two capacitors would result in the observed behaviour. The mean value of the even columns differs from that of the odd columns by 1.7 mV corresponding to 1.61 % of a decade. This value, however, is not fixed but can be influenced by varying the amplifier gain. By this means, the feedback capacitances are changed (either increased or decreased) and show a different matching behaviour. As the rms value of the distribution corresponding to the even or odd columns is reduced by only a small amount (rms for odd columns: 2.21 % of a decade), this effect of the readout amplifier plays a subordinate role.

The offset variations within the individual columns can be seen in figure 5.17. Part a) contains the column rms values plotted as a function of the column number. Part b) shows the corresponding histogram. Here, no systematic behaviour is apparent. The mean value of 2.46 % of a decade represents, besides the column-to-column variations, the second contribution to the overall fixed pattern noise. If both contributions are statistically independent, the results have to comply with equation 5.1. Substituting them into equation 5.1 yields

$$\sqrt{\sigma_{c\leftrightarrow c}^2 + \overline{\sigma}_{col}^2} = \sqrt{2.24^2 + 2.46^2}\ \%\text{ of a decade} = 3.33\ \%\text{ of a decade}. \tag{5.2}$$

This value is in agreement with the total fixed pattern noise of 3.37 % of a decade, the error amounts to about 1 %. Consequently, both contributions can be considered as independent of each other.

The same calculations have been carried out in the case of brighter and darker illuminations. Table 5.1 summarizes the results according to the three intensities 30 mW/m^2, 3 W/m^2 and 300 W/m^2. It contains the column-to-column variations, the variations within one column and the calculated (equation 5.1) and measured total fixed pattern noise. In any case, the calculated value is very similar

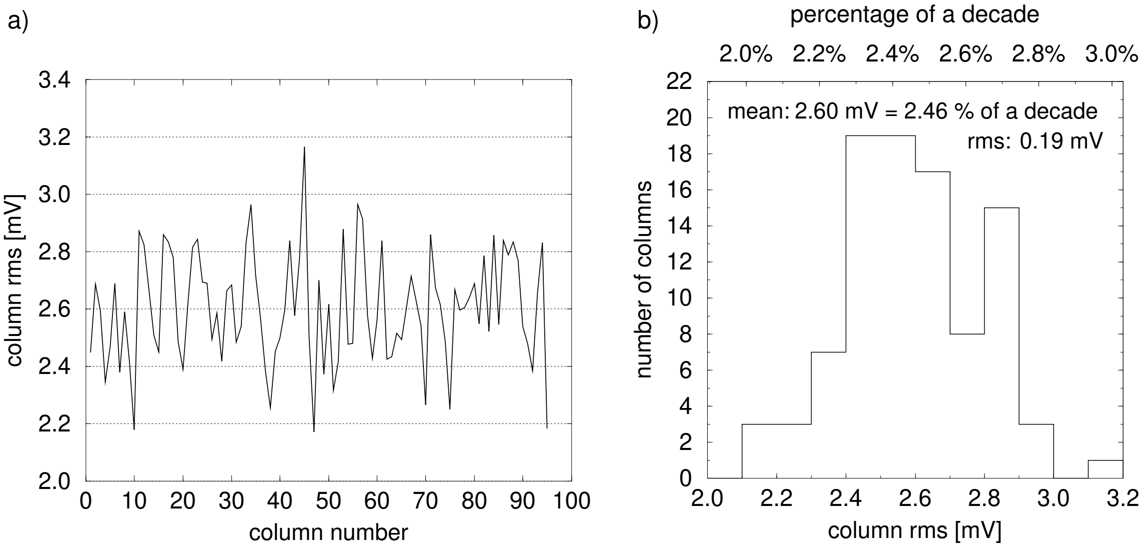


Figure 5.17: Distribution of the rms values corresponding to the individual columns, measured at an intensity of 3 W/m^2 (Vichideo).

to the measured value confirming the statistical independence of the individual contributions. On the other hand, the column-to-column variations are reduced by more than a factor of 2 compared to the results of the first image sensor Vichi shown in section 4.2.1. This improvement is achieved by the special layout of the reference current sources and by the redesign of the calibration amplifiers (cf. section 4.2).

light intensity [W/m^2]	column-to-column variations, rms [% of a decade]	variations within one column [% of a decade]	square sum of 2nd and 3rd table column [% of a decade]	total fixed pattern noise [% of a decade]
0.03	1.95	2.56	3.22	3.22
3.0	2.24	2.46	3.33	3.37
300	3.14	2.43	3.97	3.94

Table 5.1: Contributions to the Vichideo fixed pattern noise, evaluated at three different intensities.

Divichi results

The analysis of the fixed pattern noise with respect to the column-to-column variations and the non-uniformity within individual columns has also been carried out in the case of the high resolution sensor Divichi. The mean values of the individual columns representing the column-to-column fixed pattern noise are plotted in part a) of figure 5.18 as a function of the column number. The considered data refers to the fixed pattern noise in figure 5.13 and corresponds to an intensity of 1 W/m^2. Similar to the smaller sensor Vichideo, two different effects can be observed: 1. A variation on the large scale of the whole sensor with the maximum peak at column 100 and the minimum value around column 350. 2. A short range variation resulting in alternating high and low mean values. In order to clarify this behaviour, a region of 30 columns starting from column 100 has been enlarged and is shown in the same diagram.

The first effect is caused by global process parameter variations influencing the column structures like reference current sources and calibration amplifiers. The second effect results from the mismatch between the two feedback capacitors of the readout amplifier corresponding to the two alternately used readout lines. The histogram in part b) of figure 5.18 contains three different curves: The solid line refers to all column mean values, the left dashed one to the even and the right dotted one to the odd columns. The mean values of the even and odd distributions amount to 0.819 mV and 0.832 mV, respectively. The difference of 13 mV corresponds to 4.6 % of a decade due to the slope of 280 mV/decade. The standard deviation of the even or odd column mean values results in 2.3 % of a decade. This means a reduction of nearly 30 % in comparison to the rms value of all columns which is 3.25 % of a decade. Therefore, the mismatch between the feedback capacitors significantly influences the total fixed pattern noise. However, it can be reduced by decreasing the gain of the readout amplifier. By this means, the capacitor size is increased resulting in a better matching. The measurements of Vichideo (figure 5.16) are carried out at a reduced gain. They show a smaller influence of the feedback capacitors, although the sensor includes exactly the same readout components as Divichi.

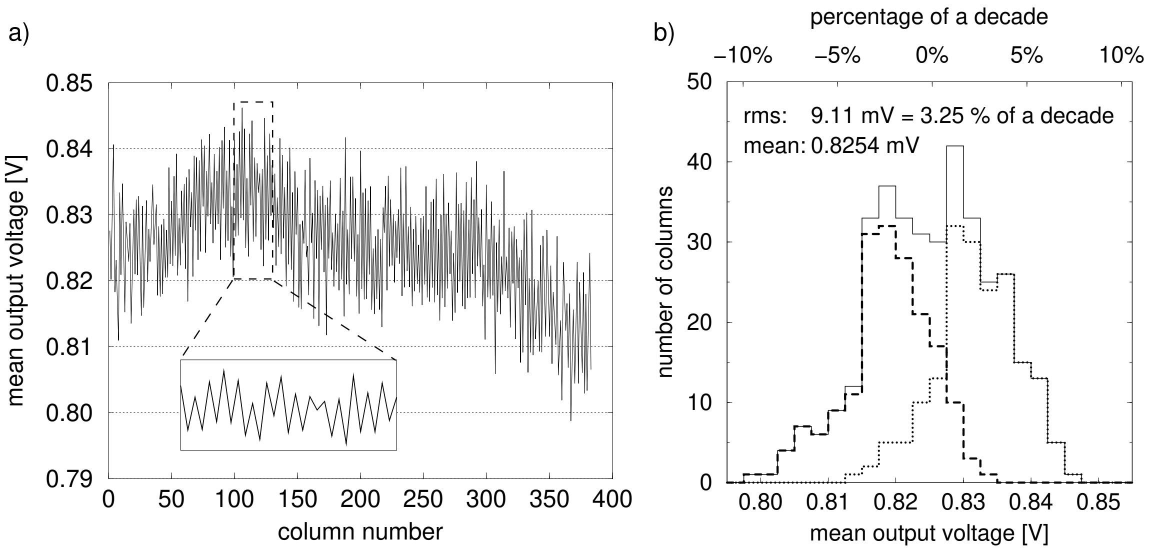


Figure 5.18: Mean of all pixels values within one column as a function of the column number (left diagram) and the corresponding histogram (right diagram). The results refer to the image sensor Divichi and are measured at an intensity of 1 W/m^2. The left dashed histogram curve contains the even, the right one the odd columns.

The left diagram in figure 5.19 shows the standard deviation of the fixed pattern noise within one column as a function of the column number. All values are filled into the histogram on the right. The mean value of the column rms values amounts to 5.73 mV corresponding to 2.05 % of a decade. The width of this distribution is relatively narrow since the standard deviation results in 0.31 mV. This equals about 5 % of the mean value. Therefore, all columns show approximately the same fixed pattern noise. Only a slight dependence on the column number can be observed.

The standard deviation of the column-to-column variations as well as the mean value of the fixed pattern noise within individual columns have been examined for the three intensities 10 mW/m^2, 1 W/m^2 and 100 W/m^2. The results are given in table 5.2. In addition, the table contains the root of the square sum corresponding to equation 5.1 and the total measured fixed pattern noise. In every case, the difference between calculated and measured fixed pattern noise is below 1 %. Consequently,

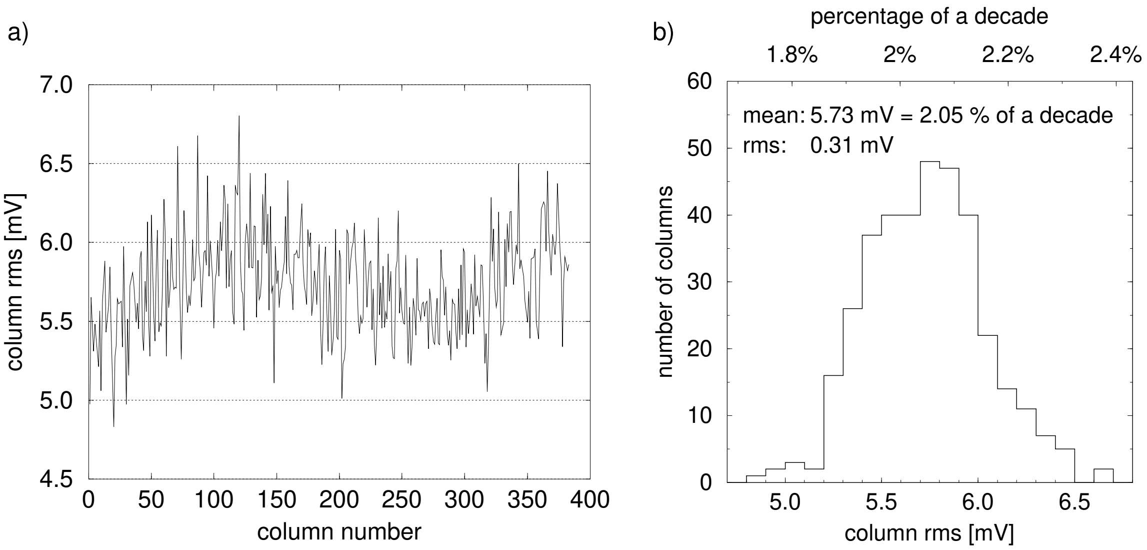


Figure 5.19: Distribution of the rms values corresponding to the offset distributions in the individual columns, measured at an intensity of 1 W/m^2 (Divichi).

the statistical independence of column-to-column variations and individual column non-uniformities is confirmed.

At high intensities, the column-to-column mismatch represents the dominant contribution. Regarding lower intensities, this percentage decreases more and more. The high total fixed pattern noise at 10 mW/m^2 is almost exclusively caused by the variations within the individual columns. These variations are caused by the large slope non-uniformities at low intensities (cf. next section). The reason for the dependence of the column-to-column rms values on the actual intensity is explained by the mismatch of the feedback capacitors in the readout path. As they influence the gain of the readout amplifier, the difference between first and second readout line depends on the absolute value of the output signal. The higher the signal, the higher the influence of the capacitor mismatch.

light intensity [W/m^2]	column-to-column variations, rms [% of a decade]	variations within one column [% of a decade]	square sum of 2nd and 3rd table column [% of a decade]	total fixed pattern noise [% of a decade]
0.01	2.45	8.18	8.54	8.53
1.0	3.25	2.05	3.84	3.82
100	4.50	1.56	4.76	4.78

Table 5.2: Contributions to the Divichi fixed pattern noise, evaluated at three different intensities.

Finally, the row-to-row variations are regarded. Therefore, the mean values of all sensor rows are calculated and plotted as a function of the row number in figure 5.20. The very low local fluctuations are apparent. The reason is the absence of any structure influencing the pixel offsets of a complete row like the reference current sources in the case of column-to-column variations. However, the row mean values show a global drift on the larger scale of the complete sensor array. This is caused by the global variations of the process parameters affecting all pixels of a row and consequently shifting the mean value. Despite the drift of the row values, the standard deviation is still relatively small. It amounts to 2.96 mV corresponding to 1.06 % of a decade.

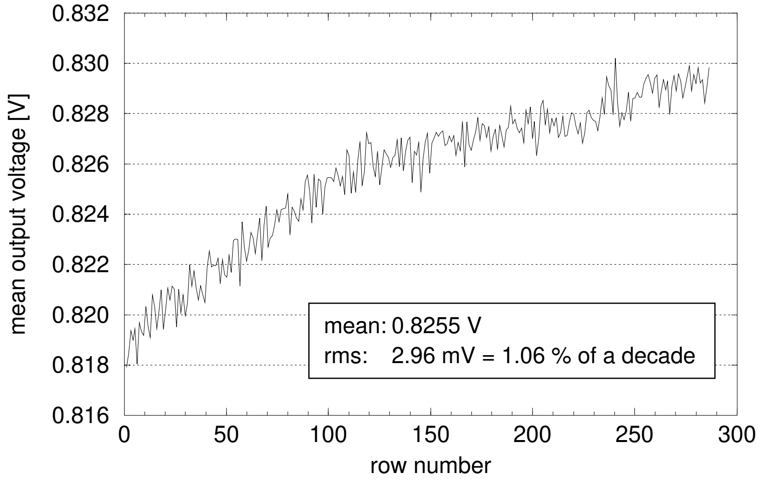


Figure 5.20: Mean value of the pixel outputs within one row as a function of the row number. The results refer to the image sensor Divichi and are measured at an intensity of 1 W/m^2.

5.2.4 Slope variations

Due to slight variations of the subthreshold slope factor n introduced in section 2.1.2, the slope of the photoreceptor response varies from pixel to pixel. Since these non-uniformities are not corrected by the self-calibration, they can result in a considerable contribution to the total fixed pattern noise. Their influence increases with the distance between the calibration point and the actual illumination. Since the calibration point typically corresponds to an intensity in the upper half of the sensitivity range in order to guarantee a reference current high enough for a stable self-calibration process, the slope variations become important particularly at very low intensities.

Figure 5.21 shows the histogram of the individual slopes averaged in a range of 4 decades. The values correspond to the 7000 pixels of the camera chip Vichideo. To verify the results, the slope variations were also measured regarding a different die of the same production run. The according

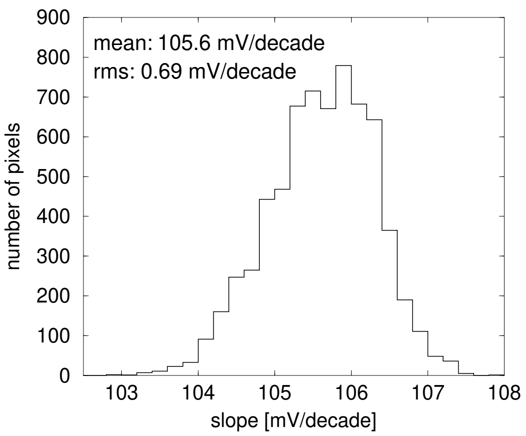


Figure 5.21: Distribution of the individual pixel slopes corresponding to the image sensor Vichideo.

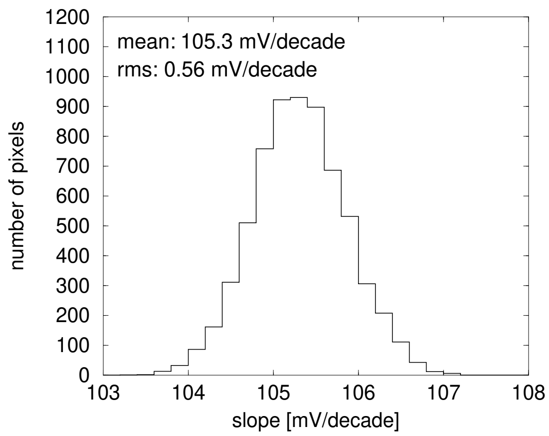


Figure 5.22: The same slope distribution as in the neighbouring histogram, however, measured with a different die.

distribution is shown in figure 5.22. Both chips possess a mean slope of about 105 mV/decade. Due to the adjustable gain of the readout amplifier, this value is not fixed but can be varied in a wide range. The standard deviations amount to 0.69 mV/decade and 0.56 mV/decade which means a relative width of 0.66 % and 0.53 %, respectively. Compared to the total fixed pattern noise of about 3.5 % of an intensity decade, the slope variations are relatively small. Therefore, their contribution in the region of the calibration point is negligible. However, since the variations have to be multiplied by the number of decades between the calibration point and the operating intensity, they can still have an important influence. If using a high reference current resulting in a fast calibration cycle, the multiplication factor can be 6 or even more when regarding low light intensities.

In the case of Divichi, the 100k individual pixel slopes are filled into the histogram of figure 5.23. The values are obtained by averaging the slopes in the range from 500 mW/m^2 to 500 W/m^2. The mean value amounts to nearly 250 mV/decade due to the gain adjustment of the readout amplifier. The rms value of 2.26 mV/decade corresponds to a relative value of 0.90 %. This is somewhat more than in the case of Vichideo, but still represents a low value compared to the total fixed pattern noise of about 4 % of a decade.

Regarding the slope variations at the low intensity of about 50 mW/m^2, the standard deviation significantly increases whereas the mean value remains more or less the same. The rms value of 12.9 mV results in a relative value of 5.2 %. The corresponding histogram can be seen in figure 5.24. This behaviour is different compared to Vichideo which shows much smaller slope non-uniformities at the lower end of the dynamic range.

The reason of this discrepancy is probably the reduced calibration and pixel relaxation time of the high resolution sensor. Since more rows have to be calibrated in the same time, the time per row is shortened. At low intensities, the difference between the calibration level and the readout level of the pixel signal is very high. Therefore, the available time does not suffice to perfectly calibrate all pixels. Consequently, the offset distribution is worsened resulting in the measured increase of the pixel slope variation. This effect is also responsible for the increased fixed pattern noise at the intensity of 10 mW/m^2 in figure 5.14. It can be somewhat reduced by changing the readout timing and the bias voltages determining the speed of the devices concerned.

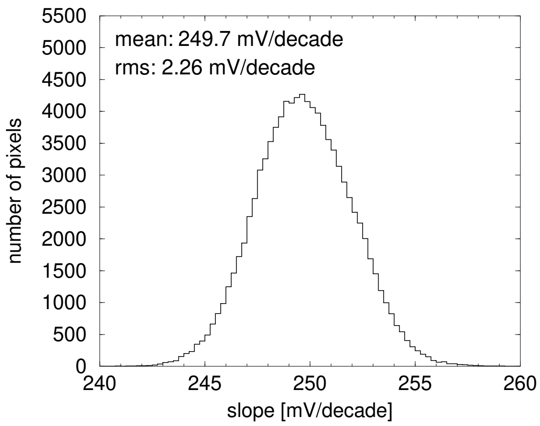


Figure 5.23: Distribution of the pixel slopes corresponding to the image sensor Divichi. The values refer to the range from 500 mW/m^2 to 500 W/m^2.

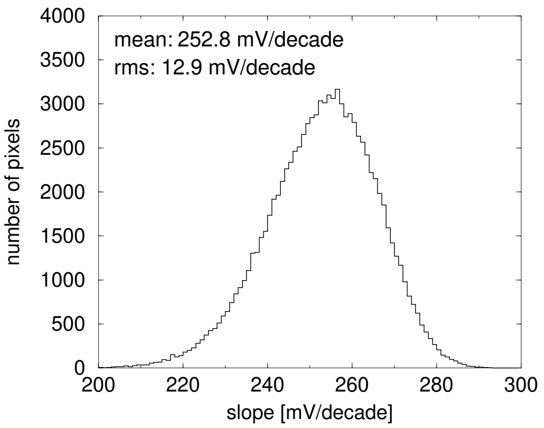


Figure 5.24: Distribution of the Divichi pixel slopes in the low intensity range around 50 mW/m^2.

5.3 Complementing measurements

The following measurements represent a further evaluation of the self-calibrating image sensor but do not refer to the remaining fixed pattern noise. In most cases, only the results of either the small chip Vichideo or the larger chip Divichi are presented. Since both sensors are composed of the same pixel types and the same surrounding components like calibration, decoder and readout circuits, they basically show the same behaviour with respect to the considered properties.

5.3.1 Temporal noise

So far, only the fixed pattern noise referring to the mean output signals of the individual pixels has been regarded. However, the pixel signals show an additional noise component which is the temporal noise. This means, that the output signal of one pixel illuminated at a fixed intensity is not constant but varies with time. The temporal noise was measured by consecutively reading out 500 frames and calculating the rms value corresponding to each pixel. The measurements were carried out under typical operating conditions, i.e. 50 Hz frame rate and a new pixel calibration before every readout.

The rms values corresponding to the temporal noise of Divichi can be seen in the histogram in figure 5.25. The measurement was carried out at an intensity of 0.5 W/m^2. The mean noise value amounts to 6.55 mV which equals 2.34 % of an intensity decade. Therefore, it is somewhat lower than the fixed pattern noise showing nearly 4 % of a decade. The rms noise values vary between the individual pixels in a range from 5 mV to 8.5 mV according to a standard deviation of 0.55 mV. Figure 5.26 contains the mean rms noise as a function of the light intensity. It turns out, that apart from small fluctuations, the temporal noise is independent of the illumination. The width of each noise distribution indicated by the error bars also shows no significant dependence on the intensity.

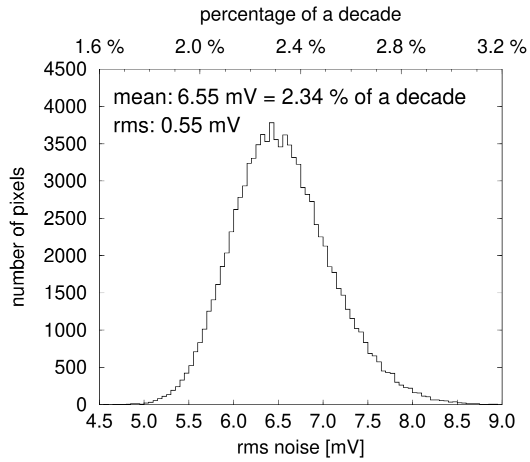


Figure 5.25: Temporal noise distribution at an intensity of 0.5 W/m^2.

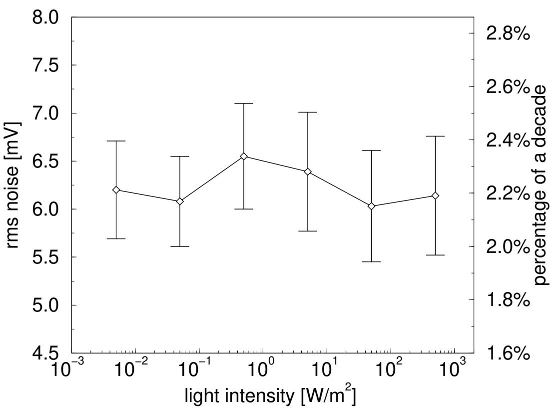


Figure 5.26: Temporal rms noise as a function of the light intensity.

In contrast to non-calibrated logarithmic image sensors, the noise is not determined by the *shot noise* of the photodiode. Otherwise, an intensity dependence of the temporal noise should be observed. The shot noise of the photocurrent I_{ph} is given by

$$\overline{i_s^2} = 2q\,I_{ph}\,\Delta f \tag{5.3}$$

where q is the elementary charge and Δf the bandwidth of the system. As the photocurrent is converted into a logarithmic voltage, the absolute value of i_s has no meaning. Instead, the ratio of i_s to

I_{ph} is the important quantity. For this reason, a dimensionless noise power is defined as follows

$$P = \frac{\overline{i_s^2}}{I_{ph}^2} = \frac{2q I_{ph} \Delta f}{I_{ph}^2} = \frac{2q\Delta f}{I_{ph}}. \tag{5.4}$$

Consequently, the shot noise depends on the absolute photocurrent and on the system bandwidth. Both effects partly compensate for each other. A lower photocurrent results in a lower pixel bandwidth because it takes longer to charge parasitic capacitances. At high intensities, however, the bandwidth is limited not by the pixel itself but by the readout circuits. Therefore, at least at high intensities, a dependence of the temporal noise on the illumination would exist if shot noise is a major contribution to the total sensor noise. Since this dependence does obviously not exist, other sources dominate the photoreceptor noise.

Several additional contributions increase the temporal noise. Because the pixels are calibrated before each readout cycle, the noise of the calibration amplifier causes a slightly different pixel correction voltage after every new calibration cycle. In addition, the diverse clocked stages from the pixel to the single output line (column buffer, multiplexer, readout amplifier, sample-and-hold stage) introduce noise, mainly due to the clock jitter of the individual control signals. Finally, the substrate coupling of digital part and analog part could result in a crosstalk between the digital and analog signals. All described contributions are basically independent of the light intensity and would lead to the observed noise behaviour. However, it is not evident which part plays the dominant role.

Combining the dynamic input range of 6 decades and the temporal noise of about 2.3 % of a decade gives the signal-to-noise ratio of the image sensor:

$$\frac{S}{N} = \frac{6\text{ decades}}{0.023\text{ decades}} = 48\,\text{dB}. \tag{5.5}$$

This value corresponds to somewhat more than 8 bits. Due to the logarithmic compression, the signal-to-noise ratio referring to the output voltage is different from the dynamic input range of the photoreceptor. Only in the case of linear systems, the signal-to-noise ratio equals the dynamic range with respect to the input signal.

5.3.2 Crosstalk

The effective resolution of an image sensor is not only determined by the number of pixels but also by the crosstalk of adjacent pixels. In order to examine the crosstalk behaviour, a single pixel of the camera chip Vichideo was stimulated with a bright laser spot (diameter about 7 μm). At the same time, the residual photoreceptors saw a low homogeneous illumination. Ideally, only the stimulated pixel would show an increased output signal whereas all other pixels stay at a constant low level.

The results corresponding to a laser spot intensity 2.5 decades higher than the background intensity can be seen in figure 5.27. The stimulated pixel shows a voltage of about 3.0 V. Regarding the directly adjacent pixels, the voltage drops by about 200 mV to 2.8 V. As the slope of the photoreceptor response amounts to 105 mV/decade, the difference between the stimulated and a neighbouring pixel corresponds to 2 decades of light intensity. One of the four adjacent pixels is somewhat higher than the others, because the laser spot was not perfectly centered on the photodiode of the middle pixel.

Figure 5.28 contains the results of a comparable measurement using an even brighter light spot. Here, one photoreceptor was stimulated with an intensity 4.5 decades higher than the background. Again, the output signal of the adjacent pixels decreases by a voltage corresponding to 2 intensity decades. The decrease by two decades per pixel is continued until the background level is reached.

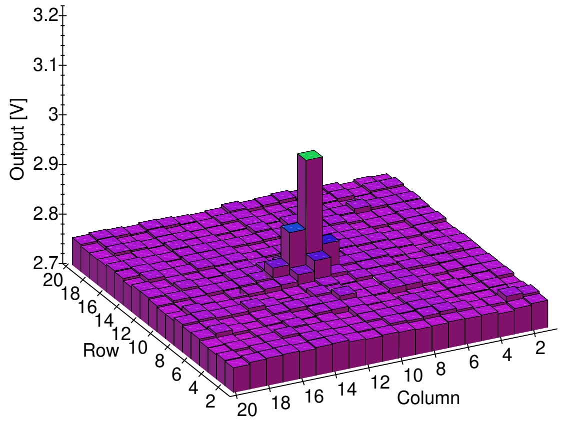


Figure 5.27: Crosstalk measured with a laser spot 2.5 decades brighter than the background.

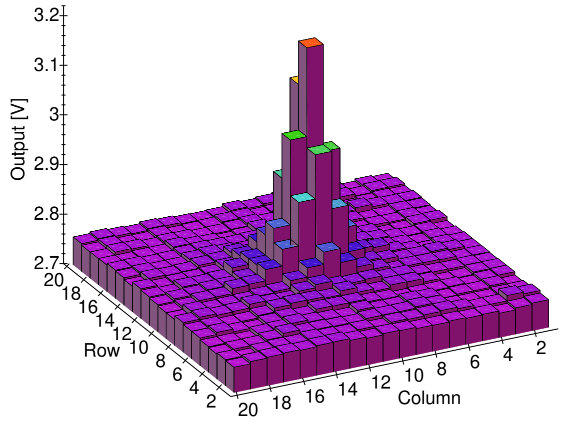


Figure 5.28: Crosstalk measured with a laser spot 4.5 decades brighter than the background.

However, the measurement results in figure 5.27 and 5.28 merely represent an upper limit for the actual pixel crosstalk. In any case, the real crosstalk is not higher, but could be lower due to the shape of the laser spot. On the one hand, the diameter is not exactly determined. It is in the region of 5 μm to 10 μm. On the other hand, the intensity does not show an abrupt drop when reaching the spot border, but more or less follows a Gaussian shape. Assuming half the diameter $d/2$ to be the standard deviation of the Gaussian curve, the intensity decreases to about 1 % of the maximum intensity at a point which is $3 \cdot d/2$ away from the centre. In the case of $d = 10\,\mu$m, the 1 % level is reached at a distance of 15 μm. Due to the pixel pitch of 24 μm, this location already corresponds to the adjacent pixel. Consequently, a part of the measured crosstalk could be caused by the surroundings of the laser spot illuminating the neighbouring pixels. The camera images of high dynamic range scenes (cf. section 5.4.1) confirm the assumption, that the effective crosstalk is lower than the measured one. Here, no visible crosstalk is apparent.

5.3.3 Adjustable readout amplifier gain

As described in section 4.4.3, the gain of the readout amplifier can be varied by changing the corresponding feedback capacitances. By this means, the slope of the photoreceptor response curve also changes. According to equation 4.1, the gain is given by

$$A_f = 1 + \frac{C_s}{C_{fb}} \tag{5.6}$$

where C_s is the storage capacitance and C_{fb} the adjustable feedback capacitance. Since C_{fb} belongs to the denominator of equation 5.6, a hyperbolic relationship between amplifier gain and selected capacitance can be expected.

The measured signal slope of the image sensor Divichi is shown in figure 5.29 as a function of the digital gain value. This gain value consists of 7 bits controlling the individual subcapacitors C_1 to C_7 of the feedback capacitance C_{fb} (cf. table 4.2). As they are active-low signals, C_{fb} decreases with an increasing control value resulting in an increasing gain. The slope can be varied in the range from 130 to 720 mV/decade with the expected hyperbolic dependence on the gain adjustment. Assuming an input range of 1 V of the subsequent device (e.g. video screen, ADC, etc.), the lowest gain allows to map more than seven intensity decades into this voltage range. This is more than the sensor's dynamic range. Increasing the gain continuously enhances the contrast until, at a slope of

720 mV/decade, about 1.5 intensity decades cover the full range of 1 V. The last setting is useful when regarding scenes with low dynamic range and low contrast, whereas the lower gain is required for high dynamic range scenes.

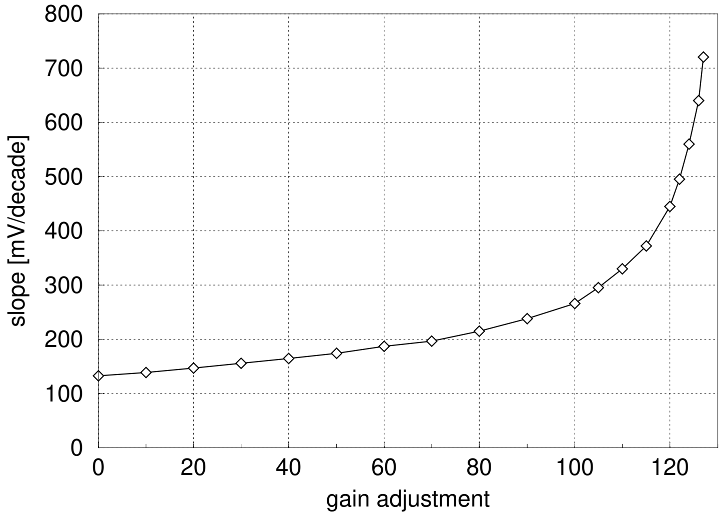


Figure 5.29: Slope of the photoreceptor response curve as a function of the gain settings of the readout amplifier (Divichi).

A comment on the different gain of the two individual readout lines leading to the mismatch between the even and odd array columns should be added. The better the capacitors C_{fb1} and C_{fb2} belonging to the readout lines 1 and 2 match, the lower the difference between the corresponding gain factors is. Since small capacitors (= high gain) show a higher mismatch than large capacitors, the alternating column structure (cf. figure 5.18) is particularly noticeable at high gain values. On the other hand, a reduced gain results in a better matching and lower column-to-column variations.

5.3.4 Storage time of the analog memory cells

The pixel correction voltage as well as the calibration amplifier offsets are stored on capacitors in order to bridge the time gap between two successive calibration or autozeroing cycles. Since the switch isolating this analog memory during the storage phase is realized as a MOS transistor, parasitic currents arising in this transistor (leakage currents and photocurrents) discharge the capacitor with time. For this reason, the calibration process has to be repeated after a certain time depending on the actual illumination level. At high intensities, the parasitic photocurrents are relatively high leading to a fast discharge of the analog memory cells. Low intensities, on the other hand, allow longer gaps between two calibration cycles due to a slower capacitor discharge.

The discharge behaviour has been examined regarding the image sensor Vichideo after stopping the calibration and autozeroing process, respectively. Figure 5.30 shows three images corresponding to the indicated times after disabling the self-calibration of the photoreceptors. As the intensity of 3 mW/m^2 is very low, the image is not influenced until some seconds have passed. At first, only a few pixels become darker whereas the residual ones stay at the calibrated level. By and by, the whole image changes. It darkens more and more due to the shifted correction voltages on the pixel capacitors.

The fact that some pixels very rapidly lose their correction voltage whereas others provide longer storage times probably results from the variations of the shielding metal layer. As there are some

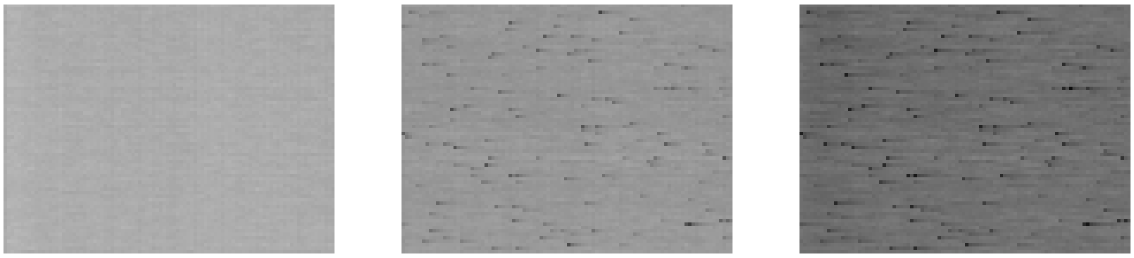


Figure 5.30: Behaviour of the image sensor Vichideo at an intensity of 3 mW/m^2 after stopping the self-calibration process.

holes in the metal layer due to the photodiode and the isolation of the two power supply lines routed with metal 3, slight displacements of the borders located near the switch transistor could cause the observed behaviour.

Figure 5.31 shows the mean output voltage of all pixels as a function of the time after stopping the calibration process. The three curves correspond to different intensities. The right diagram contains the same data as the left one enlarged in the region from -1 to 7 s. It can be seen, that the mean voltage decreases down to about 2.4 V and then stays constant. This decrease corresponds to a rise of the storage capacitor voltage V_{corr} since the pixel signal is inverted by the readout amplifier. The output voltage of 2.4 V corresponds to a correction voltage of $V_{corr} = 5$ V which is the upper supply voltage V_{dd}. As V_{corr} cannot exceed the supply potential, the final output signal stays at 2.4 V.

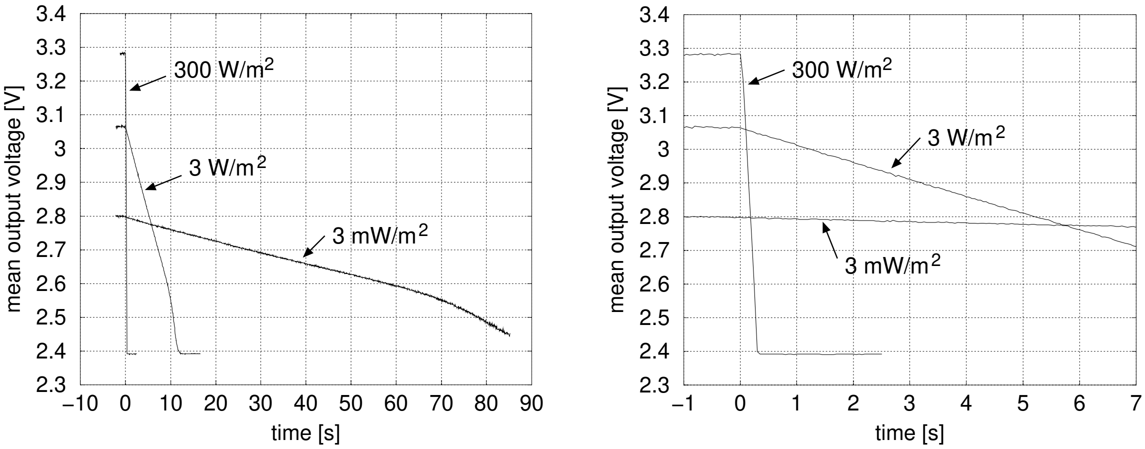


Figure 5.31: Mean output voltage of all Vichideo pixels as a function of time after stopping the self-calibration process.

A second property of the mean voltage decrease can be observed in figure 5.31: The drop rate significantly depends on the light intensity. Comparing the time required for a voltage shift of 100 mV, the following values can be read from the diagrams:

intensity [W/m^2]	0.003	3.0	300
time [s]	19.5	2	0.032

Because the maximum voltage drop acceptable for obtaining reasonable images is in the region of a few mV, the maximum time between calibration and readout (relaxation time) amounts to only a fraction of the numbers given above. This means no problem at low intensities but results in very short times of below 1 ms at high intensities. These short times, on the other hand, prevent the pixel voltages at low intensities from recovering their operating level before being read out. Therefore, a tradeoff resulting in a relaxation time corresponding to the regarded intensities has to be found. If the total dynamic range is required, a medium relaxation time should be chosen in order to obtain sensible signals at low and at high illumination.

The sensor behaviour after stopping only the autozeroing of the calibration amplifiers is shown in figure 5.32. The self-calibration process of the photoreceptors is still activated to observe the influence of a changed calibration amplifier offset. The presented images correspond to the low intensity of 3 mW/m^2. Here, the first stripes caused by a shifted offset voltage on the compensation capacitors occur after 2 s. Changing to higher intensities this time is significantly shortened and finally reaches values below 1 ms. For this reason, the autozeroing process should be carried out every time before calibrating a new array row.

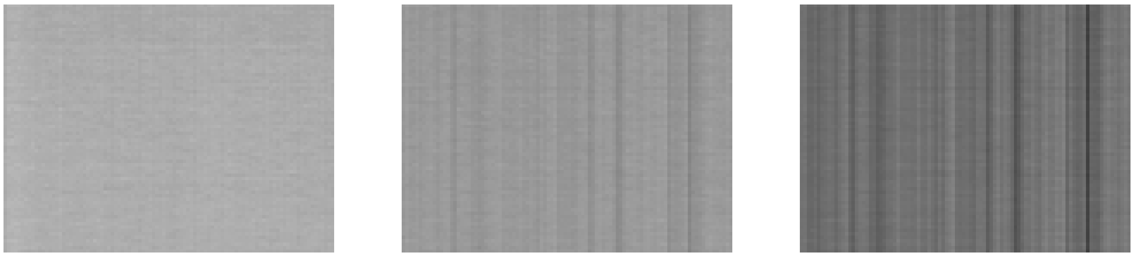


Figure 5.32: Behaviour of the image sensor Vichideo at an intensity of 3 mW/m^2 after stopping the autozeroing process of the calibration amplifiers.

5.3.5 Yield considerations

The production of microchips unfortunately suffers from a high sensitivity to any pollution of the process environment. Although the individual CMOS production steps are carried out in a cleanroom with less than 100 particles per m^3, only a fraction of all chips will perfectly operate. The yield, i.e. the ratio of properly working to produced chips decreases with increasing chip size, since the probability of getting one defect per unit area is constant. The image sensor Divichi with a size of 90 mm^2 represents a relatively large design. Thus, a high number of the produced camera chips shows some kind of defects.

Concerning the Divichi sensor, 12 chips have been bonded and examined. Only one of them shows no defects at all whereas the remaining 11 dies have at least one damaged pixel. As the sensor array includes many vertical and horizontal control and readout lines, a single defect often affects a complete row or column. Regarding the 12 analyzed chips, the number of defects averages about 3 per chip. In other words, there is one defect every 30 mm^2. Using this number, the expected yield can be calculated.

In first approximation, the probability of getting no defect in the area of 1 mm^2 is given by $p = \frac{29}{30}$. Hence, the yield of a 90 mm^2 chip amounts to $(29/30)^{90} = 4.7\,\%$. A more precise calculation is obtained by dividing the area of 1 mm^2 in n subparts with an area of $1/n$ mm^2 each. In the case of $n = 10$, the probability of no defect in 1 mm^2 results in $(299/300)^{10}$ as 10 individual parts with a probability of $(299/300)$ have to be sequently considered. To obtain the yield of Divichi, this number has to be raised to the power of 90. By increasing the integer n, a more and more precise value can be achieved. The exact solution for $n \to \infty$ yields

$$p = \lim_{n\to\infty} \left(\frac{30n-1}{30n} \right)^{nx} = e^{-\frac{x}{30}} \tag{5.7}$$

where p is the probability of getting no defect in an area of x mm^2. In the case of Divichi with a size of 90 mm^2, the yield amounts to $p = 5.0\,\%$.

Because most of the chip defects occur in the pixel matrix representing the largest sensor part, the low yield could be increased by implementing the possibility of disabling defect pixels, rows or columns. This can be done in two different ways: Either storing the addresses of missing pixels or lines and reading out the neighbouring pixels when the defect structures are selected, or always comparing the output signal to an upper limit and, if exceeding this level due to a defect pixel, using the averaged output signal of the surrounding pixels. These methods slightly reduce the effective sensor resolution if deactivating a certain number of pixels. In most applications, however, this issue is not a big problem. Unfortunately, no compensation method for defect array structures is integrated in the Divichi sensor resulting in the low yield mentioned above.

5.4 Camera images

The following sections give some examples of pictures taken with the self-calibrating logarithmic image sensors. Most pictures stem from the final camera chip Divichi with 100k pixels, images of the smaller sensors Vichi and Vichideo are only presented to illustrate special properties. Except for the Vichi pictures, which are corrected for the column-to-column variations, all images represent the original camera data. No further fixed pattern noise correction or any other image processing algorithm have been carried out. Solely, the contrast is adapted by software to the range of 256 grey levels resulting in a better reproduction when printing the pictures.

5.4.1 High dynamic range scenes

The major advantage of photoreceptors with logarithmic response is given by the high dynamic range of up to 6 decades. It allows to cope with very high and low intensities without adapting the exposure time or the optical aperture as in the case of linear camera systems. For this reason, the corresponding dark and bright structures can exist in the same image without being over- or under-exposed. This property is demonstrated in figure 5.33 showing a comparison between the logarithmic CMOS image sensor Vichideo (96 × 72 pixels) and a high resolution CCD camera[6]. The presented scene, consisting of a bright incandescent bulb in front of our ASIC-laboratory logo printed on white paper, corresponds to a dynamic range of about 4-5 intensity decades.

The logarithmic sensor on the left is capable of seeing both, the logo and the filament of the bulb. The picture looks a bit coarse due to the low Vichideo resolution of 7000 pixels. The four pictures of the CCD sensor on the right show the same scene with different lens aperture adjustments. The exposure time was set to a fixed value and the automatic gain control was disabled in order to get the pure CCD sensor values. From left to right and from top to bottom, the lens aperture is closed more and more. At first, the logo-symbol can be clearly seen whereas the bulb is significantly over-exposed. Even some CCD side effects (vertical stripes) occur around the bulb due to the high light intensity. The more the aperture closes, the darker the image gets. The second and third picture still

[6]Sony DXC-107AP with 752 × 582 pixels

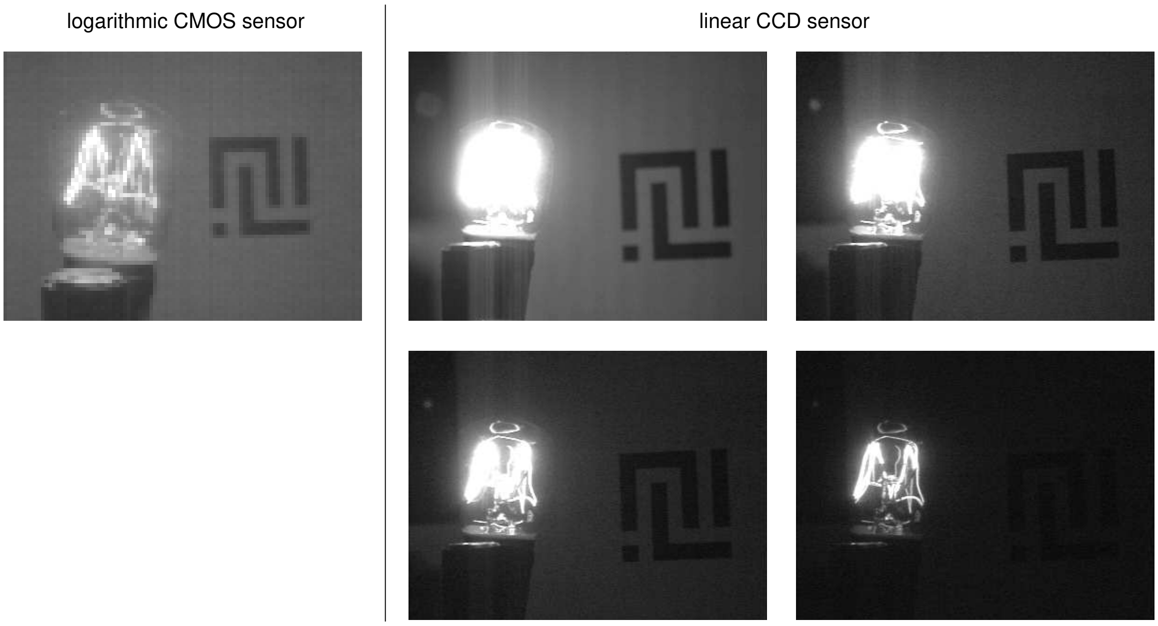


Figure 5.33: Images of a high dynamic range scene. The left one is taken with the logarithmic image sensor Vichideo, the right ones with a high resolution CCD camera.

show an over-exposed lamp whereas the ASIC-logo already starts to become unclear. In the fourth picture, finally, the bulb structure can still be recognized in full detail, but the logo has completely disappeared. Consequently, the dynamic range of the regarded scene exceeds that of the linear CCD sensor, whereas the logarithmic camera is able to manage the situation.

Figure 5.34 shows a similar high dynamic range scene taken with the logarithmic CMOS sensor Divichi. The sensor was adjusted to video mode with a frame rate of 50 Hz. Due to the higher resolution of 384×288 pixels, the image looks sharper and allows to see more details of the bulb than in the left picture of figure 5.33. As the remaining fixed pattern noise amounts to about 1 % of the presented dynamic range, it is below the grey level resolution of the printer. Only a few pixels belonging to the peaks of the offset distribution can be detected. Therefore, if only large contrasts have to be processed, fixed pattern noise is not a big problem in high dynamic range scenes .

An example of the subsequent edge detection process in the tactile vision system TVSS carried out by the analog edge detection chip EDDA [SCH99] is shown is figure 5.35. Because this image processing chip only provides 64×64 pixels, two subparts of the high dynamic range scene in figure 5.34 are considered. The upper part contains 64×64 original pixels, whereas the lower one corresponds to a cut-out of 128×128 pixels reduced to the required 64×64 pixels by averaging the respective clusters of 2×2 pixels with software.

The edges detected by EDDA can be seen at the right of the two picture cut-outs. They are calculated in a few microseconds consuming less than 1 μJ of power. In some cases, two edges in parallel are obtained although there is only one grey level transition in the image. This is an effect of the implemented edge detection algorithm which looks for different grey levels in adjacent pixels. Sometimes, the given difference level corresponding to a detected edge is exceeded twice due to a medium intensity pixel between a dark and a bright pixel leading to the observed double-edges. In the TVSS, a subsequent software step will follow, finding correlated edges belonging to the same structure and preparing the data for transmission via the tactile display.

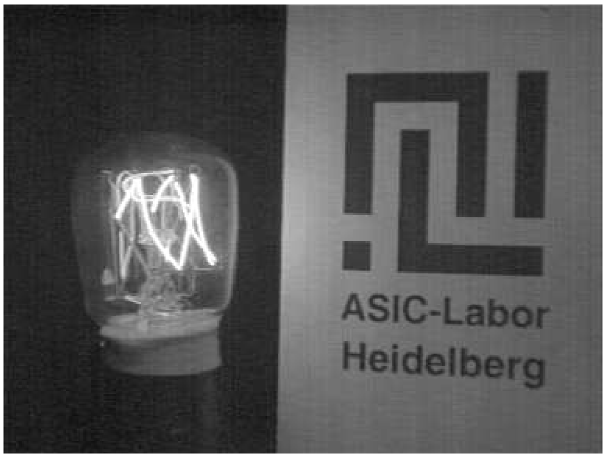


Figure 5.34: Image of a similar high dynamic range as seen in figure 5.33, taken with the logarithmic high resolution sensor Divichi.

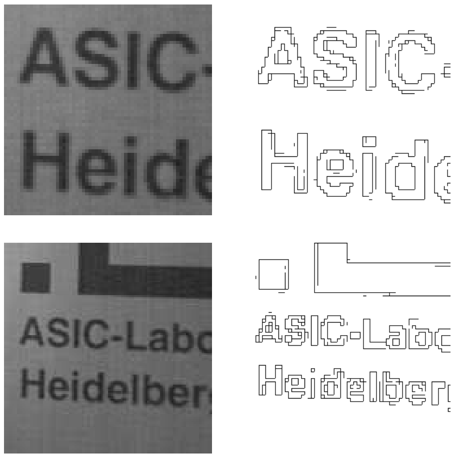


Figure 5.35: Two enlarged parts of the left picture and the corresponding results of the analog edge detection array EDDA [SCH99].

5.4.2 Typical environmental and low dynamic range scenes

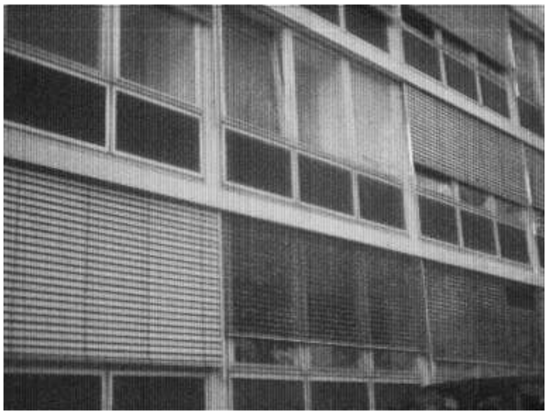
For use in the vision substitution system, not only high dynamic range scenes but also pictures from typical environmental scenes with lower contrast and lower dynamic range have to be processed. For this reason, figure 5.36 shows a few Divichi pictures of natural scenes taken around the institute building[7] and some technical pictures taken inside the ASIC laboratory. Again, the frame rate was 50 Hz according to the CCIR video standard. The first three images correspond to an illuminance of about 10 klux (sunny day), the pictures 4-6 to an illuminance of several 100 lux (artificial room light). Picture 4 represents the Divichi camera board including the image sensor directly bonded on the PCB. The same object taken with a linear CCD sensor has already been presented in figure 4.52 where the complete camera system is described. Picture 5 shows the inside of a car radio. In picture 6, containing a part of an equipped printed circuit board, an example of the on-screen display can be seen. The word BRIGHTNESS refers to one of the 13 commands selectable with the manual 3-button interface.

The dynamic range does not exceed 3 decades. In comparison to linear camera systems also capable of processing these scenes, the logarithmic pictures have a poorer contrast. This is due to the logarithmic compression mapping 120 dB (6 decades) of input data into an output voltage range of less than 50 dB. Consequently, low contrasts of the incident light which are given by the ratio of the concerned intensities are further reduced in the final logarithmic image. This effect is particularly transparent at high intensities where the contrast sensitivity of linear systems reaches its maximum.

Because the dynamic range is decreased compared to figure 5.34, the remaining fixed pattern noise becomes more important. The pictures are somewhat more noisy and slight vertical stripes can be seen due to the column-to-column variations. As mentioned in section 5.3.3, the alternating stripes can be reduced by changing the gain of the readout amplifier. In the presented pictures, the digital value controlling the gain was adjusted to about 100. The statistically distributed fixed pattern noise of individual pixels is greatly reduced by the subsequent edge detection chip, which performs a kind of spatial noise filtering with the help of a resistive network. For other applications, it depends on the specific system requirements if the applied fixed pattern noise reduction is sufficient. Regarding a scene covering 3 intensity decades, the sensor shows a signal-to-fixed pattern noise ratio of 38 dB. At a dynamic input range of 6 decades, it increases to 44 dB.

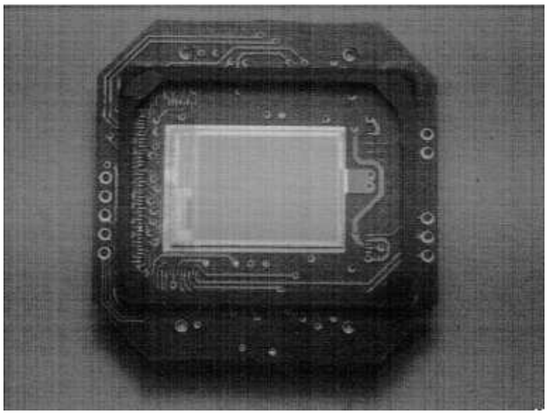
[7] Institute of high energy physics, Heidelberg University

picture 1

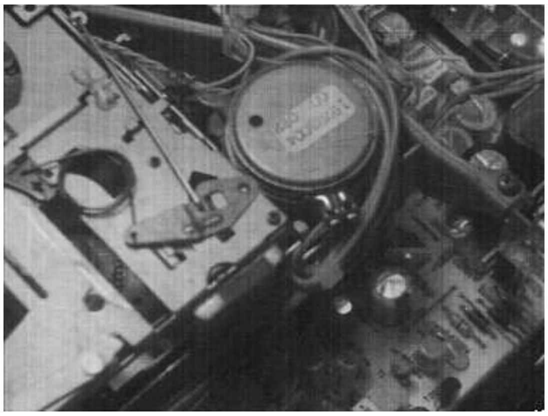


picture 2

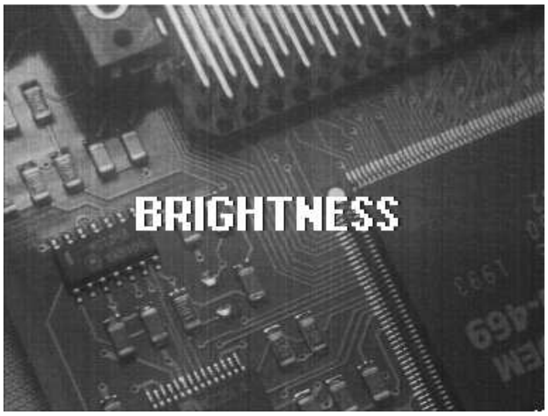
picture 3



picture 4



picture 5



picture 6

Figure 5.36: Images of some outdoor scenes (picture 1-3), of the camera chip itself (picture 4) and of two electronic components (picture 5-6) covering a low to medium dynamic range. Picture 6 gives an example of the built-in on-screen display.

5.4.3 Auto-exposure control

The developed image sensors allow to perform a kind of exposure control by extracting the reference current for the self-calibration process from small photodiodes in each pixel. The result is a constant mean output voltage averaged over all pixels independent of the actually regarded scene or the applied illumination. If the image becomes brighter, the photoreceptors are calibrated with a higher reference current compensating for the increased intensity (cf. section 3.2.1).

Figure 5.37 demonstrates this behaviour by means of the high resolution image sensor Divichi. Two images of a tree, a roof and some clouds in the sky are shown. In the right picture, the tree representing a relatively dark object occupies nearly the whole area. In the right picture, the camera is somewhat turned left. Now, the scene is dominated by the bright sky. In order to keep the mean output signal constant, the total brightness of the image is decreased by the auto-exposure control. Therefore, all structures like the roof or the tree become darker compared to the left original picture.

Figure 5.37: Example of the auto-exposure control. From left to right, the tree becomes darker since the mean intensity of the complete scene is increased.

The properties of the automatic exposure control were examined more exactly in the case of the logarithmic sensor Vichi containing 64×64 self-calibrating pixels. Figure 5.38 shows a sequence of four images representing the applied measurement procedure. As the sensor possesses significant column-to-column variations (cf. section 4.2.1), the pictures are corrected for these non-uniformities by the readout software. At first, the camera sees a bright, uniformly illuminated surface. Then, starting from the top, a dark surface is more and more moved into the visible region until the complete image is covered. The difference between dark and bright surface amounts to about 1 decade. Since the auto-exposure control tries to keep the mean output voltage constant, the image is brightened according to the ratio of dark to bright area. Finally, when the picture is completely occupied by the dark surface, it shows nearly the same grey level as in the beginning, when only seeing the bright surface.

The quantitative analysis of this behaviour can be seen in figure 5.38. Here, the output voltage of two individual pixels, one belonging to the upper array region and one to the lower array region, is plotted as a function of the dark to bright ratio in the image. At the left border of the diagram, the sensor is homogeneously illuminated at a high level. Both pixels show the same value of 2.86 V. Then, at a dark to bright ratio of about 10 %, the upper pixel raises its voltage due to the lower intensity in the upper array region. Since Vichi has no inverting readout amplifier, a lower incident intensity means a higher output voltage due to the intrinsic photoreceptor properties.

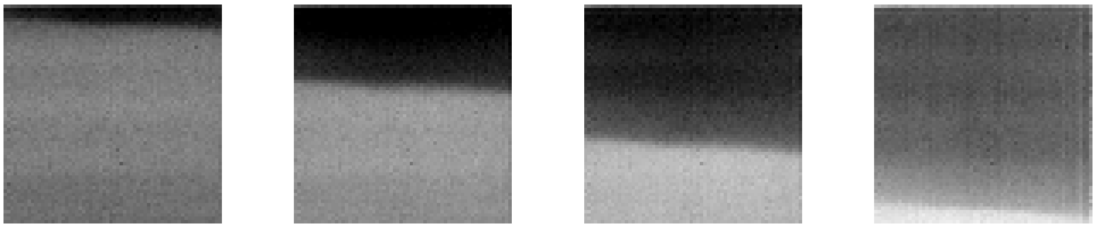


Figure 5.38: Measurement of the auto-exposure control of the sensor Vichi by moving a dark surface from top to bottom into the image.

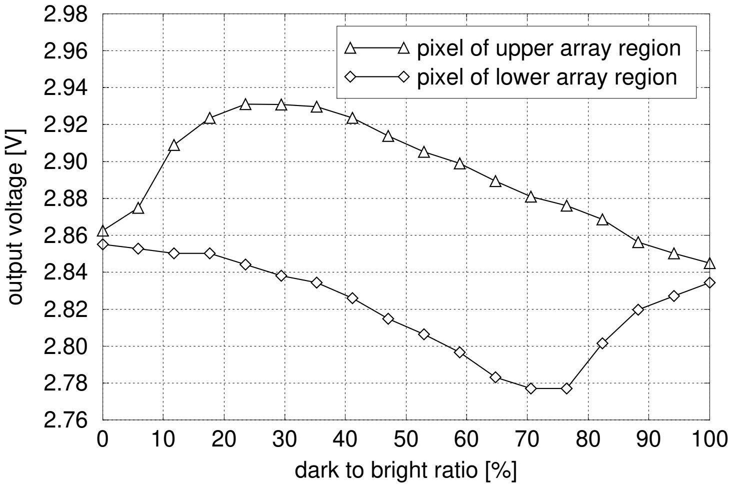


Figure 5.39: Results corresponding to the auto-exposure measurement in figure 5.38. The curves correspond to the output voltage of a pixel in the upper and in the lower array region, respectively.

The more the dark surface covers the sensor area, the more both pixel voltages are reduced. This is due to the automatic exposure control compensating for the image getting darker and darker. At about 80 %, the lower pixel is reached by the dark surface and also raises its output signal. Finally, at the right border of the diagram, both pixels again show almost the same level. This level nearly equals the initial output voltage although the sensor is illuminated at an intensity of one decade below the initial one. The camera has managed to keep the mean voltage constant. Consequently, the input range of the subsequent device can be very small without losing the camera signal when the illumination changes. On the other hand, if regarding low contrast scenes, the output contrast can be increased (higher gain of the readout amplifier) without leaving the input range of the attached device even if the image becomes significantly darker or brighter.

Another advantage of the automatic exposure control is given by the compensation for the artificial light flicker. Since the control mechanism can operate very rapidly, it follows the varying illumination caused by the 100 or 120 Hz room light frequency. Usually, image sensors composed of continuously working photoreceptors like the logarithmic pixels show a horizontal stripe pattern, because the readout of one frame takes about 20 to 50 ms. Some pixels are read out at a high and some at a low illumination depending on the actual phase of the lamps' power supply voltage. This behaviour, corresponding to a disabled exposure control, can be seen in the left image of figure 5.40. When enabling the auto-exposure control and adjusting the right time difference between calibration and readout row, the right picture is obtained. It is compensated for the light flicker and thus no longer

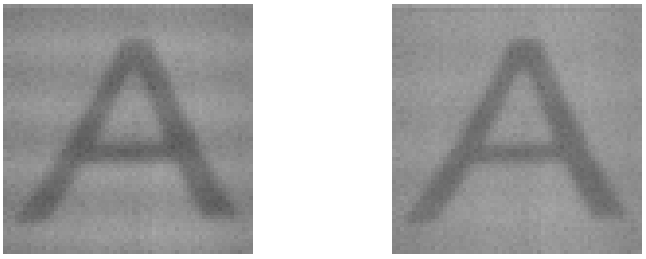


Figure 5.40: Two pictures of the letter A, taken with the image sensor Vichi. The left one shows a stripe pattern caused by the 100 Hz artificial light flicker, the right one does not due to the flicker compensation by the auto-exposure control.

shows the corresponding stripe pattern. Both images of figure 5.40 stem from the image sensor Vichi and are taken at a frame rate of 20 Hz. The contrast between the letter A and the background amounts to about 80 % of a decade.

5.4.4 Averaging

In order to examine the camera images in a lower resolution, the possibility of averaging up to 8×8 pixels has been implemented (cf. section 3.2.2). This allows to map the complete image of the high resolution sensor Divichi to the analog edge detection chip EDDA providing only 64×64 pixels. In addition, a faster readout of the whole scene is obtained because the frame rate is defined by the readout time per pixel multiplied by the number of pixels. The highest averaging level (8×8 pixels) corresponds to a resolution of $48 \times 36 = 1728$ pixels which means a maximum frame rate of about 4 kHz due to the pixel rate of 7 MHz. If no video timing is required, the pixel rate can be further increased to about 10 MHz by using a higher system clock frequency. However, this is a simulation result and has not been confirmed by measurements.

Figure 5.41 shows the high dynamic range picture of figure 5.34 for six different averaging levels. Here, the vertical averaging level always equals the horizontal averaging level although, in principal, a separate adjustment of both values is possible. The typical applications, however, do not require the asymmetric averaging. Therefore, no examples referring to different horizontal and vertical averaging levels are given. The images are taken at a pixel rate of 5 MHz with a special readout timing differing from the video timing in order to achieve higher frame rates.

Two effects can be observed concerning the averaged pictures in figure 5.41. The first point is, that the contrast seems to decrease with every higher averaging level. This is caused by the smearing of the object edges. Since some subpixels of the averaged pixel cluster see a dark and some a bright intensity, an averaged output voltage somewhere in between is obtained. The resulting contrast reduction is especially apparent when regarding the script below the ASIC-logo. The individual letters are so small, that particularly in the last picture, one single pixel covers a complete letter.

The second effect concerns the remaining fixed pattern noise. The pictures corresponding to a high averaging level seem to have higher pixel-to-pixel variations than the less averaged images. However, this is due to an optical illusion since the absolute fixed pattern noise is even decreased at a higher averaging level. The false impression is caused by the larger pixel size leading to a higher importance of individual pixels. The slight effective reduction of the remaining fixed pattern noise when averaging neighbouring pixels results from the fact, that not only the photocurrents but also the output voltages of horizontally adjacent pixels are averaged. Consequently, the non-uniformities caused by horizontal pixel-to-pixel variations are somewhat decreased.

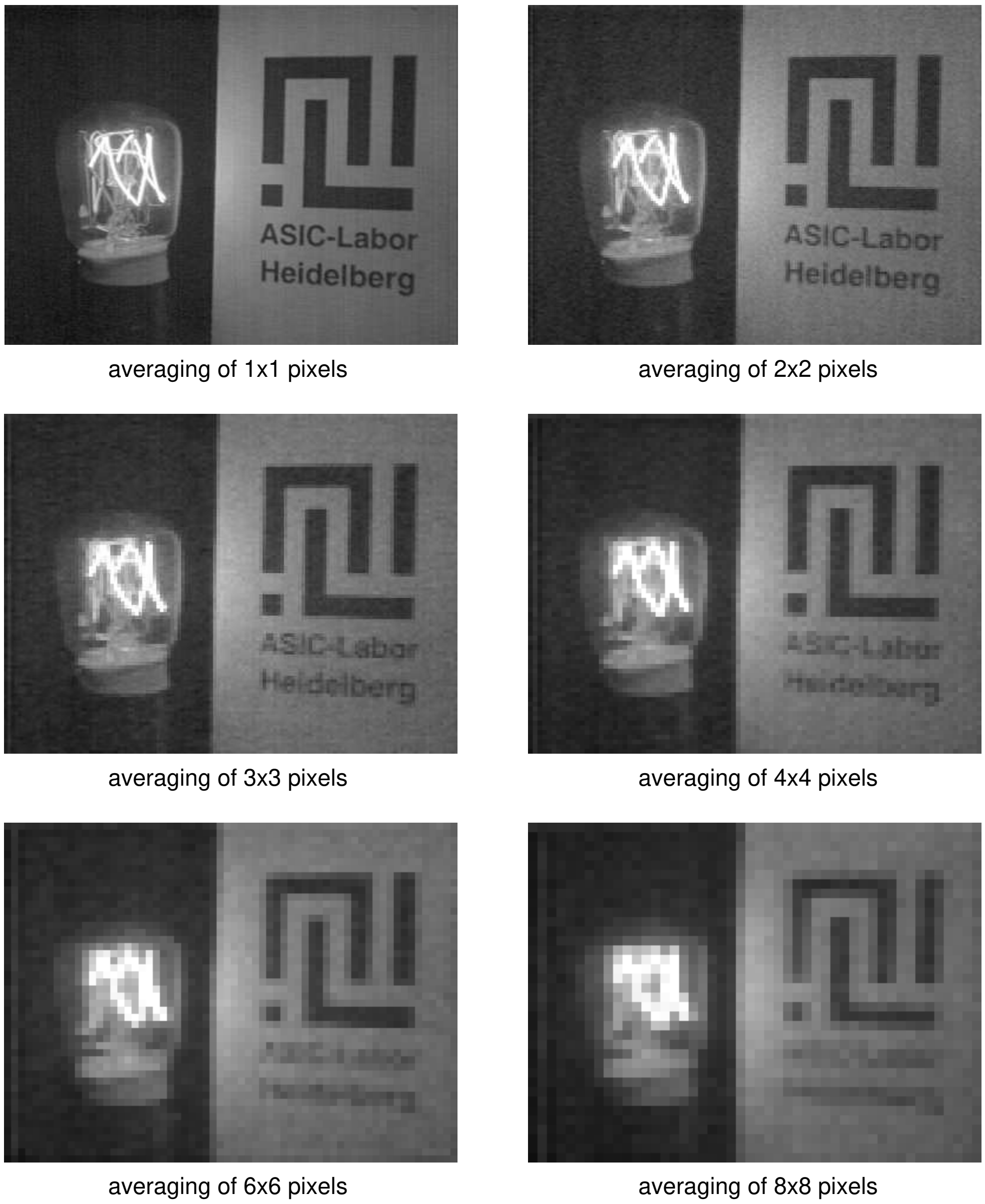


Figure 5.41: The high dynamic range scene of figure 5.34 in different resolutions corresponding to the indicated averaging levels.

5.4.5 Digital Zoom

Finally, some pictures demonstrating the digital zoom capabilities of the camera chip Divichi are presented. This feature is only available in video mode and means that a smaller subpart of the image is mapped to the full video screen. It is obtained by accordingly changing the readout timing including row and column selection and multiplexer control. Consequently, the digital zoom corresponds to the random pixel access in other readout modes.

Figure 5.42 shows the high dynamic range scene from figure 5.34 corresponding to the first four available zoom levels. Since every zoom step means an enlargement of the effective pixel size by one minimum pixel length, the first step from zoom level 0 to zoom level 1 represents the largest difference. One pixel in the zoomed image occupies the space of 2×2 pixels of the unzoomed image and the resolution is divided by four. Changing to zoom level 2, one pixel corresponds to a size of 3×3 original pixels. This means a further reduction of the resolution by a factor of 2.25 compared to zoom level 1. The difference between the individual zoom levels becomes smaller the higher the level number. The maximum selectable zoom level is 31 according to a resolution of 12×9 pixels. In this case, the size of 108 pixels is mapped to the area of 110k pixels resulting in a maximum zoom factor of about 1000 with respect to the area. However, as the highest zoom level only provides the poor resolution mentioned above, the possible applications for this zoom factor are limited.

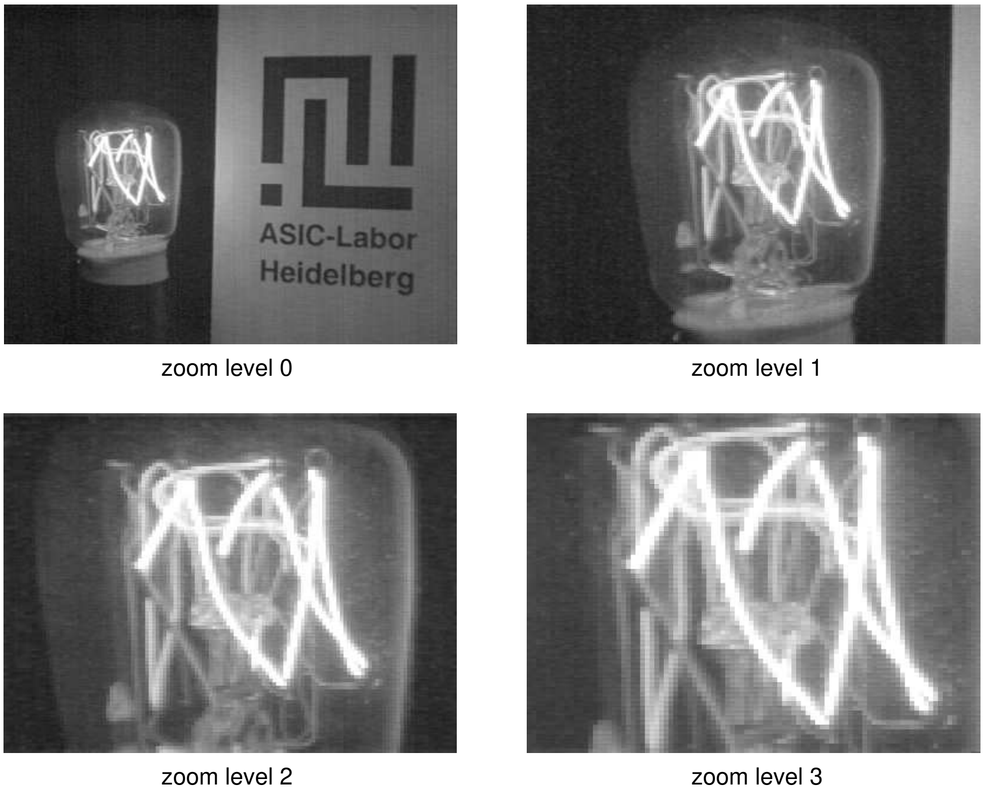
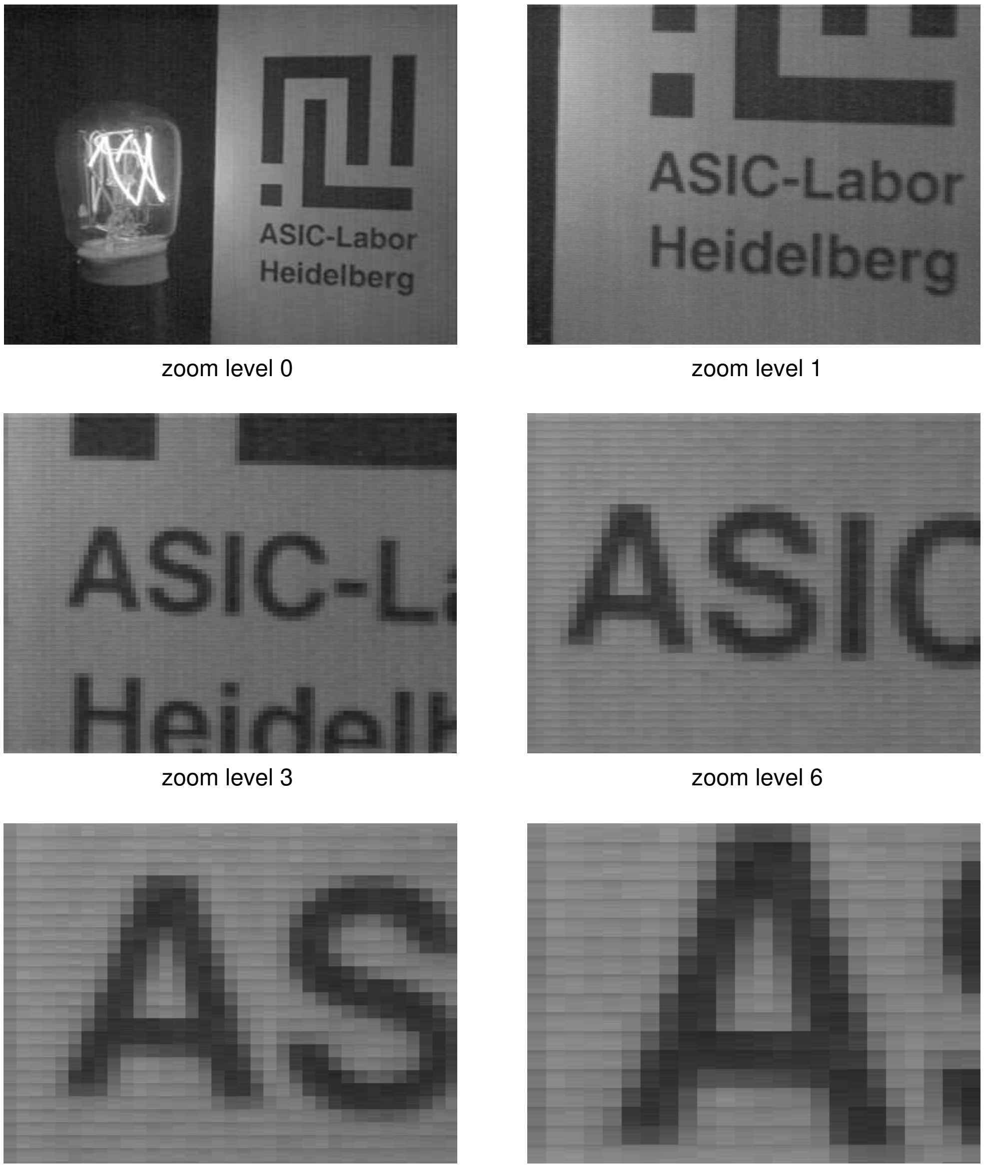


Figure 5.42: Example of the digital video zoom up to zoom level 3.

An example of the zoom feature up to zoom level 15 is given in figure 5.43. Again, the high dynamic range scene is used. This time, a part of the script is enlarged instead of the bulb structure. In the last picture corresponding to level 15, the automatic anti-aliasing characteristic of cameras using a discrete pixel structure can be seen. In contrast to an artificially generated symbol (e.g. the letter A of a computer script), the edges are blurred. Regarding an abrupt optical transition from a dark region to a bright region, some photodiodes are covered by parts of both regions. Therefore, they show a medium grey level representing the corresponding averaged intensity. The result is the observed smooth transition. This anti-aliasing effect is very important in making the scene look natural. Therefore, digitally generated pictures have to be corrected for their sharp edges if a good imitation of a natural scene is required.

The last three pictures (zoom level 6, 10 and 15) show another effect occurring at high zoom factors. Each pixel possesses a slightly darker grey level at the top border resulting in horizontal stripes. The reason for this behaviour is not completely understood. Since the number of video lines (288) stays constant independent of the actual zoom level, the same array row has to be consecutively



zoom level 0 zoom level 1

zoom level 3 zoom level 6

zoom level 10 zoom level 15

Figure 5.43: Example of the digital video zoom up to zoom level 15.

selected several times if a zoom level higher than 0 is chosen. If the pixel value changes before being selected again, the observed grey level variation within one pixel would result. The reason for the change of the pixel value could be caused either by a crosstalk of the selection clock to the storage capacitor or by an incomplete recovery of the pixel voltage after carrying out the calibration cycle. In any case, the effect is relatively small and should not be a big problem in common applications.

Conclusion

Within the scope of this thesis, the concept of a self-calibrating CMOS image sensor, providing a logarithmic response, has been realized and tested. Three prototype chips with resolutions of 64×64 or 96×72 pixels and the final camera chip *Divichi* with 384×288 pixels have been developed and examined with regard to their optical and electrical performance. Besides the self-calibration, Divichi includes all components for working as a single chip camera. A complete camera system mainly consisting of the image sensor, some external electronics, a lens and a housing has been built. The pixel values can be read out either via an analog line or via one of two digital interfaces (parallel or serial) after undergoing an analog to digital conversion on the chip.

Due to the logarithmic response, the image sensor offers a dynamic range of 6 decades of the incident light intensity. In the range from 3 mW/m^2 to 3 kW/m^2, the observed response is indeed almost perfectly logarithmic. The corresponding slope can be varied from 130 to 720 mV/decade by adjusting the gain of the readout amplifier. The self-calibration concept, implemented in each sensor pixel, decreases the overall fixed pattern noise to a standard deviation (rms) of less than 4 % of an intensity decade. This means a significant reduction by a factor of more than 20 compared to uncalibrated logarithmic sensors. The slope variations, calculated from the individual pixel slopes averaged over 3 decades, amount to less than 1 % per decade. However, due to the increased slope variations in the lowermost decade, the fixed pattern noise at an intensity of 10 mW/m^2 rises to 8.5 % of a decade. This worsens the sensor performance in the lower region of the dynamic range.

In contrast to the linear CCD sensors utilized in most of today's electronic cameras, the high dynamic range of the developed image sensor Divichi allows to run the chip under different illumination conditions without using an adjustable optical aperture or changing parameters like the exposure time. In addition, much higher contrasts can be processed within the same image. For digital image processing algorithms, the logarithmic response provides a further advantage since contrasts are no longer represented by ratios, but by differences. Compared to externally calibrated logarithmic CMOS cameras, the self-calibration concept leads to a smaller system (complete camera on a chip) and to a reduced power consumption (about 150 mW).

As the high dynamic range of six decades is mapped to an output signal range of only somewhat more than 2 decades, the major disadvantage of the logarithmic concept becomes clear: The sensitivity for low contrasts is reduced in comparison to typical linear systems. In order to overcome this drawback without losing the high dynamic range, some groups are trying to increase the dynamic range of linear CMOS sensors. This is achieved by either taking several pictures with different exposure times and subsequently combining them or individually controlling the exposure time of each pixel. However, until now, no real single chip solutions with linear response providing the high dynamic range of a logarithmic sensor have been found.

Contrasts of the typical environment like the presented outdoor scenes in chapter 5, however, are still high enough to be detected with the developed image sensor. Due to the implemented self-calibration, the fixed pattern noise is reduced to a level, which should be no problem for use in the tactile vision substitution system TVSS. Here, the attached edge detection chip EDDA additionally reduces the random fixed pattern and temporal noise due to its network architecture. The most noticeable contribution to the remaining fixed pattern noise comes from the column-to-column variations. Though the corresponding rms value does not exceed that of the variations within one column, they are more disturbing due to the geometrical correlation (vertical stripes). The obtained alternating structure from column to column, caused by the two independent readout lines, can be somewhat reduced by both changing the gain of the readout amplifier and selecting chips with a low intrinsic mismatch between the two readout lines.

Another disadvantage of the realized self-calibrating photoreceptor is the large pixel size of $24 \times 24\,\mu\text{m}^2$. The resolution of 100k pixels, realized with the image sensor Divichi, already results in a chip size of nearly 100 mm^2. Higher pixel numbers would further increase the required chip area leading to higher production costs, worse yield and larger camera systems. Furthermore, the total chip size is limited to a certain value depending on the applied CMOS process due to the production equipment. Therefore, the maximum reasonable resolution, which can be achieved at this time with the designed photoreceptor, amounts to about 250k pixels.

Some of the described drawbacks could be overcome or reduced by using a smaller CMOS process or improving the circuit design and the layout implementation. However, no quantum leap should be expected with respect to the remaining fixed pattern noise. Since it is already reduced to the charge injection variations of the switch transistors, only larger storage capacitances and MOS switches would lead to an improvement. But, by this means, the pixel size increases. Merely the column-to-column variations could be decreased by a better layout of the concerned feedback capacitances.

Using a CMOS process with smaller structure sizes (e.g. 0.35 μm or 0.25 μm) allows integrating the self-calibrating photoreceptor concept on a smaller chip area. Unfortunately, as the quantum efficiency in principal stays constant independent of the actual process, the size of the photodiode cannot be reduced without decreasing the sensitivity. Therefore, the pixel size does not decrease by the same amount as the structure size of the CMOS process. In the case of a 0.35 μm process, a pixel size of somewhat less than $20 \times 20\,\mu\text{m}^2$ may be expected. However, a new process should be first evaluated with respect to the charge injection variations and the subthreshold slope variations in order to guarantee the low level of the remaining fixed pattern noise.

Despite the problems mentioned above, the image sensor Divichi can be used for many applications in its current form. Especially in the case of high dynamic range scenes, the remaining fixed pattern noise is negligible. Nevertheless, a redesign would be necessary, if the sensor chips should be mass-produced. The reason is, that the current implementation provides a yield of less than 10 %. Most of the sensor defects are caused by damaged pixels, array rows or array columns. Therefore, the yield could be significantly increased without reducing the effective resolution too much by switching off the malfunctioning devices. This functionality can be realized by storing the number of the damaged line and reading out the adjacent line instead. This means only a small change in the digital control part without influencing the analog components and the overall chip performance.

Appendix A

ADC Design and Performance

In order to perform any kind of digital image processing, which is a common application in the field of image sensors, the analog sensor values have to be converted into digital values. As the CMOS process allows to integrate sensors and processing electronics on the same chip, the analog-to-digital conversion in the case of CMOS cameras can be carried out directly on the sensor chip. By this means, the analog signal has to travel only a short distance and is less disturbed compared to using an external ADC[1]. Besides, the image sensor still represents a single-chip solution which, in many cases, leads to a cost reduction and a smaller camera system.

For this reason, the image sensor Divichi contains an ADC on the chip providing a resolution of 10 bit and a maximum sample rate of 8 MHz. It represents a two-step flash converter with a latency[2] of two clock cycles. The concept of integrating one single high speed ADC is different from many other CMOS image sensors with on-chip digitization [KWO99, SCH97], using as many converters as array columns in parallel. The advantage of the parallel concept is in the slower conversion rate of each individual ADC. This allows to implement simpler concepts (e.g. single and double slope methods) and to achieve a lower power consumption. However, the parallel method fails, if a random pixel access with faster readout of subframes is required. In this case, only a part of the column ADCs can be used, since only the columns corresponding to the selected subframe are read out. This means, that subframes would be acquired at a slower pixel rate. Therefore, Divichi contains only one, but fast ADC converting the signal level of the multiplexed analog output line. By this means, the pixel rate is at the maximum level independent of the selected subframe or averaging level. A summary of diverse ADC concepts is given in [PLA94] and [ALL87-3].

A.1 Architecture

The straight forward implementation of a high speed analog-to-digital converter is given by the *flash ADC* concept. The analog input signal is simultaneously compared to $2^n - 1$ monotonously increasing voltages corresponding to the different digital values. The integer n is the ADC resolution. Consequently, $2^n - 1$ comparators are required. In the case of an 8 or more bit resolution, this means a considerable power and space consumption. For this reason, high resolution ADCs usually consist of several stages successively determining the individual bits of the digital output data. The more steps are used, the lower the power consumption but the higher the latency between sampling point and valid output data.

[1] ADC: analog-to-digital converter

[2] time between analog sampling point and valid output data

The block diagram of the two step concept integrated in the image sensor Divichi is shown in figure A.1. It consists of a 5 bit coarse stage generating the upper bits (MSBs[3]) and a 6 bit fine stage determining the lower bits (LSBs[4]). Each stage is realized in a flash architecture using 30 and 63 comparators, respectively. The required reference voltages are generated by a chain of 1024 resistors in series. The upper and lower end of this chain are connected to the voltages V_{ref+} and V_{ref-} representing the limits of the analog input range. Since all chain links show the same resistance, the resulting reference voltages are equidistant.

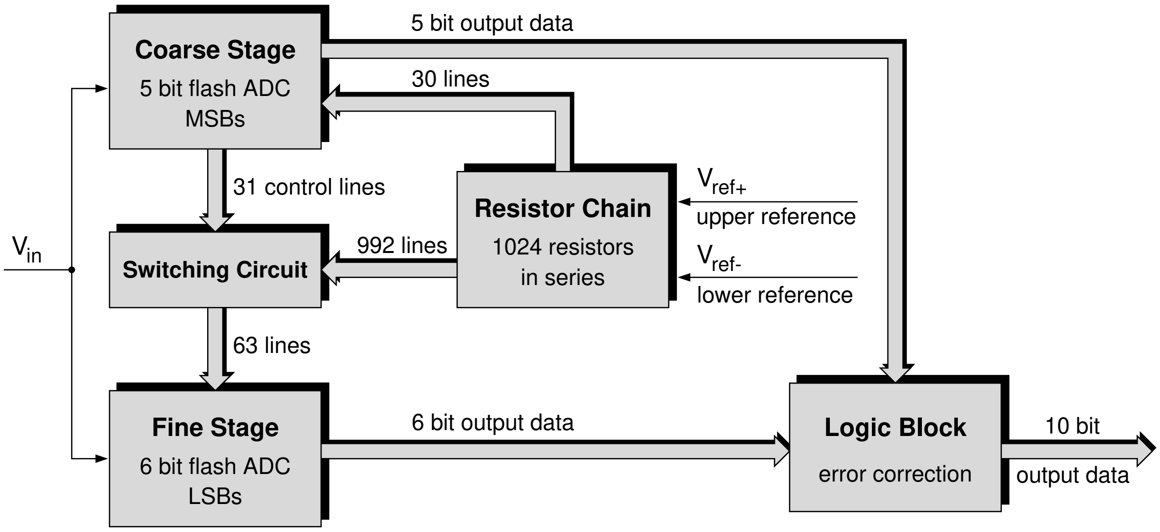


Figure A.1: Block diagram of the Divichi two-step flash ADC.

The 30 reference voltages for the coarse stage are fixed. They correspond to 30 voltages of the resistor chain with a distance of 32 resistors between two voltages in each case. The first coarse voltage equals the 48th resistor chain voltage, the second one the 80th, the third one the 112th and so on. Depending on the result of the analog-to-digital conversion of the first stage, a subpart of the chain containing 63 reference voltages is mapped to the second stage (fine stage). This mapping is carried out by a switching circuit decoding the 5 bits from the coarse stage and connecting the reference input signals of the fine stage to the corresponding voltages of the reference chain. If, for instance, the coarse stage generates a digital value corresponding to an analog value between the 5th and the 6th reference line (which are the $16 + 32 \times 5 = 176$th and the $16 + 32 \times 6 = 208$th voltage of the resistor chain), the 63 lines from reference voltage 161 to reference voltage 223 are connected to the fine stage. In other words, the first stage detects the subrange in which the input signal is located. Then, the second stage only regards this subrange for determining the signal value with a higher resolution.

Although a digital output value of only 10 bits is required, the sum of coarse (5 bits) and fine stage (6 bits) amounts to 11 bits. This produces an overlap between the MSBs and the LSBs which can be used for performing a digital error correction. Otherwise, a small offset error of the coarse comparators could already lead to the selection of a wrong subrange. In this case, the input signal would not correspond to any of the selected fine reference voltages and thus could not be detected by the fine stage.

[3] MSB: most significant bit

[4] LSB: least significant bit

To be able to adapt the ADC's input range to the actual input signal, the global reference voltages V_{ref+} and V_{ref-} are not fixed but can be adjusted to any value between ground and V_{dd}. Since the complete reference chain has the low resistance of about 1 kΩ, V_{ref+} and V_{ref-} have to be buffered by an amplifier with a very low output resistance. The required buffers have been omitted in the diagram but are also implemented on the sensor chip. The analog input signal is buffered by the video amplifier (cf. section 4.4.5). It is able to drive the input capacitance (about 10 pF) of the ADC in the required time of less than 60 ns. In addition, the sample-and-hold stage, already integrated for the analog readout, can be used for fixing the signal during the conversion cycle.

A.2 CMOS implementation

The following sections describe the individual components of figure A.1 with respect to the concrete realization in the AMS 0.6 μm CMOS process. The design uses 3 metal layers and one poly layer. Due to the missing second poly layer, it can be easily adapted to other digital CMOS processes. However, since no poly-poly capacitors are possible, capacitances are realized either as MOS transistors or, if a good linearity is necessary, as metal-metal-poly sandwich structures.

A.2.1 Architecture of coarse and fine stage

Basically, the coarse and the fine stage consist of the same components. Both architectures follow the principal circuit diagram of the 4 bit flash ADC shown in figure A.2. This structure is composed of three main blocks indicated as comparators & flipflops, thermometer converter and data encoder. In the case of the 4 bit converter, each block includes 15 cells (10 cells have been omitted in the diagram) corresponding to the 15 different reference voltages V_{ref1} to V_{ref15}. The coarse stage (5 bit) contains 30 cells and the fine stage (6 bit) 63 cells per block.

The operation principle is as follows: As soon as the clock CMPCLK switches, the input voltage V_{in} is compared to the different reference voltages by the 15 comparators COMP1 to COMP15. If V_{in} is higher than one of the reference voltages, the corresponding comparator raises its output. Otherwise, the output stays low. As the reference voltages monotonously increase from V_{ref1} to V_{ref15}, all comparators below a certain number show a high output and all comparators above that number a low output. The exact transition point is determined by the analog input signal. After the comparators have made their decisions, the current output levels are stored in the memory flipflops FF1 to FF15 by rising the clock FFCLK.

The next block is called *thermometer converter* as it has to find the end of a column consisting of high level signals which is similar to the mercury column in a thermometer. The transition point, at which the signal level changes from high to low, corresponds to the value of the analog input voltage. The detection of this point is carried out by using nand-gates combining the inverse output $\overline{Q}$ of one flipflop with the normal output Q of two neighbouring cells. The output of the nand-gate is always high, unless all input signals show a high level. This case, however, can only occur, if two flipflops store a high and one a low value corresponding to the sought transition.

The use of three adjacent cells instead of only two, which would be sufficient for detecting the high-low transition, means an additional error correction. If, for instance, one comparator does not work properly (e.g. always shows a high output level or possesses a high input offset), the high-low pattern could occur two or even more times. It is important to detect only one of them in order to generate a reasonable output value. Therefore, single errors in the thermometer column are suppressed by considering three instead of two flipflop outputs. In the fine stage, this error correction method has been further expanded by using nand-gates with five input lines taking into account the

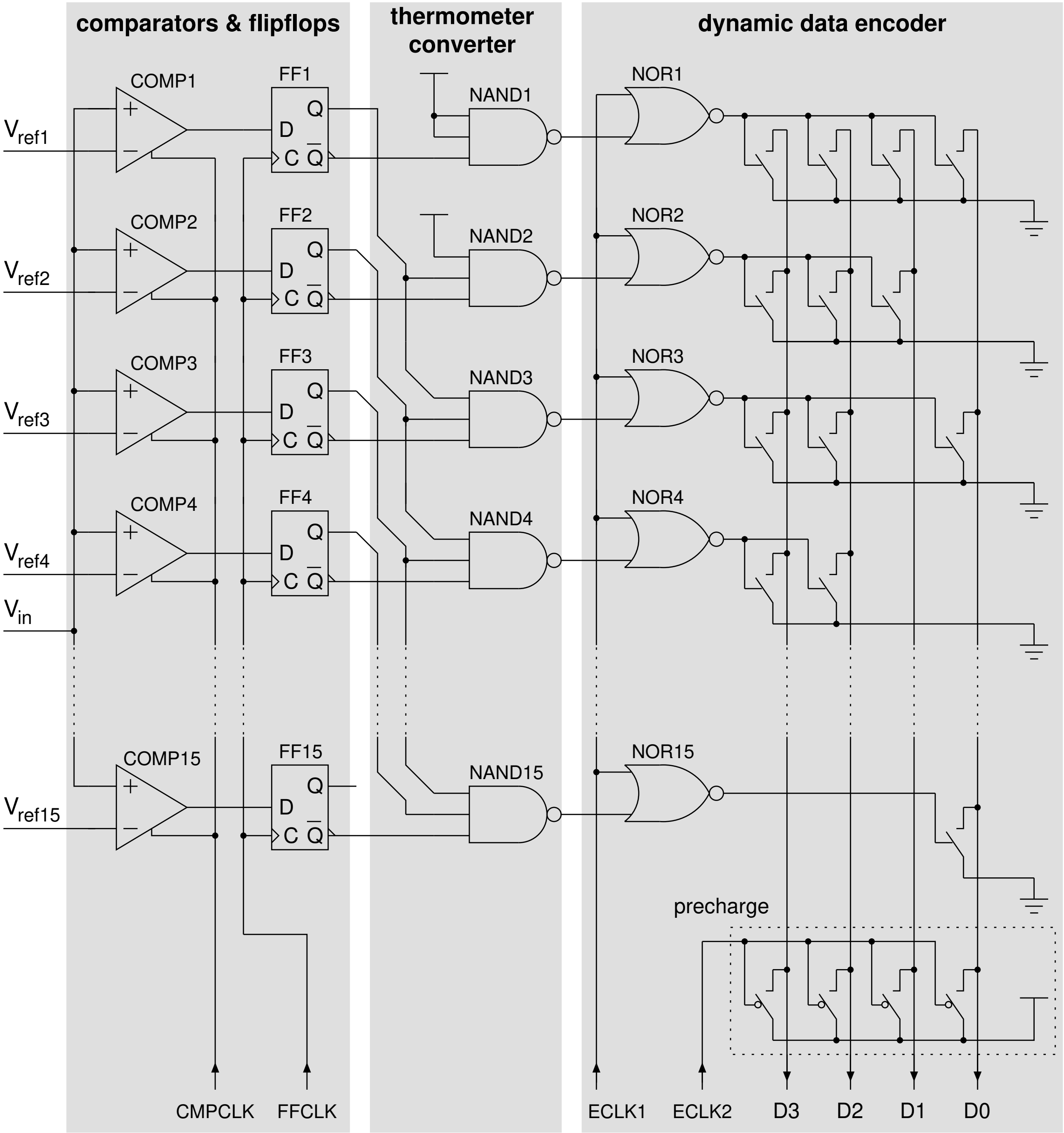


Figure A.2: Circuit diagram of a 4 bit flash ADC. This concept is basically used for the coarse and the fine stage of the Divichi ADC.

signal of five adjacent cells. This is required, because the reference voltage difference between two cells can be very small ($\approx 1\,\text{mV}$) and the individual comparator offsets could cause more than only one false output level in series.

Finally, the detected position of the high-low transition has to be converted into a binary coded digital value. This is done by the *data encoder* generating the four data bits D0 - D3. The conversion is carried out in two steps. At first, the encoder clock ECLK1 is high and ECLK2 is low. By this means, the nor-gates NOR1 to NOR15 show a low output disabling the encoder switches of the individual ADC cells. At the same time, the data lines D0 - D3 are precharged to the upper supply voltage V_{dd} by the switches drawn at the bottom of the diagram. In the next step, ECLK2 changes to a high level. Due to their parasitic capacitances, the data lines stay at the high level, although they are no longer connected to V_{dd} (except for weak pull-up resistors). Finally, ECLK1 goes low and leads to a high output signal of the nor-gate corresponding to the previously detected high-low transition of the comparator chain. This high signal activates the switches according to the position of the concerned cell. Some data lines are pulled down, whereas others stay at the high level. The resulting pattern of the four data lines represents the digital value of the analog input voltage.

The data encoder is called *dynamic*, since the high level of the data lines is not actively driven (after precharging), but held by the parasitic capacitance of the line. By this means, no DC current flows through the encoder as would be the case if using active pull-up resistors. The consequence is a significantly reduced power consumption. In order to prevent the data lines from losing their potential, weak pull-up resistors ($> 1\,\mathrm{G\Omega}$) have been added compensating for parasitic currents (e.g. leakage currents or photocurrents).

A.2.2 Comparator circuit

Typical continuously working comparator circuits like the one used in the output mixer stage of Divichi (figure 4.26) suffer from relatively large input offsets of at least a few mV. This is too much with respect to the required ADC resolution, since 10 bit in a voltage range of 1 V corresponds to a difference of about 1 mV between the individual reference voltages. For this reason, a clocked comparator circuit has been chosen which automatically compensates for its intrinsic offset. Figure A.3 shows the circuit diagram consisting of 3 inverter stages, two capacitors and four switches implemented as transmission gates. The inverter stages are realized as simple CMOS inverters including one NMOS and one PMOS transistor.

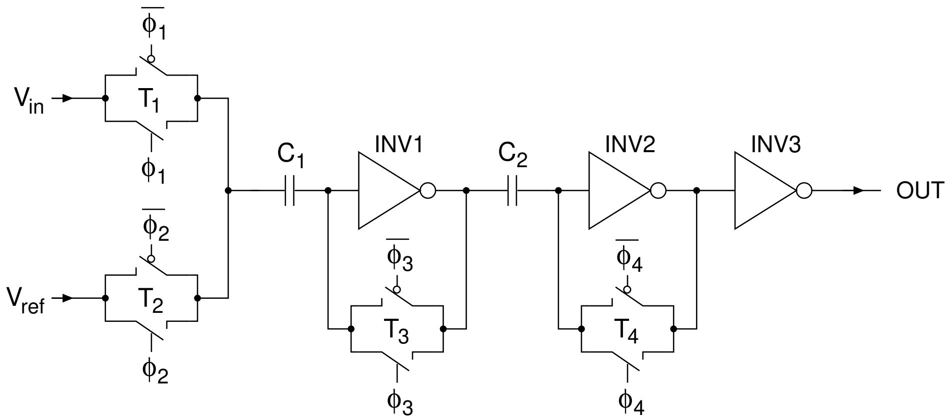


Figure A.3: Schematic diagram of the comparator used for the coarse and fine flash ADCs.

In order to understand the operation principle of the comparator, the timing diagram of the concerned clock signals is given in figure A.4. In can be divided into 2 parts, the offset correction cycle and the comparing cycle. The offset correction cycle is composed of two sub-cycles performing the main offset correction and the charge injection cancellation in the first inverter stage. With the help of the timing diagram, the behaviour of the comparator is explained in the following.

At first, the comparator changes to the offset correction mode by disabling the transmission gate T_2 (low ϕ_2) and rising the clock signals ϕ_1, ϕ_3 and ϕ_4 to enable the transmission gates T_1, T_3, and T_4. The voltage V_{in} is connected to the input node of C_1 and the outputs of the first and second inverter stage are fed back to the corresponding inverter inputs. Due to the feedback loop, the inverter input

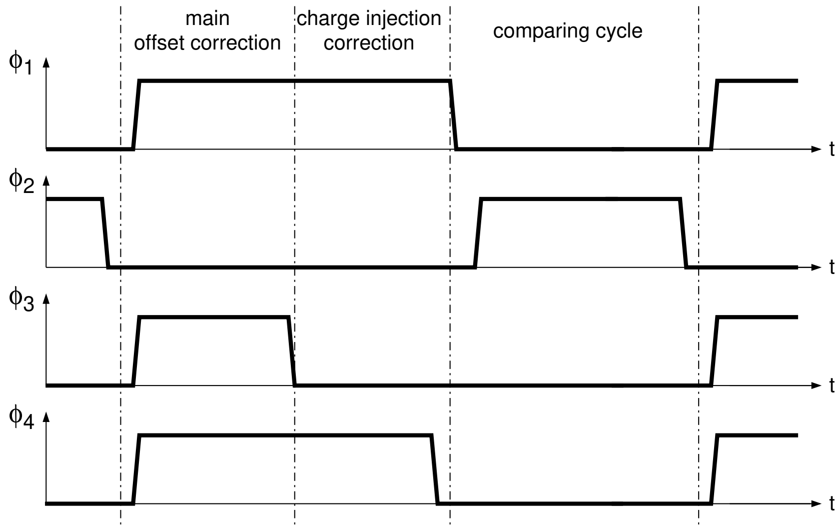


Figure A.4: Timing diagram of the comparator control clocks.

and output voltages will go to a level somewhere in the middle of the power supply range. The exact value depends on the transistor properties and varies from one inverter to the next owing to the transistor mismatch. The capacitor C_1 is charged to the difference between the input voltage V_{in} and the first inverter voltage. It therefore compensates for the intrinsic inverter offset. The same happens to the capacitor C_2 and the second inverter stage.

Subsequently, ϕ_3 goes low and interrupts the feedback of the first inverter stage. Since the switching-off process of the transmission gate T_3 causes a charge injection onto C_1, a slight voltage shift at the input of INV1 occurs. This leads to a changed output voltage of INV1 according to the gain of the inverter. The second stage, however, is still in the offset correction mode and therefore compensates for the additional charge injection offset. Finally, ϕ_4 goes low and terminates the correction cycle of the second inverter. The influence of the charge injection caused by the transmission gate T_4 can be neglected as it has to be divided by the gain of the first inverter stage ($\approx$ 100). Using the described two-step offset correction method results in remaining offsets of a fraction of 1 mV which should be enough for the 10-bit ADC.

For the comparing mode, T_1 is opened and T_2 is closed connecting the reference voltage V_{ref} to the comparator input. Depending on the difference between V_{in} and V_{ref}, the input voltage either decreases or increases. A lower reference voltage means a lower input for INV1 resulting in a higher output of INV1. Consequently, INV2 detects an increased input voltage leading to a decreased output signal. Finally, the output of INV2 is amplified and inverted again by the third inverter INV3 and results in a high output signal of the total comparator.

The total gain of the comparator is given by the product of the gain factors corresponding to the individual inverter stages. Regarding the first stage, the gain depends on the intrinsic inverter gain and the ratio of C_1 to the input capacitance of the inverter C_{inv1}. Therefore, C_1 should be as large as possible. However, a large C_1 on the one hand means a large input capacitance of the ADC and on the other hand slows down the offset correction cycle, since it has to be charged by the output of the relatively weak inverter stage. Hence, the actual size of C_1 (and C_2) represents a tradeoff. In the fine stage, C_1 and C_2 amount to 100 fF. As the input capacitance of INV1 is about 10 fF, the gain is reduced by 10 % due to the capacitive divider. The total gain of the comparator is more than 10000 allowing generation of the full output swing at input differences down to 1 mV. In case of the coarse

ADC, the second correction cycle for compensating for the charge injection in the first comparator stage has been omitted. It is not required, since the coarse decision is made using reference voltage differences of more than 30 mV. This is higher than the voltage shift caused by the charge injection onto C_1. The capacitor values of the coarse stage amount to $C_1 = 200\,\mathrm{fF}$ and $C_2 = 100\,\mathrm{fF}$. In both ADC stages, C_1 and C_2 are implemented as metal-metal-poly sandwich structures.

A very important point concerning the design of a comparator is the timing behaviour. It is determined by the speed of the individual inverter stages combined with the respective capacitive load. The frequency behaviour can be easily improved by increasing the current through the inverter transistors. By this means, however, the power consumption would also significantly increase. In order to reduce the capacitive load of the first inverter, a source follower has been inserted driving the input capacitance of the second inverter stage. The complete comparator of the fine stage, which is capable of making a decision in less than 50 ns, requires a quiescent current of about 50 μA. The corresponding transistor dimensions are $W/L = 0.8/2$ for INV1 and $W/L = 0.8/3$ for INV2. The simulated frequency response belonging to the three comparator stages is shown in figure A.5. Multiplied by 63 (number of comparators), the power consumption of the fine stage amounts to 5 V $\times$ 50 μA $\times$ 63 $\approx$ 16 mW. The comparators of the coarse stage need about the same current and give another contribution of almost 10 mW (30 comparators).

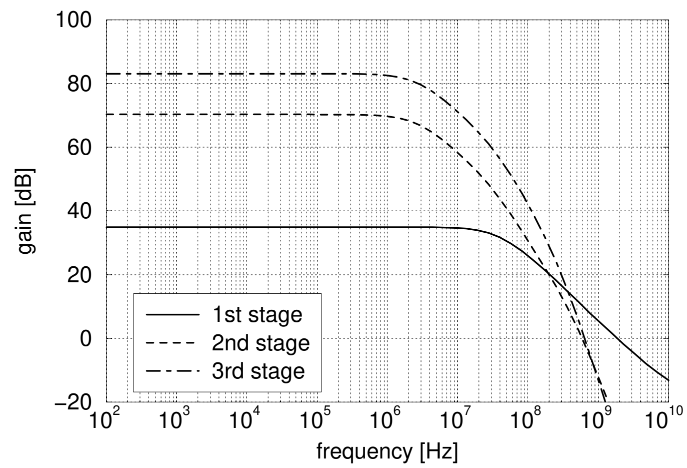


Figure A.5: Simulated frequency response of the comparator used for the fine ADC stage. The gain after the first, the second and the third inverter stage is plotted.

A.2.3 Resistor chain and switching circuit

The resistor chain generating the reference voltages for the coarse and fine ADC stages consists of 1024 resistors of 1 Ω each, arranged in a structure of 16 columns. Every column includes 64 resistors. The first four columns of the corresponding circuit diagram are shown in figure A.6. In addition to the resistor chain (highlighted in grey), the switches selecting the 63 reference voltages for the fine stage according to the current data of the coarse stage are drawn. The vertical selection lines are activated if the digital output of the coarse stage equals the indicated value. Each line controls 63 transmission gates which are drawn as single switches for the sake of simplicity.

If the coarse data is 0, the first resistor column is selected corresponding to the 63 lowest reference voltages. They are guided to the comparators of the fine stage by 63 lines indicated with C1 - C63. A coarse output of 1 enables the second selection line. Now, the lower half of the first and the lower

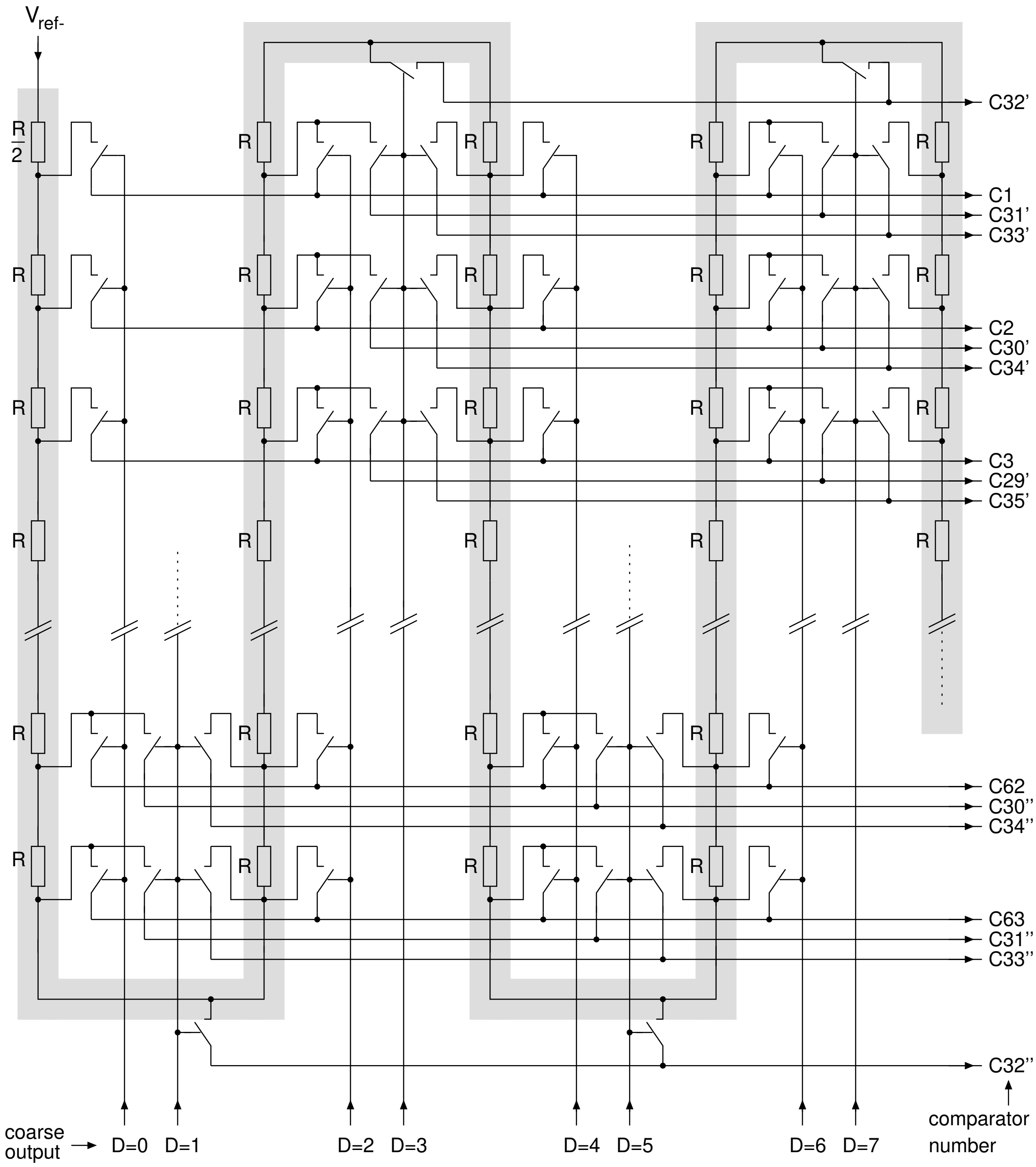


Figure A.6: Circuit diagram of the first 4 resistor chain columns combined with the switches mapping a subpart of 63 reference voltages to the fine ADC stage.

half of the second resistor column are connected to the fine stage. Increasing the coarse data by one selects all voltages of the second column and a coarse output of 3 enables the upper half of the second and the upper half of the third resistor column. A further increase of the coarse data repeats the described cycle for the following columns 3 to 16.

Using the described selection pattern leads to the following situation: If an odd resistor column is enabled, the line C1 corresponds to the lowest and C63 to the highest reference voltage of the current subrange. If, however, an even column is selected, C1 transmits the highest and C63 the lowest voltage. For this reason, the thermometer converter in figure A.2 has to detect a high-to-low transition as well as a low-to-high transition depending on the actual direction of the reference voltages (decreasing or increasing with rising comparator number). Therefore, the fine stage contains two thermometer converters, one for the increasing and one for the decreasing voltages.

The low resistance of 1 Ω per resistor resulting in about 1 kΩ for the complete chain is necessary to provide enough current for charging the input capacitances in the required time. Taking into account the total input capacitance of 6 pF of the fine stage, the resistance of 1 kΩ gives an RC-time constant of 6 ns. To achieve an accuracy of 0.1 % (10 bit), this time has to be multiplied by 7, because $e^{-7} \approx 0.001$. This means, that in the worst case, the voltages have settled not until 42 ns have passed corresponding to more than half of the total conversion time of 60 ns. Consequently, the resistance can not be increased without worsening the ADC performance.

Two problems are caused by the low resistance of the reference chain. Firstly, a high quiescent current flows through the resistors leading to a remarkable contribution to the total power consumption. Secondly, the resistors have to be implemented as metal lines, since the resistance of the normally used poly layer is too high. As the thickness of the metal layer is less precisely controlled than that of the poly layer, a higher non-linearity of the final ADC may be expected. However, it should still amount to an uncritical value.

A.2.4 Reference voltage buffering

The ends of the resistor chain are fixed to a certain potential (upper and lower reference voltage V_{ref+} and V_{ref-}) determining the overall input range of the ADC. In order to adapt this range to the actual requirements, both reference voltages can be adjusted by two channels of the integrated bias generating DAC (cf. section 4.5). As the output resistance of the DAC buffers is too high for driving a load of 1 kΩ, additional buffers with a lower output resistance have to be inserted.

Figure A.7 shows the principal circuit diagram of the complete reference system consisting of the resistor chain and two buffers for the upper and lower reference voltage. Each buffer is composed of a typical differential input stage, indicated by AMP1 and AMP2, which is similar to the first stage of the readout amplifier in figure 4.25. It includes a differential transistor pair connected to a current mirror load. An additional transistor provides the quiescent current. Since the input voltage range of the differential stage is limited depending on the transistor types, an NMOS stage has been used for the upper and a PMOS stage for the lower reference voltage. This allows to vary the upper reference in the range from 1.5 V to 5 V and the lower one in the range from 0 V to 3.5 V. However, the difference between both voltages should not exceed 3 V corresponding to a resistor current of 3 mA. Otherwise, the current would be higher than the maximum value specified by the CMOS process parameters for the implemented metal resistors.

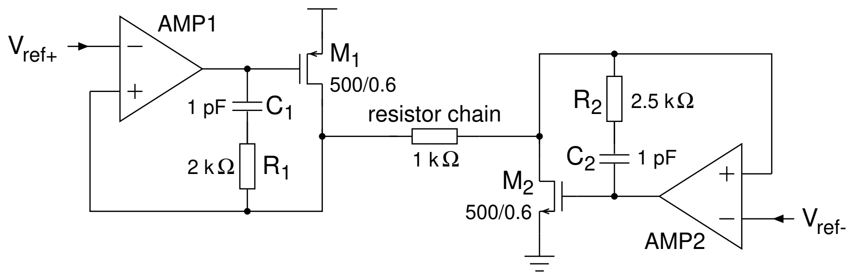


Figure A.7: Circuit diagram for the buffering of the upper and lower reference voltage.

The second stage of the reference voltage buffers consists of one transistor and the resistor chain itself forming an inverting amplifier. In order to achieve a high transconductance g_m, the transistors have a wide channel with $W/L = 500/0.6$. This leads to a minimum transistor resistance much lower than 1 kΩ ($\approx 20\,\Omega$) allowing the amplifier output to nearly reach the upper and lower supply voltage. The output is directly fed back to the positive input of the differential stage forcing the output voltage to follow the input potential (voltage follower).

For the frequency compensation, the capacitors C_1 and C_2 are inserted slowing down the input stage by causing a high output load. Due to the Miller effect, the capacitance of 1 pF is additionally increased by the gain of the output stage. The resistors R_1 and R_2 compensate for the feed forward path through C_1 and C_2 essentially influencing the stability behaviour. The voltage buffers require no external bias voltage, since the bias currents for the differential input stages are automatically generated by a few transistors included in the first buffer stage.

A.2.5 Digital logic

In order to obtain an overlap between the individual voltage ranges mapped to the fine stage, the sum of the bits from the coarse and the fine stage amounts to 11. The excessive bit (the ADC resolution is only 10 bit) is used to perform a kind of error correction compensating for a possible offset of the comparators in the coarse stage. The block diagram of the corresponding logic block is shown in figure A.8.

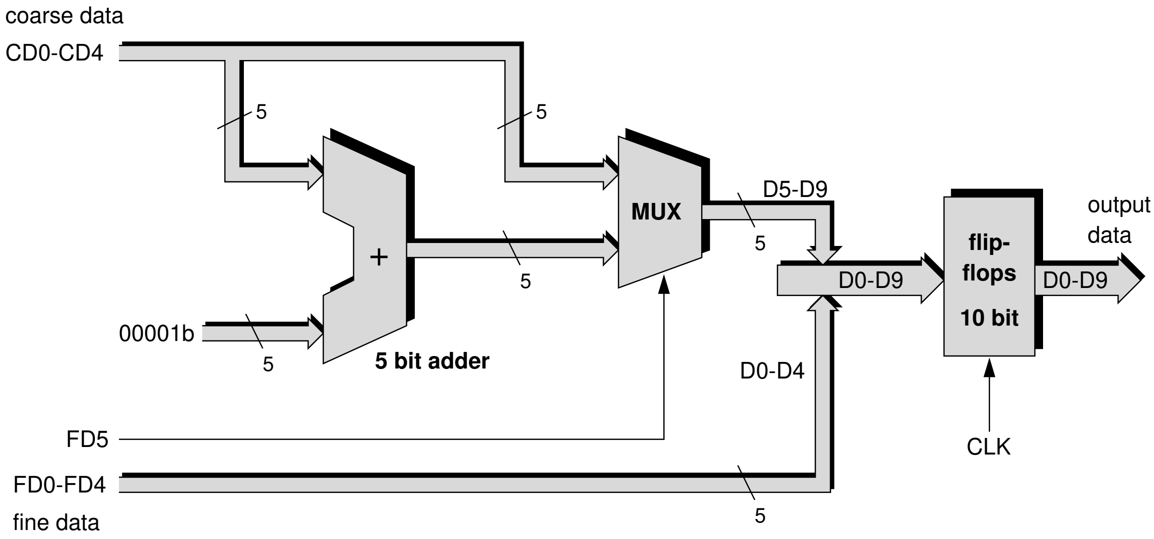


Figure A.8: Block diagram of the digital logic block combining the MSBs (coarse data) and the LSBs (fine data).

The coarse data bits are indicated as CD0 to CD4 and the fine data bits as FD0 to FD5. The lowest fine data bits FD0-FD4 are directly guided to the output memory register and represent the lower 5 bits D0-D4 of the 10 bit ADC output. The coarse data is fed to a 5 bit adder which increments the data by 1. Subsequently, the adder output as well as the original coarse data go to a multiplexer connecting one of its inputs to the output. The control line of the multiplexer, driven by the sixth bit of the fine stage FD5, decides, which input bus has to be actually enabled. A high level selects the incremented, a low level the original data of the coarse stage. The multiplexer output lines correspond to the upper 5 bits D5-D9 of the 10 bit ADC output and are also guided to the output memory register. The register flipflops are controlled by the main ADC clock and allow to easily integrate the ADC into a synchronous logic design.

The reason for the described implementation of the ADC logic is, that the highest fine bit FD5 and the lowest coarse bit CD0 correspond to the same bit of the total ADC output, namely D5. This means, that in the case of a low FD5 the 5 upper bits D5-D9 of the 10 bit output are given by the original coarse data CD0-CD4. If, however, FD5 changes to a logical one, the equivalent coarse bit CD0 has to be also increased by 1. Since this could cause an overflow affecting the higher bits CD1-CD4, all bits are taken into account by using a 5 bit adder. Finally, the incremented coarse data represents the upper 5 bits of the ADC output.

The adder and multiplexer logic has been implemented using the digital standard cell library of the AMS 0.6 μm process. The structure can be significantly simplified since, on the one hand, one operand of the adder is fixed to 1 and, on the other hand, adder and multiplexer can be combined to a single component. The final implementation except for the flipflops merely requires 9 standard cells containing about 70 transistors.

A.2.6 Layout

The concrete implementation of the described 10 bit two-step flash ADC has been realized in the AMS 0.6 μm CMOS process. The design uses 3 metal and one polysilicon layer and is included in the image sensor Divichi. Figure A.9 shows the complete layout and the principal floor plan indicating the position of the main components. Compared to the image sensor layout in figure 4.49, it is rotated by 180°. The size amounts to $736 \times 2455\,\mu\text{m}^2 = 1.8\,\text{mm}^2$. If the ADC should be used for other applications, the sample-and-hold stage, which is shared with the analog readout in the case of Divichi, has to be added. This would give a maximum additional contribution of about 0.1 mm^2 to the total size.

At the top of the layout, the two reference voltage buffers can be found. They provide the upper and lower reference potential for the resistor chain located at the left side of the design. A relatively large part is occupied by the signal routing between resistor chain and the comparators of the fine stage. The right side of the ADC contains the 63 cells of the fine stage including input transmission gates, comparators and 6 bit data encoder. The coarse stage composed of 30 identical cells can be seen at the bottom. Additional blocks for the digital logic, the clock generation and the signal routing complete the floor plan.

Figure A.10 shows three cells of the fine stage in an enlarged view. The individual components like first and second comparator stage and thermometer converter are labelled. As already mentioned, the comparator capacitances have been realized as poly-metal-metal capacitors since no second poly layer, required for the usually used poly-poly capacitors, was available. This is the reason for the relatively large capacitor size despite their small capacitance of 100 fF. In order to prevent large drops of the supply voltages in the case of many switching comparators, additional power blocking capacitors have been integrated. They amount to 1.8 pF per cell and consist of a MOS transistor providing a high capacitance per unit area.

It should be noted that all clock lines controlling the diverse switches in the two ADC stages and the resistor chain are implemented as differential signals. The positive and negative clock signals are always layed out in parallel lines. By this means, the resulting crosstalk between the clock lines and the sensitive analog signals can be significantly reduced. All control signals are generated at the border of the two ADC stages by individually designed clock driver circuits. Only one external clock is required to run the complete ADC.

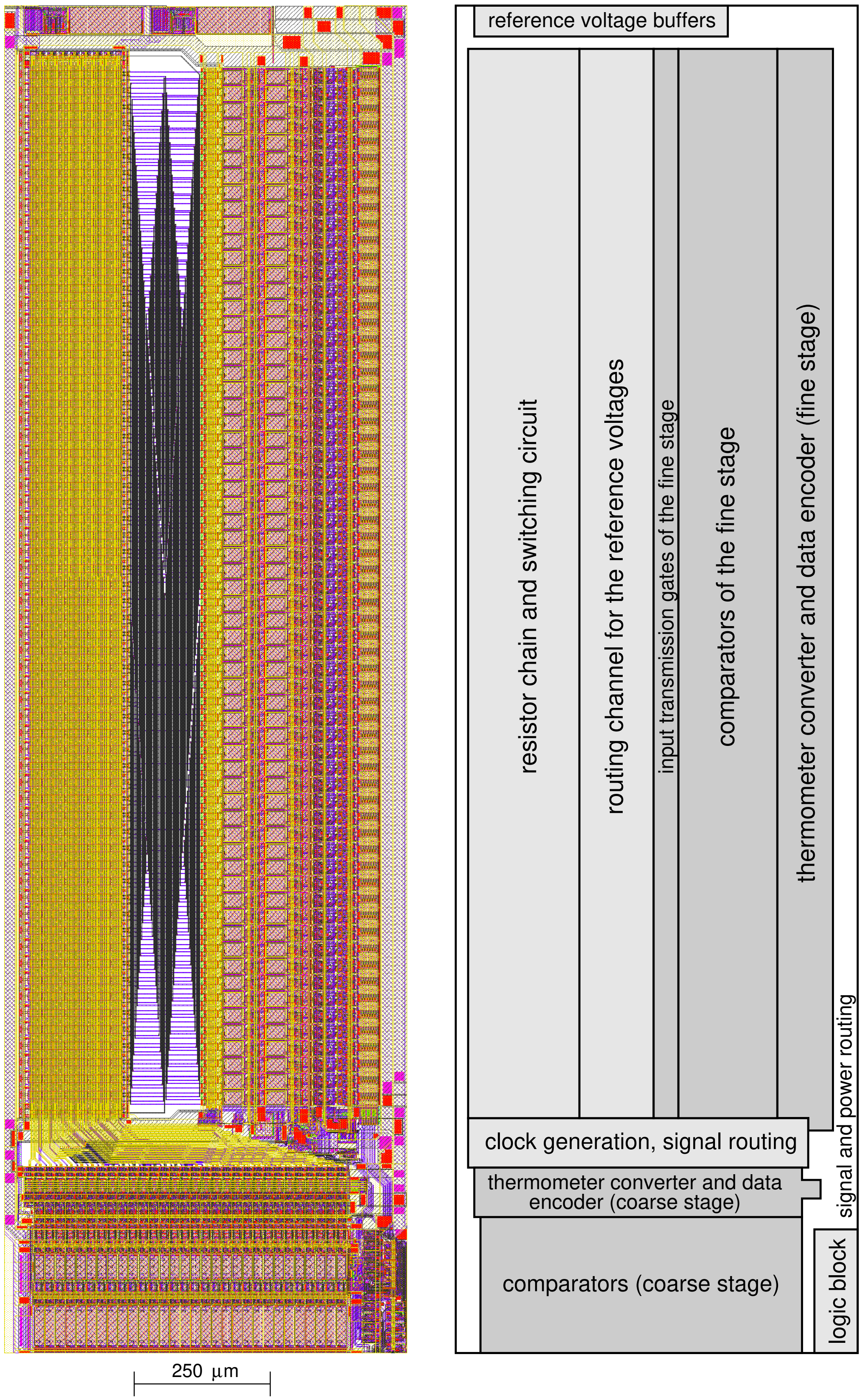


Figure A.9: Layout and floor plan of the two-step flash ADC. The size is $736 \times 2455\,\mu\mathrm{m}^2$.

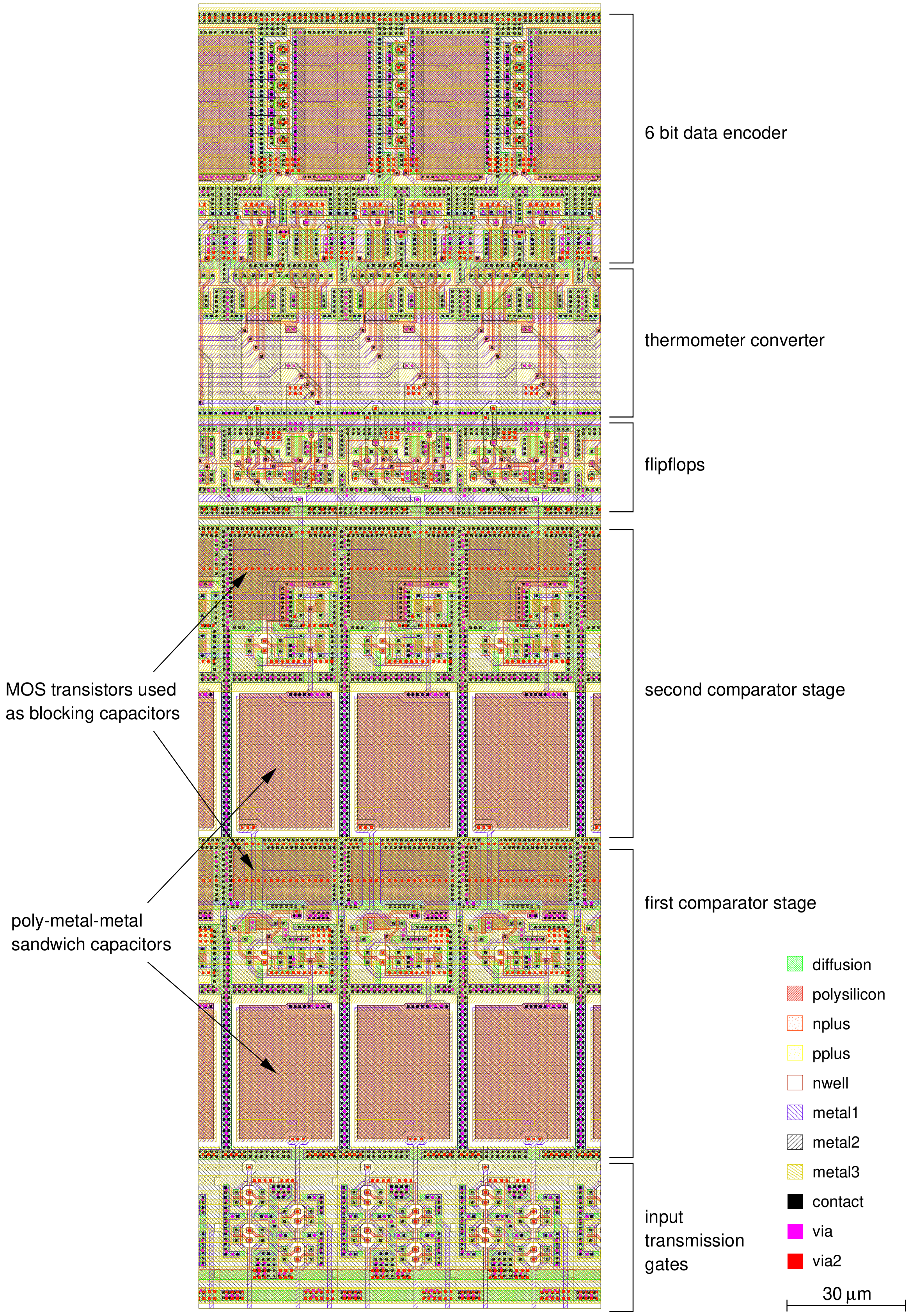


Figure A.10: Cutout of the ADC layout including three cells of the fine stage (rotated by 90°).

A.3 Measured performance

The properties of the Divichi ADC have been measured using the test setup described in section 5.1. The parallel as well as the high speed serial interface were used for the data readout. Since the serial interface in the applied test environment only reached a maximum rate of 114 Mbits/s corresponding to a sample rate of 7 MHz, the measurements at higher frequencies were realized with the parallel interface only. In order to transfer the full video rate of about 7.4 MHz via the serial interface, a rate of 120 Mbits/s would be required. This rate could probably be achieved by using a slightly changed test setup, but this has not yet been evaluated. All measurements were carried out with a voltage difference of 2 V between the upper and lower reference voltages V_{ref+} and V_{ref-}. Consequently, 1 LSB corresponds to about 2 mV.

A.3.1 Differential and integral non-linearity

Differential non-linearity

The differential non-linearity (DNL) refers to the deviation of the actual quantization step width from the ideal value of 1 LSB. It can be written as

$$\mathrm{DNL} = V_{in}(Q_{i+1}) - V_{in}(Q_i) - 1\ \mathrm{LSB} \tag{A.1}$$

where Q_i and Q_{i+1} are two adjacent quantization levels and $V_{in}(Q_i)$ is the analog input voltage corresponding to the quantization level Q_i. Hence, the differential non-linearity is zero, if every distance between successive transitions from one step to the next equals 1 LSB.

The measurement of the differential non-linearity can be carried out by using a voltage ramp covering the ADC's full scale range. The slope of the ramp has to be much slower than the sample rate in order to get many values at each quantization level. Finally, the acquired data is filled into a histogram plotted as a function of the ADC code. Ideally, all histogram bins should include the same number of occurrences which is given by

$$N_0 = \frac{N_{tot}}{2^n}. \tag{A.2}$$

N_{tot} is the total number of samples and n is the number of bits of the ADC. The differential non-linearity can be expressed by the ratio of the actual number of counts N_i in the considered histogram bin i to the ideal number of counts N_0 and yields

$$\mathrm{DNL}\ [\mathrm{LSB}] = \frac{N_i}{N_0} - 1 = \frac{N_i \cdot 2^n}{N_{tot}} - 1. \tag{A.3}$$

If the dynamic properties of the ADC should be taken into account, a faster analog input ramp must be used. In order to still get enough values per ADC code, the ramp cycle has to be applied several times (sawtooth or triangular waveform). To prevent any statistical correlation, the ratio of waveform frequency to sample frequency should be irrational.

Since, however, triangular or sawtooth waveforms in addition to the basic frequency contain higher frequency components (harmonics), they can not be used for measurements in the upper frequency region of the ADC. Here, the system bandwidth is too small for properly processing the upper harmonics leading to a distortion of the actual waveform. Therefore, the evaluation of the differential non-linearity at high frequencies is carried out with a pure sinewave. As it includes no further harmonics, its frequency can be increased up to the system bandwidth. Unfortunately, the acquired ADC codes are no longer equally distributed but show higher occurrence rates at the border than in the middle of the full scale range. This is due to the shape of the sinewave leading to a higher probability of detecting low and high values than middle values. The ideal number of counts per histogram bin as a function of the ADC code i in the case of a sinewave is given by [HEW]

$$N_0^i = \frac{N_{tot}}{\pi}\left[\arcsin\left(\frac{V(i-2^{n-1})}{A2^n}\right) - \arcsin\left(\frac{V(i-1-2^{n-1})}{A2^n}\right)\right]. \tag{A.4}$$

V is the full scale range of the ADC, A the peak amplitude of the input sinewave and n the number of ADC bits. Again, the differential non-linearity is determined by the ratio of the measured to the ideal number of counts:

$$\text{DNL [LSB]} = \frac{N_i}{N_0^i} - 1 \tag{A.5}$$

where N_0^i refers to equation A.4.

Both methods (triangle and sinewave) have been used for evaluating the Divichi ADC. Figure A.11 shows a histogram containing the number of occurrences as a function of the ADC code in the case of a triangular input waveform. The sample rate is 1 MHz and the analog signal frequency is 11 kHz. As expected, all histogram bins more or less possess the same height. In figure A.12, the results in the case of using a sinusoidal input signal can be seen. The data refers to a sample rate of 5 MHz and a signal frequency of 4990 kHz. According to the formula in equation A.4, the histogram bins vary as a function of the ADC code. Low and high ADC codes show high count numbers whereas middle codes have been hit less frequently.

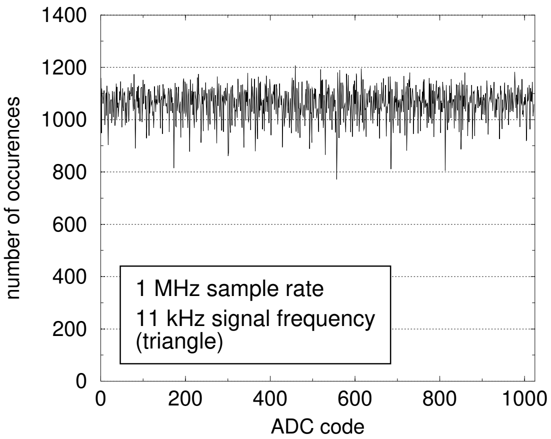


Figure A.11: Histogram obtained by sampling a triangular wave.

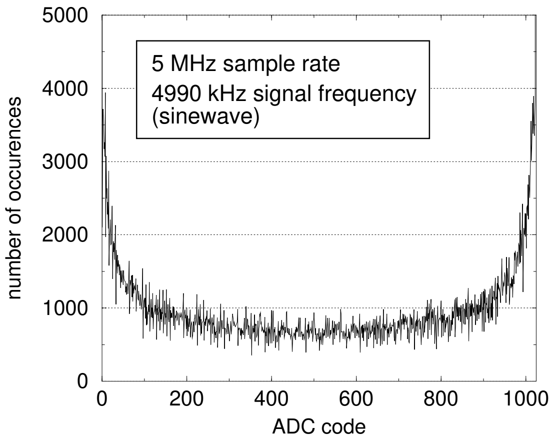


Figure A.12: Histogram obtained by sampling a sinewave.

The ADC performance has been examined at different sample rates and input signal frequencies. The differential non-linearity has been calculated from the acquired data using equation A.3 or equation A.5 depending on the applied waveform. The results corresponding to four different combinations of sample rate and signal frequency are shown in figure A.13. It can be seen, that the DNL is strongly dependent on the frequency. In the case of a low sample and signal frequency, the errors are below ± 0.25 LSB. This confirms, that the comparator offsets as well as the mismatch between individual resistors of the reference chain are below the critical level for a 10-bit ADC. Otherwise, the DNL would be higher because it is directly influenced by the mentioned effects.

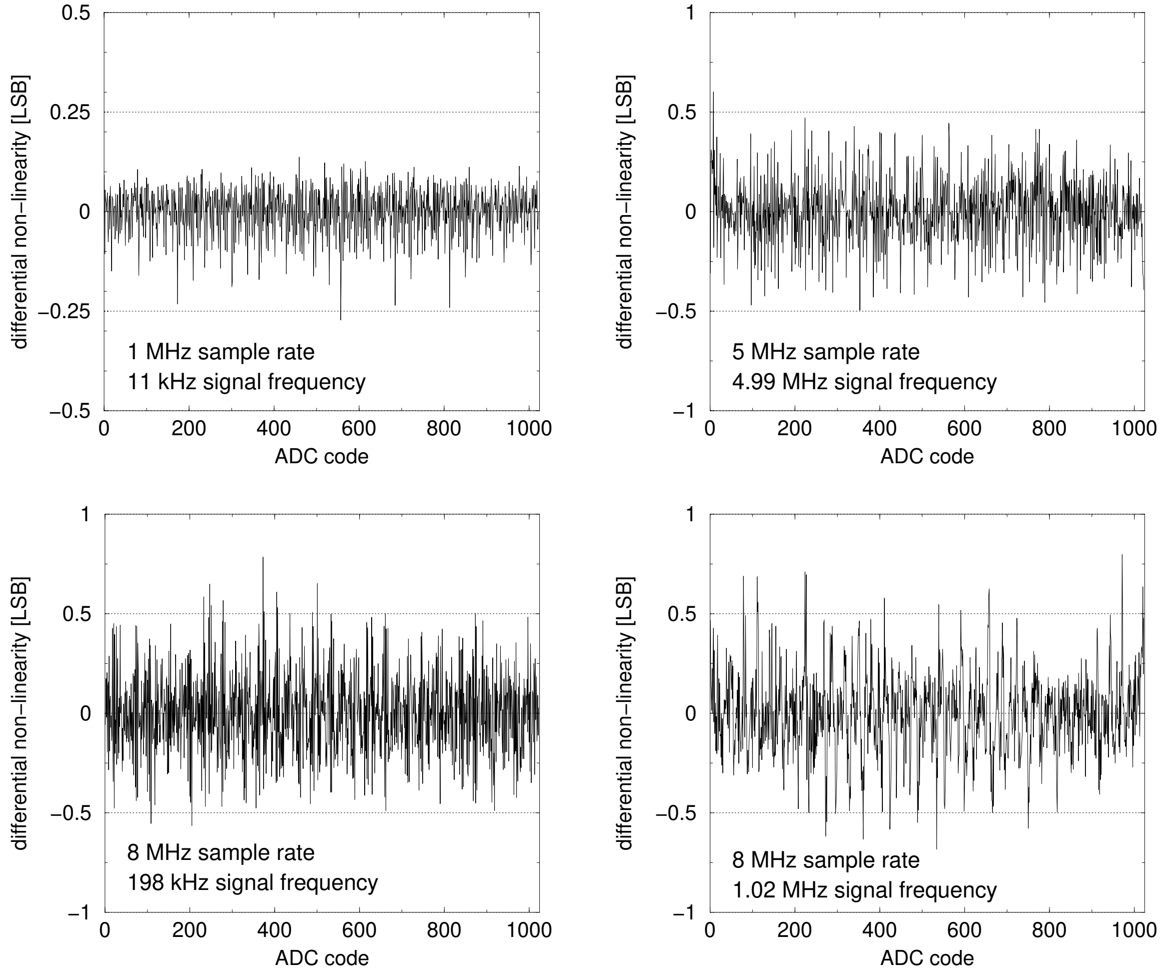


Figure A.13: Differential non-linearity measured at 4 different sample rates and analog signal frequencies.

When changing to higher frequencies, the differential non-linearity increases. The peak values amount to ± 0.5 LSB at 5 MSamples/s and to ± 0.75 LSB at 8 MSamples/s. This is due to the dynamic properties of the ADC like the frequency response of the comparators or the resistor chain including upper and lower reference buffer. The increased DNL causes a reduced effective ADC resolution since the error of the individual ADC values is higher than the width of one quantization step (1 LSB).

Integral non-linearity

The integral non-linearity (INL) is the deviation of the ADC transfer function from a best fit straight line. It does not include any gain or offset errors as they would be cancelled by the straight line fit. If the differential non-linearity is already measured, the integral non-linearity as a function of the ADC code can be easily calculated by summing the individual DNL errors up to the considered ADC code. Subsequently, a straight line is fitted to the resulting values. The final INL is obtained by correcting the calculated INL values according to the offset and the slope of the fitted curve.

The integral non-linearity curves corresponding to the four diagrams of the differential non-linearity in figure A.13 are shown in figure A.14. At low frequencies, the peak INL amounts to about ± 1 LSB. It is mainly caused but the mismatch of the resistor chain as dynamic effects only

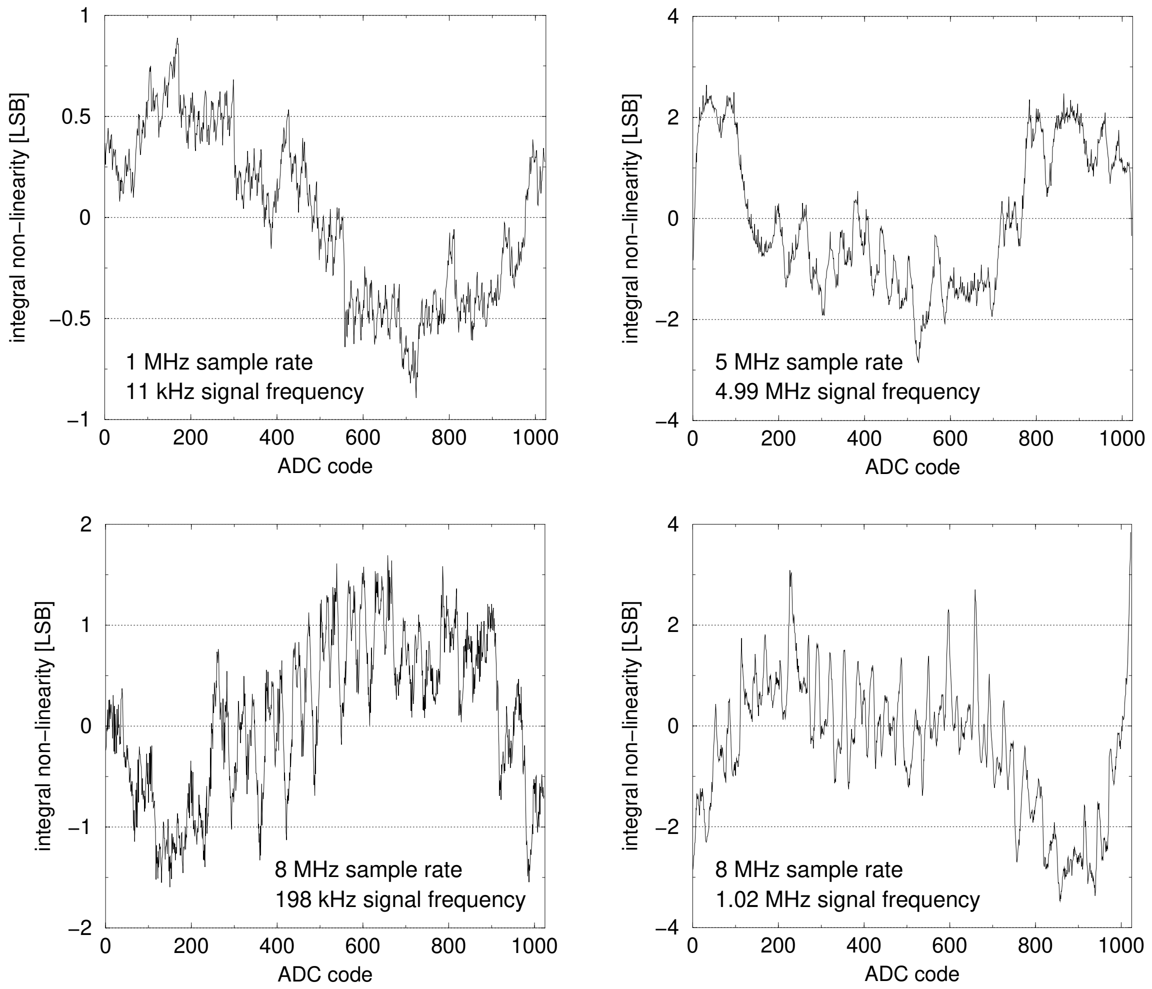


Figure A.14: Integral non-linearity measured at 4 different sample rates and analog signal frequencies.

become important at higher rates. In the case of an 8 MHz clock frequency, the INL reaches values of ± 3 LSB. Since the high frequency curves look different not only with respect to the absolute values but also with respect to the position of the peaks and the rising or falling regions, the INL seem to strongly depends on the operating conditions of the ADC.

The INL curves in figure A.14, especially in the lower right diagram, show a repetitive structure of positive and negative peaks. This is caused by the ADC architecture consisting of two sub-stages for the MSBs and the LSBs. Every peak corresponds to a change of the coarse stage output (MSBs) connecting the reference inputs of the fine stage to a different part of the resistor chain. Since the coarse stage provides a 5-bit resolution, 31 peaks should exist in each diagram. However, the INL curves represent a superposition of different effects so that the switching effect of the coarse stage sometimes disappears.

Because the ADC is used for processing analog pixel values, the absolute integral non-linearity is not a big problem. It merely causes a slight distortion of the pixel response on the scale of the full signal range. Image processing algorithms, however, do usually not depend on the exact linearity of the sensor response. In addition, any variation in the slope of the logarithmic compression would have a much higher impact on the linearity than the INL error of the ADC (see lower intensity range of the response curve in figure 5.7).

A.3.2 Signal-to-noise ratio and effective number of bits

Basically, the signal-to-noise ratio (SNR) of an ideal analog-to-digital converter is defined as the ratio of the full-scale signal RMS[5] value and the quantization RMS error [HOF96]. The RMS value of a full scale sinewave is given by the amplitude ($= 2^{n-1}$ LSB, n is the number of bits) divided by $\sqrt{2}$ due to

$$\text{RMS}_{signal} = \sqrt{\frac{(2^{n-1}\,\text{LSB})^2}{T}\int_0^T \sin^2(\omega t)\,dt} = \frac{2^{n-1}}{\sqrt{2}}\text{LSB} \tag{A.6}$$

where T is the length of one period. The quantization error q results from the difference between an ideal linear response and the characteristic ADC step function. This difference shows the shape of a sawtooth and is plotted in figure A.15.

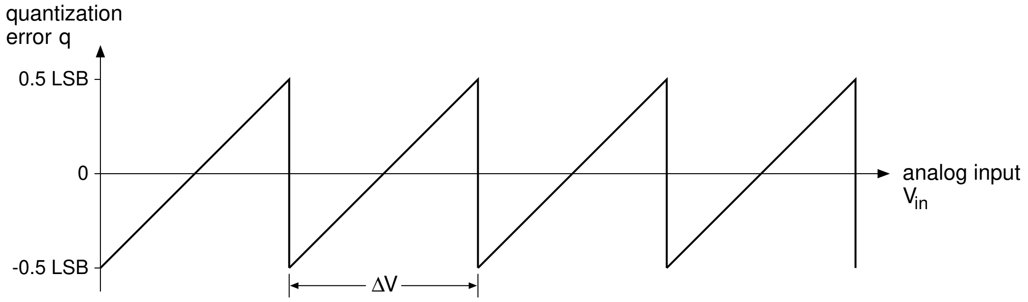


Figure A.15: Difference between an ideal linear function and the ADC response curve (step function).

The corresponding RMS value of the quantization noise yields

$$\begin{aligned}\text{RMS}_{qnoise} &= \sqrt{\frac{1}{\Delta V}\int_{\Delta V} q(V_{in})^2\,dV_{in}} \\ &= \sqrt{\frac{1}{\Delta V}\int_{\Delta V} (-\frac{1}{2}\text{LSB} + \frac{\text{LSB}}{\Delta V}V_{in})^2\,dV_{in}} = \frac{1}{2\sqrt{3}}\text{LSB}.\end{aligned} \tag{A.7}$$

Using the results from equation A.6 and equation A.7 gives the signal-to-noise ratio of an ideal ADC

$$\text{SNR} = \frac{\text{RMS}_{signal}}{\text{RMS}_{qnoise}} = \frac{\sqrt{3}}{\sqrt{2}}2^n = 1.225 \cdot 2^n \tag{A.8}$$

$$\text{or} \quad \text{SNR}_{\text{dB}} = 20 \cdot \log(1.225) + 20 \cdot n \cdot \log(2)\ \text{dB} = 1.76 + 6.02 \cdot n\ \text{dB}. \tag{A.9}$$

Unfortunately, real ADCs do not reach this theoretical value. They show an RMS noise that is somewhat increased compared to the ideal quantization noise. This is caused by additional contributions like power supply noise, reference voltage noise, RC-delays, and so on. The resulting reduced SNR is obtained by multiplying equation A.8 with the ratio of ideal quantization noise to true RMS noise. On the other hand, it can be expressed by using the ideal SNR relation and substituting n by an accordingly reduced effective number of bits n_{eff} (or ENOB):

$$\text{SNR}_{\text{true}} = \frac{\sqrt{3}}{\sqrt{2}}2^n \cdot \frac{\text{RMS}_{qnoise}}{\text{RMS}_{truenoise}} = \frac{\sqrt{3}}{\sqrt{2}}2^{n_{eff}}. \tag{A.10}$$

[5] root mean square

Solving this equation for the effective number of bits yields

$$\mathrm{ENOB} = n_{eff} = n - \log_2 \frac{\mathrm{RMS}_{truenoise}}{\mathrm{RMS}_{qnoise}}. \quad \text{(A.11)}$$

Consequently, in order to determine the signal-to-noise ratio and the effective number of bits, the actual RMS noise value has to be measured. In the case of the Divichi ADC, this was carried out by applying a sinusoidal voltage with a peak-peak amplitude covering the full scale range of the analog ADC input. Afterwards, a sinewave was fitted (least square fit) to the acquired digital data and the RMS value of the deviations between fitted and measured values was calculated. The obtained error represents a realistic value since it is measured under typical operating conditions taking into account all effects influencing the dynamic ADC performance.

The ideal error corresponding to the quantization noise is calculated by converting the fitted sinewave into digital values using a simulated, ideal ADC and subsequently determining the RMS value of the deviations between fitted curve and simulated values. This error always amounts to about 0.3 LSB due to equation A.7 but the exact value depends on the actual measured data. Figure A.16 shows a sampled sinewave and the curve fitted to the data points. The difference between measured and fitted values (= ADC error) is plotted in figure A.17. The corresponding values, referring to the simulated values of an ideal ADC, can be seen in figure A.18.

Applying the described method at different sample rates and input signal frequencies results in the effective number of bits and signal-to-noise ratios shown in figure A.19. The upper left diagram

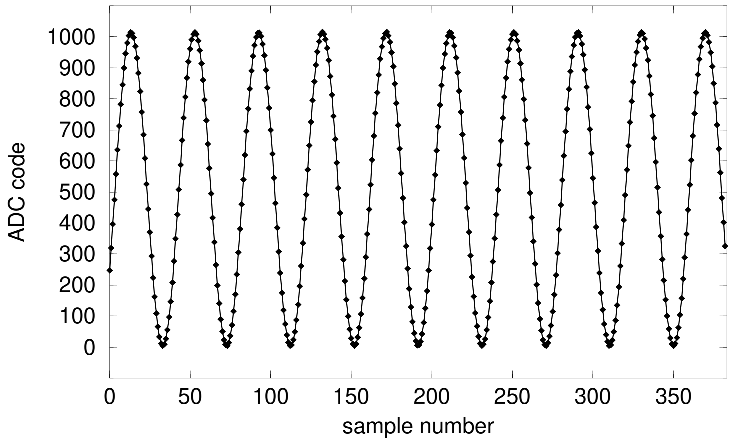


Figure A.16: Example of a 101 kHz sinewave sampled with 4 MHz. The solid line refers to the fitted curve.

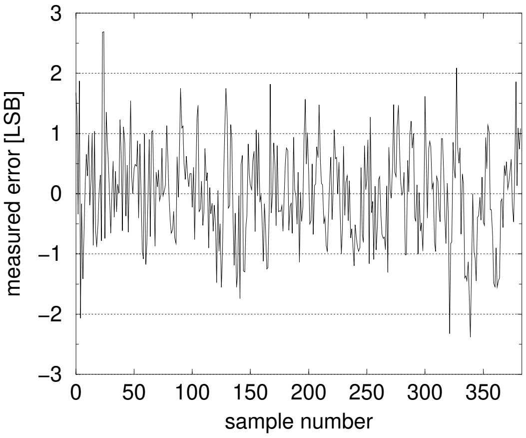


Figure A.17: Measured ADC error.

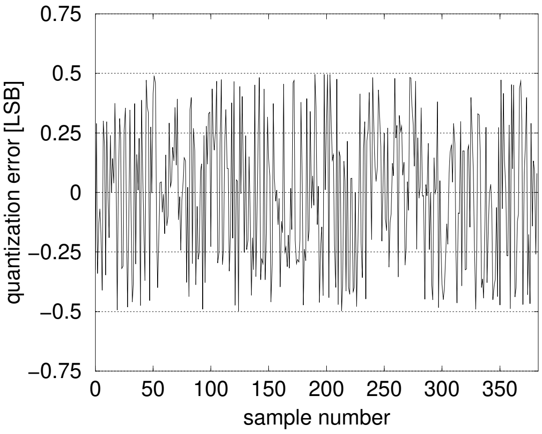
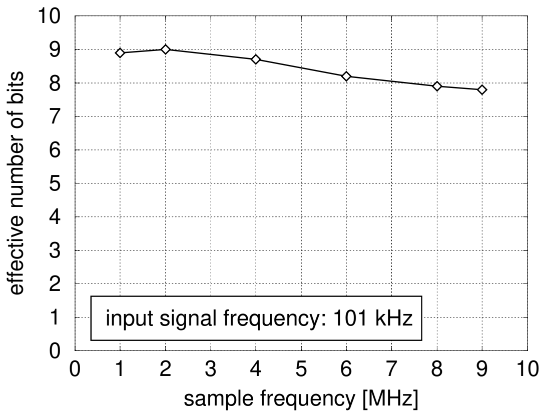


Figure A.18: Ideal ADC error (quantization noise).

contains the effective bits as a function of the sample rate at a fixed analog signal frequency of 101 kHz. The lower diagrams both correspond to the ENOBs as a function of the input frequency. The curves are measured at a sample rate of 4 MHz and 8 MHz, respectively. The tables summarize the signal-to-noise ratios gained from the measured ENOBs.

It can be seen that the ADC performance significantly decreases with increasing frequency (both sample and input frequency). This is a typical property of most ADC concepts. At sample rates below 3 MHz and signal frequencies below 200 kHz, an effective resolution of 9 bits is achieved (SNR = 56 dB). Changing to the sample rate of 8 MHz and the input frequency of 10 MHz, the effective bits drop to somewhat more than 6 (SNR = 39 dB). This deterioration of the ADC performance is caused by a number of dynamic effects like the limited bandwidth of the sample-and-hold stage, of the reference voltage buffers and of the comparators. The effective resolution at high frequencies could be improved by making the comparators faster which at the same time would increase the total power consumption. The realized ADC version consumes about 50 mW using a 5 V supply voltage.

In the case of the image sensor Divichi, the ADC runs at a maximum sample rate of 7.4 MHz (video timing) and an input frequency of 3.7 MHz (pixel rate divided by 2). Here, the ADC signal-to-noise ratio amounts to 42 dB (6.7 ENOBs). The signal-to-noise ratio of the sensor is 48 dB due to equation 5.5. This value, however, refers to the peak-peak input range, whereas the ADC SNR refers to the RMS value of a sinewave. For a sinewave, the ratio of the peak-peak value to the RMS value is $2 \cdot \sqrt{2}$ leading to an adapted sensor SNR of 39 dB. Consequently, the ADC performance is sufficient for the use in the Divichi camera.



SNR at a signal frequency of 101 kHz

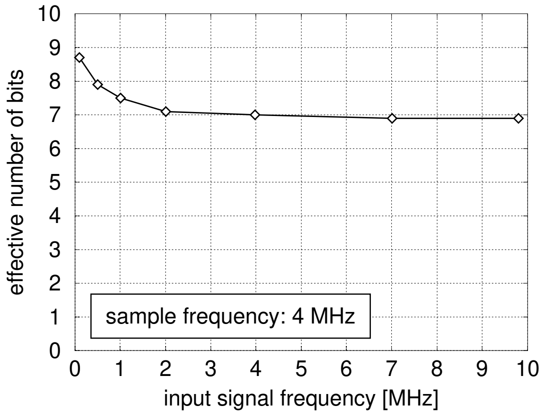
Msamples/s	1	2	4	6	8	9
SNR [dB]	55	56	54	51	49	49

SNR at a sample frequency of 4 MHz

signal [MHz]	0.1	0.5	1	2	4	10
SNR [dB]	54	49	47	45	44	43

SNR at a sample frequency of 8 MHz

signal [MHz]	0.1	0.5	1	2	6	10
SNR [dB]	49	45	44	42	41	39



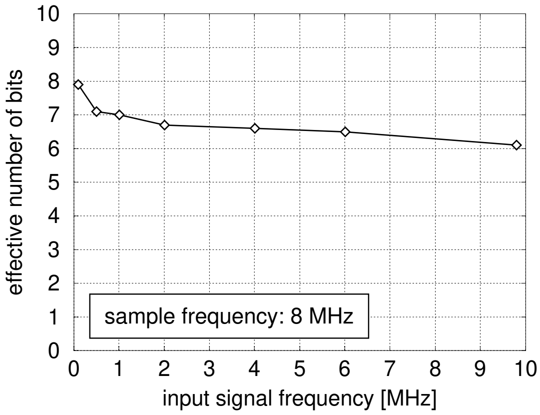


Figure A.19: Effective number of bits and signal-to-noise ratio measured at different sample and input signal frequencies.

Appendix B

Divichi Pictures of the Total Eclipse of the Sun

On August 11, 1999, a total eclipse of the sun occurred. The path of the moon's umbra began in the North Atlantic, crossed parts of Europe and Asia and finally ended in the Bay of Bengal. As the shadow also swept across the southern part of Germany including regions close to Heidelberg, it was possible to observe this phenomenon with the image sensor Divichi. In the following, some pictures, taken with the Divichi camera and a telephoto lens with a focal length of 500 mm, are presented.

Although the logarithmic sensor covers a large dynamic range, the intensity of the sun's projection corresponding to the used lens slightly exceeds the upper level of the sensitivity range. For this reason, one neutral density filter with an attenuation of 1:10 has been inserted between the sensor chip and the lens. The aperture number (focal length divided by the aperture diameter) was adjusted to 32, which is the smallest possible aperture number of the used lens. Only for the pictures of the totally covered sun, the aperture number was decreased to 8 (i.e. increased aperture) and the attenuation filter was omitted.

The pictures in the figures B.1 and B.2 show the complete cycle from the beginning to the end of the eclipse. Figure B.1 includes the pictures corresponding to the time between the first and the second contact. The first contact is the instant of the first external tangency between the moon and the sun (partial eclipse begins), the second contact means the instant of the first internal tangency between the moon and the sun (total eclipse begins). The corona, which is only visible if the sun is completely covered by the moon, can be seen in the first picture of figure B.2. The other pictures show the time between the third and the fourth contact. The third contact corresponds to the instant of the last internal tangency between the sun and the moon (total eclipse ends), whereas the fourth contact refers to the instant of the last external tangency (partial eclipse ends).

Unfortunately, the sky was very cloudy. This is the reason for the slight shadows which can be seen in some of the pictures. Additionally, the pictures show a few dark dots. They are not caused by sun-spots but by dust particles on the sensor itself. All images contain only a subpart ($270 \times 240 = 65$k pixels) of the complete Divichi frame in order to increase the relative size of the sun.

As the applied optical system (telephoto lens with tripod) possessed no automatic compensation for the movement of the sun (caused by the rotation of the earth), the sun moved across the sensor area with a velocity of 1.5 pixels per second. At regular intervals, the direction of the lens had to be adapted to the new position of the sun. Three pictures (full Divichi resolution of 110k pixels), taken at 0 s, 35 s and 70 s, are shown in figure B.3 demonstrating the relative motion of the sun.

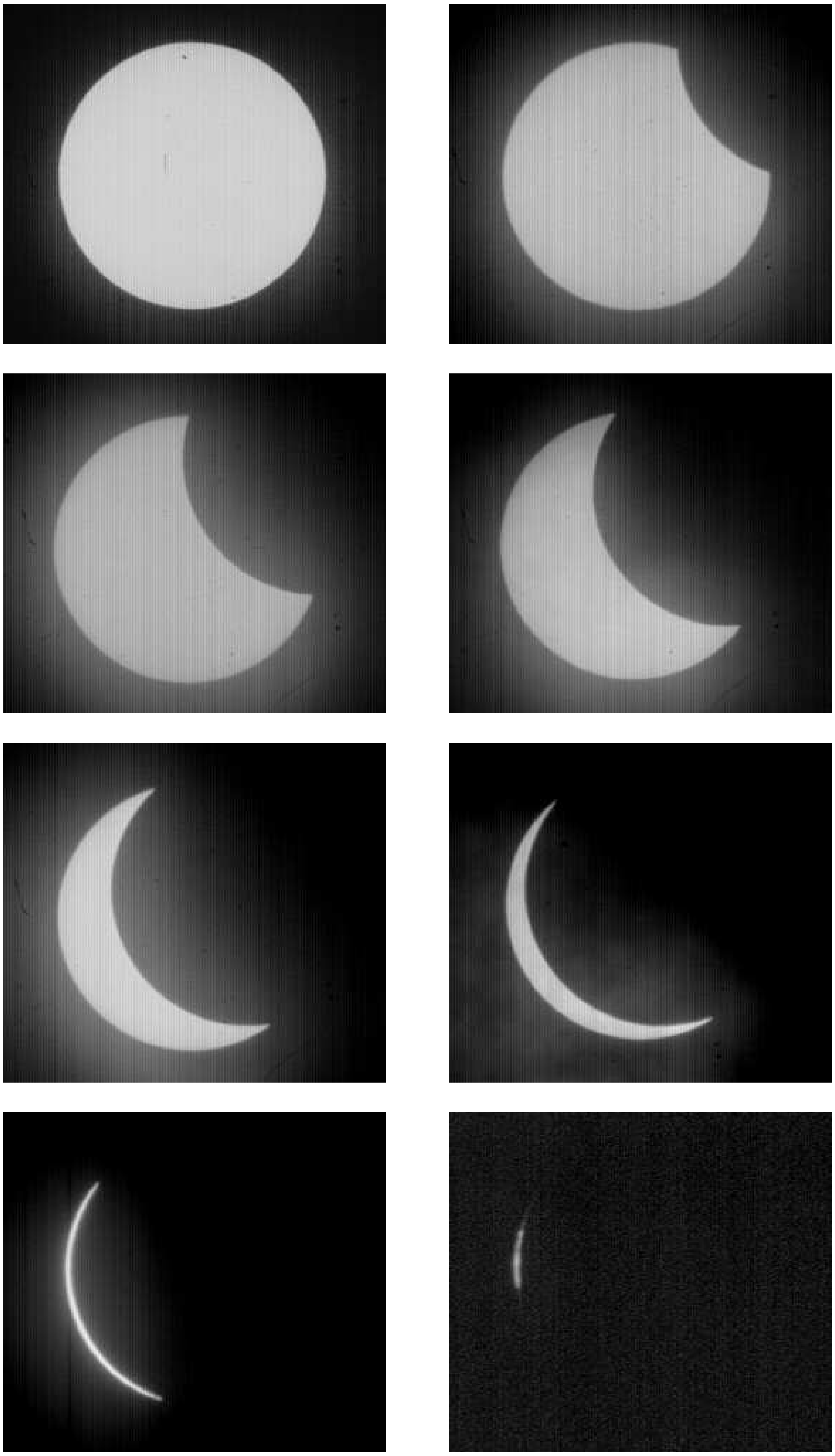


Figure B.1: Pictures taken between the first and the second contact.

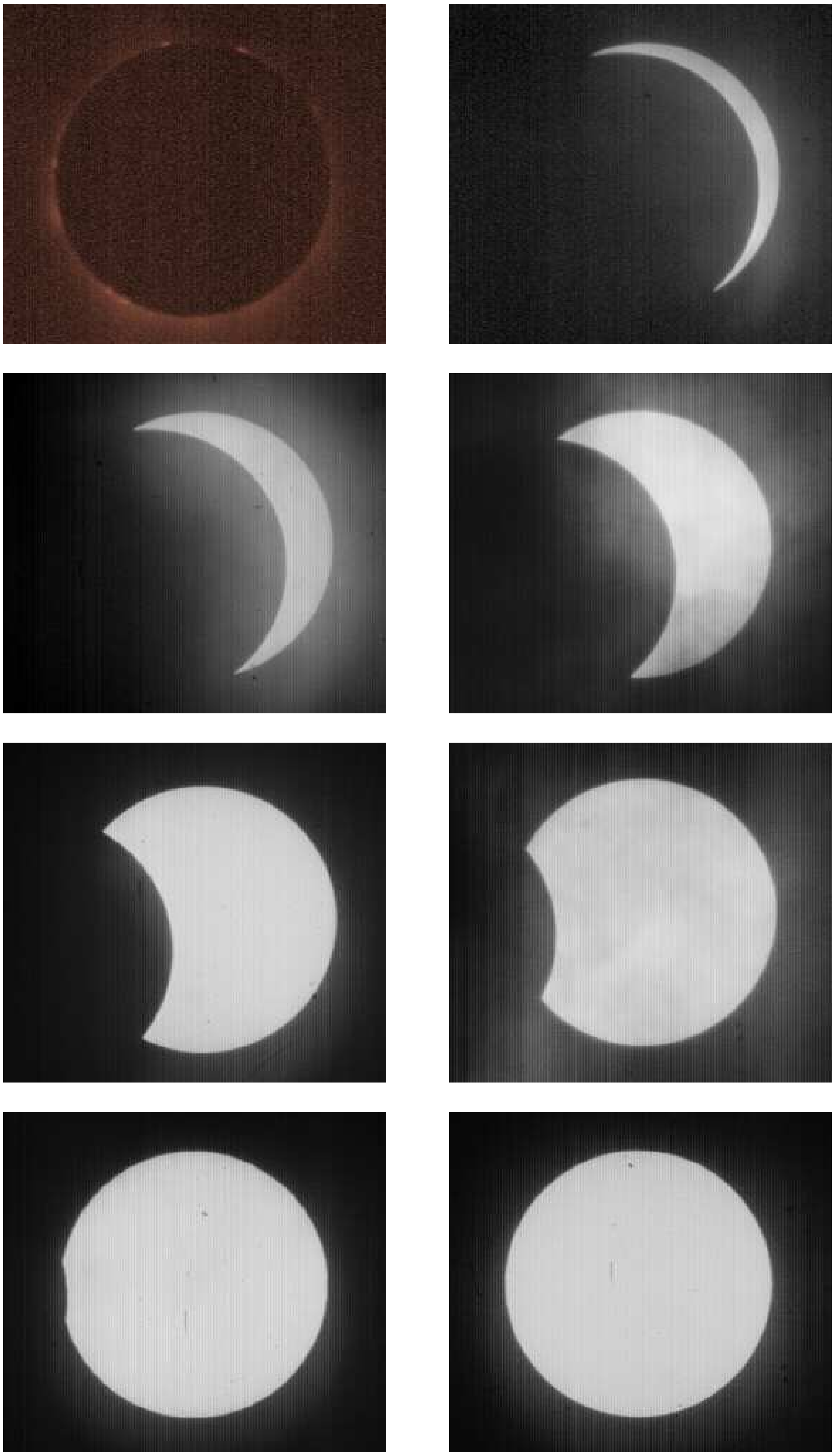


Figure B.2: Totality with the sun's corona and pictures taken between the third and the fourth contact.

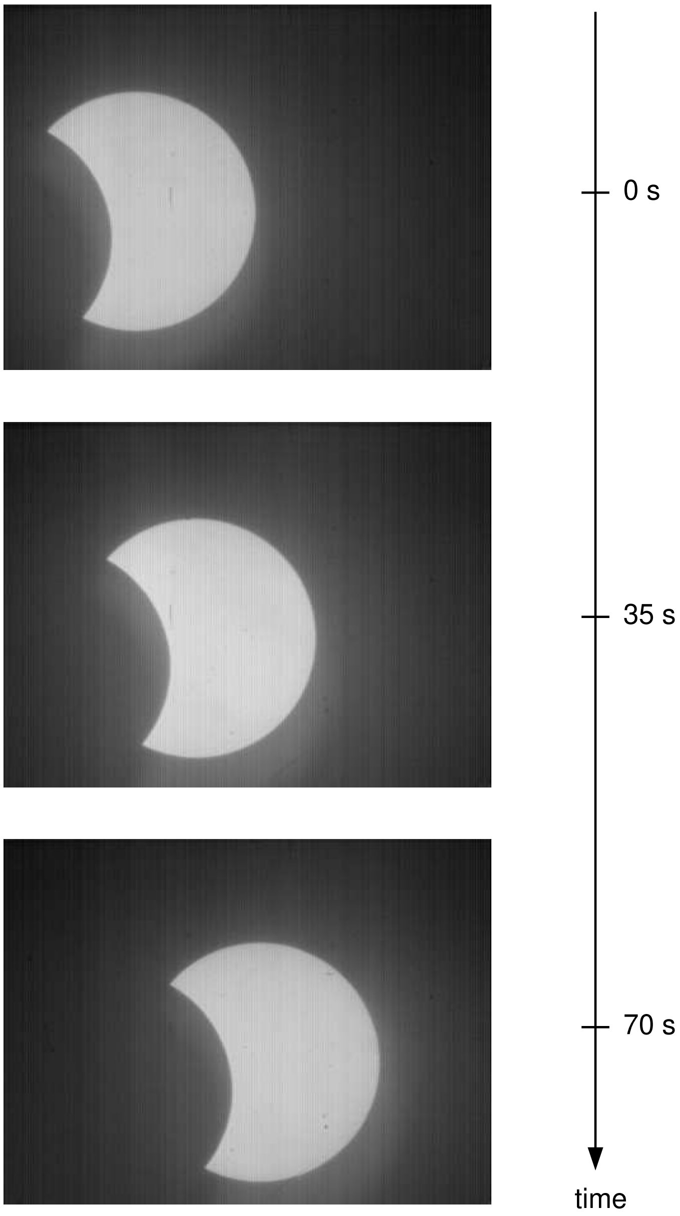


Figure B.3: Motion of the sun due to the rotation of the earth.

Appendix C

Averaging of Linear and Logarithmic Signals

Averaging two logarithmic photoreceptors can be carried out in two different ways. Either averaging the photocurrents themselves (linear averaging) or averaging the output voltages after the logarithmic compression (logarithmic averaging). A third option is obtained by simply connecting the receptor outputs amplified by the source followers. The result differs from the ideal voltage averaging because the source follower currents are summed instead of the voltages. All three cases are calculated in the following.

C.1 Current averaging

The linear averaging by connecting the photodiodes of two logarithmic pixels is shown in figure C.1. The logarithmic voltage of one pixel without averaging is given by equation 3.10

$$V_{log} = V_{off} - \tilde{n} V_t \ln \frac{I_{ph}}{I_{D0}} \tag{C.1}$$

where $\tilde{n} = (1 + \frac{1}{n})$ and $V_{off} = V_b/n^2$. The W/L dependence is included in the current I_{D0}.

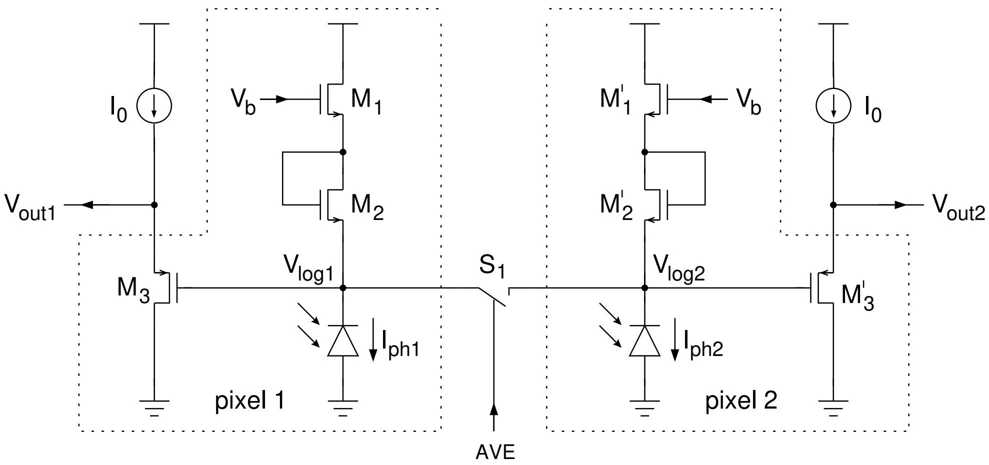


Figure C.1: Two photoreceptors averaged by connecting the photodiodes.

Closing the switch S_1 forces the voltages V_{log1} and V_{log2} to be equal. Therefore, if any device mismatch is neglected, the current flowing through the transistors M_1 and M_2 has to be the same as that through M_1' and M_2' due to equation C.1. This means that each pixel gets one half of the total current $I_{ph1} + I_{ph2}$ which results in

$$V_{log1} = V_{log2} = V_{off} - \tilde{n}V_t \ln \frac{I_{ph1} + I_{ph2}}{2I_{D0}}. \tag{C.2}$$

In principal the subsequent buffer transistor M_3 (source follower) has the voltage gain 1 and merely performs a level shift of about the threshold voltage V_T. Hence, the averaged pixel output can be written as

$$V_{out1} = V_{out2} = V_T + V_{off} - \tilde{n}V_t \ln \frac{I_{ph1} + I_{ph2}}{2I_{D0}}. \tag{C.3}$$

C.2 Voltage averaging

The implementation of an exact voltage addition which is necessary for the voltage averaging requires an additional operational amplifier [HIN95-2]. The corresponding circuit diagram is shown in figure C.2. The averaged output voltage V_{out} is given by the product RI_R where I_R is the current through the resistor R. This current is equal to the sum of the currents $V_{out1}/2R$ and $V_{out2}/2R$ caused by the pixel output voltages. Substituting equation C.1 and adding the voltage shift due to the source follower results in

$$\begin{aligned} V_{out} &= RI_R = \frac{1}{2}V_{out1} + \frac{1}{2}V_{out2} \\ &= \frac{1}{2}\left(V_T + V_{off} - \tilde{n}V_t \ln \frac{I_{ph1}}{I_{D0}}\right) + \frac{1}{2}\left(V_T + V_{off} - \tilde{n}V_t \ln \frac{I_{ph2}}{I_{D0}}\right). \end{aligned} \tag{C.4}$$

Combining the two logarithmic terms yields

$$V_{out} = V_T + V_{off} - \tilde{n}V_t \ln \frac{\sqrt{I_{ph1}I_{ph2}}}{I_{D0}}. \tag{C.5}$$

Comparing this result to the linear averaging in the previous section shows that current averaging

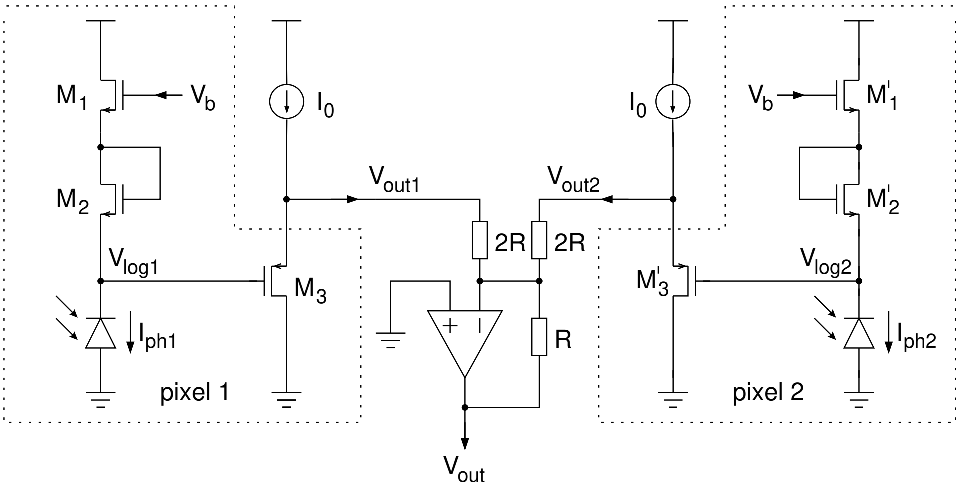


Figure C.2: Two photoreceptors with an ideal averaging of the output voltages.

corresponds to the logarithm of the arithmetic mean (equation C.3) and voltage averaging to the logarithm of the geometrical mean (equation C.5).

C.3 Simplified voltage averaging

To avoid the additional amplifier for summing the output voltages, the output lines can be directly connected to each other. Because this corresponds to an averaging of the source follower currents, a deviation compared to the ideal voltage averaging is obtained. Figure C.3 shows the corresponding circuit diagram.

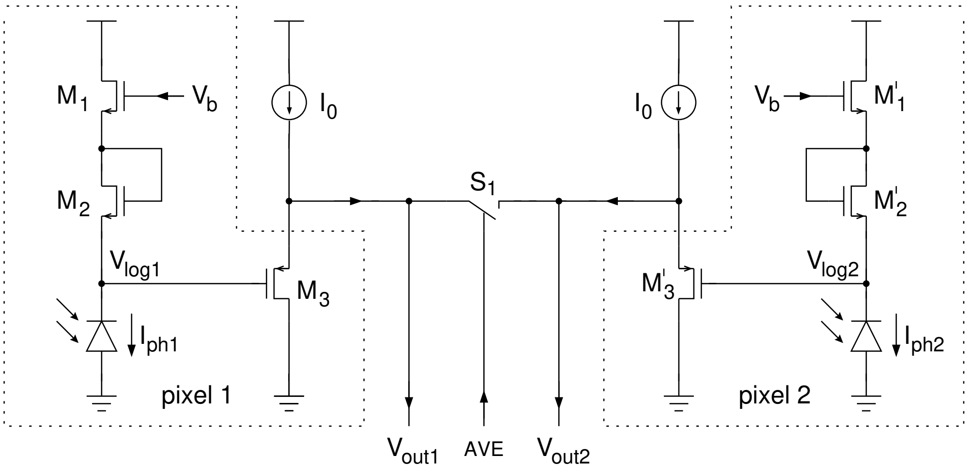


Figure C.3: Two photoreceptors averaged by connecting the output lines.

Neglecting the channel length modulation parameter λ the drain currents of the transistors M_3 and M'_3 can be written as (cf. equation 2.1)

$$I_{D1} = \frac{\beta}{2}(V_{GS}+\tilde{V}_T)^2 = \frac{\beta}{2}(V_{log1}-V_{out1}+\tilde{V}_T)^2 \tag{C.6}$$

$$I_{D2} = \frac{\beta}{2}(V_{GS}+\tilde{V}_T)^2 = \frac{\beta}{2}(V_{log2}-V_{out2}+\tilde{V}_T)^2 \tag{C.7}$$

The threshold voltage V_T has been replaced by $\tilde{V}_T$ to obtain $I_D = I_0$ if $V_{GS} = V_T$. I_0 is the current provided by the current source of the source follower. The relationship between V_T and $\tilde{V}_T$ is given by

$$\tilde{V}_T = V_T - \sqrt{\frac{2I_0}{\beta}}. \tag{C.8}$$

Closing the switch S_1 connects the pixel outputs and results in the following conditions:

$$V_{out} = V_{out1} = V_{out2} \tag{C.9}$$

$$2I_0 = I_{D1} + I_{D2} \tag{C.10}$$

Substituting equation C.6 and C.7 into the conditions C.9 and C.10 and solving for the averaged output signal V_{out} yields

$$V_{out} = \tilde{V}_T + \frac{V_{log1}+V_{log2}}{2} \underset{(-)}{+} \sqrt{\frac{2I_0}{\beta} - \left(\frac{V_{log1}-V_{log2}}{2}\right)^2}. \tag{C.11}$$

The solution with the negative square root has no physical meaning and can be neglected. The voltages V_{log1} and V_{log2} can be expressed as a function of the photocurrents I_{ph1} and I_{ph2} using equation C.1

$$V_{log1} = V_{off} - \tilde{n}V_t \ln \frac{I_{ph1}}{I_{D0}} \tag{C.12}$$

$$V_{log2} = V_{off} - \tilde{n}V_t \ln \frac{I_{ph2}}{I_{D0}}. \tag{C.13}$$

Substituting these relations into equation C.11, using equation C.8 and combining the logarithmic terms gives the final expression for the averaged output voltage

$$V_{out} = V_T + V_{off} - \tilde{n}V_t \ln \frac{\sqrt{I_{ph1}I_{ph2}}}{I_{D0}} - \sqrt{\frac{2I_0}{\beta}} + \sqrt{\frac{2I_0}{\beta} - \frac{\tilde{n}^2 V_t^2}{4} \ln^2 \frac{I_{ph1}}{I_{ph2}}}. \tag{C.14}$$

The first half of this result is identical to the exact voltage averaging of the output signals (equation C.5). The second half, however, represents a distortion which is small for small differences between I_{ph1} and I_{ph2} but becomes dominant if the photocurrents differ by several decades from each other. The three different averaging results are plotted in figure 3.9. It is included in section 3.2.2 where the finally implemented averaging method is described.

Appendix D

Correlation between Physical and Photometric Quantities

Usually, radiation in any frequency range is described by its radiant power or its radiant intensity representing general physical quantities. Systems working in the range of the visible light, however, often have to be compared to the properties of the human eye. This especially applies in the case of cameras which have to operate under the same conditions as the optical sense. Since the eye possesses a varying sensitivity depending on the wavelength, the same intensity is differently sensed at different wavelengths. Therefore, a complementary set of quantities exists in addition to the physical quantities, namely the so-called photometric quantities. They take into account the spectral sensitivity $V(\lambda)$ of the eye by accordingly weighting the individual frequency components of the considered light spectrum. The following description refers to the definitions in [TEX75].

The corresponding quantity of the *radiant power* P_e (e: energy) with the unit W (Watt) is given by the *luminous power* or *luminous flux* P_v (v: visible) with the unit lm (lumen). The luminous power P_v is defined as the product of the *luminous intensity* I_v and the solid angle Ω:

$$P_v = I_v \cdot \Omega. \tag{D.1}$$

This equation also defines the unit lm corresponding to

$$[P_v] = \text{lm} = \text{cd} \cdot \text{sr} \tag{D.2}$$

where cd (Candela) is the unit of the luminous intensity and sr (steradian) is the unit of the solid angle. For measuring reasons, the luminous intensity represents the basic photometric quantity. The corresponding unit cd has been defined by the general conference on weights and measures CGPM[1] 1979 as follows [BER93-2]:

One Candela (cd) is the luminous intensity in a certain direction of a radiation source emitting monochromatic radiation with a frequency of 540 THz ($\lambda = 555\,\text{nm}$) and with a radiant intensity of 1/683 W$\cdot$sr^{-1} in this direction.

In order to obtain a correlation between the physical (or better radiometric) quantity radiant power and the photometric quantity luminous power, the spectral sensitivity of the eye has to be regarded. The spectral sensitivity $V(\lambda)$ (*photopic luminosity function*) corresponding to the light adapted eye is shown in figure D.1 on a linear scale and in figure D.2 on a logarithmic scale. The curve represents

[1] CGPM: Conféférence générale sur les poids et measures

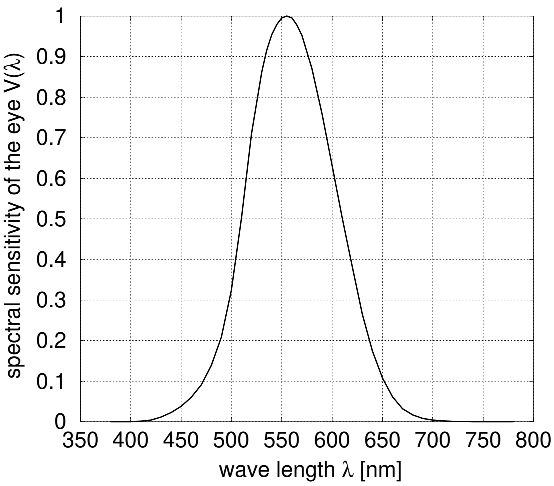


Figure D.1: Relative spectral sensitivity of the eye on a linear scale (*photopic luminosity function*) [BER93-2].

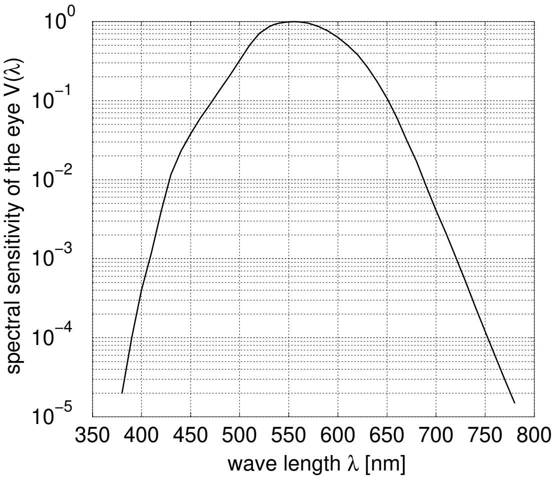


Figure D.2: Relative spectral sensitivity of the eye on a logarithmic scale [BER93-2].

the relative sensitivity with regard to the maximum sensitivity at 555 nm, which has been scaled to one. All values refer to the International Commission on Illumination (CIE) which has carried out extensive series of measurements for determining a representative mean value.

Using the eye's sensitivity curve $V(\lambda)$, the following relation applies between the luminous power P_v and the spectral radiant power $P_{e,\lambda}$:

$$P_v = K_m \int_0^\infty P_{e,\lambda}(\lambda) V(\lambda) d\lambda. \tag{D.3}$$

The proportionality constant K_m amounts to 683 cd $\cdot$ sr $\cdot$ W^{-1} due to the definition of the Candela mentioned above. The equation D.3 means, that the photometric quantity P_v is obtained by weighting each frequency component of the physical quantity P_e according to the corresponding value of the photopic luminosity function $V(\lambda)$ in figure D.1. For a monochromatic radiation of the wavelength λ, the relation simply yields

$$P_{v,\lambda} = K_m \cdot P_{e,\lambda} \cdot V(\lambda). \tag{D.4}$$

Except for the radiant power, another pair of quantities plays an important role in connection with light sensors or cameras: the *irradiance* E_e and the corresponding photometric quantity *illuminance* E_v. The irradiance refers to the radiant power per unit area and is defined by

$$E_e = \frac{P_e}{A} \quad \text{with} \quad [E_e] = \frac{\text{W}}{\text{m}^2} \tag{D.5}$$

where A is the considered area. Instead of the word irradiance, the term *intensity* with the symbol J is often used as a synonym. The illuminance E_v is defined in the same way using the photometric power P_v:

$$E_v = \frac{P_v}{A} \quad \text{with} \quad [E_v] = \frac{\text{lm}}{\text{m}^2} = \text{lx}. \tag{D.6}$$

The unit of the irradiance is lux (lx). Substituting equation D.3 into equation D.6 and using equation D.5 leads to the relation between the irradiance (or intensity) and the illuminance:

$$E_v = K_m \int_0^{\infty} E_{e,\lambda}(\lambda) V(\lambda) d\lambda. \tag{D.7}$$

Again, this equation can be simplified if only monochromatic light is considered. Similar to equation D.4, the illuminance corresponding to the frequency λ is given by

$$E_{v,\lambda} = K_m \cdot E_{e,\lambda} \cdot V(\lambda). \tag{D.8}$$

The described radiometric and photometric quantities are summarized in table D.1. Table D.2 shows some examples of the corresponding magnitudes for the light intensity (irradiance) given in W/m^2 and the illuminance given in lx.

type of quantity	quantity	symbol	formula	unit
radiometric photometric	radiant intensity luminous intensity	I_e I_v	- -	$\mathrm{W} \cdot \mathrm{sr}^{-1}$ $\mathrm{cd} = \mathrm{lm} \cdot \mathrm{sr}^{-1}$
radiometric photometric	radiant power luminous power	P_e P_v	$I_e \cdot \Omega$ $I_v \cdot \Omega$	W $\mathrm{lm} = \mathrm{cd} \cdot \mathrm{sr}$
radiometric photometric	irradiance (or intensity) illuminance	E_e (or J) E_v	$P_e \cdot A^{-1}$ $P_v \cdot A^{-1}$	$\mathrm{W} \cdot \mathrm{m}^{-2}$ $\mathrm{lx} = \mathrm{lm} \cdot \mathrm{m}^{-2}$

Table D.1: Summary of physical (radiometric) and photometric quantities.

wavelength [nm]	irradiance [$\mathrm{W} \cdot \mathrm{m}^{-2}$]	illuminance [lx]
400	1.00	0.273
480	1.00	94.9
555	1.00	683
620	1.00	260
675	1.00	16.4
740	1.00	0.171
white spectrum (380-780 nm)	1.00	178
400	366	100
480	105	100
555	0.146	100
620	0.385	100
675	6.10	100
740	585	100
white spectrum (380-780 nm)	0.562	100

Table D.2: Some examples of corresponding illuminance and irradiance magnitudes.

Appendix E

Divichi User Manual

The camera chip Divichi possesses a number of different operation modes and adjustable parameters in order to adapt the performance and the properties to the various requirements. The first part of this manual contains the individual commands which are used for programming the sensor registers. In the next section, the operation of the different interfaces, which are integrated for writing the commands and for reading out the pixel data, is explained. Subsequently, the Divichi pad layout and the corresponding I/O signals are described. In this context, the bond diagram of the sensor board and the pin configuration of the camera board connectors are shown. They refer to the complete camera system with the image sensor, the printed circuit boards, the lens and the housing. Finally, the last section summarizes the technical data and the main performance results.

E.1 Command definitions

Divichi understands 46 different commands. In contrast to many other digital systems with an internal register set, the command structure is not divided into a fixed address and a fixed data part, but consists of a varying number of address (or instruction specifying) bits and a varying number of data bits. This leads to a reduced total number of bits which have to be transmitted. In every case (except for one), the length of the complete command word is 14 bits. The MSBs (upper 5 to 8 bits) define the instruction or the register address and the LSBs (lower 2 to 9 bits) define the corresponding data.

All Divichi commands are listed in the tables E.1 - E.4. The first column contains the command name. If the command refers to one of the analog control or bias voltages, the number of the corresponding DAC is written below the command name. The second column shows the bit pattern that has to be transmitted to Divichi for executing the desired instruction. The pattern consists of the symbols 0,1,x and d. The numbers 0 and 1 define the fixed command bits. The letter x means, that the bit is undefined and can be set to any value. The letter d refers to the data bits defining the value which is written to the corresponding Divichi register. In the third column, the initial register values, which are valid after a system reset, can be seen. In some cases, a second number is written in parentheses below the first value. These values have been used for the sensor evaluation in the video mode. If only one number is given, the values both are identical. Finally, the last column contains a short command description.

Two comments should be made: At first, some explanations contain the symbols D0, D1,..., which refer to the individual bits of the command data (e.g. control registers A and B at the bottom of table E.2). The corresponding bit description only applies, if the bit is set to 1. Secondly, the last command **READPIXEL** in table E.4 consists of only three bits. By this means, a faster readout in the pixel readout mode (serial readout) can be achieved, since the command is required for every pixel.

Command	Bit Pattern	Initial Value	Description
NOP	00 0xxx xxxx xxxx	x	no operation
SETXPOS	11 010d dddd dddd	1	set the upper left x-position of the read-out frame
SETYPOS	11 011d dddd dddd	1	set the upper left y-position of the read-out frame
SETXRANGE	11 100d dddd dddd	384	set the number of pixels in x-direction (frame width)
SETYRANGE	11 101d dddd dddd	288	set the number of pixels in y-direction (frame height)
SETDISTANCE	11 110d dddd dddd	64 *(0)*	set the distance between the readout and the calibration row (video and forced calibration mode only)
SETLOWERADCREF (DAC 0)	10 0000 dddd dddd	31	set the lower reference voltage of the ADC (Vref- $= \frac{\text{data}}{256} * 5\,\text{V}$)
SETBIASVIDEO (DAC 1)	10 0001 dddd dddd	182 *(203)*	set the bias voltage for the video amplifier (Vbiasvideo $= \frac{\text{data}}{256} * 5\,\text{V}$)
SETREFCURR (DAC 2)	10 0010 dddd dddd	210 *(215)*	set the voltage controlling the calibration reference current (Vrefcurr $= \frac{\text{data}}{256} * 5\,\text{V}$)
SETADCTIME (DAC 3)	10 0011 dddd dddd	96 *(93)*	set the voltage controlling the length of the ADC offset corr. cycle for the first comparator stage (Vadc $= \frac{\text{data}}{256} * 5\,\text{V}$)
SETMULTIREF (DAC 4)	10 0100 dddd dddd	201 *(205)*	set the reference voltage for the readout multiplexer (Vrefm $= \frac{\text{data}}{256} * 5\,\text{V}$)
SETBIASREAD (DAC 5)	10 0101 dddd dddd	210 *(203)*	set the bias voltage for the pixel readout source follower (Vbiasread $= \frac{\text{data}}{256} * 5\,\text{V}$)
SETUPPERADCREF (DAC 6)	10 0110 dddd dddd	129	set the upper reference voltage of the ADC (Vref+ $= \frac{\text{data}}{256} * 5\,\text{V}$)
SETFALLTIME (DAC 7)	10 0111 dddd dddd	53 *(81)*	set the voltage controlling the fall time of the row sel. signals (Vfall $= \frac{\text{data}}{256} * 5\,\text{V}$)
SETBIASCAL (DAC 8)	10 1000 dddd dddd	202 *(205)*	set the bias voltage for the pixel calibr. source follower (Vbiascal $= \frac{\text{data}}{256} * 5\,\text{V}$)
SETBIASSOURCE (DAC 9)	10 1001 dddd dddd	66 *(67)*	set the bias voltage for the multiplexer source followers (Vbs $= \frac{\text{data}}{256} * 5\,\text{V}$)
SETVIDEOREF (DAC 10)	10 1010 dddd dddd	67 *(56)*	set the offset voltage of the video output signal (Vvideoref $= \frac{\text{data}}{256} * 5\,\text{V}$)

Table E.1: Description of the Divichi control commands (first part).

Command	Bit Pattern	Initial Value	Description
SETRISETIME (DAC 11)	10 1011 dddd dddd	179 *(191)*	set the voltage controlling the rise time of the row sel. signals (Vrise $= \frac{\text{data}}{256} * 5\,\text{V}$)
SETAZREF (DAC 12)	10 1100 dddd dddd	155 *(149)*	set the reference voltage for the autozeroing cycle of the calibration amplifiers (Vcalop $= \frac{\text{data}}{256} * 5\,\text{V}$)
SETBIASREADOP1 (DAC 13)	10 1101 dddd dddd	64 *(70)*	set the bias voltage for the 1st stage of the readout amplifier (Vb1 $= \frac{\text{data}}{256} * 5\,\text{V}$)
SETPRECHARGE (DAC 14)	10 1110 dddd dddd	255	set the precharge voltage for the reference current lines (Vcurrpre $= \frac{\text{data}}{256} * 5\,\text{V}$)
SETBIASVSF (DAC 15)	10 1111 dddd dddd	255	set the bias voltage for the output source follower (AnalogOut2 line) (Vbiasvsf $= \frac{\text{data}}{256} * 5\,\text{V}$)
SETCALIBREF (DAC 16)	11 0000 dddd dddd	73 *(85)*	set the reference voltage for the self-calibration (Vpos = Vref $= \frac{\text{data}}{256} * 5\,\text{V}$)
SETBIASREADOP2 (DAC 17)	11 0001 dddd dddd	54 *(80)*	set the bias voltage for the 2nd stage of the readout amplifier (Vb2 $= \frac{\text{data}}{256} * 5\,\text{V}$)
SETBIASCALOP (DAC 18)	11 0010 dddd dddd	198 *(206)*	set the bias voltage for the calibration amplifiers (Vbiascalop $= \frac{\text{data}}{256} * 5\,\text{V}$)
SETCONTROLA	01 0100 dddd dddd	binary 11110011 *(D5=0)*	D0: enable self-calibration D1: enable autozeroing of calibr. amp. D2: autozeroing only once per frame D3: enable forced calibration mode D4: enable precharge of the ref. curr. line D5: enable auto exposure control D6: use the array diodes for the auto exposure control D7: use the border diodes for the auto exposure control
SETCONTROLB	01 0101 dddd dddd	binary x1100011 *(D1=0, D5=0)*	D0: enable video mode D1: enable autozoom D2: set the max. size for the frame; SETXPOS, SETYPOS, SETXRANGE and SETYRANGE will be ignored D3: move upper left frame corner into visible area (video mode) D4: power-down of the video amplifier D5: enable interlaced mode D6: mirror the readout frame D7: unused

Table E.2: Description of the Divichi control commands (second part).

Command	**Bit Pattern**	**Initial Value**	**Description**
SETCONTROLC	01 0110 dddd dddd	binary 00001000 *(D1=1, D3=0)*	D0: stop the DAC update D1: update the DACs only one time per frame D2: disable DACs D3: enable ADC D4: use external ADC clock D5: enable additional hold capacitor D6: set digital output line D7: set EEPROM control lines to the high-ohmic state
SETCALTIME	01 0000 dddd dddd	32	set the calibr. time in clock cycles * 128
SETAUTOTIME	01 0001 dddd dddd	6 *(5)*	set the autozeroing time for the calibration amplifiers in clock cycles * 13
SETLINETIME	01 0010 0ddd dddd	48	set the time between the line selection and the readout of the first pixel in clock cycles * 4 (non-video mode)
SETREADTIME	01 0010 1ddd dddd	4	waiting time per pixel in clock cycles (non-video mode)
SETGAIN	01 0011 0ddd dddd	48 *(100)*	set the gain of the readout amplifier (contrast)
SETDACREF	11 0011 xxdd dddd	32 *(13)*	set the lowermost level of the DAC voltage range (DAC 0 - DAC 18)
SETAVERAGE[1]	01 1000 0xdd dddd	binary 001 001	set the number of pixels averaged in horizontal (D5-D3) and vertical (D2-D0) direction
SETZOOM	01 1000 1xxd dddd	0	set the zoom factor (video mode)
SETCHARGETIME	01 1001 0xxx dddd	2 *(0)*	set the precharge time for the column readout lines in clock cycles
SETCURRGAIN	01 1001 1xxx dddd	8	set the ratio of the reference current to the averaged current of the border or array photodiodes
SETCOLLWAIT	01 1010 0xxx dddd	8	set the number of rows that have to be calibrated before the readout will continue after a calibration-readout collision

Table E.3: Description of the Divichi control commands (third part).

[1] Correlation between the data bits of the **SETAVERAGE** command and the number of averaged pixels: The data values 1, 2, 3, 4, 6, and 7 mean an averaging of 1, 2, 3, 4, 5 or 8 pixels. The data values 0 and 5 have no meaning, the register contents will not be changed.

Command	Bit Pattern	Initial Value	Description
READSTOP	11 1110 00xx xxdd	00b	D0: stop readout immediately D1: stop readout at the end of frame
EEPROMWRITE	11 1110 10xx xxxx	-	write all parameters to the external EEPROM
EEPROMREAD	11 1110 11xx xxxx	-	read all parameters from the external EEPROM
READRESET	11 1111 00xx xxxx	-	reset the readout state machine, start with a new frame
RESET	11 1111 11xx xxxx	-	system reset, all registers are set to the initial values and subsequently loaded with the EEPROM parameters
READOUTPAR	11 1111 10xx dddd	0000b	enable digital readout via the parallel interf.: D0: a high W/$\overline{\mathrm{R}}$ signal causes a readout reset D1: a high W/$\overline{\mathrm{R}}$ signal stops the readout D2: enable the handshake using the acknowledge signal ACK/CLK D3: read out the Divichi parameter set
READOUTSER	01 0111 xxxx xddd	000b	enable digital readout via the serial interface, D1,D0 = 01: read out one complete frame 10: switch to the pixel readout mode, every new pixel value has to be requested by the **READPIXEL** command 11: read out the Divichi parameter set D2: reset the readout state machine before starting the readout
READPIXEL	001	-	if the sensor is in the pixel readout mode, this command requests a new pixel value

Table E.4: Description of the Divichi control commands (fourth part).

E.2 Sensor interfaces and readout

This section describes the diverse interfaces, that can be used for transmitting the image sensor commands, and the different readout possibilities (analog, digital serial and digital parallel). The unidirectional serial interface and the parallel interface are already explained in chapter 4. Therefore, only a few further comments are necessary. Some more detailed remarks are given with respect to the bidirectional differential serial interface and the manual 3-button interface. Finally, the EEPROM organization of the stored sensor parameter bits is shown.

Using the unidirectional serial interface is the simplest possibility of programming the Divichi chip. It represents the recommended solution, if only the analog sensor readout is required. The corresponding timing diagram can be seen in figure 4.40. The 14 command bits are clocked into the internal shift register with every rising clock edge (MSB first). The end of a command is indicated by a rising edge of the chip-select signal $\overline{\text{WRITESLCT}}$.

The parallel interface only provides 8 lines (DATA[9]-DATA[2]) for transmitting the command codes to the image sensor. Therefore, the 14 bits are divided into two parts corresponding to the description in section 4.7.2. Figure 4.41 shows the timing diagram referring to the write and the two read modes. The data direction (writing or reading) is defined by the W/$\overline{\text{R}}$ line, which has to be high for writing and low for reading. As soon as W/$\overline{\text{R}}$ goes low, the ADC outputs control the 10 data lines of the interface. The actual readout mode has to be selected by using the **READOUTPAR** command. This command includes 4 data bits, D3-D0, with the meaning according to table E.4. Any change of the bits D2-D0 is stored in the internal register until a new change occurs. The bit D3, however, is immediately reset after the parameter readout has finished. It must be noted, that due to the ADC latency of two clock cycles, the first two pixel values of a frame have to be ignored and two additional pixel values are read out at the end of a frame.

The parameter readout via the parallel interface is always carried out in the non-handshake mode independent of the value of D2, as it is coupled to the EEPROM timing. The parameter bits are serially transmitted via the DATA[9] line according to the EEPROM clock frequency ($\approx$ 2.5 Mbits/s). Every new data bit is indicated by the $\overline{\text{VALRDY}}$ signal. The bit order is given by the EEPROM organization shown in section E.2.4.

E.2.1 Analog readout timing

The camera chip Divichi provides three different analog readout modes. The first one is the video mode generating a composite video output signal according to the CCIR standard. In this case, the timing is fixed (see figure 4.39) and the internal timing parameters like LINETIME or PIXELTIME are ignored. The stop command **READSTOP** as well as the $\overline{\text{READWAIT}}$ signal are only regarded at every frame end. In addition, the calibration time (CALTIME) is limited to the readout time of one row in order to guarantee, that all rows are calibrated within one frame. The video mode is enabled by setting the bit D0 of the control register CONTROL B.

The second and third sensor readout modes are enabled by deactivating the video mode. Both modes differ from each other by the value of the forced calibration bit (D3 of CONTROL A). If this bit is deactivated, the calibration time is defined by the CALTIME register. This can cause a difference between the calibration and the readout time of one row leading to the situation, that the distance between calibration and readout row is not fixed. On the other hand, this independence of the calibration and the readout timing ensures, that all rows are calibrated, even if a small subframe or a high averaging level is selected. Activating the forced calibration bit couples the calibration and the readout row so that they are always in phase (similar to the video mode). They are separated from each other by the number of rows defined by the **SETDISTANCE** command.

If the video mode is deactivated, the readout timing is defined by the registers LINETIME and READTIME. LINETIME corresponds to the time between the selection of a new row and the readout of the first pixel of this row. During this period, the pixel source followers can charge the column readout lines to the new voltages. The value of READTIME determines the duration of one pixel cycle. The minimum time (READTIME = 0) is two clock cycles corresponding to the maximum readout frequency of 7.5 MHz.

Figure E.1 shows the exact timing of the analog sensor readout. It includes the three synchronization signals FRAMESTART, LINESTART and $\overline{\text{VALRDY}}$. All timing values are given in clock cycles (cyc) as they depend on the used crystal frequency. In the case of the video frequency of

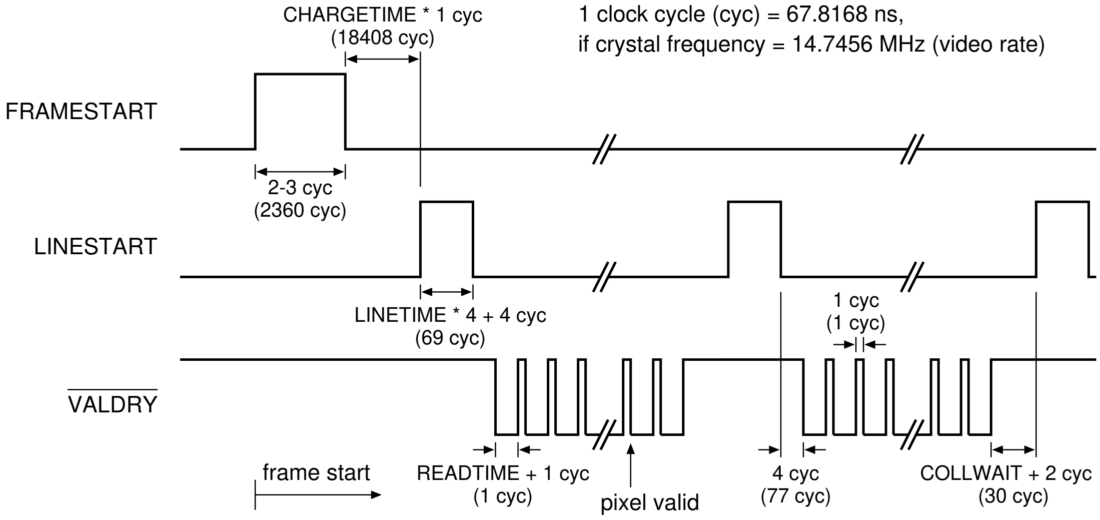


Figure E.1: Timing of the frame, line and pixel synchronization signals.

14.7456 MHz, one cycle takes 67.8168 ns. The readout can be halted at any time by a low $\overline{\text{READWAIT}}$ signal or by the **READSTOP** command. The numbers written in parentheses refer to the video timing, if no zooming and no averaging is activated.

E.2.2 High speed serial interface

The bidirectional serial interface can be used to program the sensor parameters or to read out the ADC data. The basic functionality and the timing diagram of a command writing cycle have already been explained in section 4.7.3. Figure E.2 shows the format of the data words transmitted via the FDATAP and FDATAN lines. For programming a certain command, 17 bits consisting of startbit, chip address and 14 command bits are required. The chip address can be in the range of 0 to 3 and is defined by the level of the external signals CHIPADDR[0] and CHIPADDR[1]. This allows to control and read out up to four chips with the same interface lines. It is essential to start the write cycle with a rising edge of FCLK according to the diagram in figure 4.44 (The MSB is transmitted first).

To read out the digital pixel values or the internal parameters, the sensor has to be changed to one of three serial readout modes. This is achieved by the **READOUTSER** command which is explained in table E.4. In the first mode (frame readout), the sensor immediately enables its differential data output buffer and transmits one complete frame. Subsequently, the sensor changes back to the command receiving mode. The format of the pixel data can be seen in figure E.2. It consists of one startbit, 2 address bits, three status bits and 10 data bits. The status bits indicate the actual position of the pixel. However, due to the ADC latency, the indicated status refers to the data which is transmitted two cycles later.

If more than one chip are connected to the serial interface, only the addressed chip changes to the readout mode whereas the interfaces of all others are disabled. This means, that the non-addressed chips will ignore all further data transmitted via the differential data lines in order to prevent interpreting the image data as a programming command. When the readout is finished, the sensor, which is currently read out, sends a special bit pattern, namely: 1010101010010101. This pattern indicates the end of a frame and reactivates the interfaces of the other attached chips. The readout can be interrupted at any time by holding the clock signal high for a few microseconds.

writing commands to Divichi:

17 bits:			
	1	A1	A0	14 command bits

reading ADC data from Divichi:

16 bits:							
	1	A1	A0	S2	S1	S0	10 data bits

reading sensor parameters from Divichi:

16 bits:								
	1	A1	A0	1	1	1	9 empty bits	D

A0: lower bit of the chip address
A1: upper bit of the chip address

S2, S1, S0	description
011	first pixel of a new frame
110	first pixel of a new line
000	all other pixels
111	parameter readout

D: one bit of the sensor parameters

Figure E.2: Data format of the serial high speed link.

The second serial readout mode (pixel readout) allows to transmit single pixel values. When the sensor has changed to this mode, every new pixel value has to be requested by the **READPIXEL** command. As this command only uses 3 bits (plus startbit and 2 address bits) instead of 14, a fast access is possible. After each transmission, the sensor disables its differential output buffer and accepts the programming of a new command. Since all connected sensor chips can be in the pixel readout mode at the same time, the different chips can alternately transmit their pixel values. If the **READPIXEL** command is sent to a certain sensor, all others are disabled for the duration of one pixel readout. The pixel readout mode has to be disabled by resetting the corresponding register bits with the **READOUTSER** command, whereas the frame readout mode is deactivated automatically at the end of the frame.

The third serial mode refers to the parameter readout. If activated, the internal sensor registers are transmitted using the data format of figure E.2. Every data word contains only one valid data bit. The bit order corresponds to the EEPROM organization which is described in section E.2.4. When the parameter readout is finished, the sensor sends the end sequence already mentioned above and automatically returns to the command receiving mode. For the duration of the parameter readout, all other sensors connected to the same interface line are disabled.

An important note concerning the physical implementation has to be added. The two data lines FDATAN and FDATAP require a passive pull-down and pull-up resistor, respectively, in order to fix the signal level to a low value when both differential buffers (sensor transceiver and external transceiver) are in the high-ohmic state. Otherwise, since the weak internal pull-up and pull-down resistors are implemented in the wrong direction, the line would show a high signal level. This, however, could cause a system reset. If the clock is still running after the data line has changed to the high-ohmic state, the sensor would detect the transmission of a **RESET** command whose bit code is 11111111xxxxxx.

E.2.3 Manual three-button interface

The implemented manual interface allows to change the most important video parameters by using the three buttons on the backside of the camera housing. The middle button steps through the individual commands, whereas the left and the right button increase and decrease the selected parameter value. The bitmaps of the 13 possible commands (the bitmap of the currently selected command is displayed on the video screen as soon as a button is pressed) and the corresponding explanations are shown in figure E.3. If the first command (ZOOM) is selected, the LED on the camera board is switched on. This allows to orientate in the menu structure without using a video screen. The black dots behind some of the bitmaps are only displayed, if the corresponding function is activated.

ZOOM		change the digital zoom factor (LED on)
X-START		change the upper left x-position of the readout frame
Y-START		change the upper left y-position of the readout frame
X-RANGE		change the number of pixels in x-direction
Y-RANGE		change the number of pixels in y-direction
AVERAGE		change the number of pixels averaged in horizontal and vertical direction
CONTRAST		change the contrast by adjusting the gain of the readout amplifier
BRIGHTNESS		change the brightness by adjusting the multiplexer reference voltage Vrefm
AUTOZOOM	●	enable/disable the autozoom function
XY-SHIFT	●	enable/disable the shift of the upper left frame corner into the visible image
INTERLACE	●	enable/disable the interlaced mode
AUTOEXPO	●	enable/disable the automatic exposure control
SAVE	●	save all parameters in the EEPROM

Figure E.3: List of the 13 commands accessible by the manual interface.

The AUTOZOOM function couples the zoom factor to the selected subframe. When the frame size is decreased, the zoom factor is automatically increased in order that the image always covers the whole video screen. The SAVE command stores all parameters, that can be manually adjusted, in the external EEPROM memory. They are automatically recovered after a system reset. The SAVE command is executed by simultaneously pressing the left and the right button for about 1 second. Pressing all three buttons for about 1 second performs a system reset. This can be done at any time independent of the currently selected command.

Due to a bug in the command decoding logic, the automatic exposure control (AUTOEXPO command) cannot be enabled or disabled in the normal way. Since the up/down buttons (left and right buttons) affect the 8th bit of the transfer register, but the decoding logic regards only the 7th bit, no change of the internal auto-expo register occurs. However, the 7th bit of the transfer register can be changed by using another command like the X-START or X-RANGE command. Therefore, to activate the auto-exposure control, the 7th bit has to be set by e.g. adjusting X-RANGE to its maximum value (384). Subsequently, the AUTOEXPO command has to be selected and the left or right button must be pressed. The deactivation is carried out in the same way by setting the 7th bit of the transfer register to zero (e.g. X-START = 1).

E.2.4 EEPROM organization

The different Divichi parameters, which can be stored in the EEPROM, are divided into three blocks. Block 0 contains all values of the manual interface and starts at the EEPROM address 000h. The next block is located at the address 010h and the last block at 020h. The exact data structure of each block is shown in figure E.4. In the case of the parameters consisting of 3 to 9 bits, the names correspond to the Divichi commands in table E.1 to E.4 (just omit the prefix **SET**). The single bit parameters refer to the individual bits of the control registers A, B and C (**SETCONTROL**-commands) which are given in parentheses.

When the parameters are transmitted to the EEPROM (or read back), all parameter registers form a large shift register. The individual flipflops of one parameter are connected in series and the MSB of each parameter is connected to the LSB of the parameter written below. The end of this chain is given

Block 0 (Addr 000h)

GAIN	7 bits
XPOS	9 bits
YPOS	9 bits
XRANGE	9 bits
YRANGE	9 bits
AVERAGEVERT	3 bits
AVERAGEHORI	3 bits
ZOOM	5 bits
AUTOZOOM (D1, CTRL B)	1 bit
OFFSET (D2, CTRL B)	1 bit
INTERLACED (D5, CTRL B)	1 bit
AUTOEXPO (D5, CTRL A)	1 bit
DAC 4	8 bits

data out,
bit 7 of DAC 4

Block 1 (Addr 010h)

DAC 0	8 bits
DAC 1	8 bits
DAC 2	8 bits
DAC 3	8 bits
DAC 5	8 bits
DAC 6	8 bits
DAC 7	8 bits
DAC 8	8 bits
DAC 9	8 bits
DAC 10	8 bits
DAC 11	8 bits
DAC 12	8 bits
DAC 13	8 bits
DAC 14	8 bits
DAC 15	8 bits

Block 2 (Addr 020h)

DAC 16	8 bits
DAC 17	8 bits
DAC 18	8 bits
DACREF	6 bits
CALTIME	8 bits
AUTOTIME	8 bits
LINETIME	7 bits
READTIME	7 bits
DISTANCE	9 bits
CURRGAIN	4 bits
CHARGETIME	4 bits
COLLWAIT	4 bits
CALENABLE (D0, CTRL A)	1 bit
AUTOZEROEN (D1, CTRL A)	1 bit
AUTOZEROSLOW (D2, CTRL A)	1 bit
FORCEDCALIB (D3, CTRL A)	1 bit
CURRPRE (D4, CTRL A)	1 bit
ARRAYDIODES (D6, CTRL A)	1 bit
BORDERDIODES (D7, CTRL A)	1 bit
VIDEOMODE (D0, CTRL B)	1 bit
ALLPIXELS (D2, CTRL B)	1 bit
PDVIDEOAMP (D4, CTRL B)	1 bit
MIRROREN (D6, CTRL B)	1 bit
DACSTOP (D0, CTRL C)	1 bit
DACSLOW (D1, CTRL C)	1 bit
DACPD (D2, CTRL C)	1 bit
ADCENABLE (D3, CTRL C)	1 bit
ADCCLKEXT (D4, CTRL C)	1 bit
CAPENABLE (D5, CTRL C)	1 bit
OUTBIT (D6, CTRL C)	1 bit

Figure E.4: Parameter organization in the EEPROM.

by the MSB of the DAC 4 register which is guided to the data output line. The same happens, if the complete parameter set is read out via the parallel or the serial interface. The order of the transmitted parameter bits corresponds to the order shown in figure E.4.

E.3 Pad and signal descriptions

The image sensor includes 91 pads required for the connection to the outer world. Only a fraction of the pads has to be used for the sensor operation depending on the actual application. Figure E.5 shows a schematic drawing of the pad layout. Most of the pads are located on the left side of the array. At the right border, only a few power and analog bias pads can be found. The following description is divided into digital pads, analog pads and power pads.

E.3.1 Digital pads

The digital pads of Divichi are explained in table E.5 and in table E.6. The first column refers to the pad numbers given in figure E.5 and the second column to the corresponding pin name. All digital I/O pads belong to the digital control part and are located close to that region. The digital output pads include buffers with a driver strength of 4 mA, the input pads correspond to the CMOS signal levels.

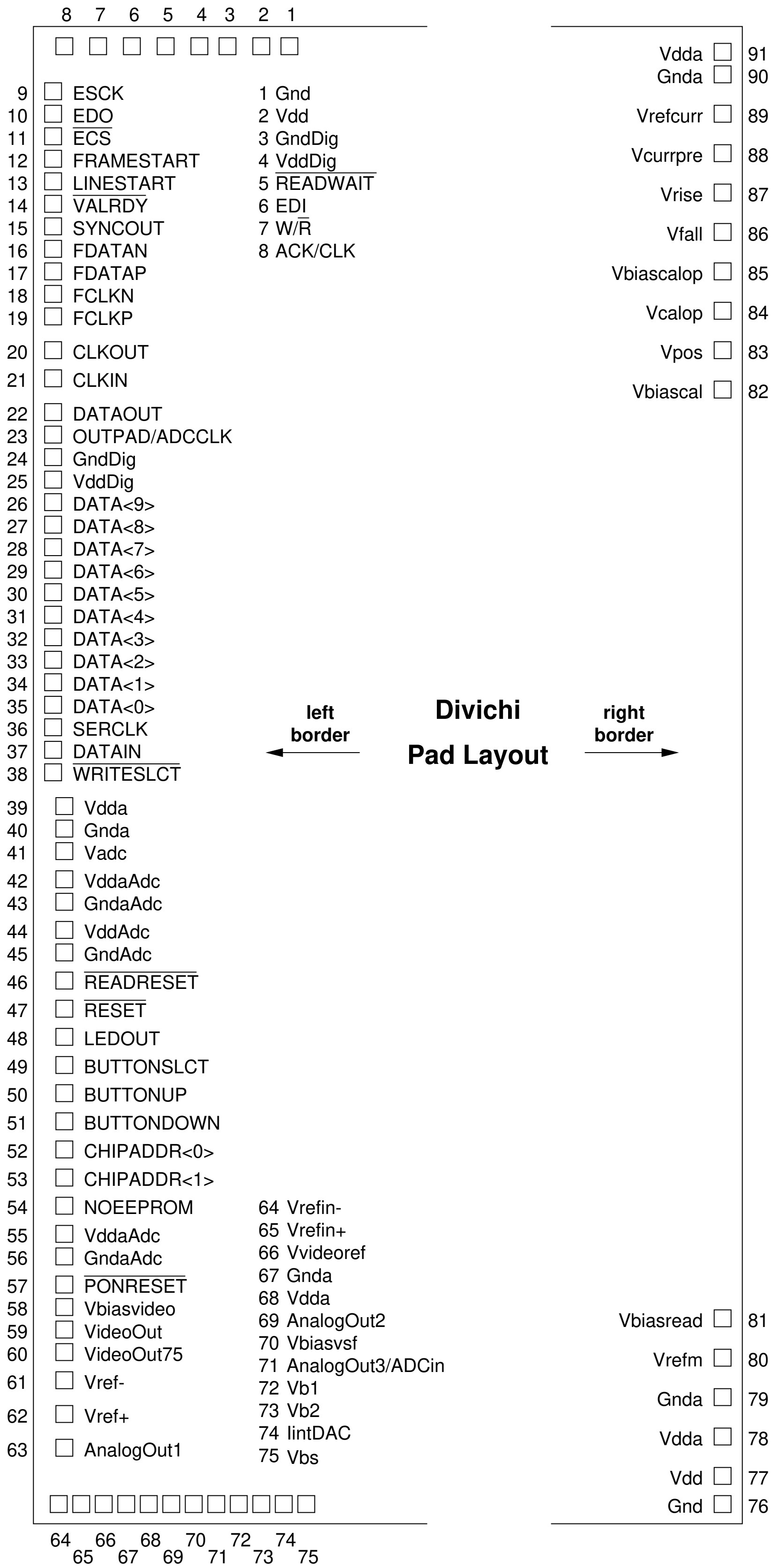


Figure E.5: Schematic drawing of the Divichi pad locations.

pad no.	pin name	type	description
5	$\overline{\text{READWAIT}}$	input (pull-up)	stops the readout at any time (active-low), in video mode only at the end of the frame
6	EDI	input	EEPROM data in, connected to the serial data output pin (SO) of the external EEPROM
7	W/$\overline{\text{R}}$	input (pull-up)	control line of the parallel interface, selects between write (high) and read (low)
8	ACK/CLK	input (pull-up)	control line of the parallel interface. In the read mode, it works as the acknowledge signal. In the write mode, data is clocked into the chip with every rising edge of ACK/CLK.
9	ESCK	output	EEPROM serial clock, connected to the SCK pin of the external EEPROM
10	EDO	output	EEPROM data out, connected to the serial data input pin (SI) of the external EEPROM
11	$\overline{\text{ECS}}$	output	EEPROM chip select (active-low), connected to the $\overline{\text{CS}}$ pin of the external EEPROM
12	FRAMESTART	output	indicates the beginning of a new frame
13	LINESTART	output	indicates the beginning of a new line
14	$\overline{\text{VALRDY}}$	output	indicates, that a new pixel value is valid (active-low), used for analog and digital (parallel) readout
15	SYNCOUT	output	separate output pin for the video synchron. signal
16	FDATAN	input/output	negative data pin of the differential, low voltage serial interface
17	FDATAP	input/output	positive data pin of the differential, low voltage serial interface
18	FCLKN	input	negative clock pin of the differential, low voltage serial interface
19	FCLKP	input	positive clock pin of the differential, low voltage serial interface
20	CLKOUT	output	system clock output of the on-chip oscillator
21	CLKIN	input	system clock input, used with CLKOUT for generating the clock signal by an external crystal and the internal oscillator
22	DATAOUT	output	serial data out of the unidirectional serial interface, used for building up a daisy-chain

Table E.5: Description of the digital I/O pads (first part).

pad no.	pin name	type	description
23	OUTPAD/ ADCCLK	input/output (pull-down)	freely programmable output pin / external clock for the ADC without sample-and-hold stage
26-33	DATA[9-2]	input/output	upper eight bits of the ADC data and data lines of the parallel interface
34/35	DATA[1-0]	output	lower two bits of the ADC data
36	SERCLK	input (pull-up)	serial clock of the unidirectional serial interface
37	DATAIN	input	serial data in of the unidirectional serial interface
38	$\overline{\text{WRITESLCT}}$	input (pull-up)	$\overline{\text{CS}}$ (chipselect) corresponding to the unidirectional serial interface (active-low)
46	$\overline{\text{READRESET}}$	input (pull-up)	reset of the readout state machine (active-low), interrupts the readout at any time
47	$\overline{\text{RESET}}$	input (pull-up)	system reset (active-low)
48	LEDOUT	output	control output for the LED indicating the state of the 3-button interface
49	BUTTONSLCT	input (pull-down)	connected to the button responsible for the command selection
50	BUTTONUP	input (pull-down)	connected to the button increasing the selected value
51	BUTTONDOWN	input (pull-down)	connected to the button decreasing the selected value
52/53	CHIPADDR	input (pull-up)	defines the actual address of the sensor chip, 4 different addresses are possible
54	NOEEPROM	input (pull-up)	must be connected to gnd, if an external EEPROM is attached. Otherwise, the EEPROM interface is disabled and the parameters are not read from the EEPROM after a system reset.
57	$\overline{\text{PONRESET}}$	input (pull-up)	power-on reset, overwrites the internal power-on reset circuit, should be connected to Vdd using a high-ohmic resistor, since the internal pull-up is affected by high illuminations

Table E.6: Description of the digital I/O pads (second part).

E.3.2 Analog pads

The description of the analog Divichi pads is shown in table E.7. Most of the input pads correspond to the diverse bias and control voltages. The pins are connected to the buffers of the integrated bias generator DACs and allow to measure or to overwrite the individual voltages externally. The number of the DAC, which is responsible for the corresponding voltage, is written in parentheses.

pad no.	pin name	type	description
41	Vadc	bias voltage	controls the length of the ADC offset correction cycle for the first comparator stage (DAC 3)
58	Vbiasvideo	bias voltage	bias voltage for the video amplifier (DAC 1)
59	VideoOut	analog in/out	direct output signal of the video amplifier, unbuffered ADC input (no sample-and-hold stage)
60	VideoOut75	analog output	video amplifier output with an internal 75 Ω resistor in series (impedance matching)
61	Vref-	analog in/out	lower end of the ADC reference resistor chain
62	Vref+	analog in/out	upper end of the ADC reference resistor chain
63	AnalogOut1	analog output	additional output of the analog sensor signal, buffered by an operational amplifier with a weaker output buffer than that of the video amplifier
64	Vrefin-	control voltage	lower ref. voltage of the ADC resistor chain (DAC 0)
65	Vrefin+	control voltage	upper ref. voltage of the ADC resistor chain (DAC 6)
66	Vvideoref	control voltage	offset of the video amplifier output
69	AnalogOut2	analog output	additional output buffered by a source follower
70	Vbiasvsf	bias voltage	bias for the output source follower (DAC 15)
71	AnalogOut3/ ADCin	analog in/out	sensor output before passing the mixer and the sample/hold stage, ADC input with sample/hold stage
72	Vb1	bias voltage	bias for the 1st stage of the readout amp. (DAC 13)
73	Vb2	bias voltage	bias for the 2nd stage of the readout amp. (DAC 17)
74	IintDAC	current input	reference current for the bias generator, $\approx 80\ \mu$A (51 kΩ to Vdd)
75	Vbs	bias voltage	bias for the multiplexer source followers (DAC 9)
80	Vrefm	control voltage	reference voltage of the readout multiplexer (DAC 4)
81	Vbiasread	bias voltage	bias for the pixel readout source follower (DAC 5)
82	Vbiascal	bias voltage	bias for the pixel calibr. source follower (DAC 8)
83	Vpos (=Vref)	control voltage	reference voltage for the self-calibration (DAC 16)
84	Vcalop	control voltage	reference voltage for the autozeroing cycle (DAC 12)
85	Vbiascalop	bias voltage	bias for the calibration amplifier (DAC 18)
86	Vfall	control voltage	fall time of the row selection signals (DAC 7)
87	Vrise	control voltage	rise time of the row selection signals (DAC 11)
88	Vcurrpre	control voltage	precharge voltage of the ref. current lines (DAC 14)
89	Vrefcurr	bias voltage	controls the ref. current for the calibration (DAC 2)

Table E.7: Description of the analog I/O pads.

E.3.3 Power supply pads

Finally, the different power pads are summarized in table E.8. The supply voltage of all sensor parts is 5 V. The digital and analog power lines are connected to separate pads to avoid crosstalk between the digital and analog components. If the ADC is not used, the corresponding power pads need not be connected.

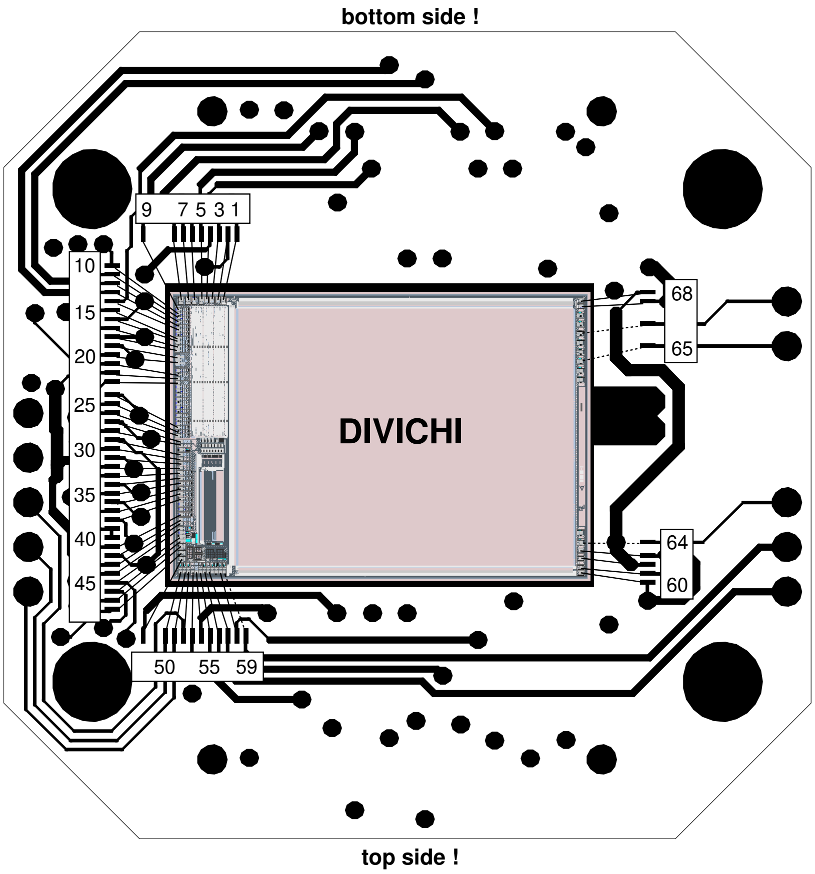
pad no.	pin name	voltage level	description
1,76	Gnd	0 V	ground potential for the digital components of the sensor array (e.g. decoder, digital line driver)
2,77	Vdd	5 V	supply voltage for the digital components of the sensor array (e.g. decoder, digital line driver)
40,67,79,90	Gnda	0 V	ground potential for the analog components of the sensor array (e.g. pixels, readout amplifier)
39,68,78,91	Vdda	5 V	supply voltage for the analog components of the sensor array (e.g. pixels, readout amplifier)
3,24	GndDig	0 V	ground potential for the digital control part
4,25	VddDig	5 V	supply voltage for the digital control part
45	GndAdc	0 V	digital ground potential for the ADC
44	VddAdc	5 V	digital supply voltage for the ADC
43,56	GndaAdc	0 V	analog ground potential for the ADC
42,55	VddaAdc	5 V	analog supply voltage for the ADC

Table E.8: Description of the power supply pads.

E.4 Bond diagram and pin configuration of the camera board

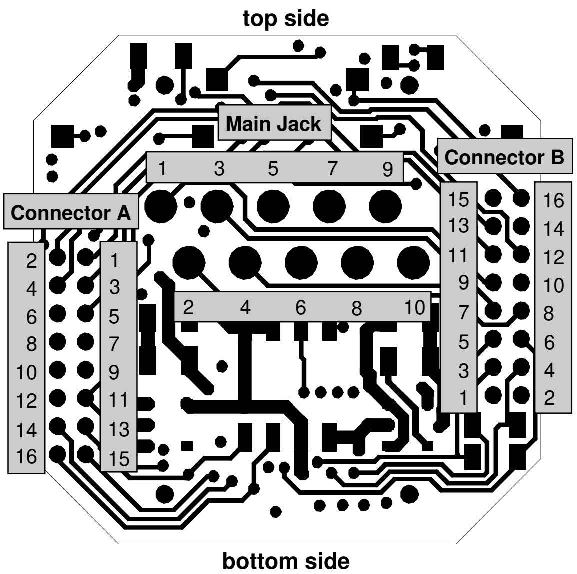
The camera, which has been built using the sensor chip Divichi, contains two printed circuit boards (PCB): the sensor board and the camera board. The sensor board carries the chip, which has been directly bonded to the pads on the PCB. The bonding diagram and the signal names corresponding to the PCB pad numbers are shown in figure E.6. The sensor is located in the middle of the board and connected to the surrounding pads. All names refer to the signals explained in the previous section. The pads labelled as “reserved” can be used for any of the analog bias voltages. They are guided to some pins on the sensor board in order to check the proper operation of the bias generator. Attention should be paid to the rotated layout. When connecting the sensor board to the camera board, it has to be rotated by 180°.

The camera board includes the additional electronics (voltage regulators, EEPROM) and the camera connectors. Figure E.7 shows the layout and the corresponding numbers of the connector pins. The connector A and the connector B are only accessible by opening the camera housing. They are required to configure and to test the camera. The main jack represents the connection to the outer world. It is similar to the RJ45-norm used for the 10-base 2 twisted pair Ethernet or the telephone cables, but provides 10 instead of 6 or 8 pins. Five pins of the main jack (bold names) have to be connected to the corresponding sensor signals by using small jumpers for the connectors A and B. If the analog readout is required, MULTI1 to MULTI4 are connected to the signals $\overline{\text{WRITESLCT}}$, $\overline{\text{READWAIT}}$, SERCLK and DATAIN. Additionally, the desired output line (one of the first 5 signals of connector A) has to be linked to the AnalogMain line. In the case of a digital readout via the serial interface, the signals MULTI1 to MULTI4 are connected to FDATAP, FDATAN, FCLKP and FCLKN.



1	Gnd	36	BUTTONSLCT
2	Vdd	37	BUTTONUP
3	GndDig	38	BUTTONDOWN
4	VddDig	39	CHIPADDR<0>
5	$\overline{\text{READWAIT}}$	40	CHIPADDR<1>
6	EDI	41	NOEEPROM
7	W/$\overline{\text{R}}$	42	VddaAdc
8	ACK/CLK	43	GndaAdc
9	ESCK	44	$\overline{\text{PONRESET}}$
10	EDO	45	VideoOut
11	$\overline{\text{ECS}}$	46	VideoOut75
12	FRAMESTART	47	Vref-
13	LINESTART	48	Vref+
14	$\overline{\text{VALRDY}}$	49	AnalogOut1
15	FDATAN	50	Vrefin-
16	FDATAP	51	Vrefin+
17	FCLKN	52	Vvideoref
18	FCLKP	53	Gnda
19	CLKOUT	54	Vdda
20	CLKIN	55	AnalogOut2
21	OUTPAD/ADCCLK		
22	GndDig	56	Vbiasvsf
23	VddDig	57	AnalogOut3 /ADCin
24	SERCLK		
25	DATAIN	58	IintDAC
26	$\overline{\text{WRITESLCT}}$	59	Vb1,Vb2,Vbs
27	Vdda	60	Gnd
28	Gnda	61	Vdd
29	VddaAdc	62	Vdda
30	GndaAdc	63	Gnda
31	VddAdc	64	reserved
32	GndAdc	65	reserved
33	$\overline{\text{READRESET}}$	66	reserved
34	$\overline{\text{RESET}}$	67	Gnda
35	LEDOUT	68	Vdda

Figure E.6: Bond diagram including the sensor board and the sensor chip Divichi. The bond pads of the board are numbered. The corresponding signal names can be seen on the right side of the diagram.



Pin	Connector A	Pin	Connector B	Pin	Main Jack
1	AnalogOut1	1	+8 V	1	**MULTI3**
2	AnalogOut2	2	Gnd	2	**MULTI2**
3	VideoOut	3	FDATAP	3	**MULTI1**
4	VideoOut75	4	FDATAN	4	**MULTI2**
5	AnalogOut3	5	FCLKP	5	$\overline{\text{RESET}}$
6	**AnalogMain**	6	FCLKN	6	$\overline{\text{VALRDY}}$
7	$\overline{\text{READRESET}}$	7	**MULTI1**	7	FRAMESTART
8	$\overline{\text{VALRDY}}$	8	**MULTI2**	8	**AnalogMain**
9	ACKCLK	9	**MULTI3**	9	+8 V
10	LINESTART	10	**MULTI4**	10	Gnd
11	FRAMESTART	11	SERCLK		
12	OUTPAD	12	DATAIN		
13	$\overline{\text{ECS}}$	13	$\overline{\text{WRITESLCT}}$		
14	ESCK	14	$\overline{\text{READWAIT}}$		
15	EDO	15	$\overline{\text{RESET}}$		
16	EDI	16	$\overline{\text{PONRESET}}$		

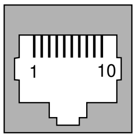


Figure E.7: Pin configuration of the camera board. The corresponding signal names of the three different connectors are written on the right side of the diagram.

E.5 Technical data and performance summary

Technology	0.6 μm single poly, triple metal CMOS process
Die size	11.5×7.7 mm^2
Pixel size	24×24 mm^2
Resolution	selectable, max. 384×288
Dynamic range	6 decades, from 3 mW/m^2 to 3 kW/m^2
Fixed pattern noise	3.8 % of a decade (rms) at an intensity of 1 W/m^2 signal-to-FPN ratio $= 44$ dB (= max. peak-peak signal divided by the rms FPN)
Temporal noise	2.3 % of a decade (rms) at an intensity of 0.5 W/m^2 signal-to-noise ration $= 48$ dB (= max. peak-peak signal divided by the rms noise)
Slope variations	0.90 % (rms) per decade
Analog output	video timing (CCIR or self-defined timing) buffered to drive a 75 Ω load
Digital output	10 bit parallel or serial
Output gain	adjustable in the range of 130 - 720 mV/decade
Supply voltage	5 V analog and digital
Power consumption	100 - 150 mW without 75 Ω load 150 - 200 mW with 75 Ω load (video impedance)
Additional features	random pixel access digital zoom (video mode only) in 32 steps, i.e. zoom factor $1 - 1000$ with respect to the area averaging of up to 8×8 adjacent pixels automatic exposure control manual 3-button interface with on-screen display (video mode) serial programming interface (unidirectional) bidirectional parallel and high speed serial interface EEPROM control for saving and loading the sensor parameters

Appendix F

List of Symbols

Symbol	Description	Unit
A	Area	m^2
	Voltage amplitude	V
A_f	Closed loop gain	-
A_L, A_W, A_{β^2}	Mismatch proportionality constants	μm
A_{VT0}	Threshold voltage mismatch proportionality constant	V$\cdot\mu$m
B_{L^2}, B_{W^2}	Mismatch proportionality constants	μm$^{3/2}$
c	Speed of light	m/s
C	Capacitance	F
C_{fb}	Feedback capacitance	F
C_{gc}	Gate-channel-capacitance	F
C_{gs}	Gate-source-capacitance	F
C_{int}	Integration capacitance	F
C_j	Junction capacitance	F
C_{off}	Offset-compensating capacitance	F
C_{ox}	Gate oxide capacitance per unit area	F/cm^2
C_p	Parasitic capacitance	F
C_s, C_{st}	Storage capacitance	F
D_n	Electron diffusivity	cm^2/s
D_p	Hole diffusivity	cm^2/s
E	Energy	eV
E_e	Irradiance	W/m^2
E_g	Energy of the bandgap	eV
E_{kin}	Kinetic electron energy	eV
E_n	Total electron energy	eV
E_{ph}	Photon Energy	eV
E_v	Illuminance	lx

Symbol	Description	Unit
$\mathcal{E}$	Electric field	V/cm
f	Frequency	Hz
g_m	Gate-channel transconductance	A/V
G_n	Electron generation rate	$m^{-3} \cdot s^{-1}$
h	Planck constant	J·s
h_{FE}	Phototransistor current gain	-
I_C	Collector current	A
I_d	Dark current of the photodiode	A
I_D	Drain current	A
I_e	Radiant intensity	$W \cdot sr^{-1}$
I_{in}	Input current	A
I_{int}	Integration current	A
I_{ph}	Photocurrent	A
I_{ref}	Reference current	A
I_v	Luminous intensity	cd
J, J_{ph}	Light intensity (irradiance)	W/m^2
J_n	Electron current density	A/m^2
k	Wavevector	m^{-1}
	Boltzmann constant	J/K
k_x, k_y, k_z	Components of the 3-dimensional wavevector	m^{-1}
K_m	Proportionality constant between radiometric and photometric quantities	cd·sr/W
l	Length, mean free path	m
L	Semiconductor length and transistor channel length	μm
L_{eff}	Effective transistor channel length	μm
L_n	Electron diffusion length	μm
L_p	Hole diffusion length	μm
m_n^*	Effective mass of the electron	kg
n	Integer, Number of bits (ADC)	-
	Subthreshold slope factor	-
$\tilde{n} = 1 + 1/n$	Effective subthreshold slope factor	-
$n(x)$	Density (concentration) of free electrons at the position x	cm^{-3}
n_i	Intrinsic charge carrier density	cm^{-3}
n_{SiO_2}	Refractive index of SiO_2	-
N	Number of states	-
	Number of occurrences (histogram)	-
N_A	Acceptor impurity density	cm^{-3}

Symbol	Description	Unit
N_D	Donor impurity density	cm^{-3}
N_t	Density of recombination centers	cm^{-3}
N_q	Number of electron-hole pairs	-
N_{ph}	Number of incident photons	-
p	Momentum	$kg{\cdot}m{\cdot}s^{-1}$
	Probability	-
P	Power	W
P_e, P_{ph}	Radiant power	W
P_v	Luminous power	lm
q	Elementary charge	C
Q	Electric charge	C
Q_{inj}	Electric charge due to charge injection	C
r_{out}	Small-signal output resistance	Ω
R	Resistance	Ω
R_{ds}	Drain-source-resistance	Ω
R_{eq}	Equivalent resistance	Ω
R_L	Load resistance	Ω
R_j	Junction resistance	Ω
R_n	Electron recombination rate	$m^{-3}{\cdot}s^{-1}$
t	Time	s
T	Absolute temperature	K
	Period of an oscillation	s
T_{int}	Integration time	s
$\mathcal{T}$	Transmittance	-
$U(t)$	Heaviside-step-function	-
v_{th}	Electron thermal velocity	m/s
V	Voltage	V
$V(\lambda)$	Photopic luminosity function	-
V_b	Bias voltage	V
V_{bi}	Diffusion or built-in potential	V
V_{dd}	Positive supply voltage	V
V_{DS}	Drain-source-voltage	V
V_{es}	Volume of a single electron state in the k-space	m^{-3}
V_{GS}	Gate-source-voltage	V
V_i, V_{in}	Input voltage	V
V_{log}	Logarithmic photoreceptor voltage	V
V_{off}	Offset voltage	V

Symbol	Description	Unit
V_o, V_{out}	Output voltage	V
V_{ref}	Reference voltage	V
V_{sp}	Sphere volume in the k-space	m^{-3}
V_{SB}	Source-bulk-voltage	V
$V_t = kT/q$	Temperature potential	V
V_T	Threshold voltage	V
$\tilde{V}_T$	Shifted threshold voltage	V
W	Transistor channel width	μm
W_{eff}	Effective transistor channel width	μm
W_d	Depletion layer width	μm
x	Position coordinate	m
y	Position coordinate	m
z	Position coordinate	m
α	Optical absorption coefficient	μm^{-1}
β	MOS transconductance factor	A/V^2
ϵ_{si}	Silicon permittivity	F/cm
η	Quantum efficiency	-
λ	Wavelength	μm or nm
	Channel length modulation parameter	-
μ_n	Electron mobility	cm^2/V·s
μ_p	Hole mobility	cm^2/V·s
ν	Photon frequency	Hz
	Amplifier Gain	-
ρ	Density of states	m^{-3}·J^{-1}
σ	Standard deviation	
τ_c	Mean free time	s
τ_n	Electron lifetime	s
τ_p	Hole lifetime	s
ϕ	Digital clock signal	-
ω	Angular frequency	rad/s
Ω	Solid angle	sr

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