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Helix128-x[1]
User Manual

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[1] includes Helix128-2.x and Helix128-3.0

Abstract

Helix128-2 and its variants 2.1, 2.2, and 2.3 are analog readout chips for silicon microstrip detectors and microstrip gaseous chambers manufactured in the 0.8μm-CMOS process of AMS. The chips integrate 128 channels with low noise charge sensitive preamplifier/shapers whose outputs are sampled into an analog pipeline with a maximum latency of 128 sampling intervals. A pipeline readout amplifier, a fast 40MHz multiplexer and a 40MHz current buffer form the backend stages of the designs. Additionally, each channel is equipped with an AC-coupled comparator behind the preamplifier/shaper. All comparators share a common threshold, the output of four neighbouring comparators being ORed and brought offchip.

The bias settings and various other parameters are programmable via a serial line protocol. The chips also integrate some monitoring functionality and the ability to report error conditions.

The latest version is the Helix128-3.0, which will also be the final version for this chip family. On this chip, remaining bugs were fixed and it is additionaly equipped with a failsafe token scheme, which makes the chip useable in long daisy chains.

Contents

List of Tables

1 Changes applied to this manual

Version	Date	Author	description
1.3	30.6.1997	MFR	Changed table 1 on page 15
		MFR	Changed table 5 on page 29
		MFR	`TrigIn` is sampled at the rising edge of `Sclk`
		MFR	Changed description of serial interface on page
		MFR	Changed description of `MuxDisable`
1.4	16.10.1997	MFR	Noted two new bugs.
1.5	28.10.1997	MFR	Changed pad description of Helix128-2.0 and included pad description of Helix128-2.1
1.6	25.2.1998	MFR	Included pad description of Helix128-2.2
1.7	2.3.1998	MFR	Removed bug in analog receiver circuit description
1.8	17.4.1998	WFB, ES	Several bugs removed
1.9	12.5.1998	MFR	Introduced change bars, corrected pad layout for Helix128-2.2/2.3 (tables 10, 15)
2.0	17.12.98	MFR	Included Helix128-3.0 description and corrected Helix128-2.2 pad layout description
2.1	3.2.98	MFR	Corrected bugs in pad layout description and test pulse circuit description. Added description of fail-safe token scheme control bits and corrected several smaller bugs.

2 Important note

This manual describes different versions of the second generation of the Helix readout-chip; the chips developed so far differ in some details, especially concerning pad layout and electrical specification of some control signals. The Helix128-2 (sometimes also called Helix128-2.0) chip is the first in this line; Helix128-2.1 emerged from it by a metal/poly mask redesign.

Helix128-2.2 is an improved version making use of a modified pipeline readout amplifier; it is equipped with LVDS line receivers for some control lines and with a pad layout that will make it compatible with a fail safe token scheme which will be implemented in future. Finally, Helix128-2.3 is a derivation of Helix128-2.2 with yet another pipeline readout amplifier.

The name Helix128-2 is used throughout this manual when describing features that are common for all versions of the chip.

The Helix128-3.0 includes some remaining bug fixes and in addition has implemented a failsafe token mechanism, which enhances reliability in systems with large daisy chains. Only changes applied to this chip with respect to its predecessors are discussed here. The chip will be completely described in its own manual.

3 Analog Signal Processing Architecture

Helix128-2 is an analog readout chip for silicon microstrip detectors and microstrip gaseous chambers specially suited to the needs of the HERA-B experiment [1]. Major electrical specifications are a 10MHz sampling clock frequency (i. e. the bunch crossing frequency) implying a shaper peaking time in the 50 ns regime, a storage time depth of about 10μs to comply with the first level trigger latency, the ability to store up to eight events to equalize statistical trigger fluctuations and the complete deadtimeless readout of the detectors in 10μs due to the mean second level trigger rate of 100kHz. Further demands are lowest possible total system noise and a moderate radiation tolerance of $\leq$2kGy.

To cope with the tremendous amount of detector channels 128 channels are integrated per chip with 41.4μm pitch (which yields in a 50μm overall pitch) of input pads as imposed by the silicon strip detector pitch.

3.1 Overview

Helix128-2 contains 128 channels (see fig. 1), each consisting of

- a low noise charge sensitive preamplifier for signals of both polarities. It is implemented as a folded cascode amplifier circuit with a 342 fF feedback capacitor yielding a gain of 11.2 mV/$\mathrm{MIP_{Si}}$ (1 $\mathrm{MIP_{Si}}$=24000 electrons).
- a CR-RC shaper forming a semigaussian pulse with a peak time of 50... 70ns.
- a buffer amplifier driving the internal pipeline write line and the pipeline cell.
- a comparator circuit indicating hit channels, the output of four neighbouring channels being ORed and brought offchip via open drain outputs.
- an analog pipeline consisting of 128+8+5 capacitors resulting in a maximum latency of 128 events and a multievent buffer capable of storing up to eight triggered events (time slots)
- a switched charge sensitive pipeline readout amplifier.

A cascaded 128+8+1 channel multiplexer and a current output buffer are provided for the fast serial readout of the analog data and the 8 bit pipeline column number.

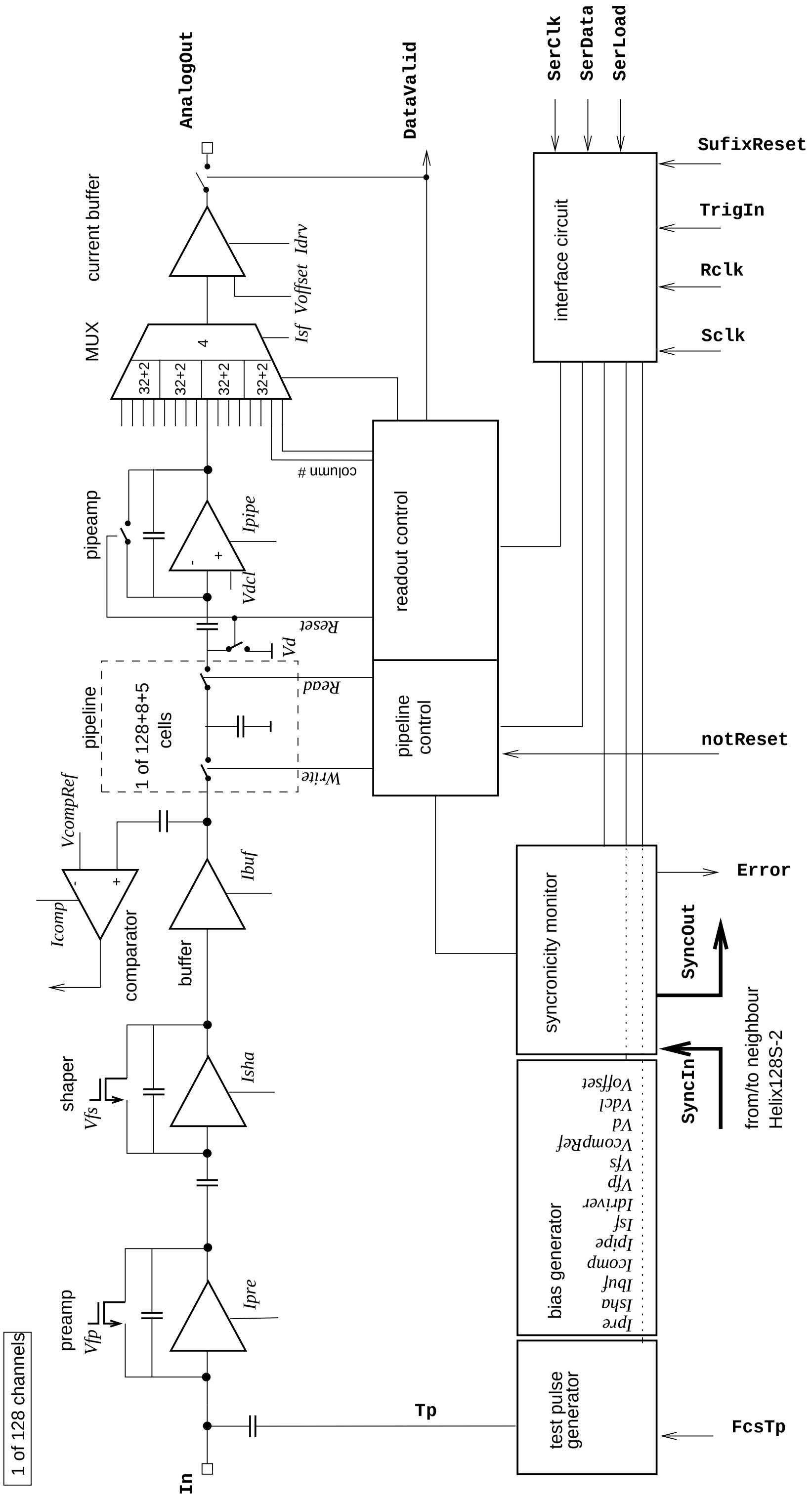

Figure 1: Schematic diagram of Helix128-2

The operation points of all Helix128-2 amplifier stages can be adjusted via programming of corresponding DAC registers. We will outline radiation compensation strategies which ensure proper operation up to the demanded dose of HERA-*B*. Further explanation of the suggested strategies can be found in [5] and [6].

3.2 The frontend (Helix2.1)

Helix128-2 uses the Helix2.1 frontend (fig. 2) which has been carefully optimized with respect to noise, pulse shape (peak time and undershoot), linearity, space and power consumption. More detailed descriptions can be found in [2] and [3].

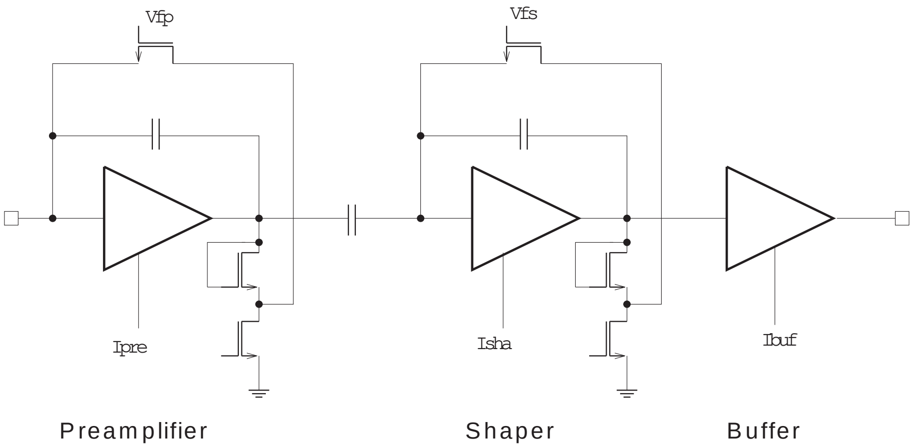

Figure 2: Helix2.1 frontend

To set the frontend operation mode and to compensate for radiation damage the frontend bias voltages and currents (not to be confused with the power supplies +2V,0V,−2V) may be adjusted via programming of the corresponding DAC registers as explained in section 4. The nominal values are listed in table 1.

- *Ipre* sets the preamplifier bias current. With *Ipre* being above a threshold of $\approx 100\mu$A no impact on the peak time is observed [7]. A higher *Ipre* current reduces noise, so that a noise degradation of the preamplifier due to decrease of the g_m of the input transistor can be cured by increasing this current (at the cost of power consumption).

- *Isha* sets the shaper bias current. *Isha* influences the shaper core cell "load resistor" leading to a smaller undershoot for higher currents. Also, the peak-time decreases (see fig. 3) with rising *Isha*. *Isha* should be kept constant under irradiation (pulse degradation should be adjusted basically by *Vfs*).

- *Ibuf* sets the buffer bias current. It hould be kept constant. If the buffer becomes too slow by a decrease of g_m (this can be observed e. g. by changing pulse heights at different `Sclk` frequencies), *Ibuf* can be increased.

- *Vfp* controls the value of the preamplifier feedback resistance. It should be as low as possible for optimum noise performance. *Vfp* should be decreased *continously* during irradiation, so that the preamplifier operates slighly above the *Vfp* cutoff edge (for DC coupled detectors this value can be quite large).

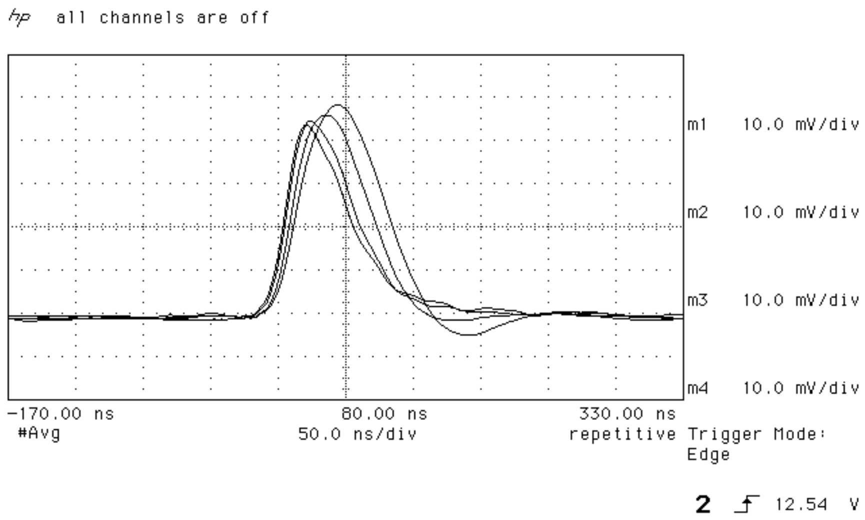

Figure 3: Impact of *Isha* on pulse shape: from slowest to fastest pulse: *Isha*=60μA,100μA,200μA, and 300μA

- *Vfs* controls the value of the shaper feedback resistance and thus determines the discharge of the shaper feedback capacitor (see fig. 4). *Vfs* should be increased *continously* during irradiation, so that the peak time remains constant.

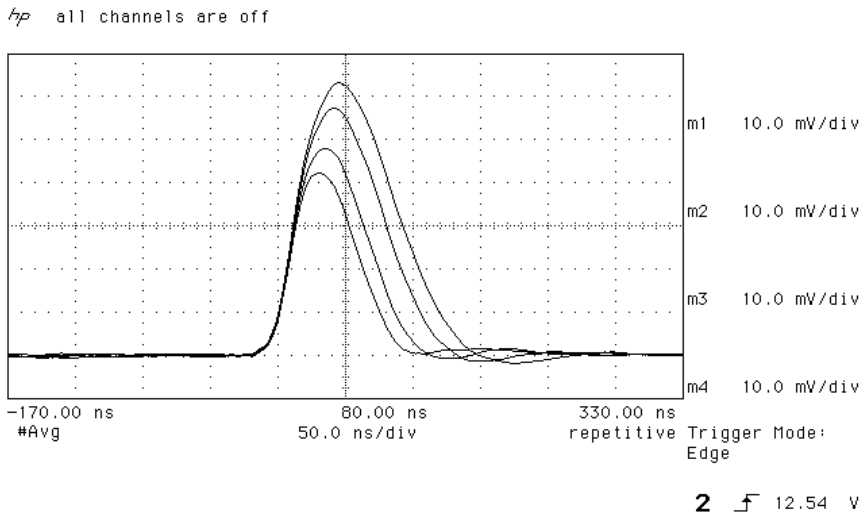

Figure 4: Impact of *Vfs* on pulse shape: from outside to inside *Vfs*=0.8V,1V,1.5V, and 2V

3.3 The comparator

The comparator (fig. 5) with programmable signal polarity is located behind the frontend to detect hit channels. To supress frontend pedestal fluctuations the comparator has been AC-coupled with a large time constant. The output of

Name	Nominal value and dec. reg. cont.	Irradiation compensation
Ipre	200μA=80	$\Rightarrow\Uparrow$
Isha	100μA=40	$\Rightarrow$
Ibuf	100μA=40	$\Rightarrow\Uparrow$
Icomp	50μA=20	$\Rightarrow\Uparrow$
Ipipe (Helix128-2.0...2.1)	50..100μA=20..40	$\Rightarrow$
Ipipe (Helix128-2.2)	40μA=16	$\Rightarrow$
Ipipe (Helix128-2.3)	20μA=8	$\Rightarrow$
Isf	100μA=40	$\Rightarrow\Uparrow$
Idriver	90μA=36	$\Rightarrow$
Vfp	0.2V=71	$\Downarrow$
Vfs	1.5V=113	$\Downarrow$
VcompRef	±20mV=71	$\Rightarrow$
Vdcl (Helix128-2.0...2.2)	1V=97	$\Rightarrow$
Vdcl (Helix128-2.3)	−1.1V=97	$\Rightarrow$
Vd (Helix128-2.0,2.1)	0V=65	$\Downarrow$
Vd (Helix128-2.2,2.3)	−840mV=65	$\Downarrow$
Voffset	−0.5V=55	$\Rightarrow\Uparrow$

Table 1: Nominal values of analog bias voltages and currents and suggested radiation compensation strategies; $\Rightarrow$ indicates no change, $\Downarrow/\Uparrow$ suggests negative/positive adjusting of the corresponding bias. Since the LSB of the 8bit wide voltage value registers is ignored the corresponding values must be multiplied by 2.

four neighbouring channels is ORed, latched on the positive edge of `CompClk` and brought offchip as open drain signals `notCompOut`$\langle$`31...0`$\rangle$ which can drive 4mA at maximum [2].

In case of radiation damage the following strategy is recommended:

- *VcompRef* controls the comparator threshold level (1 $\text{MIP}_{\text{Si}} \approx$ 50mV peak height, so a value of 20mV is a good start to detect MIP signals[3]); due to the AC-coupling this level is independent from radiation induced frontend baseline shifts and so it should not be altered.
- *Icomp* sets the comparator bias current. It can be increased slightly under irradiation (however, no strong effects expected)

3.4 The pipeline

The frontend outputs are stored in a sample&hold capacitor array of $129 \times (128 + 8 + 5)$ cells. Each cell capacitor (850 fF) is connected by a *read* switch to the *read line* (frontend output), and by a *write* switch to the *write line* leading to the

[2] This enables logically "OR"ing several comparator outputs by connecting them to a common drain resistor.

[3] cf. also appendix 6

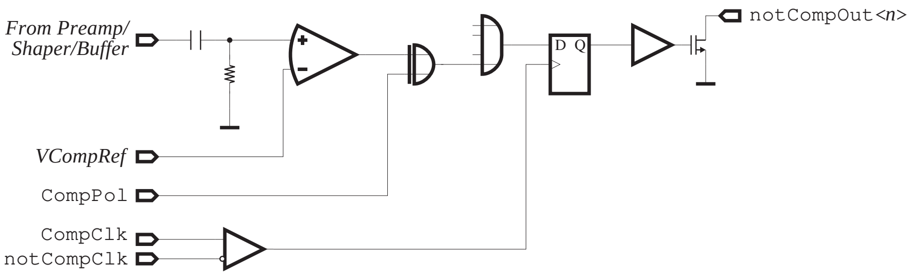

Figure 5: AC-coupled comparator

pipeline readout amplifier ("pipeamp") (fig. 1). The switches are controlled by the pipeline logic which is explained in more detail in section 4.1.

The charge stored per $\mathrm{MIP}_{\mathrm{Si}}$ is $\approx$ 260.000 electrons implying a charge gain of 11, so that the noise requirements on the pipeamp are relatively relaxed.

3.5 The pipeline readout amplifier ("pipeamp")

The pipeline readout amplifier is a switched charge sensitive amplifier (fig. 6). Before operation the internal reset signal is applied thus discharging the two capacitances (for clearness assume *Vdcl*= *Vd*). After the reset the pipeamp is sensitive to the pipeline capacitor charge; since the node at the inverting input stays on constant potential, the charge transfer between the two capacitors causes a related voltage on the output when coupling charge to the input.

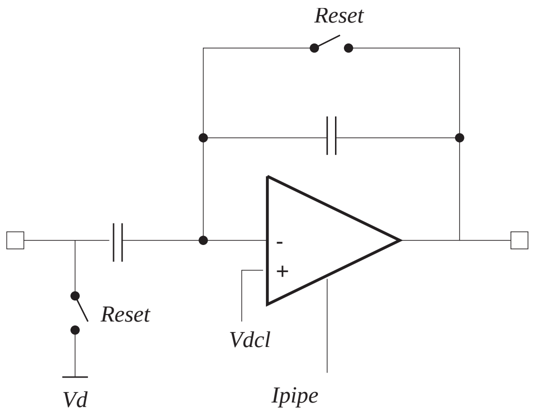

Figure 6: Pipeline readout amplifier: a switched charge sensitive amplifier

The following strategy is recommended in case of radiation damage:

- *Vd* controls the reset level; it should follow the frontend baseline shift, i. e. it should be countinously diminished.
- *Vdcl* controls the folded cascode "ground" level; it should be adjusted after the *Vd* adjustment such that the channel output offsets equal aproximately the pipeline column number's mean value in the readout figure.
- *Ipipe* sets the pipeamp bias current. It should be kept constant.

3.6 The multiplexer

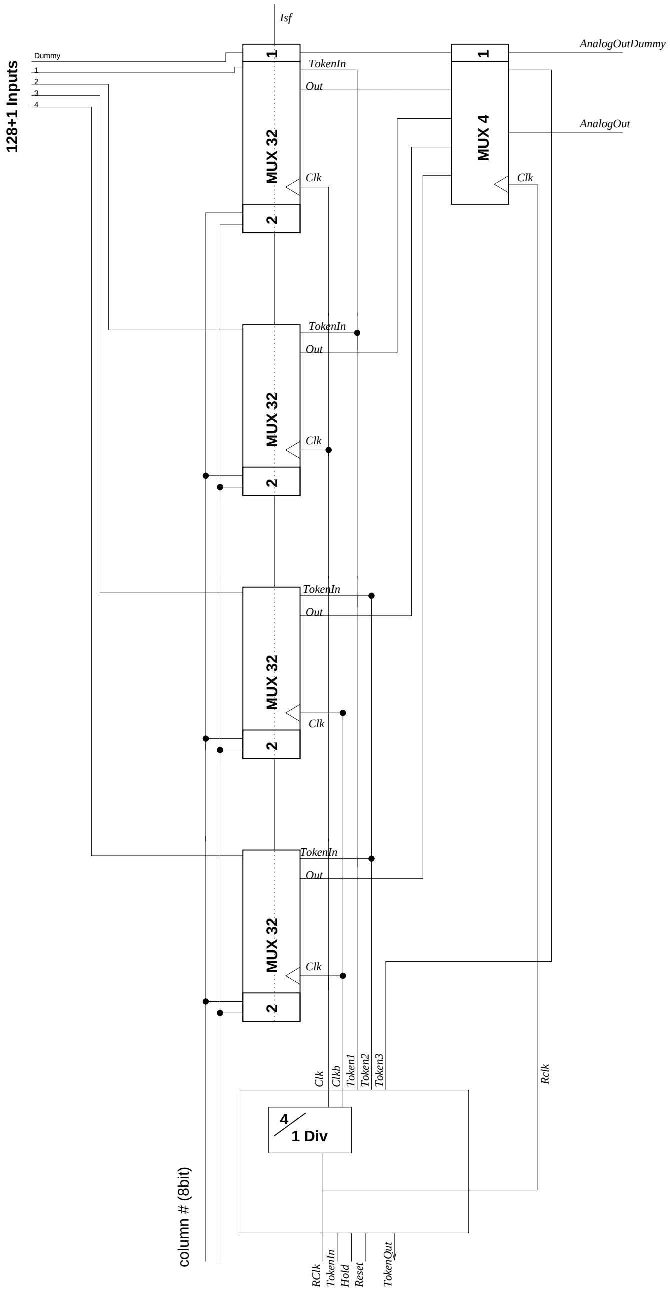

Figure 7: Cascaded 128+8+1 channel multiplexer

The multiplexer (fig. 7) has been implemented using a cascaded architecture, i. e. in the first stage four 34 channel multiplexers operate at a fourth of the `Rclk` rate with a second stage at full `Rclk` speed. This approach would lead to a reordering of the channel numbers. Thus, to equalize this effect a permutation fan through has been implemented so that the channels arrive at the output in their geometrical order. The multiplexer first stage consists of a buffered sample&hold circuit with the drive strength controlled by *Isf*.

In case of radiation damage the following strategy is recommended:

- *Isf* should be kept constant; if the buffer becomes too slow by a decrease of g_m, (this can be observed e. g. by changing pulse heights at different `Rclk` frequencies) *Isf* can be increased.

As can be seen from fig. 7 8 bits denominating the pipeline column the current event has been stored in are "weaven" into the multiplexer, appearing as trailer in the analog output (fig. 9).

3.7 The current buffer

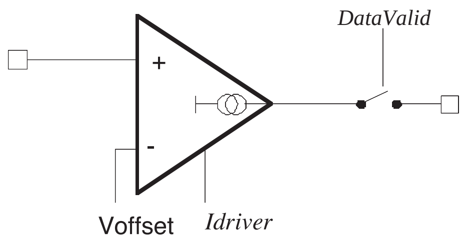

Figure 8: Current buffer

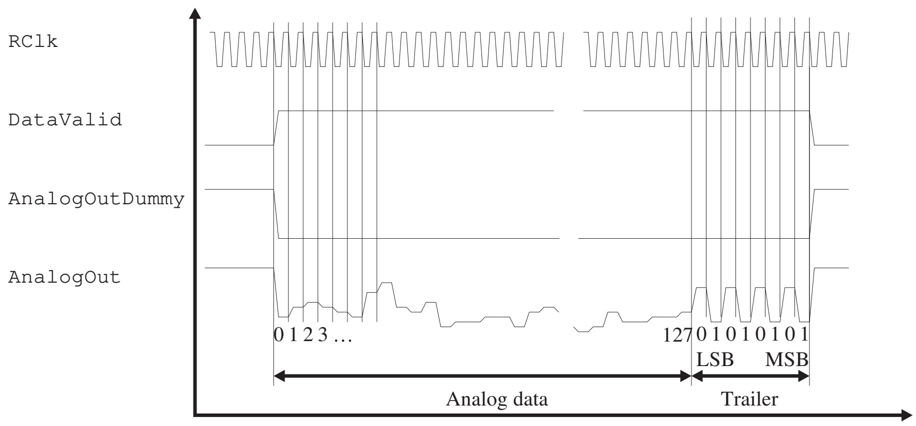

Figure 9: Format of a readout burst

The current buffer is a differential voltage input/single current output ("transconductance") amplifier (fig. 8) that converts the voltage signals delivered by the multiplexer. Linearity is achieved by a current feedback topology. The two multiplexer output voltages *AnalogOut* and *AnalogOutDummy* are amplified by two separate buffers sharing the common reference voltage *Voffset*. In case of radiation damage

- *Idriver* should be kept constant.
- *Voffset* should be adjusted so that the output offset current stays constant (probably the level must be raised).

Figure 9 shows how the chip outputs its data after receiving a trigger. Synchronously to the falling edge of `RClk` data are asserted, indicated by `DataValid` going high. The current output signals `AnalogOut` and `AnalogOutDummy` are plotted as they can be observed at the chip output shorted to ground. The 128 amplifier channels are output channel 0 first, followed by channel 1 etc. up to channel 127. Analog data are followed immediately by an 8 bit trailer showing the pipeline column number the event has been stored in. This number is coded LSB first, a "1" bit coded as ≈+2 MIP_{Si}, a "0" bit as ≈-2 MIP_{Si}. `AnalogOutDummy` should be subtracted from `AnalogOut` to cancel offset, common mode and clock feed through.

3.8 The analog receiver circuit

The current signals delivered on `AnalogOut` and `AnalogOutDummy` should be received by a fast (bandwidth 100 MHz) transimpedance amplifier to make use of the full 40 MHz drive capability of the onchip current buffer and subtracted from each other to reduce common mode interference. The schematic depicted in fig. 10 shows the suggested receiver circuit. The gain delivered at 1.5kΩ transimpedance is ≈ 85mV/MIP_{Si} (Helix128S-2/2.1) resp. 425mV/MIP_{Si} (Helix128S-2.2/2.3). The 50 Ω resistors at the inputs were chosen to terminate properly a 50 Ω cable. The Comlinear CLC 401 opamp features a high bandwidth and the ability to handle large voltage gains (voltage gain = 30 in the suggested configuration).

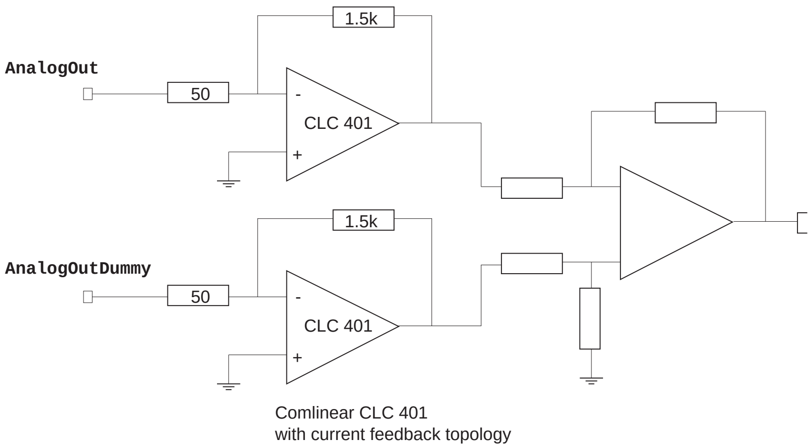

Figure 10: Suggested receiver circuit for the analog signals `AnalogOut` and `AnalogOutDummy` of the Helix128-2.0. For the Helix versions 2.2 and 2.3, 300Ω should be used as feedback resistor together with a Comlinear CLC400 instead of the CL401.

4 Digital Control Circuitry

In the predecessor version to the chip described, HELIX128 [8], the digital control circuitry necessary to operate according to the experimental requirements has been splitted between the HELIX128 itself and the support and control chip SUFIX [9]. In the present version, this separation was abandonned and all functions could be merged into Helix128-2.

4.1 The pipeline and readout control logic

The pipeline control logic (see fig. 1) receives incoming triggers via the interface circuit and tags the corresponding columns of the capacitor storage array such that they are not overwritten by new data before they are read out.

A write pointer scans over the pipeline columns incremented by the sampling clock *Sclk* which can be either internally generated from the `Rclk` or taken from the `Sclk` pad (refer to section 4.4). After `notReset` is set to +2 V, the pointer starts its walk at column 0, the one nearest to the frontend, wrapping around at column number 140 = 128 + 8 + 5 - 1. Sampling the output of the preamplifier/shaper to the storage capacitor is enabled during the high period of `Sclk`, the falling edge determining the held frontend output value.[4]

With the latency specified by the content of the *Latency* register the trigger pointer follows the write pointer. When a trigger occurs (indicated by a high `TrigIn` signal at the rising edge of `Sclk`, see fig. 11), the column number which is currently pointed at by the trigger pointer is stored into a FIFO and marked to be read out. The FIFO has a storage capacity of eight numbers.

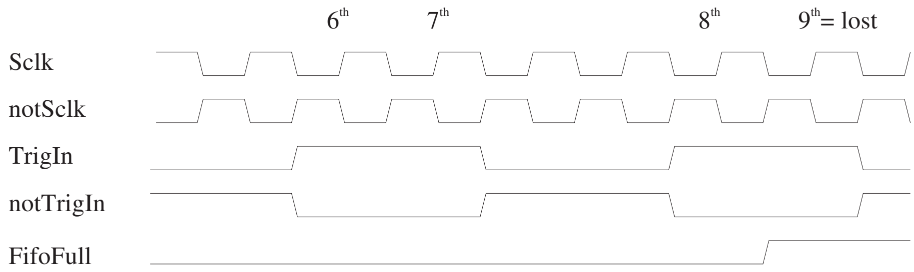

Figure 11: Sampling of the `TrigIn`-signal occurs at the rising edge of `Sclk`; if more than 8 triggers are given in fast sequence, the derandomizing buffer flows over signalling "`FifoFull`"

The "oldest" number within the FIFO is loaded into the read pointer which adresses the column of the storage capacitor array to be loaded into the readout multiplexer. Loading the multiplexer is a multi-stage process: it takes 2 *Sclk* cycles to reset the readout line and the pipeamp, followed by 1 *Sclk* cycle break and another 2 *Sclk* cycles to read the data with the pipeamp until its output is stored by the readout multiplexer. After this period the multiplexer is ready to transmit data.

[4]Since the risetime of the preamplifier/shaper is about 50ns, the high period of the external `Sclk` should be of the same value.

The condition for the multiplexer to start transmission once it has loaded data is given by a high `TransmitEnable`, a high `MultiplexerEnable` and the presence of a token (as explained in section 4.6).

After transmission of data the chip immediately starts loading data from the next tagged column into the multiplexer. In parallel, the chip watches its `ReturnTokenIn` line. When this is high during a falling edge of `Rclk`, the previous pipeline column is untagged thus being available for writing again. Thus, since all chips in a daisy chain share the *ReturnToken* line, the synchronicity of pipeline operation is maintained even in daisy chain operation.

4.2 The bias current sources

The various bias currents of the analog stages described in section 1 are generated by 8 bit digital to analog converters which are controlled by registers of the same name. The conversion slope of the DACs is 2.5μA/LSB with a register value of 0 corresponding to zero output current. To achieve correct operation of the bias generator circuit, a reference current of 100μA must be flowing into the `IrefIn` pad which can be generated either by an external source or by using the internal reference current generator. When using the latter, `IrefOut` has to be bonded directly to `IrefIn` and a resistor of $20k\Omega$ must be connected from `Rref` to `Vssa` (-2V). For good blocking of the reference current, it is recommended to have 100nF parallel to the resistor.

4.3 The control voltage sources

The control voltage sources are generated by DACs with a resolution of 7 bits (Helix128-2/2.1) resp. 8 bits (Helix128-2.2/2.3), working from rail to rail (i.e. from $-2V$ to $+2V$); the slope provided is $\approx$ 31 mV/LSB (Helix128-2/2.1) resp. 15 mV/LSB (Helix128-2.2/2.3). The voltage DACs are controlled by the registers of the same name with the LSBs of the 8 bit wide registers ignored (Helix128-2/2.1). A register setting of 0 corresponds to an output voltage of -2V.

4.4 The sampling clock generator

In the following we discuss the sampling clock *Sclk* ruling the pipeline operation. This clock should not be confused with the comparator's `CompClk` clock described in sect. 3.3 (both run at 10 MHz in the HERA-*B* experiment; both try to catch the maximum pulse height of the shaped frontend pulse but, however, the sampling transitions of the two clock should be slightly detuned to avoid mutual interference).

The falling edge of the sampling clock determines the sampling point of time, i. e. when the frontend outputs are sampled into the pipeline column "on duty". The sampling clock (nominally 10Mhz) *Sclk* can be either applied to the `Sclk` input pad or generated internally from `Rclk`. Therefore the lower four bits of the *ClkDiv* register hold the ratio of the `Rclk` (readout) and *Sclk* (sampling) clocks. Valid values are 0-15. If the content of $ClkDiv = 0$, the signal applied to the `Sclk` input pad is used for sampling. The internally generated *Sclk* will have its first **rising**

edge synchronously with the **fourth rising edge** of `Rclk` following the **rising edge** of `notReset`. This behaviour is illustrated in Fig. 12. The duty cycle of the internally generated *Sclk* signal is 50%.

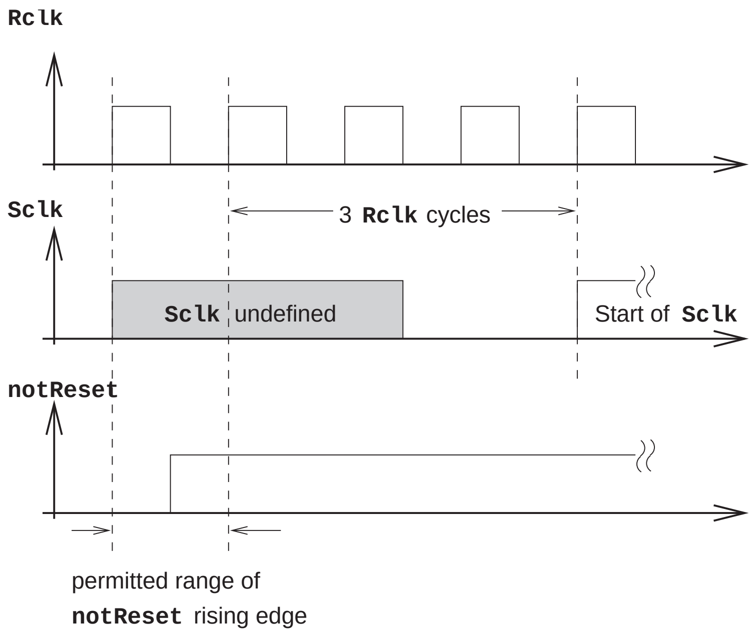

Figure 12: `Sclk` initialization for `Clockdiv` $\neq 0$

4.5 The starter circuit

Helix128-2 features two different resets: first, `SufixReset` resets all the registers as described in table 5 but, however, leaves the pipeline and multiplexer operation unaffected. Applying a `SufixReset` signal after power up is not mandatory since the internal registers should wake up atomatically in the 0 state. `notReset`, on the other hand, only resets the pipeline pointers (described in the following) and the readout multiplexer control circuitry. By activating `notReset`, which may be done asynchronously, an undefined state in the pipeline or in the multiplexer can be corrected without the need of reprogramming all internal bias registers. For an initial reset we recommend to first perform `SufixReset` and `notReset`, then release the `SufixReset` and load the internal registers as described in section 4.9, and finally release `notReset` by setting it to +2 V. The adjustment of the pipeline delay according to the desired trigger latency is done by programming the *Latency* register. To illustrate this feature, we repeat the pipeline operation for convenience (see section 4.1 for a detailed discussion): immediately after releasing the active low `notReset` (synchronously to the rising edge of `Sclk`) the write pointer starts walking over the pipeline incremented by `Sclk`. The pipeline column the `write pointer` currently points at stores the frontend output voltage at the falling edge of `Sclk`. The trigger pointer as the second pointer controlling the pipeline points to the pipeline column to be read out if a trigger on `TrigIn` was given. The start of the pipeline trigger pointer is delayed with respect to the start of the write pointer by the number of `Sclk` cycles specified in the *Latency* register thus determining the latency of the pipeline.

4.6 The readout

4.6.1 Daisy chain mode

Helix128-2 chips can be daisy-chained in order to save cost in following stages. A diagram of several Helix128-2.0/2.1 chips in a daisy chain is given in fig. 13. The following discussion holds for Helix128-2.0/2.1; Helix128-2.2/2.3 makes use of an identical scheme but with reversed token direction (i. e. the chips in a daisy-chain are read out from top to bottom). Failsafe token pads as well as pads for a reversed-polarity token have been added for compatibility with the future Helix128-3.0.

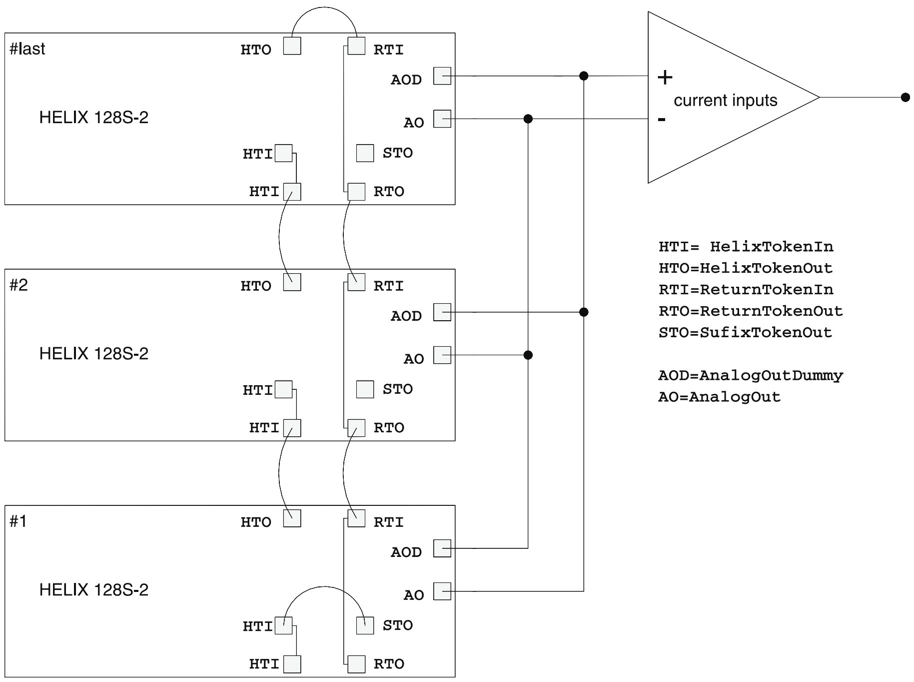

Figure 13: Helix128-2.0/2.1 in daisy chain mode; with Helix128-2.2/2.3 the token circulates in opposite direction (i. e. from bottom to top)

The first or leading Helix128-2 in the daisy chain generates the primary token at the output of `SufixTokenOut`. By bonding `SufixTokenOut` to `HelixTokenIn` on the first chip the token is transferred to the readout multiplexer which starts transmitting the analog values on the common analog busses (the outputs of chips not posessing the token are switched to high ohmic). After the final values of chip #1's analog data the token is output on `HelixTokenOut` of chip #1 to `HelixTokenIn` of chip #2. Upon receipt the second chip's multiplexer starts sending data since the `HelixTokenIn` and `SufixTokenIn` pads are internally connected (the `SufixTokenIn` pad has been added for ease of bonding). By bonding from `HelixTokenOut` to `ReturnTokenIn` on the daisy chain's last chip the *token* is fed into the token return path thus being directly transferred to the leading chip of the chain (since `ReturnTokenIn` and `ReturnTokenOut` are internally connected). By receipt of the returning token the leading chip is signaled the end of the transmission. The signal on the common output bus is illustrated in fig. 14.

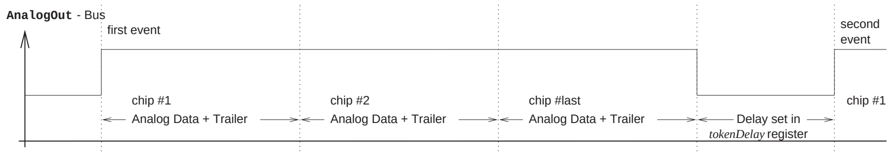

Figure 14: Analog current signal on the `AnalogOut` bus for the daisy chain illustrated in fig. 13

If only a single chip is operated, `SufixTokenOut` must be bonded to `SufixTokenIn` and `HelixTokenOut` to `ReturnTokenIn`.

4.6.2 Failsafe daisy chaining with Helix128-3.0

With Helix128-2 daisy chaining, a single chip failure would cause the complete daisy chain of chips unaccessible. This is especially disastrous when the daisy chain is very long. To decrease the impact of a single chip failure on the whole daisy chain a failsafe daisy chain mechanism has been implemented in the Helix128-3.0, which ensures that no isolated defect chip in a daisy chain can block the complete chain.

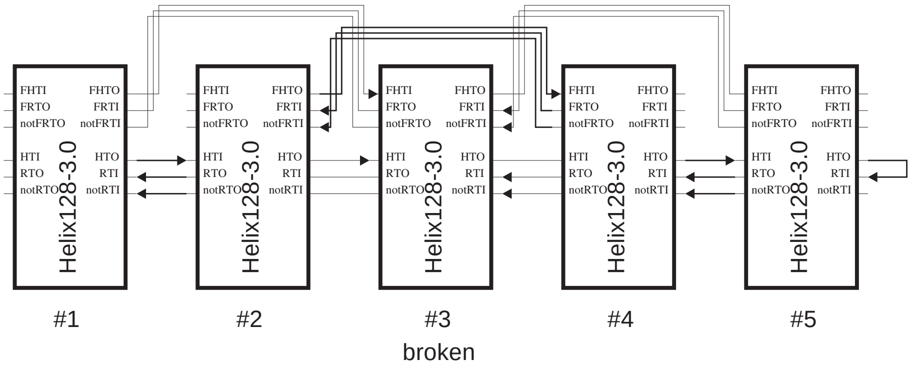

Figure 15: Failsafe daisy chain mechanism. The arrows indicate where tokens are submitted. The thick lines indicate the active token path which is routed around the broken chip in the chain.

Every chip is not only connected to its predecessor and successor in the daisy chain, but also to the second predecessor and successor (fig. 15). When a chip has sent its data it sends a token via the *HelixTokenOut* and *FailsafeHelixTokenOut* ports [5].

These tokens are routed to the chip's successor's *HelixTokenIn* port and to the second successor's *FailsafeHelixTokenIn* port. Normally, a chip starts transmission of data when the token arrives at the *HelixTokenIn* port. The successor of a broken chip can be programmed to start transmission of data upon reception of a token on its *FailsafeTokenIn* port.

The same mechanism is implemented for the *ReturnToken* ports.

[5] *HelixTokenOut* port abbreviates `HelixTokenOut` and `notHelixTokenOut` pads and for all other differential token signals accordingly

The failsafe token mechanism is programmable via the bit 4 ... 7 of the clock divider register. Table 4.6.2 shows all bits necessary for controlling the mechanism.

Bitname	Explanation	Number
BypassHelixToken	If 0 then `HelixTokenIn` is activated, if 1 then `FailsafeHelixTokenIn` is activated	4
BypassReturnToken	If 0 then `ReturnTokenIn` is activated, if 1 then `FailsafereturnTokenIn` is activated	5
LastInChain	If this chip is the last in the chain, this bit must be set to 1	6
FirstInChain	If this chip is the first in the chain, this bit must be set to 1	7

Table 2: Definition of failsafe token control bits and bit number in the *ClkDiv* register

4.6.3 *TokenDelay*

The content of the *TokenDelay* register determines the duration in `RClk` cycles the leading Helix128-2 waits before it starts sending the next event's analog data after having received the return token from the previous readout. Thus, a regular delay in processing of the sent data can be accounted for (see fig. 14). The delay is achieved by holding back the `SufixTokenOut` token output of the leading Helix128-2. A value of 0 indicates immediate sending of the next event. In case of single chip operation the delay as specified in the *TokenDelay* register is added to the time which is needed to load the multiplexer.

4.6.4 `TransmitEnable`

A sudden busy condition of the data receiving stage can be flagged to Helix128-2 by pulling low `TransmitEnable`; it then stops transmitting data and starts again when `TransmitEnable` is pulled up (this condition is checked at the falling `Rclk` edge). `TransmitEnable` is internally pulled up to +2 V.

4.7 The synchronicity monitor

The synchronicity monitor circuit checks the signals of neighbouring Helix128-2 chips to assure synchronous operation. For this purpose, internal signals *TrigMon* and *WriteMon* are generated when the write pointer resp. the trigger pointer passes by column 0 of the pipeline. The synchronicity monitor checks the simultaneous occurrence of these internal signals as well as of the `DataValid` signals with the ones received on `SyncIn<`*i*`>`. `SyncOut<`*i*`>` signals are generated depending on the comparison result according to table 3. The `DataValid` check, naturally, has to be abandonned in daisy chain operation mode.

Using a differential architecture both missing and wrong monitor pulses can be detected. If a deviation occurres, an error signal on `Error` is generated, which should be collected from the last chip in the synchronicity chain.

The content of the *SyncCtrl* register determines the behaviour of the `SyncOut<0:5>` and `Error` signals. A description is given in Tab. 4.

signal name	logic dependency	comment
`SyncOut<0>`	!*TrigMon* & `SyncIn<0>`	*active low wired or* of all *TrigMon* signals
`SyncOut<1>`	*TrigMon* & `SyncIn<1>`	*wired and* of all *TrigMon* signals
`SyncOut<2>`	!*writeMon* & `SyncIn<2>`	*active low wired or* of all *TrigMon* signals
`SyncOut<3>`	*writeMon* & `SyncIn<3>`	*wired and* of all *writeMon* signals
`SyncOut<4>`	`!DataValid` & `SyncIn<4>`	*active low wired or* of all `DataValid` signals
`SyncOut<5>`	`DataValid` & `SyncIn<5>`	*wired and* of all `DataValid` signals

Table 3: Dependencies of the `SyncIn<5:0>` and `SyncOut<5:0>` signals

bit number	function if cleared (*0*)	function if set (*1*)
7 (MSB)	`Error` pin in latch mode (i.e. signal remains high after occurrence of an error	`Error` pin in transient mode (i.e. it becomes active only during the existence of an error condition)
6	`Error` signal is generated from `Sync<0:1>` (i.e. *TrigMon*) signals	`Sync<0:1>` (i.e. *TrigMon*) is ignored for the `Error` signal
5	`Error` signal is generated from `Sync<2:3>` (i.e. *WriteMon*) signals	`Sync<2:3>` (i.e. *WriteMon*) is ignored for the `Error` signal
4	`Error` signal is generated from `Sync<4:5>` (i.e. `DataValid`) signals	`Sync<4:5>` (i.e. `DataValid`) is ignored for the `Error` signal
3	`SyncOut<0:1>` signal is generated from `SyncIn<0:1>` and *TrigMon* signals	`SyncOut<0:1>` = `SyncIn<0:1>` (i.e. *TrigMon* of this Helix128-2 does not contribute to `SyncOut<0:1>`)
2	`SyncOut<2:3>` signal is generated from `SyncIn<2:3>` and *WriteMon* signals	`SyncOut<2:3>` = `SyncIn<2:3>` (i.e. *WriteMon* of this Helix128-2 does not contribute to `SyncOut<2:3>`)
1	`SyncOut<4:5>` signal is generated from `SyncIn<4:5>` and `DataValid` signals	`SyncOut<4:5>` = `SyncIn<4:5>` (i.e. `DataValid` of this Helix128-2 does not contribute to `SyncOut<2:3>`)
0 (LSB)	`Error` = *0* (i.e. reset `Error`, only useful if bit #7 = *0*)	`Error` = *1* (i.e. set `Error`, only useful if bit #7 = *0*)

Table 4: Flags of the *SyncReg* register

4.8 The test pulse circuit

At the rising edge of a signal applied to the `FcsTp` pad, a charge equivalent to

- $\approx +2$ $\mathrm{MIP_{Si}}$ is injected into the inputs of the channels 1, 5, 9, 13 ...,
- $\approx +1$ $\mathrm{MIP_{Si}}$ into channels 2, 6, 10, 14 ...,
- ≈ -1 $\mathrm{MIP_{Si}}$ into channels 3, 7, 11, 15 ... and
- ≈ -2 $\mathrm{MIP_{Si}}$ into channels 4, 8, 12, 16 ....

with $+1 MIP_{\mathrm{Si}}$ being equivalent to a charge of 24.000 electrons.

Thus, with an appropriate trigger a stairway-like readout figure is generated . The polarity of the injected charge toggles after each application (i.e. -1 $\mathrm{MIP_{Si}}$ is injected into channels 1, 5, 9, 13 ... for an even number of test pulses).

4.9 The serial interface

The programming of the Helix128-2's internal registers is achieved via a simple serial interface of three lines. In Helix128-2.0/2.1 the three signals involved are `SerClk`, `SerData`, and `SerLoad`, in Helix128-2.2/2.3 `SerClk` has been merged with `Rclk` and `SerData` with `TrigIn`. Thus, in the latter case, programming of the registers will give rise to multiple triggers; it is therefore recommended to keep `notReset` low during programming. The following explanation applies to Helix128-2.0/2.1, but is easily extended to the new scheme by making the above stated substitution.

During programming of the chip `Rclk` and `SerClk` must run continously. A 20 bit word is applied according to the Helix128-2 data frame (fig. 16) on the `SerData` line synchronously to `SerClk` (fig. 17). The end of the word is signaled to Helix128-2 by activating `SerLoad`; note that `SerClk` must continue running at least one more cycle.

A Helix128-2 serial data frame consists of the following components:

- The *broadcast* or *common set bit*; if set, the chip address decoding is overridden and the register is set to the specified value.
- The *chip address*; the 6 bits of the chip address are compared to the signals of the `ID<5:0>` pads. If they do not match, the following bits are ignored (unless the *broadcast bit* has been set).
- The *register address*; the 5 bits specify the address of the register to be written to.
- The *data* word; the 8 bits contain the value the specified register is set to.

Data are written into the chip with the MSB first. Tab. 5 shows the map of the register addresses.

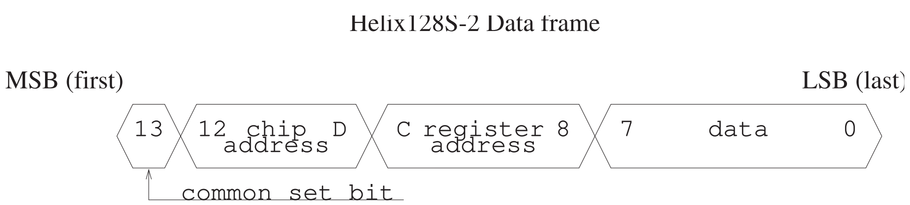

Figure 16: Data format of the Helix128-2 chip

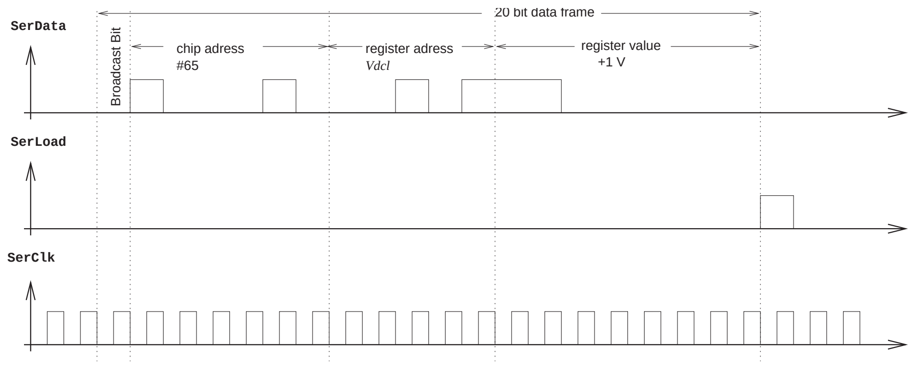

Figure 17: Serial interface timing (Helix128S-2.0/2.1); substituting `SerClk` by `Rclk` and `SerData` by `TrigIn` gives the programming sequence of Helix128S-2.2/2.3. In the example plotted the *Vdcl* bias voltage is set to its nominal (Helix128-2.0/2.1/2.2) value of +1V

4.10 Last but not least

4.10.1 `FifoFull`

The active high `FifoFull` flag is set when all eight slots in the event buffer are occupied; in this case Helix128-2 does not accept any further triggers and the corresponding events will be lost.

4.10.2 `MuxDisable`

`MuxDisable` is out of use.

Register address (*HEX*)	(*BIN*)	(*DEC*)	Register name
01	00001	01	*Ipre*
02	00010	02	*Isha*
03	00011	03	*Ibuf*
04	00100	04	*Icomp*
05	00101	05	*Ipipe*
06	00110	06	*Isf*
07	00111	07	*Idriver*
08	01000	08	*Vfp*
09	01001	09	*Vfs*
0A	01010	10	*VcompRef*
0B	01011	11	*Vd*
0C	01100	12	*Vdcl*
0D	01101	13	*Voffset*
11	10001	17	*Latency*
12	10010	18	*SyncReg*
13	10011	19	*ClkDiv*
14	10100	20	*TokenDelay*

Table 5: Helix128-2 register map

5 Appendix: Pad Description

To match the pitch of 50μm silicon microstrip detectors an overall pitch of 50μm can be obtained by placing Helix128-2 chips side by side. The 128 analog input pads are located at the front of the chip w. r. t. the detector (see fig. 18) while all pins necessary to operate the chip, i. e. power supply, digital control lines and analog output, are located at the rear side. The chip's trigger output pads are placed at the bottom side (with the input pads left) due to the relaxed space requirements of the HERA-*B* Inner Tracking Detector which makes use of the comparator information. Digital signals are categorized as outlined in table 6. For a description of the analog pads refer to the text.

All pads have been given reference numbers. Counting starts with the uppermost pad of the front (i. e. detector) side (with the input pads left) and continues with the peripheral pads counterclockwise around the chip. Finally, the probe pads in the chip's interior are counted from bottom to top. For the geometrical location refer to figure 18 on page 47 (Helix128-2), fig. 19 on page 48 (Helix128-2.1), and fig. 20 on page 49 (Helix128-2.2/2.3).

5.1 Front pads

The analog input pads and some analog supply pads are located at the front side of Helix128-2. The input pads are staggered fourfold with a pitch of 41.4μm. A description is given for Helix128-2.0 and Helix128-2.1 in table 7 on page 32, a description for Helix128-2.2/2.3 can be found in table 8 on page 32.

5.2 Bottom pads

The bottom pads of Helix128-2.0/2.1 are explained in table 9 on page 33. The bottom pads of Helix128-2.2/2.3 are explained in table 10 and 11 on page 34 and 35, respectively.

Type	Description
input	Digital CMOS input operating at -2V...+2V supply.
output	Digital CMOS output operating at -2V...+2V supply.
input (int. pulldown)	Digital CMOS input operating at -2V...+2V supply with internal pulldown resistor.
input (int. pullup)	Digital CMOS input operating at -2V...+2V supply with internal pullup resistor.
output (open drain)	Digital open drain output operating at -2V...+2V supply.
LVDS-input	Low voltage differential CMOS input ($\Delta V_{Sig,notSig} \geq 350$ mV)

Table 6: Electrical specification of digital input and output pads

Ref. no.	Pin name	Type	Description
1	`Vdda`	supply	positive analog supply voltage (+2V)
2	`Vssa`	supply	negative analog supply voltage (−2V)
3	`In⟨0⟩`	analog input	input of channel 0
4	`In⟨1⟩`	analog input	input of channel 1
5	`In⟨2⟩`	analog input	input of channel 2
6-128	⋮	⋮	⋮
129	`In⟨126⟩`	analog input	input of channel 126
130	`In⟨127⟩`	analog input	input of channel 127
131,132	`Gnda`	supply	analog ground (0V)

Table 7: Pads on the front side of Helix128-2.0/2.1. The first pad in the table corresponds to the uppermost pad of the front side (looking at the chip with the frontside left). The geometrical locations throughout the manual will always be referred to this orientation.

Ref. no.	Pin name	Type	Description
1	`Vdda`	supply	positive analog supply voltage (+2V)
2	`Vssa`	supply	negative analog supply voltage (−2V)
2a	`InTest`	input	analog input pad for test channel
3	`In⟨0⟩`	analog input	input of channel 0
4	`In⟨1⟩`	analog input	input of channel 1
5	`In⟨2⟩`	analog input	input of channel 2
6-128	⋮	⋮	⋮
129	`In⟨126⟩`	analog input	input of channel 126
130	`In⟨127⟩`	analog input	input of channel 127
131,132	`Gnda`	supply	analog ground (0V)

Table 8: Pads on the front side of Helix128-2.2/2.3. The first pad in the table corresponds to the uppermost pad of the front side (looking at the chip having the frontside left). The geometrical locations throughout the manual will always be referred to this orientation.

Ref. no.	Pin name	Type	Description
133,134	`Gnda`	supply	analog ground (0V)
135,136	`Vssa`	supply	negative analog supply voltage (−2V)
137,138	`Vdda`	supply	positive analog supply voltage (+2V)
139	`VssComp`	supply	negative supply voltage for comparator (−2V)
140	`VddComp`	supply	positive supply voltage for comparator (+2V)
141	`notCompClk`	input	active low comparator dummy clock
142	`CompClk`	input	active high comparator clock
143	`CompPol`	input	polarity switch for comparator +2V⇒ detection of positive signals
144	`notCompOut`⟨31⟩	output (open drain)	ORed active low output of comparators on channels 127. . . 124
145	`notCompOut`⟨30⟩	output (open drain)	ORed active low output of comparators on channels 123. . . 120
146-173	⋮	⋮	⋮
174	`notCompOut`⟨1⟩	output (open drain)	ORed active low output of comparators on channels 7. . . 4
175	`notCompOut`⟨0⟩	output (open drain)	ORed active low output of comparators on channels 3. . . 0
176	`MuxDisable`	input (int. pulldown)	Out of use
177	`TransmitEnable`	input (int. pullup)	−2V disables analog data transmission
178	`FifoFull`	output	indicates readout fifo overflow.
179	`HelixTokenIn`	input	to be connected to pad no. 257 `HelixTokenOut` of predecessing Helix128-2.0/2.1 if the chip is nonleading in a daisy chain (not to be connected for single chip operation and if the chip is the first in a daisy chain)
180	`ReturnTokenOut`	output	to be connected to pad no. 256 `ReturnTokenIn` of predecessing Helix128-2.0/2.1 if the chip is nonleading in a daisy chain (not to be connected for single chip operation and if the chip is the first in a daisy chain)
181	`SyncIn`⟨0⟩	input (int. pullup)	synchronicity monitoring input from neighbouring Helix128-2.0/2.1
182	`SyncIn`⟨1⟩	input (int. pullup)	“
183-185	⋮	⋮	⋮
186	`SyncIn`⟨5⟩	input (int. pullup)	“
187-197	n. c.		

Table 9: Pads on the bottom side of Helix128-2.0/2.1. The first pad in the table corresponds to the very left hand pad of the bottom side (with the frontside left).

Ref. no.	Pin name	Type	Description
133,134	`Gnda`	supply	analog ground (0V)
135,136	`Vssa`	supply	negative analog supply voltage (−2V)
137,138	`Vdda`	supply	positive analog supply voltage (+2V)
138a	`GndComp`	supply	Reference voltage for comparators' AC coupling
139	`VssComp`	supply	negative supply voltage for comparator (−2V)
140	`VddComp`	supply	positive supply voltage for comparator (+2V)
141	`notCompClk`	LVDS-input	active high comparator dummy clock
142	`CompClk`	LVDS-input	active low comparator clock
143	`CompPol`	input	polarity switch for comparator +2V⇒ detection of positive signals
144	`notCompOut`⟨31⟩	output (open drain)	ORed active low output of comparators on channels 127. . . 124
145	`notCompOut`⟨30⟩	output (open drain)	ORed active low output of comparators on channels 123. . . 120
146-173	⋮	⋮	⋮
174	`notCompOut`⟨1⟩	output (open drain)	ORed active low output of comparators on channels 7. . . 4
175	`notCompOut`⟨0⟩	output (open drain)	ORed active low output of comparators on channels 3. . . 0
176	`VssComp`	supply	−2V supply for `notCompOut`⟨1⟩
177	`TransmitEnable`	input (int. pullup)	−2V disables analog data transmission
178	`FifoFull`	output	indicates readout fifo overflow.
178a	`VssComp`	supply	−2V supply for `notCompOut`⟨1⟩

Table 10: Pads on the bottom side of Helix128-2.2/2.3. The first pad in the table corresponds to the very left hand pad of the bottom side (with the frontside left). See table 11 for pads 179. . . 197a.

Ref. no.	Pin name	Type	Description
179	`notHelixTokenOut`	output	Reserved for future use
180	`notReturnTokenIn`	input	Reserved for future use
180a	`ReturnTokenIn`	input	return path token input; must be bonded to pad no. 187 `HelixTokenOut` if the chip is the last in the daisy chain and for single chip operation (otherwise bonded to pad no. 257a `ReturnTokenOut` of following chip in the daisy chain)
181	`SyncIn`⟨0⟩	input (int. pullup)	synchronicity monitoring input from neighbouring Helix128-2.2/2.3
182	`SyncIn`⟨1⟩	input (int. pullup)	"
183-185	⋮	⋮	⋮
186	`SyncIn`⟨5⟩	input (int. pullup)	"
187	`HelixTokenOut`	output	must be bonded to pad no. 180a `ReturnTokenIn` if the chip is the last in the daisy chain and for single chip operation (otherwise bonded to pad no. 251 `HelixTokenIn` of following chip in the daisy chain)
188	`notFailsafe-HelixTokenOut`	output	Reserved for future use
189	`notFailsafe-ReturnTokenIn`	input	Reserved for future use
190	`Failsafe-ReturnTokenIn`	input	Reserved for future use
191	`Failsafe-HelixTokenOut`	output	Reserved for future use
192	n. c.		
193-197a			Removed

Table 11: Pads on the bottom side of Helix128-2.2/2.3 (continued). The first pad in the table corresponds to the very left hand pad of the bottom side (with the frontside left). See table 10 for pads 133…178a.

Ref. no.	Pin name	Type	Description
179	n. c.		Reserved for future use
180	`notReturnTokenIn`	input	Reserved for future use
180a	`ReturnTokenIn`	input	return path token input; must be bonded to pad no. 187 `HelixTokenOut` if the chip is the last in the daisy chain and for single chip operation (otherwise bonded to pad no. 257a `ReturnTokenOut` of following chip in the daisy chain)
181	`SyncIn⟨0⟩`	input (int. pullup)	synchronicity monitoring input from neighbouring Helix128-2.2/2.3
182	`SyncIn⟨1⟩`	input (int. pullup)	"
183-185	⋮	⋮	⋮
186	`SyncIn⟨5⟩`	input (int. pullup)	"
187	`HelixTokenOut`	output	must be bonded to pad no. 180a `ReturnTokenIn` if the chip is the last in the daisy chain and for single chip operation (otherwise bonded to pad no. 251 `HelixTokenIn` of following chip in the daisy chain)
188	n. c.		Reserved for future use
189	`notFailsafeReturnTokenIn`	input	To be connected to `notFailsafeReturnTokenOut` of the next but one chip in the chain.
190	`FailsafeReturnTokenIn`	input	To be connected to `FailsafeReturnTokenOut` of the next but one chip in the chain.
191	`FailsafeHelixTokenOut`	output	To be connected to `FailsafeHelixTokenIn` of the next but one chip in the chain.
192	n. c.		Reserved for future use
193-197a			Removed

Table 12: Pads on the bottom side of Helix128-3.0 (continued). The first pad in the table corresponds to the very left hand pad of the bottom side (with the frontside left). See table 10 for pads 133…178a.

5.3 Rear pads

The pads on the rear side of Helix128-2.x are placed in a 140μm pitch. A description of the pads of Helix128-2.0 is given in table 13 on page 38, of Helix128-2.1 in table 14 on page 39, and of Helix128-2.2 in table 15on page 40.

Ref. no.	Pin name	Type	Description
240	`Vddg`	supply	positive pad guard supply voltage (+2V)
239,238	`Vddd`	supply	positive digital supply voltage +2V)
237-234	`Vdda`	supply	positive analog supply voltage (+2V)
233-230	`Vssa`	supply	negative analog supply voltage (−2V)
229,228	`Vssd`	supply	negative digital supply voltage (−2V)
227	`Vssg`	supply	negative pad guard supply voltage (−2V)
226	`Rref`	output	to be connected to external resistor (20kΩ) if internal reference current source is used.
225	`IrefOut`	output	output of internal reference current source
224	`IrefIn`	input	reference current input for internal current DAC; may either be connected to an external reference current source or to the `IrefOut` pin, if internal reference current source is to be used
223	`Voffset`	blocking outp.	should be connected to external blocking capacitor
222	`Idriver`	blocking output	"
221	`Vdcl`	blocking output	" $> 1\mu F$
220	`Vd`	blocking output	" $> 1\mu F$
219	`VcompRef`	blocking output	"
218	`AnalogOutDummy`	output	dummy serial analog output, should be subtracted from `AnalogOut`
217	`AnalogOut`	output	serial analog output
216,215	n. c.	n.c.	not connected
214	`Id⟨0⟩`	input (int. pulldown)	active high chip id adress
213-209	⋮	⋮	⋮
209	`Id⟨5⟩`	input (int. pulldown	"
208	`FcsTp`	input	digital test pulse input; the rising edge signals moment of charge injection
207	`SufixReset`	input (int. pulldown	active high reset signal for bias generator and controller part
206	`notReset`	input	active low pipeline reset signal
205	`DataValid`	output	active high signal indicating valid data on `analogOutDummy` and `analogOut`
204	`Error`	output	active high signal indicating an error condition on the chip
203	`SerLoad`	input	active high load signal for serial line interface
202	`SerData`	input	active high data signal for serial line interface
201	`TrigIn`	input	active high readout trigger input
200	`SerClk`	input	active high clock of serial line interface
199	`Rclk`	input	active high readout clock for data multiplexer
198	`Sclk`	input	active high sampling clock; the falling edge signals the sampling point of time

Table 13: Pads on the rear side of Helix128-2.0. The first pad in the table corresponds to the uppermost pad of the chip's rear side (with the frontside left).

Ref. no.	Pin name	Type	Description
240	`Vddg`	supply	positive pad guard supply voltage (+2V)
239,238	`Vddd`	supply	positive digital supply voltage (+2V)
237-234	`Vdda`	supply	positive analog supply voltage (+2V)
233-230	`Vssa`	supply	negative analog supply voltage (−2V)
229,228	`Vssd`	supply	negative digital supply voltage (−2V)
227	`Vssg`	supply	negative pad guard supply voltage (−2V)
226	`Rref`	output	to be connected to external resistor (20kΩ) if internal reference current source is used.
225	`IrefOut`	output	output of internal reference current source
224	`IrefIn`	input	reference current input for internal current DAC; may either be connected to an external reference current source or to the `IrefOut` pin, if internal reference current source is to be used
223	`Voffset`	block. outp.	should be connected to external blocking capacitor
222	`Idriver`	block. outp.	"
221	`Vdcl`	block. outp.	" $> 1\mu F$
220	`Vd`	block. outp.	" $> 1\mu F$
219	`VcompRef`	block. outp.	"
218	`AnalogOutDummy`	output	dummy serial analog output, should be subtracted from `AnalogOut`
217	`AnalogOut`	output	serial analog output
216	`Id⟨0⟩`	input (int. pulldown)	active high chip id adress
215-211	⋮	⋮	⋮
211	`Id⟨5⟩`	input (int. pulldown)	"
210	`FcsTp`	input	digital test pulse input; the rising edge signals moment of charge injection
209	`SufixReset`	input (int. pulldown)	active high reset signal for bias generator and controller part
208	`notReset`	input	active low pipeline reset signal
207	`DataValid`	output	active high signal indicating valid data on `AnalogOutDummy` and `AnalogOut`
206	`Error`	output	active high signal indicating an error condition on the chip
205	`SerLoad`	input	active high load signal for serial line interface
204	`SerData`	input	active high data signal for serial line interface
203	`TrigIn`	input	active high readout trigger input
202	`SerClk`	input	active high clock of serial line interface
201	`notRclk`	input	active low readout clock for data multiplexer
200	`Rclk`	input	active high readout clock for data multiplexer
199	`notSclk`	input	active low sampling clock; the rising edge signals the sampling point of time
198	`Sclk`	input	active high sampling clock; the falling edge signals the sampling point of time

Table 14: Pads on the rear side of Helix128-2.1. The first pad in the table corresponds to the uppermost pad of the chip's rear side (with the frontside left).

Ref. no.	Pin name	Type	Description
240	`Vddg`	supply	positive pad guard supply voltage (+2V)
239,238	`Vddd`	supply	positive digital supply voltage (+2V)
237-234	`Vdda`	supply	positive analog supply voltage (+2V)
233-230	`Vssa`	supply	negative analog supply voltage (−2V)
229,228	`Vssd`	supply	negative digital supply voltage (−2V)
227	`Vssg`	supply	negative pad guard supply voltage (−2V)
226	`Rref`	output	to be connected to external resistor (20kΩ) if internal reference current source is used.
225	`IrefOut`	output	output of internal reference current source
224	`IrefIn`	input	reference current input for internal current DAC; may either be connected to an external reference current source or to the `IrefOut` pin, if internal reference current source is to be used
223	`Idriver`	blocking outp.	should be connected to external blocking capacitor
222	`VcompRef`	blocking outp.	"
221	`Vd`	blocking outp.	"
220	`Vdcl`	blocking outp.	"
219	`Voffset`	blocking outp.	"
218	`AnalogOutDummy`	output	dummy serial analog output, should be subtracted from `AnalogOut`
217	`AnalogOut`	output	serial analog output
216	`Id⟨0⟩`	input (int. pulldown)	active high chip id adress
215	`Id⟨1⟩`	input (int. pulldown)	"
214-211	⋮	⋮	⋮
211	`Id⟨5⟩`	input (int. pulldown)	"
210	`FcsTp`	input	digital test pulse input; the rising edge signals moment of charge injection
209	`SufixReset`	input (int. pulldown)	active high reset signal for bias generator and controller part
208	`notReset`	input	active low pipeline reset signal
207	`DataValid`	output	active high signal indicating valid data on `analogOutDummy` and `analogOut`
206	`Error`	output	active high signal indicating an error condition on the chip
205	`SerLoad`	input	active high load signal for serial line interface
204	`notTrigIn`	LVDS-input	active low readout trigger input
203	`TrigIn`	LVDS-input	active high readout trigger input
202	n. c.	n.c.	Not connected
201	`notRclk`	LVDS-input	active low readout clock for data multiplexer
200	`Rclk`	LVDS-input	active high readout clock for data multiplexer
199	`notSclk`	LVDS-input	active low sampling clock; the rising edge signals the sampling point of time
198	`Sclk`	LVDS-input	active high sampling clock; the falling edge signals the sampling point of time

Table 15: Pads on the rear side of Helix128-2.2/2.3. The first pad in the table corresponds to the uppermost pad of the chip's rear side (with the frontside left).

5.4 Top side pads

A pad description for Helix128-2.0 and Helix128-2.1 is given in table 16 on page 42, the description for Helix128-2.2 in table 17 on page 43.

The top side pads of Helix128-3.0 are described in table 18 on page 44.

5.5 Core pads

Some pads have been located in the chip's core. Most of them are for diagnostic purposes, but on Helix128-2.x pad no. 267 `SufixTokenOut` and no. 268 `HelixTokenIn` play an important role in the daisy chain token scheme; in Helix128-2.2/2.3 `SufixTokenOut` can also be obtained from the top side (pad no. 246). The pads for Helix128-2.0 and Helix128-2.1 are explained in table 19 on page 45, the pads for Helix128-2.2/2.3 in table 20 on page 46.

Ref. no.	Pin name	Type	Description
266,265	`Gnda`	supply	analog ground (0V)
264,263	`Vssa`	supply	negative analog supply voltage (−2V)
262,261	`Vdda`	supply	positive analog supply voltage (+2V)
260	`TestOut`	output	test channel preamplifier output
259	`HelixTokenOut`	output	token output; must be bonded to pad no. 256 `ReturnTokenIn` if the chip is the last in the daisy chain and for single chip operation (otherwise bonded to pad no. 179 `HelixTokenIn` of following chip in the daisy chain)
258	`ReturnTokenIn`	input	return path token input; must be bonded to pad no. 257 `HelixTokenOut` if the chip is the last in the daisy chain and for single chip operation (otherwise bonded to pad no. 180 `ReturnTokenOut` of following chip in the daisy chain)
257	`SyncOut`⟨0⟩	output	synchronicity monitoring output to neighbouring Helix128-2.0/2.1
256	`SyncOut`⟨1⟩	output	"
255-253	⋮	⋮	⋮
252	`SyncOut`⟨5⟩	output	"
251	`SufixBus`⟨7⟩	test outp.	bias generator data bus; used for verification of correct internal operation; no connection needed for normal operation
250	`SufixBus`⟨6⟩	test outp.	"
249-245	⋮	⋮	⋮
244	`SufixBus`⟨0⟩	test outp.	"
243	`notSel`⟨6⟩	test outp.	select bus in bias generator; strobes access to the *Idriver* DAC; used for verification of correct internal operation; no connection needed for normal operation
242	`notSel`⟨5⟩	test outp.	select bus in bias generator; strobes access to the *Isf* DAC; used for verification of correct internal operation; no connection needed for normal operation
241	`notSel`⟨4⟩	test outp.	select bus in bias generator; strobes access to the *Ipipe* DAC; used for verification of correct internal operation; no connection needed for normal operation

Table 16: Pads on the top side of Helix128-2.0/2.1. The first pad in the table corresponds to the uppermost pad of the chip's top side (with the frontside left).

Ref. no.	Pin name	Type	Description
266,265	`Gnda`	supply	analog ground (0V)
264,263	`Vssa`	supply	negative analog supply voltage (−2V)
262,261	`Vdda`	supply	positive analog supply voltage (+2V)
260	`TestOut`	output	test channel preamplifier output
259c	`GndComp`	supply	Reference voltage for comparators' AC coupling (0V)
259b	`VssComp`	supply	Comparators' most negative supply (-2V)
259a	`VddComp`	supply	Comparators' most positive supply (+2V)
259	`notHelixTokenIn`	input	Reserved for future use
258	`notReturnTokenOut`	output	Reserved for future use
257a	`ReturnTokenOut`	output	to be connected to pad no. 180a `ReturnTokenIn` of predecessing Helix128-2.2/2.3 if the chip is nonleading in a daisy chain (not to be connected for single chip operation and if the chip is the first in a daisy chain)
257	`SyncOut`⟨0⟩	output	synchronicity monitoring output to neighbouring Helix128-2.2./2.3
256	`SyncOut`⟨1⟩	output	"
255-253	⋮	⋮	⋮
252	`SyncOut`⟨5⟩	output	"
251	`HelixTokenIn`	input	to be connected to pad no. 187 `HelixTokenOut` of predecessing Helix128-2.2/2.3 if the chip is nonleading in a daisy chain (not to be connected for single chip operation and if the chip is the first in a daisy chain)
250	`notFailsafeReturnTokenOut`	output	Reserved for future use.
249	`FailsafeReturnTokenOut`	output	Reserved for future use.
248	`FailsafeHelixTokenIn`	input	Reserved for future use.
247	`FailsafeHelixTokenOut`	output	Reserved for future use.
246	`SufixTokenOut`	output	Output of token generator (see pad no. 267)
245-240a	n. c.		Removed

Table 17: Pads on the top side of Helix128-2.2/2.3. The first pad in the table corresponds to the uppermost pad of the chip's top side (with the frontside left).

Ref. no.	Pin name	Type	Description
266,265	`Gnda`	supply	analog ground (0V)
264,263	`Vssa`	supply	negative analog supply voltage (−2V)
262,261	`Vdda`	supply	positive analog supply voltage (+2V)
260	`TestOut`	output	test channel preamplifier output
259c	`GndComp`	supply	Reference voltage for comparators' AC coupling (0V)
259b	`VssComp`	supply	Comparators' most negative supply (-2V)
259a	`VddComp`	supply	Comparators' most positive supply (+2V)
259	n. c.	n. c.	Reserved for future use
258	`notReturnTokenOut`	output	Reserved for future use
257a	`ReturnTokenOut`	output	to be connected to pad no. 180a `ReturnTokenIn` of predecessing Helix128-2.2/2.3 if the chip is nonleading in a daisy chain (not to be connected for single chip operation and if the chip is the first in a daisy chain)
257	`SyncOut`⟨0⟩	output	synchronicity monitoring output to neighbouring Helix128-2.2./2.3
256	`SyncOut`⟨1⟩	output	"
255-253	⋮	⋮	⋮
252	`SyncOut`⟨5⟩	output	"
251	`HelixTokenIn`	input	to be connected to pad no. 187 `HelixTokenOut` of predecessing Helix128-2.2/2.3 if the chip is nonleading in a daisy chain (not to be connected for single chip operation and if the chip is the first in a daisy chain)
250	n. c.	n. c.	Reserved for future use
249	`FailsafeReturnTokenOut`	output	To be connected to `FailsafeReturn-TokenIn` of the 2^{nd} previous chip.
248	`FailsafeHelixTokenIn`	input	To be connected to `FailsafeHelixToken-Out` of the 2^{nd} previous chip.
247	`FailsafeHelixTokenOut`	output	To be connected to `FailsafeHelixToken-In` of the 2^{nd} previous chip.
246	n. c.	n. c.	Reserved for future use
245-240a		n. c.	Removed

Table 18: Pads on the top side of Helix128-3.0. The first pad in the table corresponds to the uppermost pad of the chip's top side (with the frontside left).

Ref. no.	Pin name	Type	Description
267	`SufixTokenOut`	output	initial token out of first chip in daisy chain; to be bonded to pad no. 268 `HelixTokenIn` for the first chip in a daisy chain and for single chip operation (otherwise not to be connected)
268	`HelixTokenIn`	input	internally connected to the adjacent pad no. 182; to be bonded to pad no. 267 `SufixTokenOut` for the first chip in a daisy chain and for single chip operation (otherwise not to be connected)
269	`TrigMon`	test outp.	test pad to probe the `TrigMon` signal (no connection needed for normal operation)
270	`WriteMon`	test outp.	`WriteMon` signal
271	`Trigger`	test outp.	`Trigger` signal
272	`notTrigger`	test outp.	`notTrigger` signal
273	`notReset`	test outp.	`notReset` signal
274	`notTReset`	test outp.	`notTReset` signal
275	`Voffset`	test outp.	buffer *Voffset* voltage
276	`Vdcl`	test outp.	pipeamp *Vdcl* voltage
277	`Vd`	test outp.	pipeamp *Vd* voltage
278	`VcompRef`	test outp.	comparator *VcompRef* voltage
279	`Vfs`	test outp.	shaper *Vfs* voltage
280	`Vfp`	test outp.	preamplifier *Vfp* voltage

Table 19: Description of the Helix128-2.0 and Helix128-2.1 core pads. The first pad in the table corresponds to the lowest right hand side core pad (with the frontside left).

Ref. no.	Pin name	Type	Description
267	`SufixTokenOut`	output	initial token out of first chip in daisy chain; to be bonded to pad no. 268 `HelixTokenIn` for the first chip in a daisy chain and for single chip operation (otherwise not to be connected)
268	`HelixTokenIn`	input	internally connected to the adjacent pad no. 182; to be bonded to pad no. 267 `SufixTokenOut` for the first chip in a daisy chain and for single chip operation (otherwise not to be connected)
269	`TrigMon`	test outp.	test pad to probe the `TrigMon` signal (no connection needed for normal operation)
270	`WriteMon`	test outp.	`WriteMon` signal
271	`Trigger`	test outp.	`Trigger` signal
272	`notTrigger`	test outp.	`notTrigger` signal
273	`notReset`	test outp.	`notReset` signal
274	`notTReset`	test outp.	`notTReset` signal
275	`Voffset`	test outp.	buffer *Voffset* voltage
276	`Vdcl`	test outp.	pipeamp *Vdcl* voltage
277	`Vd`	test outp.	pipeamp *Vd* voltage
278	`VcompRef`	test outp.	comparator *VcompRef* voltage
279	`Vfs`	test outp.	shaper *Vfs* voltage
280	`Vfp`	test outp.	preamplifier *Vfp* voltage

Table 20: Description of the Helix128-2.2/2.3 core pads. The first pad in the table corresponds to the lowest right hand side core pad (with the frontside left).

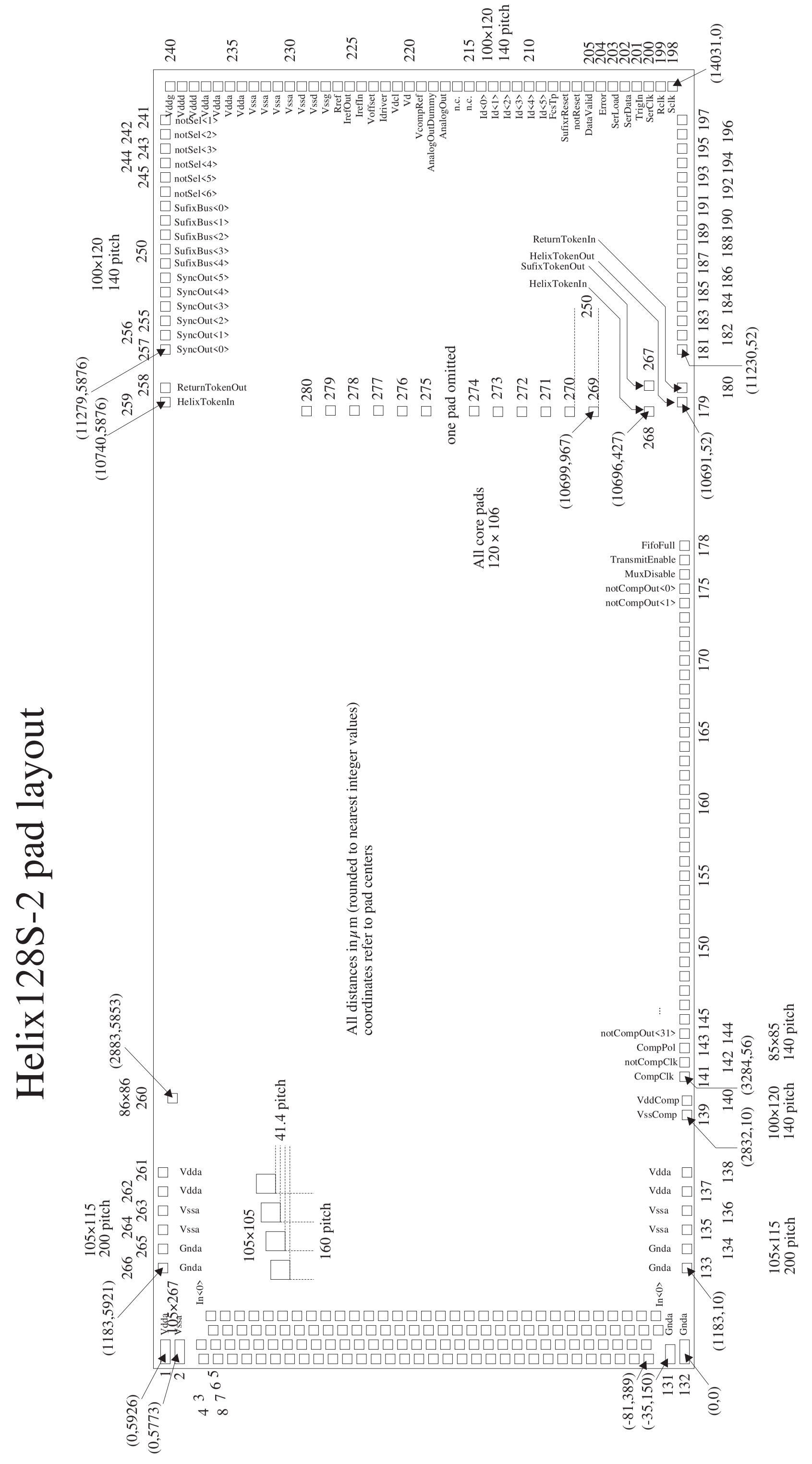

Figure 18: Schematic drawing of the Helix128-2.0 pad locations. The overall chip dimension is 14,385μm x 6,146 μm; the frontside (facing the detector) is the bottom side in this view; in the descriptions we will refer to this side as the left side in regard of the “normal” signal flow from left to right

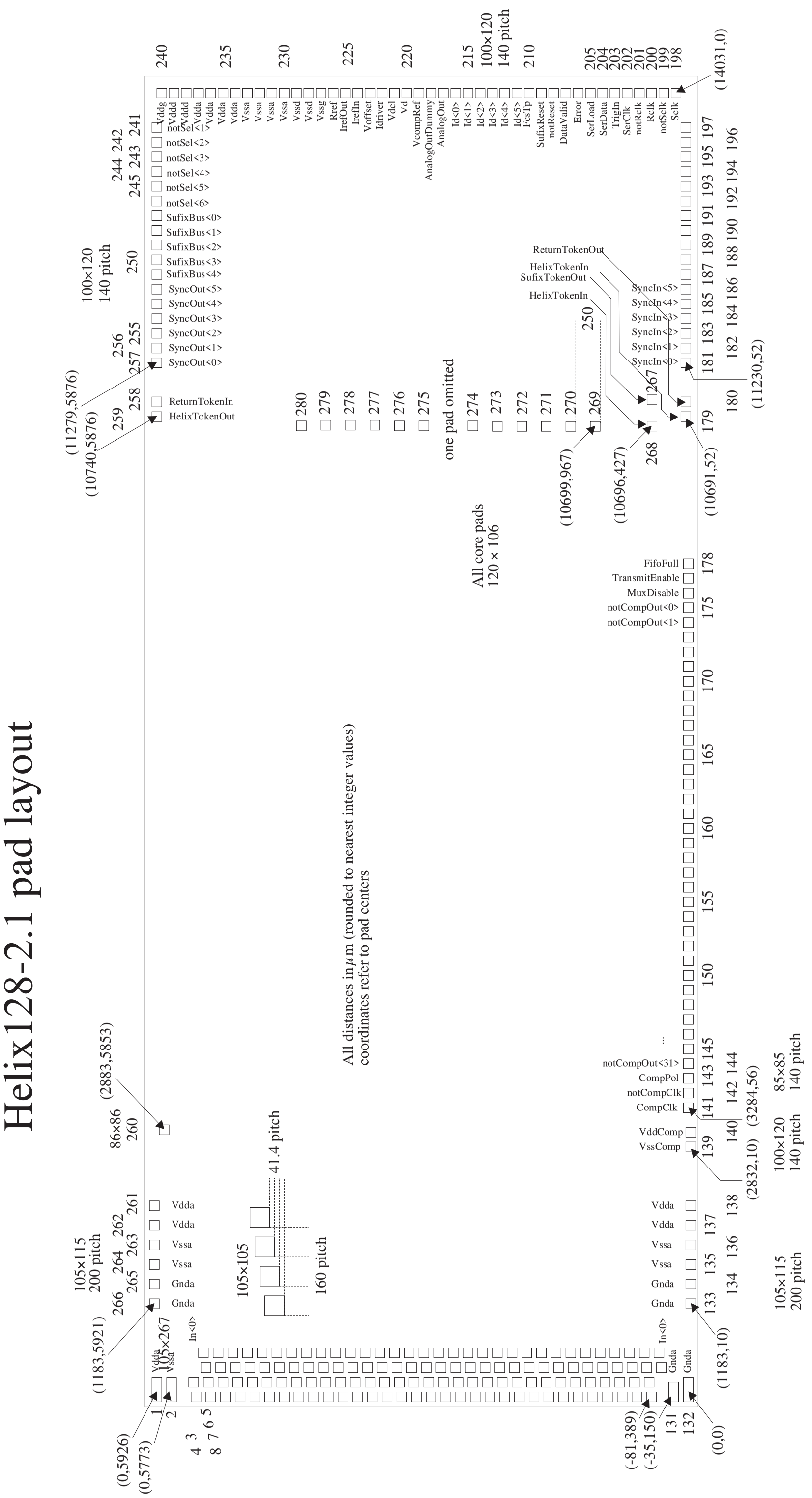

Figure 19: Schematic drawing of the Helix128-2.1 pad locations. The `Sclk` and `Rclk` pads are now differential CMOS inputs.

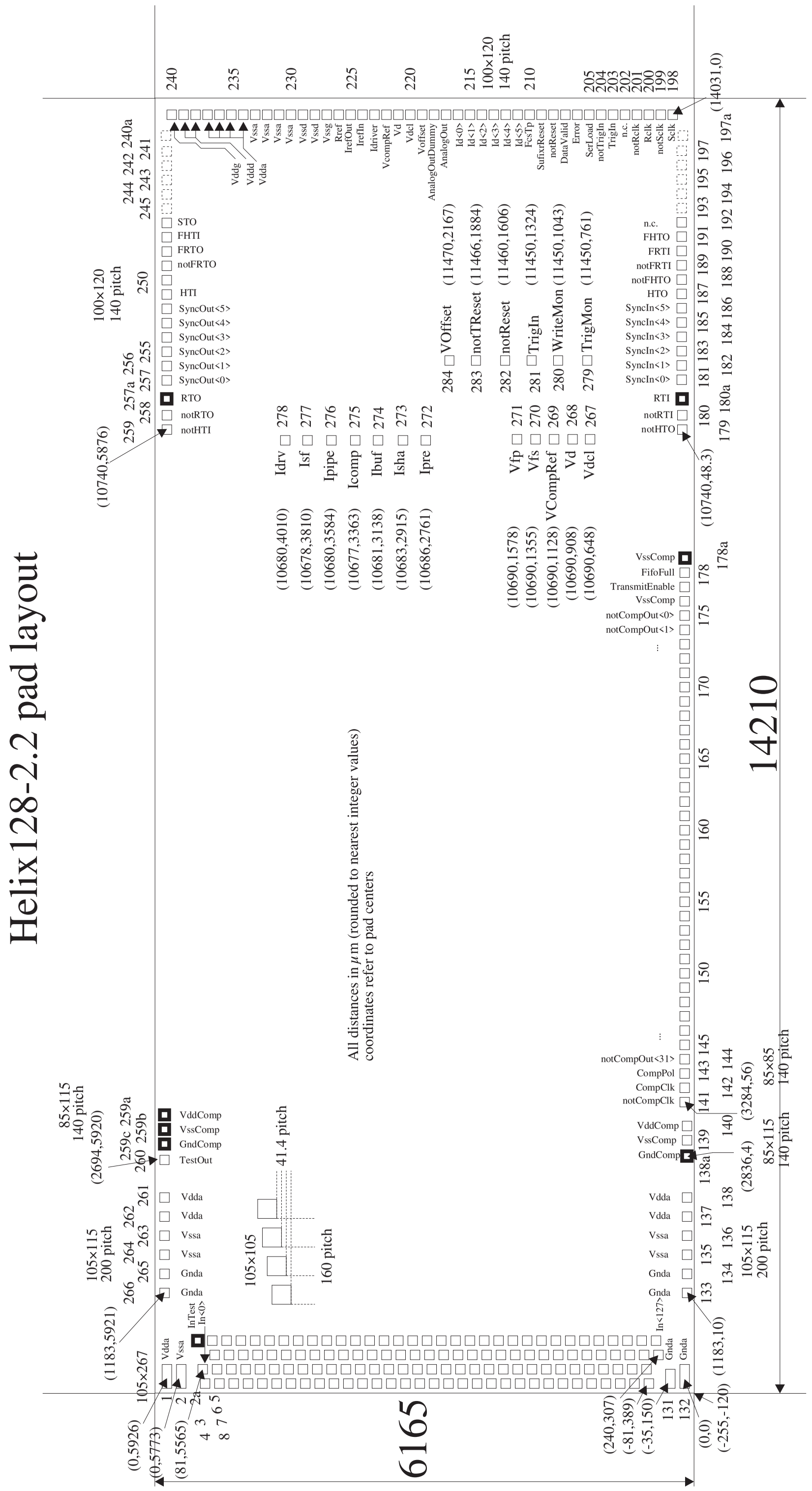

Figure 20: Schematic drawing of the Helix128-2.2/2.3 pad locations. Token pads and power supply pads for the comparator outputs have been added.

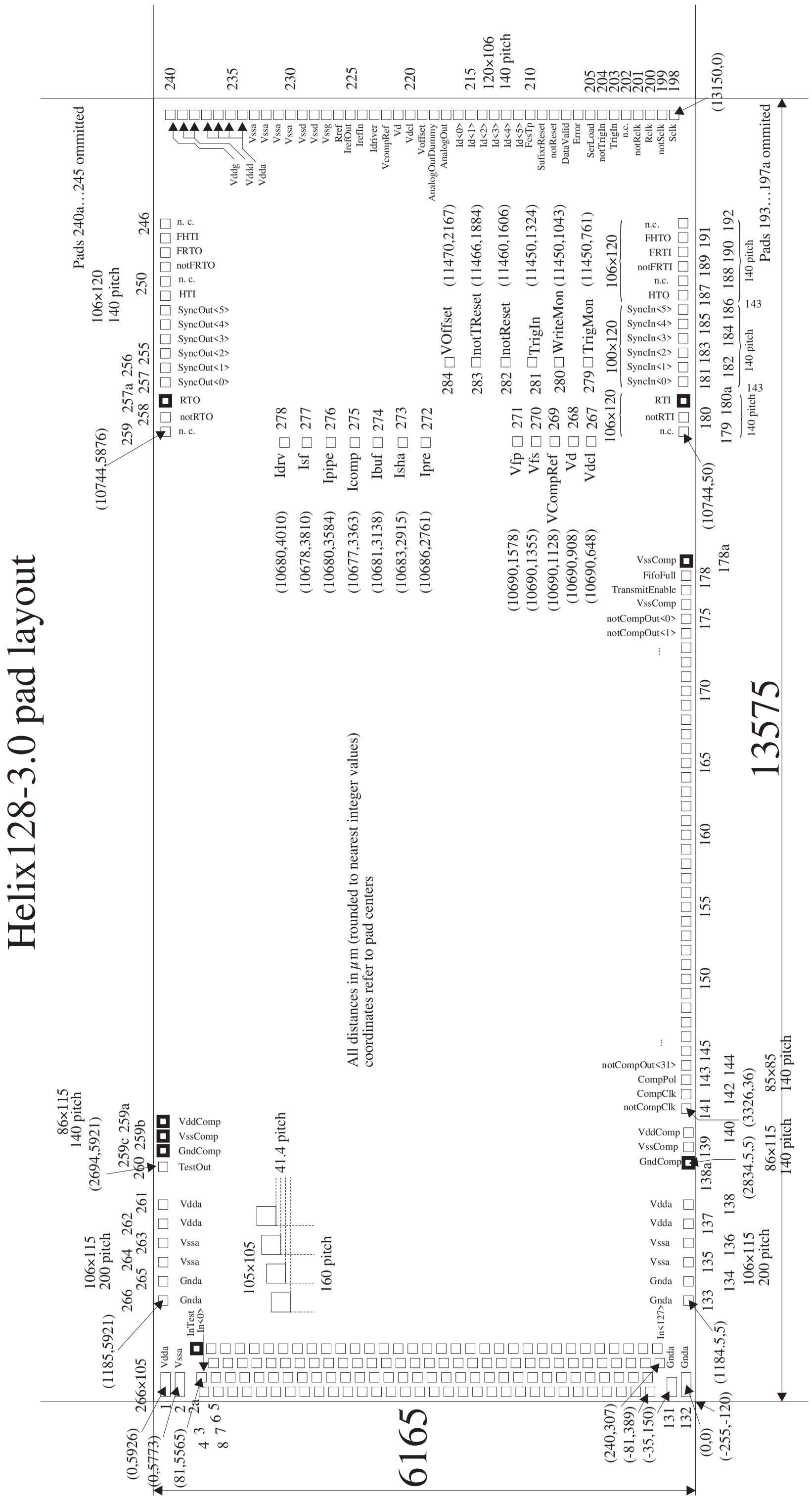

Figure 21: Schematic drawing of the Helix128-3.0 pad locations.

6 Appendix: List of Known Problems

1. Multi-event buffer non functional (1);
   due to unfavorable routing of `Sclk` the chip has to be reset after each trigger. The employment of Helix128-2.0 should be restricted to laboratory evaluation.

2. Multi-event buffer (2);
   at certain well defined conditions a trigger can halt the chip.

3. *VcompRef* adjustment;
   VcompRef is the dicriminator reference voltage of the comparators. It runs from -2V to +2V in 128 steps, giving a resolution of $\approx$ 31mV. Compared to the response to a signal of 1MIP_{Si} (24.000 electrons) of $\approx$ 50mV, this is much to coarse.

4. `Sclk` and `Rclk`;
   `Sclk` and `Rclk` are unipolar (nondifferential) signals which may cause excess noise on the chip, especially at fast `Rclk` timings.

5. `SerClk` and `Rclk`;
   `Rclk` must run faster than `SerClk` otherwise data might be lost.

6. `DataValid`, `AnalogOut` and `AnalogOutDummy`;
   `AnalogOut` and `AnalogOutDummy` jitter with respect to `DataValid`. The jitter can be up to 4 `Rclk` cycles, but is the same for all chip that have their `notReset` released at the same time.

7. Offset of `AnalogOut` and `AnalogOutDummy`;
   due to unfavorable voltage level transitions in the pipeline readout amplifier, `AnalogOut` and `AnalogOutDummy` have a `Sclk`-dependent offset, which limits the dynamic range.

8. Crosstalk of switching comparator to all channels;
   feedback via the open-collector discriminator outputs at the chip's bottom side to the amplifier inputs is suspected.

9. Pairwise crosstalk between channels (2n,2n+1) of approx. 8 %;
   even if the pattern follows an asymmetry in the pipeline, the origin is not yet clear.

10. Radiation softness of Pipeline amplifier; The functionality of the Pipeamp suffers from very low radiation doeses. It is believed that this problem is related with problem 7.

11. Light sensitivity of the pipeline amplfier; The pipeline read ot amplifier suffers from extreme light sensitivity. Exposure to light drives the amplifier into saturation when the chip is not read out and the reset period before each read out cycle is not long enough to recover the amplifier from this state. This problem mainly occurs at low trigger rates (less than 100Hz). Higher trigger rates keep the amplifier operable.

12. Startup of the internal bias current source; Some chips do not become operation because the internal current source does not start.

13. Oscillation of the internal current source; The internal current source shows oscillation, which increases common mode noise and limits the comparator threshold. The nearly sine-shaped oscillation of approx. 10MHz can be eliminated completely at most chips by blocking the reference resistor connected to the `Rref` pad. However, then some chips still show a saw-tooth like oscillation of some 100kHz.

6.1 Solved problems at Helix128-2.1

Problems 1, 3, 4 have been solved

6.2 Solved problems at Helix128-2.2

Problems 6, 7 have been solved; problem 8 has been improved; problem 10 is currently under investigation

6.3 Solved problems at Helix128-3.0

Problem 2, 8, 10, 11 and 12 have been solved. Problem 13 is currently under study.

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