The Helix128 trigger functionality and problems related to its use at the HERA-B Inner Tracker MSGC system

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1 Abstract

The Helix128 is an analogue pipeline chip used for reading out the HERA-B Silicon Vertex Detector and the Inner Tracker, a Microstrip Gaseous Chamber system. Besides using the analogue pipeline functionality for tracking, a unique feature of the chip, a separate binary data path which outputs the discriminated frontend's shaper output, is used at the Inner Tracker to provide information for the HERA-B First Level Trigger.

Tests of the complete chamber - electronics system revealed a very unsatisfactory behaviour: if the comparator threshold is set too low, the whole system starts oscillating, preventing a sufficient trigger efficiency and disturbing the analogue readout functionality.

This paper describes the relevant parts of the MSGC readout electronics and the measurements and design changes which were performed up to now to get satisfactory results. It is the starting point for a review to be done.

2 Helix128

In general, documentation of the Helix128 chip is available via WWW at the following URL:

`http://wwwasic.ihep.uni-heidelberg.de/~feuersta/projects/Helix/index.html`

Specific documentation cited in the text can sometimes also be accessed via WWW. In this case the URL is given in the References.

2.1 Overall structure of the chip

Helix128 contains 128 channels (fig. 1), each consisting of

- a low noise charge sensitive preamplifier for signals of both polarities.
- a CR-RC shaper forming a semigaussian pulse with a peak time of 50... 70ns.
- a buffer amplifier driving the internal pipeline write line and the pipeline cell.
- a comparator circuit indicating hit channels, the output of four neighbouring channels being ORed and brought offchip via open drain outputs.
- an analogue pipeline consisting of 128+8+5 capacitors resulting in a maximum latency of 128 events and a multievent buffer capable of storing up to eight triggered events (time slots)
- a switched charge sensitive pipeline readout amplifier.

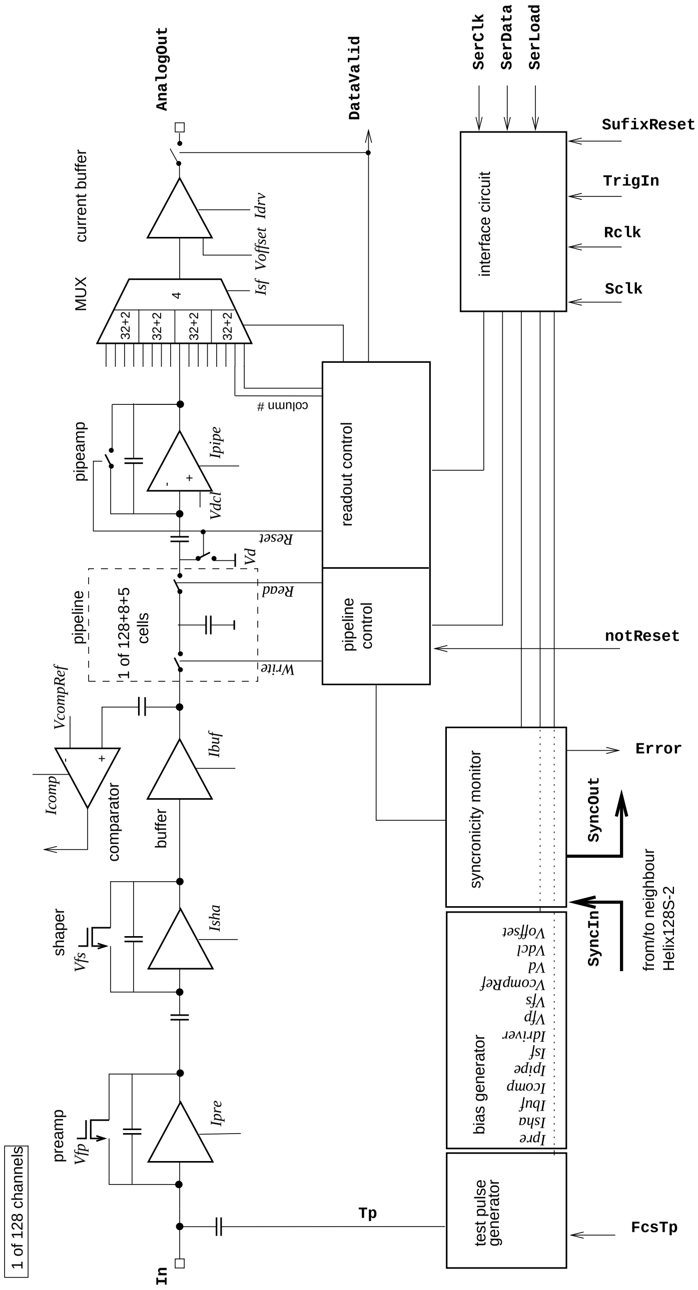

Figure 1: Helix128 block diagram

A cascaded 128+8+1 channel multiplexer and a current output buffer are provided for the fast serial readout of the analogue data and the 8 bit pipeline

Table 1: Helix128 power supply

Name	Value	Description
`Gnd`	0V	Detector ground, reference potential for preamplifier
`Vssa`	-2V	Analogue VSS
`Vdda`	+2V	Analogue VDD
`Vssd`	-2V	Digital VSS
`Vddd`	+2V	Digital VDD
`VssComp`	-2V	Comparator VSS
`VddComp`	+2V	Comparator VDD
`VssCompOut`	-2V	Comparator output driver VSS

column number.

2.2 Helix128 version history

Helix128-2.2 was the first chip to be used at HERA-B in larger scale. From this the Helix128-3.0 was derived, which solved several problems, besides improving the performance of the trigger.

2.3 Power supply

The Helix128 is operated between VDD=+2V and VSS=-2V. Detector ground `Gnd`=0V is the reference potential for the preamplifier.

The chip has separate power supply for analogue and digital parts (table 1).

The positive power supply for the open drain comparator output drivers is connected internally to `Vddd`, since no large current supply is needed.

2.4 The frontend

Helix128 uses the Helix2.1 frontend (fig. 2) which has been carefully optimized with respect to noise, pulse shape (peak time and undershoot), linearity, space and power consumption.

It is implemented as a folded cascode amplifier circuit with a 342 fF feedback capacitor yielding a gain of 11.2 mV/$\mathrm{MIP_{Si}}$ (1 $\mathrm{MIP_{Si}}$=24000 electrons). The peaking time is adjustable via the bias currents in the range of 45ns...70ns.

The total gain of the preamplifier/shaper and output buffer (as seen by the pipeline and the comparator) is about 40mV/MIP_{Si}.

The ENC was measured to be better than 395.7e + 39.4e/pF.

More detailed descriptions can be found in [1], [2] and [3].

2.5 The comparator

The comparator (fig. 3) with programmable signal polarity is located behind the frontend to detect hit channels [4]. To suppress frontend pedestal fluctuations the comparator has been AC-coupled with a large time constant. The

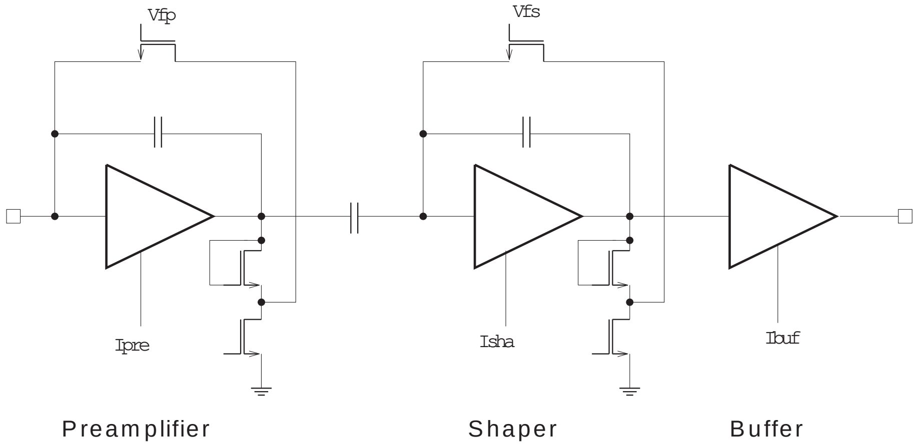

Figure 2: Helix2.1 frontend

output of four neighbouring channels is ORed (after passing an EXOR gate to switch polarity of the signal), latched on the positive edge of **`CompClk`** and brought offchip as open drain signals `notCompOut`⟨`31...0`⟩ which can drive 4mA at maximum [1].

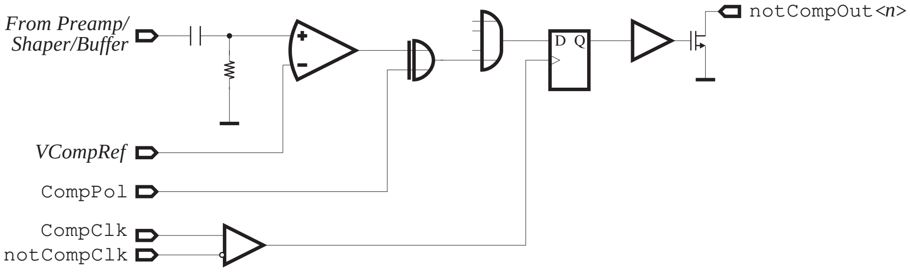

Figure 3: AC-coupled comparator

The comparator circuit itself (fig. 4) is a standard differential stage with cross-coupled pair input transistors followed by an inverter as high gain amplifier. The input transistors have been optimized to an expected offset variation of about ±4mV, which is in the same order as the noise from the preamp. The rise time of the comparator is 30ns, faster than the preamp/shaper.

[1] This enables logically "OR"ing several comparator outputs by connecting them to a common drain resistor.

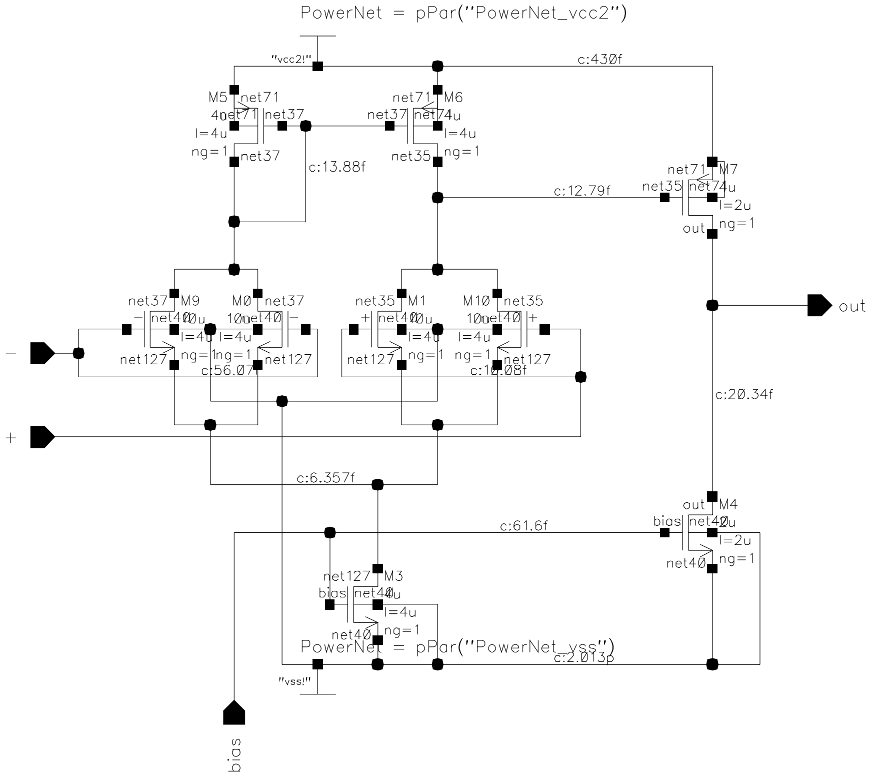

Figure 4: Comparator circuitry

The AC-coupling (fig. 5) is realized with a poly-poly capacitor of 2pF and an NMOS and a PMOS transistor as high ohmic resistors to ground. The time constant of this configuration larger than 4.8μs.

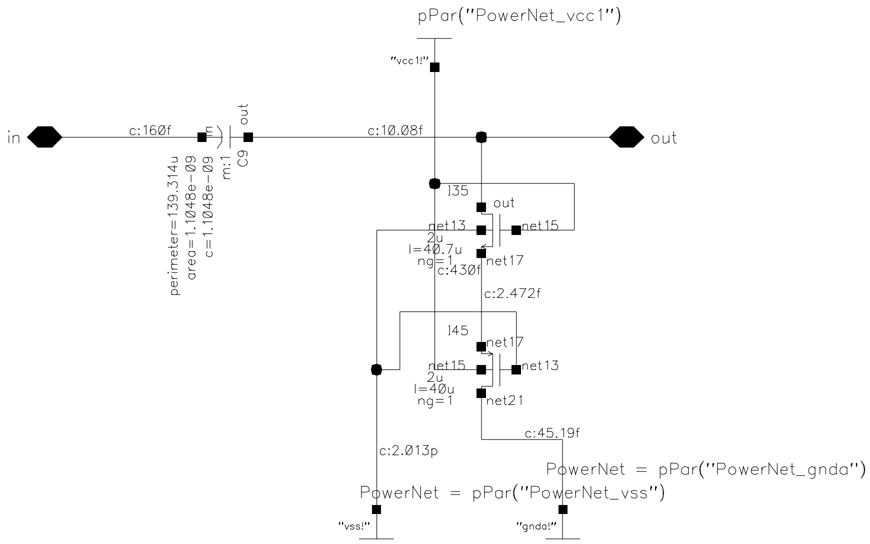

Figure 5: AC-coupling

The layout of the comparator (fig. 6) is enclosed by a guardring connected to `VssComp`. The clock for all 128 / 4 = 32 flip-flops is routed differentially to compensate for clock feedthrough via the substrate, though only one polarity is actually connected.

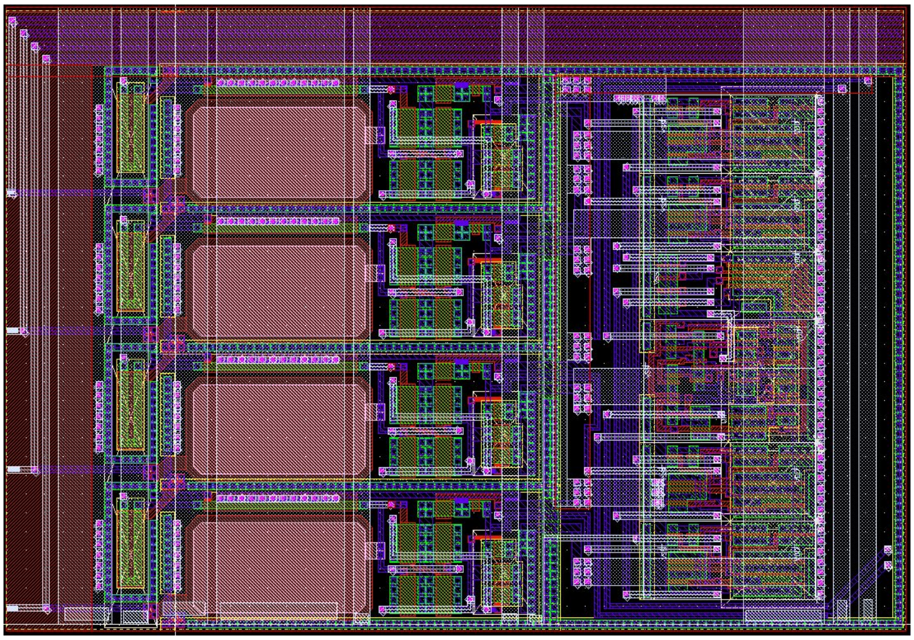

Figure 6: Layout of four comparators which are combined to a single channel

The analogue signals had to be routed through the comparator layout block but are shielded against substrate coupling with a layer of polysilicon connected to the guardring.

The flip-flop's output is send differentially to the bottom side of the chip, where the output drivers are located. Since it must cross the shaper's output to the pipeline, care has been taken to have equal overlap between the output of the comparators and the analogue lines for both polarities of the signal.

2.6 The comparator output driver

The comparator output drivers are standard AMS open drain drivers with 4mA maximum current. This high current was necessary to safely discharge the parasitic capacitance of the PCB lines and plugs of about 20pF within 100ns.

The return current of the output driver is drained via separate pads and the scribe line surrounding the whole chip (which is connected to `Vssa`) is opened left and right to the row of output pads and put to a separate VSS. This change was introduced in the move from the Helix128-2.2 to the Helix128-3.0 and improved the performance a lot (though it is still not sufficient).

3 The chamber electronics

The chamber is a Micro-Strip-Gaseous Chamber with a Gas Electron Multiplier foile as a preamplifier stage (MSGC-GEM). The whole chamber is mounted on a 300μm thick glas of about 25cm $\times$ 25cm. The anodes are DC-coupled to the Helix chip via z-axis glued capton pitch adapters and a ceramic thinfilm hybrid which serves as a further pitch adapter and integrates HV spark protection resistors of 600Ω value. The anode capacitance is about 30pF. The expected noise for this configuration is 4000 electrons, to be compared to a signal between 25000-40000 electrons, depending on the gas amplification. Noise was calculated from data (random triggers on electronics attached to an MSGC) to be 8400 electrons without common mode noise suppression and 5500 electrons with common mode noise suppression.

In trigger layers, two MSGC-GEM chambers of same stereo angle are mounted on opposite sides of a carbon fibre (CFK) support layer. The bottom side MSGC-GEM is read out via an AS7 type Helix-PCB, whereas the top side chamber is read out via an AS8 type Helix-PCB.

Power supply, control signals (`Sclk`, `Rclk`, `TrigIn`, `notReset`, `SerLoad`) and analogue outputs are routed via the AS7 board to a signal distribution board, which is plugged on the backside of the AS7. The AS8 is connected to the AS7 and gets all these signals via the AS7 to the signal distribution board AS15 (fig. 7).

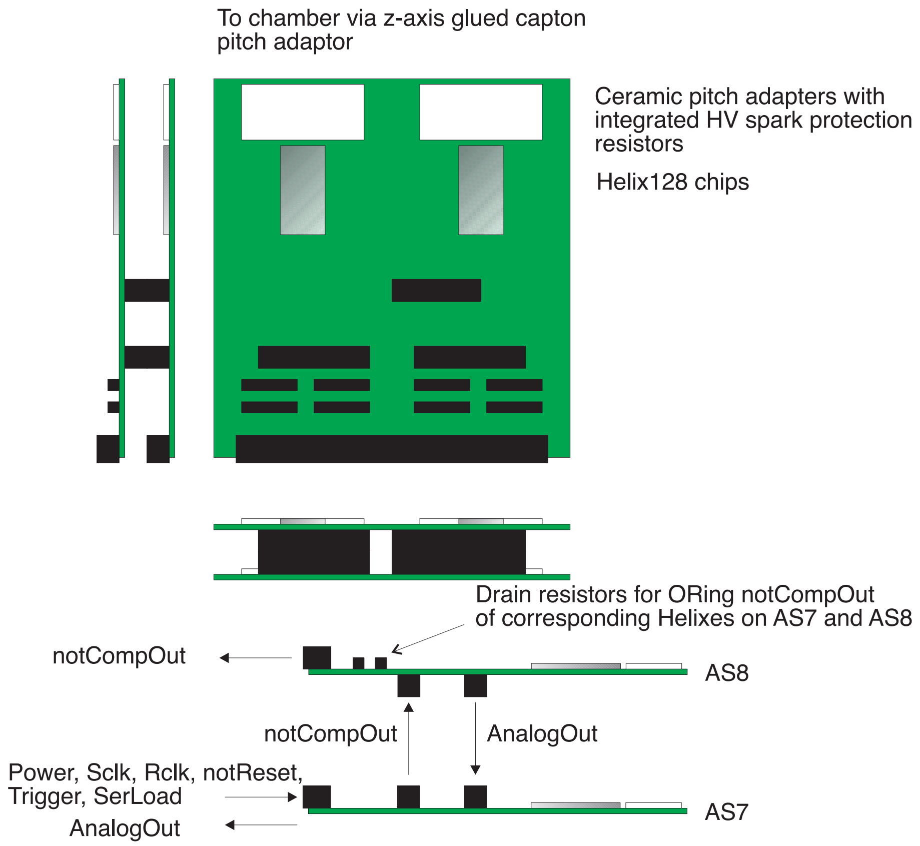

Figure 7: Principle arrangement of AS7 ans AS8 Helix-PCBs

The comparator outputs of both boards are collected on the AS8 board (the AS7 signals are put to the AS8 via another intermediate plug). The corresponding outputs of the Helix chips on the AS7 and AS8 are connected and share a common drain resistor. Thus a logic OR of corresponding anode strip groups on both chambers is performed.

The combined comparator signals of both the AS7 and the AS8 board are connected to the trigger driver board, which multiplexes them by a factor of 4 and sends them to the off-detector electronics.

3.1 The Helix PCB

The Helix-PCBs AS7 and AS8 were produced in two versions differing mainly in the power supply concept (fig. 8, 9):

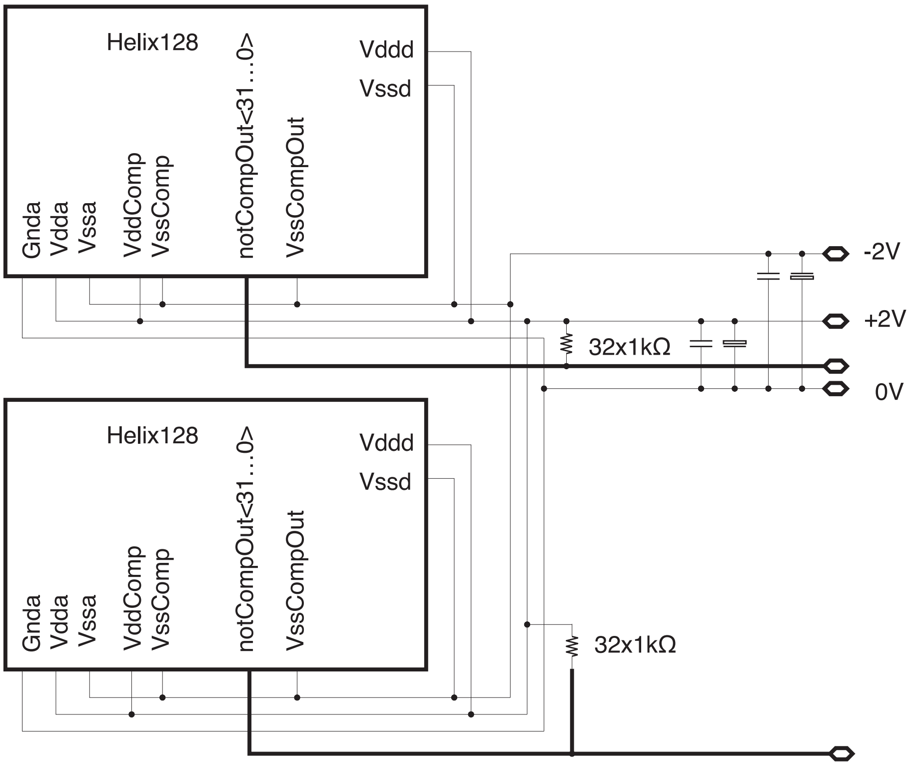

Figure 8: Power distribution of AS7-1 and AS8-1 Helix-PCBs

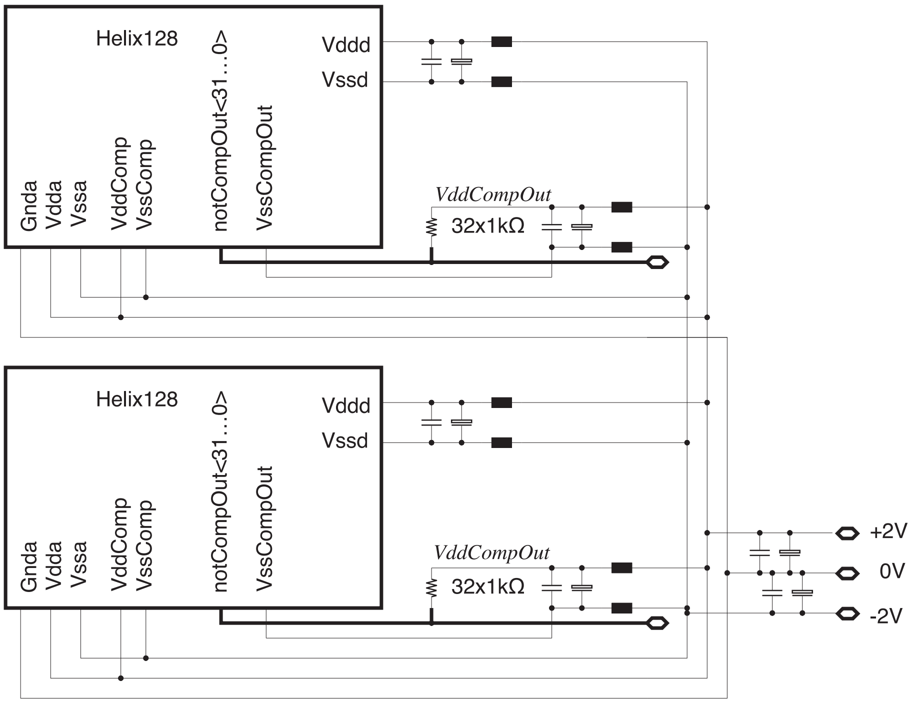

Figure 9: Power distribution of AS7-2 and AS8-2 Helix-PCBs

- AS7-1 and AS8-1 have separate planes for +2V and -2V (fig. 11) and the ground (0V) plane (fig. 10) is on one signal layer, the ground area well separated from any other layer on this plane. The +2V layer and the -2V layer are used to directly contact the several power supplies of the Helix chips. All blocking is done against the 0V layer.

- AS7-2 and AS8-2 have separate planes for +2V (fig. 16) and -2V (fig. 15) in which there is also a separation between `Vdda` and `Vddd`, separate for each chip. Both `Vddd` and `Vssd` are derived on the PCB from `Vdda` and `Vssa`, respectively, via inductive coupling of 0.68μH. Ground (0V) is now on a separate plane (fig. 14) and the plane is sparsified where it overlaps with the (potentially) noisy `Vddd` planes. `VssCompOut`, the return current from the output drivers, is also on a separate plane, layouted such that the current flows along the same path in opposite direction to the `notCompOut` lines to cancel any magnetic fields caused by the currents of $32 \times 4\text{mA} = 128\text{mA}$ maximum (fig. 12, 13). It is individual for each Helix chip, also. Blocking of `Vssa` and `Vdda` is against `Gnd`, whereas `Vssd` and `Vddd` are directly blocked without touching ground (because no current should flow from the digital part into `Gnd`, which is purely analogue). Blocking between `VssCompOut` and the positive supply of the drain resistors (which could be denominated as *VddCompOut*) is also direct, thus the large currents flowing in this path should not disturb the rest of the PCB.

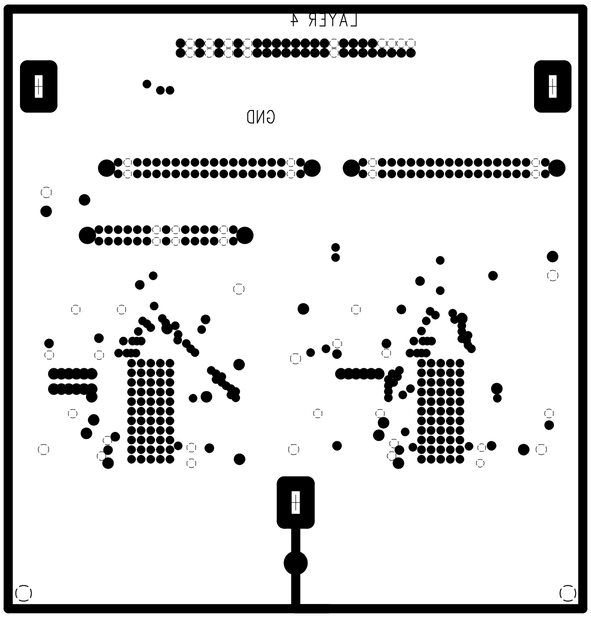

Figure 10: Layout AS7-1, Ground plane (negative plot)

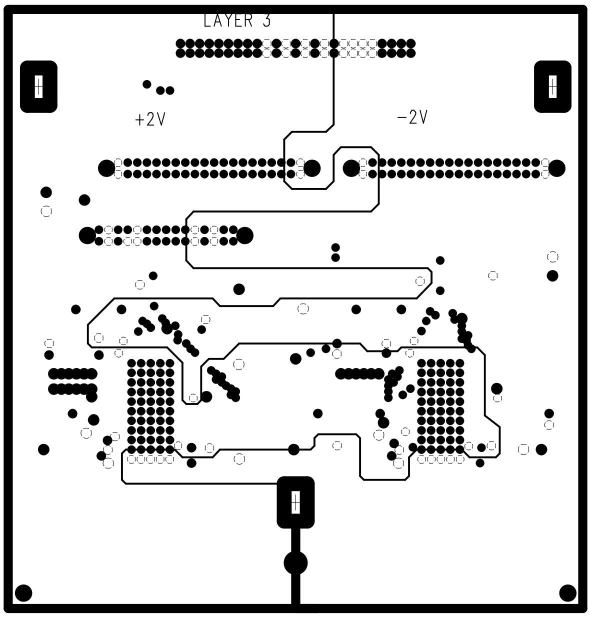

Figure 11: Layout AS7-1, +2V/-2V plane (negative plot)

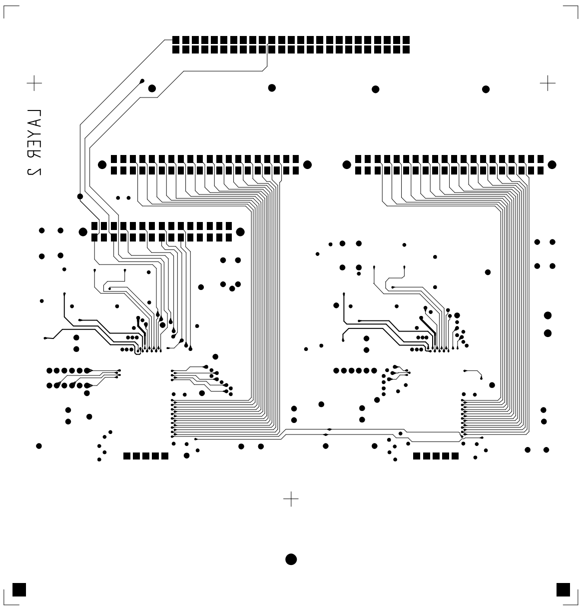

Figure 12: Layout AS7-2, Layout of `notCompOut`¿31. . . 0¿ signals

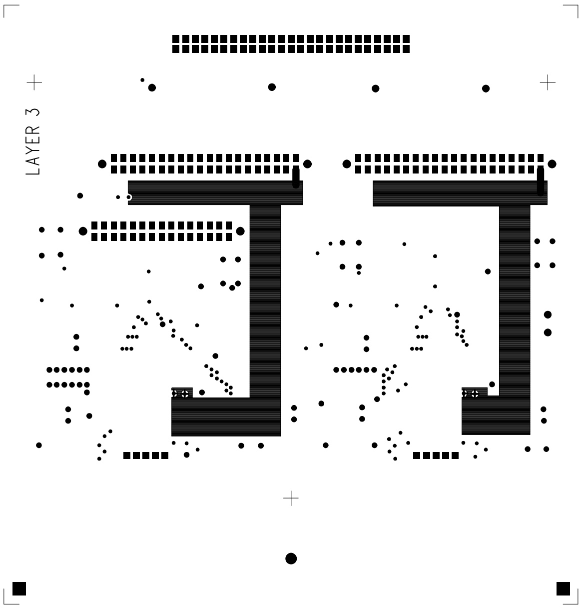

Figure 13: Layout AS7-2, `VssCompOut`, return current for `notCompOut`¡32…0¿ signals

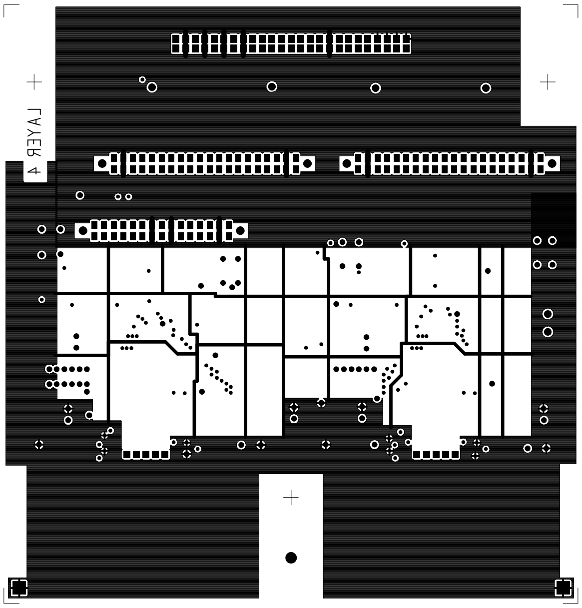

Figure 14: Layout AS7-2, Ground plane

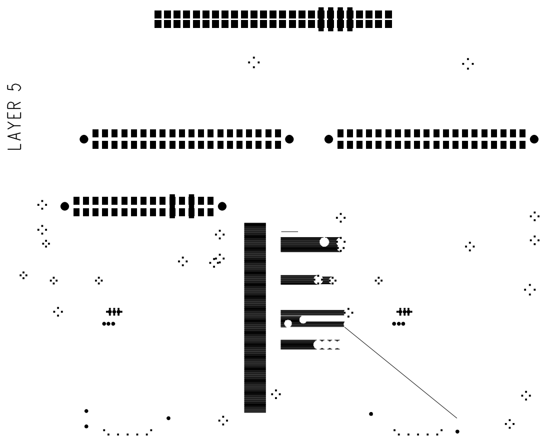

Figure 15: Layout AS7-2, -2V plane (negative plot)

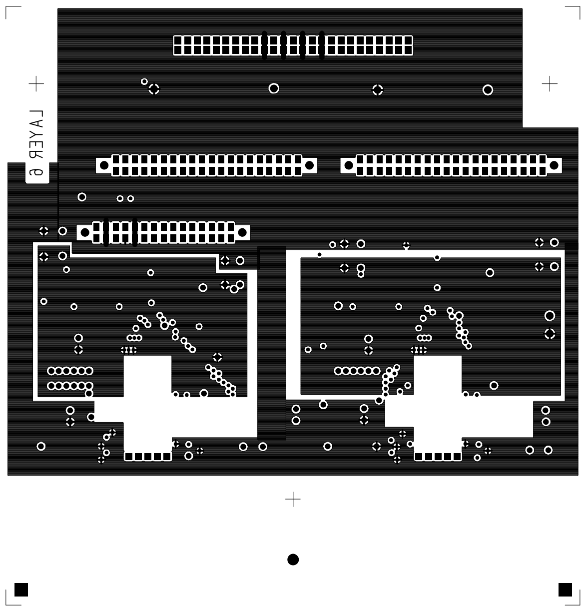

Figure 16: Layout AS7-2, `Vdda` and `Vddd` (+2V) plane

In general, blocking is done in the usual way with larger Tantal capacitors accompanied by ceramics.

3.2 The signal distribution board AS15

The signal distribution board AS15 is responsible for distributing power and control signals from a cable tree running by the side of the detectors to the three Helix-PCBs that read out one MSGC module. It is connected to the backside of AS7 type boards (fig. 17).

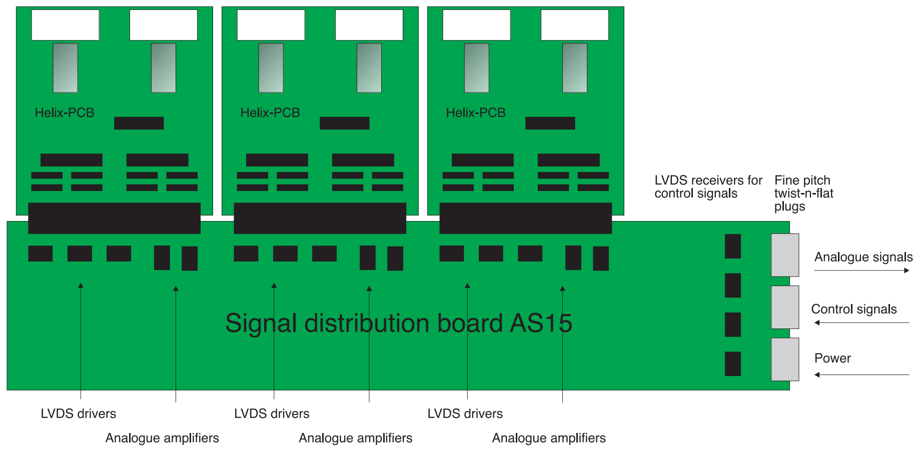

Figure 17: Signal distribution board AS15 connecting three Helix-PCBs type AS7-1 or AS7-2

Control signals (`Sclk`, `Rclk`, `notReset`, `TrigIn`, `SerLoad`) are LVDS signals on fine pitch twisted pair flat ribbon cables. The signal distribution board receives them via DS90C032 differential line receivers and translates them to CMOS 5V signals (all digital electronics on the signal distribution boards operates between -2V and +3V). The signals are routed between two ground/power supply layers to minimize noise.

Just in front of the connector to each Helix PCB the CMOS level signals are converted back to LVDS signals via DS90C031 differential line drivers.

Hence no active components are needed on the Helix-PCBs.

The analogue signals from the Helix-PCBs are amplified by transconductance amplifiers CLC415 and AnalogOutDummy is subtracted from AnalogOut. The differential signal obtained by this is put on a twisted air flat ribbon cable. The CLC415 are operated between 0V and +5V.

All power blocking is done with reference to ground (0V).

3.3 The trigger driver board

The trigger driver board receives the combined comparator outputs of the AS7 and AS8 Helix-PCBs and sends them to the electronics at the outer frame of the Outer Tracker. It is built with the 74Fxxx logic family.

Comparator outputs from the Helix-PCB are latched with 74F573 transparent latches operated at -2V/+3V. The outputs are level shifted to 0V/+5V via LEDs and 1kΩ resistors and are received by AT41 differential line drivers. Multiplexing by a factor of 4 is done via selectively switching the 74F573 outputs at 50MHz. Every four clock cycles an empty data frame is sent which is used for synchronisation.

3.4 Grounding scheme

There exists a single grounding point on the (conducting) CFK support layer for all electronics of the layer (fig. 18). The backplane of the MSGC is connected to the `Gnd` (0V) net of the Helix-PCBs, which are then connected together to the grounding point.

External tubing (e. g. for water cooling and gas supply) is isolated before entering the screening volume.

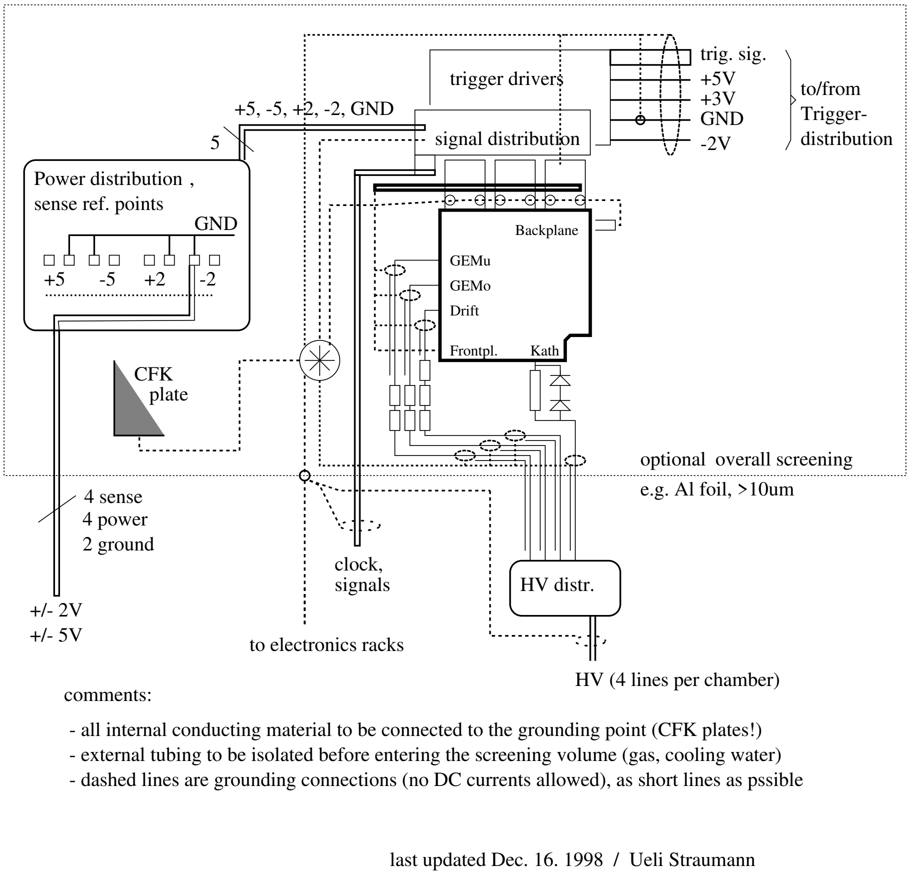

Figure 18: Grounding scheme

Table 2: Threshold-Values for Comparator vs. external load, measured at one chip on AS7-1 PCB with HELIX128-2.2, 5 x **notCompOut** connected to 1kΩ drain resistors

Signal $[MIP]$ $1\ MIP_{Si} = 24.000e^-$	C_{Load} $[pF]$	Min. $V_{CompRef}$ $[mV]$
1 (ext.)	0	25
1 (ext.)	10	63
1 (ext.)	15	75
2 (int.)	0	55

4 Measurements

4.1 Minimum threshold without chamber

The Helix128-2.2 chip already shows oscillation at a rather high comparator threshold even without being attached to a chamber. Table 2 shows the minimum threshold to detect safely a 1 MIP signal without causing oscillation versus the external load.

We tried to identify the cause of the oscillation by producing various pulse shape scans. In a pulse shape scan, the sampling time of the pipeline (i. e. the **Sclk** signal) is shifted versus the comparator clock (**CompClk**) and a test pulse. The testpulse may either be applied by usage of the internally generated test pulse to all channels (activating **FcsTp**) or by an external signal coupled via a charge division circuitry to a single channel. When the comparator is switching and the open drain driver is driving current, a perturbation of the pulse shape can be observed when the open drain driver is switching on an off (fig. 19, green curve). The perturbation causes a fake signal of the comparators which in turn causes another perurbation. In effect the whole chip oscillates.

It can even be seen that a channel farer away from the drivers (channel 4, red) is less disturbed than a channel nearer to the drivers (channel 124, black and green). Hence the perturbation is not caused by the comparator circuit nearby the preamp/shaper, but solely by the output drivers. This was verified by adjusting the comparator threshold to a level that causes oscillation and successively removing the drain resistor contacts to +2V, so that no current flows into the drivers any longer. Without connecting the drain resistors to +2V no oscillation can be oberved, even when the comparators are switching.

An investigation of the Helix128-2.2 layout showed that the scribe line, surrounding the whole chip and put on **Vss** potential, was contacting the ESD protection diodes of the output drivers. In turn the scribeline has direct contact to the guard ring surrounding the preamplifier and to the ESD protection of the preamplifier input transistors. Thus, switching noise was coupled efficiently to the substrate around the preamplifier input.

This connection was removed by a "scribeline scratch" and results were far better (fig. 20).

The scribeline scratch was introduced into the Helix128-3.0 design as scribeline-

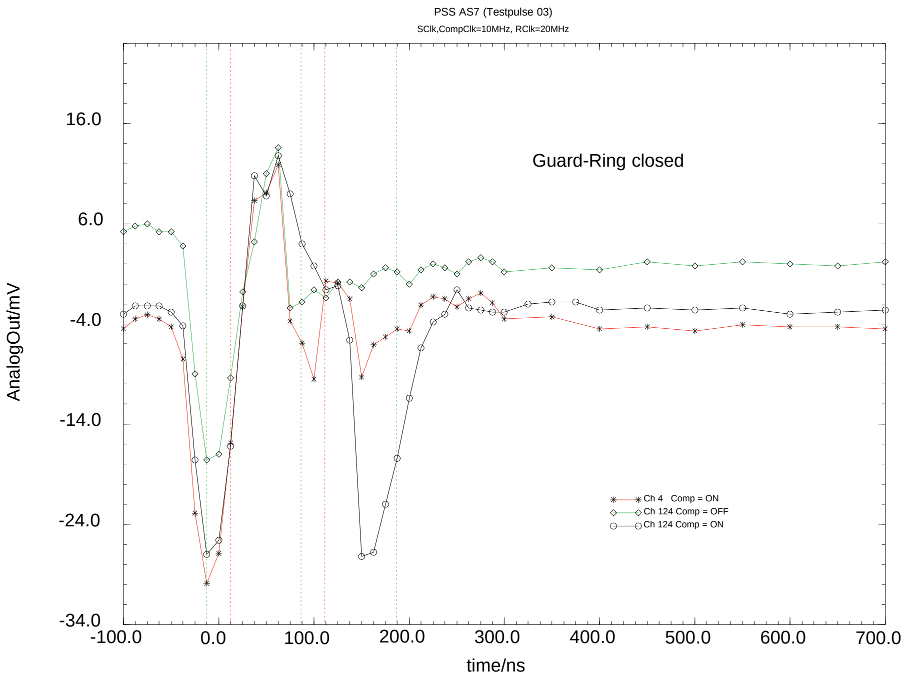

Figure 19: Pulse shape scan at Helix128-2.2, all comparators switching, no connection to MSGC

cut and the Helix128-3.0 behaved the same like a "scratched" Helix128-2.2.

The oscillation can be identified as a hysteresis in a plot where first the comparator threshold is lowered until oscillation is reached and than increased again until oscillation stopps.

The Helix128-2.2 clearly shows a large hysteris (fig. 21) whereas the Helix128-3.0 does not (fig. 22).

4.2 Minimum threshold with chamber

When the Helix chips are attached to a MSGC they show a much larger minimum threshold due to the capacitive load on the input. This load has two effects:

- It increases the white noise of the preamplifier
- It scales noise coupling on the power supply or the reference ground

Thus we now think that measuring without attached chamber is not useful.

Table 3 shows the minimum threshold which can be achieved when a Helix-PCB type AS7-2 with Helix128-3.0 chips is bonded to a chamber.

When no signal is applied and if all power nets of same tension are short-circuited (i. e. the same situation like on a AS7-1), 38mV minimum threshold

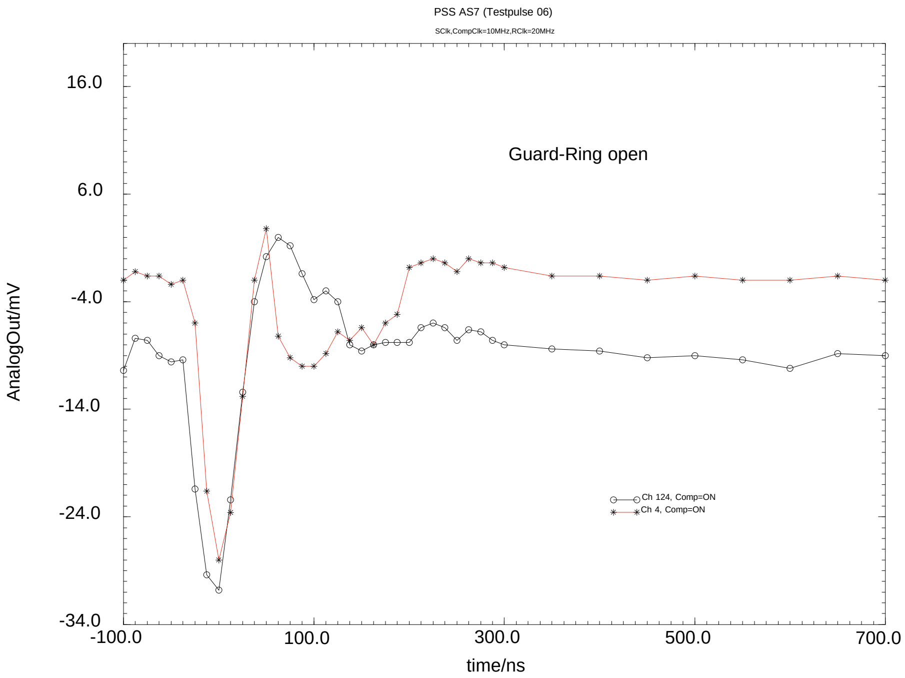

Figure 20: Pulse shape scan at Helix128-2.2 with scribeline scratch, all comparators switching, no connection to MSGC

can be achieved before the chips start oscillating; to be compared with a input of 1 $\mathrm{MIP_{Si}} = 24000\mathrm{e}^-$ causing a 40mV signal at the comparator. Providing separate power for `VssCompOut` and *VddCompOut* results in a marginal better threshold value of 37mV. Deriving these power nets on board via 0.68μH inductances from `Vdda` and `Vssa` (fig. 9) results in a better value of 24mV.

The same behaviour can be observed when the internal test pulse is applied. Here, the minimum threshold is defined by the comparators being ON for 1...2 bunch crossings after activating the test pulse.

Thus, deriving the drain resistor power supply *VddCompOut* and the return current supply `VssCompOut` via an inductance from `Vssa` and `Vdda` seems to be the optimal solution.

PCBs with this configuration were tested for their behaviour when one or several chips are activating their comparator outputs (table 4). It can clearly be seen that activating two chips instead of one makes the situation worse.

If the PCBs are powered via the signal distribution board AS15 the results again are worse compared to power a PCB directly.

Connecting the drain resistors to 0V instead of 2V improves the situation (essentially the energy of the perturbation is halved).

Since two chips operating in parallel perform worse than a single chip, we think that the perturbation is globally coupling via the power supply to the

Table 3: Minimum threshold at various power interconnections with Helix-PCBs attached to chamber and a single Helix PCB operated without signal distribution board

Signal $[MIP]$ $MIP_{Si} = 24000e^-$	Power interconnection Analog, Digital	Start value VCompRef $[mV]$	Minimum value Comparator = ON for 1-2 BX after test pulse VCompRef $[mV]$
0	Common		38
0	`VssCompOut` separately supplied		37
0	`VssCompOut` separated by 0.68μH		24
2 (int.)	Common	60…65	50
2 (int.)	`VssCompOut` separately supplied	60…65	50
2 (int.)	`VssCompOut` separated by 0.68μH	60…65	46

Table 4: Minimum threshold with Helix-PCBs attached to a chamber and with `VssCompOut` and *VddCompOut* decoupled via 0.68μH inductance

PCB / Chip	Signal $[MIP]$	Start value VCompRef $[mV]$	Minimum value VcompRef $[mV]$
$1 \times$ AS7-2, 2 chips operated	2 (int.)	60…65	41
$1 \times$ AS7-2, 1 chip operated	2 (int.)	55…60	40
$1 \times$ AS7-2, 1 chip operated	0		16
$1 \times$ AS7-2, 2 chips operated, *VddCompOut* to 0V (`Gnd!`)	2 (int.)	55…60	28
$1 \times$ AS7-2, 2 chips operated, *VddCompOut* to 0V (`Gnd!`)	0		20
MSGC with AS15, 3 PCBs operated	2 (int.)	75	55
MSGC with AS15, 3 PCBs operated	0		32

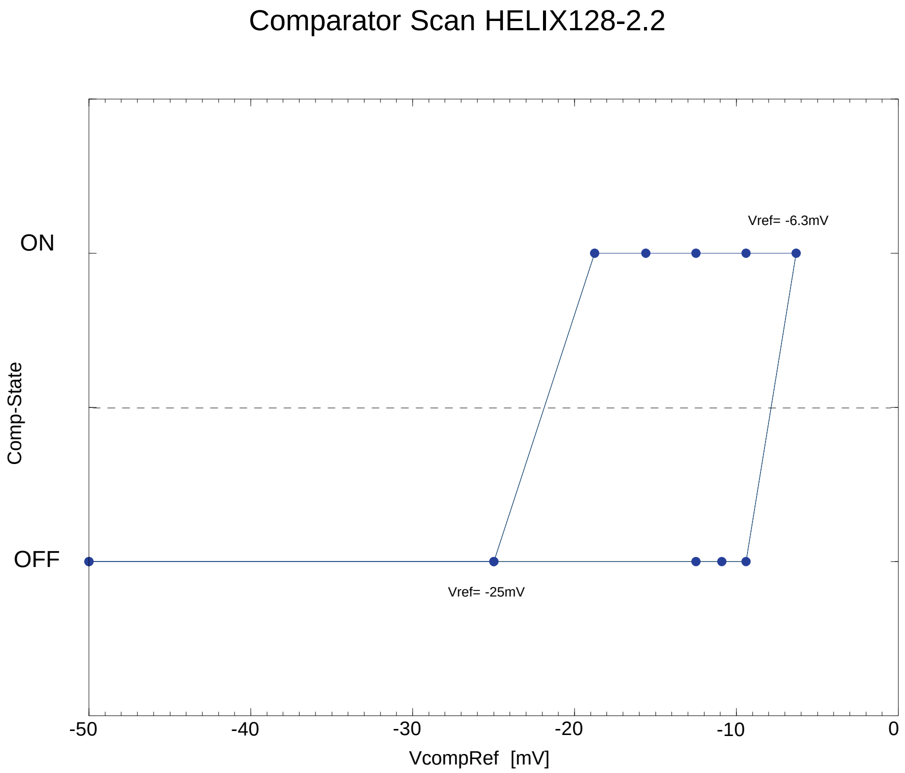

Figure 21: Threshold hysteresis at Helix128-2.2

frontend.

5 Ideas to solve the problem

Improving the stability of the power supply is difficult in the HERA-B Inner Tracker due to the limited amount of material that is allowed to bring into the detector. Thus, the magnitude of the perturbation has to be decreased. Two ways are possible:

- Decrease the voltage swing of the open drain drivers
- Use a differential signal transmission, where two perturbations cancel.
- A combination of both items above, i. e. a LVDS (Low Voltage Differential Signal) scheme or something similar. LVDS in special has the advantage that the current flowing int the chip remains constant even when the drivers are switching. Thus substrate bouncing is minimized.

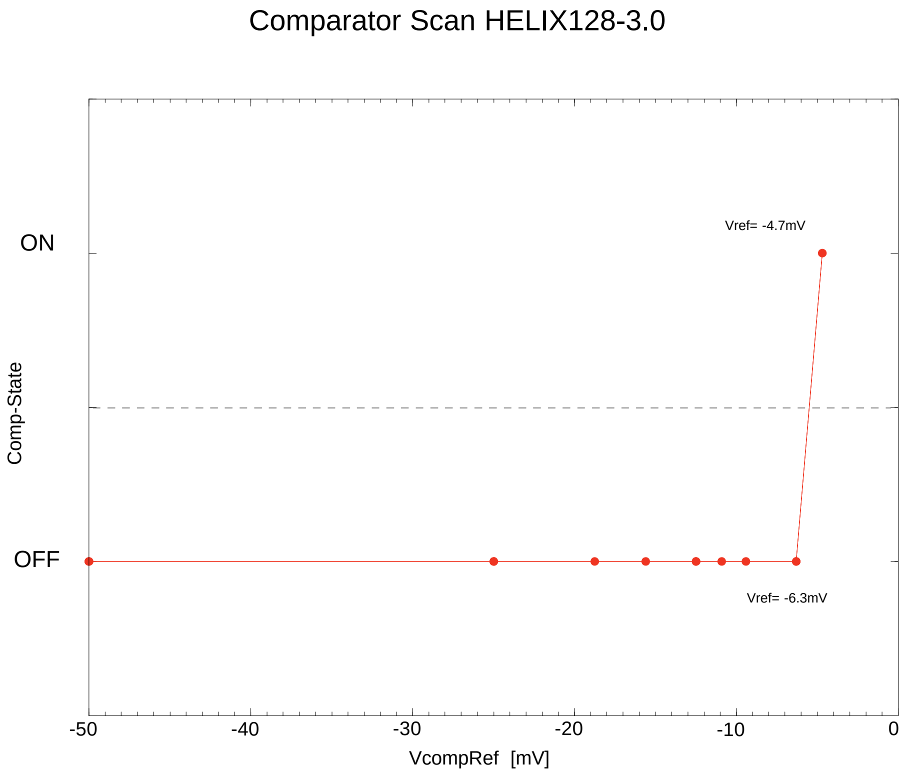

Figure 22: Threshold hysteresis at Helix128-3.0

A differential scheme has the drawback that it doubles the number of signals. Since this is not affordable, the comparator outputs had to be multiplexed by a factor of two, i. e. half of the comparator signals have to be send at the low period of **Sclk**, the other half at the high period.

Minimize substrate coupling can also (still) be discussed, by means of:

- using PMOS transistors as drivers, which are located n a separated well
- using a separate substrate.

A chip (TRIX) has been submitted that should allow testing several opportunities. It can be placed to the side of the Helix128 chip and contains 32 receivers with controllable current sources for the opendrain drivers of the Helix and two alternative driver sets:

- a CMOS driver in which both the NMOS and the PMOS can be switched off to emulate either a PMOS or and NMOS open drain driver
- a LVDS output driver

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