# AdvancedAnalog Building Blocks
# Two Stage amplifiers
# Fully Differential amplifiers

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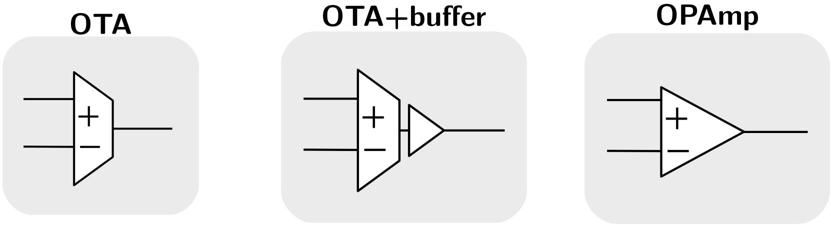
## OTA and OPAmp

- **OTA**: *Operational Transconductance Amplifier*
  Voltage input → Current output
- **OPAmp**: *Operational Amplifier*
  Voltage input → Voltage output (buffered)

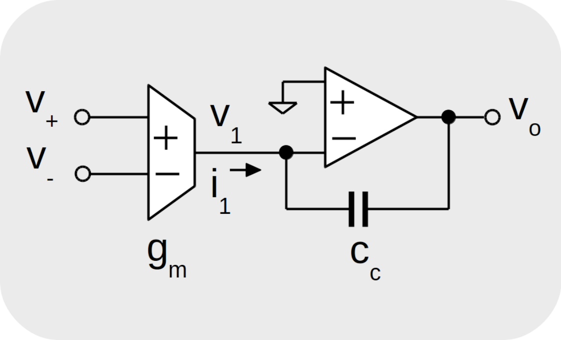



Key parameters;

- Gain Bandwidth Product
- DC Gain
- Stability (Phase margin)
- Biasing (symmetry and matching)

## General OPAmp model

### General model

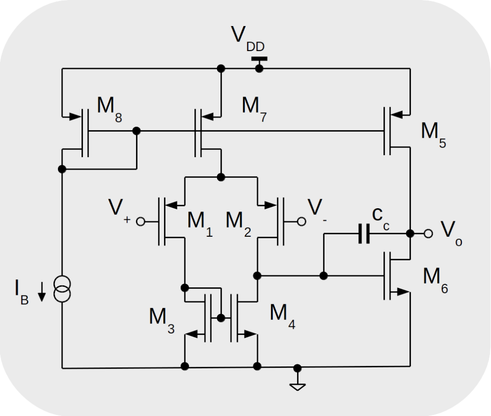



- First stage OTA; $i_1 = (v_+ - v_-) \times g_m = v_{diff} \times g_m$
- Virtual short circuit in $v_1$; $\rightarrow \frac{v_o}{i_1} = -\frac{1}{sC_c}$
- Thus; $|A_v(f)| = \frac{g_m}{2\pi \times f \times C_c}$
- $GBW = A_v(f)_{f_T=1} = \frac{g_m}{2\pi \times C_c}$

## Miller OTA - Circuit

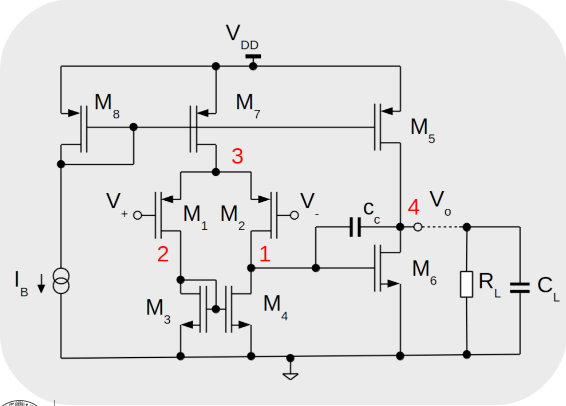
Two stage amplifier;

- Fist stage: OTA
- Second stage: Inverter
- Miller capacitance between first and second stage



## Miller OTA - Circuit nodes

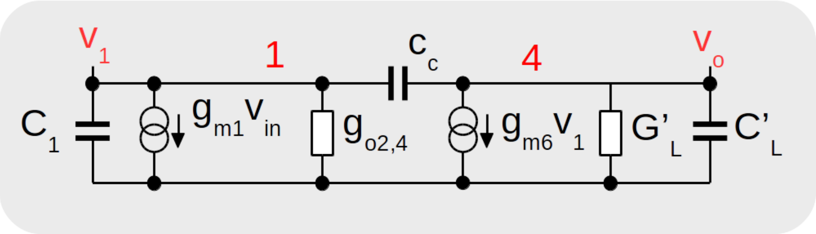
- 3-node for analisys (3 virtually grounded in ac)
- Load affects stability!




$$\left(\frac{W}{L}\right)_8 = \left(\frac{W}{L}\right)_7$$
$$\left(\frac{W}{L}\right)_5 >> \left(\frac{W}{L}\right)_7$$
(Typically x10)

# Miller OTA - Circuit DC gain

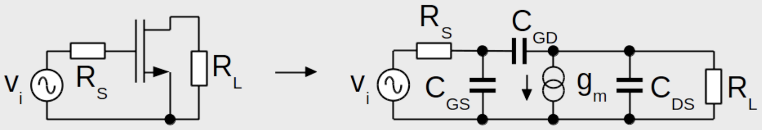
- Small-signal model (node 2 is low-resistance node).

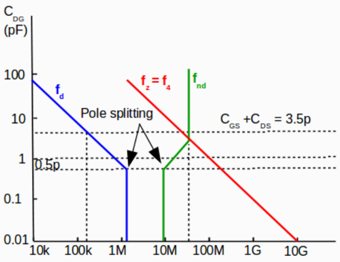


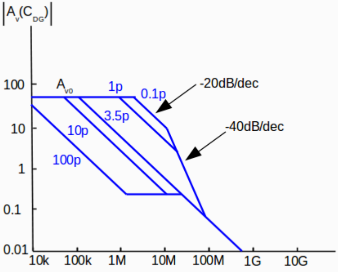

$$g_{o2,4} = g_{o2} + g_{o4}$$
$$G'_L = G_L + g_{o5} + g_{o6}$$
$$C'_L = C_L + C_4$$

$$A_v = \frac{v_o}{v_{in}} = \frac{v_i}{v_{in}}\frac{v_o}{v_i} = \left(\frac{g_{m1}}{g_{o2,4}}\right)\left(\frac{g_{m6}}{G'_L}\right) = A_{v1}A_{v2}$$

# Miller OTA - Pole splitting effect



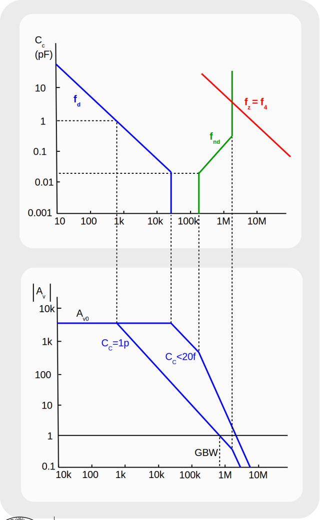



## Miller OTA - Circuit poles

- Circuit poles without $C_c$
  - $f_{p1} = \frac{g_{o2,4}}{2\pi C_1} \rightarrow C_1 = C_{GD2} + C_{DB2} + C_{GD4} + C_{DB4} + C_{GS6}$
  - $f_{p4} = \frac{G_L'}{2\pi(C_L+C_4)} \rightarrow C_4 = C_{GD5} + C_{DB5} + C_{DB6}$
  - $f_{p2} = \frac{g_{m3}}{2\pi C_2} \rightarrow C_2 = C_{GS3} + C_{DB3} + C_{GS4} + C_{GD4} + C_{GD1} + C_{DB1}$
- $f_{p2}$ goes to high frequency forming a pole-zero pair, so can be neglected.
- **Adding $C_c$ the dominant pole becomes more dominant;**
  $BW \approx f_d = \frac{g_{o2,4}}{2\pi Av_2 C_c}$ (applying Miller effect)
  $GBW \approx \frac{g_{m1}}{2\pi C_c}$
- Non-dominant pole, assuming $C_1 << C_c, C_L' and g_{m6} >> G_L'$;
  $f_{nd} \approx \frac{g_{m6}}{2\pi C_L'}$
- $PM \approx 90^\circ - arctg \frac{GBW}{f_{nd}} \rightarrow f_{nd} = 3GBW \ (PM \approx 70^\circ)$

# Miller OPamp - $C_c$ and GBW,PM



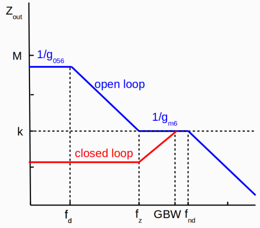

- Variation of poles and zeros with $C_c$
- $C_c$ value is fundamental to achieve enough GBW and PM
- $GBW \approx \frac{g_{m1}}{2\pi C_c}$
- $PM \approx 90^\circ - arctg \frac{GBW}{f_{nd}}$
- $f_{nd} \approx \frac{g_{m6}}{2\pi C_L'}, g_m = \frac{2I_D}{(V_{GS}-V_T)}$
- $f_{nd} = 3GBW \; (PM \approx 70^\circ)$

## Miller OTA - Steps for design

- Take a value for $I_{D6} = I_{D5}$
- For $M_6$;
  1. Choose the overdrive voltage (ex. $V_{GS} - V_T = 0.2$).
  2. Obtain $g_{m6} = \frac{2.I_{D6}}{V_{GS6} - V_T}$ and $\left(\frac{W}{L}\right)_6 = \frac{g_{m6}}{K'(V_{GS5} - V_T}$
  3. Use minimum $L_6$ to get $W_6$
- Repeat for $M_5$ (now use $V_{GS} - V_T = 0.5$ for better matching, reduced swing)
- Calculate $C_c$ for desired $A_v$.
- Use around a factor 10 between $M_5$ and first stage bias.
- Iterate on simulation to fine tune values.

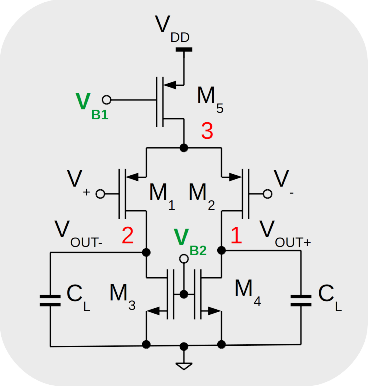
## Miller OTA - characteristics

- Common mode input:
  $V_{CMinMAX} = V_{DD} - V_{GS1} - V_{DS7}$
  $V_{CMinMIN} = V_{SS} + V_{GS3} - V_{DS1} - V_{GS1}$
- Output voltage range, with no $R_L$ rail-to-rail with some distortion due to MOS linear operation close to rails.
- Slew rate, non linear effect. Maximum rate output voltage variation. $SR = \frac{I_{bias1^{st}stage}}{C_c}$
- Output impedance: (will limit output voltage when $R_L$)



## Fully Differential - schematic

Fully differential amplifiers show excellent CMRR and PSRR which make them very useful for mixed-signal design.

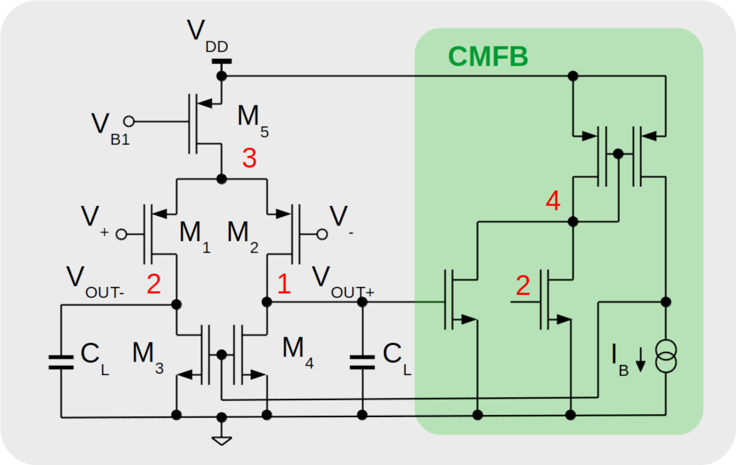



- No current mirror as load, just current sources.
- Nodes 1 and 2 become symmetric.
- $GBW \approx \frac{g_{m1}}{2\pi C_L}$

**Problem**

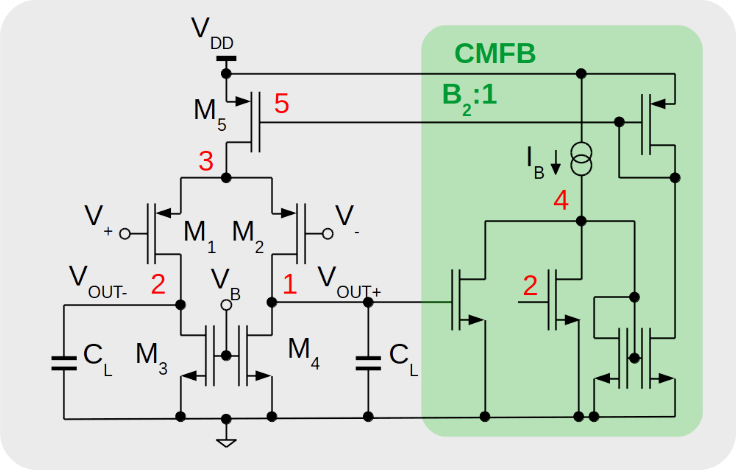
Keep all transistors saturated, regulation of $V_{B1,2}$

## Fully Differential - CMFB



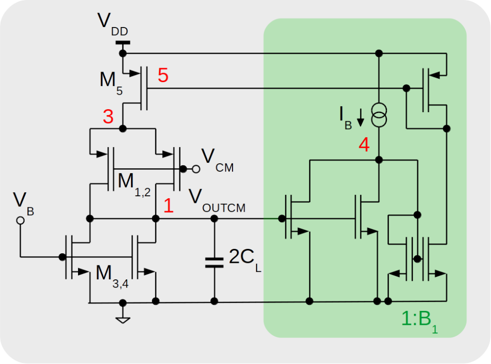

- The common-mode output voltage is sensed and fed back to load sources (CMFB: Commmon-Mode FeedBack).

## Fully Differential - CMFB




- More usual implementation

## Fully Differential - Common mode equivalent circuit




- Open loop gain:
  $A_{vCM} = B_1 B_2 g_{m6} R_L$
  $GBW_{CM} = \frac{B_1 B_2 g_{m6}}{2\pi C_L}$
- GBW can be made high with more power.
- Condition:
  $GBW_{CM} > GBW_{DIFF}$
- The CMFB increases the CMRR.

## Exercise 1: Miller OTA

Design a Miller OTA with the following specifcations:

- $A_{vDC} = 100$
- $BW = 100MHz$
- $PM > 70^\circ$
- Try to minimize power consumption.

Use $R_L = 1M$, $C_L = 1pF$.

## Exercise 2: Fully differential amplifier

Design a Fully differential amplifier with CMFB with the following specifcations:

- $A_{vDC} = 100$
- $BW = 100MHz$
- $PM > 70^\circ$
- Try to minimize power consumption.

Use $R_L = 1M$, $C_L = 1pF$.