Advanced Analog Building Blocks
Current mirrors

Albert Comerma (PI)
(comerma@physi.uni-heidelberg.de)

Course web
SoSe 2017
Introduction: CMOS transistors

- Several possibilities for representation of transistors.

**NMOS**

![NMOS Diagram]

\[ I_D = \frac{\mu C_{ox}}{2} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \]

\[ g_m \approx \sqrt{2\mu C_{ox} \frac{W}{L} I_D} \]

**PMOS**

![PMOS Diagram]

\[ I_D = \frac{\mu C_{ox}}{2} \frac{W}{L} (V_{SG} - |V_T|)^2 (1 + \lambda V_{SD}) \]

\[ g_m \approx \sqrt{2\mu C_{ox} \frac{W}{L} |I_D|} \]

- For simplicity usually only one type of circuits are depicted even if both implementations are possible.
**Introduction: Diode connected transistor**

**Drain and Gate connected NMOS**

Always on saturation!

\[ V_{DS} = V_{GS} \rightarrow V_{DS} > V_{GS} - V_T \]

\[ I_D = \frac{\mu C_{ox} W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \]

**DIODE CONNECTED**

For any given \( I_D \), the \( V_{GS} = V_{DS} \) will adapt to permit the current flow.
Introduction: Use of current mirrors

Several applications:
- Biasing of circuits.
- Current amplification
- Active loads.
- Current-mode signal processing.

Best current mirror:
- High output impedance (ideally $\infty$).
- Rail-to-rail output swing (from $V_{DD}$ to $GND$).

Current mirrors performance is strongly dependent on transistor matching!!
Good layout techniques needed.
Simple current mirror: Same $V_{GS}$ transistors circuit

**Assuming saturation:**

- $I_{M1} = \frac{\mu C_{ox}}{2} \frac{W}{L} (V_G - V_T)^2 (1 + \lambda V_{D1})$
- $I_{M2} = \frac{\mu C_{ox}}{2} \frac{W}{L} (V_G - V_T)^2 (1 + \lambda V_{D2})$

For same $L$:

The ratio of $I_{M2} / I_{M1}$ is given by $\frac{W_2}{W_1} \frac{L_2}{L_1} \frac{1 + \lambda V_{D2}}{1 + \lambda V_{D1}}$

Early effect cancelled for $V_{D2} = V_{D1}$
**Simple current mirror: circuit operation**

**$M_1$ connected as a diode:**

\[
I_{M1} = \frac{\mu C_{ox}}{2} \frac{W}{L} (V_G - V_T)^2 (1 + \lambda V_G)
\]

\[
I_{M2} = \frac{\mu C_{ox}}{2} \frac{W}{L} (V_G - V_T)^2 (1 + \lambda V_D)
\]

\[
\frac{I_{M2}}{I_{M1}} = \frac{W_2}{W_1} \frac{1 + \lambda V_D}{1 + \lambda V_G}
\]

**Output swing:**

\[
V_{D,min} = V_{Dsat}
\]

---

**Current is copied "mirrored":**

The ratio of \(\frac{I_{M2}}{I_{M1}}\) is given by \(\frac{W_2}{W_1}\) (for same L)

Early effect cancelled for \(V_D = V_G\) (same L desired)
Simple current mirror: output impedance

- The output resistance \((r_o)\) depends only on \(M_2\) output transistor.
- \(v_{gs} = 0\) since gate voltage is DC.
- \(r_o = r_{ds}\) value depends on current and geometry of transistor.
Wilson current mirror: circuit operation

**Same principle of operation:**

\[ V_{GS_1} = V_{GS_2} \rightarrow I_{M1} \approx I_{M2} \]

\[ \frac{I_{out}}{I_{ref}} = \frac{W_2}{L_2} \frac{1 + \lambda V_{DS_2}}{1 + \lambda V_{DS_1}} \]

\[ V_{DS_1} = V_{DS_2} + V_{GS_3} \rightarrow \text{error} \]

\[ \frac{I_{out}}{I_{ref}} = \frac{W_2}{L_2} \frac{1 + \lambda V_{DS_2}}{1 + \lambda (V_{DS_2} + V_{GS_3})} \]

**Output swing:**

\[ V_{out, min} = V_{GS_2} + V_{DS sat_3} \]

\[ V_{out, min} > V_{Th} + 2V_{DS sat} \]
Wilson current mirror: output impedance

- $R_L$ ($I_{\text{ref}}$ current generator impedance) must be large.

\[
\begin{align*}
  v_{g2} &= v_{s3} = \frac{i_x}{g_{m2}} \\
  v_{g3} &= -g_{m1}v_{g2}r_T \rightarrow r_T = R_L/|r_{ds1}| \\
  r_{out} &= \frac{v_x}{i_x} = \frac{1}{g_{m2}} + r_{ds3} \left[ 1 + \frac{g_{m3}}{g_{m2}} + \frac{g_{m3}}{g_{m2}} g_{m1}r_T \right] \\
  r_{out} &\approx r_{ds3} \frac{g_{m3}}{g_{m2}} g_{m1}r_T \approx r_{ds3} \frac{g_{m3}}{g_{m2}} g_{m1} r_{ds1}
\end{align*}
\]
Wilson current mirror: improved

Same principle of operation:

\[ V_{DS1} = V_{DS2} + V_{GS3} - V_{GS4} \]
\[ V_{DS1} = V_{DS2} \text{ if } V_{GS3} = V_{GS4} \]

\[
\frac{I_{out}}{I_{ref}} = \frac{W_2}{L_2} \frac{1+\lambda V_{DS2}}{1+\lambda(V_{DS1})} \]
\[
\frac{I_{out}}{I_{ref}} = \frac{W_2}{L_2} \frac{1}{W_1 L_1} \]

No error introduced
Wilson current mirror: improved output impedance

\[ v_{g3} = -g_{m1}v_{g2}r'_T \frac{R_Lg_{m4}}{1+R_Lg_{m4}} \]

\[ r'_T = r_{ds1}/\left( R_L + \frac{1}{g_{m4}} \right) \]

\[ r_{out} \approx r_{ds3}g_{m3}g_{m2}g_{m1}r'_T \frac{R_Lg_{m4}}{1+R_Lg_{m4}} \approx r_{ds3}g_{m3}g_{m2}g_{m1}r_{ds1} \]
Cascode current mirror: circuit operation

**Principle of operation:**

\[
V_{DS_1} = V_{DS_2} + V_{GS_3} - V_{GS_4}
\]

\[
V_{DS_1} = V_{DS_2} \text{ if } V_{GS_3} = V_{GS_4}
\]

\[
\frac{I_{out}}{I_{ref}} = \frac{W_2}{W_1} \frac{1+\lambda V_{DS_2}}{1+\lambda(V_{DS_1})}
\]

**Output swing:**

\[
V_{out,min} = V_{GS_1} + V_{GS_4} - V_{GS_3} + V_{DS_{sat_3}}
\]

\[
V_{out,min} = V_{GS_2} + V_{DS_{sat_3}}
\]

\[
V_{out,min} > V_{Th} + 2V_{DS_{sat}}
\]
Cascode current mirror: output resistance

\[
i_x = g_{m3} v_{gs3} + \frac{v_x - v_{s3}}{r_{ds3}}
\]

\[
i_x = \frac{v_{s3}}{r_{ds2}}
\]

\[
v_x = \left( i_x - g_{m3} (-v_{s3}) \right) r_{ds3} + i_x r_{ds2}
\]

\[
r_{out} = \frac{v_x}{i_x} = \frac{i_x r_{ds3} + g_{m3} v_{s3} r_{ds3} + i_x r_{ds2}}{i_x}
\]

\[
r_{out} = r_{ds2} + r_{ds3} + r_{ds3} g_{m3} r_{ds2} \approx r_{ds3} g_{m3} r_{ds2}
\]
## Basic current mirrors comparison

<table>
<thead>
<tr>
<th>Type</th>
<th>Complexity</th>
<th>Output impedance</th>
<th>Output swing ((V_{0,\text{min}}))</th>
</tr>
</thead>
<tbody>
<tr>
<td>Simple</td>
<td>low ✓</td>
<td>(r_{ds} \times)</td>
<td>(V_{DSsat} \checkmark)</td>
</tr>
<tr>
<td>Wilson(^1)</td>
<td>medium ✓</td>
<td>(r_{ds3} \frac{g_{m3}}{g_{m2}} g_{m1} r_{ds1} \checkmark)</td>
<td>(V_{Th} + 2V_{DSsat} \checkmark)</td>
</tr>
<tr>
<td>W. Improved</td>
<td>high ✗</td>
<td>(r_{ds3} \frac{g_{m3}}{g_{m2}} g_{m1} r_{ds1} \checkmark)</td>
<td>(V_{Th} + 2V_{DSsat} \checkmark)</td>
</tr>
<tr>
<td>Cascode</td>
<td>high ✗</td>
<td>(r_{ds3} g_{m3} r_{ds2} \checkmark)</td>
<td>(V_{Th} + 2V_{DSsat} \checkmark)</td>
</tr>
</tbody>
</table>

\(^1\)Introduces an error in current copy, not desirable.
Use examples: bias distribution

- PACIFIC design bias distribution.
- 4x3.85 mm² die size.
- Bias voltages distributed everywhere.
- Long distances for biasing (drop in different supply voltages!!).
Use examples: binary weighted DAC

- Binary weighted DAC.
- $n$ is the number of bits.
- Lower transistors just enable output.
- $I_{\text{out,\ max}} = I_{\text{ref}}$.
- Other implementations possible (cascode).

\[
V_{\text{out}} = I_{\text{out}} R = R \sum_{i=1}^{n} I_n b_{n-1}
\]

$b_n$ is a digital signal which can be 0 or 1
Widar current mirror

- Current copy does not need to have a linear response.

**Principle of operation:**

\[
V_{S2} = RI_{M2}
\]

\[
I_{M1} = \frac{\mu C_{ox}}{2} \frac{W}{L} (V_G - V_T)^2 (1 + \lambda V_G)
\]

\[
I_{M2} = \frac{\mu C_{ox}}{2} \frac{W}{L} (V_G - V_{S2} - V_T)^2 (1 + \lambda V_D)
\]

\[
I_{M2} = \left( 1 - \sqrt{1 + 2R \sqrt{2\mu C_{ox} \frac{W_2}{L_2} I_{M1}}} \right)^2 \frac{2\mu C_{ox} \frac{W_1}{L_1} R^2}{2\mu C_{ox} \frac{W_1}{L_1} R^2}
\]

Useful for small currents generation.
More cascode stages can be stacked to increase $r_o$.

Output impedance:

$$r_{out} \approx (r_{ds}g_m)(n - 1)r_{ds}$$

$n \rightarrow$ number of stages

Saturation voltage increases to:

$$V_{out,min} = (n - 1)V_{Th} + nV_{DSsat}$$
High-swing Cascode

Principle of operation:

- The voltage increase shifts $V_{DS1}$ enough to bias $M3$ without operating $M2$ out of saturation.
- The change results in more swing at the output.
Possible implementation

Voltage increase:

$$\Delta V = V_{GS4} - V_{GS5}$$

$$\Delta V = \sqrt{\frac{2}{k'}} \left( \frac{L_4}{W_4} \right) I_{ref} - \sqrt{\frac{2}{k'} \left( \frac{L_5}{W_5} \right) I_5}$$

$$\Delta V = \sqrt{\frac{2}{k'} \left( \frac{L_4}{W_4} \right) I_{ref} \left( 1 - \sqrt{\frac{L_5}{W_5} \frac{L_6}{W_6} \frac{L_1}{W_1} \frac{L_4}{W_4} \frac{L_1}{W_1}} \right)}$$

- $\Delta V$ fixed by dimensions of $M_{1,4,5,6}$.
- Output swing:
  $$V_{out,\text{min}} = V_{DS2} + V_{DS3} = 2V_{DSat}.$$  
- Systematic error since $V_{DS1} \neq V_{DS2}$.
- Only for strong inversion conditions (which may not be the case).
Regulated cascode

Principle of operation:

- \( V_D \) is kept constant.
- \( V_b \) reference needed. 
\[
V_c = A(V_b - V_{DS2})
\]
Regulated cascode: output resistance

\[ r_{out} = r_{ds3} + r_{ds2} (1 + (1 + A)g_{m3}r_{ds3}) \]
Regulated cascode: implementation

Possible implementation

Output impedance;

\[ A \approx g_{m3} r_{ds3} \]

\[ r_{out} \approx r_{ds1} g_{m2} r_{ds2} g_{m3} r_{ds3} \]

- Low threshold on M3 increases output swing (low VT transistor may help).
Fabrication process introduce variations in transistor size (dashed line).

Area variation dependent on transistor size.

Ideally use **fixed transistor size** for mirrors.

Change number of transistors to obtain different sizes.

Other layout techniques also useful (common centroid).
Schematic considerations

- Same dimensions transistors are desirable.
- Replicate constant size transistors.