Status of OTIS development

Outer Tracker meeting

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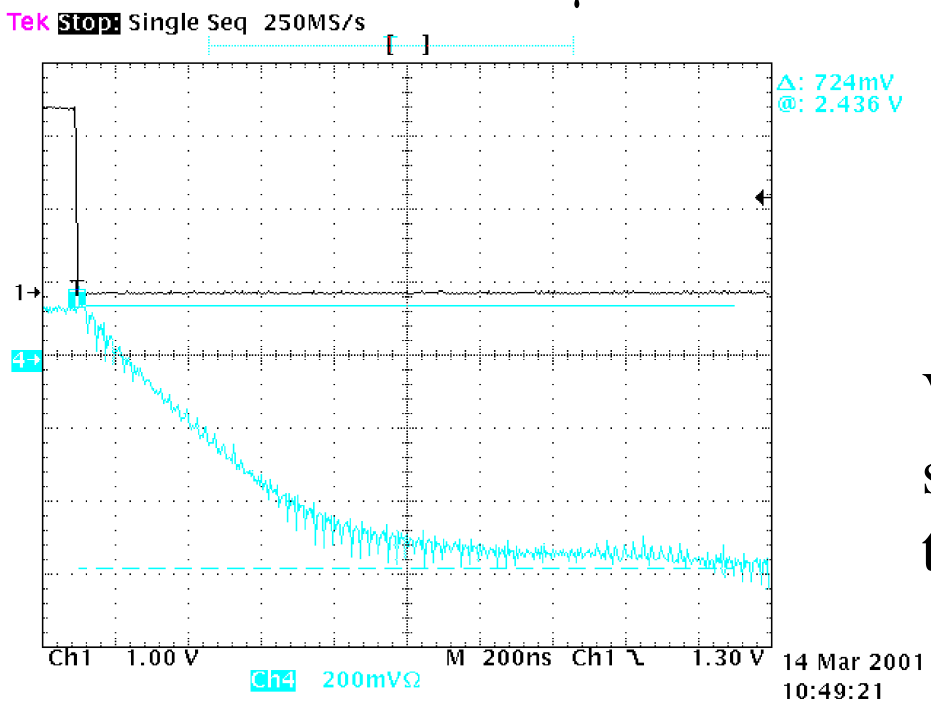
Harald Deppe , Martin Feuerstack-Raible , Uwe Stange , Andr Srowig
Heidelberg University

OTIS submission overview

- DLL1.0, submitted september 2000, measurements in work (partly presented here)
  - First DLL prototype, contains
    - 32 stage delay chain with 32 taps
    - Mean delay per stage = 781ns nominal
- OTISDLL1.0, submitted february 28, 2001
  - 2nd DLL prototype, contains
    - 32 stage delay with 64 taps
    - Mean delay per tap = 390ns nominal
- OTISMEM1.0, submitted february 28, 2001
  - Contains rad hard L0 pipeline & derandomizer memory
    - 32 channels * (1 + 6)bit/ch. + 16 bit = 240bit wide
    - 186 bit long

DLL1.0 measurements(1)

- Lock time is well below 2μs



Voltage controlling delay settles 2μs after reset of the circuit

Accidentally the lock gets lost and the DLL needs a reset

- Not yet understood, maybe a problem in the test setup (e. g. switching on a neighbouring monitor causes loss of lock state), but operation of several hours w/o problems also possible.

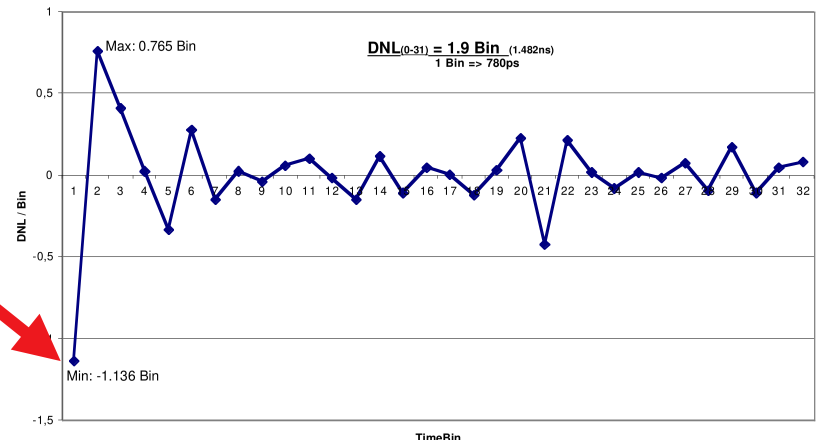
DLL1.0 measurements (2)

- Lock range = 22 44MHz at 300K
  - Spec is 30 50MHz at 300K.
  - This is fully understood
    - an old W/L extraction rule for the transistors was used when the design was done
    - using the old layout with the new extraction rules yields an simulated lock range 20 40MHz (within an 10% error)
    - OTISDLL1.0 layout has been corrected for lock range within specs

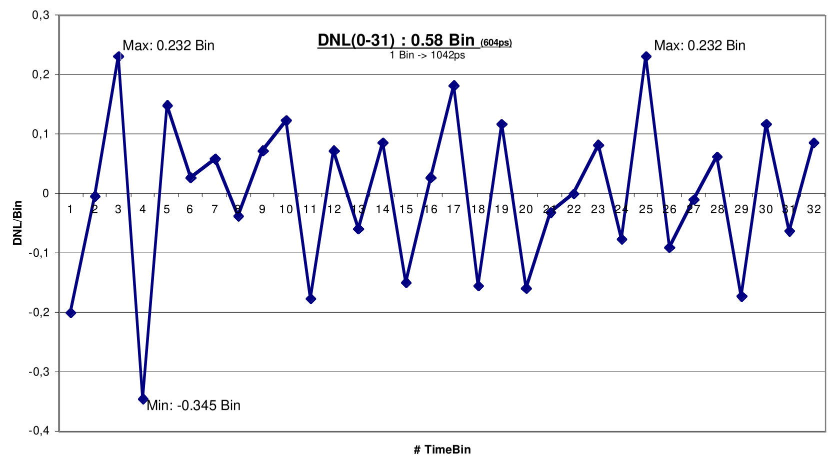
DLL1.0 measurements (1)

- Differential non-linearity (DNL)
  - 1.9bins at 40MHz
    - Large due to non-controlled dummy delay before first delay tap
  - 0.58bins at 30MHz (in the middle of the actual lock range, which fits better with the dummy delay)
- This translates to a resolution of
  - 1.482ns at 40MHz
  - 0.604ns at 30MHz
- Extrapolation to OTISDLL1.0
  - DNL = 0.58bins at 40MHz => resolution 0.45ns (within spec)

f = 40MHz



f =30MHz



Next steps

- OTISDLL1.0 and OTISMEM1.0 expected back in july 2001
  - Detailed measurements will be done asap
- Currently working on
  - behavioral model of the components
  - Overall design of chip OTIS1.0
- Expect specification workshop in june