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Requirements to the Front End Chip for the LHCb Vertex Detector

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Abstract

The specifications of the front end chip for the LHCb vertex detector, resulting from requirements of the Level-0 trigger and the properties of the detector, are discussed and summarized.

1 Introduction

A front end chip for LHCb needs to sample data from a detector with the LHC bunch crossing frequency of 40 MHz. For applications in the vertex detector it has to be radiation hard, if used to readout the inner tracker or the RICH detectors, radiation hardness is still desirable. The data have to be stored on the chip for the latency of the Level-0 trigger decision. The chip specifications thus are driven by the requirements of the specific detector and the Level-0 trigger. For applications in the vertex detector and the inner tracker the chip has to store analogue data, in case of the RICH binary readout is sufficient.

2 Basic Requirements

The most important design parameters for a front end chip of the LHCb vertex detector are collected in tab. (1). The dynamic range was chosen to correspond to ± 10 times the charge deposited by a minimum ionizing particle in $150\,\mu$m silicon. The peaking time and sampling frequency is determined by the LHC bunch crossing rate of 40 MHz, the readout speed must match the Level-0 accept rate of 1 MHz. A signal over noise ratio S/N > 14 is required for reliable operation of the silicon tracker even after irradiation. The radiation hardness must be such, that the chip withstands 5 years of operation at an estimated load around 2 Mrad per year. The length of the pipeline is given by the $4\,\mu$s latency of the Level-0 trigger decision plus the size of the multi-event buffer, which has to be large enough to have negligible dead time at nominal operating conditions. A buffer depth of 16 events ensures that at readout speed of 900 ns/event and a trigger rate of 1 MHz the remaining deadtime is below 1% [1].

readout pitch	40-60 μm
channels per chip	128
detector capacitance	5 – 30 pF
required S/N	> 14
tolerable irradiation dose	$\geq$ 10 Mrad in 5 years
power consumption	< 6 mW/channel
peaking time	≤ 25 ns
pulse spill-over	$< 30\%$ after 25 ns
dynamic range	$\pm$ 110,000 electrons
required linearity	$\leq 5\%$ over full range
sampling frequency	40 MHz
L0 trigger rate	1 MHz
consecutive L0 triggers	yes
multi-event buffer	16 events
max. latency	4 μs (160 $\times$ 25 ns)
readout time	$\leq$ 900 ns/event
slow control interface	I^2C [2]

Table 1: Principal requirements to the readout chip of the LHCb vertex detector.

A single chip has 128 analog inputs. The data are brought off-chip at a clock frequency of 40 MHz, multiplexed to 4 lines. In addition every line transmits two samples of control information which code the pipeline number of the data that follow and thus allow to check the internal cosistency of the data and the operation of the frontend. With 34 bits of information per line and 40 MHz clock frequency the readout of one event is done in 850 ns.

Additional functionalities of the chip are a programming interface via I^2C-bus, internal test pulse generation and support for different reset modes to ensure synchronous operation of the DAQ and trigger chain. In addition to a power-up or full reset, going beyond the specifications of the LHCb front-end architecture, a soft-reset is provided which resets the write and trigger pointers to the pipeline.

3 Additional Requirements

The specifications given above correspond to the minimal requirements by the LHCb vertex detector. For use in the pileup-veto a fast digital signal is is required which has to be derived by routing the output of the front end amplifier to a comparator stage with extra outputs pads on the chip. For read out of the inner tracker, the front end has to be able to operate also with larger input capacitances. Finally, in case the RICH will be equipped with multi-anode PMTs, the chip should also be usable for this detector. In that case the front end would have to tolerate very large pulse heights and run in binary readout mode. In order to have an as homogenuous front end achitecture as possible, the chip should be designed such that it can be produced with different front end amplifiers, leaving the functionality, dimensions and pad layout unchanged. The design of the *Beetle*-chip was based on this philosophy.

4 Summary

This document summarizes the general requirement to a front end chip of the LHCb vertex detector. Detailed information about actual realizations in the SCTA_VELO and the Beetle chip can be found in references [3, 4] and [5, 6, 7], respectively.

References

[1] M. Schmelling, Event Loss Rates and Readout Chips, LHCB/98-057.

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[6] D. Baumeister et al., Characterization of the Beetle-1.0 Front End Chip, LHCb 2001-049.

[7] N. van Bakel et al., Investigation of Characteristics and Radiation Hardness of the BeetleCO10 Chip, LHCb 2001-037.