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Investigation of characteristics and radiation hardness of the Beetle1.0 FrontEnd chip

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Abstract

Noise characteristics of the Beetle1.0 FrontEnd chip have been investigated as a function of input capacitance. Values for the equivalent noise charge and ballastic deficit have been extracted. Amplification and pulse shape have been studied by varying the bias settings over a wide range. Results are compared with simulations that include realistic impedances at the input and output. The chip has been subjected to 10 Mrad of radiation. Subsequently, its behaviour has been measured again and compared to that preceeding the irradiation. Observed radiation damage effects are discussed.

1 Introduction

A collaboration between the ASIC-lab in Heidelberg and NIKHEF is developing a radiation hard frontend chip for the silicon detectors of the LHCb-experiment. Various components of the frontend chip have been submitted in the 0.25 μm CMOS technology in the course of 1999 and 2000. In September 2000 the first 128 channel 40 MHz (full-size) Beetle1.0 chips, featuring pipelines and I^2C control logic, came back from the manufacturer. A testchip BeetleCO10, which contains a copy of the Beetle1.0 FrontEnd (FE), has been used in the measurements presented here.

In section 2 the experimental setup and DAQ-system used are described. The noise performance results are presented in section 3. The characteristics of the frontend are discussed in section 4, where also fits to the measured pulse shapes are presented and compared to simulations. The radiation hardness has been investigated by exposing the chip to 10 MRad of X-rays. The method applied and results obtained are discussed in section 5. This report ends with some conclusions which are presented in section 6.

2 Experimental setup

An overview of the test setup is given in Fig. 1, the core of which consists of the Beetle preamplifier and shaper, which is mounted on a 5 * 5 cm^2 testboard. This testboard is placed in a Faraday cage, grounded together with the scope. The scope is used to measure the pulse shape of the frontend and is triggered by the input signal of the chip, which is generated by a free running pulse generator. Readout of the oscillosope is done through a standard GPIB interface by a PC running LABVIEW software. This program stores the data and furthermore controls an 8 channel DAC board, which supplies the bias settings to the chip via a converter box.

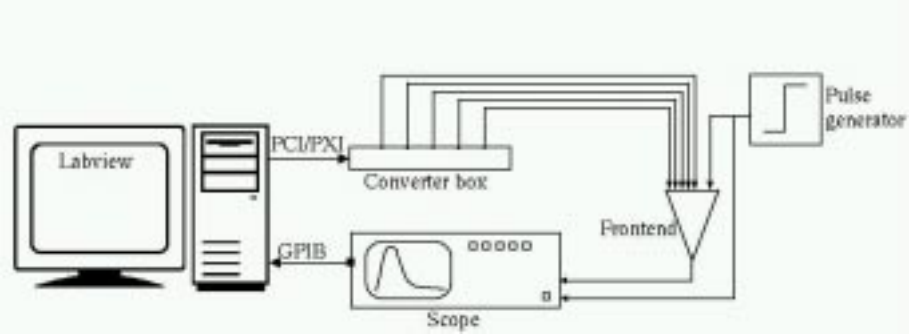

Figure 1: Layout of the test setup used.

2.1 Beetle preamp and shaper

The Beetle frontend is presented in Fig. 2. The behaviour of the chip can be tuned with 5 parameters (V_{fp}, V_{fs}, I_{pre}, I_{sha} and I_{buf}) [1]. The testsignal is a square wave with an amplitude of 18 mV (1.49 MIP) and a frequency of 100 kHz. The output of the chip is directly connected to the scope via a 15 cm long coaxial cable.

2.2 Oscilloscope

The oscilloscope used is a HP 16500C Logic Analysis System, containing 2 ADC channels with a maximum sample rate of 1 Gsamples/sec. The output signal of the chip and the trigger signal from the pulsegenerator are connected to inputs with an input impedance of 1 $M\Omega$ AC and 1 $M\Omega$ DC, respectively. The output signal of the chip is connected to the oscilloscope input with a short (15 cm) coaxial cable, the input capacitance of the scope amounts to 15 pF. A second pulsegenerator output provides a stable trigger signal

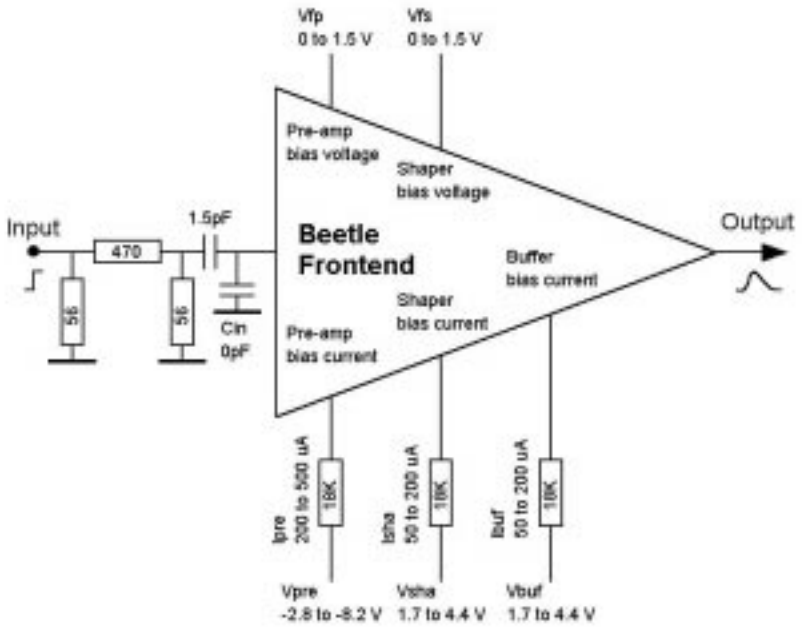

Figure 2: Schematics of the Beetle frontend.

to the scope. On each trigger 1000 samples are taken during 500 ns. The samples are converted to 8 bits numbers and are read by the computer through the GPIB interface.

2.3 Labview program and DAC board

The LABVIEW program interfaces to the scope through GPIB and receives a train of 1000 samples about every 2 seconds. Each pulse (trigger) is written to a separate file on disk. The number of repetitions of a measurement can be specified. LABVIEW also controls the PCI/PXI DAC board, model 7671 from National Instruments, which features 8 DAC's, 12 bits each. By means of the conversion box, the bias voltage levels can be varied between -10 and +10 Volts. The program is capable of varying the input parameters mentioned in section 2.1 in a given range with a specified step size, exploiting all possible input combinations.

3 Noise

To study the dependence of the preamplifier signal on the detector capacitance, we measured the output signal of the amplifier for 6 values of the input capacitance (see C_{in} in

Fig. 2). Table 1 shows the default bias settings and values of the capacitors used, which were measured with a precision RLC-meter (Wayne Kerr model 6425).

Table 1: Input capacitors and default bias settings used for the noise measurements.

C_{in} (pF)						V_{fp}	V_{fs}	I_{pre}	I_{sha}	I_{buf}
0.0	4.9	7.2	15.7	22.5	27.9	1.0 V	0.5 V	350 μA	80 μA	100 μA

For every capacitor value, 3000 oscilloscope traces were recorded. For each of the 1000 sample points (taken at 0.5 ns intervals) a histogram was filled with the 3000 entries. The corresponding mean and standard deviation were extracted from Gaussian fits. The results for the 0 pF measurement are shown in Fig. 3. The mean plot shows the pulseshape of the Beetle1.0 FrontEnd chip, the RMS plot shows that the measured noise is uncorrelated with the testpulse signal.

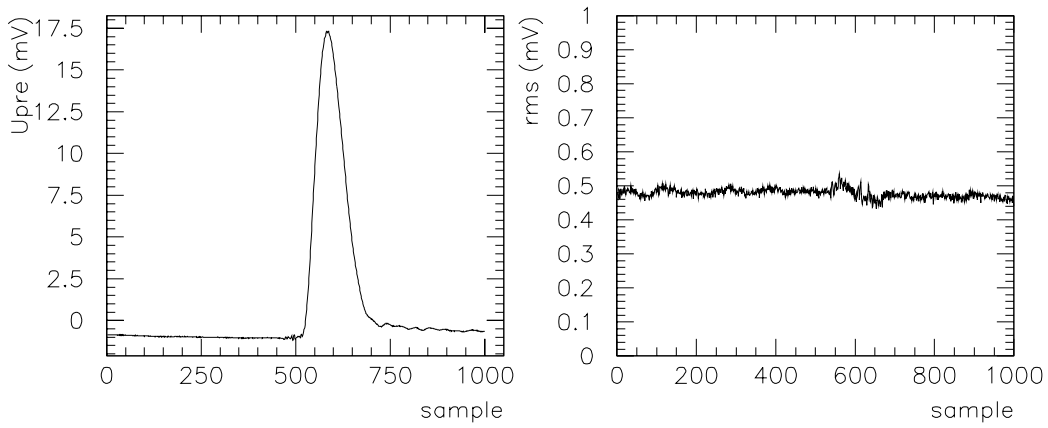

Figure 3: Mean and rms signal versus sample number for an input capacitance of 0 pF.

3.1 Effective input capacitance

Due to the limited input impedance of the preamplifier, not all charge will be collected within the shaping time, which results in a reduction of the amplitude of the output pulse. In Fig. 4 the relative pulseheight is plotted versus the input capacitance. An estimate of the input impedance (capacitance) of the amplifier, C_{amp}, is obtained by fitting the datapoints to the function $\frac{C_{amp}}{C_{amp}+C_{in}}$. This yields a value of 45.8 pF for C_{amp}.

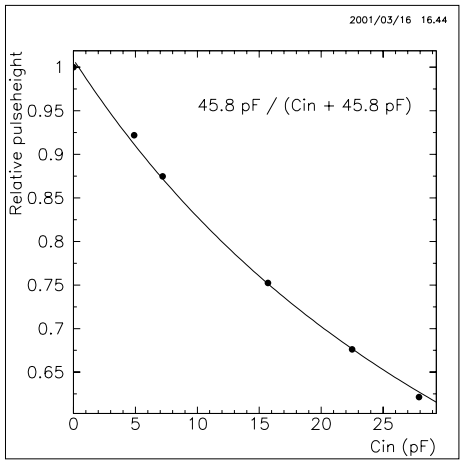

Figure 4: Relative pulseheight versus input (detector) capacitance.

3.2 Equivalent noise charge

To calibrate the measurements in terms of equivalent noise charge (ENC) we used the following calibration. The amplitude of the testpulse was 18 mV at the input of the resistive divider, which gives 1.91 mV at the coupling capacitor of 1.5 pF and is equivalent to a testcharge of 2.87 fC. For each value of the input capacitor we can now calculate the conversion gain by dividing the peak amplitude of the output signal by the injected testcharge. In the 0 pF case this gives 18.3 mV/2.87 fC = 1.02 mV per 1000 electrons. The equivalent noise charge is obtained at each value of the input capacitor by dividing the rms output noise voltage by the corresponding conversion gain.

Fig. 5 shows the noise behaviour of the frontend versus input capacitance. The noise results, represented by the open circles, are the mean values over all sample points. However, the capacitances of the input-pad, bond wire and pcb-pad, the sum of which is estimated to amount to 3 pF, should be accounted for.

The full circles in Fig. 5 represent data that are shifted over 3 pF. A straight line fit to these shifted data, represented by the solid line in Fig. 5, results in a noise slope of 45.3 electrons/pF.

Realistic noise measurements should only be corrected for the capacitance of the pcb, which is estimated to be 2 pF. The final result of a fit to our corrected data yields: 706 + 45.3 electrons/pF. A straight-line fit to results of noise simulations of the circuit, performed with Hspice using mosfet model49 and noisemodel nlev=2, yields the line 609 + 40.9 e^-/pF, as represented by the dashed line. The difference between data and simulations is expected to be due to noise from the environment in which the measurements

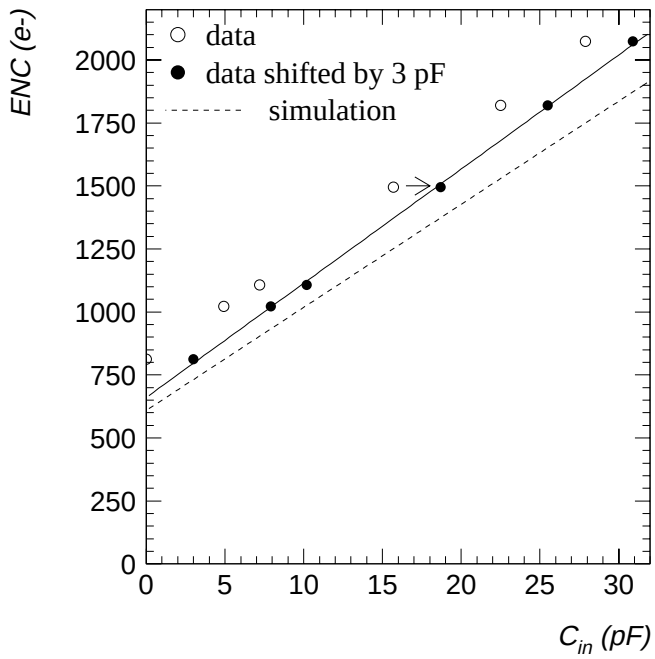

Figure 5: Equivalent noise charge versus input (detector) capacitance. The open circles represent the measurements. The solid circles are the result of a shift of 3 pF of the measurements to account for the capacitances of the input-pad, bond wire and pcb-pad. The solid (dashed) line represents the result of a straight-fit to the shifted data (simulation results).

were performed. Our values are compared to those of measurements by Edgar Sexauer (page 87 of [2]) in Table 2. The main noise contribution comes from the preamp NMOS

Table 2: Noise figures

	Noise offset $[e^-]$	Noise slope $[e^-]$
NIKHEF measurements	706	45.3
NIKHEF simulations	609	40.9
Thesis E.Sexauer	409	38

input transistor. To calculate the noise slope the $1/f$ noise contribution can be neglected for an input transistor with a big area. Remains the thermal noise contribution given by [3]

$$ENC = \frac{e}{q} \cdot \sqrt{\frac{\Gamma}{T_s} \cdot \frac{(1+\eta)kT}{3g_m}} \, [e^-/F]$$

with

- $q = 1.6 \cdot 10^{-19}$ C, $k = 1.38 \cdot 10^{-23}$ J/K, $T = 293$ K
- Γ is the excess noise factor; value between 1 and 1.5 (see Ref.[3] and [4])
- T_s is the peaking time of the shaper; ~ 30 ns
- $\eta = \frac{g_{mb}}{g_m} = \frac{2.71 \cdot 10^{-3}}{6.75 \cdot 10^{-3}}$ is the ratio between the bulk-to-channel and gate-to-channel transconductances for $I_{preamp} = 350\,\mu A$ [5].

The equation above is based on the channel thermal noise formula

$$\frac{\overline{i_{ds}^2}}{\Delta f} = 4kT\frac{2}{3}(g_m + g_{mb})$$

According to Anelli [6], the factor $\frac{2}{3}$ (γ) reduces to $\frac{1}{2}$ for transistors operating in the weak inversion region, thus reducing the ENC by a factor $\sqrt{\frac{4}{3}}$.

The noise slope is calculated, see Table 3, for the two values of the excess noise factor mentioned above and for the two values of γ.

Reasonable agreement is found between the calculated value of the noise slope and the value extracted from our measurements, i.e. 45.3 e^-/pF.

Table 3: Calculated noise slope.

Γ	γ	ENC $[e^-/\text{pF}]$
1	0.5	44.9
1	0.667	51.9
1.5	0.5	55.0
1.5	0.667	63.5

4 Characteristics

4.1 Settings

The 5 bias settings of the Beetle1.0 FrontEnd chip have been varied over the ranges specified in Table 4. In this way we scan the BeetleCO10 chip for the optimal bias settings regarding the pulse shape characteristics. An input pulse corresponding to a 1.49 MIP signal (17900 electrons) is provided at the FrontEnd input.

Table 4: Ranges and stepsizes used for the bias parameters in the scan of the characteristics of the Beetle1.0 FrontEnd chip.

Bias parameter	Range	Step-size
I_{preamp}	$200 - 500\,\mu$ A	$75\,\mu A$
I_{shaper}	$50 - 200\,\mu$ A	$37.5\,\mu A$
I_{buffer}	$50 - 200\,\mu$ A	$75\,\mu A$
$V_{preamp\,feedback}$	$0 - 1.5$ V	0.3 V
$V_{shaper\,feedback}$	$0 - 1.5$ V	0.375 V

4.2 Fitting

Important FE-chip characteristics are the gain and the rise and fall time of the pulse shape. These chip characteristics are extracted from the data obtained with the bias parameter scan. For each bias setting a data file contains an average pulse shape of 1000 sample points with error bars. A parabola has been fitted through the peak of the pulse, which defines the pulse amplitude $A\,[V]$ at the corresponding time $t_{top}\,[s]$. Next the rise time is calculated using the moments at which the amplitude of the pulse amounts to 90% and 10 % of A, respectively:

$$t_{rise} = t_{90\%} - t_{10\%}\ [s].$$

The tail of the peak has been characterized by the quantity residue, defined as the relative

amplitude at 25 ns after the maximum of the pulse:

$$residue = \frac{A[t_{peak}+25\ ns]}{A[t_{peak}]} * 100\%.$$

The distributions of extracted chip characteristics are shown in Fig. 6: the rise time varies between 20 and 100 ns, while the values for the residue lie, Gaussian-like distributed, in the range 20-85 %. The remarkable peak between 90 and 99 % corresponds to bias settings in which the shaper voltage, V_{fs}, amounts to 1.5 V, causing the DC feedback of the shaper not to work properly. The mutual relations between parameters describing the chip characteristics are shown in Fig. 7. Some bias settings combine fast timing, i.e. small values for rise time and residue, with sufficient amplification. Settings leading to a slow response, i.e. t_{rise} $\geq$45 ns and residue$\geq$65 %, feature a considerably larger gain.

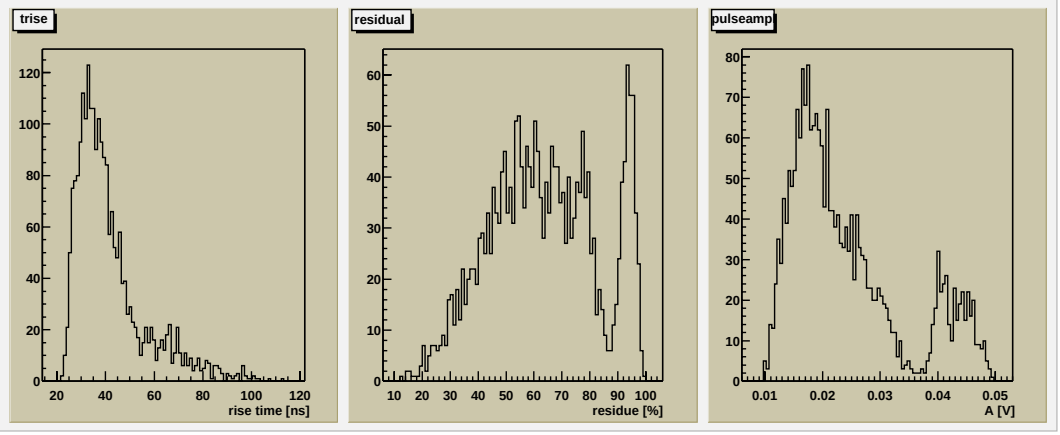

Figure 6: Histograms of the extracted FE characteristics: rise time (left), residue (middle) and amplitude (right).

4.3 Measurement and simulations

4.3.1 BeetleFE10

The first submit in the 0.25 micron technology for the Beetle chip development resulted in a test chip with three different preamp-shaper stages. Test results of this BeetleFE10 are compared with two chips from the second submit (Beetle10 and BeetleCO10). Therefore the bias settings of the different chips have to be consistent. The results shown in Table 5 reveal some differences. The first three measurements can be compared and display a discrepancy in the rise and fall time. The BeetleFE10 exhibits undershoot, while the BeetleCO10 does not with compatible bias settings. It has to be noted that the input transistor of the preamp in the second submit has extra substrate contacts in the layout.

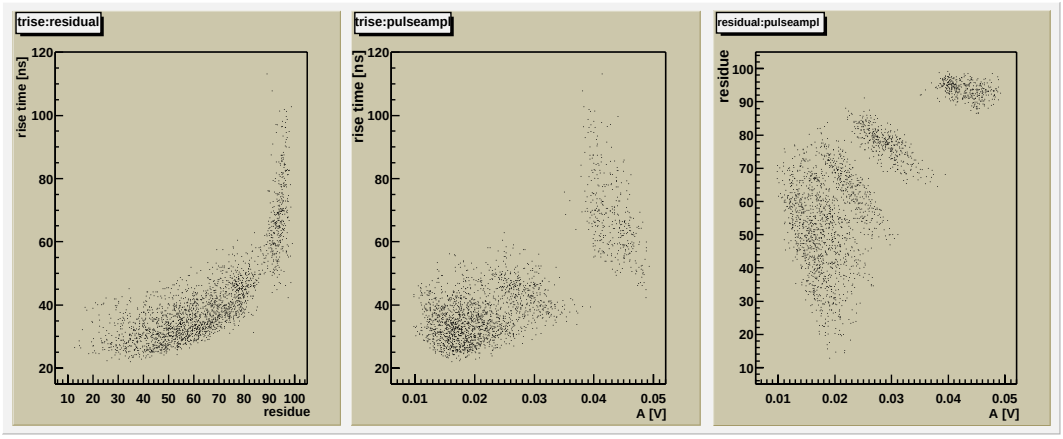

Figure 7: Scatter plots of the measured FE characteristics: rise time versus residue (left), rise time versus amplitude (middle) and residue versus amplitude (right)

Table 5: NIKHEF and Heidelberg measurements on BeetleFE10 (set 4 [7],[8]) and Beetle10 [9] compared with measurements on BeetleCO10.

Beetle	measured at	V_{fp}	V_{fs}	I_{pre}	I_{sha}	I_{buf}	$MIP(*)$	t_{rise}	t_{fall}	$residue$	A	C_{input}
		$[V]$	$[V]$	$[\mu A]$	$[\mu A]$	$[\mu A]$		$[ns]$	$[ns]$	[%]	$[mV]$	$[pF]$
FE10	Nikhef	1	0.5	260	100	100	3	12.2	23.87 (u)		16	10+(10 a 15)
CO10	Nikhef	1.125	0.6	275	87.5	125	1.49	32.5		50.5	19.9	3
FE10	Heidelberg	1	0.5	350	80	100	1	25.6 (22.8)	(u)		22.3 (19.9)	10+?
10	Heidelberg	0	0	500	80	100	1	30 (19)	(u)		16 (19.2)	?
CO10	**Nikhef**	0	0	500	87.5	125	1.49	28.0		27.4	19.4	3

(u)=undershoot, (...) =simulation value, (*) 1 MIP=12000 electrons

But this is not expected to have a significant influence in the FE behaviour. A possible cause of the discrepancies could be that the various test set-ups are not completely identical. We think of differences in load capacitances at the input and output.

The last two rows in Table 5 show similar characteristics for the Beetle10 and BeetleCO10 chip measured in Heidelberg and at NIKHEF. One of the differences is the undershoot of the pulse shape in the Beetle10 measurement, an effect that is not vissible in the BeetleCO10 measurement. This has to be investigated further in the near future.

Two pulse shapes, measured with the BeetleCO10 and used in the above comparison with other measurements, are shown in Fig. 8.

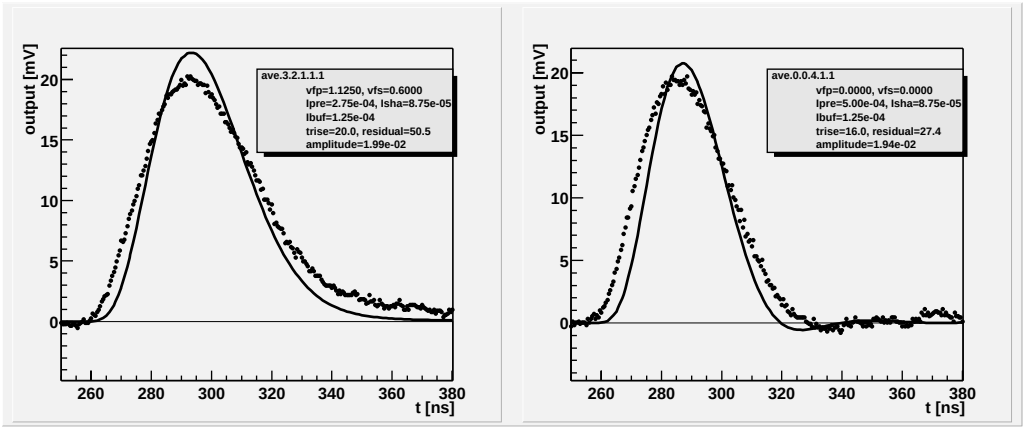

Figure 8: Test pulse measured with BeetleCO10 with bias settings compatible with the NIKHEF (BeetleFE10) and Heidelberg (Beetle10) measurements. The solid curves represent the results of the simulations.

4.3.2 BeetleCO10

The bias settings that result in a good FE performance according to the LHCb requirements are extracted from the settings scan (see section 4.1). We find 8 bias settings resulting in a rise time < 25 ns and residue $< 30\%$. Two of these "fast" pulse shapes, one with and one without undershoot, are shown in Fig. 9. The corresponding chip characteristics and bias settings are shown in the inset.

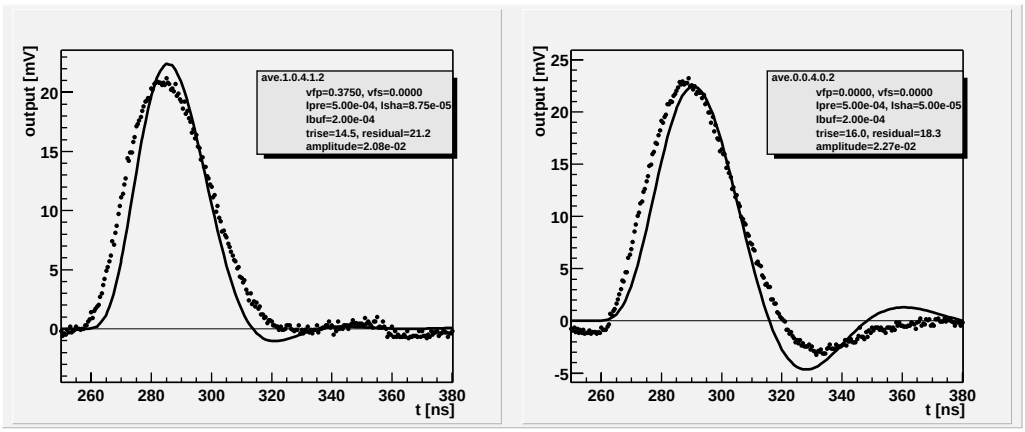

Figure 9: Dedicated bias settings of BeetleCO10 producing a fast pulse without and with undershoot. The solid curves represent the results of the simulations.

Important for understanding and future development of the chip is the compatibility

with design software simulations [5]. For the simulations a testbench schematic is used with realistic impedances at the input and output of the BeetleCO10. An input capacitance of 3 pF represents the traces of the Printed Circuit Board. The output termination of 30 pF represents the probe/wire capacitance. Results of simulations on the extracted layout file, as shown in Figs. 8 and 9, are in good agreement with the measurements.

5 Radiation hardness

5.1 Experimental conditions

The LHCb readout electronics will be placed at 5 cm from the LHC beams and will suffer from radiation damage. LHCb requires radiation tolerance of the readout electronics upto 10 Mrad(SiO_2) total dose in an LHCb environment of 2 MRad/year [10]. The total ionisation dose (TID) effect on the BeetleCO10 is tested, which is the first irradiation test in the development of the Beetle.

For the irradiation test a calibrated X-ray facility [11] is used with a spectrum centered at 10-20 keV. The dose rate can be changed by adjusting the tube current and supply voltage. The test chip is positioned at 3 cm from the X-ray source with 40 kV supply voltage, 19 mA tube current and an irradiation curve

$$\text{DoseRate (rad}(SiO_2)\text{/min)}=68+529.13*I_{tube}(\text{mA})$$

This results in a dose rate of 10.12 kRad/min. The chip is irradiated in two intervals; first 3 hours of irradiation giving ≈1.8 MRad, followed by an additional 13.5 hours irradiation bringing the total dose to 10 Mrad. During irradiation the chip was biased at its default setting using a 2.5 V battery.

5.2 Radiation damage observed

After irradiation the peak value of the output signal of the Beetle1.0 FrontEnd chip was reduced from 18 mV to ≈2 mV when using the default settings, while the pulse shape was unaltered. The full output amplitude could be retrieved by lowering the voltage of the preamplifier feedback (V_{fp}) to 0.3 Volts, thereby increasing the conductance of the p-channel feedback transistor, see Fig .10.

For p-channel mosfets, radiation damage leads to an increased threshold voltage [12]. The threshold shift for pmos transistors is about 30 mV after 10 Mrad. Also the large nmos input transistor shows a threshold shift of about 15 mV. However, the expected total shift in threshold of 45 mV can not explain the large change in V_{fp} that is needed. Further tests and simulations showed that at the default settings the feedback transistor of the preamplifier is switched off ($V_{gs} > 0$, pmos!). The dc feedback is then maintained by the (very small) leakage current of the pmos transistor. During irradiation positive charges

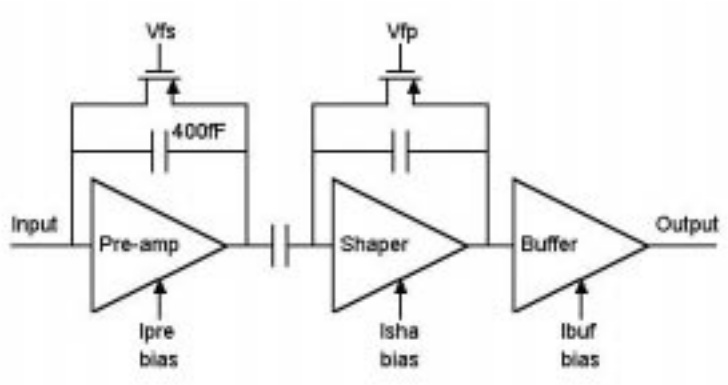

Figure 10: Details of preamp.

are trapped in the SiO_2 layer which reduce the leakage current. The dc feedback is now no longer existent and the baseline of the amplifier drifts into saturation. By lowering V_{fp} the feedback transistor is operated again in (very) weak inversion. So operation of the feedback after irradiation is not guaranteed by the design.

5.3 Saturation of the preamp

The performance of the FE under extreme hit rates is examined. The occupancy is defined as the percentage of channels per triggered event which has non-zero data, taken over a group of channels with the highest occupancy. We have chosen to test at the maximum value, i.e. an occupancy of 1.5% [10], which corresponds to a hit rate of 0.6 MHz.

The calculated margin of the preamp for piled-up events is 83 MIP (for a feedback capacitance of 400 fF and 1 MIP= $12000e^-$). To retain linearity for a 10 MIP signal the margin reduces to 73 MIP.

A hit rate of 1 MHz (2.5 % occupancy) is used in the measurements and simulations with an input pulse equal to 1 MIP . The maximum time constant τ =C_{fb}· R_{fb} of the preamp feedback at which saturation just occurs can be determined with

$$\tau = \frac{-T}{\ln(1-\frac{1}{m_M+1})}\ [\mathrm{s}],$$

where T [s] is the minimum hit rate period and m_M the required margin in MIP. For a strip occupancy of 1 MHz one finds $\tau_{max} = 83.5\ \mu$s. According to the current design specs the time constant is 8 μs [2]. However, the simulations and measurements show similar results, as shown in Figs. 11 and 12, respectively.

Clearly visible is the effect of saturation of the preamp after 270 μs; the amplitudes of the output pulses are reduced by ≈20 %. The time constant can be extracted from Fig. 12. After 265 μs saturation of the preamp is reached, causing the dynamic range to

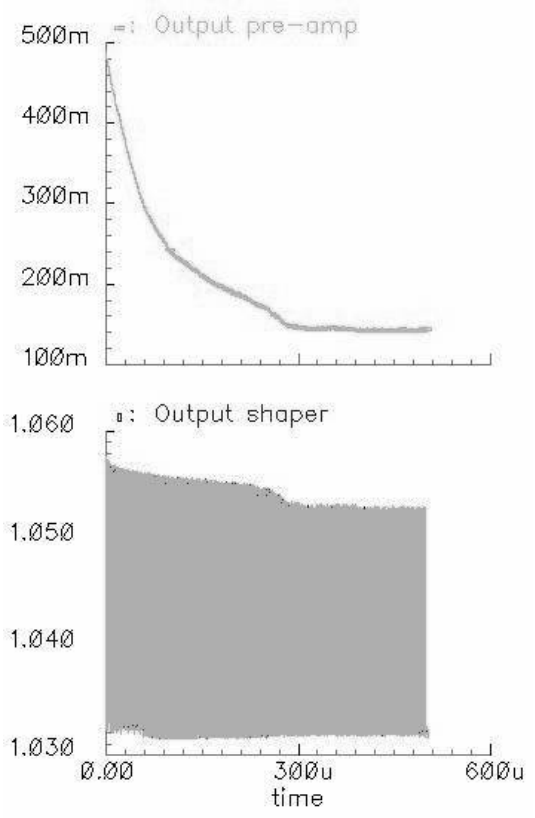

Figure 11: Simulation of saturation. Output of preamplifier (top) and shaper (bottom).

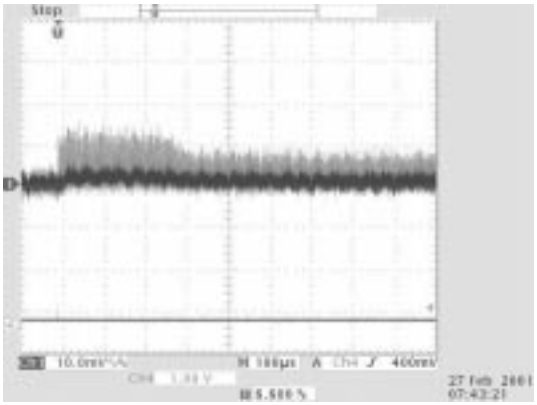

Figure 12: Measurement of saturation in the output of Beetle1.0 FrontEnd.

be reduced from 83 to $\leq$1 MIP. This corresponds to a time constant τ of 60 μs, which is significantly more than the design specification of 8 μs, mentioned above. It has to be noted that V_{fp}=0 V already biases the feedback transistor to its lowest value, which leaves no space for tuning. After irradiation the feedback resistance increases, as discussed in the previous section. So there is a danger of saturating the preamp at high particle fluxes.

6 Conclusions

The results presented in this report can be summarized as follows:

- *noise characteristics*
  The measured values for the equivalent noise charge are 706 + 45.3 e^-/pF. The calculated value for the slope lies in the range 44.9-63.6 e^-/pF, so in reasonable agreement with the experimental value. For the input capacitance of the preamplifier a value of 45.8 pF is found.

- *pulse shape*
  Pulse shape characteristics are investigated for a wide range of bias settings. Settings, featuring fast timing ($t_{90\%}$-$t_{10\%}$=t_{rise} $\leq$ 25 ns and residue$\leq$ 30 %), with and without undershoot, are found.

- *measurements versus simulations*
  Good agreement is found between the data and simulations that take realistic impedances at the input and output of the frontend into account.

- *radiation hardness*
  Radiation hardness has been investigated by exposing a biased Beetle1.0 FrontEnd chip to 10 Mrad (SiO_2) of X-rays. Afterwards, at the the default settings, the output signal turned out to be reduced from 18 to $\approx$2 mV. This is believed to be due to an increased threshold voltage of the p-channel feedback transistor of the preamplifier. Moreover, the present operation point of the feedback transistor lies at the extreme of its adjustable range. This issue needs improvement in the next design.

- *performance under high hit rate*
  Possible saturation of the preamp under high hit rates is investigated. Measurements and simulations result in a time constant in the order of 60-80 μs, while the design goal is 8 μs.

The layout of the preamplifier has to be modified in order to circumvent the problems mentioned above. Various approaches are possible like substitution of the PMOS feedback by a series of edgeless NMOS transistors, including an extra level shifting stage

for the PMOS feedback transistor or creating an additional power point in-between the positive and negative rail. These, and other possible modifications will be evaluated and implemented shortly.

Acknowledgements

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