Beetle − A Radiation Hard Readout Chip for the LHCb−Experiment

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Chip Architecture

The *Beetle* ASIC is a 128 channel pipelined readout chip which will be used in the silicon vertex detector and the silicon tracker of the LHCb experiment at the future LHC collider. It is also an option for the ring imaging Cherenkov counters in case of multi-anode photomultiplier readout.

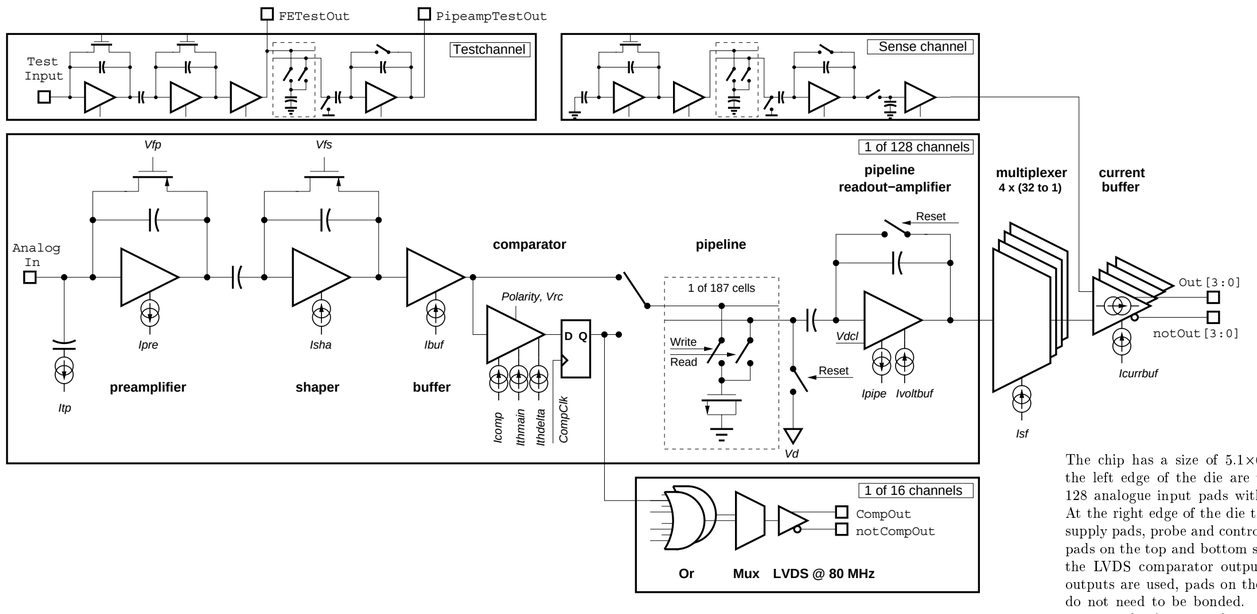
The chip can be operated as an analogue or alternatively as a binary pipelined readout chip and provides in addition prompt binary information of the front-end pulse discrimination. It implements the basic RD20 front-end electronics architecture [1, 2, 3]. Each channel consists of a low-noise charge-sensitive preamplifier, an active CR-RC pulse shaper and a buffer. They form the analogue front-end.

A comparator discriminates the front-end's output pulse. The threshold is adjustable per channel with a resolution of 5 bits and input signals of both polarities can be processed. Four adjacent comparator channels are grouped by a logic OR, latched, multiplexed by a factor of 2 and routed off the chip via low voltage differential signalling (LVDS) ports at 80 MHz.

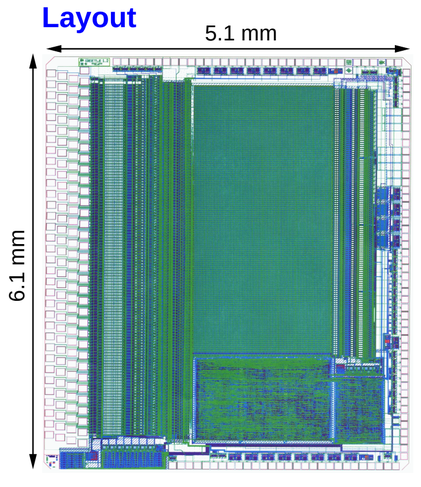
The memory for intermediate storage (pipeline) is realized as a switched-capacitor array of 130 × 187 cells, using the gate oxide capacitance of a transistor. Either the shaper- or the comparator output is sampled with the LHC bunch-crossing frequency at 40 MHz into the pipeline. The memory provides a programmable latency of maximum 160 clock periods (4 μs at 40 MHz sampling frequency) and integrates a derandomising trigger buffer of 16 stages which enables the readout of 16 consecutive events without dead time.

A resetable charge-sensitive amplifier (pipeamp) retrieves the stored signal from the pipeline and transfers it to an (analogue) multiplexer for serialisation. The multiplexer can operate in three different modes carrying the 128 channels on either 1, 2 or 4 output ports. Within a readout time of minimum 900 ns, differential current drivers bring the serialised data off chip. The output of a sense channel is subtracted from the analogue data to compensate common mode effects.

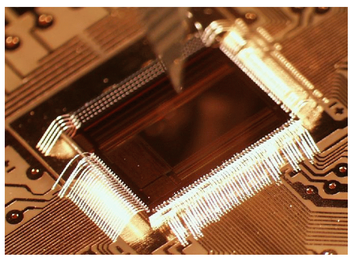
All amplifier stages are biased by forced currents. On-chip digital-to-analog converters (DACs) with 8 bit resolution generate the bias currents and voltages. For test and calibration purposes a charge injector with adjustable pulse height is implemented on each channel. The bias settings and various other parameters like the trigger latency can be controlled via a standard I^2C-interface [4]. All digital control and data signals, except those for the I^2C-ports, are routed via LVDS ports.



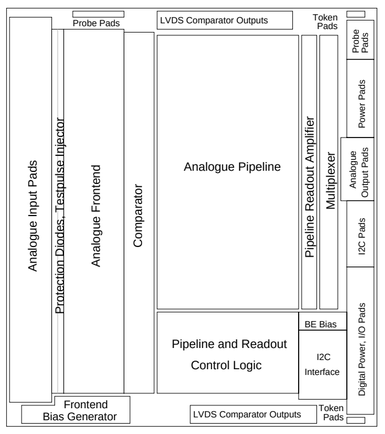
Layout



The chip has a size of 5.1×6.1 mm^2. Located at the left edge of the die are the fourfold staggered 128 analogue input pads with a pitch of 40.24 μm. At the right edge of the die the output pads, power supply pads, probe and control pads are placed. The pads on the top and bottom side of the chip provide the LVDS comparator outputs. If no comparator outputs are used, pads on the top and bottom side do not need to be bonded. This allows an overall input pitch of 50 μm when mounting several chips side by side.



Floor Plan

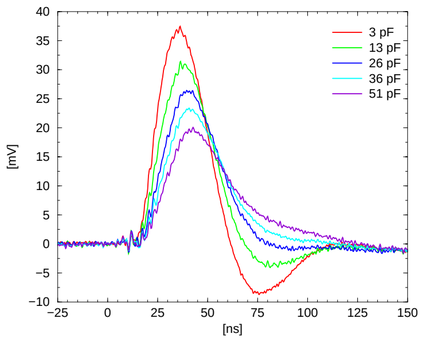


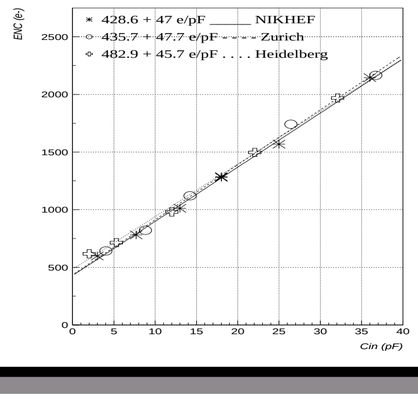
Front−end

The analogue front-end is formed by a charge-sensitive preamplifier, an active CR-RC shaper and a source-follower as buffer. Preamplifier and shaper use folded-cascode amplifier cores with an NMOS input transistor (W/L = 3744/0.42) in case of the preamplifier and a PMOS input transistor in case of the shaper.

The shape of the front-end pulse can be chosen according to the specific requirements of the application. The minimum risetime (10-90%) is well below 25 ns, the remainder of the peak voltage after 25 ns can be adjusted to less than 30% for load capacitances $\leq$ 35 pF.

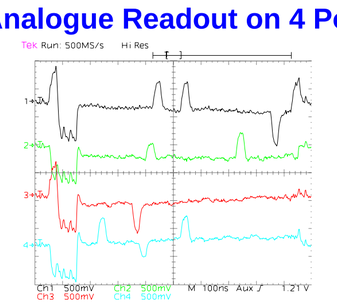
The equivalent noise charge (ENC) of the front-end has been measured as $\mathrm{ENC} = 497\,e^- + (48.3\,e^-/\mathrm{pF}) \cdot C_{in}$.



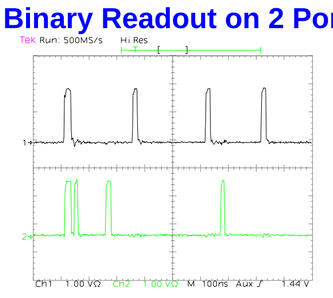


Readout Modes

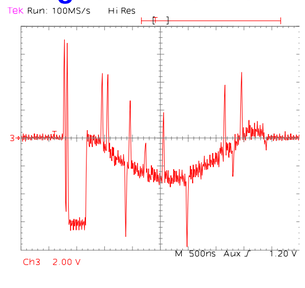
Analogue Readout on 4 Ports



Binary Readout on 2 Ports



Analogue Readout on 1 Port



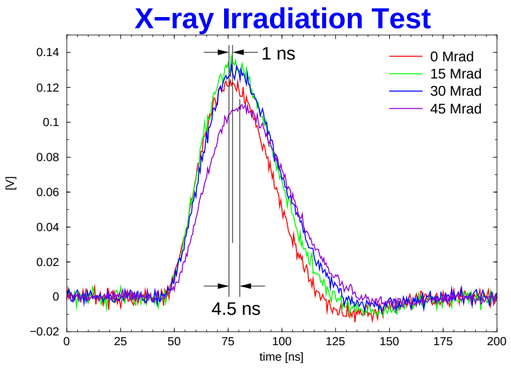
Radiation Hard VLSI Design

The requirements on the *Beetle* chip concerning radiation hardness are defined by it's use in the silicon vertex detector. The expected dose rate is 2 Mrad per year. Several measures have been taken to assure the resistance against total ionising dose (TID) as well as single event effects.

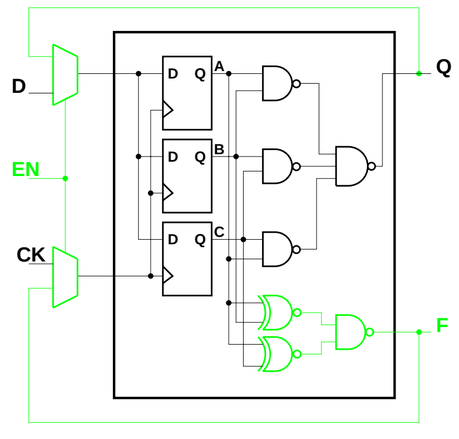
The chip is fabricated in a standard CMOS deep-submicron technology featuring a 0.25 μm lithography. The thin gate oxide of $\approx$ 62 Å reduces a shift in the transistor threshold voltage under irradiation. The consistent use of enclosed NMOS transistors eliminates "end-around" leakage currents. Analogue stages are biased with constant currents instead of voltages. This establishes a total ionising dose radiation hardness in excess of 10 Mrad. An X-ray irradiation test up to an accumulated dose of 45 Mrad showed only minor degradations in the analogue performance and no functional failure of the chip.

Single Event Latch-up (SEL) is suppressed due to the implementation of guard-rings. The continuous use of triple-redundant logic ensures a robustness against Single Event Upset (SEU), which is expected to occur at a rate of 1 μHz per chip in the vertex detector of LHCb. Static parts of the logic, i.e. bias and configuration registers, implement a self-correction mechanism against SEU-induced errors.

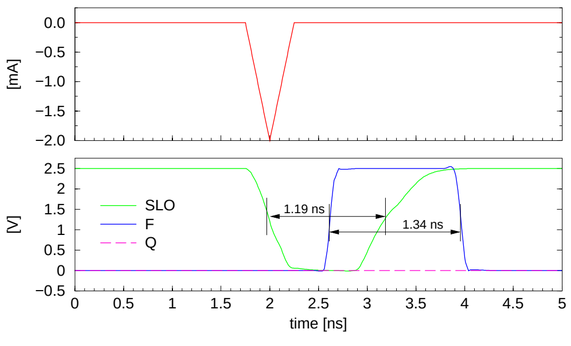
X−ray Irradiation Test



SEU Protection: Triple−Redundancy



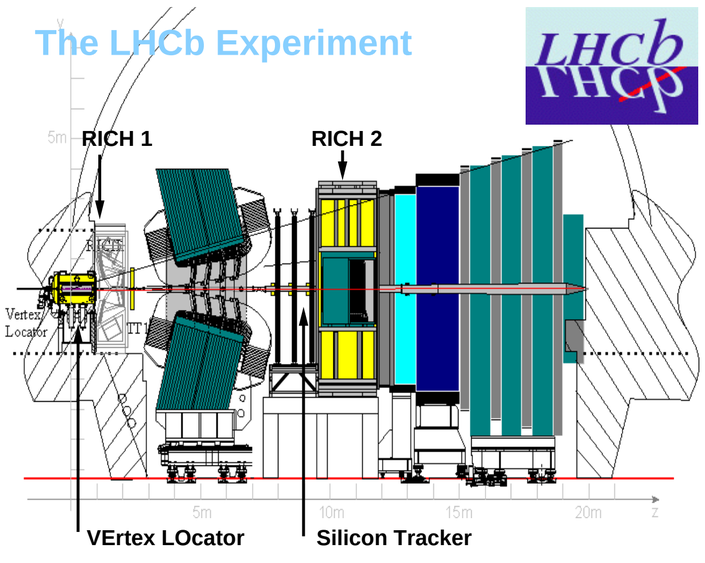
self−triggered correction



Simulation result of a self-triggered correction process. A total charge of 500 fC has been injected as a triangular pulse to a sensitive node (SLO). The disturbance takes 1.2 ns. The clock (F) triggering the self-correction has a width of 1.34 ns. The flip-flop output Q remains unchanged all the time.

Applications

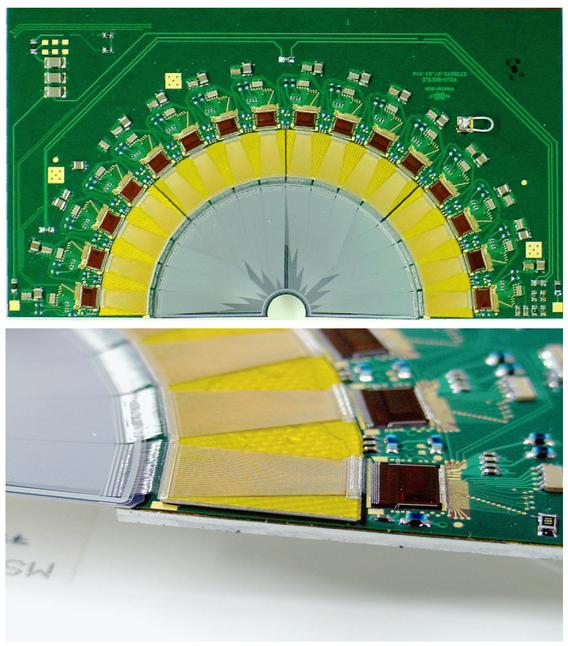
The LHCb Experiment



LHCb is a next-generation experiment to study B-physics in pp-collisions at LHC. It is a precision measurement experiment for $\mathcal{CP}$-violation and rare decays in the B-meson system, being able to perform redundant measurements of all angles in the unitarity triangle and to test the Standard Model of electroweak interaction with unpredecedented precision.

The *LHCb*-experiment plans to operated at a pp centre-of-mass energy of 14 TeV and a bunch crossing frequency of 40 MHz with an average luminosity of $\mathcal{L} = 2 \times 10^{32}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$. The $b\bar{b}$-production cross section $\sigma_{b\bar{b}}$ is $\approx 500\,\mu$b, which is far larger than at any existing machines. From the total inelastic cross section $\sigma_{tot} = 100$ mb the ratio of events with b quarks is 5×10^{-3}. Hence, at *LHCb* 100,000 B-mesons/s are produced at an interaction rate of 40 MHz. They are hidden in 200 times more non-B events.

Vertex Detector Hybrid



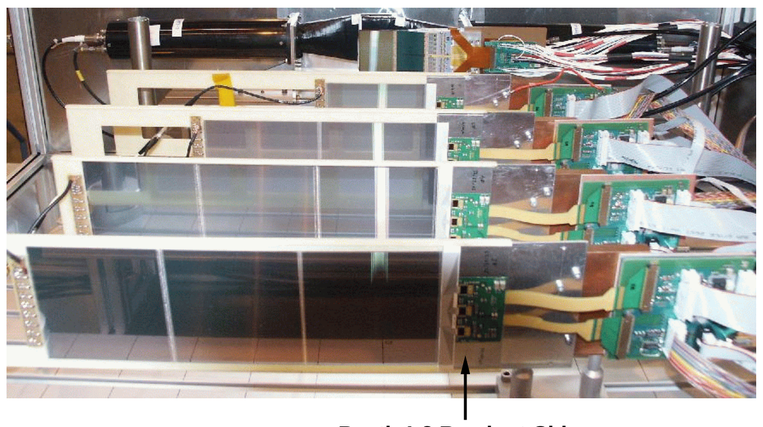
Vertex Detector

The silicon sensors of the vertex detector use n-strips on n-bulk material with AC coupling to the electronics and polysilicon biasing. Due to radiation damage it is expected, that they have to be replaced every 3 years. The sensors have a half-disc shape with azimuthal (r-measuring) or radial (ϕ-measuring) strips. This layout has been chosen to optimise the speed of the pattern recognition in the L1 trigger. The number of strips per half-disc is 2,048 with varying length to restrict the occupancy below 1% everywhere.

Silicon Tracker

The Silicon Tracker uses rectangular sensors with p-strips on an n-bulk. In order to minimise the number of readout channels, a large strip pitch of $\sim$ 200 μm together with long readout strips of 22 cm has been chosen. A ladder is formed by two silicon sensors, which are read out by 3 *Beetle* chips. For one station of the tracking system, even ladders consisting of 3 silicon sensors with a total strip length of 33 cm are being constructed.

Silicon Tracker Hybrids (Testbeam Setup)



References

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[3] R. Horrisberger et al., A novel readout chip for silicon strip detectors with analog pipeline and digitally controlled analog processing, NIM A326 (1993) 92

[4] The I^2-bus and how to use it, Philips Semiconductors, 1995