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Development, Optimisation and Characterisation of a Radiation Hard Mixed-Signal Readout Chip for LHCb

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Zusammenfassung

Der *Beetle* Chip ist ein strahlenharter, 128-Kanal-Auslesechip für Silizium-Streifen-Detektoren. Die analoge Eingangsstufe besteht aus einem ladungsempfindlichen Vorverstärker, dem ein CR-RC Pulsformer folgt. Der analoge Speicher besteht aus einer Kapazitätsmatrix und gewährleistet eine Latenzzeit von maximal 4 µs. Die Daten der 128 analogen Kanäle werden zusammengefasst und über vier Stromtreiber in 900 ns vom Chip übertragen. Neben dem Signalpfad, der durch den analogen Speicher führt, stellt der *Beetle* Chip eine schnelle Komparatorentscheidung des geformten Eingangspulses bereit.
Innerhalb der vorliegenden Arbeit wurden Teile des strahlenharten *Beetle* Auslesechips für das LHCb Experiment entwickelt. Die Gesamtleistungsmerkmale des Chips wie Rauschen, Stromverbrauch, Eingangsladungsrate wurden verbessert wie auch die Beseitigung von Fehlern, so dass der *Beetle* alle Anforderungen des Experiments erfüllt. Ein weiterer Hauptbestandteil dieser Arbeit war die Charakterisierung des Chips. Neben den ausführlichen Messungen der Leistungsmerkmale des Chips wurden mehrere Bestrahlungstests und ein Single Event Upset-Test durchgeführt. Eine Langzeitmessung mit einem Silizium-Streifen-Detektor ist ebenfalls Bestandteil dieser Arbeit wie auch die Entwicklung und der Test eines Messaufbaus zur Durchführung erster Serientests.
Der *Beetle* Chip zeigte kein funktionales Versagen und nur leichte Verschlechterungen im analogen Verhalten nach einer Bestrahlung bis 130 Mrad. Der *Beetle* Chip erfüllt alle Anforderungen des Vertex-Detektors (VELO), des Trigger-Spurdetektors (TT) und des Inneren Spurdetektors (IT) und ist somit bereit für den Start von LHCb Ende 2007.

Abstract

The *Beetle* chip is a radiation hard, 128 channel pipelined readout chip for silicon strip detectors. The front-end consists of a charge-sensitive preamplifier followed by a CR-RC pulse shaper. The analogue pipeline memory is implemented as a switched capacitor array with a maximum latency of 4 µs. The 128 analogue channels are multiplexed and transmitted off chip in 900 ns via four current output drivers. Beside the pipelined readout path, the *Beetle* provides a fast discrimination of the front-end pulse.
Within this doctoral thesis parts of the radiation hard *Beetle* readout chip for the LHCb experiment have been developed. The overall chip performances like noise, power consumption, input charge rates have been optimised as well as the elimination of failures so that the *Beetle* fulfils the requirements of the experiment. Furthermore the characterisation of the chip was a major part of this thesis. Beside the detailed measurement of the chip performance, several irradiation tests and an Single Event Upset (SEU) test were performed. A long-time measurement with a silicon strip detector was also part of this work as well as the development and test of a first mass production test setup.
The *Beetle* chip showed no functional failure and only slight degradation in the analogue performance under irradiation of up to 130 Mrad total dose. The *Beetle* chip fulfils all requirements of the vertex detector (VELO), the trigger tracker (TT) and the inner tracker (IT) and is ready for the start of LHCb end of 2007.

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Introduction

In the generally accepted Big Bang theory of the formation of our universe, one conclusion is that equal amounts of matter and antimatter were created in the beginning. There is good experimental evidence that everything we observe in the universe is made of matter rather than antimatter. This is a very surprising result. Interestingly, Heavy Flavour Physics and in particular the study of $\mathcal{CP}$-violation may provide a key to the puzzle why all the antimatter has disappeared.

$\mathcal{CP}$-violation was discovered in decays of neutral kaons in 1964. It was a small effect, but it showed that fundamental interactions are not necessarily invariant when matter is replaced by antimatter. Later it became clear, that $\mathcal{CP}$-asymmetries can be large for decays of B-mesons. Therefore, precision measurements of such decays allow a detailed study of $\mathcal{CP}$-violation mechanism. Of particular interest is the search for $\mathcal{CP}$-violating effects which are caused by physics beyond the Standard Model. Cosmological arguments suggest that such contributions exist.

Decays of heavy quarks can be studied at hadron colliders like the Large Hadron Collider (LHC), where the production cross section is large and particles containing such quarks are produced at high rates. In the LHCb experiment, which will start in 2007 with data taking, proton beams will collide with a bunch crossing rate of 40 MHz and a centre-of-mass energy of 14 TeV. Within these collisions B-mesons will be produced at a rate of 100 kHz. Therefore, LHCb will observe more B-mesons in one year of data taking than the currently running B-factories over their entire lifetime. In addition, also heavier B-hadrons are produced which are not accessible by experiments at lower energies. LHCb is optimised to exploit the huge B-physics potential of LHC. Precision measurements of $\mathcal{CP}$-violation in many different channels will over-constrain the parameters of the Standard Model. Any inconsistency which might show up would be a clear sign for New Physics.

One requirement to the LHCb experiment is the possibility to analyse all interactions occurring in the detector. All events which are accepted by the first level trigger system, will be read out with a mean trigger rate of around 1 MHz. The high particle fluxes and event rates expected at LHCb lead to extremely high demands on the front-end readout electronics of the detector. The readout chips in the interaction region and in the innermost part around the beam pipe have to be radiation hard (up to 10 Mrad are expected for the entire lifetime of the experiment). The chips must also be able to read out a large number of channels ($\approx 450\,000$) within a very short time of 900 ns. For the silicon strip detectors of the vertex detector (VELO) and of the tracking system (TT and IT) of the LHCb experiment this is done with the *Beetle* readout chip. The basic design of the chip was defined in 1998 after the technical proposal of the LHCb experiment was presented [TP98]. In the following years the ASIC-laboratory in

Heidelberg[1] in cooperation with NIKHEF Amsterdam and the University of Oxford developed the *Beetle* readout chip. This doctoral thesis describes the development, optimisation and characterisation of the final *Beetle* readout chip for the LHCb experiment.

It is organised as follows:

A brief introduction into the theoretical background of $\mathcal{CP}$-violation is given in chapter 1, with special focus on B-meson decays. A short description of the LHCb experiment and its sub-detectors is presented in the following chapter 2.

The silicon strip detector as a detection device of particles, which will be read out by the *Beetle* chips, is discussed in chapter 3. Chapter 4 describes the basic processes induced by radiation to integrated microelectronic devices, including the consequences on the performance of the circuit.

Chapters 5 and 6 deal with the core activities of this thesis work. First, in chapter 5, after a general description of the chip's architecture, the components designed in the context of this thesis are described. This covers the front-end amplifier for the *Beetle* chip, the programmable test pulse circuity for internal testing of the analogue channels, the digital logic and the analogue bypass of the comparator, the final pipeline memory design, the improved pipeline readout amplifier, the analogue multiplexer and the implementation of a balanced analogue current output driver. In addition certain optimisations done on the current source and the Digital-to-Analogue-Converters are discussed.

Following this, chapter 6 presents the detailed characterisation of the *Beetle* front-end and the overall performance of the readout obtained during this work. Then the results of several total dose irradiation tests, an SEU-test and a long-time cosmic-ray measurement with a silicon strip detector read out with *Beetle* chips done for this thesis is described. Finally the development of a first mass production test setup is shown together with corresponding results from the wafer tests are given.

After summary and outlook the thesis concludes with an appendix of 'The *Beetle* Reference Manual'.

[1] The ASIC-laboratory in Heidelberg is a joint facility of the Kirchhoff Institute for Physics (University of Heidelberg), the Physics Institute (University of Heidelberg) and the Max-Planck-Institute for Nuclear Physics.

Chapter 1

$\mathcal{CP}$-Violation

Physics Introduction

$\mathcal{CP}$-violation was first discovered in neutral kaon decays by Christenson, Cronin and Fitch in 1964. They investigated the decay of the long-lived neutral K-meson, K_L[1], which predominantly decays into a $\mathcal{CP}$-odd three-pion final state, and found that a small fraction also decays into a $\mathcal{CP}$-even two-pion final state [Chr64]. The study of $\mathcal{CP}$-violation and the search for its origin is still one of the central issues in elementary particle physics.

The Standard Model with three quark families can naturally accommodate $\mathcal{CP}$-violation in both weak and strong interactions, but so far $\mathcal{CP}$-violation has never been detected in the strong interaction. In the Standard Model, $\mathcal{CP}$-violation in weak interactions arises from a complex phase in the unitary CKM-matrix[2], which describes the mixing between mass and flavour eigenstates of down-type quarks [Kob72]. The observed $\mathcal{CP}$-violating phenomena in the neutral-kaon system are consistent with this mechanism. However, it cannot be excluded that physics beyond the Standard Model contributes, or even fully accounts for the observed phenomena.

$\mathcal{CP}$-violation also plays an important role in cosmology. It is one of the three ingredients required to explain the excess of matter over antimatter observed in our universe [Sak67]. But the level of $\mathcal{CP}$-violation generated by the weak interaction in the Standard Model is insufficient to explain the dominance of matter in the universe [Gav94]. This calls for new sources of $\mathcal{CP}$-violation beyond the Standard Model.

Since its discovery, $\mathcal{CP}$-violation has been measured precisely in the neutral kaon system. Experimental efforts in the kaon sector will continue for some time. In the B-meson system there are many more decay modes available, and the Standard Model gives precise predictions for $\mathcal{CP}$-violation in a number of these. The B-meson system is therefore a very attractive field to study $\mathcal{CP}$-violation, and to search for hints of physics beyond the Standard Model [TP98].

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[1] Two different K-mesons are observed with strongly different life times: K_S (K-short) mesons have a life time $\tau_S = 0.895 \cdot 10^{-10}$ s, the K_L (K-long) of $\tau_L = 5.15 \cdot 10^{-8}$ s [PDG04].

[2] Cabbibo-Kobayashi-Maskawa (CKM)

$\mathcal{CP}$-violation

The CKM matrix describes the mixing of the flavour eigenstates of the quarks into their mass eigenstates and is given by

$$V_{\mathrm{CKM}} = \begin{pmatrix} V_{\mathrm{ud}} & V_{\mathrm{us}} & V_{\mathrm{ub}} \\ V_{\mathrm{cd}} & V_{\mathrm{cs}} & V_{\mathrm{cb}} \\ V_{\mathrm{td}} & V_{\mathrm{ts}} & V_{\mathrm{tb}} \end{pmatrix}. \tag{1.1}$$

The elements V_{ij} are related to the relative strengths of the transition of down-type quarks (j = d, s, b) to up-type quarks (i = u, c, t) in charged current weak interactions, normalised to $\sqrt{G_{\mathrm{F}}}$, where G_{F} is the Fermi coupling constant. A complex 3×3 matrix has in principle 18 independent parameters. General principles require unitarity which reduces the number of parameters to 9. These 9 complex matrix elements are not independent from each other and can further be reduced to a set of four parameters: three real rotation angles and one complex phase. Among various parametrisations, a very convenient one for many applications is that proposed by Wolfenstein [Wol83]:

$$V_{\mathrm{CKM}} = V^{(3)}_{\mathrm{CKM}} + \delta V_{\mathrm{CKM}} \tag{1.2}$$

where the four independent parameters A, λ, ρ and η are used. The expansion up to third order in λ is given by

$$V^{(3)}_{\mathrm{CKM}} = \begin{pmatrix} 1 - \frac{1}{2}\lambda^2 & \lambda & A\lambda^3 (\rho - i\,\eta) \\ -\lambda & 1 - \frac{1}{2}\lambda^2 & A\lambda^2 \\ A\lambda^3 (1 - \rho - i\,\eta) & -A\lambda^2 & 1 \end{pmatrix}. \tag{1.3}$$

The parameter λ is given by the sine of the Cabibbo angle [Cab63], measured to be 0.2243 ± 0.0016 [PDG04] from decays involving s-quarks. $\mathcal{CP}$-violation is associated with a non-zero value of the parameter η.

For a qualitative discussion of $\mathcal{CP}$-violation in B-meson systems, $V^{(3)}_{\mathrm{CKM}}$ is sufficient and the second term δV_{CKM} is usually ignored. For $\mathcal{CP}$-violation in K^0-$\overline{\mathrm{K}}^0$ oscillations, the correction to V_{cd} is important. For B-meson systems, the correction to V_{td} and V_{ts} becomes relevant once the sensitivity of experiments to $\mathcal{CP}$-violation parameters becomes 10^{-2} or better.

Six of the nine unitarity conditions of the CKM matrix can be visualised as triangles in the complex plane. The two triangles relevant for the B-meson systems are shown in fig. 1.1. The related unitarity conditions are given by

$$\begin{array}{rcl} V_{\mathrm{ud}}V^*_{\mathrm{ub}} + V_{\mathrm{cd}}V^*_{\mathrm{cb}} + V_{\mathrm{td}}V^*_{\mathrm{tb}} & = & 0 \\ V_{\mathrm{tb}}V^*_{\mathrm{ub}} + V_{\mathrm{ts}}V^*_{\mathrm{us}} + V_{\mathrm{td}}V^*_{\mathrm{ud}} & = & 0\,. \end{array} \tag{1.4}$$

The two triangles become identical if δV_{CKM} is ignored.

The angles of the triangles can be extracted either indirectly by measuring the lengths of the sides, or, within the Standard Model, directly from $\mathcal{CP}$-asymmetries. Different results from the two different methods would indicate physics beyond the Standard Model.

Since λ is well known, the two triangles are completely determined by ρ and η, which can be derived from $|V_{\mathrm{cb}}|$, $|V_{\mathrm{ub}}|$ and $|V_{\mathrm{td}}|$, as seen from fig. 1.1. The parameter A is extracted from measurements of $|V_{\mathrm{cb}}|$ and λ. The values of $|V_{\mathrm{cb}}|$ and $|V_{\mathrm{ub}}|$ are extracted from various B-meson decays and are currently known to be [Nie05]

$$|V_{\mathrm{cb}}| = (41.6 \pm 0.5) \cdot 10^{-3} \tag{1.5}$$

$$|V_{\mathrm{ub}}| = (3.90 \pm 0.12) \cdot 10^{-3}\,. \tag{1.6}$$

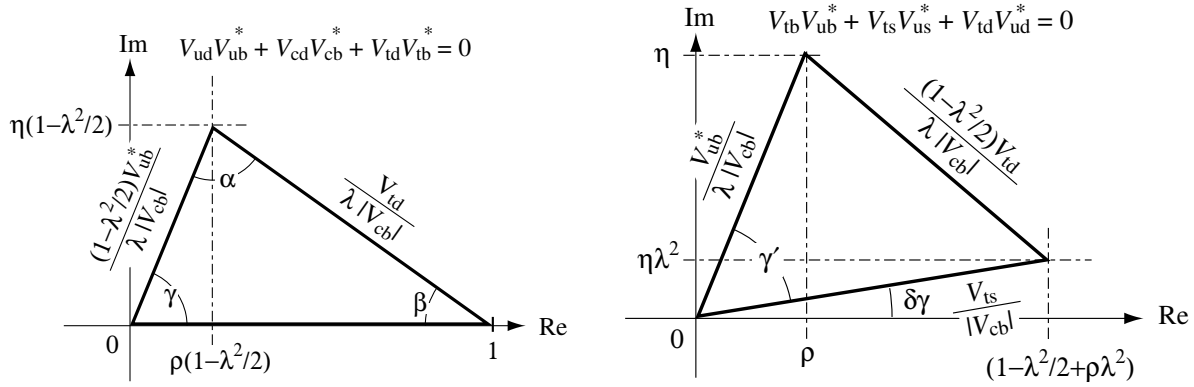


Figure 1.1: Two unitarity triangles in the Wolfenstein parametrisation with an approximation valid up to $\mathcal{O}(\lambda^5)$ [TP98].

The value of $|V_{\rm td}|$ is currently determined from the frequency of $\rm B_d^0$-$\overline{\rm B}_d^0$ oscillations. Due to difficulties in evaluating the effects of hadronic interactions, the extracted value $|V_{\rm td}|$ has a large uncertainty [Nie05]

$$|V_{\rm td}| = (8.38^{+0.32}_{-0.44}) \cdot 10^{-3} \ . \tag{1.7}$$

This situation can be improved considerably once $|V_{\rm ts}|$ is extracted from the frequency of $\rm B_s^0$-$\overline{\rm B}_s^0$ oscillations and when $|V_{\rm td}/V_{\rm ts}|$ is used instead of $|V_{\rm td}|$, since the Standard Model calculation of this ratio has a greatly reduced hadronic uncertainty.

Once ρ and η are derived from $|V_{\rm cb}|$, $|V_{\rm ub}|$ and $|V_{\rm td}|$, the angles α, β, γ and $\delta\gamma$ can be calculated. Table 1.1 shows the state-of-the art extracted angles from a global fit of ρ and η to the unitarity triangle [Nie05].

Parameter	Central	CL	
		$\pm1\,\sigma$	$\pm2\,\sigma$
ρ	0.204	$^{+0.035}_{-0.033}$	$^{+0.095}_{-0.069}$
η	0.336	$^{+0.021}_{-0.021}$	$^{+0.045}_{-0.060}$
α [deg]	98.4	$^{+6.1}_{-5.6}$	$^{+16.8}_{-11.8}$
β [deg]	22.77	$^{+0.87}_{-0.83}$	$^{+1.92}_{-2.04}$
γ [deg]	58.8	$^{+5.3}_{-5.8}$	$^{+11.2}_{-15.4}$

Table 1.1: Results of a global fit to the unitarity triangle [Nie05].

In the framework of the Standard Model, direct measurements can either be made of the angles α, β, γ and $\delta\gamma$, or of their combinations from $\mathcal{CP}$-asymmetries in different final states of B-meson decays. Well known examples are [Bur97]:

$$\begin{aligned} \beta+\gamma \quad &\text{from} \quad \rm B_d^0 \to \pi^+\pi^- \\ \beta \quad &\text{from} \quad \rm B_d^0 \to J/\psi K_S \end{aligned}$$

$$\begin{aligned} \gamma - 2\delta\gamma \quad &\text{from} \quad \mathrm{B_s^0} \to \mathrm{D_s^{\pm} K^{\mp}} \\ \delta\gamma \quad &\text{from} \quad \mathrm{B_s^0} \to \mathrm{J/\psi\phi} \\ \gamma \quad &\text{from} \quad \mathrm{B_d^0} \to \overline{\mathrm{D}}^0\mathrm{K}^{*0}, \mathrm{D}^0\mathrm{K}^{*0}, \mathrm{D_1 K}^{*0} \end{aligned}$$

where $\mathrm{D_1}$ is the $\mathcal{CP} = +1$ state of the neutral D meson. The charge-conjugated decay processes can also be used for measurements. The angle α can not be measured directly. It can be determined through the triangle relation $\alpha = \pi - \beta - \gamma$. Within the framework of the Standard Model, β, $\gamma - 2\delta\gamma$ and γ can be measured from the decay channels with very little theoretical uncertainty.

If a new flavour-changing neutral current is introduced by physics beyond the Standard Model, it possibly has a large effect on $\mathrm{B_d^0}$-$\overline{\mathrm{B}}_\mathrm{d}^0$ and $\mathrm{B_s^0}$-$\overline{\mathrm{B}}_\mathrm{s}^0$ oscillations, since the contribution of the weak interaction is second order [TP98]. In that case, the experimentally extracted values from B-$\overline{\mathrm{B}}$ oscillations of $|V_{\mathrm{td}}|$ and $|V_{\mathrm{ts}}|$ do no longer correspond to the angles defined by the CKM-matrix elements. The angles $\beta + \gamma$, β, $\gamma - 2\delta\gamma$ and $\delta\gamma$ are also affected. The results obtained from the two methods of angle measurements will no longer match.

The angle γ can be determined by using $\mathrm{B_d^0}$ decays, or by using $\mathrm{B_s^0}$ decays. Since $\mathrm{B_d^0}$-$\overline{\mathrm{B}}_\mathrm{d}^0$ and $\mathrm{B_s^0}$-$\overline{\mathrm{B}}_\mathrm{s}^0$ oscillations can be affected differently by a possible new flavour-changing neutral current, the two measurements of γ may differ.

Since only a small contribution from flavour-changing neutral current is expected in D^0-$\overline{\mathrm{D}}^0$ oscillations, γ extracted from latter decay modes would be very close to the value of the Standard Model. Therefore, the γ values that are obtained from the different decay channels will not agree.

In the Standard Model, $\delta\gamma$ is expected to be in the order of 10^{-2}, and the $\mathcal{CP}$-asymmetry in $\mathrm{B_s^0} \to \mathrm{J/\psi\phi}$ decays should be very small [TP98]. A new flavour-changing neutral current could, however, generate a large $\mathcal{CP}$-violating effect in this decay channel.

This illustrates how new physics could be detected from precise measurements of $\mathcal{CP}$-violation in various B-meson decays, combined with ρ and η determined from other B-meson decays.

Another way to search for physics beyond the Standard Model is the study of B-meson decays, which are rare or even forbidden in the Standard Model. For example, B-meson decays generated by the penguin processes are first order in the weak interaction, and their branching ratios are less likely affected by new physics. However, these decay modes may exhibit a sizeable $\mathcal{CP}$-violating effect through interference, if new physics is present [Wol94]. Similarly, a large effect could be seen in the energy asymmetry of lepton pairs produced in $\mathrm{b} \to \mathrm{s}\ell^+\ell^-$ decays [Cho96].

There are many ways to look for signs of new physics. In all cases, large numbers of both $\mathrm{B_s^0}$ and $\mathrm{B_d^0}$ mesons are required, and many different decay modes have to be reconstructed.

Chapter 2

The LHCb Experiment

LHCb[1] is a next-generation experiment to study B-physics at the European Organisation for Nuclear Research (CERN)[2]. CERN is the world's largest particle physics laboratory, situated just west of Geneva on he French-Swiss border. It has been founded in 1954 by 12 European states and has grown to 20 member states at present. At CERN the particle accelerators are located which are needed for high energy physics research. Numerous experiments have been constructed at CERN by international collaborations to make use of them.

For the precision measurements of the $\mathcal{CP}$-violation and rare B-mesons decays, the LHCb particle detector is being built, which will make use of the Large Hadron Collider (LHC) accelerator. The aim of this chapter is to give an introduction to the accelerator, to the physics perspective of the LHCb experiment and the detector itself.

2.1 The Large Hadron Collider

The LHC accelerator is a proton-proton collider. It makes use of the existing tunnel of the former Large Electron Positron (LEP) collider with a circumference of 27 km. The particle bunch crossings will occur at LHC with a rate of 40 MHz, a centre of mass energy of 14 TeV[3] and a nominal luminosity[4] $\mathcal{L}$ of $10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$. Figure 2.1 gives an overview of the whole LHC accelerator complex and the location of the four major experiments ALICE, ATLAS, CMS[5] and LHCb. ATLAS and CMS are located at interaction point 1 resp. 5 and are general-purpose detectors covering a wide range of physics. In particular they are optimised to detect the Higgs particle as well as the supersymmetric partners of the Standard Model (SM) particles. The physics program of these two detectors demands for the highest possible luminosity. The ALICE experiment will study the quark gluon plasma in heavy ion collisions[6]. LHCb is located at interaction point 8 and is dedicated to study $\mathcal{CP}$-violation in the B-mesons system. It will run at a lower luminosity of $2 \cdot 10^{32}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ to maximise the number of events with single proton–proton interactions.

[1] Large Hadron Collider beauty (LHCb) experiment

[2] Originally a French acronym for Conseil Européen pour la Recherche Nucléaire.

[3] The effectively available energy in a quark–quark collision is roughly one third of the total energy.

[4] Luminosity $\mathcal{L}$ is a measure of the collision rate. The measurable process rate is calculated from the luminosity multiplied with the cross section σ of this process.

[5] Another experiment called TOTEM is placed symmetrically on both sides of the CMS experiment.

[6] The LHC accelerator can also be used as a heavy ion collider (e.g. Pb–Pb collisions). The nominal luminosity $\mathcal{L}_{\mathrm{Pb}}$ that will occur is $1.95 \cdot 10^{27}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$.

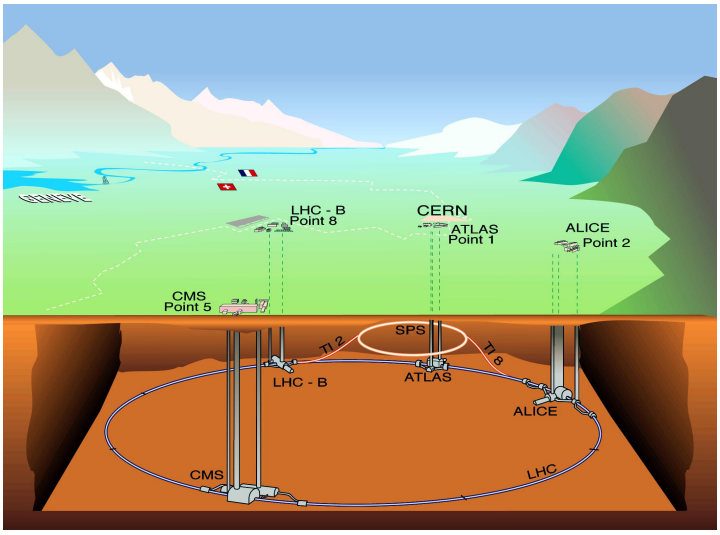


Figure 2.1: Overview of the experiment sites and location at the LHC accelerator at CERN.

The LHC design luminosity will be achieved by filling each of the two proton rings with 2 808 bunches[7] of 10^{11} particles each. The resulting large beam current of $I_{\mathrm{LHC}} = 0.53\,\mathrm{A}$ poses a challenge for the design of the LHC machine built of superconducting magnets which operate at cryogenic temperatures of 1.9 K. Both beam pipes are embedded in a single super-conducting magnet with a magnetic field of 8.3 T. This strong field is needed to keep the protons on the 27 km long circular trajectory. In the present acceleration scheme the beams will be stored at high energy for about 10 hours.

2.2 Perspective at LHCb

With the start of operation in 2007, the LHC accelerator will be by far the most copious source of B-mesons, due to the high $b\bar{b}$ cross section and the high luminosity. A variety of b-hadrons, such as B_u, B_d, B_s, B_c and b-baryons will be produced at high rate.

The LHCb experiment operates at a proton–proton centre-of-mass energy of 14 TeV and a bunch crossing frequency of 40 MHz. To generate valid trigger decisions at LHCb and to reconstruct tracks with high efficiency, the detector occupancy must be kept low. For a given detector, the minimum occupancy is achieved if only single pp-interactions are considered. The probability of n pp interactions in a bunch crossing is described by a Poisson distribution

$$P_n = \frac{\mu^n}{n!}\, e^{-\mu} \tag{2.1}$$

with a mean of

$$\mu = \frac{\mathcal{L}\,\sigma_{\mathrm{tot}}}{f_{\mathrm{eff}}} \tag{2.2}$$

where $\mathcal{L}$ is the luminosity and σ_{tot} is the total inelastic pp cross section, which is expected to be around 80 mb at LHCb energies [TP98]. f_{eff} is the effective bunch crossing frequency of

[7] 3 564 bunch positions are possible at LHC, but only 2 808 bunches are filled. 2 808 bunches will find colliding partner bunches at IP 1 & IP 5 (ATLAS resp. CMS), 2 736 at IP 2 (ALICE) and 2 632 at IP 8 (LHCb).

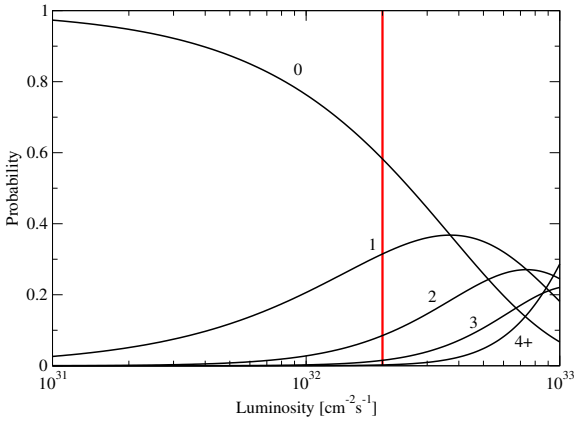


Figure 2.2: Probabilities for having 0, 1, 2, 3 or more than 3 proton–proton interactions per bunch crossing as a function of the machine luminosity at LHCb.

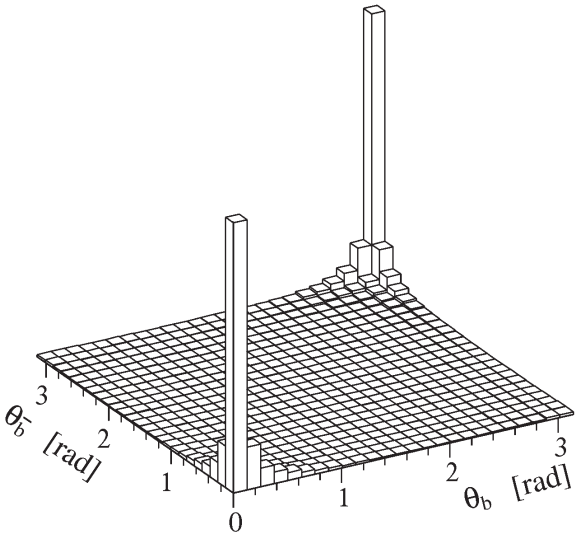


Figure 2.3: Polar angles of the b- and $\bar{\text{b}}$-hadrons calculated by the PYTHIA event generator [Pyt06]. The simulation is taken from the LHCb technical proposal [TP98].

29.6 MHz[8]. Figure 2.2 shows the probability for having n pp interactions as a function of the luminosity, calculated by eqs. 2.1 and 2.2. Multiple pp interactions are not desired since they can lead to ambiguities (and misinterpretation) in the event reconstruction. Therefore, LHCb intends to operate with an average luminosity of $\mathcal{L}_{\text{LHCb}} = 2 \cdot 10^{32}\,\text{cm}^{-2}\text{s}^{-1}$, as indicated by the red line in fig. 2.2. Compared to the nominal LHC luminosity of $10^{34}\,\text{cm}^{-2}\text{s}^{-1}$, this 'low' luminosity should be available right from the beginning of LHC operation. The luminosity at the LHCb interaction point 8 can be kept at its nominal value while the luminosities at the other interaction points of the other experiments are being progressively increased to their design values[9]. This will allow the experiment to collect data for many years under constant conditions. A further advantage of the small LHCb luminosity is reduced radiation damages to the sensors and readout electronics. With a $\text{b}\bar{\text{b}}$ production cross section of $\sigma_{\text{b}\bar{\text{b}}} \approx 500\,\mu\text{b}$, about 10^{12} $\text{b}\bar{\text{b}}$ pairs are expected to be produced in one year of LHCb data taking.

For some relevant decay channels an overview of the expected event rates are given in table 2.1, the corresponding precision on the angles in the unitarity triangle is listed in table 2.2.

2.3 The LHCb Detector

The $\text{b}\bar{\text{b}}$ production in pp interactions is dominated by gluon-gluon fusion processes, $\text{gg} \rightarrow \text{q}\bar{\text{q}}$. The simulation of these processes shows that at high energies both b-hadrons are predominantly emitted at small angles relative to the beam direction into the same hemisphere. This is

[8] As only 2 632 of the possible 3 564 bunches will cross at LHCb, the LHC bunch crossing frequency f_{LHC} of 40.08 MHz is reduced by this factor: $f_{\text{eff}} = f_{\text{LHC}} \frac{2\,632}{3\,564}$.

[9] The luminosity at the interaction point is directly related to the local beam focus system. It will be adjusted so that the luminosity is kept at a constant value.

Decay Modes	Visible Br. fraction	Off-line Reconstructed
$B_d^0 \to \pi^+\pi^-$ + tag	$0.7 \cdot 10^{-5}$	6 900
$B_d^0 \to K^+\pi^-$	$1.5 \cdot 10^{-5}$	33 000
$B_d^0 \to \rho^+\pi^-$ + tag	$1.8 \cdot 10^{-5}$	551
$B_d^0 \to J/\psi K_S$ + tag	$3.6 \cdot 10^{-5}$	56 000
$B_d^0 \to \overline{D}^0 K^{*0}$	$3.3 \cdot 10^{-7}$	337
$B_d^0 \to K^{*0}\gamma$	$3.2 \cdot 10^{-5}$	26 000
$B_s^0 \to D_s^-\pi^+$ + tag	$1.2 \cdot 10^{-4}$	35 000
$B_s^0 \to D_s^- K^+$ + tag	$8.1 \cdot 10^{-6}$	2 100
$B_s^0 \to J/\psi\phi$ + tag	$5.4 \cdot 10^{-5}$	44 000

Table 2.1: Expected numbers of events reconstructed off-line in one year (10^7 s) of data taking with an average luminosity of $2 \cdot 10^{32}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ [TP98].

Parameter	Decay Mode	σ [deg]	Exploited features of LHCb
$\beta+\gamma$	B_d^0 and $\overline{B}_d^0 \to \pi^+\pi^-$; no penguin	0.03	K/π separation
$(=\pi-\alpha)$	penguin/tree$= 0.20 \pm 0.02$	0.03–0.16	K/π separation
β	B_d^0 and $\overline{B}_d^0 \to J/\psi K_S$	0.01	—
$\gamma - 2\delta\gamma$	B_s^0 and $\overline{B}_s^0 \to D_s^\pm K^\mp$	0.05–0.28	K/π separation and σ_t
γ	$B_d^0 \to \overline{D}^0 K^{*0}, D^0 K^{*0}, D_1 K^{*0}$ and $\overline{B}_d^0 \to \overline{D}^0 \overline{K}^{*0}, D^0 \overline{K}^{*0}, D_1 \overline{K}^{*0}$	0.07–0.31	K/π separation
$\delta\gamma$	B_s^0 and $\overline{B}_s^0 \to J/\psi\phi$	0.01	σ_t
x_s	B_s^0 and $\overline{B}_s^0 \to D_s^\pm \pi^\mp$	up to 90 (95% CL)	σ_t

Table 2.2: Expected precision on the angles of the unitarity triangles and related parameters obtained by the LHCb experiment in one year of data taking [TP98]. Special features of the LHCb detector, i.e. particle identification and excellent decay time resolution (σ_t), are indicated if they are crucial for the measurement.

demonstrated in fig. 2.3, showing the polar angles of the b- and $\overline{b}$-hadrons [TP98]. The polar angle is defined with respect to the beam axis in the pp centre-of-mass system. This fact leads to the specific geometry of the LHCb detector. It is a single-arm spectrometer[10] with a forward angular coverage from approximately 10 mrad to 300 mrad in the bending plane and 250 mrad in the non-bending plane. The detector layout after the 'LHCb light' optimisation [TDR9] is shown in fig. 2.4. The forward geometry has additional advantages [Nak02]:

- The spectrometer can be built in an open geometry with an interaction region which is not surrounded by all the detector elements.
- An open geometry allows an easier access for installation, maintenance and possible upgrade.

[10] Only one of the two possible forward regions is covered.

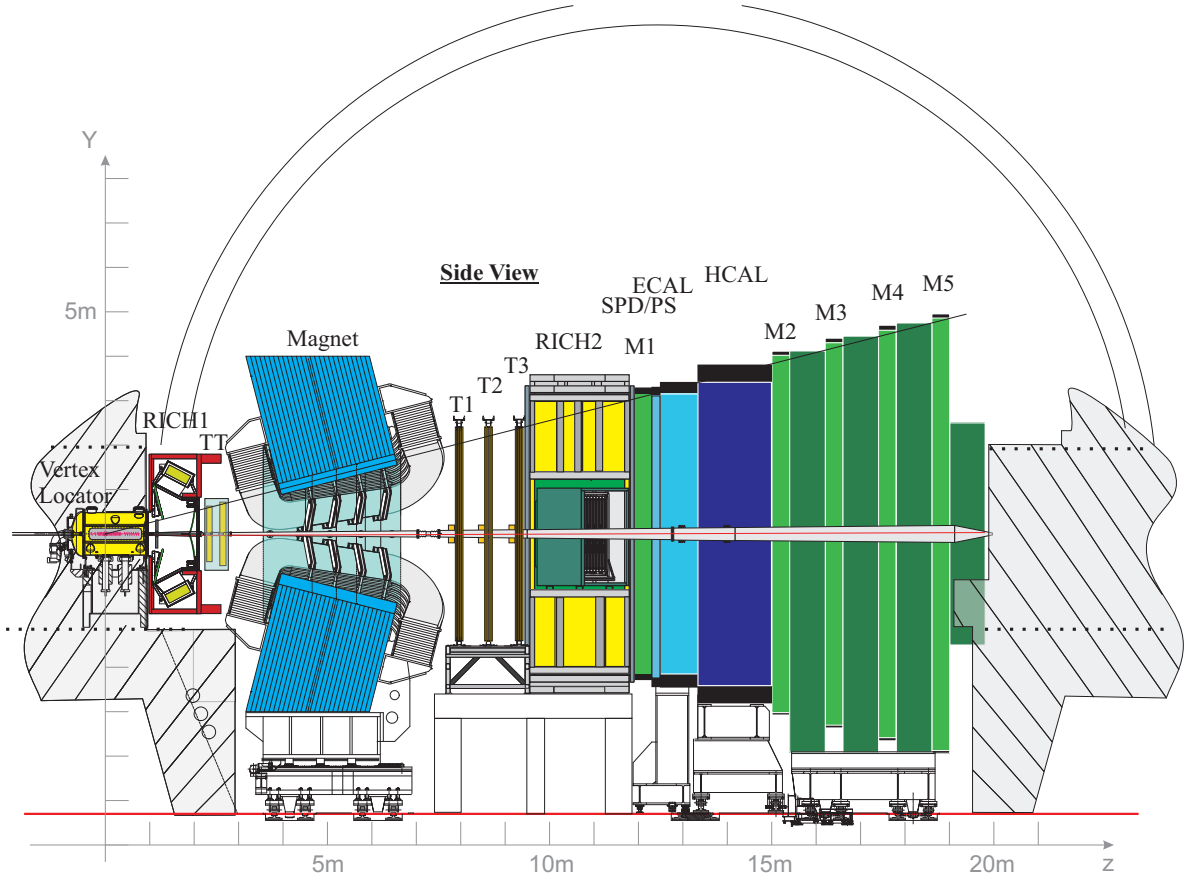


Figure 2.4: Reoptimised LHCb detector layout, showing the Vertex Locator (VELO), the dipole magnet, the two Ring-Imaging Cherenkov (RICH) detectors, the Trigger Tracker (TT) station, the three tracking stations T1-T3 (including the Inner Tracker (IT) and Outer Tracker (OT) system), the Scintillating Pad Detector (SPD), Preshower (PS), Electromagnetic Calorimeter (ECAL), Hadronic Calorimeter (HCAL) and the five muon stations M1-M5. It also shows the direction of the y and z coordinate axes; the x axis completes the right-handed framework [TDR9].

- A trigger on transverse momenta of the order of half the b-mass is more efficient in the forward region, which is dominated by low-p_{T} particles.

- A good decay time resolution for reconstructed b-hadrons can be obtained, since b-hadrons produced in the forward direction are faster than those from the central region. Their average momentum is about 80 GeV/c, corresponding to a mean decay length of ≈ 7 mm.

To avoid major civil construction the LHCb detector has been adapted to the existing experimental area at intersection point 8 that was used by the DELPHI experiment during the LEP era. The complete detector is about 20 m long and 10 m wide and comprises a vertex detector system (VELO), a pile-up veto counter (PUS), an aerogel and a gas RICH counter, a tracking system (Trigger Tracker, Inner Tracker and Outer Tracker), an Electromagnetic Calorimeter (ECAL) with preshower detector, a Hadronic Calorimeter and a muon detector.

Detector component	Detector shortcut	Technology	Number of channels
Vertex Locator	VELO	R-ϕ-silicon sensors	172 032
Pile-Up System	PUS	R-ϕ-silicon sensors	8 192
Trigger Tracker	TT	silicon-strip sensors	143 360
Inner Tracker	IT	silicon-strip sensors	129 204
Outer Tracker	OT	straw tubes with Ar/CO_2	55 000
Ring-Imaging Cherenkov 1	RICH 1	HPD, Aerogel and C_4F_{10}	172 000
Ring-Imaging Cherenkov 2	RICH 2	HPD, CF_4	268 000
Scintillating Pad Detector	SPD	MaPMT	6 000
Preshower	SPD	MaPMT	6 000
Electromagnetic Calorimeter	ECAL	lead / scint. 'shashlik'	6 000
Hadronic Calorimeter	HCAL	iron / scint. tiles	1 500
Muon-system	Muon	MWPC 3-GEM with $Ar/CO_2/CF_4$	25 920

Table 2.3: Detector technologies and number of readout channels employed in the LHCb experiment [Chr05, Vol05].

A summary of all detector components with the used technology and the number of readout channels is shown in table 2.3.

2.3.1 Vertex Detector System

The vertex detector system comprises a silicon Vertex Locator (VELO) and a Pile-Up System (PUS). The vertex detector has to provide precise measurements of the track coordinates of charged particles close to the interaction region. All channels of the VELO have to be read out within 900 ns. The Pile-Up System is used in the Level-0 trigger to suppress all events that contain multiple pp interactions in a single bunch-crossing by counting the number of primary vertices.

Vertex Locator System

The Vertex Locator system consists of 21 stations between z = −18 cm and +80 cm, where $z = 0$ is the cross section point of the two beam bunches. The arrangement of the stations along the beam axis is shown in fig. 2.5. Each station is split in two halves each covering 182° of azimuthal angle (left and right detector module). In their foreseen position perpendicular to the beam pipe the two halves slightly overlap. Each module contains two discs of silicon sensors, with circular (radially R-measuring) and quasi-radial (azimuthal angle ϕ-measuring) strips respectively.

Figure 2.6 depicts the layout of a R- and a ϕ-sensor. Tracking coverage extends radially from 1 to 6 cm and provides at least three space points on tracks with polar angles down to 15 mrad. The active area of the silicon strip sensors is 300 µm thick[11]. In total each half

[11] A thicker sensor will increase the Signal-to-Noise (S/N) ratio but also multiple scattering. A thickness of 300 µm has been chosen as a compromise between noise performance and loss of resolution due to multiple scattering and secondary interactions.

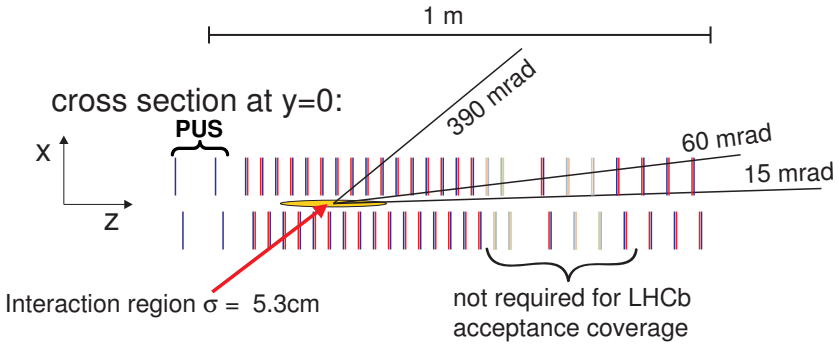


Figure 2.5: VELO station setup. The stations which are not required for covering the LHCb acceptance are marked. The stations which have been removed in the reoptimised LHCb detector layout are indicated with grey shading [TDR9]. The two Pile-Up System (PUS) stations are positioned upstream on the left side.

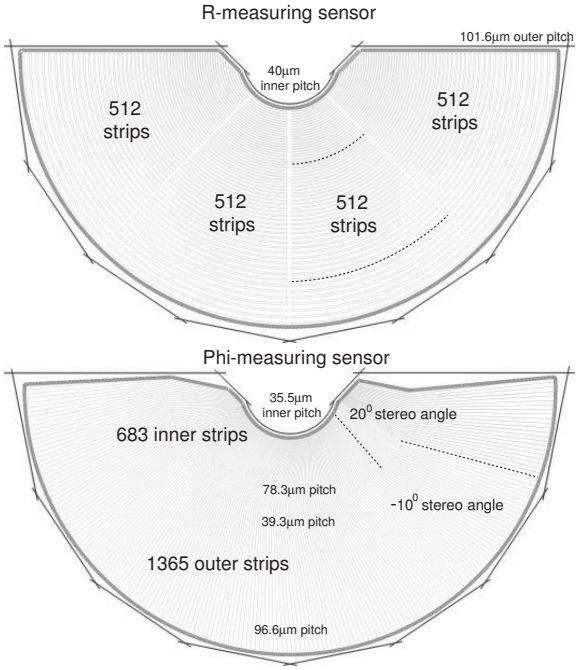


Figure 2.6: R- and ϕ-sensor layout. Some strips are indicated with dotted lines for illustration [TDR9].

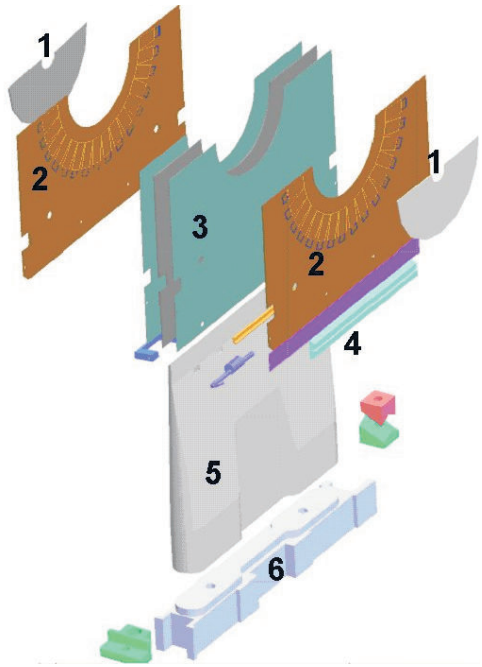


Figure 2.7: Schematic of the VELO module showing the key components. The labelled components are detailed in the text [TDR9].

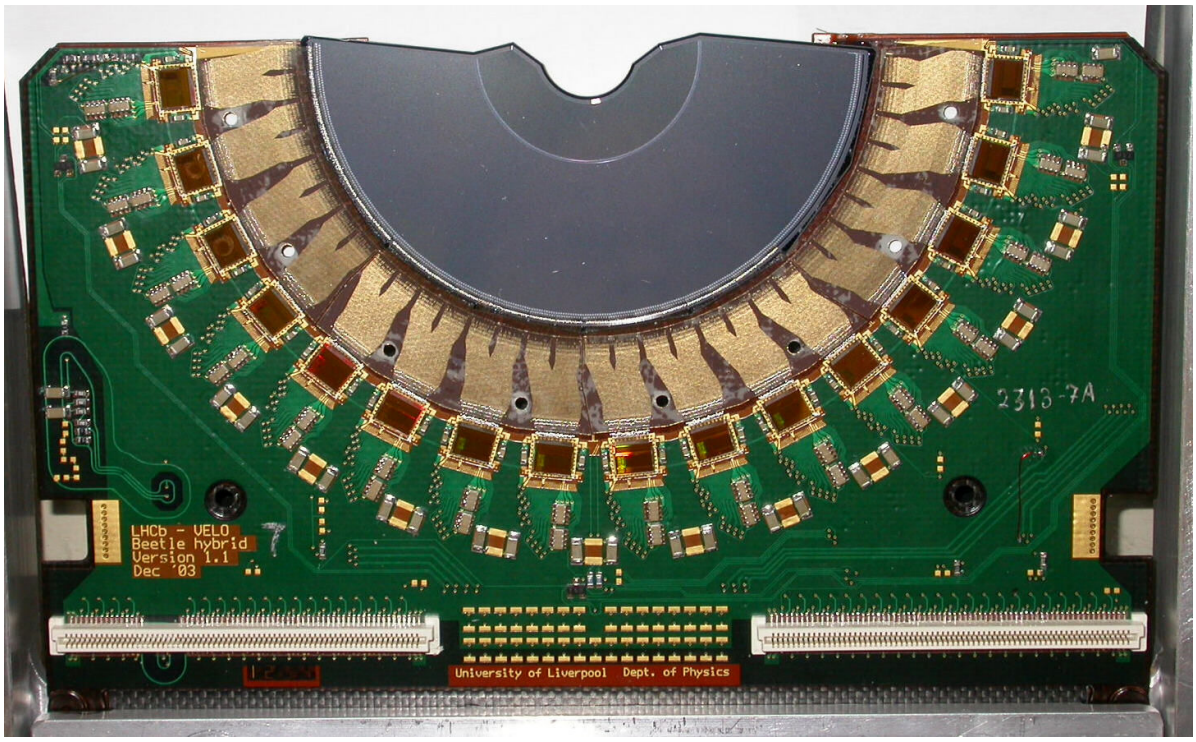


Figure 2.8: View of a fully equipped VELO module including the 16 *Beetle* front-end chips.

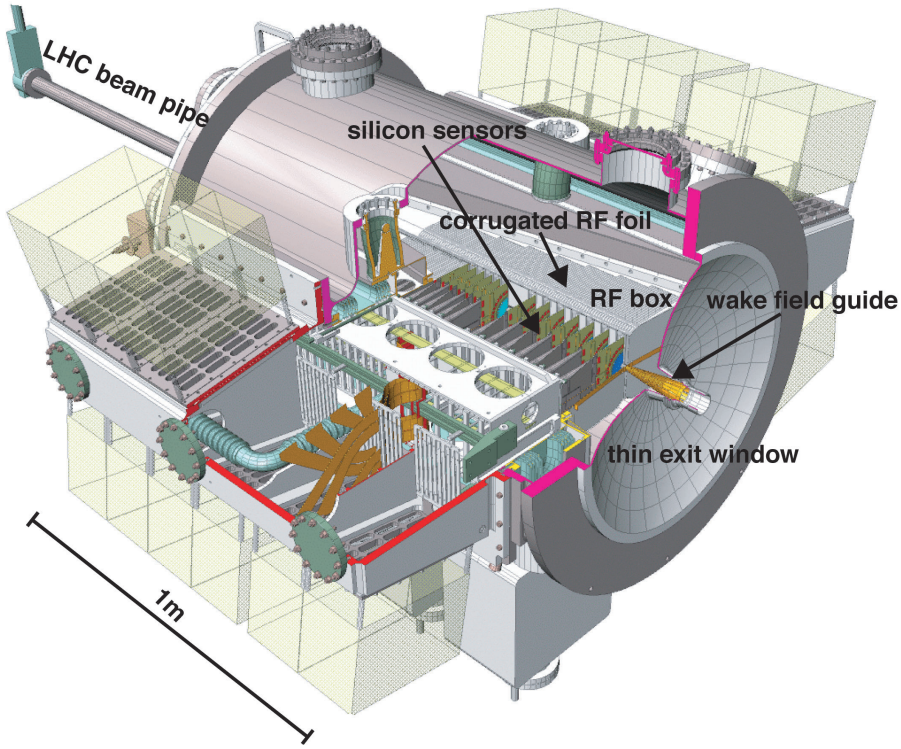


Figure 2.9: The VELO vacuum vessel with the silicon sensors, RF box, wakefield guides and exit window [TDR9].

disc sensor contains 2 048 strips and will be read out by 16 front-end chips. The R-measuring sensor is subdivided into four sectors of approximately 45° and the strip pitch varies from 40.0 µm (inner part) to 101.6 µm (outer part). For the ϕ-measuring sensors the strips are divided azimuthally into an inner and outer region with 683 and 1 365 strips respectively, chosen to equalise the occupancy in the two regions. Here, the pitch of the inner region varies from 35.5 µm to 78.3 µm and of the outer region from 39.3 µm to 96.6 µm. The sensors are flipped from station to station and the strips are tilted with a stereo angle, which is different in sign and magnitude for the inner and outer region. This provides hit resolutions between 6 µm and 10 µm for double-channel clusters and for single-channel hits a resolution between 9 µm and 18 µm. From this R-ϕ sensor arrangement, a resolution of approximately 42 µm can be obtained for the z-direction on the impact parameter of high-momentum tracks.

The exploded view of a single VELO module is shown in fig. 2.7. Figure 2.8 shows a photograph of the module including the 16 *Beetle* front-end chips. The key components of the exploded view are [TDR9]:

1. Silicon sensor half discs.

2. Front-end electronics mounted on a thin Kapton sheet placed approximately at 7 cm distance from the beam axis.

3. Substrate (complex carbon-fibre thermo-pyrolytic graphite composite) performing the dual role of mechanical support and thermal pathway.

4. Cooling block manufactured from fibre composite to match the thermal expansion coefficient of the substrate, which provides the thermal connection to the cooling system.

5. Low mass carbon-fibre paddle which is designed to rigidly hold the substrates and allow the sensors to be placed close to the interaction point.

6. Paddle base made of carbon-fibre. The base is connected via location pins to the platform that supports the two halves of the VELO telescope.

The arrangement of the detector modules along the beam axis is shown in fig. 2.10. The modules are placed in *Roman pots* which are made out of 250 µm thick aluminium foil. The pots act as RF shield against the wake field of the circulating proton bunches. A secondary vacuum is maintained inside the Roman pots to avoid the risk of vacuum leaks. The closest distance between a strip sensor and the beam is 8 mm. This is less than the aperture required by the LHC machine during beam injection. Therefore, the detector modules are retractable by approximately 3 cm. The vertex detector tank with the retractable modules is shown in fig. 2.9. Analogue information from 172 032 amplifier channels is transmitted on 5 376 twisted-pair cables from the vacuum tank to the readout electronics at a distance of about 10 m from the detector.

The silicon sensors are subjected to a harsh radiation environment due to the close distance to the interaction region. At the innermost radius of 8 mm the particle flux is dominated by charged particles, reaching levels of $\approx 10^{14} \mathrm{n_{eq}/cm^2}$ per year of LHCb operation[12]. n-strip sensors on n-bulk material (n-on-n) with AC coupling to the readout electronics and polysilicon resistors for biasing are used.

[12] $\mathrm{n_{eq}}$ is the damage equivalent of a 1 MeV neutron.

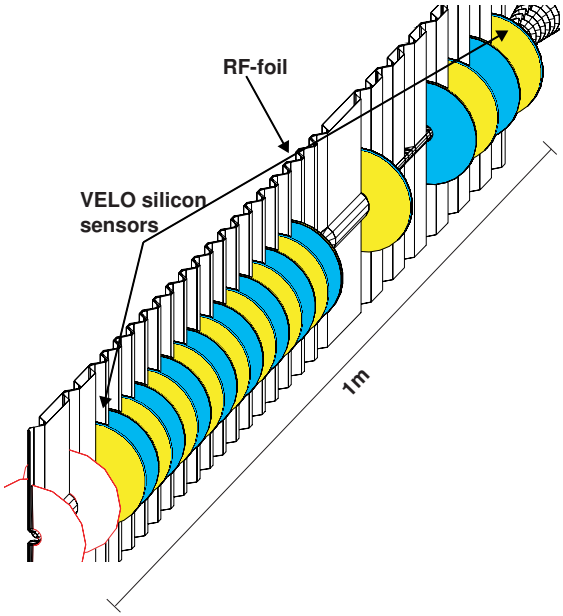


Figure 2.10: Arrangements of detectors along the beam axis. Only the silicon sensors on one side of the RF-foil, which separates the LHC vacuum from the detector vacuum, can be seen. The first two detectors (unshaded) belong to the Pile-Up System [TDR9].

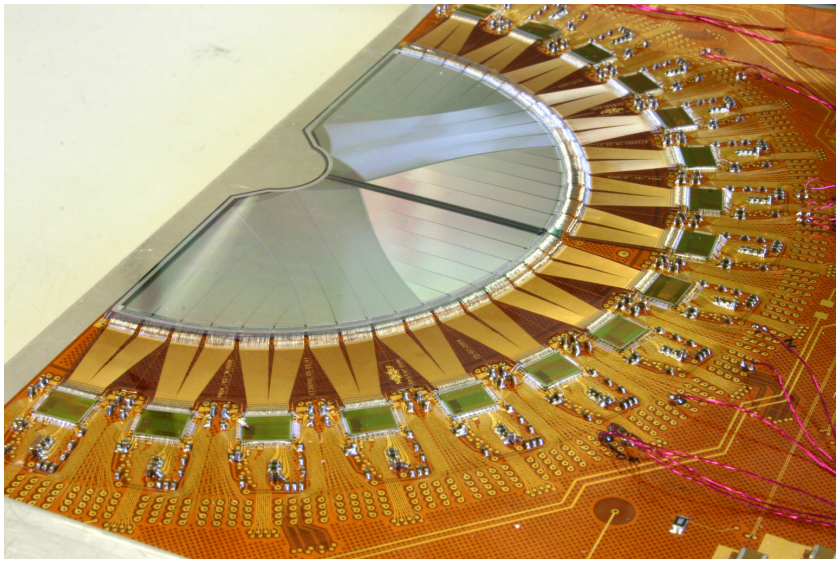


Figure 2.11: Photograph of a Pile-Up System hybrid. 2 048 analogue sensor channels are read out by 16 *Beetle* front-end chip. Each hybrid has 64 pairs of differential signal lines for the analogue readout and 256 LVDS output pairs for the 80 MHz digital Level-0 readout.

Pile-Up System

The VELO detector does not only cover the full forward angular acceptance but also part of the backward hemisphere (cf. fig. 2.5). To facilitate the task of the Level-0 trigger to select events with only one pp interaction per bunch crossing, two additional R-sensors are placed upstream of the VELO stations (indicated in blue on the left of fig. 2.5). The two stations form the Pile-Up System (PUS). Each channel of the PUS front-end chips implements a comparator to discriminate the sampled input signals. Groups of four data channels are ORed and read out directly via 80 MHz LVDS lines [NSC04]. The resulting track information contributes to the vertex reconstruction and the Level-0 trigger decision process.

Figure 2.11 shows a hybrid of the PUS station, including 16 *Beetle* readout chips. Each hybrid contains 256 LVDS output lines for the Level-0 readout (digital trigger information) plus 64 differential signal traces for analogue detector output[13]. The design of the hybrid fulfils the demanding requirements concerning the suppression of crosstalk from the digital output (80 MHz) back to the input of the analogue front-end.

2.3.2 RICH

Particle identification at LHCb is provided by two Ring-Imaging Cherenkov (RICH) detectors [TDR3, TDR9]. The Cherenkov light is produced when charged particles traverse a medium with a speed larger than the speed of light in that medium. The required momentum range to be covered by the RICH detectors is between 1 and 150 GeV/c [14]. Low momentum particles (up to 60 GeV/c) are identified by RICH1. The top view of the RICH1 schematic layout is shown in fig. 2.12. The sub-detector is located between the VELO station and the magnet. RICH1 uses silica aerogel with a refraction index n = 1.03 and C_4F_{10} gas (n = 1.0014). The angular acceptance is 250 mrad and matches that of the complete LHCb spectrometer. High momentum particles are identified by the RICH2 detector (cf. fig. 2.13). RICH2 covers a momentum range of up to 150 GeV/c using gaseous CF_4 (n = 1.0005). It is placed between the Trigger Tracker station and the calorimeter system.

The Cherenkov light is collected by pixel Hybrid Photo Detectors (HPDs) that are placed outside the acceptance of LHCb. The pixel detectors are read out with a dedicated 1024 channel binary pixel chip. Multianode Photomultiplier Tubes (MaPMTs) were foreseen as a backup solution for the detection of the Cherenkov light. In that case the MaPMTs would have been read out by the *Beetle* front-end chip.

2.3.3 The Magnet

A warm dipole magnet with a standard aluminium coil provides an integral field of 4 Tm. It is vertically oriented and has a maximum field strength of 1.1 T [TDR1]. The pole faces of the magnet are shaped to follow the acceptance angle of the experiment (cf. fig. 2.4) to reduce the power dissipation to about 4.2 MW. The magnet itself is built of 50 tons of aluminium conductors and a 1450 tons heavy steel yoke. The polarity of the magnetic field can be changed

[13] In the original electronic detector readout scheme it is not foreseen to read out analogue data from the PUS detectors. Since the *Beetle* front-end chip is able to provide both output modes in parallel (digital to Level-0, analogue to HLT), the analogue readout path is implemented for a further use.

[14] The lower limit is defined by tagging kaons and tracks of high multiplicity decays, the upper limit for π–K separation is determined by $B_d^0 \to \pi^+\pi^-$.

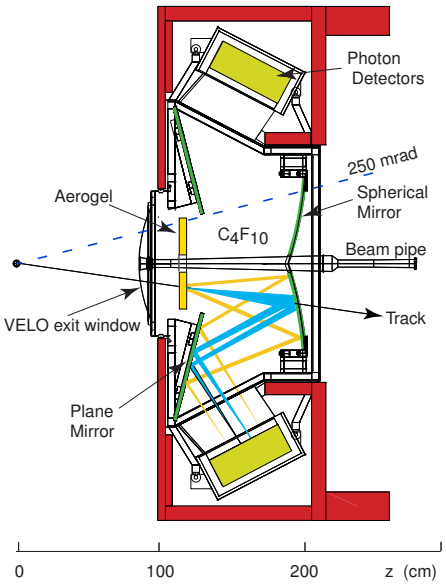


Figure 2.12: Schematic layout of the RICH1 detector (seen from above). The focusing of Cherenkov light from a track passing through the detector is illustrated [TDR9].

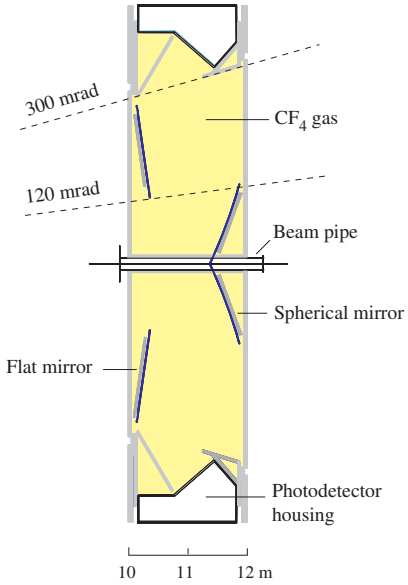


Figure 2.13: Layout of the RICH2 detector [TDR3].

to control systematic errors in the $\mathcal{CP}$-violation measurements that might arise from left-right asymmetries of the detector.

2.3.4 The Tracker

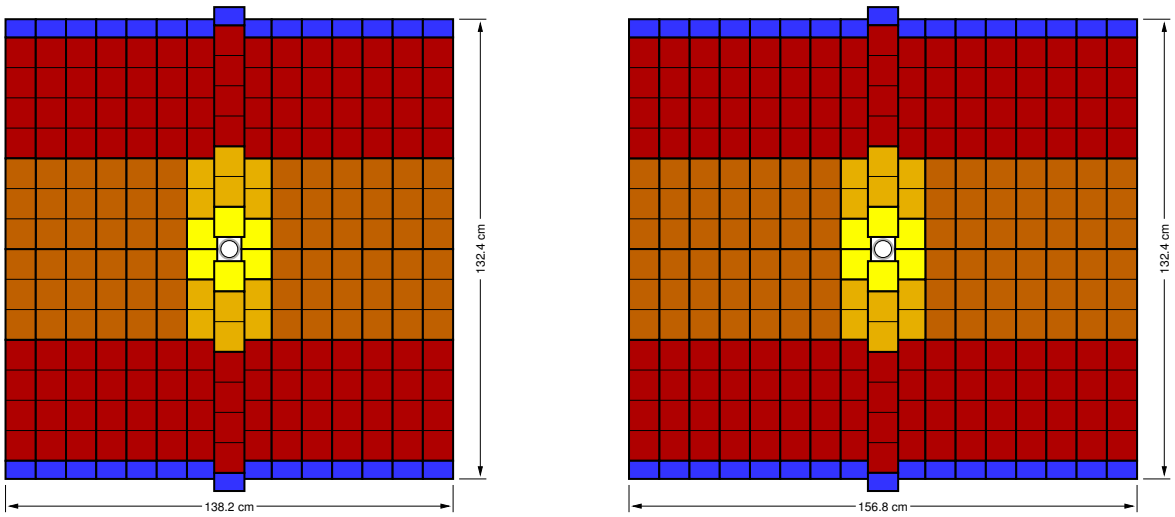
The main purpose of the LHCb tracking system is the precise reconstruction of charged particle tracks in the detector. It consists of four stations – TT and T1-T3 [TDR9]. The T1, T2 and T3 stations are split into the Inner Tracker, located around the beam pipe, and the Outer Tracker.

The sign of the charge and the momentum of the particles are determined by measuring the deflection of their trajectory when passing the magnetic dipole field. The resolution of the momentum is determined by the accuracy of the track measurement. To simplify the track reconstruction the occupancy of single tracking channels has to be kept low. This requires a fine detector granularity. The high track density that is expected around the beam pipe leads to silicon strip sensors as detector technology for the Trigger Tracker (TT) and the Inner Tracker (IT). The Outer Tracker employs drift chamber (straw tubes) technology.

Trigger Tracker

The Trigger Tracker (TT) station is located downstream of RICH1 in front of the magnet. It is part of the High Level Trigger (HLT) system[15] that measures the transverse momentum information of large impact parameter tracks by using the fringe field of the magnet. The information of the TT station is also used in the off-line analysis that reconstructs the trajectories

[15] Former part of the Level-1 trigger system.



(a) Half-station TTa (b) Half-station TTb

Figure 2.14: Layout of the Trigger Tracker station. The x-layer of TTa is shown on the left side, TTb is shown on the right. The readout sectors are made of one, two, three and four silicon strip sensors, connected in series. In the centre of the station the beam pipe is located. The active silicon area of the complete TT detector is 7.7 m^2 divided into 280 readout sectors.

of long-lived neutral particles (e.g. kaons) decaying outside the VELO. Furthermore, with the use of the TT detector, low-momentum particles, that bend out of the detector acceptance before reaching the tracking stations T1-T3, can be detected.

The TT station is made of four layers of silicon strip detectors with an overall active area of approximately $157 \times 132\,cm^2$. The TT is subdivided into two half-stations (TTa and TTb), which are separated in z-direction by about 30 cm. The strip sensors of the first and fourth layer are orientated vertically while the sensors of the second and third layer are tilted by $+5°$ resp. $-5°$ with respect to the other layers.

Figure 2.14 shows the x-layer layout of the two half-stations TTa and TTb. Each layer is divided into 30 modules (TTa) respectively 34 modules (TTb). A module itself is built from several readout sectors of different sizes. Since the readout sectors at the upper and the lower end of each module are made of four individual silicon strip sensors, the inner sectors consist of three sensors that are connected in series. For the area around the beam pipe, the sector is furthermore divided into one- and two-sensors readout sectors to limit the hit occupancy on the sensor strips. The size of each silicon strip sensor is $94 \times 96\,mm^2$ implementing 512 strips with a pitch of 183 µm[16]. The thickness of the silicon sensor is 500 µm, which results in a sufficiently high Signal-to-Noise ratio of about 20 for a single sensor [Aga04] and 12.4 in the worst case situation[17] [Gas03b].

All the front-end readout components (indicated in blue in fig. 2.14) are located at the upper and lower ends of the modules. This reduces the amount of material inside the detector

[16] A pitch of 183 µm results in a measurement precision of 53 µm (eq. 3.12). This is in good agreement with the spatial resolution of 70 µm for single measurements in the bending plane of the dipole field.

[17] Worst case condition: 3 silicon sensors in series, connected via a cable to the readout chip, mid-strip signal measurement.

Number of sensors	Sensor length [cm]	Polyimide cable length [cm]	Total strip capacitance [pF]
1	9.44	58.0	41.4
2	18.88	39.1	47.1
3	28.32	39.1	60.3
4	37.76	—	57.9

Table 2.4: Total strip capacitance for different readout sectors of the TT-station [Gas03b].

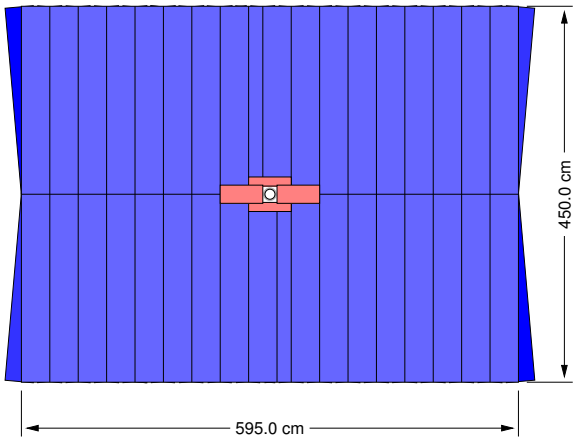


Figure 2.15: Layout of a tracking station. The outer regions with low particle densities are covered by the Outer Tracker (blue) while the area around the beam pipe is equipped with the Inner Tracker (red).

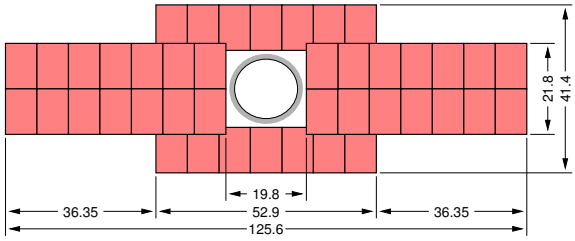


Figure 2.16: Layout of the Inner Tracker station T2. All dimensions are given in cm [TDR8].

acceptance and minimises multiple scattering. The strips of the inner sectors are connected to the readout electronic via polyimide cables. The total input load capacitance of the front-end chips depends on the number of sensors connected in series (strip capacitance) and on the routing length of the cable connection. An overview of the strip capacitances for different TT-sectors is given in table 2.4 [Gas03b]. The column 'Total strip capacitance' is the sum of the sensor strip capacitance, the cable capacitance and 3 pF to account for bond wires and pitch adapter capacitances.

The total active silicon area of the combined four layers has a size of 7.7 m^2. It is divided into 280 readout sectors with 512 strips in each sector. This results in a total number of 143 360 channels, read out by 1 120 front-end chips.

Inner Tracker

The Inner Tracker (IT) is part of the tracking stations T1-T3 and covers the high track density region around the beam pipe (cf. fig. 2.15). It is located downstream of the magnet in front of the RICH2 detector. The IT is built of silicon strip detectors with an strip pitch of 198 µm and has an active area of $78 \times 110\,mm^2$. A detailed view of the Inner Tracker (station T2) is depicted in fig. 2.16. The layout and the dimensions are chosen to keep the channel occupancy in the Outer Tracker at an acceptable level.

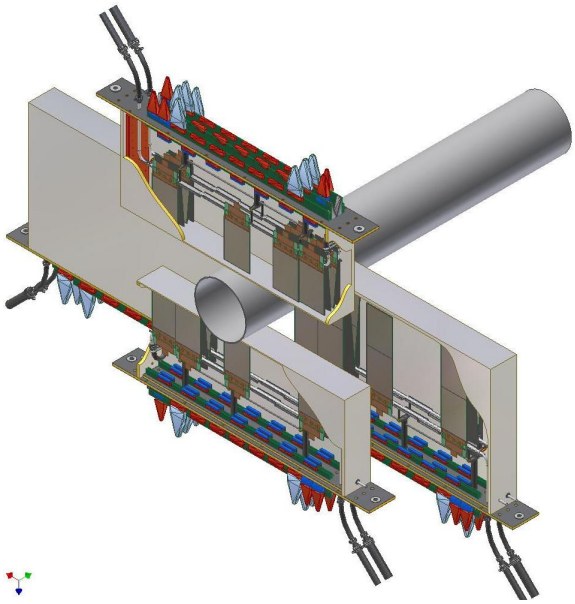


Figure 2.17: Setup of an Inner Tracker station. It consists of 4 individual boxes per station and 4 layers in each box (2 vertical layers and 2 stereo layers).

Figure 2.18: Photograph of an one-sensor Inner Tracker module. A pitch adapter connects sensor and front-end chips. The module is equipped with 3 *Beetle* front-end chips.

Figure 2.17 shows an Inner Tracker station in detail. A station is split into four detector boxes, each including four detection layers placed back-to-back. These are arranged with different stereo angles (0°, +5°, −5° and 0°). A layer is again divided into 7 modules. This results in 28 modules per detector box. The upper and lower boxes are equipped with one sensor per module. The modules in the bending plane consist of two silicon strip sensors which are connected in series. The photograph of an one-sensor module (including the silicon strip sensor and 3 *Beetle* front-end chips) is shown in fig. 2.18.

The length of the Inner Tracker readout strips is shorter than for the strips of the Trigger Tracker. They have therefore a lower load capacitance. Hence, thin silicon sensors are used for the IT to minimise the amount of material inside the detector acceptance. These sensors still generate enough signal to obtain the required Signal-to-Noise ratio of 10[18].

An overview of the total load capacitances of the IT sensor modules is given in tabel 2.5. Again, the table already includes 3 pF to take the capacitance of the bond wires and pitch adapter into account.

The total active silicon area of the three Inner Tracker stations is 4.13 m^2. It is divided into 336 readout sectors with 384 strips in each sector. This results in a total number of 129 024 channels, read out by 1 008 front-end chips.

[18] The generated signal decreases with thinner silicon sensors and the noise decrease with shorter strip lengths.

Number of sensors	Sensor length [cm]	Sensor thickness [µm]	Total strip capacitance [pF]
1	11.0	320	22.5
2	22.0	410	40.0

Table 2.5: Total strip capacitance for different readout sectors of the IT-station. The table includes 3 pF to account for bond wires and pitch adapter capacitances [Vol05].

Outer Tracker

The Outer Tracker (OT) detector covers the outer region of the three tracking stations T1-T3 (cf. fig. 2.15). Its 55 000 channels measure tracks up to a 300 mrad acceptance in the bending plane and 250 mrad in the non-bending plane of LHCb [TDR6]. The OT modules consist of straw tube drift cells, which are 5 mm in diameter. Ar/CO_2 is used as counting gas with a mixing ratio of 70% Argon and 30% CO_2. The main focus of the detector is on the precise measurement of tracks in the x-z bending plane. Each station has two layers with vertical wires and two stereo layers which are tilted by either $+5°$ or $-5°$. The channel occupancy is kept below 10% to ensure an efficient track reconstruction. This gives constraints on the maximum wire length and cell size of the OT. The delay time between particle crossing and signal arrival at the ASDblr preamplifier chips[19] is the sum of the drift time and the propagation delay along the wire. The drift times are expected to stay below 50 ns. The measurement of the drift time is performed by the OTIS TDC[20].

2.3.5 The Calorimeters

The calorimeters consist of the Electromagnetic Calorimeter (ECAL), the Hadronic Calorimeter, the Preshower (PS) and Scintillating Pad Detector (SPD). The calorimeters are used to identify photons, electrons and hadrons and to measure their energies. The detector output information is also included in the Level-0 trigger process system [TDR2].

The SPD and the PS are located on either side of a 12 mm thick lead wall. They are both implemented as 15 mm thick square scintillator pads which are read out by photo-detectors. The SPD plane is used for reduction of the high-p_T tail background of π^0 in the electron trigger system. The PS is used for an accurate spatial detection of photons and electrons by the topology of the electromagnetic showers measured in the subsequent ECAL. The ECAL uses the 'shashlik' technology. It is built from 2 mm thick lead plates as absorber material and scintillator plates to measure the energy of photons and electrons. The last calorimeter element is the HCAL, which measures the energy of the hadrons and separates the high-energy hadrons from electrons. It is built from 4 mm thick scintillating tiles which are embedded in a 16 mm thick iron structure. The scintillators are read out with MaPMTs.

2.3.6 The Muon Detector

The muon triggering and on-line identification is an important requirement of the LHCb experiment due to the fact that muons are present in the final states of many $\mathcal{CP}$-sensitive

[19] The ASDblr preamplifier chip was originally developed for the ATLAS detector

[20] The Outer tracker Time Information System (OTIS) chip measures the time alignment of the digitised straw tube pulse with respect to the bunch crossing clock. The nominal resolution of the OTIS is 390 ps [Sta05].

B-hadron decays [TDR4, TDR4a, TDR4b]. Muons are the only charged particles traversing the calorimeter system. The muon detector consists of five stations (M1-M5) and each station is made of Multi Wire Proportional Chambers (MWPCs). In addition triple-Gas Electron Multiplier (GEM) detectors are used in the innermost part of station M1. The first station M1 is important for the measurement of the transverse momentum of a muon track, which is used for the Level-0 trigger decision. Stations M2-M5, located after the calorimeter system, are additionally embedded in iron plates.

2.4 The Trigger System of LHCb

LHCb uses a two-level trigger system to reduce the primary input rate of 40 TByte/s down to a reasonable level for storage [TDR10]. The first trigger (Level-0 or L0) is implemented in custom electronic hardware, whereas the second trigger is a computer algorithm running on a computing farm. The second trigger level is called High Level Trigger (HLT).

The Level-0 trigger uses information from the PUS, Muon, ECAL and HCAL detector. The PUS is used to count the number of primary vertices and to reject events that have multiple pp interactions. Events that have a single muon, electron or hadron with a high transverse momentum (high-p_{T})[21] cluster are accepted by the Level-0 trigger. If the event is accepted, the information on the high-p_{T} cluster, which triggered the event, is passed to the HLT process to start the analysis. The complete information of all LHCb detector stations is used in the HLT to reconstruct the B-hadron decay modes of interest.

All LHCb detectors, expect those already contributing to the Level-0 trigger, have to store their signals in pipeline memories until the Level-0 trigger accepts or rejects the data. Its trigger latency[22] is chosen to be a constant of 4 µs at maximum. The Level-0 trigger rate is 1 MHz, which means a reduction of the input data by factor 40 in this first trigger stage. All key parameters of the LHCb trigger and readout system are summarised in table 2.6.

With a trigger signal from the HLT, all information of the detectors are stored in the memory of the computing farm. The total reduction of the HLT is approximately a factor 500 which will result in an output rate of 2 kHz divided in four main streams:

- Exclusive B-decays (≈ 200 Hz):
  The core physics stream with exclusively reconstructed decays including side-bands and control channels.

- $\mathrm{D}^{\star}$ (≈ 300 Hz):
  Without particle identification, $\mathrm{D}^{\star}$ events with $\mathrm{D}^0 \rightarrow \mathrm{hh}$ and no D^0 mass cut. These events allow to measure the particle identification efficiency and misidentification rate and can also be used for $\mathcal{CP}$-measurements in D-decays.

- Di-muons (≈ 600 Hz):
  Time unbiased di-muons with a mass above 2.5 GeV. These events are used to measure the uncertainty on lifetime measurements.

[21] High transverse momenta are $1 - 2$ GeV/c, which is large compared to typically $p_{\mathrm{T}} \approx 300$ MeV/c in hadronic interactions.

[22] Level-0 latency is defined as the time between a pp interaction and the time when the trigger signal is received at the front-end chips.

Parameter	Value	Description
Bunch crossing frequency	40.08 MHz	given by the LHC machine
Maximum L0 trigger rate	1.1 MHz	defined by the readout time of the L0 derandomiser
L0 latency	4 µs	time between data sampling and arrival of the L0 trigger decision at the L0 front-end electronics (= 160 clock periods)
L0 gap	none	number of bunch crossings with no L0 trigger accept between two consecutive L0 accepts
Consecutive L0 triggers	max. 16	maximum number of accepted consecutive triggers, when the L0 derandomising buffer is empty
L0 derandomiser depth	16	derandomising buffer is required at LHCb to sustain the high L0 trigger rate of ≈ 1 MHz
L0 readout time	900 ns	= (32 analogue channels + 4 verification bits) × 25 ns
Access to front-end chip setup registers	write & read	read-access for verification of a correct data transmission

Table 2.6: Basic specifications of the LHCb trigger and readout system for all front-end readout electronics [Chr01].

- Inclusive $b \to \mu$ (≈ 900 Hz):
  Events with one high p_T and one muon, used for systematic studies of the trigger efficiency and for data mining. Because of the muon this sample is highly tagging-enriched.

2.5 Radiation Fluxes

The highest particle fluxes in the LHCb experiment are expected in the Vertex Locator. Figure 2.19 shows the total hadron flux normalised to the damage of 1 MeV neutrons as a function of the radius [TDR5]. The innermost detector regions are subjected to a particle flux which is equivalent to $1.3 \cdot 10^{14}$ 1 MeV neutrons per cm^2 and per year.

The radiation levels at LHCb have been calculated with the FLUKA software [FLU]. Table 2.7 gives total dose and particle fluxes at the place of the detector hybrids (VELO, TT, IT, OT and RICH) for 10 years of LHCb operation[24] [Rad04].

[23] 4 VELO stations are removed in the reoptimised LHCb detector [TDR9]. Therefore the old station 25 is now quoted as station number 21. Figure 2.5 depicts the reoptimised VELO detector. The now missing stations are indicated in grey.

[24] Assuming an average $\mathcal{L} = 2 \cdot 10^{32}\text{cm}^{-2}\text{s}^{-1}$ and $\sigma_{\text{tot}} = 80$ mb, hence $1.6 \cdot 10^7$ interactions per second and 10^7 seconds of data taking per year.

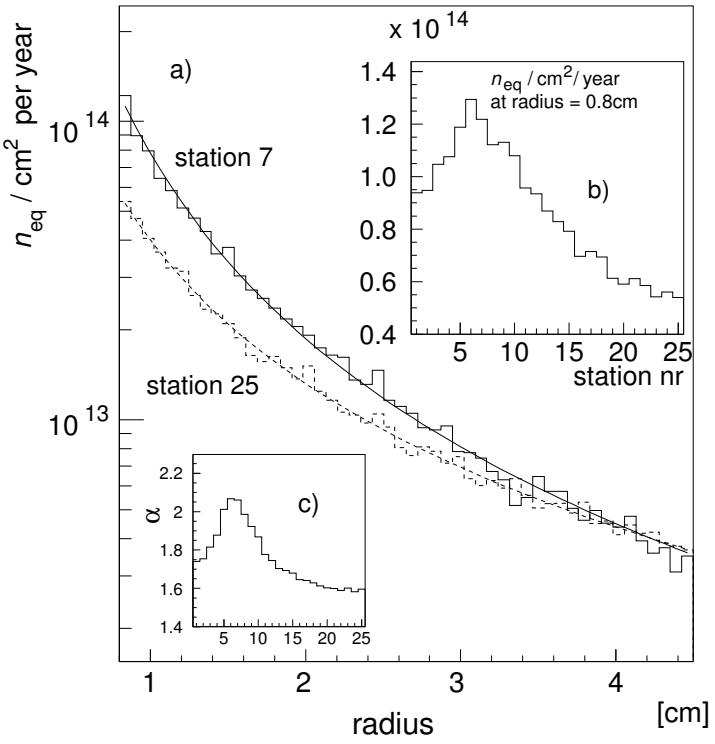


Figure 2.19: Total hadron flux normalised to the damage of 1 MeV neutrons, for two VELO stations as function of the radius [TDR5]. The flux at a radius of 8 mm as a function of the station number is shown in b). The radial distribution shows the expected $r^{-\alpha}$ dependency. The parameter α is plotted in c) as a function of the station number. The station numbers are still depicted in the old VELO numbering schema[23].

	x [cm]	y [cm]	z [cm]	Total dose [Mrad(SiO_2)]	1 MeV eq. neutrons [$10^{13}cm^{-2}$]	Hadrons >20 MeV [$10^{13}cm^{-2}$]
VELO	radius: 5 to 10		−20 to +80	**max = 5.8** **ave = 2.5**	**9.0** **4.1**	**14.0** **5.6**
TT	−70 to +70	−68 to +68	+229 to +234	**max = 7.00** **ave = 0.37**	**8.70** **0.66**	**13.00** **0.47**
IT T1	+9 to +61 −9 to −61	+11 to +14	+780	**max = 1.10** **ave = 0.49**	**1.20** **0.58**	**1.40** **0.55**
	+30	+19 to +23 −19 to −23				
IT T2	+10 to +62 −10 to −62	+11 to +14	+850	**max = 0.83** **ave = 0.34**	**1.10** **0.57**	**1.10** **0.52**
	+30	+20 to +24 −20 to −24				
IT T3	+11 to +63 −11 to −63	+11 to +14	+920	**max = 0.95** **ave = 0.37**	**1.20** **0.62**	**1.10** **0.46**
	+30	+21 to +25 −21 to −25				
OT T1	−291 to +291	+240 to +243 −240 to −243	+800	max = 0.002 ave = 0.002	0.11 0.10	0.004 0.003
OT T2	−291 to +291	+240 to +243 −240 to −243	+870	max = 0.004 ave = 0.003	0.13 0.12	0.006 0.005
OT T3	−291 to +291	+240 to +243 −240 to −243	+940	max = 0.007 ave = 0.005	0.16 0.14	0.009 0.007
RICH1	−100 to +100	+100 to +120 −100 to −120	+160	max = 0.024 ave = 0.017	0.34 0.29	0.031 0.027
RICH2	≈ +400 ≈ −400	−100 to +100	≈ +1 000	max = 0.009 ave = 0.007	0.11 0.09	0.006 0.005

Table 2.7: Summary of expected total dose, 1 MeV neutron equivalent and high energy hadrons (> 20 MeV) for the readout electronics of the different LHCb detector systems. The data is listed for 10 years of LHCb operation [Rad04]. The total accumulated dose, the expected numbers of neutrons respectively hadrons that will be seen by the *Beetle* chip are emphasised in this table.

Chapter 3

Silicon Strip Detectors

The detection of charged particles in the LHCb Vertex Locator (VELO) and Silicon Tracker (ST)[1] is based on single-sided silicon strip detectors. This chapter details the principle of particle detection with silicon detectors. The signal and noise generation are discussed as well as the effects of radiation on the detectors performance.

3.1 Properties of Intrinsic Semiconductor Materials

Semiconductors have unique properties compared to other materials, that make them very suitable for the detection of ionising particles. The biggest advantage of semiconductors – especially silicon – is the wide spread use as basic material for electronic components (e.g. diodes, transistors) and more recently for complete microelectronics circuits. The already existing process technology for microelectronics can be taken or adapted for the production of detectors.

The unique properties of semiconductor materials are not accessible with other radiation detectors (e.g. detectors that are based on ionisation in gas). These are:

- The small band gap of 1.12 eV at T = 300 K leads to a large number of charge carriers per unit energy loss of the traversing ionising particles. The average energy for the creation of an electron-hole pair in silicon is 3.62 eV. This value is an order of magnitude smaller than the ionisation energy of gases ($\sim 30\,\mathrm{eV}$).

- The density of silicon is $\rho_{\mathrm{Si}} = 2.33\,\mathrm{g/cm^3}$. This leads to a large energy loss per traversed length of ionising particles. A Minimum Ionising Particle (MIP) loses on average 3.8 MeV/cm in silicon. It is therefore possible to build thin detectors that still produce signals large enough to be measured.

- The range of δ-electrons[2] in silicon is very small. This prevents a large shift in the centre of gravity from a track's origin of primary ionisation. Therefore, extremely precise position measurements in the order of a few µm are possible.

[1] The Silicon Tracker is a synonym for the combination of the Trigger Tracker (TT) and the Inner Tracker (IT) stations. Both stations are using silicon strip detectors for readout.

[2] Energetic electrons ejected from atoms in matter by the passage of ionising particles. In every primary ionising collision between a charged particle and an atom, one or more electrons are ejected. Delta electrons are that small fraction of these emitted electrons having energies which are large compared to the ionisation potential.

- Electrons and holes can move almost freely in semiconductors. The mobility of electrons in silicon is $\mu_{\mathrm{n}}^{\mathrm{Si}} = 1\,450\,\mathrm{cm}^2/\mathrm{Vs}$ and $\mu_{\mathrm{p}}^{\mathrm{Si}} = 450\,\mathrm{cm}^2/\mathrm{Vs}$ for holes at room temperature. Both are only moderately influenced by doping. The time for charge collection in a typical sensor with a thickness of 300 µm is in the order of 10 ns (cf. eq. 3.10 and fig. 3.3). This allows the use of silicon detectors in high-rate environments.

- The integration of detector and readout electronic into a single device is possible.

- Special doping of the used crystals allows the creation of fixed space charges with rather sophisticated field configurations without obstructing the movement of the signal charges. This allows the development of detector structures with new properties that have no analogy in gas detectors [Lut99].

3.2 Carrier Generation

Simultaneously to the lifting of electrons from the valence band into the conduction band an equal number of holes is generated. This is accomplished by various mechanisms that only have to supply the necessary energy, e.g. thermal agitation, optical excitation and ionisation by penetrating charged particles.

Mobile charge carriers in particle detectors are generated by charged particles traversing the material. They lose part of their energy through elastic collisions with electrons. The basic theory has been developed first by Bohr using classical arguments, and later in a quantum mechanical way by Bethe [Bet30], Bloch [Blo33] and Landau [Lan44]. The rate of ionisation loss for charged particle in matter is given by the Bethe-Bloch formula. The Bethe-Bloch formula in eq. 3.1 contains corrections for density and shell effects [Leo94]:

$$\frac{dE}{dx} = \underbrace{2\pi N_{\mathrm{A}} r_e^2 m_e c^2}_{=0.1535\,\mathrm{MeV}\,c^2/\mathrm{g}}\ \rho \frac{Z}{A}\frac{z^2}{\beta^2}\left[\ln\left(\frac{2m_e\gamma^2c^2\beta^2W_{\max}}{I^2}\right) - 2\beta^2 - \underbrace{\delta}_{\substack{\text{density}\\\text{correction}}} - \underbrace{2\frac{C}{Z}}_{\substack{\text{shell}\\\text{correction}}}\right] \tag{3.1}$$

with

x	–	path length [in $\mathrm{g/cm}^2$],
N_{A}	–	Avogadro-constant ($6.02205 \cdot 10^{23}\,mol^{-1}$),
r_e	–	classical electron radius ($= \frac{e^2}{4\pi m_e c^2} = 2.817 \cdot 10^{-15}\,\mathrm{m}$),
m_e	–	electron mass ($511\,\mathrm{keV/c}^2$),
ρ	–	density of medium (e.g. $\rho_{\mathrm{Si}} = 2.33\,\mathrm{g/cm}^3$),
Z	–	atomic number of the medium (e.g. $Z_{\mathrm{Si}} = 14$),
A	–	atomic weight of the medium (e.g. $A_{\mathrm{Si}} = 28.1$),
z	–	charge of the traversing particle,
β	–	velocity of the traversing particle in units of speed of light ($= \frac{v}{c}$),
γ	–	$= \frac{1}{\sqrt{1-\beta^2}}$,
$W_{\max}$	–	maximum energy transfer in a single collision,
I	–	effective ionisation potential averaged over all electrons (e.g. $I_{\mathrm{Si}} = 173\,\mathrm{eV}$),
δ	–	density correction,
C	–	shell correction.

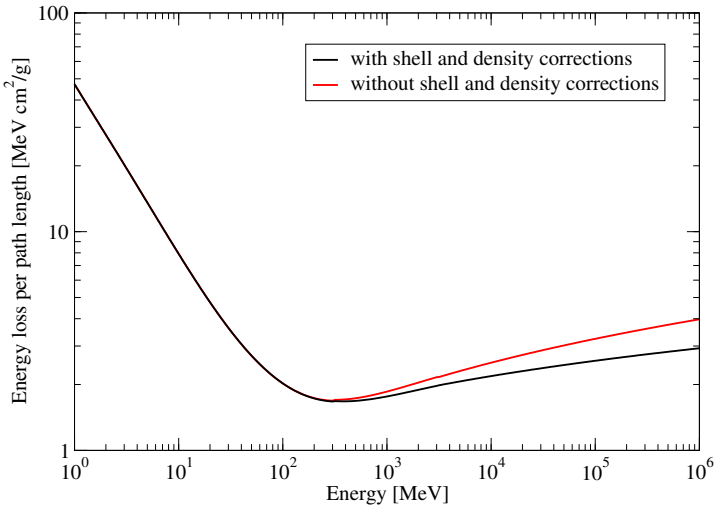


Figure 3.1: Energy loss due to ionisation as a function of kinetic energy of a charged pion traversing silicon with (black line) and without (red line) density and shell corrections. Data taken from [Lut99].

δ is a correction term which takes the reduction in energy loss due to the so-called density effect into account. This becomes more important at high energies due to the media being polarised with increasing velocity of the incident particle. As a consequence, the atoms in a medium can no longer be considered independent. To correct for this effect the approximation of Sternheimer is used [Ste82]. The shell correction $\frac{C}{Z}$ term accounts for the fact that, at low energies for light elements and at all energies for heavy ones, the probability of collision with electrons of the inner atomic shells (K, L, etc.) is negligible.

The typical energy loss rate as a function of the particle energy for a charged particle (e.g. a pion) traversing silicon is shown in fig. 3.1. The energy and the velocity of the incident particle with mass m are related by the relativistic kinematics as

$$E \;=\; \gamma mc^2 \;=\; \frac{mc^2}{\sqrt{1-\beta^2}} \tag{3.2}$$

which reduces to $E_{\text{kin}} = E - mc^2 = \frac{1}{2}mv^2$ for small velocities.

The maximum energy transfer appears by a head-on collision. It is given by

$$W_{\max} \;=\; \frac{2m_e c^2\beta^2\gamma^2}{1 + 2s\sqrt{1+\beta^2\gamma^2} + s^2}\;, \qquad \text{with} \;\; s = \frac{m_e}{m}\;. \tag{3.3}$$

For $m \gg m_e$ $W_{\max}$ reduces to

$$W_{\max} \;\approx\; 2m_e c^2\beta^2\gamma^2\;. \tag{3.4}$$

For low (non-relativistic) energies, the energy loss rate $\frac{dE}{dx}$ is inversely proportional to the energy or respectively to the velocity squared. With rising energy a minimum is reached followed by the relativistic rise showing logarithmic characteristics. At very high energies a saturation is observed. This is due to the polarisation of the medium. A particle depositing a minimum of energy per path length is called a Minimum Ionising Particle (MIP).

In a sample of finite thickness the average energy loss can be obtained from eq. 3.1 by integration. There are in addition statistical fluctuations about the average energy loss, leading to an energy loss distribution, first derived by Landau [Lan44][3].

The average energy loss in silicon for the creation of electron-hole pairs is 3.62 eV at room temperature, which is three times larger than the band gap energy ($E_{\mathrm{g,Si}} = 1.12\,\mathrm{eV}$) between the valence band and the conduction band[4].

The fraction of energy that is used for electron-hole pair creation is a property of the detector material. It only weakly depends on the type and energy of the radiation [Lut99][5]. For a given radiation energy, the signal fluctuates around a mean value N given by

$$N = \frac{E}{\epsilon} \tag{3.5}$$

with the absorbed energy E in the detector and the mean energy ϵ for electron-hole pair creation. The variance in the number of signal electrons (resp. holes) N is given by

$$\langle \Delta N^2 \rangle = F \cdot N = F\frac{E}{\epsilon} \tag{3.6}$$

with the Fano factor F [Fan47][6]. The reason for this fluctuation is the variation in the fraction of deposited energy (which ends up in electron-hole separation) and phonon generation (which eventually means thermal energy). If for example the total energy is converted into electron-hole generation, their number would be fixed and the Fano factor F would be zero. A factor significantly below unity indicates, that charge creation dominates over the phonon excitation.

For silicon the Fano factor is 0.115, which is significantly below unity [Lut99]. From eq. 3.1 and eq. 3.6, the most likely energy loss for a MIP (e.g. $1-2\,\mathrm{MeV}$ electrons or $300-400\,\mathrm{MeV}$ charges pions) can be determined. It is in silicon approximately $270\,\mathrm{eV}/\,\mu\mathrm{m}$, which results in the creation of about 75 electron-hole pairs per µm [Nee03]. For a 300 µm (500 µm) thick silicon detector the most likely charge signal amounts to 22 400 electrons (37 300 electrons).

3.3 Charge Collection

A silicon detector basically operates as a reverse-biased diode[7]. The free charge carriers of the n-doped material have negative sign (electrons) while the p-doped material features positively charged holes, which both contribute to the electrical current. At the junction of the p- and n-material the free charge carriers from both doped regions recombine. A region free of mobile charge carriers builds up, the *depletion region*. This region forms the sensitive volume of a

[3] A review of this subject, including refinements of Landau's original treatment can be found in [Bak87] and [Bic88].

[4] To lift an electron from the valence band to the conduction band using an energy equal to the minimum band gap spacing requires a momentum transfer from the lattice, since silicon is an indirect semiconductor (e.g. the valence band maximum is not at the same position in momentum space than the conduction band minimum) [Lut99].

[5] Except at very low energies that are comparable with the band gap energy.

[6] Fano derived this expression by considering the probabilities of ionising and non-ionising collisions of charged particles in gases. His approach has been adapted to semiconductors by Shockley [Sho52]. The dependence of the mean energy needed for electron-hole pair creation and the dependence of the Fano factor on the energy of the radiation are described in [Ali80].

[7] By joining together oppositely doped semiconductor materials, a pn-junction (= contact region) is created which shows diode characteristics.

detector. The majority charge carriers diffuse into the oppositely doped regions (electrons diffuse from n into p region, holes vice versa). Therefore, a negative charge builds up in the p-material and a positive one in the n region. This introduces an electric field counteracting the diffusion process. An equilibrium appears between both currents, building the depletion region.

If an external voltage is applied to the diode, the system is no longer in thermal equilibrium. The depth d of the depletion layer depends on the external voltage and is given by [Lut99]

$$d = \sqrt{\frac{2\epsilon_0\epsilon}{e}\,\frac{n_\mathrm{A}+n_\mathrm{D}}{n_\mathrm{A}n_\mathrm{D}}\,(V_\mathrm{bi}-V)} \tag{3.7}$$

where
- d – depletion depth,
- n_A – doping concentration of acceptors,
- n_D – doping concentration of donors,
- ϵ_0 – permittivity of free space ($8.854\cdot10^{-12}\,\mathrm{F/m}$),
- ϵ – permittivity of the medium ($\epsilon_\mathrm{Si}=11.8$),
- e – elementary charge,
- V_bi – built-in voltage or diffusion voltage of the pn-junction ($\approx 0.5\,\mathrm{V}$),
- V – external bias voltage.

The built-in voltage V_bi is given by

$$V_\mathrm{bi} = \frac{kT}{e}\ln\frac{n_\mathrm{A}n_\mathrm{D}}{n_i^2} \tag{3.8}$$

where k is the Boltzmann's constant ($k=1.3807\cdot10^{-23}\,\mathrm{J\,K^{-1}}$), T is the absolute temperature and n_i is the intrinsic charge carrier concentration. At room temperature the concentration for silicon is $n_{i,\mathrm{Si}}\approx10^{10}\,\mathrm{cm^{-3}}$. Equation 3.7 shows, that the depletion depth d is proportional to the square root of the external bias voltage.

Biasing the diode in reverse direction[8] increases the depth of the depletion region and hence the sensitive detector volume. At the same time the detector capacitance decreases:

$$C_\mathrm{sb} = \epsilon_0\epsilon\frac{A}{d} = A\cdot\sqrt{\frac{e\epsilon_0\epsilon}{2(V_\mathrm{bi}-V)}\,\frac{n_\mathrm{A}n_\mathrm{D}}{n_\mathrm{A}+n_\mathrm{D}}} \tag{3.9}$$

where
- C_sb – strip-to-backplane capacitance,
- A – area of the depletion layer.

Here, the capacitance is now proportional to one over the square root of the external bias voltage V.

A fully depleted detector volume[9] is very desirable, since [Lut99]

- the Charge Collection Efficiency (CCE), i.e. the signal is proportional to the depletion depth,
- the noise is $\propto C_\mathrm{sb}\propto 1/d$,
- the resolution is decreased by charge spread in a partially depleted detector volume.

[8] The p-side on a negative potential compared to the n-side.
[9] The full depletion depth d is equal to the detector thickness.

3.4 Spatial Signal Resolution

High spatial resolution across a large detector area is achieved by segmentation into parallel strips or by segmentation into an array of pixels. Each of the segments is read out separately. In comparison with a standard single-sided strip sensor a pixel array provides a direct two dimensional detection of the signals. This technique helps to avoid ambiguities at high track multiplicities. Due to the fact that the *Beetle* front-end chip is designed to read out strip sensors, the pixel sensors technique is not discussed in this chapter.

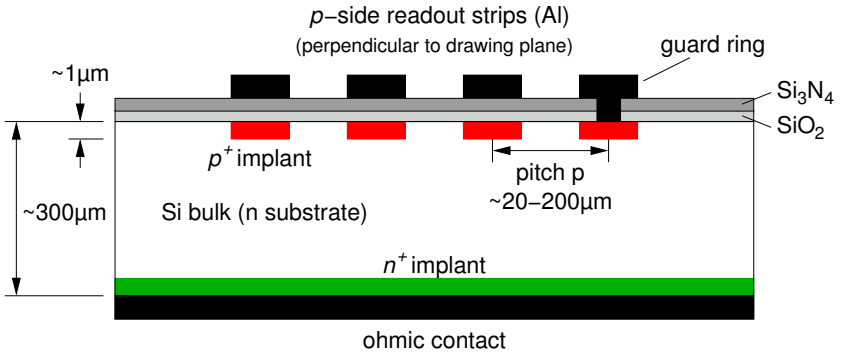


Figure 3.2: Cross section of an AC-coupled single-sided silicon strip detector.

A typical cross section of a single-sided silicon strip detector is shown in fig. 3.2. The AC coupling between the strip and the readout line is usually realised by separating both with an isolation layer (SiO_2 and Si_3N_4). To avoid charge transfer to neighbouring strips, the coupling capacitance has to be large compared to the interstrip capacitance. For biasing the diffusion regions, three choices exist [Lut99]:

- the integration of a *punch-through*[10], which is difficult to operate and suffers from radiation damage,
- the use of *implant resistors*, which are only usable on the p-side in an n-bulk but are radiation hard,
- the implementation of *polysilicon resistors* (cf. fig. 3.2), which are also radiation hard but require a larger area than implant resistors.

The resolution of a silicon strip sensor depends mainly on the strip spacing, the diffusion width of the charge cloud and the method of readout. Usually the pitch of the strips matches the diffusion width σ_x. In a fully depleted silicon strip sensor the diffusion width depends on the drift time t_{drift} and the diffusion constant D_p of the charge carriers. The drift time is roughly estimated from the average field and one half of the detector depletion thickness

$$t_{drift} \approx \frac{d/2}{\mu_p V_{dep}/d} = \frac{d^2}{2\mu_p V_{dep}} = \frac{\epsilon_0 \epsilon}{\mu_p e n_D} \tag{3.10}$$

[10] Strips are biased by means of a punch-through structure between the biasing electrode and the strips

with depletion voltage $V_{\mathrm{dep}} \approx \frac{e n_{\mathrm{D}} d^2}{2\epsilon_0 \epsilon}$ according to eq. 3.7. The holes will diffuse in a lateral direction. The resulting distribution can be described by a Gaussian. The RMS value of the projected distribution is

$$\sigma_{\mathrm{x}} = \sqrt{2 D_{\mathrm{p}} t_{\mathrm{drift}}} = \sqrt{2 \frac{kT}{e} \mu_{\mathrm{p}} t_{\mathrm{drift}}} = \sqrt{2 \frac{kT}{e} \frac{\epsilon_0 \epsilon}{e n_{\mathrm{D}}}} \quad . \tag{3.11}$$

Matching the readout pitch to the diffusion width results in strip pitches of about 10 µm for a 300 µm thick silicon sensor. Reading out each individual strip in this high-density strip arrangement is very difficult. One approach to avoid this problem is the use of resistive or capacitive charge division (cf. [Lut99]). In this case not every strip but only every k^{th} strip is read out.

As long as only quasi digital information is used[11], the resolution Δx (RMS deviation from the true coordinate) is given by the strip pitch p as

$$\left\langle \Delta x^2 \right\rangle \;=\; \frac{1}{p} \int_{-\frac{p}{2}}^{+\frac{p}{2}} x^2 \, dx \;=\; \frac{p^2}{12} \quad . \tag{3.12}$$

Typical strip pitches are $20 - 200$ µm, which results in resolutions of approximately $6 - 60$ µm.

If the strip pitch is chosen small enough so that the signal charge is collected on more than one strip, the measurement precision can be substantially improved with an analogue readout. The coordinate is found by interpolation, i.e. by the centre of gravity of the input charge cloud. The position resolution is then limited by the Signal-to-Noise (S/N) performance of the electronics and the readout strip pitch p, as follows [Lut99]:

$$\Delta x \;\approx\; \frac{p}{S/N} \quad . \tag{3.13}$$

Also, in highly segmented strip sensors, the interstrip capacitances C_{ss} dominate over the strip-to-backplane capacitance C_{sb} (eq. 3.9) by a factor of 5. For strip pitches of $25 - 100$ µm, C_{ss} is typically $1 - 2$ pF/cm in silicon [Spi01].

3.5 Noise Sources

The two main noise sources which contribute in silicon detectors are the *detector capacitances*[12] and the *leakage* currents. These leakage currents introduce shot noise, since the origin of the shot noise is the random motion of the electrons as they are discrete charge carriers. Its magnitude is expressed as the variance of the current and is proportional to the current itself. It has a white spectral distribution and is given by $i^2 = \left\langle (I - \langle I \rangle)^2 \right\rangle = 2e \cdot I_{\mathrm{leak}} \cdot BW$, whereas BW is the bandwidth. The detector leakage current is also strongly temperature dependent[13]. Therefore, cooling the sensor is a possibility to reduce the leakage current. For example, cooling a silicon sensor from room temperature down to 0°C reduces the leakage current by a factor of 6 [Lut99]. Beside this the most simplest approach against leakage currents is the segmentation of the silicon sensor, since the leakage current is then shared with other strips.

[11] Taking the centre position of the strip as the measured coordinate and neglecting the effects arising from track inclination and charge diffusion during collection.

[12] More precisely, the input FET of the front-end preamplifier is the noise source (channel noise). The detector capacitance is only the reason that a larger part of the channel noise will contribute the system.

[13] $I_{\mathrm{leak}}(T) \propto T^2 e^{-E/2kT}$, E being the electron-hole creation energy.

In case of AC coupling between detector and the readout electronics, the coupling capacitance has to be large compared to the interstrip capacitances C_{ss}. The leakage current of a sensor is more important for DC readout electronics than for AC coupled readouts. In the case of DC readout the input amplifier has to sink the leakage current, which can lead to a pedestal shift, a reduction of the dynamic range and/or a saturation of the amplifier. An AC coupled design avoids these drawbacks. Here, only the AC part of the signal current is used while the DC part is coupled to the bias network of the silicon sensor. Because of the shot noise of the leakage current this fluctuation also couples into the amplifier as an additional noise source.

3.6 Radiation Damages in Silicon Sensors

The irradiation of silicon sensors causes displacement damages in the material. These damages lead to defects states in the silicon bulk which create thermal excitations and enable a possible charge carrier transfer to the conduction band. Hence, the dark current of the reverse-biased *pn*-junction increases [Lut99]. Additionally, the defect complexes also act as recombination centres which result in a decrease of the output signal of a silicon sensor. A possible change in the doping concentration will also affect the depth of the depletion area (eq. 3.7) or increases the full depletion voltage. The increase of the leakage current of the sensor results in an increase of the total power consumption, an increase of the shot noise and/or an increase of the DC signal current that bypass the AC coupling[14].

3.7 Signal Readout

The output signal of a silicon sensor is a short current pulse I_s with a signal duration of about $0.1 - 30\,\text{ns}$ for a $10 - 500\,\mu\text{m}$ thick sensor. A typical output pulse for a $300\,\mu\text{m}$ prototype IT sensor is shown in fig. 3.3. The total charge Q_s created in a silicon sensor is proportional to

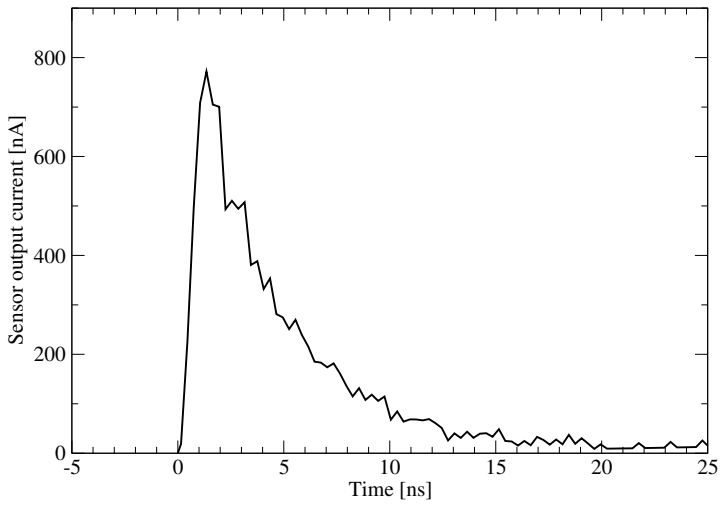


Figure 3.3: Typical primary current pulse of a silicon sensor [Sie02].

[14] For long integration times the increase of the DC current can drive the subsequent readout amplifier into saturation.

the energy E deposited in the detector

$$Q_{\mathrm{s}} \;=\; \int I_{\mathrm{s}}(t)\,dt \propto E\;. \tag{3.14}$$

To read out a silicon sensor, the output is connected to a subsequent amplifier. Three different readout amplifier configurations exist [Lut99, Spi01]:

- *Voltage amplifier*
  The sensor output signal is integrated on the sensor capacitance C_{d} and the voltage across the capacitor is amplified. The output voltage is given by

  $$V_{\mathrm{out}} \;=\; -A\frac{Q_{\mathrm{s}}}{C_{\mathrm{d}}+C_{\mathrm{in}}}\;, \tag{3.15}$$

  where C_{in} is the capacitive input load. Since the amplifier output voltage depends directly on the detector capacitance C_{d} this configuration should only be used if C_{d} is constant (i.e. the strip length is equal for all sensor strips and the depletion depth is constant).

- *Current amplifier*
  The output current is directly amplified and transformed into a voltage signal. The main drawback of this feedback configuration is the inductive input impedance [Gat84], which limits the use in systems with large capacitive loads.

- *Charge-Sensitive Amplifier*
  The configuration of a Charge-Sensitive Amplifier (CSA) integrates the output current actively on the feedback capacitor. A CSA features a purely resistive input impedance (for $\frac{1}{RC} \ll f \ll GBW$) and is the best configuration concerning noise behaviour.

The CSA configuration is chosen as the preamplifier concept of the *Beetle* readout chip. A more detailed discussion of the CSA is given in section 5.4.

Chapter 4

Introduction to VLSI Electronics and Radiation Hardness

The high energy physics experiments at the LHC accelerator deal with dose rates of up to 10 Mrad per year and with fluences of about $10^{15}\,\mathrm{cm}^{-2}$ (neutrons and hadrons). These hostile radiation environments require radiation hard electronics. The high readout channel densities for silicon strip and pixel detectors require the application of Very Large Scale Integration (VLSI) circuits. This chapter describes the interaction of various kind of incident particles with matter (section 4.1), the effects and degradations in Metal Oxide Semiconductor (MOS) devices (section 4.2) and the Single Event Effects (SEEs), phenomena induced in a semiconductor device or a circuit by the impact of a single particle or ion (section 4.3). A short overview of radiation hard VLSI design techniques is given in section 4.4.

4.1 Radiation interaction in matter

The way in which radiation interacts with solid materials depends on the type, mass, charge and kinetic energy of the incident particle and on atomic number, mass and density of the target material. The incident particles are divided into two groups: neutral particles and charged particles.

The neutral particles of interest are neutrons and photons. Neutrons may interact with the atomic nuclei by *elastic collisions*, *inelastic collisions* or *nuclear reactions*. Photons can interact with matter via *Compton scattering*, the *photoelectric effect* or *pair production*. The probability of these three effects strongly depends on the energy of the incident photon and on the atomic number of the target, as shown in fig. 4.1. The photons used in the irradiation test of this work (cf. section 6.6) were 20 keV to 60 keV X-rays, which interact with silicon mainly by photoelectric effect.

Charged particles differ from the neutral particles since they mainly interact through Coulomb attraction or repulsion with the electronic clouds of the target atoms. The charged particles of interest are protons, heavy ions an electrons.

All effects induced by these particles can be grouped in two different classes: *ionisation effects* and *nuclear displacement*. Neutrons cause nuclear displacement, whereas photons and electrons are responsible for ionisation effects.

The ionisation effects creates electron-hole pairs in semiconductors or insulating materials. The number of created pairs is proportional to the amount of energy deposited in the ma-

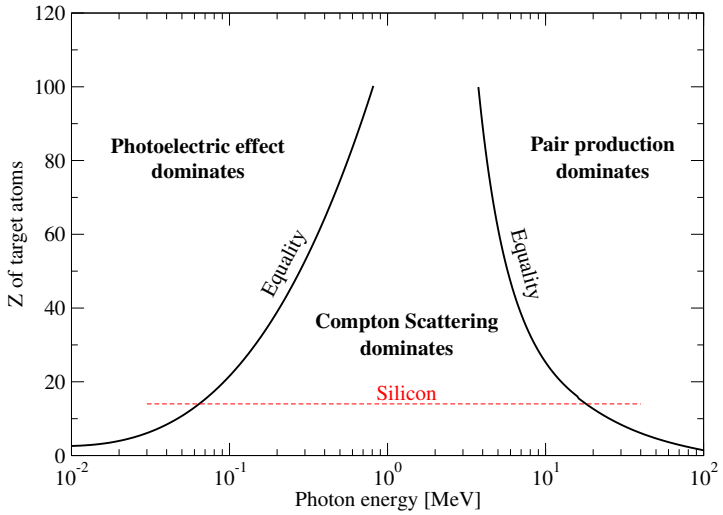


Figure 4.1: Relative importance of the photoelectric effect, Compton scattering and pair production as a function of the incident photon energy. Data taken from [Sch94].

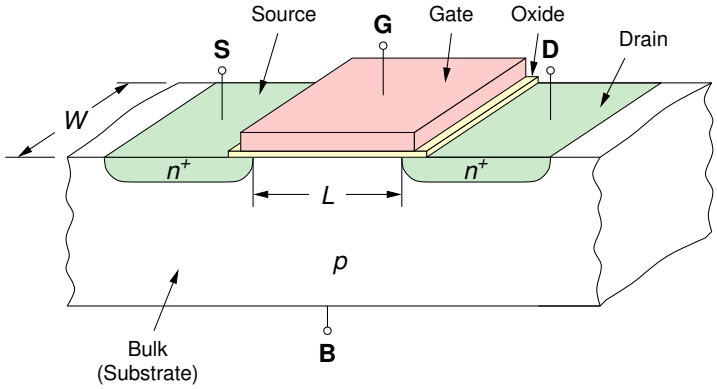


Figure 4.2: Structure of an n-channel MOS transistor. The conductive channel between the source and drain region is underneath the SiO_2-Si interface.

terial. It is expressed through the total absorbed dose. Nuclear displacement gives rise to a neighbouring interstitial atom and vacancy, which are called a *Frenkel pair*. In silicon dioxide at room temperature 90% of the Frenkel pairs recombine within a minute after the end of the irradiation [Ane00]. Displacement damage is usually studied by means of neutron sources.

In the irradiation tests of this thesis (cf. section 6.6) X-rays are used due to the fact that Metal Oxide Semiconductor (MOS) transistors are almost entirely insensitive to displacement damage. In a MOS device (fig. 4.2) the conduction is based on the flow of majority carriers below the SiO_2-Si interface.

4.2 Radiation Effects in MOS Transistors

In contrast to bulk devices like e.g. silicon detectors (cf. section 3), Metal Oxide Semiconductor (MOS) structures are surface devices. The active structures penetrate only a few micrometers into the silicon bulk. A major effect of displacement damage is the reduction of the minor-

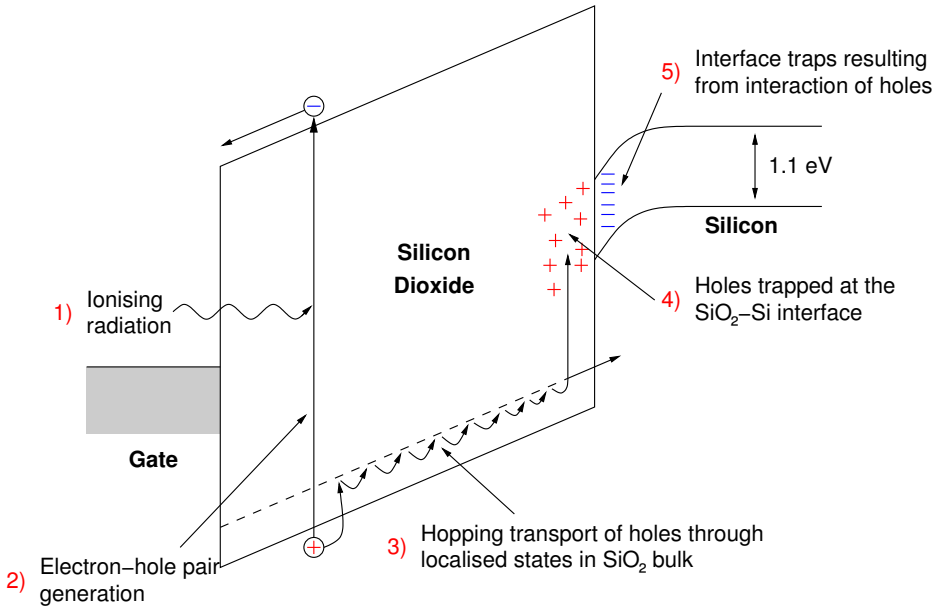


Figure 4.3: Energy band diagram of the effects induced by ionising radiation in a MOS device when the gate is positively biased [McL89]

ity carriers lifetime in the semiconductor bulk. Since the properties of MOS devices do not significantly depend on the minority charge carriers lifetime, they are relative insensitive to displacement damages. In general, displacement damage in MOS transistors is of secondary concern. The primary source of device degradation under irradiation are damages in the surface layers caused by ionisation effects [McL89, Sch94].

4.2.1 Total Dose Effects

The part of the MOS structure (fig. 4.2) which is sensitive to ionising radiation is the insulation layer (silicon dioxide) between the silicon substrate and the electrodes. The insulation layer underneath the gate electrode (gate oxide) is only a few nanometres thick[1] increasing to some 10 nm above the source and drain diffusion regions (field oxide).

Two basic radiation induced effects exist: the *trapping of holes* in the silicon oxide near the SiO_2-Si interface and the creation of SiO_2-Si *interface traps*, which produce inter-bandgap states in the silicon [McL89, Sch94]. Figure 4.3 depicts the energy band diagram of a MOS device with a positively biased gate. When an ionising particle passes through a MOS transistor (fig. 4.3 ①), electron-hole pairs are generated[2]. In the gate (metal or polysilicon) and in the substrate the electron-hole pairs quickly disappear since these are materials of small resistance. In the oxide, which is an insulator, electrons and holes have different behaviours as their mobilities differ by five to twelve orders of magnitude. A fraction of the radiation induced electron-hole pairs will recombine immediately after being generated. The rest of the electron-hole pairs which do not recombine are separated in the oxide by the electrical field (fig. 4.3 ②). In case of a positively biased gate, the electrons drift to the gate in a very short time (order of picoseconds). The holes move towards the SiO_2-Si interface (fig. 4.3 ③) with a very different

[1] For the used 0.25 µm CMOS process of the *Beetle* chip the gate oxide is 6.2 nm thick.
[2] The electron-hole pair creation energy in SiO_2 requires 17 ± 1 eV.

characteristic transport mode. The time scale for this process is in the order of 1 s at room temperature. Close to the interface, but still in the oxide, some of the holes may be captured in long-time traps, giving origin to a fixed positive charge in the oxide (fig. 4.3 ④). This causes a negative voltage shift (e.g. in threshold voltage V_{th} of flatband voltage V_{FB}[3]) which is insensitive to the silicon surface potential. It can persist in time for hours to years. This voltage shift is the most commonly observed form of radiation damage in MOS devices. Also the amount of trapped charge is proportional to the number of defects in the silicon dioxide. For this reason one of the fundamental steps for the fabrication of radiation hardened technologies is the control of the gate oxide quality. Moreover electrons from the silicon may tunnel from the interface border into the oxide and recombine with trapped holes, giving origin to a *tunnel-effect-based annealing*. This tunnel annealing, which tends to reduce the amount of positive charge trapped in the oxide, is explained by two phenomena:

- The recombination of an electron with a trapped hole depends strongly on the local density of the trapped holes and on the cross section of the electron capture. It increases with the total dose and is one of the effects of the threshold voltage shift saturation at high doses.
- Electrons in the oxide valence band, which have a sufficient thermal energy to jump into the oxide, recombine with the holes trapped in the oxide (*thermal annealing*).

The tunnel annealing has an almost logarithmic temporal behaviour. This is a consequence of the tunnel effect probability p_{tun}, which decreases exponentially with the distance from the SiO_2-Si interface. At a given time t the electrons recombine with the holes at a distance $x(t)$ from the interface. $x(t)$ is expressed as [Ben85]

$$x(t) \;=\; \frac{1}{2\beta} \ln \frac{t}{t_0} \tag{4.1}$$

where β is related to the height of the potential barrier and $\frac{1}{t_0}$ is the frequency at which the electrons try to cross the potential barrier. The hole discharge process by tunnel annealing can therefore be seen as a front of electrons moving with a speed of

$$v \;=\; \frac{dx(t)}{d(\log_{10} t)} = \frac{dx(t)}{d(\ln t)} \cdot \ln 10 = \frac{1}{2\beta} \cdot \ln 10 = \frac{1.15}{\beta} \tag{4.2}$$

per decade in time [Ane00]. With an increase of the electrical field (and therefore a reduction of the potential barrier which has to be crossed) the tunnel annealing becomes more effective.

The emission probability p_{em} of an electron from the oxide valence band to the trap where the hole is captured is

$$p_{\text{em}} \;=\; AT^2 e^{-\frac{q\phi}{kT}} \tag{4.3}$$

where ϕ is the difference in energy between the trap and the valence band and A is a constant correction parameter which mainly depends on the trap capture cross section. This expression shows that the thermal annealing is strongly related to the temperature T and does not depend on the spatial distribution of the traps.

[3] The flatband voltage is the voltage that has to be applied to the gate of a MOS in order to have flat energy bands inside the silicon.

Another effect of radiation to MOS devices is the increase of the trap density at the SiO_2-Si interface by several orders of magnitude (fig. 4.3 ⑤) [Win89]. These traps have an energy between the valence and the conduction bands of the silicon. The major part of the traps present above the midgap are acceptors while traps below are donors. A donor trap releases an electron when it passes from below to above the Fermi level E_F[4] and an acceptor trap captures an electron when it passes from above to below the E_F level[5]. Therefore, the threshold of both n-channel and p-channel MOS transistors increases in absolute values after irradiation due to the creation of new interface traps. The creation depends on different parameters like dose and dose rate, electric field, temperature, radiation energy, oxide thickness and more. The dependence on the dose follows a $D^{2/3}$ law and the dependence on the oxide thickness follows a ${t_{ox}}^n$ law (with $0.5 \leq n \leq 2.0$ in a t_{ox}-range of 15 to 100 nm).

4.2.2 Consequences of Radiation on the Electrical Device Characterisation

The consequences of hole trapping in the oxide and of interface traps at the SiO_2-Si interface on the electrical device parameters of a MOS transistor are described in this section.

Threshold Voltage Shift

The threshold voltage V_{th} of a MOS transistor changes if the device is irradiated. The total change of ΔV_{th} is the sum of the two contributions ΔV_{ox} and ΔV_{it}. These two contributions are related to the hole trapping in the silicon dioxide and to the charge state of the interface traps respectively.

Trapped charges in the oxide cause a shift in the flatband voltage V_{FB} and therefore in the threshold voltage. This voltage is given by [Mul86]

$$\Delta V_{ox} = -\frac{1}{C_{ox}} \int_0^{t_{ox}} \frac{x}{t_{ox}} \rho(x)\, dx \tag{4.4}$$

with
- C_{ox} – oxide capacitance per unit area,
- t_{ox} – gate oxide thickness,
- x – distance from the gate-oxide interface,
- $\rho(x)$ – charge distribution in the oxide per unit volume as a function of the distance x.

An important consequence of eq. 4.4 is that the effect of the oxide charge on the voltage shift is determined by the position in the oxide: the closer the charge is located to the SiO_2-Si interface, the bigger the threshold voltage shift will be. Also the voltage shift is e.g. negative when the trapped charge is positive.

The charge distribution, associated with the radiation induced interface traps, can be considered as two-dimensional [Ane00] and is expressed as

$$\Delta V_{it} = -\frac{\Delta Q_{it}}{C_{ox}} \tag{4.5}$$

where ΔQ_{it} is the difference of the charge per unit area which fills the interface states before and after irradiation. The voltage shift ΔV_{it} can have positive or negative values.

[4] Donor traps are neutral when full and positively charged when empty.
[5] Acceptor traps are neutral when empty and negatively charged when full.

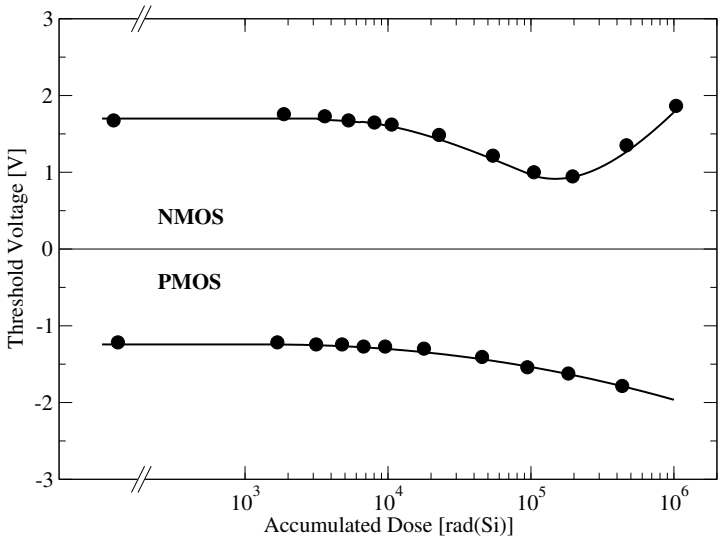


Figure 4.4: Threshold voltage shift of an NMOS and PMOS transistor as a function of the accumulated dose. Data taken from [Win89].

The increase of the interface states is a slower phenomenon than the build-up of positive charge in the oxide. Figure 4.4 shows the threshold voltage shift as a function of the dose. At low accumulated doses ($< 10^5$ rad(Si)) the contribution of the trapped oxide charges ΔV_{ox} dominates and results in a decrease of V_{th}. Above 10^5 rad(Si) negatively charged acceptor interface traps (for NMOS transistors) and positively charged donor interface traps (for PMOS transistors) are formed. For NMOS transistors this results in a turnaround of the threshold voltage shift[6]. For PMOS devices the decrease of the threshold voltage shift continues.

The slower temporal evolution of the radiation-induced interface traps also plays an important role in the annealing of irradiated circuits. During the annealing process ΔV_{ox} decreases and ΔV_{it} increases for both n-channel and p-channel MOS transistors. Therefore, the bias conditions of the circuit are affected by the annealing of MOS devices.

McLean et al. derived an analytical form for the threshold voltage shift [McL89]:

$$\begin{aligned} \Delta V_{\mathrm{th}}(\mathcal{E}_{\mathrm{ox}}, E) &= -\frac{q}{\epsilon_{\mathrm{ox}}} \cdot K_{\mathrm{g}}(E) \cdot f_{\mathrm{y}}(\mathcal{E}_{\mathrm{ox}}, E) \cdot f_{\mathrm{tr}}(\mathcal{E}_{\mathrm{ox}}) \cdot {t_{\mathrm{ox}}}^2 \cdot D(E) \\ &\propto {t_{\mathrm{ox}}}^2 \end{aligned} \tag{4.6}$$

with

$\mathcal{E}_{\mathrm{ox}}$	–	effective electrical field in the oxide,
E	–	energy of the ionising radiation,
K_{g}	–	charge generation coefficient,
f_{y}	–	fraction of generated charge that remains free,
f_{tr}	–	fraction of radiation generated holes that are trapped,
t_{ox}	–	thickness of the silicon oxide,
D	–	accumulated dose.

[6] This effect is also known as *rebound* effect.

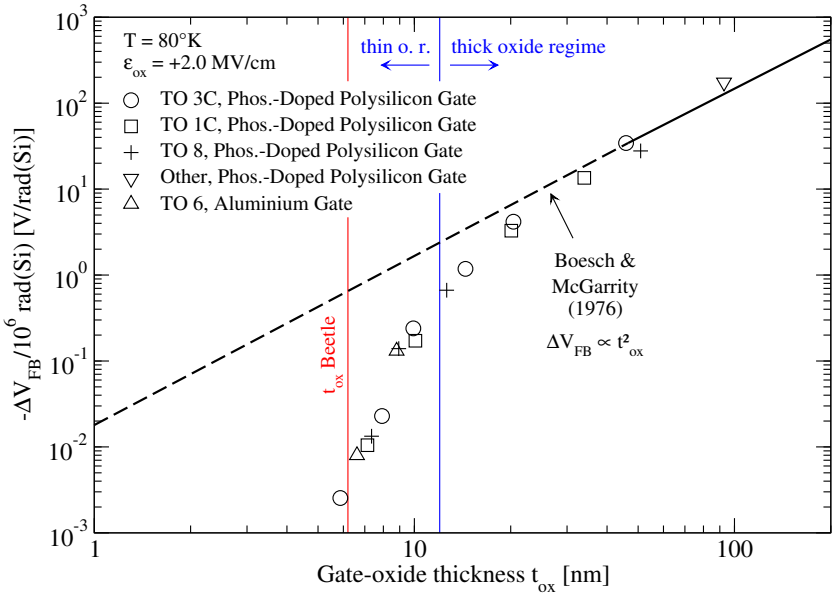


Figure 4.5: Shift of the flatband voltage V_{FB} after an accumulated dose of 10 Mrad(Si) as a function of the gate-oxide thickness t_{ox} of different MOS structures. Data taken from [Sak84].

Figure 4.5 depicts the shift of the flatband voltage V_{FB} after an accumulated dose of 1 Mrad(Si) as a function of the gate-oxide thickness t_{ox} of various MOS structures. The flatband voltage is related to the threshold voltage $V_{\mathrm{th},0}$ with

$$V_{\mathrm{th},0} \;=\; V_{\mathrm{th}}(V_{\mathrm{bs}}=0) \;=\; V_{\mathrm{FB}} + 2|\phi_{\mathrm{F}}| + \gamma\sqrt{2|\phi_{\mathrm{F}}|} \tag{4.7}$$

where ϕ_{F} is the surface or Fermi potential and γ is the bulk threshold parameter. The quadratic dependence of the threshold voltage shift on the oxide thickness (eq. 4.6) is indicated by the dashed line in fig. 4.5. This model is valid for an oxide thickness $t_{\mathrm{ox}} > 12$ nm, where the distance of hole traps to the SiO_2-Si interface $\delta x \ll t_{\mathrm{ox}}$. For thinner oxides the trapped holes are rapidly removed by tunnelling effects (cf. section 4.2.1).

Increase of Leakage Currents

The current through a MOS transistor in its 'off-state' is defined as the current which flows from drain to source when $V_{\mathrm{gs}} = 0$. This current is also called *leakage current*. In an irradiated n-channel MOS transistor, two effects lead to an increase in the 'off-state' current:

- the increase of the *sub-threshold* current and
- the generation of *parasitic* currents.

Both phenomena can be critical for many applications, especially when the transistor is used as a switch.

The increase in the *sub-threshold* current is related to two factors. The first is the decrease of the threshold voltage and the second is the radiation induced decrease of the sub-threshold slope. Figure 4.6 shows a series of sub-threshold $I-V$ curves for n-channel MOS transistors. The transistors are irradiated in steps to a total dose of 1 Mrad(SiO_2) at a dose rate of

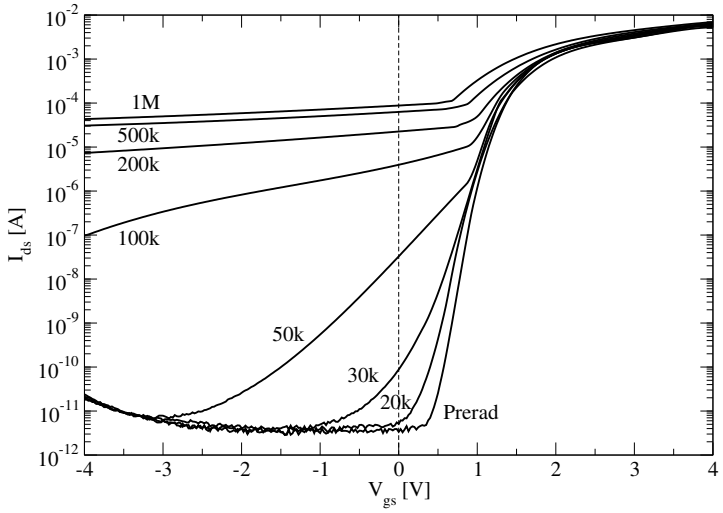


Figure 4.6: Sub-threshold $I - V$ curves for n-channel MOS transistors irradiated at room temperature in steps to 1 Mrad(SiO_2) using 10 keV X-rays at 167 rad(SiO_2)/s. Data taken from [Sha98].

167 rad(SiO_2)/s [Sha98]. The decrease of the sub-threshold slope affects the switching speed of the MOS transistor because a higher swing in gate voltage is required to bring the transistor to strong inversion.

Another contribution to the 'off-state' current of an irradiated n-channel MOS transistor is given by the creation of two *parasitic* paths, illustrated in fig. 4.7. The first parasitic path is in the so called bird's beak region near the thin gate oxide. The bird's beaks are present in CMOS technology when the isolation between devices is done by employing a Local Oxidation of Silicon (LOCOS) process. In deep submicron technologies this isolation has been replaced by Shallow-Trench Isolation (STI), removing the bird's beak effect. The second parasitic path is further away from the MOS device, underneath the thick field oxide, and is present in both manufacturing methods (LOCOS and STI). The contribution of the parasitic paths to the total leakage current dominates over that one due to the sub-threshold current. The parasitic paths are easily created by the radiation since the oxide in these regions is very thick. Therefore, a large amount of holes can be trapped there.

Decrease of Mobility and Transconductance

The mobility degradation after irradiation is related to the increase of the interface traps, since the conduction in a MOS transistor is due to the carrier transport close to the silicon oxide interface. The mobility trend as a function of the increase of the traps is expressed by the empirical formula [Sex85]

$$\mu = \frac{\mu_0}{1 + \alpha \cdot \Delta N_{\text{it}}} \tag{4.8}$$

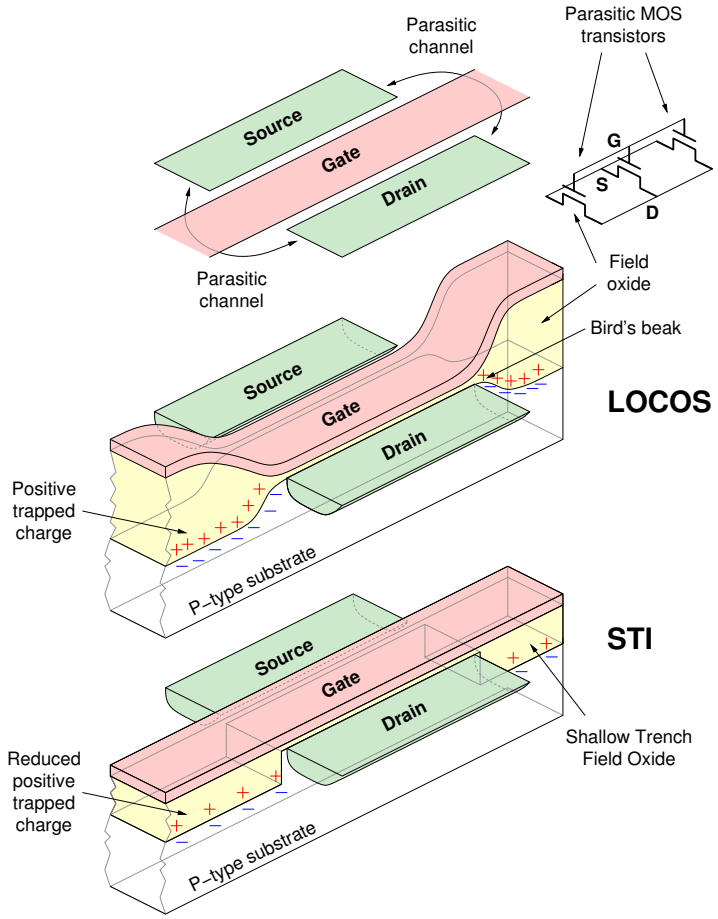


Figure 4.7: Illustration of the parasitic transistors and of the parasitic leakage paths. The parasitic transistors are in parallel to the main transistor. The possible leakage paths are in the bird's beak region or underneath the field oxide which connects the source and the drain.

where μ_0 is the mobility before irradiation, ΔN_{it} is the increase of the interface traps and α is a technology dependent parameter[7]. The degradation of the mobility gives rise to a degradation in the transconductance. It depends on the bias condition of the device and is [Bau03]

$$g_{\mathrm{m}}|V_{\mathrm{gs=const}} = \frac{g_{\mathrm{m0}}}{1+\alpha\cdot\Delta N_{\mathrm{it}}} \quad \text{for fixed voltage biasing,} \tag{4.9}$$

$$g_{\mathrm{m}}|I_{\mathrm{d=const}} = \frac{g_{\mathrm{m0}}}{\sqrt{1+\alpha\cdot\Delta N_{\mathrm{it}}}} \quad \text{for fixed current biasing.} \tag{4.10}$$

Therefore, radiation hard circuit designs use constant biasing of the devices because this is less sensitive to mobility degradation.

[7] Typical value of α is between $6\cdot 10^{-13}\,\mathrm{cm}^2$ and $10^{-12}\,\mathrm{cm}^2$ [Bau03].

4.3 Single Event Effects

Single Event Effects (SEEs) are phenomena caused by an energetic particle passing through an integrated circuit. A SEE generates an immediate malfunctioning of one or more transistors, which can influence the complete circuit. The generated errors can be divided into two groups:

- *reversible errors* or soft errors, which are non destructive effects and
- *non reversible errors* or hard errors, which are destructive effects.

In the 0.25 µm CMOS technology, which is used for the *Beetle* chip, only two effects are of importance: Single Event Upset and Single Event Latch-up [Fac98]. Both effects are discussed in more detail since they can cause a malfunction of the chip during operation at LHCb. Other possible SEEs are described briefly. A more detailed analysis of SEEs can be found in [Ker89, Bea95, Fac99b, Wea02].

4.3.1 Reversible Errors

Single Event Upset (SEU)

An SEU is the instantaneous reversible modification of the logic state of an elementary memory cell like a Static Random Access Memory (SRAM) cell or a Dynamic Flip-Flop (DFF). It is induced by the charges created along the track of an incoming ionising particle (electron-hole pairs by Coulomb-scattering with the lattice atoms), which are collected in the sensitive node of the circuit due to the electrical field. The charge collection dynamics have two contributions [Mas93, Pet97]:

- a *fast* component in the order of 100 ps due to the drift in the depletion region of the *pn*-junction and
- a *slow* component in the order of nanoseconds, which arises from the diffusion in the bulk of the device.

The charge collection can be significantly extended by the *funnelling* effect [Mes86, Mes97]. Figure 4.8 illustrates this funnelling process. The created electron-hole pairs in the depletion region due to an incoming ionising particle distort temporarily the equipotential surfaces of the electric fields in the surrounding area of the particle track. This distortion results in funnel-shaped equipotential surfaces that can extend deep into the bulk region and create a large potential gradient. An enhanced charge collection to the sensitive device node is then the result.

The number of electron-hole pairs created in the silicon depends on the total amount of energy deposited in the matter by the incident charged particle. This amount is related to the Linear Energy Transfer (LET) from the particle to the material. The LET depends on the nature and on the energy of the incident particle and on the absorbing material. It is expressed by

$$\mathrm{LET} = \frac{1}{\rho}\frac{dE}{dx} \tag{4.11}$$

where ρ is the mass per unit volume expressed in $\mathrm{kg/m^3}$ and dE/dx is the mean energy transferred to the material per unit path length. The LET is measured in $\mathrm{J \cdot m^2 \cdot kg^{-1}}$ or, more

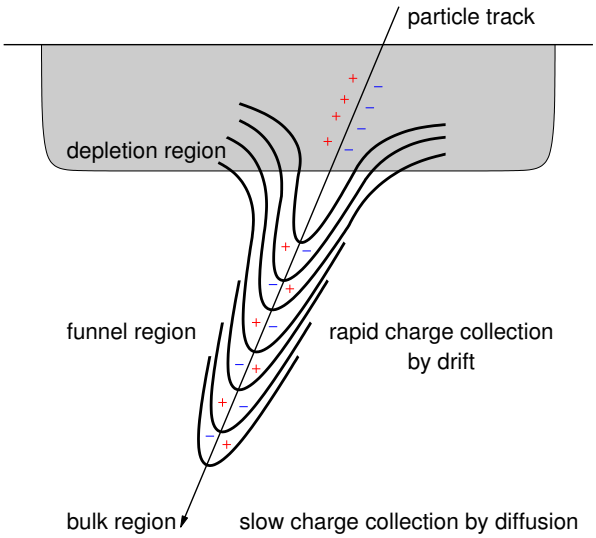


Figure 4.8: Enhanced charge collection by funnelling [Mes86].

conveniently, in $\mathrm{MeV} \cdot \mathrm{cm}^2 \cdot \mathrm{mg}^{-1}$. The number of electron-hole pairs is obtained by dividing the total deposited energy by the energy that is necessary to create an electron-hole pair. In SiO_2 this is equal to $17 \pm 1\,\mathrm{eV}$ per electron-hole pair respectively 3.6 eV in silicon [Ben86].

For each device there is a minimum charge quantity called *critical charge*, which is needed to generate an SEU. Since the charge generated by the incident particle is directly proportional to its LET, for each device there is a critical LET. If the incident particle has a LET higher than the critical LET, the device will be vulnerable to SEUs.

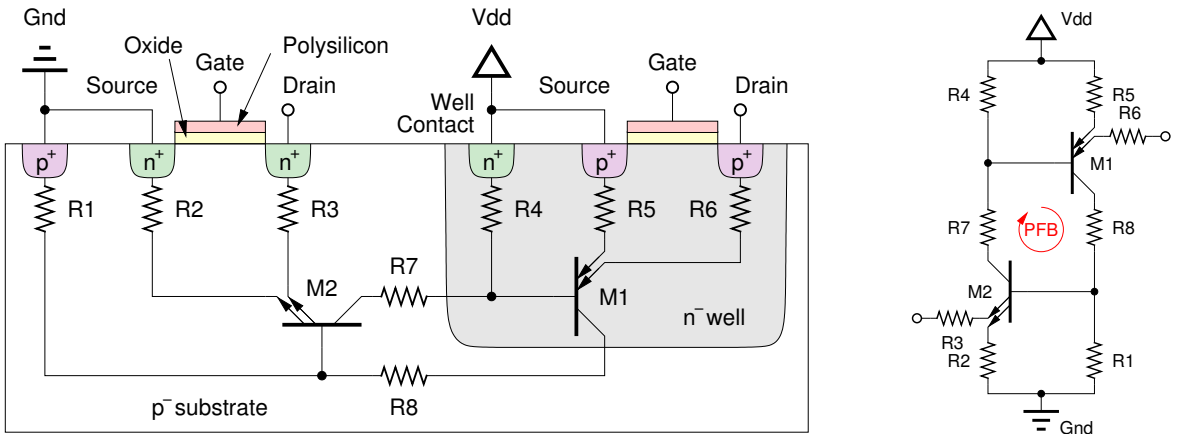
To create an Single Event Upset, potential candidates are *heavy ions* which have a large stopping power or *hadrons* such as protons, pions or neutrons which have a low LET[8]. Here the recoil energy of the inelastic interaction creates the SEU. The recoils typically have rather low energies, rarely exceeding 10 MeV. Thus, their range is very limited (below about 10 µm) which means that they have to be produced locally in the chip itself in order to induce an SEU (cf. also the cross section of the used CMOS technology in fig. 4.10).

Multiple Bit Upset (MBU)

A MBU error is analogous to the SEU, but more than one device is affected at the same time. There are three possibilities that can cause this error:

- A particle strikes the Integrated Circuit at an angle very close to 90°, crossing in this way the sensitive volume of more adjacent devices at the same time.
- A particle strikes the IC almost perpendicularly but has enough energy to be able to change the information contained in more than one sensitive node.
- Two particles hit two adjacent devices, modifying the information contained in them.

[8] E.g. for 65 MeV protons used in the SEU irradiation test (cf. section 6.7) the LET is $0.008\,\mathrm{MeVcm^2mg^{-1}}$ and the penetration depth in silicon is 18 mm [Joh99].



(a) Cross section

(b) Circuit schematic

Figure 4.9: Schematic illustration of the parasitic thyristor in an n-well CMOS process.

Single Event Functional Interrupt (SEFI)

A SEFI error can also be thought as a particular case of SEU. In complex memories, the memory cells and the peripheral circuits are connected to other circuits with additional features, as for example Error Detection and Correction. If an energetic particle strikes one of these circuits, the error will influence the functioning of the whole ciruit.

Single Event Disturb (SED)

A SED is a temporary disturbance of digital information stored in a memory bit.

Single Event Transient (SET)

A SET consists of a transient voltage pulse generated at that node that propagates to the device output. It appears there as the same voltage transient, an amplified version of this transient or a change in the logical output.

4.3.2 Non Reversible Errors

Single Event Latch-up (SEL)

Single Event Latch-up is a phenomenon which can occur in CMOS circuits [Mul86, Joh96]. It consists of the turning on of a parasitic *pnpn* sandwich structure (called thyristor) which can short the power lines. This allows a sudden current flow which can destroy the device if not interrupted promptly. Figure 4.9(a) illustrates such a CMOS transistor pair and its parasitic structures. The thyristor structure provides a positive feedback (PFB) since the collector of the *npn* transistor `M2` is connected to the base of the *pnp* transistor `M1` and visa versa (fig. 4.9(b)). This high current state (latch-up) is only possible if the following conditions are satisfied:

- the parasitic thyristor structure must be present,
- the two parasitic bipolar devices must be forward biased,

- the loop gain product must be $\beta_{npn} \cdot \beta_{pnp} \geq 1$,
- the power supply must be able to sink the current which is required by the parasitic thyristor.

Electrical latch-up may also be initiated by electrical transients on the input/output lines, high temperature or improper sequencing of power supply biases. These causes are normally only addressed by the manufacturer and are avoided by special design and layout constraints (e.g. antenna rules).

A latch-up can be prevented by decreasing the loop gain of the structure. This can be achieved in the circuit layout by a geometrical separation of the CMOS device pairs which helps to reduce the β_{npn} since the base of the `M2` increases. Also the reduction of the contact resistances `R1` and `R4` by adding additionally substrate or well contacts or surrounding the MOS devices with guard rings (cf. section 4.4.3) will help. Since the resistances are smaller, more current has to flow through the resistances to gain a sufficiently high voltage drop to forward bias the base-emitter junction of both parasitic bipolar transistors.

Single Hard Error (SHE)

If an energetic particle crosses the gate oxide layer of a MOS transistor, it can deposit a sufficiently large total dose to induce a threshold voltage shift [Duf92]. The sub-threshold current of an NMOS transistor in a SRAM cell can then become high enough to block the stored information in the high or low logic state.

Single Event Snapback (SES)

The SES effect relies on a feedback mechanism, but it does not need a parasitic *pnpn* structure (like SEL) to occur. In an NMOS transistor, which carries a large current, the parasitic *npn* bipolar transistor can be turned on by an avalanche mechanism. This mechanism is initiated in the drain junction by an ionising particle and provokes the injection of holes in the substrate region underneath the gate. This act as the base current of the parasitic bipolar transistor which induces the injection of electrons from the source (emitter) to the drain (collector). This again increases the current intensity, reinforces the avalanche mechanism and closes the feedback loop. SES is in most cases related to high power supply voltages [Bei88].

Single Event Burn Out (SEBO)

The SEBO effect is present in power MOSFETs and bipolar transistors, since these devices contain a parasitic bipolar transistor [Hoh87]. An ionising particle can turn on the bipolar transistor. If the transistor is able to conduct enough current, the locally dissipated power can be high enough to melt the transistor.

Single Event Gate Rupture (SEGR)

The SEGR event consists of the localised dielectric breakdown of the gate oxide by an ionising particle. It is especially important in the situation where there is a high electrical field on the gate oxide (e.g. during the write or erasing phase of an EEPROM or in power MOSFETs) [Whe94].

Quantity	Scaling factor	Quantity	Scaling factor
Device dimension (L, W, t_{ox}, d)	$1/\alpha$	Capacitances	$1/\alpha$
Gate area	$1/\alpha^2$	Capacitances per unit area	α
Devices per unit of chip area	α^2	Charges	$1/\alpha^2$
Doping concentration N_a	α	Charges per unit area	1
Bias voltages and threshold voltage V_{th}	$1/\alpha$	Electric field intensity	1
Bias currents	$1/\alpha$	Body effect coefficient (γ)	$1/\sqrt{\alpha}$
Power dissipation for a given circuit	$1/\alpha^2$	Transistor transit time (τ)	$1/\alpha$
Power dissipation per unit of chip area	1	Transistor power-delay product	$1/\alpha^3$

Table 4.1: Constant field scaling factors [Ane00].

4.3.3 Summary on Single Event Effects

In the last two sections all possible Single Event Effects which can occur in Integrated Circuits have been described. Since this thesis focuses on the development of the *Beetle* chip in a deep submicron CMOS technology, several of these effects can be ignored. Single Hard Error was a problem in older technologies with thick gate oxide, Single Event Burn Out is an issue in power MOSFET transistors and Single Event Snapback need high supply voltages. Single Event Gate Rupture could be an issue, since the electrical field in the oxide increases by scaling down the technology. However, in the total dose irradiation test (cf. section 6.6) and in the Single Event Upset irradiation test (cf. section 6.7) with the *Beetle* chip no Single Event Gate Rupture could be found. Therefore, this work will concentrate in Single Event Effect related sections only on Single Event Upset and Single Event Latch-up effects.

4.4 Radiation Hard VLSI Design

In this section the scaling laws of CMOS technologies (section 4.4.1) and the choice of the process technology are described (section 4.4.2). An overview of the radiation hard layout techniques follows in section 4.4.3.

4.4.1 Technology and Transistor Scaling

The scaling of the technology is directly associated with the scaling of the transistor device parameters. A VLSI technology is characterised by the minimum structure width, which is in case of a CMOS technology the gate length of a transistor. The technological gain of scaling towars smaller dimensions is to reduce the device dimension, to increase the transistor density and circuit speed and to lower the power consumption without introducing effects which can disturb the good operation of the devices in a former technology. For process technologies below 0.8 µm minimum structure size, the underlying scaling principle is the *constant field scaling* [Dav95]. In this approach the device and its depletion region are a scaled down version of a larger device. All physical device dimensions are divided by a factor α to obtain the scaled down version. Also the voltages are divided by this factor α. In this way the electrical fields in the scaled device are similar to that of the larger one. A summary of the scaling factors for the various physical quantities of a CMOS technology is given in table 4.1. Present technology scaling uses a factor $\alpha \approx 1.43$ or 30% parameter change ($1/\alpha \approx 0.7$) from one technology generation to the next.

The constant field scaling presents some problems related to the decrease of the power supply voltage and to the fact that the weak inversion slope does not scale. In practice the threshold voltage can not be scaled by $1/\alpha$ to avoid too high off-state weak inversion currents. This will lead to some problems to analogue designers in future technologies.

An alternative approach is the *constant voltage scaling*. In this case the device dimensions are scaled as before, but the voltages are not scaled. The big disadvantage of that scaling procedure is the increase of the electric field in the oxide, causing serious undesirable effects like SEGR.

A further advantage of scaling the process technologies down to smaller feature sizes is the higher tolerance concerning irradiation (cf. section 4.2.1). Process modifications and special layout techniques, described in section 4.4.3, reduces the vulnerability to Single Event Latch-up (section 4.3.2). The major disadvantage due to scaling is an increased sensitivity to Single Event Upset effects (section 4.3.1).

4.4.2 Process Technology

As described in section 4.2, the threshold voltage shift is dominated by the holes trapped in the silicon oxide. The inherent sensitivity to irradiation can be drastically reduced by scaling down the technology and therefore the device dimensions (cf. fig. 4.3). Below an oxide thickness of about 12 nm the quadratic dependence of the threshold shift ΔV_{th} on the oxide thickness is, due to tunnelling of the trapped charges out of the oxide, no longer given. Therefore process technologies with an oxide thickness smaller than 12 nm should be used for a radiation hard circuit design.

For the development of the *Beetle* chip a standard commercial 0.25 µm CMOS process was chosen with a gate oxide thickness of 6.2 nm. A cross section of this technology is shown in fig. 4.10. The process features three metal layers for interconnections (M1, M2 and MZ), one metal layer for capacitors (Q2) and one polysilicon layer (PC). The RX area represents the thin oxide and $n+/p+$ diffused regions, CA, V1 and V2 are the vertical interconnecting contacts between the different routing lines. Besides the use of NMOS and PMOS transistors, this process allows to build resistors (polysilicon, diffusion, n-well) and linear Metal-Insulator-Metal Capacitors (MIMCAPs) which are important devices for analogue circuit designs. In this technology the bulk is formed of a p-doped epitaxial layer on a strongly p-doped ($p+$) substrate. The nominal power supply voltage is 2.5 V.

4.4.3 Layout Techniques

Edgeless Transistor (ELT)

The primary problem which has to be addressed is the post-irradiation leakage current inside the n-channel MOS devices. Figure 4.7 shows this leakage problem in a linear transistor. MOS transistors using an enclosed gate structure, also called Edgeless Transistors (ELTs), avoid the parasitic paths between source and drain. Figure 4.11(b) shows the principle drawing of the ELT geometry. The disadvantages in using the ELT layout instead of a linear layout (fig. 4.11(a)) are:

- increase of the transistor area (decrease of the device density),
- lack of symmetry,

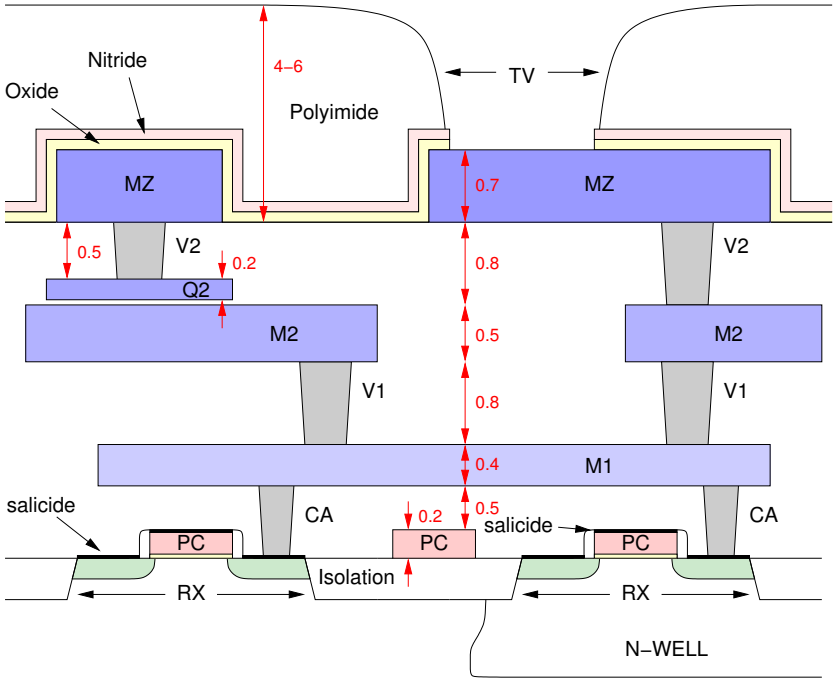


Figure 4.10: Cross section of the 0.25 µm CMOS technology. All dimensions (red) are given in µm and are rounded to one position after the decimal point.

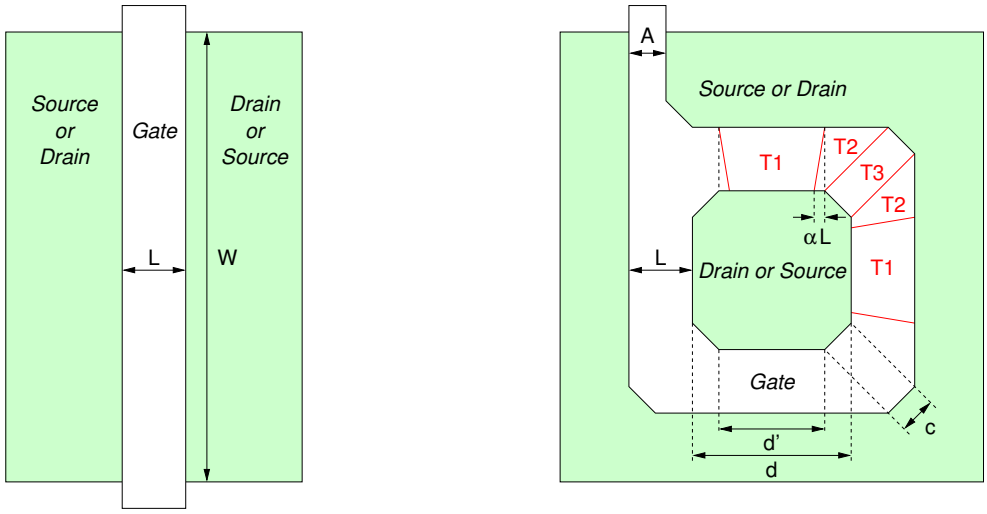
- difficulties in modelling the W/L ratio,
- increase in the gate, source and drain capacitances,
- limitations in the choice of the W/L ratio.

The modelling of the W/L ratio of an ELT shape depicted in fig. 4.11(b) is given by [Fac98, RD00]

$$\left(\frac{W}{L}\right)_{\text{eff}} = \underbrace{4 \cdot \frac{2\alpha}{\ln \frac{d'}{d'-2\alpha L}}}_{\texttt{T1}} + \underbrace{2K \cdot \frac{1-\alpha}{\frac{1}{2}\sqrt{\alpha^2+2\alpha+5} \cdot \ln \frac{1}{\alpha}}}_{\texttt{T2}} + \underbrace{3 \cdot \frac{c}{\sqrt{2}\,L}}_{\texttt{T3}} \tag{4.12}$$

where c, d, d'[9] and α are marked in the drawing. Equation 4.12 has been derived by decomposition of the ELT in three parts, labelled `T1`, `T2` and `T3` in fig. 4.11(b) which are represented in the formula by three terms. The first part (`T1`) corresponds to the linear edges of the transistor, the second part to the transistor corners (`T2`) without the transistor `T3` and the third part to the 45° angle transistors (`T3`). Due to the presence of the polysilicon strip which is necessary to integrate the gate contact outside the thin gate oxide region, the third term in eq. 4.12 is multiplied only by 3. Since the strip has a constant width A, independent from the gate length L, the parameter K is geometry dependent. For short channel transistors ($L \leq 0.5\,\mu\text{m}$) typical value $K = 3.5$ since the polysilicon strip hides one of the transistor `T2`. For longer channel devices one has $K = 4$. The fitting parameter α is needed to identify the borderline between `T1` and `T2` and is almost technology independent ($\alpha = 0.05$) [Gir00].

[9] $d' = d - c\sqrt{2}$



(a) Linear Transistor (b) Enclosed Transistor

Figure 4.11: Geometry of linear (a) and enclosed (b) transistors. The enclosed transistor can be thought of as being formed by three different transistors in parallel, labelled with T1, T2 and T3.

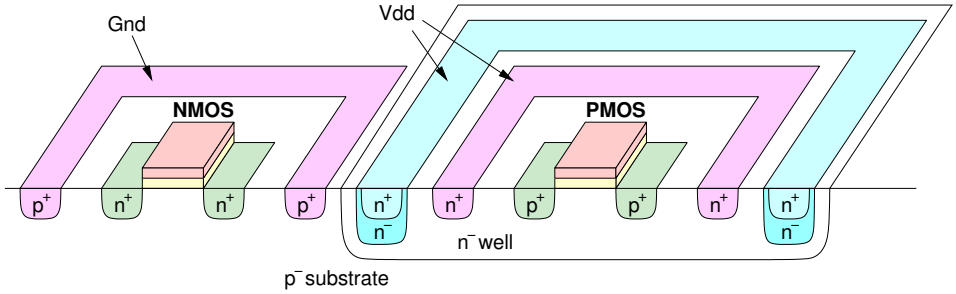


Figure 4.12: Principle of guard rings around MOS structures.

The ELT is not a symmetric device because the two diffusion regions (inner and outer region) differ in area. The outer diffusion region acts usually as the transistor source, providing a higher output conductance but also a larger overlap capacitance. This asymmetry increases with the gate length and has to taken into account in the circuit design.

Guard Rings

The implementation of guard rings surrounding the MOS is shown in fig. 4.12. This layout structure offers a low impedance path to the local substrate – for an NMOS transistor it is the p-substrate and for a PMOS transistor it is the n-well. This prevents the generation of a Single Event Latch-up (cf. section 4.3.2) because the resistances `R1` and `R4` in fig. 4.9 are reduced. In addition the distance of the diffusion regions between neighbouring MOS transistors is increased (`R7` and `R8`) which suppresses the positive feedback of the thyristor structure. The disadvantage of the systematic use of guard rings is the higher area consumption. For example, a logic gate integrating guard rings needs about 60% more area [Bau03].

Chapter 5

The *Beetle* Readout Chip

This chapter describes the *Beetle* readout chip. The chip is developed for the Large Hadron Collider beauty (LHCb) experiment, more precisely for the readout of the Vertex Locator, the Pile-Up System, the Trigger Tracker, the Inner Tracker and the Ring-Imaging Cherenkov detector. The latter only in case of multi-anode photomultiplier readout option. The chip integrates 128 channels with low-noise charge-sensitive preamplifiers and shapers, an analogue pipelined memory and a multiplexer. The chip meets all specifications given by the experiment and will be used in its present state in the LHCb experiment.

In section 5.1 the key parameters of the detectors as well as the requirements on the readout chip are described in detail. Section 5.2 gives an overview of the basic functionality and the different signal flows through the *Beetle* chip. In section 5.4 to 5.12 the circuitry of the major subcomponents are described. The chapter will refer to *Beetle1.3* and is valid for the later chip versions *1.4* and *1.5*, unless otherwise noted.

5.1 Requirements on a Readout Chip

The requirements on the *Beetle* readout chip are specified by the parameters of the different sub-detectors that will be read out by the *Beetle* and by the constraints of the standardised LHCb trigger and data acquisition system, which are common to all electronic devices in the corresponding trigger level. For the Pile-Up System (PUS) the *Beetle* operates within the Level-0 (L0) electronic and provides a prompt trigger information. As the readout chip for the Vertex Locator (VELO), the Trigger Tracker (TT), the Inner Tracker (IT) and the Ring-Imaging Cherenkov (RICH), the *Beetle* operates within the High Level Trigger (HLT) and must therefore cover the Level-0 latency. The key parameters of the LHCb sub-detectors to be read out by the *Beetle* chip are summarised in table 5.1. Together with the trigger and readout requirements (cf. table 2.6) this results in the *Beetle* specifications that are listed in table 5.2.

The sampling frequency of the *Beetle* chip equals the LHC bunch crossing frequency of 40.08 MHz and defines therefore the peaking time of the shaper. Pulse remainder and Signal-to-Noise (S/N) ratio are related to the hit finding efficiency. Depending on the channel strip occupancy, a long undershoot setting time also results in an efficiency loss due to the effect of signal reduction at the front-end output. The maximum input charge rate directly correlates with the channel occupancy. The power consumption of the *Beetle* chip is limited by the maximum cooling capability of the VELO system, where the chip operates in the secondary

Parameter	VELO	PUS	Silicon Tracker TT	Silicon Tracker IT	RICH
Technology	silicon strip (r-ϕ) single-sided, n-on-n		silicon strip single-sided, p-on-n		MaPMT
Number of channels	172 032	8 192	143 360	129 024	440 000
Channel pitch	r: $40-100\,\mu m$ ϕ: $35-100\,\mu m$		$183\,\mu m$	$198\,\mu m$	—
Detector thickness	$300\,\mu m$		$500\,\mu m$	$320\,\mu m$ $410\,\mu m^\star$	—
Detector capacitance	$<10\,pF$		$41-60\,pF$	$22-40\,pF$	$\approx 2\,pF$
Charge of a MIP	$22\,500\,e^-$		$37\,500\,e^-$	$24\,000\,e^-$ $30\,000\,e^-$	$\approx 300\,000\,e^-$
Channel occupancy	$\leq 1\%$		$\leq 2\%$	$\leq 2.3\%$	$\leq 4\%$
Readout coupling	AC		AC		DC
Total accumulated dose in 10 years (maximum)	5.8 Mrad		7.00 Mrad	1.10 Mrad	24 krad
Total accumulated dose in 10 years (average)	2.5 Mrad		0.37 Mrad	0.49 Mrad	17 krad
Operation environment	secondary vacuum		air/nitrogen		air
Ambient temperature	-10 to -5°C		5°C		25°C

Table 5.1: Summary of the key parameters of the LHCb sub-detectors, which are read out by the *Beetle* chip [Rad04, TDR3, TDR5, TDR8, TDR9, Sma04, Nee05, Vol05].

* IT sensor thickness: 410 µm for the left/right sensors, 320 µm for top/bottom sensors.

Beetle parameter	Value	*Beetle* parameter	Value
Input channels	128	Acceptance of consecutive triggers	yes
Input channel pitch	$40-60\,\mu m$	Depth of multi-event buffer	16 events
Front-end peaking time t_p [0/100]	≤ 25 ns	Time between two readouts	0 ns
Pulse remainder 25 ns after peak	$< 30\%$	Readout time per event	≤ 900 ns
Signal-to-Noise ratio after 10 Mrad	> 14	Power consumption per channel	≤ 6 mW
Dynamic input range	$\pm 110\,ke^-$	Analogue output driving capability	≥ 10 m
Linearity of dynamic range	$\leq 5\%$	Acceptable total dose	≥ 10 Mrad
Tolerable DC input current	> 15 nA*	SEU detection and correction	yes
Detector capacitance	$5-30\,pF^\dagger$	Synchronisation check	yes
Sampling frequency	40.08 MHz	Programming interface	I^2C
Acceptable trigger rate	1.1 MHz	Digital input signals	LVDS
Maximum latency	4 µs		

Table 5.2: Requirements to the *Beetle* readout chip [Sch01].

* Assuming a 10% channel occupancy and an input charge signal of $24\,000\,e^-$.

† The requirements on the *Beetle* chip were defined before the knowledge of a possible future TT station. So the detector capacitance parameter violates of the *Beetle* the requirements on the TT station (cf. table 5.1).

vacuum. The input pitch of 40.24 µm of the *Beetle* chip adapts to the average strip pitch of the silicon strip detectors which are used in the VELO system.

5.2 *Beetle* Chip Overview

The development of the *Beetle* profited from the experience with the *HELIX128* readout chip for HERA-B [Sex97, Fal98, Tru00], which has been developed in the ASIC laboratory Heidelberg [ASIC]. Both chips implement the basic front-end electronics architecture from the CERN-research group RD-20 [Gad92, Bin93, Hor93, Bre94a, Bre94b], with adjustments to the specific requirements set by the detector and readout applications in the HERA-B and LHCb experiments. Figure 5.1 depicts the schematic block diagram of the *Beetle* chip. The chip integrates 128 channels, each consisting of a low-noise charge-sensitive preamplifier, an active CR-RC pulse shaper and a buffer. Together, they form the analogue front-end of the *Beetle*. The outputs of the front-ends are sampled into the pipeline in parallel with the nominal LHC bunch-crossing frequency of 40.08 MHz. The pipeline is an analogue memory realised as a switched-capacitor array of 130 × 187 cells. The memory provides a programmable latency at maximum 160 clock cycles and integrates a 16 stages derandomising buffer. Each pipeline cell of a single channel is connected via a *write*-switch to the output-line of the front-end or the output of the comparator respectively and via a *read*-switch to the resettable charge-sensitive pipeline readout amplifier (pipeamp). The operation of all switches is controlled by the *pipeline and readout control*. It receives the incoming trigger signals, flags the corresponding pipeline column such that it is not overwritten by the front-end until readout, and stores the Pipeline Column Number (PCN) into the derandomising trigger buffer (FIFO). The oldest FIFO number indicates the next column to be read out by the pipeline amplifier, which is done concurrently to the write-operation to the pipeline. The pipeline readout amplifier then loads the stored signal to the analogue multiplexer for serialisation, which can be operated in three different modes (carrying the information of the 128 channels on either 4, 2 or 1 output ports). The output of a *sense channel* is subtracted from the analogue output of the multiplexer to compensate on-chip common mode effects. Within the Level-0 readout time of 900 ns, differential current drivers bring the data off chip. Behind the front-end, each channel is equipped with a comparator, which optionally discriminates the front-end output pulses. The threshold is adjustable for each channel individually and both signal polarities can be processed by the comparator.

A charge injector with adjustable pulse height and different polarities (*test generator*) is implemented in front of each preamplifier and allows test and calibration of the analogue readout path. For laboratory test purposes a *test channel* is implemented. This channel enables direct access to the output of the front-end and to the pipeline readout amplifier.

For the biasing of the analogue stages, 5 different voltages and 11 different currents are needed. They are generated on-chip by Digital-to-Analogue-Converters (DACs) with a resolution of 8 bits and a maximum output of 2.5 V or respectively 2 mA. An integrated stabilised current source provides the necessary reference current for the DACs. The programming of all bias and configurations registers is controlled by the I^2C-interface of the *Beetle*, which meets the I^2C-standard [Phi95]. It provides write and read access to the configuration registers, which is a requirement to the LHCb front-end electronics (cf. sec. 5.1).

The layout of the *Beetle1.3* and the corresponding floor plan are depicted in fig. 5.2. The chip has an overall size of $5.4 \times 6.1\,mm^2$. The arrangement of the different building blocks

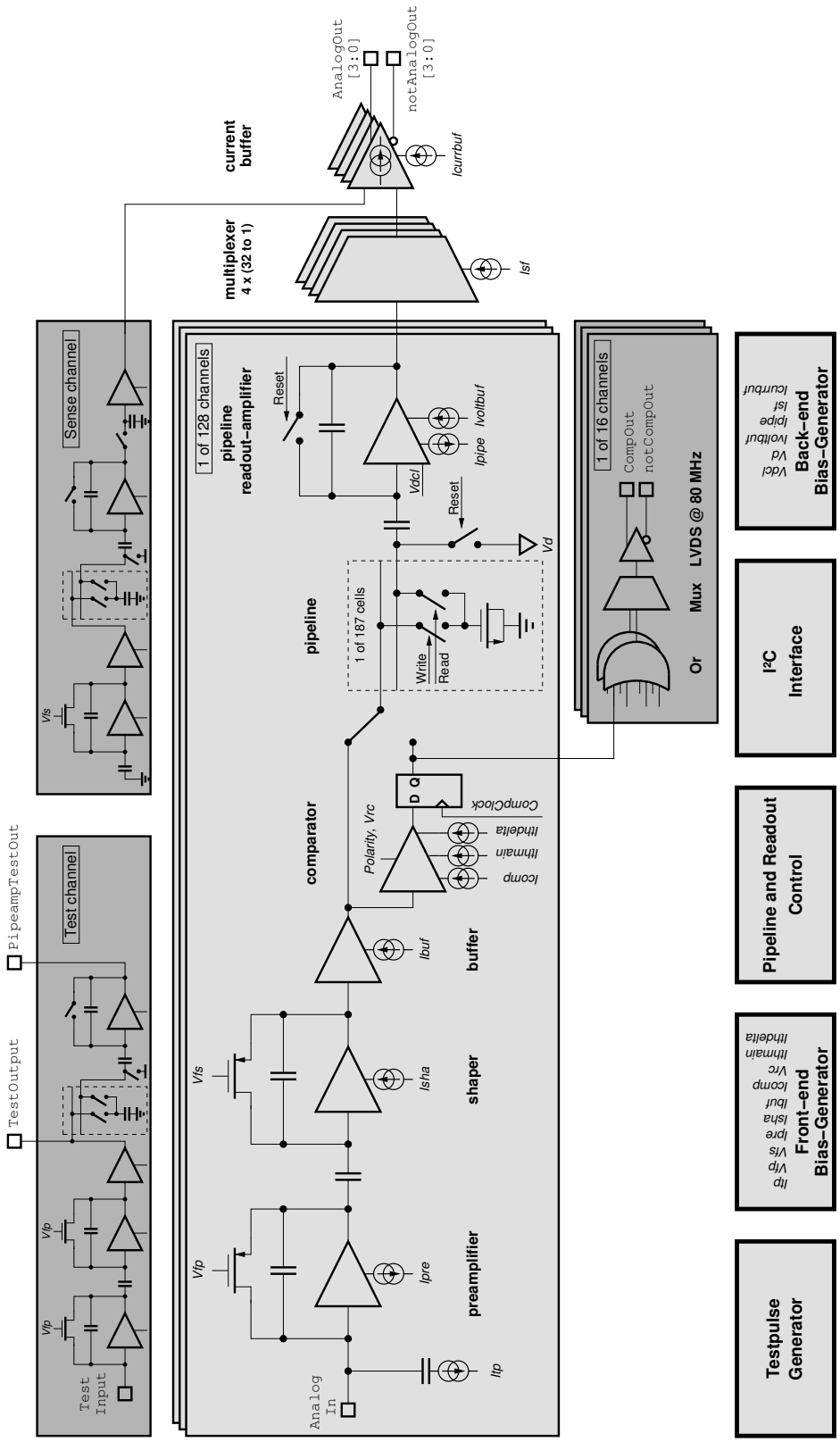
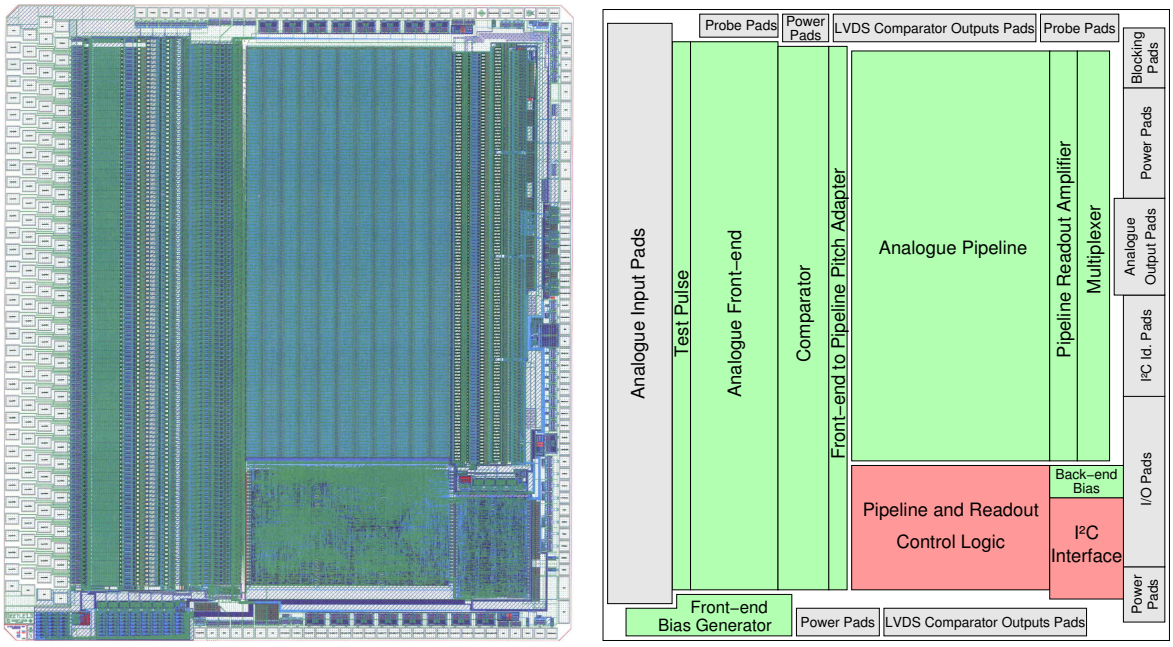


Figure 5.1: Schematic block diagram of the *Beetle* readout chip.



(a) Layout (b) Floor plan

Figure 5.2: Layout (a) of the *Beetle1.3* chip and its corresponding floor plan (b). All analogue building blocks in the floor plan are coloured in green whereas the digital parts are kept in red. The chip dimension is 5.4 mm × 6.1 mm.

follows to some extend the signal path of the block diagram of fig. 5.1. On the left side of the chip the 128 analogue input pads are located. They are designed in a fourfold staggered layout which leads to an effective input pitch of 40.24 µm with an elongated pad opening size of 120×95 µm^2 for each front-end input. Each input pad has its own protection diode to prevent damage to the front-end circuitry caused by Electro-Static Discharge (ESD) events. The test pulse circuitry, the front-end and the comparator are linked up to one common building block with a channel-to-channel pitch of 40.24 µm. Below this the front-end bias generators are placed, which provide the 7 currents and 3 voltages for the latter building blocks. Between the comparator and the pipeline a pitch adapter is implemented to reduce the channel-to-channel pitch from 40.24 µm to 30 µm. This channel width is kept fixed for the following pipeline, pipeline amplifier and multiplexer part. Below the analogue pipeline, the digital pipeline and readout control circuitry (*fast control*) is placed. Right to the fast control the I^{2}C-interface (*slow control*) is located. Below the pipeline amplifier and multiplexer and atop of the I^{2}C-interface the back-end bias generator block is placed. It generates the necessary 3 currents and 2 voltages for the pipeline readout amplifier, the analogue part of the multiplexer and the programmable current for the four analogue output drivers. These drivers are located at the right edge of the *Beetle* chip, together with control, blocking and power supply pads. The pads on the top and bottom side of the chip provide the LVDS outputs as well as the power supply pads for the comparator. If the comparator operation is not used, the pads on the top and bottom side do not need to be connected. This allows then an overall pitch of less than 50 µm when mounting several chips side by side. A list and a description of all *Beetle* bond pads is given in appendix C.7.

5.3 Readout paths

The *Beetle* chip provides two different possibilities of sampling the signal information into the pipeline:

- In the *analogue pipelined readout* the analogue output of the front-end is routed to the pipeline. The semi-Gaussian output pulse is sampled with the sampling clock (*Sclk*) and stored into the pipeline.
- In the *binary pipelined readout* mode the output of the front-end propagates to the comparator and is discriminated. The logic output levels are converted to two analogue voltages, matching the dynamic range of the *Beetle*, and are stored into the pipeline.

The mode of operation is controlled by the *PipelineMode* bit of register *CompCtrl*. A trigger signal reads the stored event from the pipeline via the pipeline readout amplifier to the multiplexer. Here, three different multiplexer readout options (controlled by register *ROCtrl*) can be used:

- In the *analogue output mode* 4 current output driver ports are running in parallel, each reading out 32 channels. The readout works at the nominal data rate and needs 36 clock cycles (4 clock cycles for the readout header and 32 cycles for the channel information). This option is the readout mode for the VELO, PUS, TT and IT detectors.
- In the *binary output mode* 2 ports are running in parallel, each carrying the information of 64 channels. The readout works with double date rate and needs again 36 clock cycles. This operation mode is designed for the RICH MaPMT readout option.
- The *test output mode* transmits all 128 channels analogue on 1 output port. The readout lasts 144 clock cycles (16 for the header and 128 for the channels) and is used for applications with less demanding readout speed requirements or the need for a minimum number of output lines.

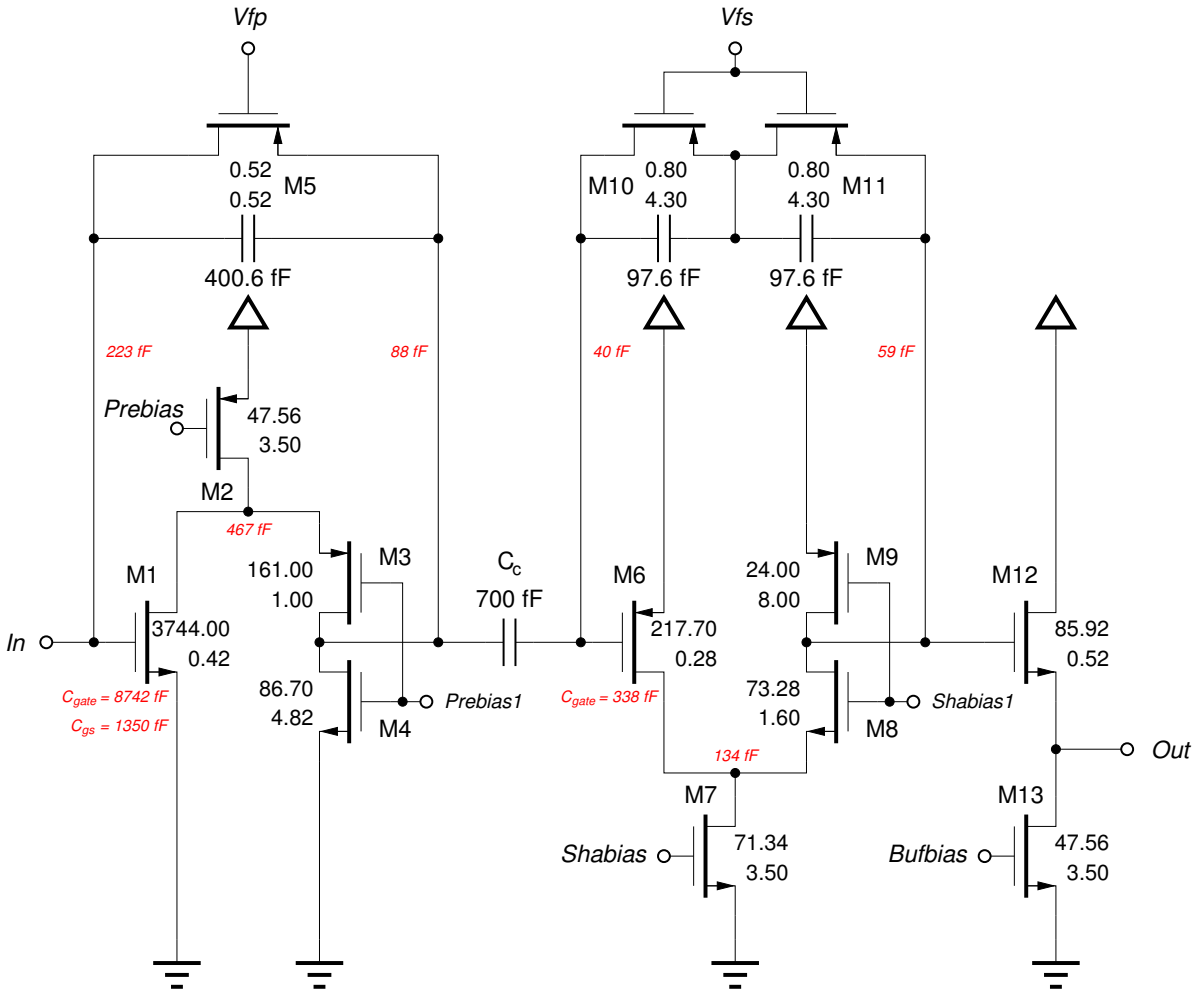
In the case that the *binary pipelined readout* is used, the output characteristics meet the LVDS standard [NSC04].

Independent from both pipelined modes the *Beetle* provides a so-called *prompt binary readout* mode. Here the discriminator output of the comparator is synchronised with the comparator clock (*CompClock*). Always four adjacent channels are logically ORed and routed directly off chip via the LVDS drivers at the top and bottom side of the chip. The transmission is done on both clock phases (double data rate) to reduce the number of necessary output drivers.

In the following sections the main analogue components of the *Beetle* chip are described. The underlying design concepts are discussed, following the signal flow from the front-end to the analogue output buffer (cf. fig. 5.1).

5.4 Front-end

The front-end of the *Beetle* chip consists of a charge-sensitive preamplifier, followed by a CR-RC shaper and an output buffer. The core of the preamplifier and the shaper is designed as a *folded cascode* whereas as the buffer is built as a *source follower*. Figure 5.3 shows the schematic of the three front-end stages.



(a) Preamplifier (b) Shaper (c) Buffer

Figure 5.3: Schematic of the *Beetle* Charge-Sensitive Amplifier (CSA). It is formed by the preamplifier, the shaper and the buffer. The W/L dimensions of the transistors, the capacitances and the current nodes are depicted in the schematic as well as the parasitic capacitances of the line routing (red), extracted from the final layout. The gate-oxide capacitance ($C_{\text{gate}} = 8.74\,\text{pF}$) and the gate-source overlap capacitance ($C_{\text{gs}} = 1.35\,\text{pF}$) of the input transistor `M1` and the routing capacitance (223 fF) contribute to the input capacitances.

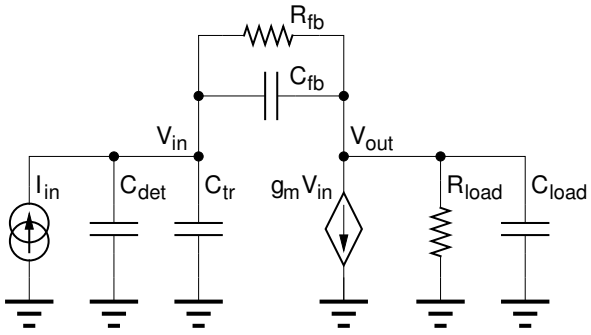


Figure 5.4: Small signal model of the preamplifier. The parameters to be inserted are given in table 5.3.

g_m	9.4 mA/V	R_load	4.8 MΩ
C_det	10 pF	GBW_rad	6.77 rad/ns
C_tr	10.75 pF [1]	GBW	1.08 GHz
C_fb	400.6 fF	τ_1	260 ns [2]
R_fb	649 kΩ [2]	τ_2	7.8 ns
C_load	988 fF	ν_1	611 kHz [2]
C_in	21.15 pF	ν_2	20.4 MHz
C_out	1.39 pF	t_rise	17.2 ns

Table 5.3: Small signal parameters of the *Beetle* preamplifier. The parameters are taken from simulations, parasitic capacitance extractions from the final layout and from the design manual [PDM01].

5.4.1 Preamplifier

The preamplifier integrates the current delivered by the input source – the silicon strip detector or the Multianode Photomultiplier Tube. Its low input impedance reduces the impact of the source capacitance. The actual design of the preamplifier influences the overall performance of the *Beetle* chip to a large extent since the noise is completely dominated by its input device and its signal shaping. A large part of the overall chip power has to be spent in the preamplifier (*Ipre*) to achieve a low-noise operation. Apart from the low-noise requirement, the preamplifier time constant τ_2 of the rising edge has to be smaller than the time constant of the subsequent shaper stage. Otherwise the following pulse shaper will lose a significant amount of gain. Therefore an amplifier with a high gain-bandwidth (GBW) is required to achieve the fast rise time at the output. Furthermore the integrator has to be discharged to avoid a charging by subsequent input events.

5.4.2 Preamplifier Small Signal Modell

To study the transient characteristics of the charge-sensitive preamplifier stage of fig. 5.3 (a), a small signal model is used. It is shown in fig. 5.4 and drops the cascode configuration of the schematic for simplicity. The parameters of the small signal model are given in table 5.3. C_det

[1] $C_\mathrm{tr} = C_\mathrm{gate}\,(8.74\,\mathrm{pF}) + C_\mathrm{gs}\,(1.35\,\mathrm{pF}) + C_\mathrm{para}\,(223\,\mathrm{fF}) + C_\mathrm{tp}\,(100\,\mathrm{fF}) + C_\mathrm{input}\,(330\,\mathrm{fF})$

[2] For preamplifier feedback setting $Vfp = 0\,\mathrm{V}$. Alternative settings are listed in table 5.4.

Vfp	R_{fb}	τ_1	ν_1
0 mV	649 kΩ	260 ns	611 kHz
50 mV	1.47 MΩ	590 ns	270 kHz
100 mV	3.56 MΩ	1.43 µs	112 kHz

Table 5.4: Preamplifier feedback resistor R_{fb}, the resulting time constant τ_1 and the critical frequency ν_1 for different *Vfp* settings.

represents the load capacitance of the detector, C_{fb} the feedback capacitor of the preamplifier and R_{fb} the feedback resistor. R_{fb} is equal to the on-resistance of transistor `M5`, which operates in the triode (linear) region and is controlled by voltage *Vfp*. As an addendum to table 5.3 the on-resistance values for different *Vfp* settings are shown in table 5.4. C_{tr} is the sum of the gate-source capacitance C_{gs} of the input transistor `M1`, the gate-oxide capacitance C_{gate}, the interconnecting capacitances C_{para} of the preamplifier layout, the injection capacitance of the test pulse circuitry C_{tp} and the interconnecting capacitances C_{input} between the input pad and the front-end. The variable g_{m} denotes the input transistor transconductance, R_{load} and C_{load} ($R_{\mathrm{load}} \parallel C_{\mathrm{load}}$) the output impedance of the preamplifier.

For a large feedback resistance ($g_{\mathrm{m}} R_{\mathrm{fb}} \gg 1$) and a high output impedance ($g_{\mathrm{m}} R_{\mathrm{load}} \gg 1$), the transfer function $V_{\mathrm{out}}/I_{\mathrm{in}}$ is given by [Cha91]

$$\frac{V_{\mathrm{out}}(\omega)}{I_{\mathrm{in}}(\omega)} = \frac{g_{\mathrm{m}}}{\frac{g_{\mathrm{m}}}{R_{\mathrm{fb}}} + \omega g_{\mathrm{m}} C_{\mathrm{fb}} + \omega^2 C_{\mathrm{in}} C_{\mathrm{out}}} \tag{5.1}$$

where

$$C_{\mathrm{in}} = C_{\mathrm{det}} + C_{\mathrm{tr}} + C_{\mathrm{fb}} \tag{5.2}$$

$$C_{\mathrm{out}} = C_{\mathrm{load}} + C_{\mathrm{fb}} \tag{5.3}$$

This is a second order transfer function in ω, using the same notation as in fig. 5.4.

The frequency transfer function $V_{\mathrm{out}}/I_{\mathrm{in}}$ is obtained from eq. 5.1 by replacing $\omega = 2\pi\nu$ and by taking the absolute values. For the present *Beetle* preamplifier the Bode-plot of the transfer function is shown in fig. 5.5. The two poles, which are widely spread in the frequency domain, are marked in the plot. These poles are found at

$$\nu_1 = \frac{1}{2\pi\tau_1} = \frac{1}{2\pi R_{\mathrm{fb}} C_{\mathrm{fb}}} \tag{5.4}$$

$$\nu_2 = \frac{1}{2\pi\tau_2} = \frac{g_{\mathrm{m}} C_{\mathrm{fb}}}{2\pi C_{\mathrm{in}} C_{\mathrm{out}}} = GBW_{\mathrm{rad}} \frac{C_{\mathrm{fb}}}{2\pi C_{\mathrm{in}}} = GBW \frac{C_{\mathrm{fb}}}{C_{\mathrm{in}}} \tag{5.5}$$

The first pole at ν_1 is given by the large feedback time constant $R_{\mathrm{fb}} C_{\mathrm{fb}}$ and determines the continuous reset of the integrator whereas the second pole ν_2 is the result of the capacitive feedback. The position of ν_2 is very important for the stability of the front-end.

In the range between at ν_1 and ν_2 of fig. 5.5 the preamplifier integrates currents according to

$$V_{\mathrm{out}} = \frac{1}{\omega} \frac{I_{\mathrm{in}}}{C_{\mathrm{fb}}} = \frac{Q_{\mathrm{in}}}{C_{\mathrm{fb}}} \tag{5.6}$$

where Q_{in} denotes the integral of the input current [Fal98].

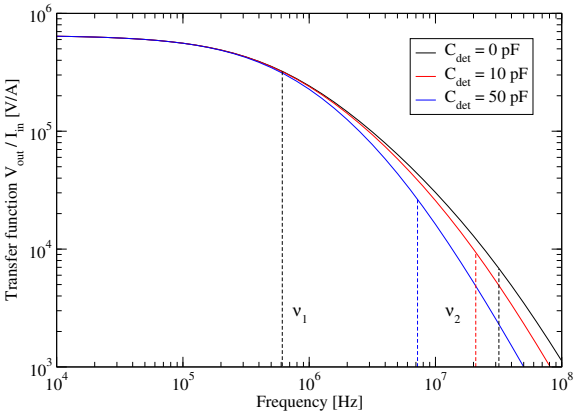


Figure 5.5: Bode-plot of the frequency transfer function $V_{\text{out}}/I_{\text{in}}$ of the charge-sensitive preamplifier for different input detector load capacitances C_{det}. Between ν_1 and ν_2 the preamplifier integrates currents.

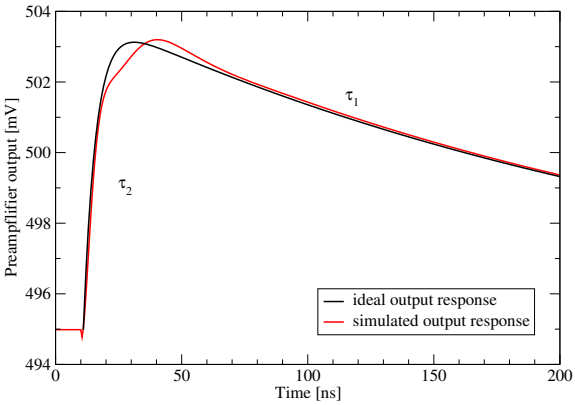


Figure 5.6: Simulated output of the preamplifier. The black curve is the output response to a δ-like current pulse of a 3.6 fC charge ($= 22\,345\,\text{e}^-$). The red curve represents the output response of the final *Beetle* preamplifier with all parasitic capacitances included.

The response of the preamplifier output in the time domain $V_{\text{out}}(t)$ can be obtained from the inverse Laplace transformation of the transfer function of eq. 5.1 in the frequency domain. The input current is approximated by a delta-pulse with an integrated area of Q. In the time domain this results to

$$V_{\text{out}}(t) \approx \frac{Q\tau_1}{C_{\text{fb}}(\tau_1 - \tau_2)} \left(e^{-\frac{t}{\tau_1}} - e^{-\frac{t}{\tau_2}}\right) \quad . \tag{5.7}$$

Since for all practical cases $\tau_2 \ll \tau_1$, $V_{\text{out}}(t)$ represents an exponentially rising step with a slowly decaying tail, introduced by the DC path via the feedback resistor R_{fb}. Figure 5.6 shows the simulated preamplifier output response for a charge of 3.6 fC, including all parasitic capacitances to the simulation circuitry. Atop of this, the expected preamplifier output response of eq. 5.7 is plotted. The parameters τ_1, τ_2 and C_{fb} in eq. 5.7 are taken from table 5.3. The small difference between the signal increasing (determined by τ_2) and the exponential decreasing (determined by τ_1) is mainly caused by the coupling capacitance C_{c} to the subsequent shaper stage.

The time constant τ_2 determines the rise time t_{r} of the preamplifier output, which is usually defined between 10% and 90% of the output signal amplitude. The rise time t_{r} can be calculated from eq. 5.7 to

$$t_{\text{r}} = 2.2\,\tau_2 = 2.2\,\frac{C_{\text{in}}}{GBW\,C_{\text{fb}}} \quad . \tag{5.8}$$

For a given gain-bandwidth, the rise time can be minimised by decreasing the input capacitance C_{in} and/or increasing the feedback capacitance C_{fb}.

The maximum GBW is limited by the stability constraint. Since the second pole in eq. 5.5 is equal to the unity loop gain frequency of the feedback loop, all non-dominant poles of the preamplifier have to be higher than the second pole. For the folded cascode configuration of the

Beetle preamplifier this criterion can be easily met. The first non-dominant pole is determined by the cut-off frequency of the cascode transistor [Hu95] and is given by

$$\nu_{\mathrm{nd}} = \frac{g_{\mathrm{mcasc}}}{C_{\mathrm{nd}}} \tag{5.9}$$

where g_{mcasc} is the transconductance of the cascode transistor (cf. fig. 5.3) and C_{nd} is the total capacitance connected to the node between the cascode transistor `M3` and the current source transistor `M2`. Noise considerations lead to a large input transistor (`M1` in fig. 5.3) and therefore to a relative high W/L-ratio for the cascode transistor `M3`.

5.4.3 Preamplifier Noise

Due to the quadratic contribution of noise currents of amplifier transistors, the noise optimisation of a charge-sensitive preamplifier can be limited to the input transistor (`M1` in fig. 5.3). Since the drain noise current i_{dn} of a MOS-transistor is given by [Nyg91]

$${i_{\mathrm{dn}}}^2 = \frac{8}{3} kT \frac{g_{\mathrm{m}}}{1+\eta} = \frac{8}{3} kT \frac{g_{\mathrm{m}}}{1+\frac{g_{\mathrm{mb}}}{g_{\mathrm{m}}}} \tag{5.10}$$

the transconductance g_{m} of the usually very large input transistor dominates. To achieve a minimum Equivalent Noise Charge (ENC), the input transistor parameters have to match the expected detector capacitance. In general these parameters are defined by the geometry of the transistor (width W and channel length L) and the drain current i_{d} through the device. The noise sources that are relevant for the preamplifier are

- the series contribution from the channel thermal noise of the input transistor,
- the $1/f$-noise,
- the parallel contribution of the detector leakage current,
- the feedback current of the resistive preamplifier feedback.

The subsequent shaper additionally influences the overall noise performance of the front-end due to its bandpass characteristics. Since the requirements to the shaping stage are given by LHCb system aspects (cf. table 5.2), this section only discusses the improvement of the preamplifier input transistor.

Figure 5.7 shows the preamplifier schematic and all noise sources which are relevant for the preamplifier. The noise contribution of the input transistor can be characterised by an equivalent input noise voltage ${v_{\mathrm{i}}}^2$ and an input noise current ${i_{\mathrm{i}}}^2$ [Hu95, San87]. These are defined as

$${v_{\mathrm{i}}}^2 = \underbrace{\frac{8}{3} kT \frac{1+\eta}{g_{\mathrm{m}}}}_{\substack{\text{channel thermal}\\ \text{noise}}} + \underbrace{\frac{K_{\mathrm{f}}}{2\mu_0 {C_{\mathrm{ox}}}^2 W L f}}_{\substack{1/f\\ \text{noise}}} + \underbrace{\frac{{i_{\mathrm{sn}}}^2}{{g_{\mathrm{m}}}^2}}_{\substack{\text{detector shot}\\ \text{noise}}} + \underbrace{\frac{{i_{\mathrm{p}}}^2}{{g_{\mathrm{m}}}^2}}_{\substack{\text{parallel feedback}\\ \text{noise}}} \tag{5.11}$$

$${i_{\mathrm{i}}}^2 = |j\omega C_{\mathrm{in}}|^2 \, {v_{\mathrm{i}}}^2 \tag{5.12}$$

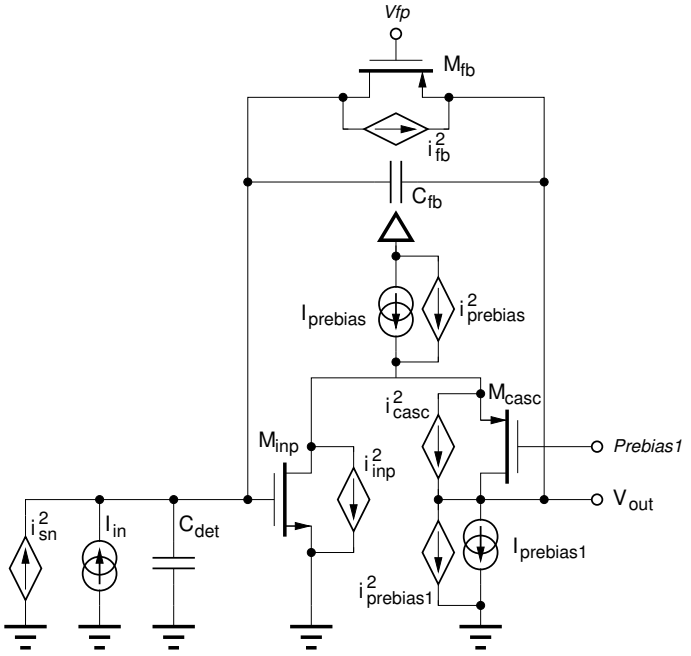


Figure 5.7: Noise sources of the charge-sensitive preamplifier.

with:

g_m	–	transistor transconductance,
η	–	$= \frac{g_\mathrm{mb}}{g_\mathrm{m}}$ ratio of bulk-source transconductance to transistor transconductance,
k	–	Boltzmann's constant $k = 1.3807 \cdot 10^{-23}\ \mathrm{J\,K^{-1}}$,
T	–	absolute temperature,
K_f	–	flicker noise coefficient,
μ_0	–	channel charge carrier mobility,
C_ox	–	specific oxide capacitance per area,
W, L	–	width and length of the transistor.

The correlation between input signal v_i and the equivalent noise voltage v_equi is given by [Cha91]

$$v_\mathrm{equi}{}^2 = \left(\frac{C_\mathrm{in}}{C_\mathrm{fb}}\right)^2 v_\mathrm{i}{}^2 \tag{5.13}$$

where C_in is the total input load capacitance and C_fb the feedback capacitance of the preamplifier. Using eq. 5.2 and combining all chip internal input load capacitances to a common value C_internal[3], eq. 5.13 can be rewritten to

$$v_\mathrm{equi}{}^2 = \left(\frac{C_\mathrm{gate} + C_\mathrm{det} + C_\mathrm{internal}}{C_\mathrm{fb}}\right)^2 v_\mathrm{i}{}^2 \quad . \tag{5.14}$$

A more detailed analysis of the channel thermal noise and the $1/f$-noise of eq. 5.11 with the consideration that $g_\mathrm{m} \propto \sqrt{\frac{W}{L}}$ and $C_\mathrm{gate} \propto WL$, shows that an optimum $W_\mathrm{opt} = W(L)$ must

[3] C_internal is defined from eq. 5.2 as: $C_\mathrm{in} = C_\mathrm{det} + (C_\mathrm{gate} + \underbrace{C_\mathrm{gs} + C_\mathrm{para} + C_\mathrm{tp} + C_\mathrm{input}}_{C_\mathrm{internal}}) + C_\mathrm{fb}$.

exist that minimises v_i. The optimum width W of the input transistor cannot be determined in a closed form [Cha91] for the channel thermal noise and $1/f$-noise together. Therefore at first the optimum width is calculated separately for both noise types.

Inserting $g_\mathrm{m} = \sqrt{2\mu_0 {C_\mathrm{ox}}^2 I_\mathrm{d} \frac{W}{L}}$ and $C_\mathrm{gate} = C_\mathrm{ox} W L$ into eq. 5.14 and taking the derivative for the channel thermal noise part with respect to W, this results in an optimum width

$$W_\mathrm{opt,th} = \frac{C_\mathrm{det} + C_\mathrm{internal}}{2 C_\mathrm{ox} L} \tag{5.15}$$

for the channel thermal noise and in

$$W_\mathrm{opt,1/f} = 3\frac{C_\mathrm{det} + C_\mathrm{internal}}{2 C_\mathrm{ox} L} = 3 W_\mathrm{opt,th} \tag{5.16}$$

for the $1/f$-noise.

For a fixed input transistor length L the optimum width W for a minimum $1/f$-noise is three times larger than for an optimum channel thermal noise. Equation 5.15 shows that the optimum transistor geometry is independent from the frequency. It is therefore independent from the time constant τ of the following shaper stage. Depending on the amount of $1/f$-noise encountered for a given process technology, a value in between the two extremes, given by eq. 5.15 and 5.16, has to be chosen.

Eq. 5.15 can also be expressed in terms of the gate capacitance C_gate of the input transistor. This then results to

$$C_\mathrm{gate,th} = \frac{C_\mathrm{det} + C_\mathrm{internal}}{2} \quad . \tag{5.17}$$

By assuming that the internal capacitances C_internal are much smaller than the external detector load capacitance C_det, the maximum of the channel thermal noise is then given by

$$C_\mathrm{gate,th} \approx \frac{1}{2} C_\mathrm{det} \tag{5.18}$$

whereas the gate capacitance of the $1/f$-noise maximum is given by

$$C_\mathrm{gate,1f} \approx \frac{3}{2} C_\mathrm{det} \quad . \tag{5.19}$$

The minimum noise contribution of the input transistor is therefore given by the following relation between C_det and C_gate:

$$\frac{1}{2} C_\mathrm{det} < C_\mathrm{gate} < \frac{3}{2} C_\mathrm{det} \quad . \tag{5.20}$$

For detector capacitances C_det between 5.8 pF and 17.5 pF this equation is fulfilled by the input transistor of the *Beetle* chip.

The shaper time constant τ appears in the parallel and series noise terms. The parallel noise is proportional to the shaper time τ, the series thermal noise is inversely proportional to τ and the $1/f$-noise is independent of it. Thus, a τ exists for which v_i is minimised. The differentiation of eq. 5.13 with respect to τ yields [Fal98]

$$\tau_c = C_\mathrm{in} \sqrt{\frac{8kT/3g_\mathrm{m}}{2qI_0 + 4kT/R_\mathrm{fb}}} \quad . \tag{5.21}$$

At the noise-corner time constant τ_c the contribution of the equivalent thermal noise ($v_\mathrm{i,th}$) equals the equivalent feedback plus detector shot noise ($v_\mathrm{i,Rfb} + v_\mathrm{i,sn}$).

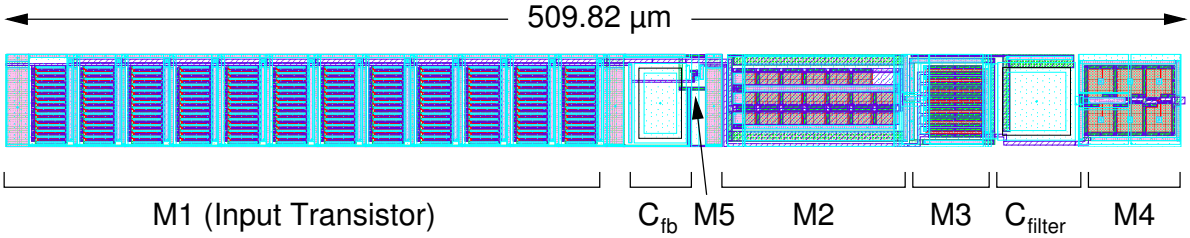


Figure 5.8: Layout of the *Beetle* front-end preamplifier. The length of the layout is 509.82 µm and the width for each channel is 40.24 µm, which is defined by the overall pitch of the input pads. Approximately 50% of the area is used by the input transistor `M1`. The width W of `M1` is 3.744 mm, which is achieved in the layout by connecting an array of $12 \times 13 = 156$ devices of $W/L = 24/0.42$ in parallel. The on-resistance of `M5`, which operates in the triode (linear) region, is the feedback resistor R_{fb} of the preamplifier.

5.4.4 Preamplifier Schematic and Layout

Figure 5.3 (a) shows the detailed schematic of the *Beetle* preamplifier with the corresponding design parameters. The current source transistor `M2` provides the large current for the preamplifier (nominal 600 µA) and is adjustable via the register *Ipre*. The current ratio between input branch and cascode branch is 9 : 1. Since g_{m} of the input transistor `M1` is proportional to $\sqrt{W/L}$, a short transistor length L is desirable. However, to avoid short channel effects[4], the length of the NMOS input transistor has been chosen to 420 nm, which is substantially bigger than the minimum possible feature size of the chosen technology ($L_{\mathrm{eff}} = 240$ nm). The width W of the input transistor is 3 744 µm. This width can be realised in the layout by using 156 NMOS devices in parallel, each with a W/L-ratio of 24/0.42. Figure 5.8 shows the overall layout of the *Beetle* preamplifier. The input transistor `M1` consumes approximately 50% of the total area of the preamplifier. A very low-ohmic ground connection of the input FET is important to prevent sensitivity to common mode variations. Therefore the input transistor is completely covered with two metal layers (layer M2 and MZ, cf. fig. 4.10) serving as the ground plane with an channel-to-channel resistance of only 4.5 mΩ/channel. Substrate contacts are added around each group of 13 input FETs. The resulting low-ohmic bulk connection reduces noise contributions from high bulk resistances.

A precise and linear feedback capacitor is required for a proper operation of the preamplifier. Therefore, the feedback capacitor `C_fb` is realised as a linear Metal-Insulator-Metal Capacitor (MIMCAP) with a length of $L = 18.4$ µm and a width of $W = 30.4$ µm. The equation describing the MIMCAP capacitance is as follows [PDM01]:

$$C_{\mathrm{mim}} = \underbrace{[C_{\mathrm{a}} \cdot (L \cdot W) + 2C_{\mathrm{p}} \cdot (L + W)]}_{\text{Geometric factor}} \cdot \underbrace{[1 + C_{\mathrm{VQ}}(V - V_0)^2]}_{\text{Voltage factor}} \cdot \underbrace{[1 + TC \cdot (T - 25)]}_{\text{Temperature factor}} \quad (5.22)$$

[4] Different effects are summarised under this item, for example: *drain induced barrier lowering*, *channel length modulation*, *punch through*, *threshold voltage roll-off*, *mobility reduction*.

where:

T	–	temperature [in ℃],
V	–	potential difference between two nodes [in V],
L, W	–	design width and length of the MIMCAP [in µm],
$C_\mathrm{a} = (0.69 \pm 0.05)\,\mathrm{fF}/\,\mu\mathrm{m}^2$	–	capacitance of the MIMCAP dielectric,
$C_\mathrm{p} = (0.15 \pm 0.25)\,\mathrm{fF}/\,\mu\mathrm{m}$	–	perimeter capacitance of the MIMCAP,
$C_\mathrm{VQ} = C_{\mathrm{VQ}_0} + C_\mathrm{VQT} \cdot (T - 25)$	–	quadratic voltage coefficient of capacitance[5],
$C_{\mathrm{VQ}_0} = -7.63 \cdot 10^{-6}\,\mathrm{V}^{-2}$	–	value of C_VQ at $T = 25$℃,
$C_\mathrm{VQT} = 2.76 \cdot 10^{-8}\,\mathrm{V}^{-2}{}^\circ\mathrm{C}^{-1}$	–	derivative of C_VQ with respect to temperature,
$V_0 = V_{00} + V_{0\mathrm{T}} \cdot (T - 25)$	–	value of V at which the capacitance is maximum,
$V_{00} = -0.3\,\mathrm{V}$	–	value of V_0 at $T = 25$℃,
$V_{0\mathrm{T}} = -2.8 \cdot 10^{-3}\,\mathrm{V}/^\circ\mathrm{C}$	–	derivative of V_0 with respect to temperature,
$TC = -4.37 \cdot 10^{-5}/^\circ\mathrm{C}$	–	temperature coefficient of capacitance.

The geometrical factor is the most dominant part for small capacitor sizes. The effects due to voltage or temperature variations can be neglected in a first approximation. Taking only the geometrical term of eq. 5.22 leads to a preamplifier feedback capacitance of $(400.6 \pm 37.1)\,\mathrm{fF}$. Further, the mismatch between different located capacitors has to be calculated. The 3 sigma mismatch tolerance of two capacitors on the same chip and with same dimensions, separated by the distance S is given by [PDM01]

$$\frac{\Delta C}{C} = 0.03\sqrt{\frac{1.805}{WL} + 10^{-8}S^2} \tag{5.23}$$

where W, L, and S are in µm.

With eq. 5.23 the channel-to-channel mismatch of the capacitance calculates to 0.2% and the mismatch between first and last channel is 1.6%. Therefore the contribution due to mismatches of the capacitance feedback is negligible for the preamplifier.

5.4.5 Pulse Shaper

A pulse shaping stage subsequently follows to the preamplifier. It transforms the voltage step of the preamplifier into a fast decaying pulse with a peak height, that is proportional to the charge at the front-end input. The following basic conditions have been considered during the development of the pulse shaper stage:

- the pulse peaking time has to be approximately 12.5 ns to comply with the 25 ns bunch crossing period of LHCb,
- preferably no undershoot of the output pulse shape to prevent a negative pile-up in case of consecutive pulses and therefore minimise the inefficiency,
- a small shaper gain so that the preamplifier gain can be maximised and therefore the shaper noise does not add significantly to the total noise,
- the feedback resistance R_fb and the g_m of the input transistor should be large because of the parallel and series noise contribution,

[5] The tolerance on C_p contains variation due to both fringe capacitance and dimensional variation.

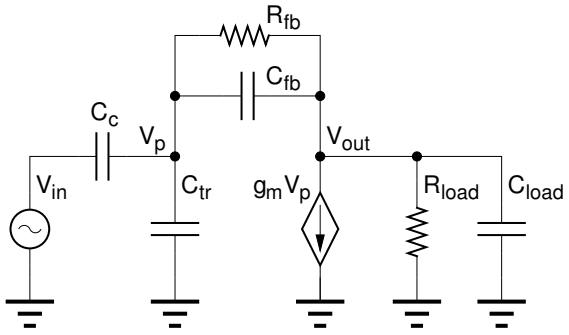


Figure 5.9: Small signal model of the shaper. The parameters to be inserted are given in table 5.5.

- the design of the feedback transistors `M10` and `M11` (cf. fig. 5.3 (b)) limits the linearity of the pulse shaper because these resistors change their values for large output swings,
- the core cell transistors should cover the complete required dynamic range,
- the shaper stage has to operate with a low-power consumption,
- the size of the pulse shape layout has to fit into the front-end channel pitch of 40.24 µm.

Weighting all these requirements leads to the decision to use an active CR-RC bandpass filter and a single sampling method for the shaping stage. In a standard CMOS technology the use of a CR-RC filter is quite simple and the achievable S/N ratio is reasonable for the limited power consumption. Higher orders of shaping filters increase the complexity of the circuit as well as the power consumption and are therefore not practicable in the front-end of the *Beetle*. The double correlated sampling method, which would improve the noise performance of the front-end, could also not be applied. This method would introduce a dead time and the need of more than one sampling clock.

The pulse shaper stage of the *Beetle* is therefore only a first order stage, which means that one differentiator is followed by one integrator. The frequency spectrum is confined by filtering low frequencies by differentiation (CR) and high frequencies by integration (RC). The time constants of the differentiator and the integrator should be identical in order to optimize the band pass characteristics. Hence, the output signal of the shaper stage is a so-called *semi-Gaussian* pulse shape.

For a given shaper configuration the Equivalent Noise Charge (ENC) varies with the shaping time: the channel thermal noise is inversely proportional to the shaping time whereas the noise due to the detector leakage current rises proportional to the shaping time. In contrast the $1/f$-noise is independent from the shaping time constant. With respect to the total noise of the front-end, an optimum shaping time exists. In case of the *Beetle*, this optimisation cannot be realised due to the requirement of the output pulse peaking time of 25 ns and the signal remainder of maximum 30% in the next bunch crossing cycle (cf. table 5.2).

g_m	1.08 mA/V	C_in	1.18 pF
C_c	700 fF	C_out	404.6 fF
C_tr	378 fF	t_peak	12.7 ns
C_fb	48.8 fF	ν_max	12.53 MHz
R_fb	181 kΩ	$t_\mathrm{peak,sG}$	10.1 ns
C_load	307 fF	$\nu_\mathrm{max,sG}$	15.85 MHz
R_load	7.2 MΩ	GBW_rad	915.2 rad/µs
$g_\mathrm{m}R_\mathrm{fb}$	195.5	GBW	146 MHz

Table 5.5: Small signal parameters of the *Beetle* shaper. The parameters are taken from simulations, parasitic capacitance extractions from the final layout and from the design manual [PDM01].

5.4.6 Pulse Shaper Small Signal Model

The small signal model of the pulse shaper can be inferred from the schematic in fig. 5.3 (b) similar to the preamplifier case and is shown in fig. 5.9. The gain calculation from the small signal model uses the approximation $g_\mathrm{m} \ll (\frac{1}{R_\mathrm{fb}} + \omega C_\mathrm{fb})$ and results in eq. 5.24 [Fal98]:

$$\begin{aligned} \frac{V_\mathrm{out}(\omega)}{V_\mathrm{in}(\omega)} &= -\frac{\omega g_\mathrm{m} C_\mathrm{c}}{\frac{1}{R_\mathrm{fb}}(\frac{1}{R_\mathrm{fb}\|R_\mathrm{load}} - g_\mathrm{m}) + \omega(\frac{2C_\mathrm{fb}-C_\mathrm{in}-C_\mathrm{out}}{R_\mathrm{fb}} - g_\mathrm{m}C_\mathrm{fb} - \frac{C_\mathrm{in}}{R_\mathrm{load}}) + \omega^2({C_\mathrm{fb}}^2 - C_\mathrm{in}C_\mathrm{out})} \\ &= A(\omega) \end{aligned} \tag{5.24}$$

where

- g_m – transconductance of the shaper input transistor `M6` of fig. 5.3 (b),
- C_in – total input capacitance with $C_\mathrm{in} = C_\mathrm{c} + C_\mathrm{tr} + C_\mathrm{fb}$,
- C_out – total output capacitance with $C_\mathrm{out} = C_\mathrm{load} + C_\mathrm{fb}$,
- C_c – coupling capacitance between preamplifier and shaper,
- C_tr – gate oxide capacitance and input routing parasitics,
- C_fb – feedback capacitance of shaper,
- C_load – output load capacitance,
- R_fb – feedback resistor, formed by `M10` and `M11`,
- R_load – load resistance of `M9`.

The parameters for the shaper are given in table 5.5. The quoted shaper peaking time t_peak is extracted from a simulation of the present shaper version, including all parasitic components and the preamplifier stage (limited bandwidth). The simulation of the shaper stage using an ideal input signal (infinite bandwidth) results in a slightly smaller shaper peaking time $t_\mathrm{peak,sG}$. The dominant pole of the shaper stage is associated with the input node V_p in fig. 5.9 so that the gain-bandwidth product is defined by

$$\mathrm{GBW} = \frac{v_0}{R_\mathrm{fb}C_\mathrm{in}} = \frac{g_\mathrm{m}}{C_\mathrm{in}} \tag{5.25}$$

with $v_0 = g_\mathrm{m}R_\mathrm{fb}$.

Equation 5.24 can be expressed as

$$\frac{v_\mathrm{out}(\omega)}{v_\mathrm{in}(\omega)} = -\frac{\omega}{(\omega+\beta)^2 + \alpha^2} \quad . \tag{5.26}$$

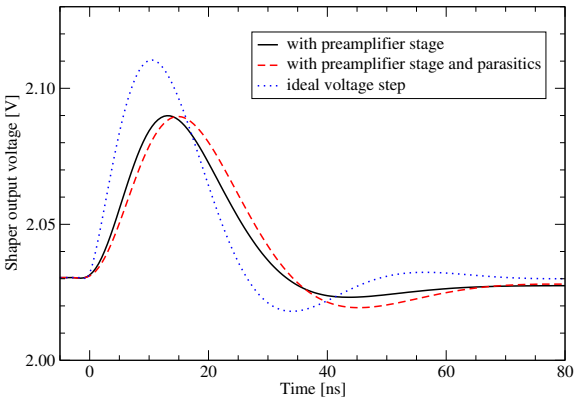


Figure 5.10: Simulation of the output voltage of the *Beetle* pulse shaper. The solid line shows the pulse response of the combined preamplifier and shaper stage for a 22 ke$^-$ input signal. In addition, the dashed simulation includes all parasitic capacitances. The dotted line shows the output response of an ideal voltage step.

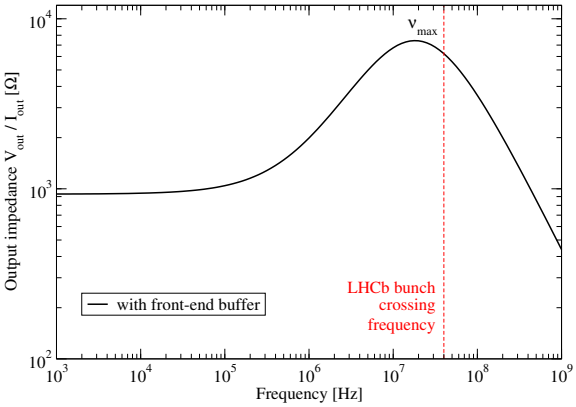


Figure 5.11: Bode plot of the pulse shaper output impedance $V_{\text{out}}/I_{\text{out}}$ including the subsequent output buffer stage.

This denotes an one-zero two-pole transfer function. Taking $v_{\text{in}}(\omega) = -1/\omega$, the inverse Laplace transformation of eq. 5.26 is the transformation of a step function. This can be used in a first-order approximation to model the preamplifier output pulse shape. In the time domain this is equal to

$$v_{\text{out}}(t) = \frac{1}{\alpha} \sin(\alpha t)\, e^{-\beta t} \quad . \tag{5.27}$$

Due to the negative sine half-wave an undershoot is expected for v_{out}. A transfer function of the type

$$v_{\text{out}}(\omega) = \frac{\omega}{(\omega+\beta)^2} \cdot \frac{1}{\omega} \tag{5.28}$$

on the other hand gives an ideal pulse response in the time domain of

$$v_{\text{out}}(t) = t\, e^{-\beta t} \tag{5.29}$$

which is a semi-Gaussian pulse. The peak of the pulse is given at time $\tau = 1/\beta$, which is equal to the time constant of the low-pass respectively the high-pass filter. Comparing the transfer function of the ideal pulse (eq. 5.28) with eq. 5.24, it can be deduced that in the ideal case the denominator polynomial has a double real pole [Fal98]. By the right choice of R_{load} in the denominator, the shaper output will form an ideal semi-Gaussian pulse. The pulse maximum is then reached at

$$t_{\text{peak,sG}} = \frac{1}{\omega_{\max}} = \frac{1}{2\pi\nu_{\max}} \quad . \tag{5.30}$$

Figure 5.10 shows the simulated response of the preamplifier output for a 22 ke$^-$ front-end input signal. The parasitic capacitances from the final layout are also included in this simulation.

The result is plotted with a dashed line in fig. 5.10. The shaper model with the parasitics has a slower peaking time and a more pronounced undershot. The shaper response to an ideal voltage step input signal is shown in the diagram as dotted line. It is obviously much faster but has a much larger undershot. The comparison of results from simulation and measurements (see section 6.2) shows a good agreement between simulation model and laboratory measurements.

The output signal of the shaper is supposed to be written to the pipeline capacitor. Therefore the output impedance has to be derived from the small signal model with the same assumptions made for eq. 5.24. It is given by

$$\frac{V_{\mathrm{out}}(\omega)}{I_{\mathrm{out}}(\omega)} = -\frac{\frac{1}{R_{\mathrm{fb}}} + \omega C_{\mathrm{in}}}{\frac{1}{R_{\mathrm{fb}}}\left(\frac{1}{R_{\mathrm{fb}} \| R_{\mathrm{load}}} - g_{\mathrm{m}}\right) + \omega\left(\frac{2C_{\mathrm{fb}} - C_{\mathrm{in}} - C_{\mathrm{out}}}{R_{\mathrm{fb}}} - g_{\mathrm{m}} C_{\mathrm{fb}} - \frac{C_{\mathrm{in}}}{R_{\mathrm{load}}}\right) + \omega^2 \left({C_{\mathrm{fb}}}^2 - C_{\mathrm{in}} C_{\mathrm{out}}\right)} \quad . \tag{5.31}$$

The result of eq. 5.31 in the frequency domain is plotted in fig. 5.11. The simulation shows the Bode plot of the impedance for the shaper output with a subsequent buffer stage as the output load. For low frequencies the shaper output impedance remains around 1 kΩ which is uncritical. At the zero's break frequency ($1/R_{\mathrm{fb}}C_{\mathrm{in}}$) the output impedance rises proportional to the frequency, which shows an inductive behaviour. At LHCb the interesting signal band is at $\frac{40}{2}$ MHz. Here, the output impedance is approximately 7.4 kΩ which will not lead to a bandwidth limitation. Unfortunately, the shaper output impedance does not allow to drive the pipeline capacitance and the line capacitance directly[6]. Also, without a subsequent buffer stage, changes of the pipeline capacitances (due to the operation of the write-switches) would directly influence the pulse shape.

5.4.7 Pulse Shaper Schematic and Layout

The schematic of the pulse shaping stage is shown in fig. 5.3 (b). Here transistor `M7` acts as the adjustable current source. It is controlled by the register *Isha* and provides a nominal current of 80 µA. For the shaper stage, the current ratio between input branch and cascode branch is 5 : 1.

Simulations showed that a feedback capacitance of ≈ 50 fF fulfils the shaper requirements. However, the smallest possible MIMCAP capacitance in this technology is 75 fF[7]. Therefore the feedback capacitor is formed out of two identical MIMCAPs of 97.6 fF each, connected in series. This leads to an overall feedback capacitance of $C_{\mathrm{fb}} = 48.8$ fF with a standard deviation obtained from eq. 5.22 and eq. 5.23 of $\Delta C_{\mathrm{fb}} = \pm 4.7$ fF. Figure 5.12 shows the layout of the pulse shaping stage. The two feedback capacitors and the feedback resistor (transistor `M10` and `M11`) are located in between the input branch (formed by the input transistor `M6`) and the cascode branch (load transistor `M9` and cascode transistor `M8`). The NMOS current source `M7` is placed right to the cascode branch. The layout of the shaper stage includes two gaps (between coupling capacitor C_{c} and the input transistor `M6` and at the right hand side of the current source `M7`), used for power routing traces. This reduces the channel-to-channel resistances of the power lines.

[6] ≈ 2.5 pF can be assumed for the capacitance of the pipeline write-line.

[7] The minimum MIMCAP dimension is $10 \times 10\,\mu\mathrm{m}^2$.

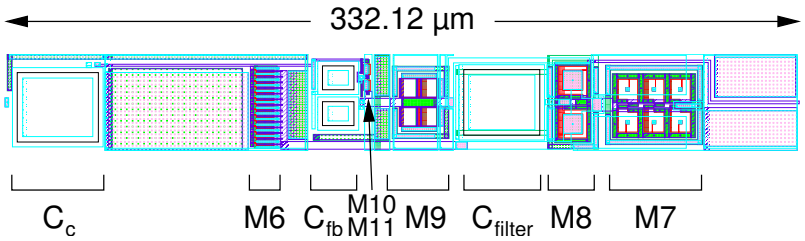


Figure 5.12: Layout of the coupling capacitor C_c and the front-end shaper. `M10` and `M11` build the feedback resistor R_{fb} of the shaper. The channel width of the shaper is 40.24 µm.

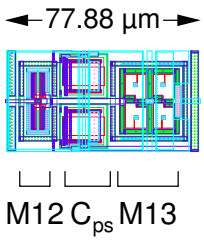


Figure 5.13: Layout of the front-end output buffer.

5.4.8 Buffer

The output buffer of the analogue front-end is designed as a standard NMOS source follower [Cha91]. The schematic is given in fig. 5.3 (c) and the layout is shown in fig. 5.13. It has to drive the pipeline capacitance, the input capacitance of the comparator and the parasitic capacitance, which is the capacitive sum of the comparator routing lines, the pitch adapter and the pipeline write-line. The total load capacitance C_{load} is extracted from the layout and is given between 2.47 and 2.51 pF, depending on the different routing lengths and cross-coupling capacitances from the front-end to the pipeline pitch adapter.

Between transistor `M12` and `M13`, two 0.65 pF power supply filter capacitances `C_ps` are implemented into the buffer stage to suppress interferences from the buffer to the power supply lines (and therefore to neighbouring channels). A detailed description of the coupling capacitor is given in section 5.13.

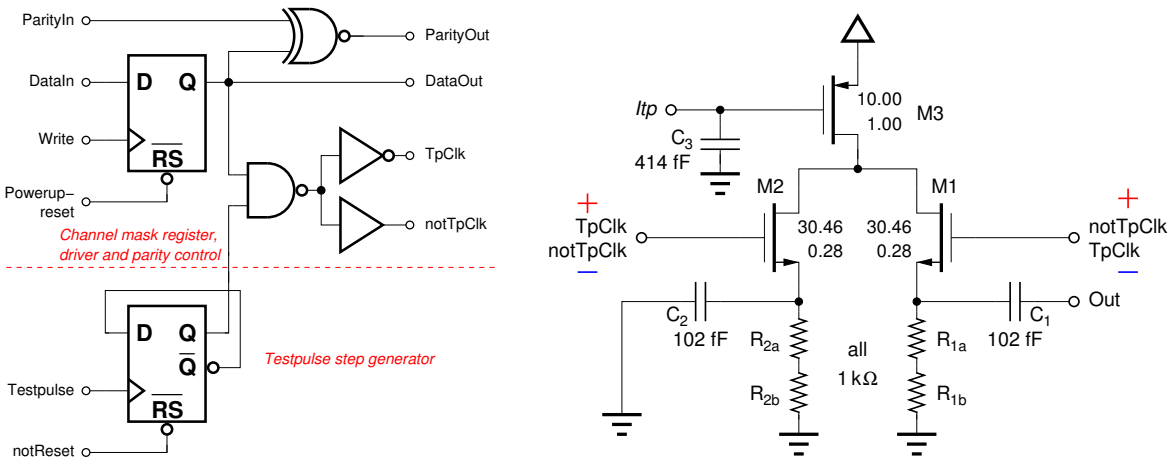
5.5 Test pulse

To detect dead channels, either in the complete detector system or during the wafer testing of the chips, it is mandatory to apply a defined test stimulus to individual or all front-end amplifiers. Therefore an on-chip test pulse circuitry has been implemented for each input channel. The test pulse circuitry is shown in fig. 5.14. It consists of a digital core (a) with the channel mask register, the clock driver and the parity control and the analogue core (b) for the charge injection. The corresponding layout is depicted in fig. 5.15.

Unfortunately, injecting the same charge to all preamplifier channels at the same time is not feasible. The load on the power supply lines by 129 simultaneously pulsed channels[8] will cause a huge common mode signal. To overcome this, an easy to recognise readout pattern, resulting from symmetrical charge injection of both polarities has been chosen for the test pulse signal. An alternating pattern of +1 and −1 times a common input signal amplitude is applied to all 129 channels.

From one test pulse injection to the next, the polarity of the charge injection is changed, so that signals with both polarities are injected to each front-end channel (test pulse step generator in fig. 5.14(a)). A positive step uses the signal distribution (`TpClk`, `notTpClk`) indicated by '+' in fig. 5.14(b), a negative step uses the inverted combination (`notTpClk`, `TpClk`) labelled with '−'.

[8] 129 test pulse circuits for 128 detector channels and one test channel.



(a) Digital core (b) Analogue core

Figure 5.14: Schematic of the internal *Beetle* test pulse circuitry. It consists of two parts: the digital core (a) with the mask register, the driver and the parity control and the analogue core (b) for the charge injection. Two different versions of this analogue core exist: a positive step uses the signal distribution (`TpClk`, `notTpClk`) indicated by '+', a negative step uses the inverted combination (`notTpClk`, `TpClk`), labelled with '−'. The amplitude of the injected charge is controlled by the current *Itp*.

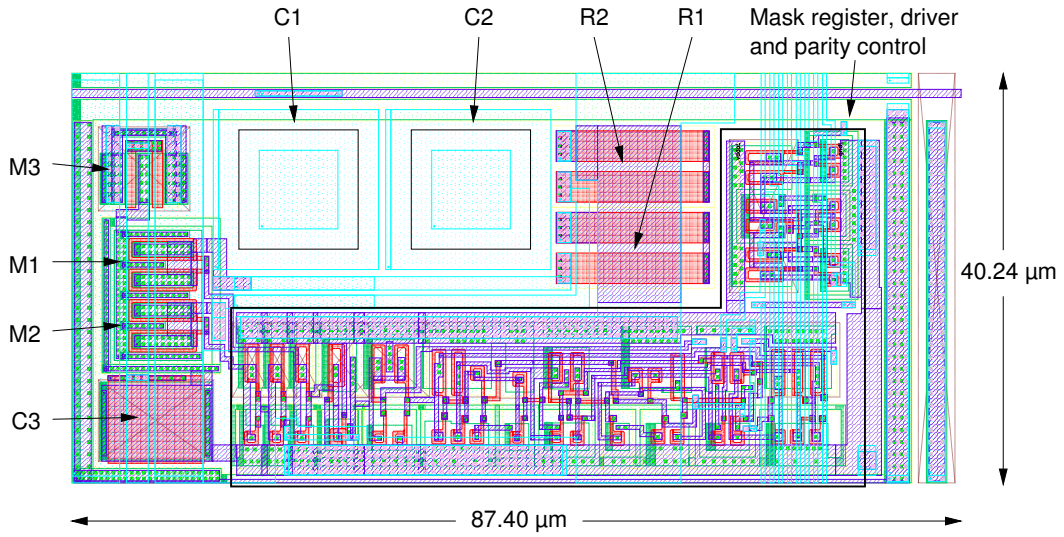


Figure 5.15: Layout of the test pulse circuitry, with a dimension of 87.40 µm × 40.24 µm for each channel. The framed area marks the digital core of fig. 5.14(a). For the analogue part the components from the schematic in fig. 5.14(b) are marked in the layout.

Additionally, single channels can be selected to inject a test pulse into the front-end. This is controlled by the channel mask register *TpSelect* which is implemented as a 129 bit shift register (cf. table C.16). The channel test pulse select information is stored locally in the digital core as indicated in fig. 5.14(a). As a control mechanism, the parity information of all 129 bits is generated and flagged in the analogue readout header (cf. fig. C.8).

The signal amplitude of the injected pulse is adjustable via the register *Itp*. The programmed current value of *Itp* is reduced by a factor of 10 and mirrored to the current source transistor `M3` in fig. 5.14(b). The constant current of `M3` is switched with respect to the *Testpulse* signal between the charge injection branch, formed by transistor `M1`, load resistor `R1a` + `R1b` and the coupling capacitor `C1`, and the dummy branch, formed by `M2`, `R2a` + `R2b` and `C2`. The output `Out` of `C1` is directly connected to the preamplifier input, whereas `C2` is connected to ground. The dummy branch is necessary to keep the voltage between current source `M3` and transistor `M1` at a defined potential.

The charge that is injected into the preamplifier is given by

$$Q_{\text{out}} = C_1(R_{1a} + R_{1b})\frac{Itp}{10} \quad . \tag{5.32}$$

The load resistor R_{1a} and R_{1b} are formed by polysilicon resistors. For the used technology, the resistance is defined as:

$$R_{\text{poly}} = 2\frac{R_{\text{end}}}{W + \Delta W} \cdot T_{\text{c1}} + R_{\text{s}}\frac{L + \Delta L}{W + \Delta W} \cdot T_{\text{c2}} \tag{5.33}$$

with

$$T_{\text{c1}} = 1 + TCR_{\text{end}}(T - 25) \qquad \text{Temperature effect of the end resistance}$$
$$T_{\text{c2}} = 1 + TCR(T - 25) \qquad \text{Temperature effect of the resistance}$$

where:

T	–	temperature [in °C],
L, W	–	width and length of the polysilicon resistor [in µm],
$R_{\text{s}} = (210 \pm 42)\,\Omega$	–	sheet resistance of the polysilicon resistor,
$R_{\text{end}} = (110 \pm 70)\,\Omega\,\mu\text{m}$	–	end resistance of the polysilicon resistor,
$\Delta L = \pm 0.15\,\mu\text{m}$	–	length tolerance,
$\Delta W = \pm 0.05\,\mu\text{m}$	–	width tolerance,
$TCR = 2.0 \cdot 10^{-4}/°\text{C}$	–	temperature coefficient of the resistance,
$TCR_{\text{end}} = -1.1 \cdot 10^{-3}/°\text{C}$	–	temperature coefficient of the end resistance,

The large variation of the sheet resistance R_{s} and end resistance R_{end} are the most dominant source of mismatches for polysilicon resistors. The effects due to temperature variations (eq. 5.34 and eq. 5.34) can be neglected in a first approximation. Further, the mismatch between different resistor locations on the same chip has to be calculated. The 3 sigma mismatch tolerance of resistors with the same dimensions, separated by the distance S, is given by

$$\frac{\Delta R}{R} = 0.01\sqrt{\frac{144}{WL} + 5.29 \cdot 10^{-4}S} \tag{5.34}$$

where W, L, and S are in µm.

The injected charge Q_{out} calculated from eq. 5.32, eq. 5.22 ($L = W = 11.72\,\mu\text{m}$) and eq. 5.33 ($L = 13.24\,\mu\text{m}$, $W = 3\,\mu\text{m}$) to

$$Q_{\text{out}} = 2.04 \cdot 10^{-2}\frac{\text{fC}}{\mu\text{A}} \cdot Itp$$

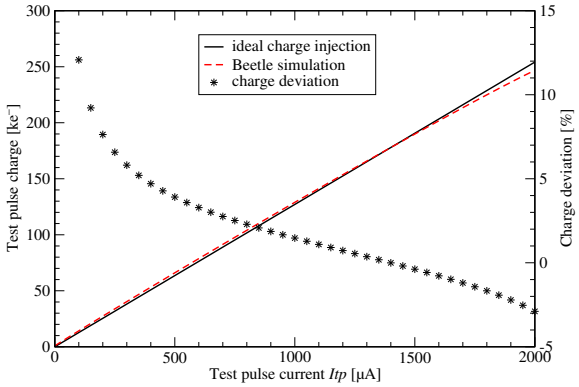


Figure 5.16: Injected test pulse charge as a function of *Itp*. The solid line represents the ideal charge injection from eq. 5.35, the dashed line shows the results from a simulation of the test pulse and preamplifier circuitry. The deviation between the ideal and simulated charge injection is also plotted in the diagram.

$$= \quad 127 \, \frac{\mathrm{e}^-}{\mu\mathrm{A}} \cdot \mathit{Itp} \tag{5.35}$$

with a channel-to-channel variation of the test pulse charge injection circuitry on the same chip of $\frac{\Delta Q_{\mathrm{out}}}{Q_{\mathrm{out}}} = 1.9\%$[9] and a variation between different chips of $\frac{\Delta Q_{\mathrm{out}}}{Q_{\mathrm{out}}} = 19.1\%$. Thus it is not advised to use the test pulse for calibration purposes between different chips. But the test pulse circuitry may be used for channel-to-channel comparisons within single chips.

The ideal test pulse charge injection of eq. 5.35 is plotted in fig. 5.16 for the complete *Itp* range between 0 mA and 2 mA. The results from a test pulse injection simulation of test pulse and amplifier circuitry is also drawn into the diagram. The ratio between the simulated and the ideal charge shows a large deviation for small *Itp* values due to additional charge injections of the transistor `M1` (cf. section 5.7.1, charge injection).

5.6 Comparator

The Pile-Up System (PUS) of LHCb must derive a fast digital inhibit signal indicating too many hit channels. Therefore a comparator stage is implemented in the *Beetle* to compare the output of the front-end with an adjustable threshold. The requirements on the comparator are driven by the need to detect signals produced by a Minimum Ionising Particle (MIP) with a very high efficiency, which should be limited only by the noise level of the front-end. The response of the comparator should be within 25 ns to keep up with the bunch crossing period of the LHCb experiment. The homogeneity between different comparator channels should be high enough, so that a common threshold can be applied to all channels.

For the present *Beetle* comparator (basically designed by Hans Verkooijen), a low-pass filtering configuration as shown in fig. 5.17 has been chosen. It consists of an integrator, a threshold generator and a discriminator stage [Ver99, Beu03]. Subsequent to the digital output of the discriminator a channel mask register, a synchronisation stage, a pulse generator and a level shifter follows.

[9] The mismatch for devices on the same chip is calculated with equation 5.23 and 5.34.

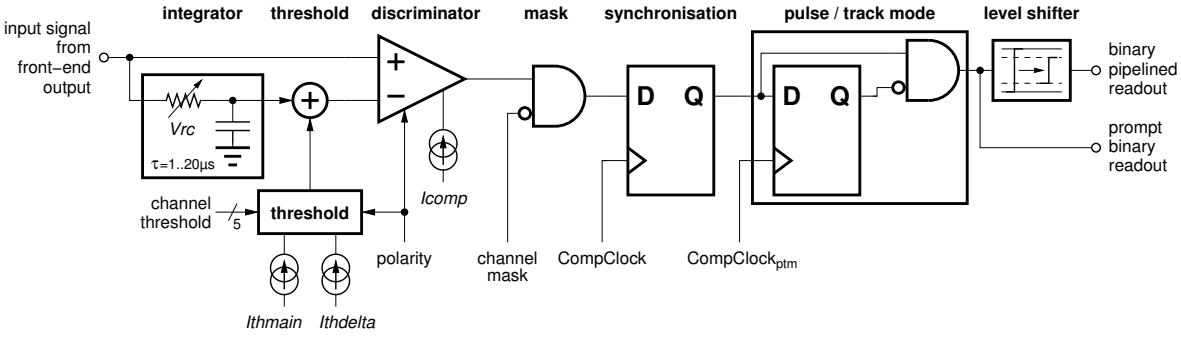


Figure 5.17: Schematic block diagram of the comparator.

The DC-offset of the front-end is compensated by adding it to the threshold voltage via a low-pass filter. The time constant τ is adjustable between 16 µs and 10 ms, controlled by the voltage DAC *Vrc*. For each channel the threshold voltage itself is generated as the voltage drop across the resistance at the low-pass filter of two different threshold currents:

- a *common threshold current*, sunk from the '−' node. It is the 512th part of the adjustable output current of DAC *Ithmain*.
- a *channel threshold current*, forced into the '−' node. It is adjustable per channel with a resolution of 5 bits (register *CompChTh*). The current of the LSB corresponds to the 1024th part of the programmable output current of DAC *Ithdelta*.

The schematic of the discriminator core is shown in fig. 5.18. It consists of two differential amplifiers, operating with bias *Icomp*.

CompPolarity and *notCompPolarity* switch between detection of positive or negative input signals. The choice of the polarity is set via the *Beetle* register bit `CompCtrl[1]`. Bad or noisy detector channels can be masked out individually after the discriminator output, so that they do not contribute to the further signal processing. The masking is accessible via the shift register *CompMask* (cf. section C.3.7). After the masking mechanism, the discriminator decision is synchronised to the comparator clock (*CompClock*), which may differ from the sampling clock (*Sclk*) by a constant phase.

The comparator of the *Beetle* features two programmable operation modes. Figure 5.19 shows the simulation results of both modes. In *track mode* operation (`CompCtrl[4]` = 0) the output of the comparator circuit is as long active as the discriminator signal is above the threshold. In *pulse mode* (`CompCtrl[4]` = 1) the output is only active for one *CompClock* period, independent from the time over threshold of the input signal. This mode is implemented to prevent ghost hits in case of large front-end pulse remainders. However, this implies that after an active pulse the output of the discriminator must be below the threshold for at least one clock period to rearm the pulse mode detection mechanism.

After the threshold mode stage the signal path of the comparator is split into two different readout paths:

- *prompt binary* readout: the information is read out immediately via LVDS output drivers. To reduce the number of prompt readout channels, each driver sends data of eight combined comparator channels (cf. fig. 5.20). The data of the first four neighbouring channels

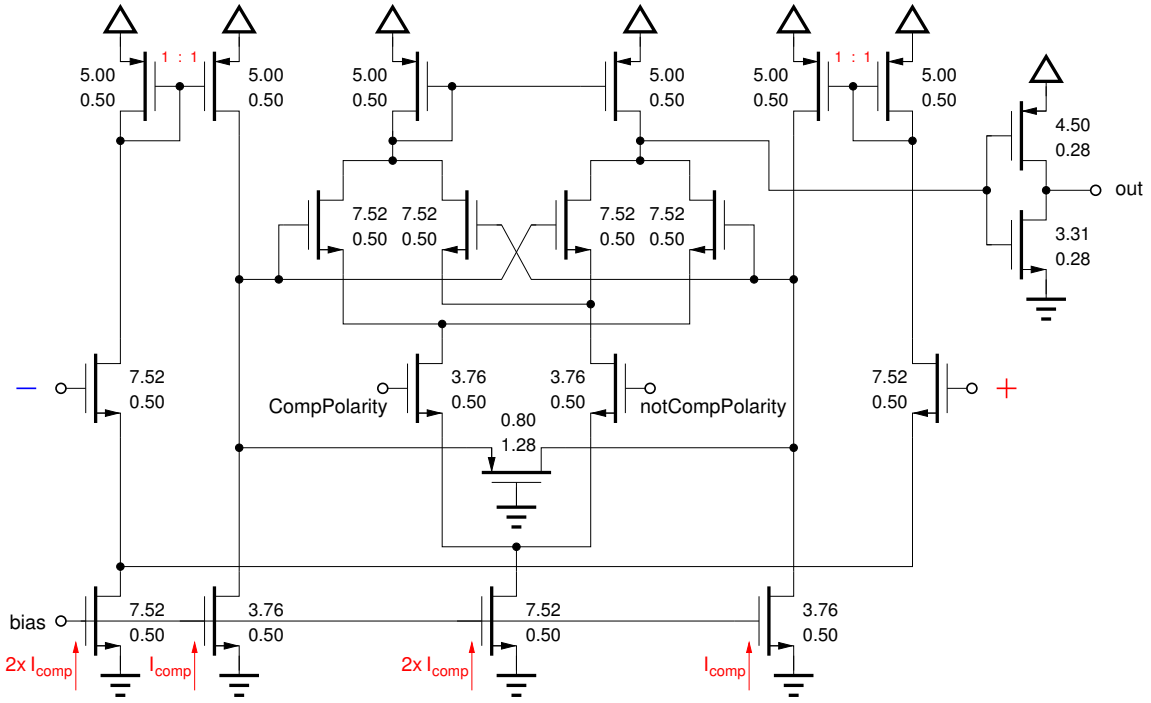


Figure 5.18: Schematic of the discriminator core. The signal input nodes are labelled with '+' and '−'. All W/L dimensions of the transistors as well as the current through the different branches are depicted in the schematic. The polarity of the discriminator is controlled by the signal *CompPolarity* and its inverted signal *notCompPolarity*. It is accessible via the *Beetle* register bit `CompCtrl[1]`.

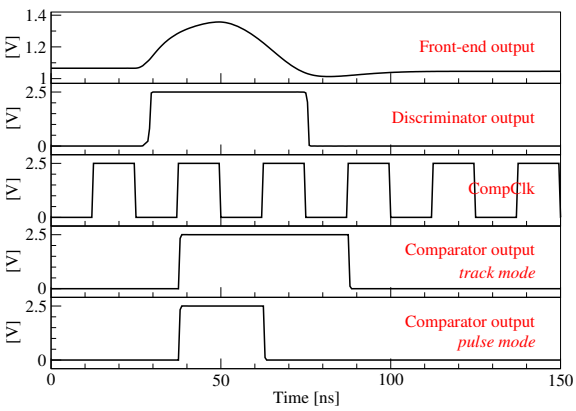


Figure 5.19: Simulation of the comparator response to a front-end pulse for the comparator operating in *track mode* respectively in *pulse mode*. The first row shows the front-end output signal, the second row gives the discriminator output response. In line three the given synchronisation clock is shown, whereas in the last two rows the outputs for the different threshold modes are shown.

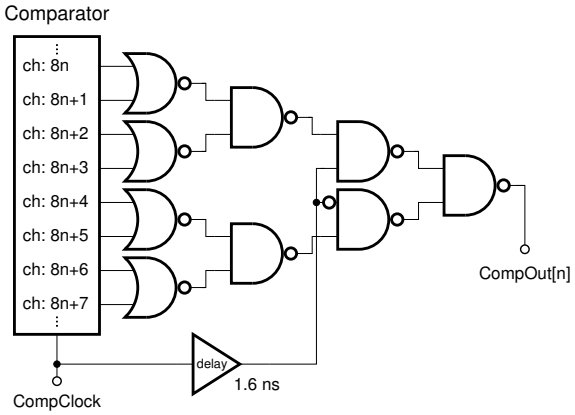


Figure 5.20: Schematic of the prompt binary output generation. Always eight neighboured comparator channels are combined to one LVDS output pad. At LVDS pad `CompOut[n]` the comparator decision from channel $8n$ to $8n + 7$ are transmitted ($0 \leq n \leq 15$).

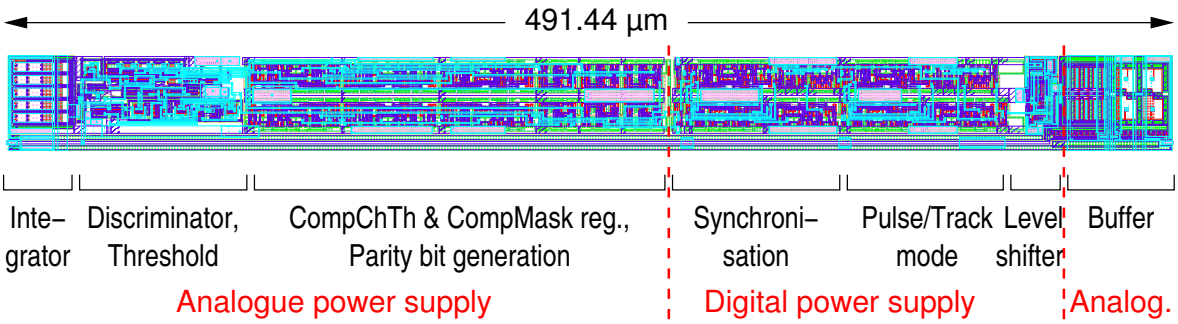


Figure 5.21: Layout of the *Beetle* comparator. The length of the layout is 491.44 µm and the width for each comparator channel is 40.24 µm. The design is split into three parts, each connected to a different power supply node.

are ORed and sent off chip during the high phase of *CompClock*, the second group of four channels during the low phase. To keep the exact timing between the comparator synchronisation stage and the LVDS output generation, the clock is delayed by 1.6 ns. The mapping of the comparator channels to the LVDS output pads of the prompt binary readout is shown in fig. 5.20. At LVDS pad `CompOut[n]` the comparator output information from channel $8n$ to $8n + 7$ are transmitted off chip ($0 \leq n \leq 15$).

- *binary pipelined* readout: a level shifter transforms the comparator output signals from 0/2.5 V to 1.120 V resp. 1.362 V, which matches the dynamic range of the subsequent analogue pipeline memory and the pipeline readout amplifier. The sense channel output voltage is set to a constant value of 1.227 V. The output buffer of the analogue encoded comparator signals uses the same source follower design as for the front-end output buffer. The biasing of the comparator buffer is also controlled via the front-end current DAC *Ibuf*.

If the detector readout system does not require the comparator functionality, the comparator part can be disabled by disconnecting the power supply nodes `VddComp`/`GndComp`, `VddCPB`/`GndCPB`, `VddCPT`/`GndCPT`[10] of the comparator block. If connected to the power supply, the comparator can temporarily be disabled by the control bit *CompDisable* (`CompCtrl[3]`), which internally switches off the analogue bias network and the comparator clock. If the *prompt binary* readout mode is not used, the LVDS output pads can be switched off separately with the control bit *DisableCompLVDS* (`CompCtrl[0]`) to reduce the overall power consumption of the *Beetle* chip.

Figure 5.21 depicts the layout of one comparator channel. The width of a single channel matches the size of a front-end channel. So both layouts exactly fit together without any pitch adapter in between. Below the layout of all comparator channels the common comparator bias and control block is located.

In the layout, the power supply nets of the comparator channels are split into three parts connecting to different power supply nodes each. This reduces the crosstalk between the possible noisy digital part and the sensitive analogue part:

- integrator, threshold and discriminator stage, output buffer and as well as the comparator configuration register *CompChTh* and *CompMask* are connected to the analogue power

[10] and also power supply node `VddaComp` in case of *Beetle1.5*.

supply of the front-end. Only for chip version *1.5* this analogue part is separated from the front-end power supply and connected to the power net `VddaComp`.

- synchronisation, pulse/track mode and level shifter stage are connected to the digital power net `VddComp/GndComp`.

5.7 Analogue Memory Cell and Pipeline

The analogue signal storage memory of the *Beetle* is implemented as a switched capacitor array. It operates as a ring buffer and is therefore called *pipeline*. The implementation of the basic functionality of an analogue pipeline cell, the sampling and storage of the front-end output information, calls for the availability of zero-offset, low-leakage switches. The MOS transistor satisfies this request. It also provides a high impedance control terminal desirable for charging the capacitor of the pipeline cell. One of the drawbacks of MOS switches is that error voltages are introduced at turn-off of the devices [She84, Kuo86, Shi87, Weg87, Hal94]. These errors are expressed as a function of the circuit parameters for two different kind of switch implementations: the NMOS transistor switch and the CMOS transmission gate switch.

5.7.1 NMOS Switch Resistance and Voltage Error

In the analogue pipeline cell the MOS transistor acts as a voltage switch inserted in the signal path. In fig. 5.22 the sample-and-hold configuration utilising an NMOS transistor (*Write*) and a storage capacitor C_S is shown. As long as the write switch is conducting, the voltage across

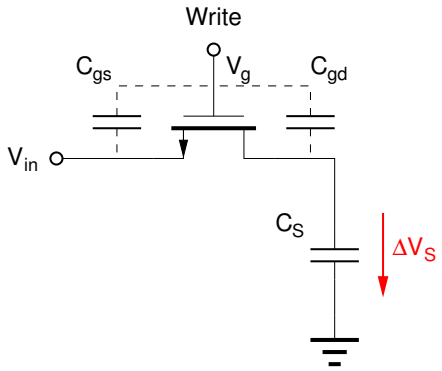


Figure 5.22: Sample-and-hold stage using an NMOS transistor as a switch.

the capacitance tracks the input voltage V_{in}. The time constant τ, which determines the voltage across C_S follows a change in input voltage, depends on the on-resistance R_{ds} of the sampling switch and on the capacitor

$$\tau = R_{ds} C_S \quad . \tag{5.36}$$

For small drain-to-source voltages the transistor is in the linear region ($V_{gs} - V_{th} > V_{ds}$), and the current through the device is given by

$$I_{ds} = \mu_n C_{ox} \frac{W}{L} \left(V_{gs} - V_{th} - \frac{V_{ds}}{2} \right) V_{ds} \quad . \tag{5.37}$$

and the on-resistance of the channel can be approximated by

$$R_{\mathrm{ds}} = \frac{1}{\frac{dI_{\mathrm{ds}}}{dV_{\mathrm{ds}}}} \approx \frac{1}{\mu_{\mathrm{n}} C_{\mathrm{ox}} \frac{W}{L} (V_{\mathrm{gs}} - V_{\mathrm{th}})} \tag{5.38}$$

with:

V_{ds}	–	drain-to-source voltage,
V_{gs}	–	gate-to-source voltage,
V_{th}	–	threshold voltage, necessary to open a conductive channel between source and drain (inversion layer at the semiconductor surface),
μ_{n}	–	electron mobility in the channel,
C_{ox}	–	specific oxide capacitance per area,
W, L	–	width and length of the transistor.

Thus the resistance of the channel is inversely proportional to the ratio $\frac{W}{L}$ of width W and length L of the transistor channel. Furthermore the resistance is non-linear since it depends on the gate-to-source voltage.

The NMOS turns off when the gate voltage drops to less than the threshold voltage V_{th} above the source potential. In the ideal case, the voltage across the storage capacitor in fig. 5.22 after turn-off is given by $\Delta V_{\mathrm{s}} = V_{\mathrm{in}}$. However, for fast sampling systems the result is disturbed by two principle error sources: the gate-overlap capacitance C_{gd} between gate and drain of the NMOS and the charge Q_{ch} in the transistor channel.

The error voltage e_{gd} due to the overlap capacitance is

$$e_{\mathrm{gd}} = -\frac{C_{\mathrm{gd}}}{C_{\mathrm{gd}} + C_{\mathrm{S}}} (V_{\mathrm{in}} + V_{\mathrm{th}} - V_{\mathrm{L}}) \tag{5.39}$$

where V_{L} is the low level gate voltage of the transistor. The total charge Q_{ch} in the channel of the transistor before turn-off is given by

$$Q_{\mathrm{ch}} = -C_{\mathrm{ox}} W L (V_{\mathrm{H}} - V_{\mathrm{in}} - V_{\mathrm{th}}) \tag{5.40}$$

where V_{H} is the high level voltage of the gate control signal. At turn-off a fraction Q_{tr} of this charge is trapped in the transistor channel

$$Q_{\mathrm{tr}} = \alpha_{\mathrm{tr}} Q_{\mathrm{ch}} \qquad \text{with } 0 \leq \alpha_{\mathrm{tr}} \leq 1 \ . \tag{5.41}$$

The value for the coefficient α_{tr} depends on the fall time t_{f} of the gate voltage and the channel transit time τ_0. It reaches its maximum when t_{f} is short compared to τ_0 [She84, Kuo86, Shi87, Weg87]. The fraction of the trapped charge that is subsequently injected onto the storage capacitor depends on the impedances at the source and drain nodes of the transistor and is one half for equal impedances. A mismatch of these impedances changes the amount of injected charge

$$Q_{\mathrm{inj}} = \alpha_{\mathrm{m}} \frac{Q_{\mathrm{tr}}}{2} \qquad \text{with } 0 \leq \alpha_{\mathrm{m}} \leq 2 \tag{5.42}$$

where α_{m} is the impedance mismatch factor. When the impedance of the signal that drives the circuit increases, less channel charge returns to the transistor and Q_{inj} becomes larger [She84, Shi87, Weg87]. For equal impedances of source and drain, α_{m} is equal one.

For the sample-and-hold circuit, the voltage error e_{ch} caused by the injected channel charge becomes

$$e_{\mathrm{ch}} = \frac{Q_{\mathrm{inj}}}{C_{\mathrm{S}}} = \alpha \frac{Q_{\mathrm{ch}}}{2C_{\mathrm{S}}} \tag{5.43}$$

where $\alpha = \alpha_{\mathrm{m}}\alpha_{\mathrm{tr}}$. With eq. 5.40 the voltage error becomes

$$e_{\mathrm{ch}} = -\frac{\alpha C_{\mathrm{ox}} WL}{2C_{\mathrm{S}}}(V_{\mathrm{H}} - V_{\mathrm{in}} - V_{\mathrm{th}}) \quad . \tag{5.44}$$

The voltage across the capacitor after turn-off of the sampling switch is

$$\Delta V_{\mathrm{s}} = V_{\mathrm{in}} + V_{\mathrm{ped}} \tag{5.45}$$

where the pedestal voltage is defined as

$$V_{\mathrm{ped}} = e_{\mathrm{gd}} + e_{\mathrm{ch}} \tag{5.46}$$

Both voltage errors e_{gd} and e_{ch} can be split into a gain and an offset error

$$V_{\mathrm{ped}} = \epsilon V_{\mathrm{in}} + V_{\mathrm{of}} \ . \tag{5.47}$$

The gain error in the circuit is given by

$$\varepsilon = -\frac{C_{\mathrm{gd}}}{C_{\mathrm{gd}} + C_{\mathrm{S}}} + \frac{\alpha C_{\mathrm{ox}} WL}{2C_{\mathrm{S}}} \tag{5.48}$$

and the offset voltage is

$$V_{\mathrm{of}} = -\frac{C_{\mathrm{gd}}}{C_{\mathrm{gd}} + C_{\mathrm{S}}}(V_{\mathrm{th}} - V_{\mathrm{L}}) - \frac{\alpha C_{\mathrm{ox}} WL}{2C_{\mathrm{S}}}(V_{\mathrm{H}} - V_{\mathrm{th}}) \quad . \tag{5.49}$$

From eq. 5.45 through eq. 5.48 it is apparent that the error voltage impressed on the sampling capacitor during turn-off depends on the input signal level.

5.7.2 Distortion and Timing Errors

For AC input signals, two additional error sources appear and must be taken into account: the potential input voltage dependency of the sampling point and the amplitude dependency of the switch resistance.

The finite slew rate of the sampling clock transition causes an input level dependency in the sampling point, and therefore sampling time errors. The fall time of the gate control signal *Write* in fig. 5.22 is t_{f}, its amplitude is A_{Write}. The input MOS transistor turns off when the gate control voltage falls below a threshold voltage above the source/drain potential, which is equal to the input signal level. Hence, the input transistor turns off earlier for high level input signals compared to low level inputs. The time $t_{\mathrm{s}}{}'$ when the signal is actually sampled is related to the ideal sampling point t_{s} as

$$t_{\mathrm{s}}{}' = t_{\mathrm{s}} + (A_{\mathrm{Write}} - V_{\mathrm{in}} - V_{\mathrm{th}})\frac{t_{\mathrm{f}}}{A_{\mathrm{Write}}} \quad . \tag{5.50}$$

The input signal dependent term causes the resulting slope dV_{s}/dt to be smaller for rising input signals and larger for falling signals. The dependency of dV_{s}/dt on dV_{in}/dt can be expressed as

$$\frac{dV_{\mathrm{s}}}{dt} = \left(1 - \frac{A_{\mathrm{S}}}{t_{\mathrm{tr}}}\frac{t_{\mathrm{f}}}{A_{\mathrm{Write}}}\right)\frac{dV_{\mathrm{in}}}{dt} \tag{5.51}$$

where A_S is the amplitude of the pulse input and t_{tr} is the rise (resp. fall) time of the pulse. The ratio A_S/t_{tr} is positive for a rising input signal and negative for a falling input signal.

The second effect leading to signal distortion at the sample-and-hold stage is the dependency of the switch resistance on the input signal level. The voltage across the storage capacitor follows the input signal with the time constant $\tau = R_{ds}C_S$, where the switch resistance is a non-linear function of the input voltage (cf. eq. 5.38). For AC waveforms the signal across the storage capacitor is therefore distorted. The magnitude of the error voltage depends on the amplitude and frequency of the AC input signal.

5.7.3 CMOS Switch Resistance and Voltage Error

The presence of PMOS transistors in a CMOS technology allows for a switch configuration commonly called a CMOS transmission gate. There NMOS and PMOS transistors are connected in parallel to a complementary switch. The sample-and-hold configuration using a CMOS switch is shown in fig. 5.23. Such a transmission gate requires the generation of complementary control signals (*Write* and *notWrite*), which is a challenge for the design of high speed sampling circuits.

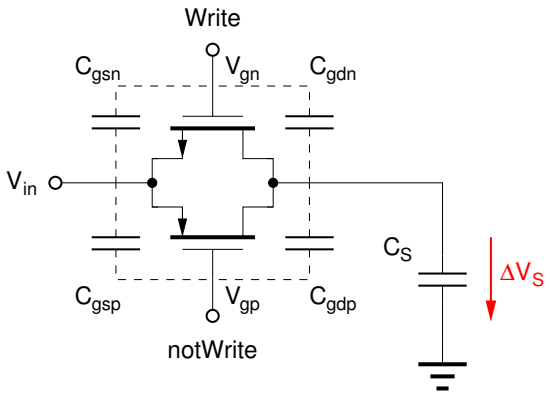


Figure 5.23: Sample-and-hold stage using a CMOS transmission gate as a switch.

The resistance of the PMOS switch is

$$R_{ds,p} = \frac{1}{\frac{dI_{ds,p}}{dV_{ds,p}}} \approx \frac{1}{\mu_p C_{ox} \frac{W_p}{L_p} (-V_{gs,p} + V_{th,p})} \tag{5.52}$$

where μ_p is the hole mobility. The gate-to-source voltage $V_{gs,p}$ and the threshold voltage $V_{th,p}$ of the PMOS transistor are negative.

The conductance of the CMOS switch is the sum of the individual NMOS and PMOS conductances

$$\frac{1}{R_{ds}} \approx \mu_n C_{ox} \frac{W_n}{L_n} (V_{gs,n} - V_{th,n}) + \mu_p C_{ox} \frac{W_p}{L_p} (-V_{gs,p} + V_{th,p}) \quad . \tag{5.53}$$

With $V_{gs,n} = V_{g,n} - V_s$, $V_{gs,p} = V_{g,p} - V_s$ and $V_{th,n} = -V_{th,p} = V_{th}$, this equation can be rewritten as

$$\frac{1}{R_{ds}} \approx g - \left(\mu_n C_{ox} \frac{W_n}{L_n} - \mu_p C_{ox} \frac{W_p}{L_p} \right) V_s \tag{5.54}$$

with

$$g = \mu_{\mathrm{n}} C_{\mathrm{ox}} \frac{W_{\mathrm{n}}}{L_{\mathrm{n}}} \left(V_{\mathrm{g,n}} - V_{\mathrm{th}}\right) + \mu_{\mathrm{p}} C_{\mathrm{ox}} \frac{W_{\mathrm{p}}}{L_{\mathrm{p}}} \left(-V_{\mathrm{g,p}} - V_{\mathrm{th}}\right) \tag{5.55}$$

where g is independent from the source voltage V_{s} [She84, Shi87, Weg87]. In the ideal case V_{s} is equal to the input signal voltage V_{in}. Thus the conductance of the transmission gate depends on the input signal level, as expressed in eq. 5.54. The second term in this equation can be eliminated by choosing the W/L ratios of the transistors according to their carrier mobility ratio

$$\frac{W_{\mathrm{n}} L_{\mathrm{p}}}{L_{\mathrm{n}} W_{\mathrm{p}}} = \frac{\mu_{\mathrm{p}}}{\mu_{\mathrm{n}}} \quad . \tag{5.56}$$

In practice, a small fraction of the input level dependency will still remain since the ratio of the carrier mobilities cannot be accurately controlled in the fabrication process.

If it is assumed that the NMOS and PMOS transistors turn off simultaneously, then the introduced error voltages of both can be summed. The voltage ΔV_{s} sampled across the storage capacitor C_{S} is again given by eq. 5.45, with

$$V_{\mathrm{ped}} = e_{\mathrm{gdn}} + e_{\mathrm{chp}} + e_{\mathrm{gdp}} + e_{\mathrm{chp}} \ . \tag{5.57}$$

Both error voltages e_{gdp} and e_{chp}, introduced by the PMOS at turn-off, can be derived in a similar way to those for the NMOS transistor:

$$e_{\mathrm{gdp}} = \frac{C_{\mathrm{gdp}}}{C_{\mathrm{gdp}} + C_{\mathrm{S}}} \left(V_{\mathrm{H}} - V_{\mathrm{in}} - V_{\mathrm{thp}}\right) \tag{5.58}$$

$$e_{\mathrm{chp}} = \frac{\alpha C_{\mathrm{ox}} W_{\mathrm{p}} L_{\mathrm{p}}}{2 C_{\mathrm{S}}} \left(V_{\mathrm{in}} + V_{\mathrm{thp}} - V_{\mathrm{L}}\right) \tag{5.59}$$

With the approximation that the threshold voltages V_{thn} and V_{thp} are identical and the gate-to-drain overlap capacitances are equal for both transistor types ($C_{\mathrm{gd}} = C_{\mathrm{gdn}} = C_{\mathrm{gdp}}$), the pedestal voltage V_{ped} is given by eq. 5.47 and the gain error is defined as

$$\epsilon = -2 \frac{C_{\mathrm{gd}}}{C_{\mathrm{gd}} + C_{\mathrm{S}}} + \frac{\left(W_{\mathrm{n}} L_{\mathrm{n}} + W_{\mathrm{p}} L_{\mathrm{p}}\right)}{2} \frac{\alpha C_{\mathrm{ox}}}{C_{\mathrm{S}}} \quad . \tag{5.60}$$

The offset voltage component V_{of} is

$$V_{\mathrm{of}} = \frac{C_{\mathrm{gd}}}{C_{\mathrm{gd}} + C_{\mathrm{S}}} \left(V_{\mathrm{H}} + V_{\mathrm{L}}\right) - \left[W_{\mathrm{n}} L_{\mathrm{n}} \left(V_{\mathrm{H}} - V_{\mathrm{th}}\right) + W_{\mathrm{p}} L_{\mathrm{p}} \left(V_{\mathrm{L}} + V_{\mathrm{th}}\right)\right] \frac{\alpha C_{\mathrm{ox}}}{2 C_{\mathrm{S}}} \quad . \tag{5.61}$$

If both CMOS switches do not turn off simultaneously, then parts of the injected channel charges do not cancel. Therefore the error voltage may be larger than suggested by eqs. 5.47, 5.60 and 5.61.

5.7.4 Capacitors

The performance of the analogue memory also depends on the quality of the capacitor structures. Important issues are the relative matching of nominally identical capacitors and their absolute sizes. Also the matching of associated parasitic capacitances plays an important role. Capacitors suitable for analogue circuit design in the chosen technology can be classified into

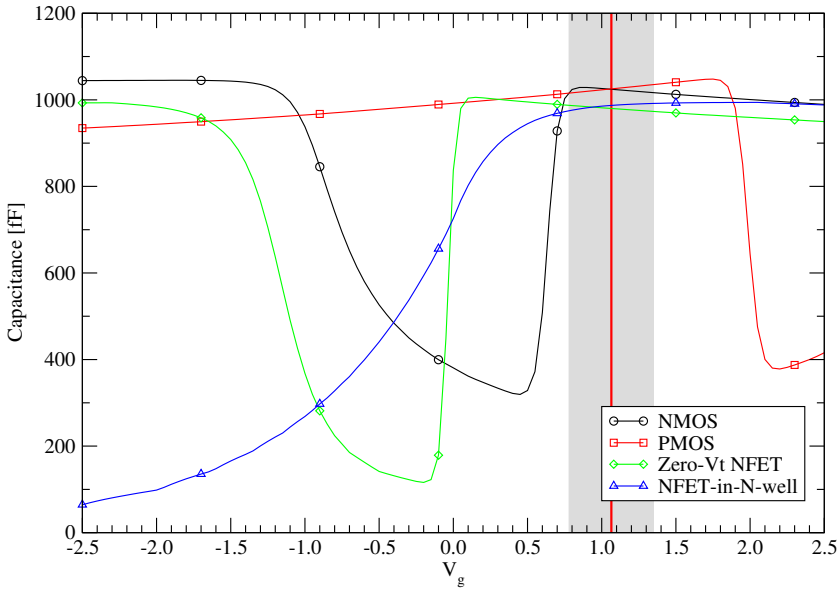


Figure 5.24: Low frequency capacitance-voltage dependency for different types of capacitors, all with the same width W and length L. The nominal front-end output offset is marked with a red line, whereas the standard operational range of the front-end is indicated by the grey area. For the PMOS transistor $V_\mathrm{d} = V_\mathrm{s} = 2.5\,\mathrm{V}$, for all other devices $V_\mathrm{d} = V_\mathrm{s} = 0\,\mathrm{V}$.

two different categories.

The first type employs the gate-source capacitance of a transistor (MOSCAP). It is a series of the gate oxide capacitance C_ox and the diffusion layer capacitance C_D underneath the gate. Depending on the applied voltage a depletion or inversion layer builds up in the device. Figure 5.24 shows the capacitance-voltage dependency of four possible capacitor models for the analogue memory cells. The characteristics for each type can be divided into three regions: But only the curves for the NMOS and the Zero-Vt devices show all regions within the selected V_g-range.

- *accumulation* region: electrons are swept out of the gate region and holes are accumulated (e.g. $V_\mathrm{gs} < -1.1\,\mathrm{V}$ for the NMOS device).
- *depletion* region: all mobile charge carriers are removed underneath the gate and a depletion layer is formed (e.g. $-1.1\,\mathrm{V} < V_\mathrm{gs} < V_\mathrm{th} \approx 0.7\,\mathrm{V}$ for the NMOS device). This results in a decrease of the total capacitance.
- *inversion* region: an inversion layer exists (e.g. $V_\mathrm{gs} > V_\mathrm{th}$ for the NMOS device). The total capacitance is nearly constant.

The voltage dependency of the total capacitance C per unit area is given by [Gre86]

$$C = \frac{C_\mathrm{ox}\,C_\mathrm{D}}{C_\mathrm{ox} + C_\mathrm{D}} = C_\mathrm{ox}\,\frac{1}{\sqrt{1 - \dfrac{2{\epsilon_\mathrm{ox}}^2 (V_\mathrm{g} - V_\mathrm{s})}{q\,n_\mathrm{D}\,\epsilon_\mathrm{Si}\,{t_\mathrm{ox}}^2}}}\quad . \tag{5.62}$$

The typical value for the gate oxide capacitance per unit area in the used 0.25 µm CMOS technology is $C_\mathrm{ox} = 5.56\,\mathrm{fF}/\,\mu\mathrm{m}^2$.

The second type of capacitor uses the capacitance between two metal layers (MIMCAP). The advantage of this capacitor structure is its low voltage dependency. The total capacitance of such a capacitor device is given by eq. 5.22. A typical value for the capacitance per unit area in the used technology is $C_a = 0.69\,\mathrm{fF}/\,\mu\mathrm{m}^2$.

5.7.5 *Beetle* Pipeline

The analogue pipeline of the *Beetle* is realised as a matrix of 130 × 187 memory cells. The number of pipeline rows is identical to the number of front-ends: 128 input channels plus one test channel and one sense channel for the common mode correction. The total number of 187 columns is given by the maximum trigger latency of 160 sampling intervals (cf. table 2.6), the integrated trigger readout buffer of 16 stages and an additional computation overhead of 17 intervals [Tru00, Bau03].

For the memory cell of the *Beetle* a sample-and-hold configuration consisting of only an NMOS transistor as the write switch and a MOSCAP of 982 fF as the sampling capacitor is used. Since the layout of the NMOS is very small and the capacitance of a MOSCAP per unit area is very high, this helps to minimise the total chip area (total area of pipeline memory: $7.8\,\mathrm{mm}^2$)[11]. The drawbacks of this configuration are distortion of the analogue signal, voltage dependency of the sampling capacitor and the matching over the complete pipeline.

For each cell a second NMOS transistor (*Read*) is added to the sampling-and-hold configuration. It is necessary for reading out the analogue information to the subsequent pipeline readout amplifier. The final schematic of the pipeline storage cell is shown in fig. 5.25.

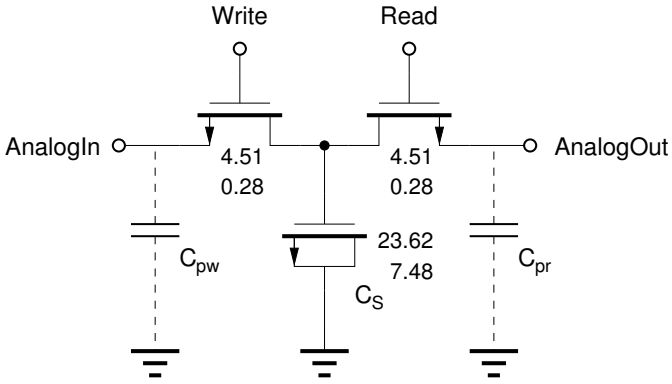
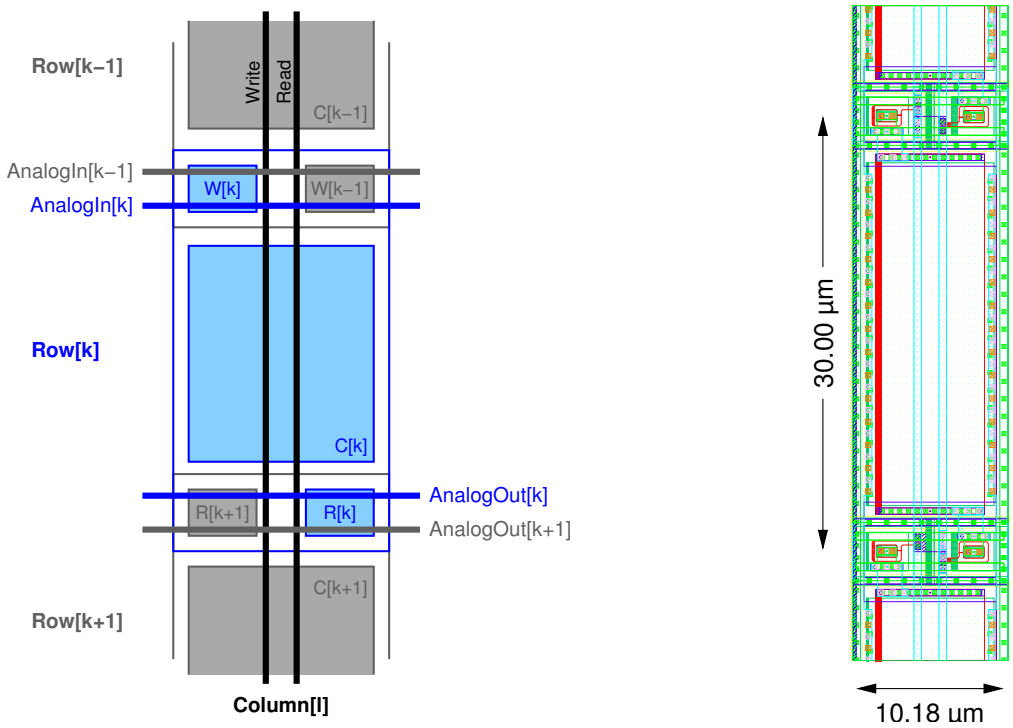


Figure 5.25: Schematic of the analogue pipeline cell. The capacitance of the MOSCAP sampling capacitor C_S is 982 fF. The parasitic line capacitances of the input line (C_{pw}) and of the output line (C_{pr}) is drawn into the schematic.

The design of the analogue pipeline cell is shown in fig. 5.26. The input lines (`AnalogIn`) and the output lines (`AnalogOut`) of the cells are shared by all columns of the same channel. But the layout provides maximum separation between both lines. This reduces possible signal crosstalk from the input to the output line or vice versa. The layout of neighbouring rows is flipped, such that the input resp. output lines of two adjacent channels are routed together.

[11] The total area for the memory, using ideal transmission gates and MIMCAPs, would be approximately 5 times larger ($38.6\,\mathrm{mm}^2$).



(a) Principle (b) *Beetle1.3* layout

Figure 5.26: Principle design (a) and final layout (b) of a *Beetle* pipeline cell. The analogue storage cell `C[k]` with the nearby cells `C[k±1]` is shown. The layout of neighbouring rows is flipped with respect to each other, such that the input resp. output lines of two adjacent channels are located close together. Underneath the input lines the write switches (`W`) of the two neighbouring channels are placed, whereas underneath the output lines the two read switches (`R`) are grouped.

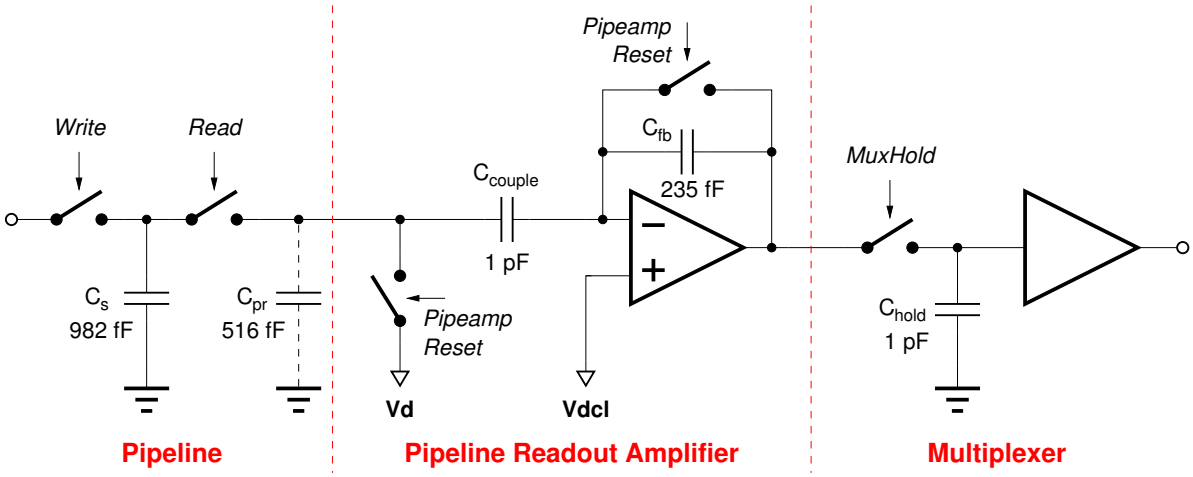


Figure 5.27: Schematic of the pipeline readout amplifier. The schematic of the sampling & hold stage of a pipeline cell as well as of the track & hold circuit in the subsequent multiplexer stage are also shown. The timing sequence of all control signals is depicted in fig. 5.30.

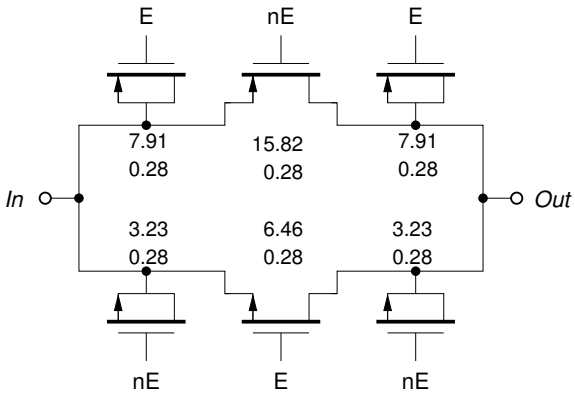


Figure 5.28: Schematic of a transmission gate with dummy MOS transistors for compensation of charge injection during turn-on/turn-off.

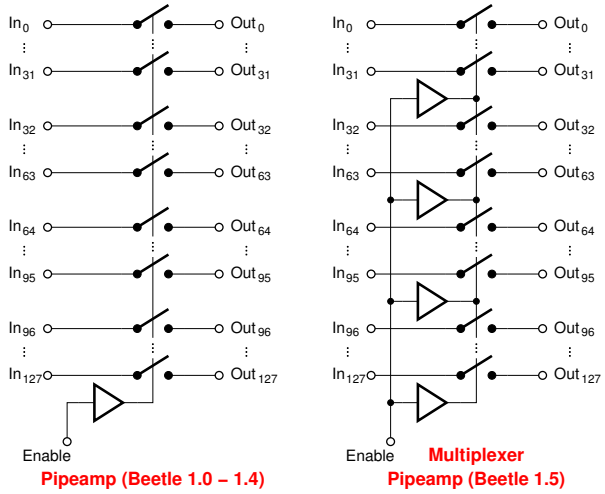


Figure 5.29: Control signal distribution scheme of the transmission gates. The *PipeampReset* transmission gates are driven by only one output buffer for all 128 channels (left), whereas for the *MuxHold* transmission gates four buffers are spread across the channels (right). *Beetle1.5* uses the latter scheme also for its *PipeampReset* signal.

5.8 Pipeline Readout Amplifier (Pipeamp)

The analogue signal information, stored as charge in the pipeline memory cell, is read out by the *pipeline readout amplifier* (or short *pipeamp*). It is implemented as a resettable, AC-coupled Charge-Sensitive Amplifier (CSA) with a folded cascode configuration as amplifier core cell (designed by Daniel Baumeister [Bau03]). The purpose of the pipeamp is to read out the charge from the pipeline capacitor (C_S) and to pass it to the hold capacitor of the multiplexer (C_{hold}). The schematic of the pipeamp, together with a corresponding pipeline cell and the subsequent track & hold stage of the multiplexer is shown in fig. 5.27. Transmission gates are used for all switches in the pipeamp (reset of amplifier and pipeline-to-pipeamp readout line) and the multiplexer hold stage. Figure 5.28 shows the schematic of such a transmission gate. It is realised as a fully compensated transmission gate using NMOS and PMOS transistors switching simultaneously (cf. 5.7.3) and dummy transistors of half the size connected to source and drain of the switching transistors [Gei90].

For the control of the transmission gates two different signal distribution schemes are implemented. A sketch of these is shown in fig. 5.29. One uses only one large buffer for all transmission gates of all 128 channels. The advantage is that the layout of all channels can be placed close to each other and that there is only one digital control line that intersects the sensitive analogue signal lines. The drawback is the huge R-C delay of the distributed signals, which will cause a switching delay between different channels. This one buffer scheme is implemented for all transmission gates in the pipeline readout amplifier, except for *Beetle1.5* chips. The maximum delay of the switching point between pipeamp channel 127 and 0 is 1.5 ns. In the second model four buffers are spread across all channels, which will reduce the R-C delay

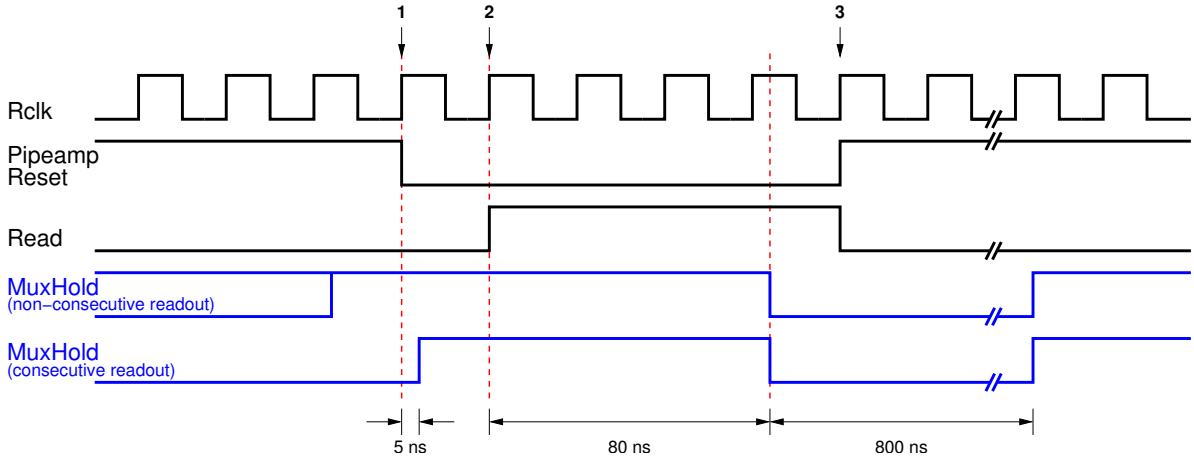


Figure 5.30: Timing sequence of the pipeamp control signals. The time intervals corresponds to the nominal LHCb readout frequency of $Rclk = Sclk = 40\,\text{MHz}$. *PipeampReset* controls the feedback switch of the pipeamp and the reset switch of the input line between pipeline and pipeamp, *Read* the readout switch of the pipeline cell and *MuxHold* the sampling switch of the subsequent multiplexer stage. All signal changes are driven by the positive edge of *Rclk*, whereas an additional delay of $\approx 5\,\text{ns}$ is added to *MuxHold* to prevent a simultaneous switching of *PipeampReset* and *MuxHold*.

of the transmission gate control signals. In this case the drawback is that two digital lines intersect the analogue lines. Also, additional buffers have to be added in the layout (one every 32 channels), which break apart the regular layout structure. The distributed buffer model is applied for the transmission gates of the multiplexer and for the pipeamp in the *Beetle1.5* chip. Here, the maximum switching delay between channel 127 and channel 0 is 0.3 ns which improved the uniformity of the channel offsets.

The timing sequence of the control signals is depicted in fig. 5.30. If a trigger signal is received by the *Beetle*, the reset signal of the pipeline readout amplifier (*PipeampReset*) is released. One clock cycle after the release, the read-switch of the pipeline cell, that will be read out, is closed. The charge from the sampling capacitor C_S is now integrated by the pipeamp. Another three clock cycles later, the track & hold switch *MuxHold* of the multiplexer is closed and the output voltage of the pipeamp is sampled on the hold capacitor C_{hold}. Another clock cycle later the *Read* switch is released and the pipeamp is set back into the reset state ($PipeampReset = 1$). In between two pipeline readouts the pipeamp is permanently in the reset state to avoid a shift of the DC operation point caused by leakage currents. At the end of the serialised readout of all 128 channels, the track & hold capacitor is switched back into track mode ($MuxHold = 1$). The hold capacitor is then connected to the defined output voltage of the pipeamp, which is now in the reset state between two readout events. Otherwise the hold capacitor would be in a floating state and by leakage currents the capacitor would leave its DC operation point (cf. A.2.2 low trigger rate problem).

The timing sequence of the signal *MuxHold* differs for *non-consecutive* or *consecutive* readout modes[12]. If the *Beetle* is triggered for a consecutive readout, the timing of the *MuxHold* start position is critical. In between the release of the *PipeampReset* signal and the start of the

[12] The *Beetle* chip has two different possible readout timings called *non-consecutive* and *consecutive* readout. A non-consecutive readout starts after a trigger occurs during a non-readout period. If the *Beetle* receives a sec-

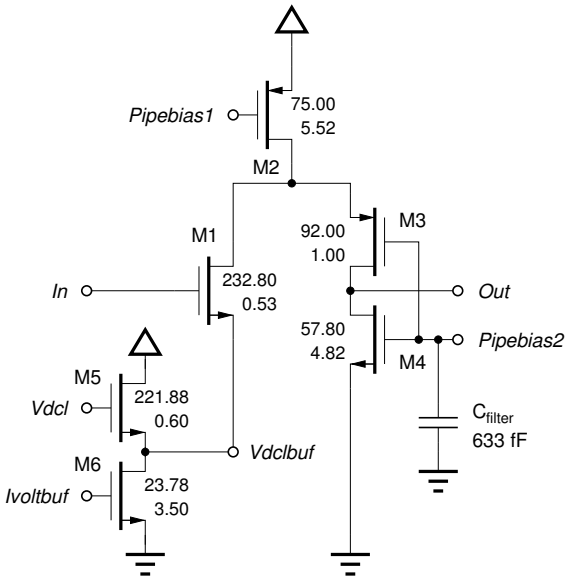


Figure 5.31: Schematic of the pipeline readout amplifier core and the *Vdcl* input buffer. C_{filter} is implemented as a blocking capacitor for the common bias node *Prebias2* to reduce possible distortions during signal integration.

g_{m}	0.95 mA/V
C_{tr}	878 fF [15]
C_{fb}	235 fF
C_{load}	1 000 fF
C_{in}	1.11 pF
C_{out}	1.24 pF
GBW_{rad}	769 rad/ µs
GBW	122 MHz
τ	38.7 ns
ν	4.1 MHz
t_{r}	85.1 ns

Table 5.6: Parameters of the *Beetle* pipeline readout amplifier. The parameters are taken from simulations, parasitic capacitance extractions from the final layout and from the design manual [PDM01].

Read signal, *MuxHold* has to switch into track mode (*MuxHold*=1). A switching of *MuxHold* at the same time as the release of *PipeampReset* is forbidden, otherwise the reset condition of the pipeamp would be disturbed. Also, it is not possible to switch *MuxHold* before *PipeampReset* because the multiplexer is still occupied with channel serialisation and readout[13]. Therefore a delay circuit has been added into the signal path of *MuxHold* between the digital control logic and the multiplexer. This circuit delays a low to high transition of *MuxHold* by 5.1 ns and a high to low transition by 3.9 ns[14].

The amplifier core of the pipeamp is implemented as a folded cascode. Its transient behaviour and the small signal model behaviour is similar to the preamplifier case (cf. section 5.4.1). The detailed schematic of the amplifier core cell is shown in fig. 5.31. The biasing of the amplifier core requires one current and one voltage. The operating current is controlled via the *Beetle* register *Ipipe*. The bias voltage (`Vdclbuf`) acts as the non-inverting input of the amplifier. It shifts the operating point towards the dynamic range of the pipeline. The node `Vdclbuf` has to sink the current of the input branch. Therefore a zero-Vt source follower (`M5` and `M6`) is implemented into each pipeamp channel. The zero-Vt input transistor[16] `M5` is controlled by the voltage DAC *Vdcl* whereas the current through the load transistor `M6` is set via the

ond trigger during a readout cycle, the next readout is transmitted as a consecutive readout (cf. section C.3.8 and fig. C.12).

[13] In case of a non-consecutive readout the multiplexer is in the idle state. Therefore it is possible to set the track & hold signal *MuxHold* at least one clock cycle before the release of *PipeampReset* into track mode.

[14] In case of *Beetle1.5*, the delay at a low to high transition is 5.2 ns but a high to low transition is only 98 ps. Therefore the multiplexer is switched off ≈ 3.7 ns earlier at the end of a readout.

[15] $C_{\text{tr}} = C_{\text{gate}}\,(686\,\text{fF}) + C_{\text{gs}}\,(102\,\text{fF}) + C_{\text{para}}\,(90\,\text{fF})$

[16] An NMOS transistor with a threshold voltage V_{th} close to 0 V (≈ 10 mV).

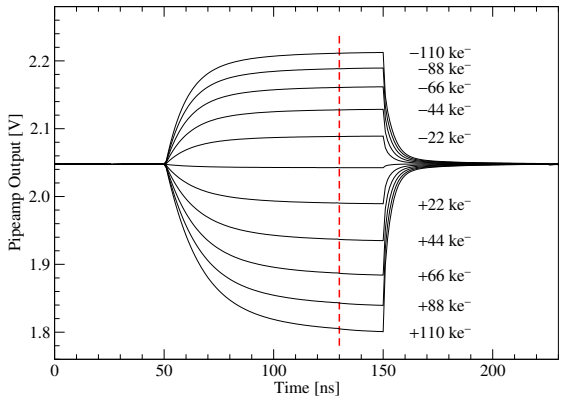


Figure 5.32: Transient simulation of the pipeline amplifier output. The equivalent input charge varies from $-110\,\mathrm{ke}^-$ to $+110\,\mathrm{ke}^-$. The sampling point of the subsequent track & hold stage of the multiplexer is marked with a dashed line.

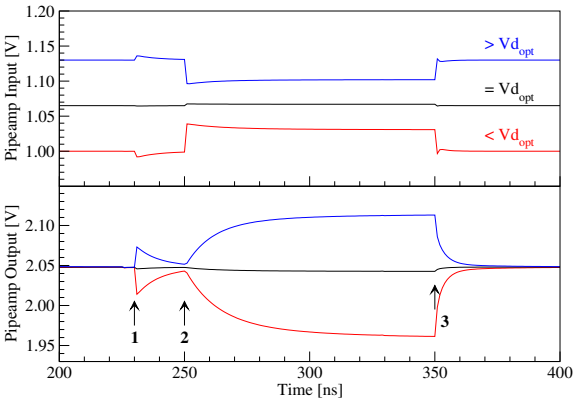


Figure 5.33: Behaviour of the pipeamp for three different pipeamp reset voltages *Vd*. The transient simulation of the pipeline-to-pipeamp readout path is shown in the upper plot, the pipeamp output in the lower plot. The marked positions correspond to the marks in the timing diagram of fig. 5.30.

current DAC *Ivoltbuf*. All 130 channel buffer output nodes (`Vdclbuf`) are interconnected and routed to the pad `Vdclbuf` for external blocking. A second bias voltage `Vd` is used for discharging the parasitic pipeline-to-pipeamp readout line capacitor C_{pr} and the capacitor C_{couple} (cf. fig. 5.27). `Vd` is controlled by the voltage DAC register *Vd* and represents the DC potential of the readout line. Its voltage should be identical to the DC output offset of the front-end buffer. In between two readout sequences the pipeline readout amplifier is reset to this voltage. This avoids a drift of the DC operation point due to leakage currents. The node `Vd` also has to sink a current and needs to be buffered. Unlike the channel buffering of `Vdcl`, `Vd` is only buffered once for all 130 channels. The buffered node is also connected to a pad (`Vdbuf`) for external blocking.

The rise time t_{r} of the pipeamp can be calculated by eq. 5.8. With the extracted parameters for the pipeamp of table 5.6, the rise time calculates to $t_{\mathrm{r}} = 85\,\mathrm{ns}$. This is well acceptable with the 80 ns integration resp. setup time from fig. 5.30.

Figure 5.32 shows the transient output response of the pipeline readout amplifier for front-end input signals that are equivalent to $\pm 110\,\mathrm{ke}^-$. 80 ns after the beginning of the integration, the output of the pipeamp is sampled to the hold capacitor of the subsequent multiplexer (dashed line). The intrinsic nonlinearity of the pipeline amplifier (fig. 5.32) is almost compensated by the subsequent multiplexer and contributes only insignificantly to the overall nonlinearity of the chip. A transient simulation of the pipeamp for three different reset potentials *Vd* is shown in fig. 5.33. The pipeline cell is loaded with the front-end DC output offset for all simulations. For $Vd = Vd_{\mathrm{opt}}$ (black line) the reset voltage is identical to the output offset of the front-end buffer. In this case the pipeline readout signal shows no disturbance. If *Vd* differs from the ideal reset potential, all pipeline readout lines are charged and discharged within each readout sequence. The pipeline readout amplifiers of the 128 input channels as well as the pipeamp of the sense channel then integrate this mismatch and store the signal on the track & hold capacitor of the subsequent multiplexer channel. But, due to the on-chip sub-

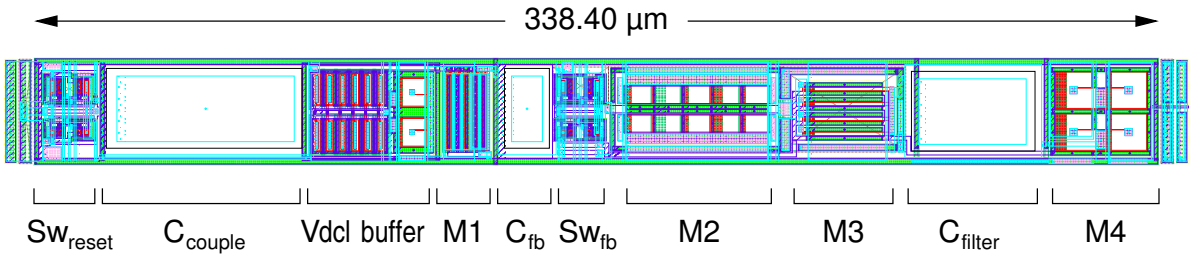


Figure 5.34: Layout of one *Beetle* pipeline readout amplifier. The length of one pipeamp channel is 338.40 µm and has a width of 30 µm, defined by the channel pitch of the previous pipeline cell. The corresponding schematic of the pipeamp is shown in fig. 5.27 and fig. 5.31.

traction of the sense channel, this mismatch is almost completely compensated in the analogue output driver (cf. section 5.10).

Finally the layout of a pipeline readout amplifier channel is shown in fig. 5.34. The length of a complete channel is 338.4 µm and has a width of 30 µm, which is defined by the channel pitch of the previous pipeline. The large CMOS transmission gates with the dummy transistors ($\mathtt{Sw}_{\mathrm{reset}}$ and $\mathtt{Sw}_{\mathrm{fb}}$) are clearly visible in the channel layout. All capacitors ($\mathtt{C}_{\mathrm{couple}}$, $\mathtt{C}_{\mathrm{fb}}$ and $\mathtt{C}_{\mathrm{filter}}$) are implemented as MIMCAP devices.

The pipeamp is connected to the analogue power supply of the *Beetle*. In the overall layout of all pipeamp channels, all operating currents are supplied from the top (channel 0) and bottom side (channel 127). The supply voltage of the single channels drops to the centre channels of the pipeamp due to the resistance in the power supply lines. It is important to keep this voltage mismatch small. Otherwise the pipeamp output offset will vary across all channels. For the pipeline readout amplifiers the resistance of the power net *Vdda* is $R_{\mathrm{Vdda}} = 11.23\,\frac{\mathrm{m}\Omega}{\mathrm{ch.}}$ and for *Gnda* the resistance is $R_{\mathrm{Gnda}} = 20.24\,\frac{\mathrm{m}\Omega}{\mathrm{ch.}}$. The higher ground net resistance is a disadvantage of the design[17]. This bottleneck has been removed for *Beetle1.5* chips by a modified power scheme. Here the resistance per pipeamp channel has dropped to $Vdda = 9.97\,\frac{\mathrm{m}\Omega}{\mathrm{ch.}}$ and $Gnda = 9.51\,\frac{\mathrm{m}\Omega}{\mathrm{ch.}}$.

5.9 Multiplexer

The task of the *Beetle* multiplexer is to serialise the data of the 128 parallel channels and to generate the readout header information. It operates with the readout clock *Rclk* which is derived internally from the sampling clock *Sclk*. The ratio is programmable via register *RclkDiv* (cf. section C.4.2) and is by default 1, so that $Rclk = Sclk$, i.e. 40 MHz.

The time for reading out all 128 channels off chip is limited by the LHCb Level-0 specification to 900 ns (cf. section 5.1). Using the *nominal data rate*[18] limits the multiplexer serialisation factor to 32 : 1. Therefore, 4 parallel operating multiplexer and readout ports are necessary to fulfil the LHCb requirement.

An increase by a factor of 2 at the same clock frequency can be obtained using *double data rate*, i.e. transferring data synchronous to both clock edges with effectively 80 MHz.

[17] If a ground net has a higher impedance than the corresponding *Vdd* net, equalising currents may flow through the substrate of the chip

[18] The definition of nominal data rate is here: running with a LHCb clock frequency of 40 MHz, sending the analogue data synchronous to one edge of the clock and keeping the information for one clock cycle period.

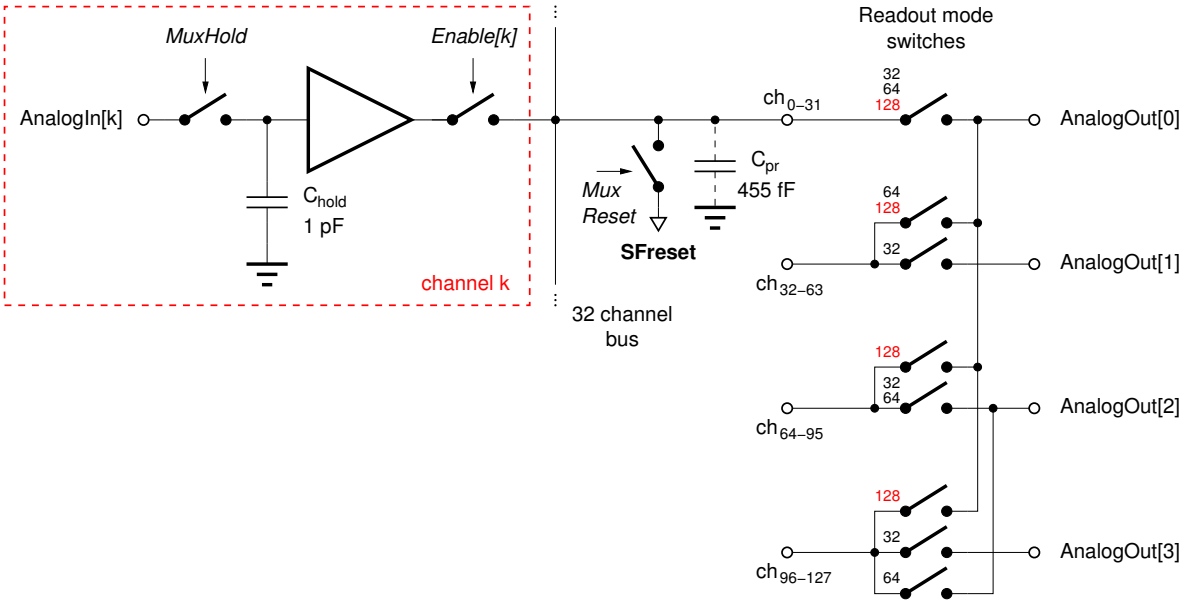


Figure 5.35: Schematic of the analogue multiplexer stage. Each channel of the multiplexer includes an input switch (*MuxHold*), a sampling capacitor (C_{hold}), a source follower and an output switch (*Enable[k]*). Groups of 32 multiplexer channels are connected to one of the four internal buses which are then multiplexed depending on the multiplexer readout mode.

The *Beetle* multiplexer provides three different operation modes:

- Analogue readout on 4 ports
  4 readout ports are running in parallel, each carrying 32 channels. The readout works with nominal data rate and needs 800 ns. This is the nominal analogue readout mode for the Vertex Locator, Trigger Tracker and the Inner Tracker detectors.

- Binary readout on 2 ports
  2 ports are running in parallel, each carrying 64 channels. The readout works with double data rate and needs 800 ns. This is the readout mode for RICH's MaPMT option.

- Analogue readout on 1 port
  1 port is carrying 128 channels. The readout for the analogue channels needs 3.2 µs. This mode is for applications with less demanding readout speed requirements or the need for a minimum number of output lines.

These readout modes are controlled via the register *ROCtrl* (cf. section C.3.5 for details).

The schematic diagram of the multiplexer is depicted in fig. 5.35. Its internal structure reflects the modes of operation of the multiplexer. At the beginning of a readout, the output of the predecessor pipeline readout amplifier stage is sampled onto the hold capacitance C_{hold} of the multiplexer and buffered by a source follower. Groups of 32 input channels are serialised by the first multiplexer stage onto one of four internal buses (ch_{0-31}, ch_{32-63}, ch_{64-95} and ch_{96-127}). The multiplexing onto the internal 32 channel bus is controlled by the *Enable* signal, which is the output of a flip-flop (fig. 5.36). The flip-flops of each group form a shift-register. The

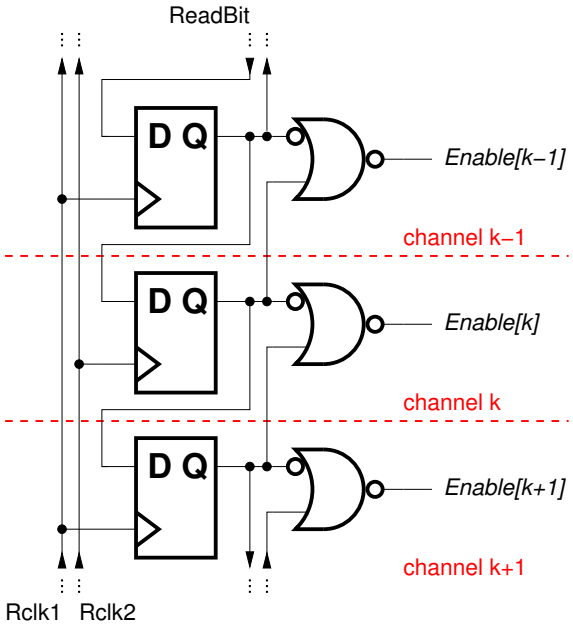


Figure 5.36: Shift register and readout switch control schematic of the multiplexer.

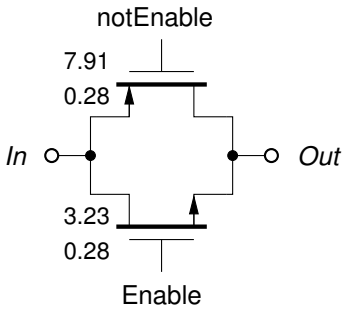


Figure 5.37: Schematic of a transmission gate, used as a signal switch in the multiplexer output stage.

control bit (*ReadBit*) is shifted with the *Rclk1* respectively *Rclk2* from channel to channel[19]. The source follower is necessary to drive the capacitive load of the 32 channel bus line and the switches of the other channels contributing to the same bus ($C_{\mathrm{pr}} = 455\,\mathrm{fF}$).

Special care has been taken concerning charge injection of the switches. In the multiplexer complementary switches are used without any direct charge injection compensation mechanism (cf. section 5.7.3). The switching action between neighbouring channels is therefore controlled in such a way, that opening a switch takes place at the same time ($\mathcal{O}\,10\,ps$) when closing the switch of the subsequent channel. This is achieved by ORing the flip-flop outputs of channel k with the adjacent channel $k+1$ as shown in fig. 5.36. The channel charge released by the opening switch is almost absorbed by the closing one since the switches are connected via the 32 channel bus.

The second stage of the multiplexer in fig. 5.35 is responsible for the three different readout modes. These readout mode switches connect the 4 different groups of the first multiplexer stages to the corresponding output ports. The second stage is also responsible for the adding the readout header in front of the first analogue channel data.

5.10 Analogue Output Driver

The task of the analogue output driver is to drive the analogue output signal to the successive stage in the readout chain, which is usually an Analogue-to-Digital-Converter (ADC). In case of the VELO the ADC is located about 1 m [TDR5] away from the *Beetle* chip, whereas for the ST the length of the readout path is 5 m [TDR8]. The output driver is realised as a

[19] In case of double data rate $Rclk1 = \overline{Rclk2} = Rclk$. In all other operation modes $Rclk1 = Rclk2 = Rclk$.

fully differential Operational Transconductance Amplifier (OTA). The advantage of a current amplifier compared to a voltage amplifier is a reduced power consumption and an insensitivity to high capacitive loads of the external readout lines.

The maximum operating frequency of the current output driver is defined by the multiplexer. In case of *binary readout* operation (cf. section 5.9), the multiplexer runs at an effective frequency of 80 MHz. The dynamic range covers the full signal range of the preceding circuits and the differential output has to be able to drive at least an impedance of 50 Ω.

The output drivers went through different levels of development [Sex01, Bau03]. The final circuit schematic is depicted in fig. 5.38 and the corresponding layout is shown in fig. 5.39. The current through the current source transistor is controlled by the node *bias* and is exactly half the current of the current DAC *Icurrbuf*. The output operation of the four amplifiers depends on the serialisation mode of the multiplexer. In case an amplifier is not used for reading out data, the biasing of the complete circuit is switched off via *EnableRO* to reduce the total power consumption of the *Beetle* chip. *EnableRO* is generated by the digital part of the multiplexer circuit. To prevent any influence from this possibly noisy signal onto the bias network, a buffer is connected upstream of the NMOS switch. The buffer itself is connected to the noiseless analogue power supply.

The differential amplifier is completely symmetric and uses NMOS input transistors with a threshold voltage close to 0 V (zero-Vt). This allows to operate in a large dynamic signal range. The negative input node '−' of the amplifier is connected to the sense channel of the *Beetle* and is therefore subtracted from the serialised output data, which is connected to the positive input node '+'. The output stage of both branches uses very large transistors to drive the large currents. The current through the PMOS transistor ($\frac{W}{L} = \frac{316.40}{0.28}$) in the output branch corresponds to the twentyfold current of the corresponding input branch. For the NMOS transistor ($\frac{W}{L} = \frac{129.20}{0.28}$) transistor the twentyfold current of the opposite branch is used as the reference. At maximum input signal amplitude the current through the amplifier output stage is 10-times the output of current DAC *Icurrbuf* and is therefore limited to 20 mA per output driver. All dimensions in the layout, like current densities in different metal layers, contact current limitations and power supply lines, are designed to handle these maximum currents. Therefore the output stage of the analogue driver cell is spread across the complete layout with large routing layers in between (cf. fig. 5.39). In addition decoupling capacitors (cf. section 5.13) are included into the design to reduce possible noise effects to the analogue signals. They are connected to the power supply lines and to the bias network and add up to a total blocking capacitance of 50.3 pF resp. to 17.8 pF for all four output driver circuits.

In the case that the voltage of the sense channel at node '−' is equal to the signal voltage of the readout data at node '+', the currents through both input branches exactly match. Therefore the currents in both output stages are the same and no current is driven off chip. For this case the DC output voltage at *AnalogOut* and *notAnalogOut* is 877 mV [20].

When reading out the *Beetle* in *binary pipelined mode* (cf. section 5.6), the binary signals of the comparator are transmitted via the output driver by changing the direction of the output current. The transmission fulfils the LVDS specifications [NSC04] and can be read out by commercial LVDS receivers.

[20] The operational current of the analogue output driver is set to *Icurrbuf* = 800 µA.

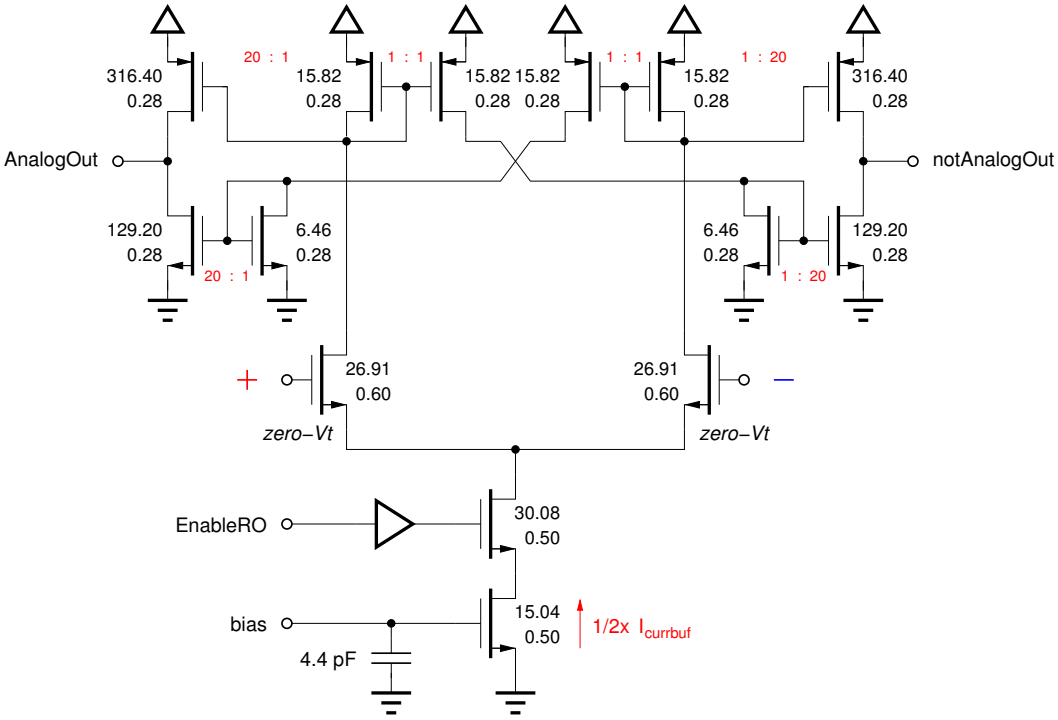


Figure 5.38: Schematic of the differential analogue output driver.

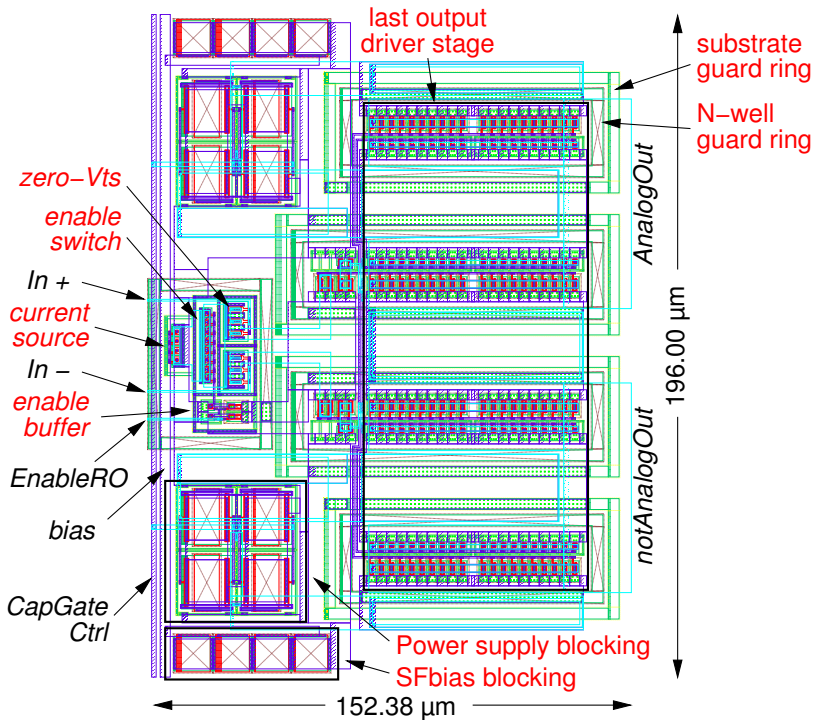


Figure 5.39: Layout of the analogue output driver.

5.11 Digital Control Logic

Two digital control circuits are integrated in the *Beetle* chip, operating at two different clock domains. The first one is the so-called *slow control*. It implements the programming interface of the chip with the corresponding decoders for register access. The slow control works within the I^2C-clock domain of about 100 kHz, which is asynchronous to the LHCb sampling clock. The second digital part is the *fast control* with event storage and readout as main functions. It is running in the sampling clock domain of 40 MHz. Both parts are also separated in the layout of the chip (cf. fig. 5.2).

The logic functionality of the *Beetle* chip is modelled with the Hardware Description Language (HDL) *Verilog*® [Tho02] and synthesised[21] using the *Synopsys*® software [Syn00]. The ensuing placement and routing of the logic is done with *Silicon Ensemble* [CDS][22].

This section characterises briefly the slow and fast control of the *Beetle* and the methods to achieve Single Event Upset (SEU) robustness of the two digital logic blocks. A more detailed discussion of the control logic is included in [Bau03].

5.11.1 Slow Control

At LHCb a dedicated communication and control path is used between the various components of the detector and the Experiment Control System (ECS) [TDR7, TDR7a]. The ECS system foresees I^2C or JTAG[23] protocols for the communication with the front-end devices.

The programming interface of the *Beetle* chip uses the I^2C-protocol [Phi95] which is a simple serial communication bus system with two bi-directional wires (Serial Clock (SCL) and Serial Data (SDA)). The two bus lines are connected with external pull-up resistors to a positive supply voltage and perform a wired-AND connection of all connected bus devices. The I^2C-bus is multi-master capable, but only one master device at a time is allowed to initiate data transfers. The *Beetle* operates as a slave device and needs to be addressed by an unique 7-bit number[24] before it responds to data transfers. Besides this individual access, a *general call* broadcast is possible, where all devices on the I^2C-bus are programmed simultaneously.

The data transfer on the I^2C-bus is initiated by the I^2C-master, which generates the clock signal and addresses the slave devices. All data are transferred asynchronous to the LHCb sampling clock but synchronous to the I^2C-clock SDA with a rate up to 100 kbit/s. The communication is byte oriented and the Most Significant Bit (MSB) is always transferred first.

Figure 5.40 shows the transfer sequences of a I^2C-read and write access. The master device initialises the I^2C-bus (`S`) and transmits the 7-bit address of the slave device. A direction bit ($\mathtt{R}/\overline{\mathtt{W}}$) indicates transmission or request of data. The addressed slave device responds with an acknowledge bit (`A`). Subsequently the 8-bit data frames follow, each acknowledged by the slave. In write mode ($\mathtt{R}/\overline{\mathtt{W}} = 0$) the *Beetle* chip always interprets the first data byte as the pointer byte to a register. The data transmission can continue as long as each data byte is acknowledged by the slave device. The data transmission will stop immediately after the I^2C-master sends a stop condition (`P`). In read mode ($\mathtt{R}/\overline{\mathtt{W}} = 1$) two possibilities exist:

[21] Synthesis: the schematic is generated automatically based on the HDL description.

[22] The development of the fast and slow control is independent from each other. Only the final layouts of both blocks are placed together on the final chip.

[23] JTAG, an acronym for Joint Test Action Group, is the usual name used for the IEEE 1149.1 Standard Test Access Port and Boundary-Scan Architecture. It is used for testing access ports of printed circuit boards via a boundary scan.

[24] The 7-bit address space has only 112 valid entries (8...119), cf. section C.4.1.

Figure 5.40: I^{2}C-bus write and read sequences for register access on the *Beetle*. Each 8-bit frame of the transfer is acknowledged by the receiver with one bit (`A`). `P` indicates the stop condition sent by the master device.

- *Preset pointer*: the data transfer starts immediately after the bus initialisation and an acknowledge of the *Beetle* chip. In this mode the address pointer has been set in a previous readout.
- *Pointer set followed by immediate readout*: after initialising the transfer and sending the chip address, the pointer byte is transmitted within the second frame. Then the I^{2}C-bus is re-initialised (`Sr`), the chip address is sent and the data from the *Beetle* are read out.

In contrast to the write mode, the master device acknowledges the data bytes in the read mode.

In total the *Beetle* contains 24 addressable registers (cf. table C.14), classified into four different groups:

- Current and voltage DAC registers (reg. 0 to 15),
- Configuration registers (reg. 16 to 19),
- Shifter registers for individual channel settings (reg. 20 to 22),
- Read-only information register (reg. 23).

The standard configuration of a 8-bit register (e.g. reg. 0 to 19) and its connection to the internal bi-directional data bus of the *Beetle* is shown in fig. 5.41. Both *Write* and *Read* signals are served by the slow control whereas the *notReset* signal is controlled by the on-chip power-up reset generator (cf. section C.3.4). The three shift registers differ from the standard

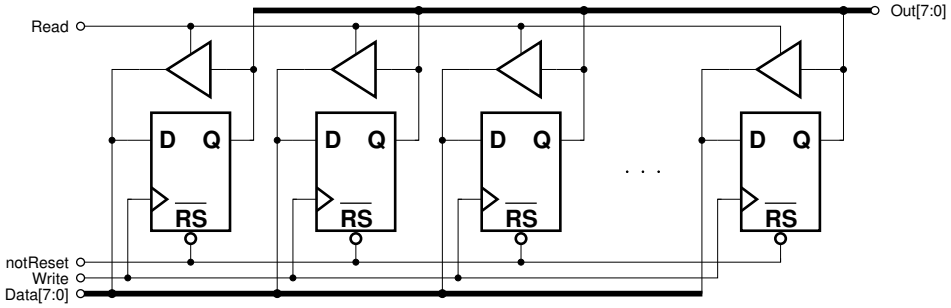


Figure 5.41: Standard configuration of a 8-bit *Beetle* register. The read back of the stored register data is realised via tristate buffers that are connected to the internal bi-directional data bus.

register configuration. Register *TpSelect* (reg. 22) contains 129 single bits, segmented in 17 8-bit registers[25]. Register *CompMask* (reg. 21) implements 128 bits, segmented in 16 8-bit groups. The last shift register *CompChTh* (reg. 20) has a width of 5-bit and 128 shift stages. A consecutive access to the corresponding register address shifts the data into the next frame. The data information at the end of the shifting chain is readable, which allows a verification of the shifted data. A detailed diagram which maps the shift data processing is shown in fig. C.16.

All *Beetle* registers are part of the slow control clock domain, but are not implicitly part of the slow control layout. For example, the bias registers (reg. 0 to 9) and the comparator configuration register (reg. 19) are part of the front-end bias generator layout (cf. fig. 5.2) and the shift registers (reg. 20 to 22) are embedded into the channel layout of the test pulse and comparator circuits. All other registers are included in the slow control core layout.

A detailed description of the register programming, internal register organisation and operation of the *Beetle* chip can be found in *The Beetle Reference Manual* (cf. appendix C).

5.11.2 Fast Control

The *fast control* is the central control unit of the *Beetle* chip and provides the logic control for the whole chip. It accomplishes the following tasks:

- Control of the write and read switches of the analogue pipeline,
- Allocation of pipeline locations that are marked by a readout trigger signal until they are read out,
- Provision of the reset signals to the pipeline readout amplifier,
- Generation of the control and start signals for the multiplexer,
- Control of the *daisy chain* if several chips share their output lines.

The development of the digital *Beetle* core is partly based on the *Verilog* code of the Helix chip [Tru00]. It was adapted by Daniel Baumeister to comply with the requirements for the

[25] Only one bit is implemented in the 17th register for the test channel. The remaining 7 unused bits are not implemented as register devices (cf. fig. C.16).

LHCb Level-0 front-end electronics (cf. section 5.1) and it is implemented into the readout electronics of the dedicated LHCb subsystems.

The specifications foresee a clock driven operation at 40 MHz and a maximum Level-0 trigger rate of 1.1 MHz with a maximum latency of 160 clock cycles (cf. table 2.6). The digital fast control operates clock driven and clock synchronous to the LHC bunch crossing signal (= *Sclk*) and follows all specifications given by the LHCb experiment.

The basic operation of the fast control logic is described as follows: all write switches of one complete pipeline column are closed when the internal write pointer contains the address of this column. Each *Sclk* cycle the write pointer is increased until it reaches the physical size of the pipeline (= 187) then it starts again from zero[26]. The trigger pointer follows the write pointer at a defined distance, which represents the latency. Upon an external trigger signal, the content of the trigger pointer is stored in a derandomising buffer (FIFO) and the corresponding pipeline column is protected from write cycles by the write pointer. Up to 16 triggered pipeline locations can be stored in the FIFO. Triggered events are read out by releasing the pipeline readout amplifier from the reset state and closing all read switches of the corresponding pipeline column. The signal is now loaded from the pipeline via the pipeline readout amplifier into the multiplexer. If the event read out is completed by the multiplexer, the corresponding pipeline location is released in the FIFO and the pipeline column can be overwritten with new front-end data. The write and read access to the pipeline operate independently and thus allow a readout without dead times within the limits of the FIFO.

5.11.3 Single Event Upset Robustness of Digital Memory Devices

On the *Beetle* chip all digital memory devices are sensitive to Single Event Upsets (SEUs), which are mainly induced by the radiation environment caused by the operation of the LHCb detector. These redundant devices are realised as D-type flip-flops and can be classified into *quasi-static* and *clocked* devices [Bau03]. The *quasi-static flip-flops* are used in all bias and configuration registers of the *Beetle*. These are clocked only when a write access via the I^2C-interface occurs (cf. fig. 5.41. Inside the control logic the so-called *clocked flip-flops* are used. They form the state registers of finite state machines, the derandomising buffer, shift registers and counters. These are clocked with the sampling clock or a small fraction of it.

An unexpected change due to SEU can have severe consequences to the operation of the *Beetle* chip. For example:

- a change of the state register bit can cause the logic to stop operating correctly or to get stuck in an undefined state,
- a change in the configuration register can switch the chip into another operation mode,
- a change in the bias registers can move the operating point of an amplifier,

Therefore a protection mechanism is necessary on the *Beetle* chip. The choice of a specific mechanism to prevent the propagation of an SEU error is mainly driven by the following constraints:

- *Topology*
  The sensitive devices are spread across the *Beetle* chip area. For example, the bias registers are placed close to the current and voltage DACs of the front-end and back-end

[26] A monitoring pad is implemented to the *Beetle* chip for test purpose. Each time the internal write pointer contains the address of column number 0, pad `WriteMon` is pulsed for one sampling clock cycle.

bias generator blocks, with a distance of several millimetres in between (cf. fig. 5.2). The comparator synchronisation and operation flip-flops are located in each channel of the comparator. All configuration registers and other flip-flops are spread in the logic blocks underneath the pipeline, pipeline readout amplifier and multiplexer.

- *Area*
  Especially the front-end bias registers are limited in area. These are constrained by the front-end at top and the control logic at right.

- *Error latency*
  The time between the occurrence of an SEU and the detection and correction should be as fast as possible to avoid an error transfer to the next bunch crossing (e.g. one clock cycle or less).

For the *Beetle* chip an implementation of redundant flip-flips with a *majority voting* mechanism has been chosen [Bau03]. These flip-flops are used for the quasi-static as well as for the clocked devices. Figure 5.42 shows the circuit of such a redundant flip-flop device. It consists of three internal flip-flops, operating in parallel (thus called *triple redundant*). The majority output of the three internal flip-flops is indicated with `Q`. The second output `F` indicates if the logic states of the three internal flip-flops are not equal. This new flip-flop device is called Triple-Redundant Flip-indicating D-type Flip-Flop (TRFDFF). In addition to this large device, a smaller version without a flip indication mechanism is used in some parts of the *Beetle* chip. This subset version is named TRDFF.

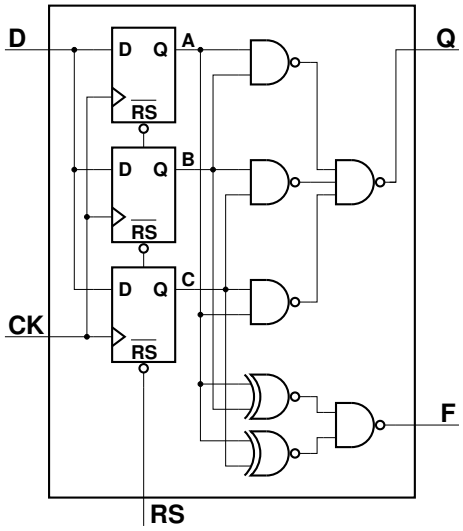


Figure 5.42: Triple redundant flip-flop. The majority output is labelled with `Q`. An additional output `F` flags a logic difference of the internal flip-flop outputs.

Input			Output	
A	B	C	Q	F
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	1
1	0	0	0	1
1	0	1	1	1
1	1	0	1	1
1	1	1	1	0

Table 5.7: Truth table of the triple redundant flip-flop. `A`, `B` and `C` are the nodes of the internal standard flip-flops. `Q` is the majority output and `F` is the flip indication output.

The derivation of the majority voting combinational logic and the flip indication mechanism is given by [Bau03]

$$Q = \overline{\overline{A \cdot B} \cdot \overline{A \cdot C} \cdot \overline{B \cdot C}} \tag{5.63}$$

$$F = \overline{\overline{A \oplus B} \cdot \overline{A \oplus C}} \tag{5.64}$$

The implementation of eqs. 5.63 and 5.64 with logic gates avoids glitches which occur if the propagation delays of signals are not equal. The corresponding truth table of the majority output `Q` and the flip indication `F` is depicted in table 5.7.

All quasi-static registers are made of TRFDFF type flip-flops with a flip indication output node. This allows the implementation of a stand-alone *self-triggered correction* mechanism. The flip-flop output `Q` as well as the flip indication output `F` are fed back to the data respectively to the clock input (cf. fig. 5.43). Two switches select between the feedback loop and the external

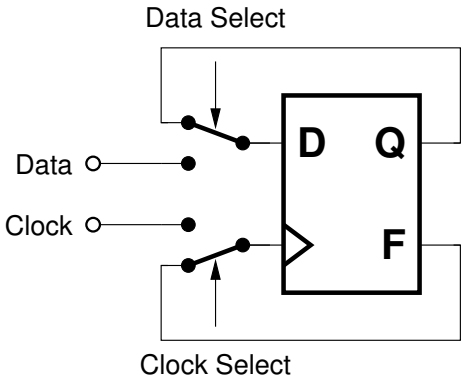


Figure 5.43: Schematic of a self-triggered SEU correction flip-flop. The switches select between feedback loop and external access control.

inputs. The control strobes *Data Select* and *Clock Select* are served by the I^{2}C-interface. As long as the I^{2}C-bus is busy the external inputs of the flip-flops are activated whereas a free bus selects the internal feedback loop[27]. The switching sequence of the data and clock control signals is important for proper operation. At a transition from external to internal control the data port is switched first and then, with a delay of $\approx 200\,\text{ps}$, the clock port follows[28]. This guarantees that at the moment of switching a meanwhile occurred SEU cannot trigger the flip-flop and violate the setup time. At an opposite transition from internal to external control, the clock port is switched first. This avoids a self-triggering of the flip-flop while external data is present at the data input.

All clocked registers of the digital control logic use only the TRDFF type flip-flop without a flip indication and self-triggered correction mechanism. An occurred SEU, that flipped one of the three internal flip-flops of a TRDFF, will be fixed automatically by the continuous refreshing of the control logic.

As a special feature an 8-bit SEU counter is integrated in the *Beetle* to indicate the number of occurred upsets. All *Beetle* registers, including the three shift registers, are contributing to the SEU counter. The flip-flops used in the control logic are not taken into account. The clock for the counter is generated as the logic OR connection of the flip indication outputs of the TRFDFFs. The counter output is mapped to a read-only register (reg. 23), which is accessible via the I^{2}C-interface. The SEU counter is reset with an I^{2}C-write access to this register. Besides

[27] The I^{2}C-stop condition activates the correction mechanism. An interrupted I^{2}C-data transfer without an proper I^{2}C-stop condition can lead to a malfunction of the correction mechanism.

[28] The delay corresponds to the setup time $t_{\text{su}} \approx 200\,\text{ps}$ of a flip-flop.

this the two Least Significant Bits (LSBs) of the counter are flagged into the header of the analogue readout. This allows a fast monitoring of SEUs during readout.

5.12 Bias Generators

The *Beetle* chip needs different voltages and currents to set the numerous DC operating points within the chip. These bias values have an effect on the overall chip performance, e.g. the noise and shaping time of the front-end, the threshold of the comparator or the pipeline readout amplifier operating points. To allow performance optimisations, all important biasing nodes need to be adjustable. But in LHCb with thousands of readout chips it is impossible to provide this large number of bias voltages or currents. Therefore all necessary *Beetle* bias nodes are generated on-chip. For biasing the *Beetle*, 5 voltages and 11 currents are necessary. These are adjustable via 8-bit Digital-to-Analogue-Converters (DACs). All digital DAC inputs are controlled by registers accessible via the I^2C-interface of the *Beetle* chip (cf. section 5.11.1).

In this section the three main biasing components of the *Beetle* are described: the current source, which provides a constant reference current, the current DAC and the voltage DAC.

5.12.1 Current Source

The *Beetle* chip integrates two identical but independently operating current sources. These provide the necessary reference currents for the current DACs[29]. As an ideal current source, the current output response over the complete range of load voltages should be constant. Therefore the output resistance R_{out} needs to be large, which is achieved by a small drain current I_{d} of the output FET. The differential output resistance r_{out} of a FET for small-signals is the derivative $\frac{\delta V_{\text{d}}}{\delta I_{\text{d}}}$ in the saturation region and should by infinite in the ideal case. The exact value of r_{out} can be extracted from

$$r_{\text{out}} = \frac{|V_{\text{A}}|}{I_{\text{d}}} = \frac{1}{\lambda I_{\text{d}}} \tag{5.65}$$

where $|V_{\text{A}}|$ is the 'Early voltage'[30] and λ the channel modulation parameter[31]. On the other hand the reference current I_{d} needs to be large compared to the foreseen LSB current ($\approx 8\,\mu\text{A}$) of the subsequent current DACs to neglect the effect of noise coupling and current fluctuations. Both, a large output current I_{out} and a large output resistance R_{out} can be achieved by employing 'bootstrapping' methods[32]. A current source that makes use of this method is the *regulated cascode* configuration, which is implemented in the *Beetle*.

Figure 5.44 depicts the schematic of the implemented regulated cascode current source and fig. 5.45 the corresponding layout of this cell, both originally developed by Nigel Smale [Sma04] and enhanced by minor changes to the actual version. The two resistors (each $6\,035 \pm 541\,\Omega$) and the PMOS transistor `M5` form a voltage divider that sets the gate voltage of `M3` to the

[29] One current source supplies the current for all analogue stages before the pipeline (biased by the *front-end bias generator* block), the second current source provides the current for all parts after the pipeline (biased by the *back-end bias generators* block). See also the schematic block diagram (fig. 5.1) of the *Beetle* chip.

[30] 'Early voltage' is the intersection point on the negative V_{ds} axis of the extrapolation of an I_{d} vs. V_{ds} plot from the linear part of the curve when in saturation.

[31] Typical values of λ, normally defined for minimum channel length dimension, range from greater than $0.1\,\text{V}^{-1}$ for short channel devices to $0.01\,\text{V}^{-1}$ for long channels.

[32] 'Bootstrapping' is a DC feedback mechanism that uses an amplifier to constrain a circuit node to a fixed voltage or current value.

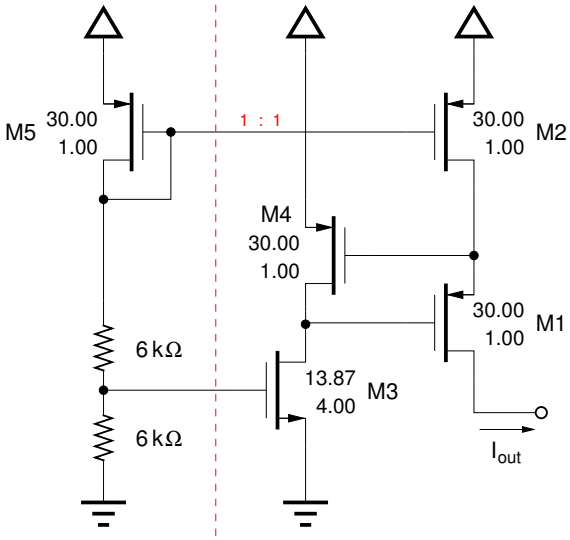


Figure 5.44: Schematic of the regulated cascode current source.

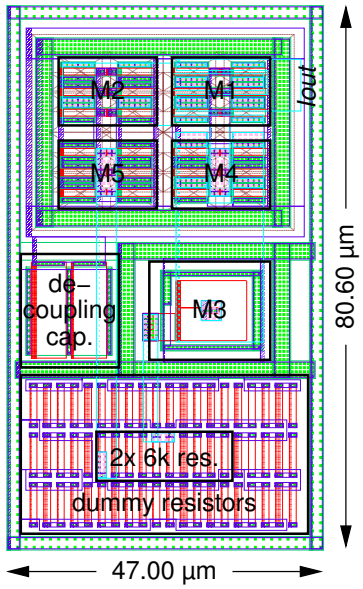


Figure 5.45: Layout of the regulated cascode current source.

saturation region. M5 is used to act as a current mirror to the load transistor M2 of the cascode with a current aspect ratio of 1. The cascode itself is formed by the PMOS transistors M1 and M2. The feedback loop is composed of the transistors M1, M3 and M4, where M3 and M4 form a common source amplifier and M1 works as source follower. This configuration stabilises the drain-source voltage V_{ds} of the load transistor M2 and increases the output resistance of it.

The voltage gain A_{v} of common source amplifier, with a fixed V_{gs} of M3 as an active load-resistor, is given by

$$A_{\mathrm{v}} = g_{\mathrm{m4}}(r_{\mathrm{out4}} \parallel r_{\mathrm{out3}}) \ . \tag{5.66}$$

In the ideal case, a large voltage gain requires that the differential output resistances r_{out3} of M3 and r_{out4} of M4 have large values. Because of the $\frac{W}{L}$ aspect ratio limitation of enclosed transistors, the NMOS load transistor M3 has a larger I_{d} and therefore a reduced r_{out3}.

When all transistors operate in the saturation region, the output resistance R_{out} of the *Beetle* regulated cascode current source is given by [Gei90]

$$R_{\mathrm{out}} \simeq r_{\mathrm{out2}} \cdot \frac{g_{\mathrm{m1}} g_{\mathrm{m2}}}{g_{\mathrm{ds1}}(g_{\mathrm{ds4}} + g_{\mathrm{m3}})} \tag{5.67}$$

where g_3 is the conductance of M3 and r_{out2} is the incremental output resistance of M2.

The simulation of the current output behaviour of I_{out} for different load voltages V_{load} is depicted in fig. 5.46. For load voltages smaller than 1.9 V the output I_{out} supplies a constant current of 126.2 µA.

To increase the performance and stability of the regulated cascode, special design techniques have been applied to the layout (cf. fig. 5.45):

- a common centroid configuration of matched PMOS devices to decrease the mismatch,
- dummy resistors around the voltage divider to reduce the resistance mismatch due to geometry fringe effects,

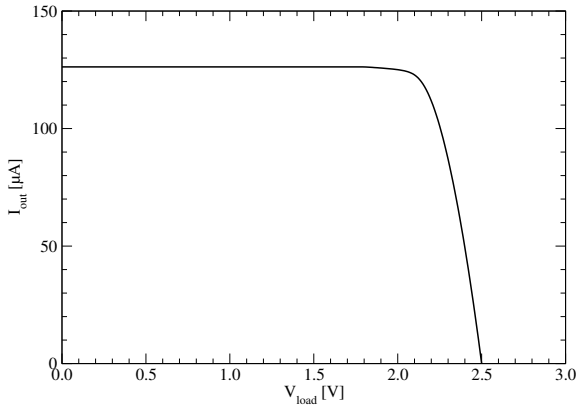


Figure 5.46: Simulated output current I_{out} vs. load voltage V_{load} of the regulated cascode.

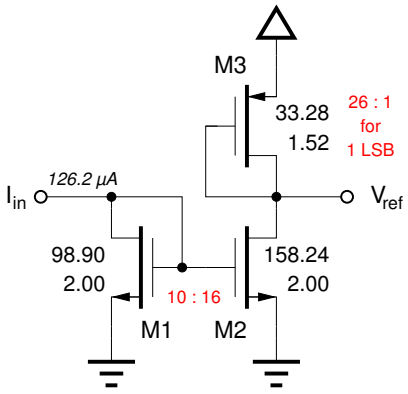


Figure 5.47: Schematic of the current mirror used for generating the reference gate voltage of the current DAC.

- use of a local decoupling capacitor.

5.12.2 Current DAC

The operating currents of the different analogue stages of the *Beetle* are supplied by 11 adjustable current Digital-to-Analogue-Converters (DACs). Each DAC has a resolution of 8-bit and is formed by $2^8 - 1 = 255$ current sources, arranged in a binary-weighted configuration (cf. fig. 5.48). For the current source a PMOS transistor, operating in the saturation region, is used.

Ideal current sources have a low g_{m} to make the transistors insensitive to fluctuations of the gate-source voltage V_{gs}. This reduces the effects due to noise at the transistor gate and improves the drain current of duplicated devices. Ideal current sources also have a high output resistance compared to the load to keep the variations of the output current small for varying voltage load conditions.

To fulfil the low g_{m} and high output resistance requirements, three parameters can be varied: the width W, the length L and the DC operating point ($= V_{\text{gs}}$) of the PMOS current source transistor. Small values are chosen for the transistor dimensions ($W = 1.28$ µm, $L = 1.52$ µm[33]) since the physical size of the eleven current DACs is also an important design criteria.

The gate voltage of the PMOS transistor is derived from the common current source of the *Beetle* (cf. section 5.12.1) via two current mirrors. Figure 5.47 depicts the schematic of these devices. The first current mirror, formed by `M1` and `M2`, multiplies the input current ($= I_{\text{out}}$ of the common current source) by a factor of $\frac{16}{10} = 1.6$. This results in a current of 201.9 µA through transistor `M3`. The PMOS transistor `M3` itself is diode-connected and forms the second current mirror in each current source of the DAC. With a ratio of 26 : 1 the current through the output branch is divided down to 7.77 µA per LSB transistor. The corresponding reference voltage V_{ref} at the gate of a current source results in 1.293 V, which biases the PMOS in the

[33] Using a channel length L larger than the minimum allowed will reduce the value λ of eq. 5.65. Reducing λ increases r_{out}, which is the current source output resistance in this case. The width W has no influences in this case and can be made closer to the design rules without the consequences due to short channel effects.

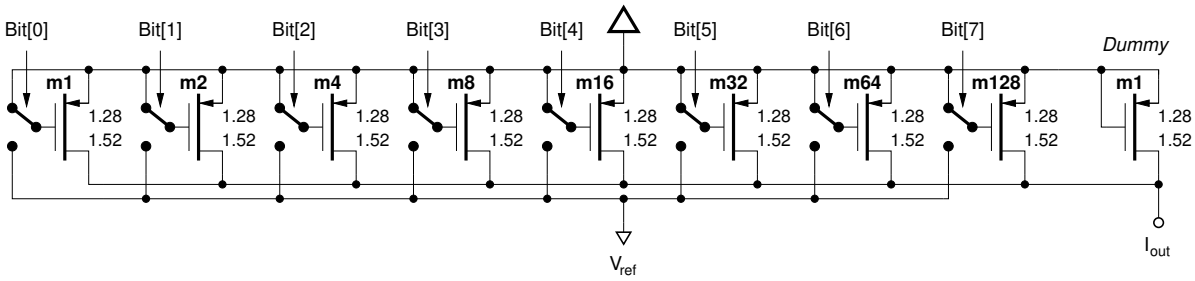


Figure 5.48: Schematic of the binary weighted current DAC output stage. The label m represents the multiplier of LSB-FETs used per binary weighted stage.

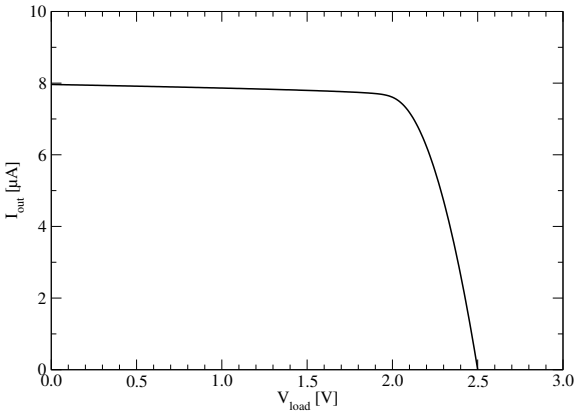


Figure 5.49: Simulated LSB output current I_{out} vs. load voltage V_{load} of the current DAC.

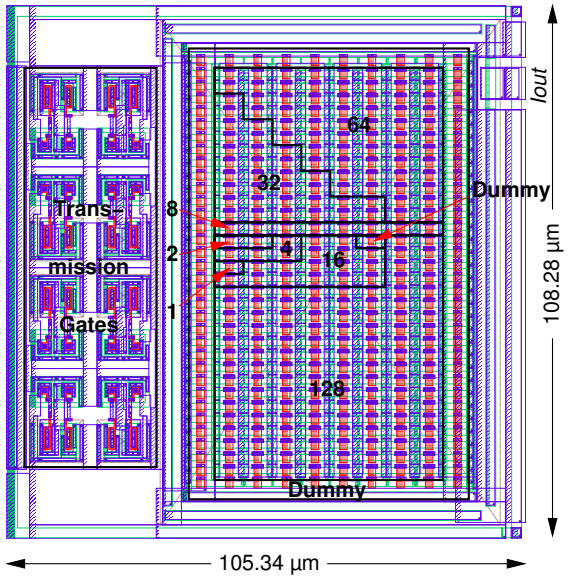


Figure 5.50: Layout of the analogue core of a 8-bit binary weighted current DAC. The numbers represent the numbers of LSB-FETs used per binary weighted stage (cf. fig. 5.48).

saturatuion region. A simulation of the device output current I_{out} (=1 DAC LSB) versus the load voltage V_{out} for the chosen geometry and bias setting is shown in fig. 5.49. The output current is nearly constant for load voltages up to 2 V. It drops to 0 A above 2 V.

The schematic of the binary-weighted current DAC core is shown in fig. 5.48. The label m denotes the number of PMOS current sources connected in parallel. The corresponding digital control bit obtained from the register output (TRDFF, cf. fig. 5.42) controls a CMOS transmission gate switch (cf. section 5.7.3) connected to the gate of the PMOS transistors. It switches between two voltages: the positive analogue supply voltage *Vdda* (switching the transistor off) and the reference voltage V_{ref} (which results in a DC current of 7.72 µA per device).

Figure 5.50 shows the layout of analogue part of the current DAC. On the left side the eight transmission gates are placed, the binary-weighted PMOS output stage is shown on the right. The layout of the DAC is critical as the accuracy and linearity depend on the matching

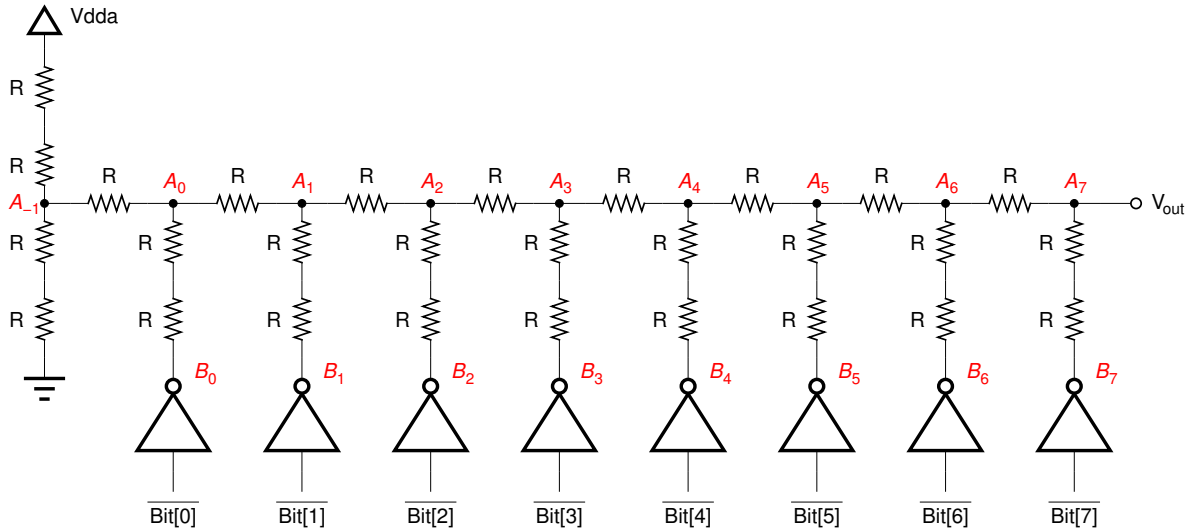


Figure 5.51: Schematic of the 8-bit R-2R voltage DAC converter. The implemented value R of each resistor is 8.45 kΩ with a maximum error of $\Delta R = 0.73\,\text{k}\Omega$ from chip to chip, caused by process variations.

of the 255 transistors. A non-monotonic DAC results if the Differential Nonlinearity (DNL) error exceeds ±1 LSB. This leads to the requirement that the matching of the MSB group of transistors to the LSB transistor must be better than $\frac{1}{2^{8-1}}$ or 0.78%. To facilitate this requirement, the preferred configuration is a common centroid layout of all PMOS transistors of the same group. This ideal solution can not be achieved due to routing constraints and area consumption. Therefore all transistors are grouped together with respect to their associated bit number. The distribution of the 8 binary weighted groups is marked in the layout of fig. 5.50. The numbers represent the number of LSB current sources used per stage. An additional dummy PMOS transistor, connected to *Vdda*, is added to the design to keep the regular symmetric structure of the DAC. Another 84 dummy transistors enclose the core structure to suppress geometric fringe effects.

5.12.3 Voltage DAC

The *Beetle* chip requires five different, externally adjustable voltage nodes (cf. fig. 5.1). All voltages nodes have high input impedance[34] and a low voltage-precision requirement. The implemented voltage DACs use a R-2R ladder configuration, which has nearly a full rail-to-rail dynamic range. A R-2R design only requires n switches and $2n + 2$ resistors, where n is the resolution of the DAC in bits. The main disadvantage is a poor DNL characteristic, caused by the impedance of the inverters or the resistance of the switches respectively. The DNL is also influenced by the matching of the polysilicon resistors of the different R-2R networks.

Figure 5.51 depicts the schematic of an 8-bit R-2R voltage DAC. The resistor chain connected between the power supplies forms a voltage source with an output resistance of R and a voltage of $\frac{Vdda}{2}$ at the node A_{-1}. The R-2R configuration consists of a network of resistors

[34] Two nodes (*Vd* and *Vdcl*) do have some current demand. Therefore these voltages are buffered at their inputs.

that alternate in value by R and $2R$[35]. Each group forms a voltage divider of a factor of 2. The output B_i of an ideal inverter[36] is either 0 V or the positive supply voltage $Vdda$. In general the node voltage A_i then is

$$A_i = \begin{cases} \frac{Vdda}{2} & \text{for } i = -1 \\ \frac{A_{i-1}}{2} + \frac{1}{2}B_i & \text{for } i \geq 0 \end{cases} \tag{5.68}$$

where $i = -1$ is associated with the voltage source and $i = 0$ with the LSB. B_i is the voltage which corresponds to the i$^{\text{th}}$ bit ($B_i = 0$ V resp. 2.5 V for the i$^{\text{th}}$ bit = 0 resp. 1) of the DAC register. The output voltage V_{out} as a function of the applied binary number is given by

$$\begin{aligned} V_{\text{out}} \;=\; A_{n-1} \;&=\; \frac{Vdda}{2^{n+1}} + \frac{1}{2^{n+1}} \sum_{i=0}^{n-1} 2^{i+1}\, B_i \\ &=\; \frac{Vdda}{2^{n+1}} \cdot \left(1 + 2 \cdot \sum_{i=0}^{n-1} 2^i \frac{B_i}{Vdda} \right) \\ &=\; \frac{Vdda}{2^n} \cdot \left(\frac{1}{2} + \sum_{i=0}^{n-1} 2^i\, b_i \right) \\ &=\; \frac{Vdda}{2^n} \cdot \left(\frac{1}{2} + reg \right) \end{aligned} \tag{5.69}$$

where n is the number of bits of the R-2R ladder configuration, b_i the digital register content of bit i (0 or 1) and reg the value of the register itself. The first term of eq. 5.69 is the LSB voltage resolution of the DAC. The factor $\frac{1}{2}$ inside the brackets counts for the half LSB voltage offset error (V_{offset}) which is inherent to a R-2R ladder design[37]. For the given *Beetle* parameters ($n = 8$ and $Vdda = 2.5$ V) the offset is calculated to $V_{\text{offset}} = 4.88$ mV.

Each voltage DAC of the *Beetle* consists of 28 identical resistors. These are made of non-silicided[38] polysilicon with a resistance of $R = 8.45\,\text{k}\Omega$ each. The relative large process variations of polysilicon resistors results in a maximum error of $\Delta R = 0.73\,\text{k}\Omega$ from chip to chip. A larger resistance R would be advantageous by reducing the power consumption and improving the DNL. Otherwise the noise voltage output is $\sqrt{4kTR\Delta f}$ which would increase for higher resistance values. Additionally, for this voltage DAC design the power consumption is more important than the analogue noise behaviour, which is not a critical parameter here.

To calculate the effects of the resistance on the DNL, the impedance of the inverter switches must be taken into account. This resistance is in series with the 2R branch of the R-2R ladder and causes an imbalance in the ladder network. The resistance of the inverter, operating in the ohmic region, is given by

$$R_{\text{FET}} = \frac{V_{\text{ds}}}{I_{\text{d}}} \approx \frac{1}{K'(V_{\text{gs}} - V_{\text{th}})} \cdot \frac{L}{W} \tag{5.70}$$

where $V_{\text{ds}} \leq V_{\text{gs}} - V_{\text{th}}$. The process transconductance parameter $K^{'}$ is given by

$$K^{'} = \mu \cdot C_{\text{ox}} \tag{5.71}$$

[35] For device matching purposes only multiples of R are used.
[36] Ideal inverter means in this case that the output impedance is zero.
[37] Node V_{out} is the output of a voltage divider resistor network formed by the last two resistors in the ladder.
[38] A silicide is a compound that has silicon with more electro-positive elements, e.g. electrically conductive isolated silicon atoms (Cu_5Si or Fe_3Si), non-conductive isolated silicon atoms (Ge_2Si, Sn_2Si or Ni_2Si) or open three-dimensional Si skeletons ($SrSi_2$ or $ThSi_2$).

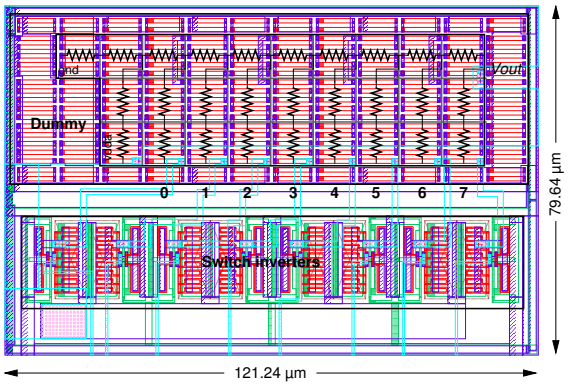


Figure 5.52: Layout of the analogue core of a 8-bit R-2R voltage DAC.

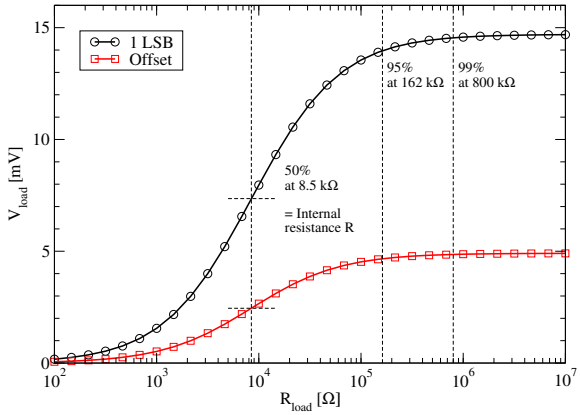


Figure 5.53: Voltage DAC output V_{out} vs. R_{load} for two register settings `0x00` (offset) and `0x01` (only 1 LSB).

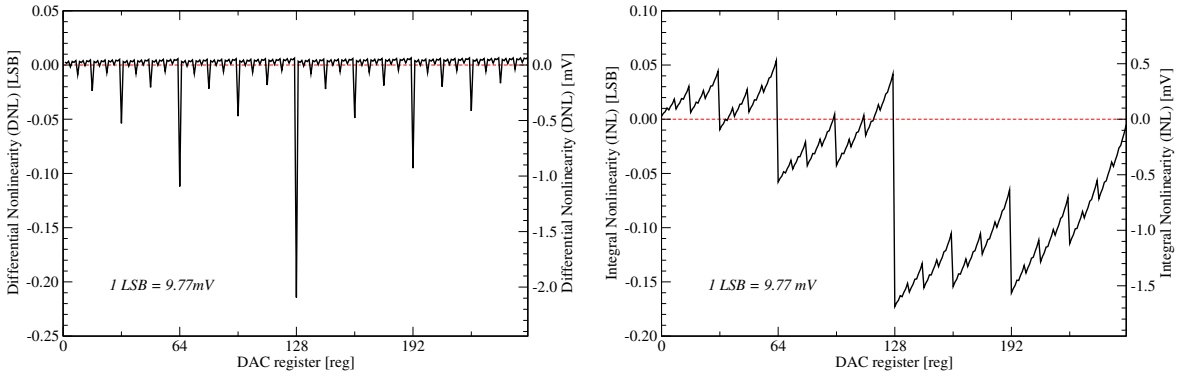
where C_{ox} is the oxide capacitance and μ is the mobility factor.

In general the output impedances of NMOS and PMOS transistors with same $\frac{W}{L}$ ratio are different due to different mobility factors. The electron mobility μ_{n} is two to three times larger than the hole mobility μ_{p}. This difference is compensated by a larger $\frac{W}{L}$ of the PMOS transistor compared to the NMOS device. The chosen values for the PMOS inverter switch transistor are $\frac{W}{L} = \frac{63.28}{0.28}$ and $\frac{30.46}{0.28}$ for the NMOS transistor. This leads to a resistance of both devices of approximately 160 to 180 Ω (2% of R). A compensation of the switch resistance is achieved by using the interconnect line resistance and slightly increased resistors in the single R legs of the R-2R ladder.

The layout of the voltage DAC and its floor plan description is shown in fig. 5.52. The corresponding digital DAC register is not shown here. The 28 identical polysilicon resistors `R` are placed in a common centroid configuration. Each resistor `R` is composed of 5 sub-resistors in series. Dummy resistors enclose the active resistor part to reduce geometric fringe effects. The 8 inverter switches are placed next to the resistor block. The numbers in the layout indicate the corresponding bit numbers of the R-2R ladder configuration.

The output voltage V_{out} vs. the resistive load R_{load} is plotted in fig. 5.53 for two different register settings. For a register setting of `0x00` the output of the DAC only shows the offset voltage. For a setting of `0x01` the sum of one LSB output voltage plus the offset voltage is plotted. The value of V_{out} when $R_{\text{load}} = \infty$ is normalised to 100%. With loads greater than 162 kΩ (800 kΩ) the variation of V_{out} is less than 5% (1%). The value of the load resistance that gives $\frac{V_{\text{out},\infty}}{2}$ (or 50%) is defined as the DC output resistance. It is obvious that the DC output resistance is equal to the resistance R of the R-2R ladder (8.45 kΩ).

The simulated Differential Nonlinearity (DNL) and the Integral Nonlinearity (INL) of the voltage DAC as a function of the binary input number is shown in fig. 5.54(a) resp. fig. 5.54(b). All results are quoted in units of LSB (1 LSB = 9.77 mV) and as absolute voltages. The intrinsic DNL is simulated to be less than ±0.22 LSB and the INL is calculated to be less than ±0.18 LSB. Both values fulfil the intrinsic nonlinearity requirement of ≤ ±0.5 LSB.



(a) Differential Nonlinearity (DNL) (b) Integral Nonlinearity (INL)

Figure 5.54: Simulation of the voltage DAC linearity. The Differential Nonlinearity (a) and the Integral Nonlinearity (b) are depicted. One LSB of the voltage DAC corresponds to 9.77 mV.

5.13 Decoupling Capacitor

In the design of the *Beetle*, critical and noisy power supply lines (e.g. digital control logic) are connected to decoupling capacitors to filter out current spikes. Since decoupling capacitors are connected directly between the power supply net *Vdd* and the ground net *Gnd*, an oxide defect can result in a direct short between *Vdd* and ground. In case of this defect, in theory the current is only limited by the series resistance of the power and ground nets. The resulting currents can lead to chip failure due to electromigration in the power and ground wiring or simply to failure through reduction of the local *Vdd* voltage. Therefore a special decoupling capacitor cell employing several safety features is used to minimise possible defects.

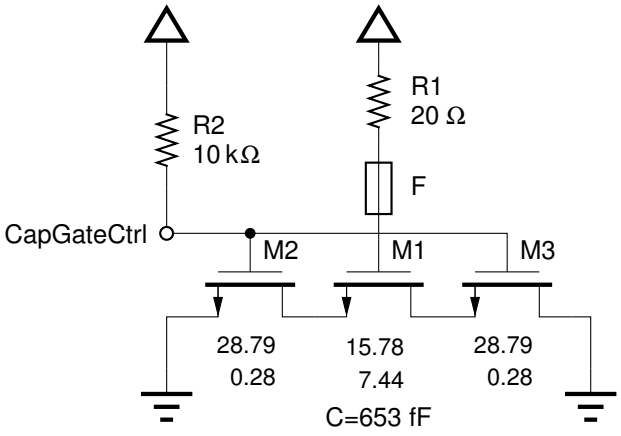


Figure 5.55: Schematic of a decoupling capacitor cell.

The schematic of the decoupling capacitor and the fail-safe circuit is shown in fig. 5.55. Figure 5.56 depicts the corresponding layout. Here, the gate capacitance of an NFET-in-n-well transistor (`M1`) is used as the decoupling capacitor. With nominal process parameters the capacitance of this cell is $C \approx C_{\text{ox}} \cdot W \cdot L = 653\,\text{fF}$ and the decoupling capacitor will roll off beyond 2 GHz. To increase the reliability, the circuit is designed with a fuse. It will be

blown if an excessive amount of current is drawn due to oxide defects or a Single Event Gate Rupture (SEGR) (cf. section 4.3.2). The fuse `F` in the layout consists of a minimum first level metal line (M1) connected to polysilicon (PC) through a minimum stud contact (CA). It is designed to be instantaneously blown when a constant current of about $20 - 30\,\mathrm{mA}$ passes through it. In the event that the fuse does not open, it would later become open as a result of electromigration, long before other lines in the power supply network are affected.

The decoupling capacitor evaluated here includes also two NMOS control devices (`M2` and `M3`) in series with the decoupling capacitor `M1`. Both transistors limit the possible leakage current to values in the range of 30 to 40 mA per defect and cell. The power nets of the *Beetle* chip are designed to tolerate the maximum DC current from approximate 10 defective capacitor cells. So the *Beetle* is insensitive to decoupling capacitor defects even if the fuse mechanism does not open. Intensive stress tests with the *Beetle* have never revealed a failure of the decoupling cells and a switch-off control logic has not been implemented into the *Beetle* chip[39]. Instead the series NMOS transistors `M2` and `M3` are always conductive as the common control node *CapGateCtrl* is connected to *Vdd* via the $10\,\mathrm{k}\Omega$ resistor `R2`. The complete decoupling capacitor is enclosed by a guard ring to provide a low-impedance connection to the local substrate. This will prevent the creation of Silicon Controlled Rectifier (SCR) structures (cf. section 4.3) and hence the triggering of a Single Event Latch-up (SEL).

1375 decoupling capacitors are distributed across the *Beetle* chip providing a total on chip blocking capacitance of 0.9 nF covering a chip area of $\approx 0.5\,\mathrm{mm}^2$.

[39] Special circuits can be designed that monitor the voltage on the drain of the series NMOS transistors. The failed individual decoupling capacitor is disconnected via the control node *CapGateCtrl*.

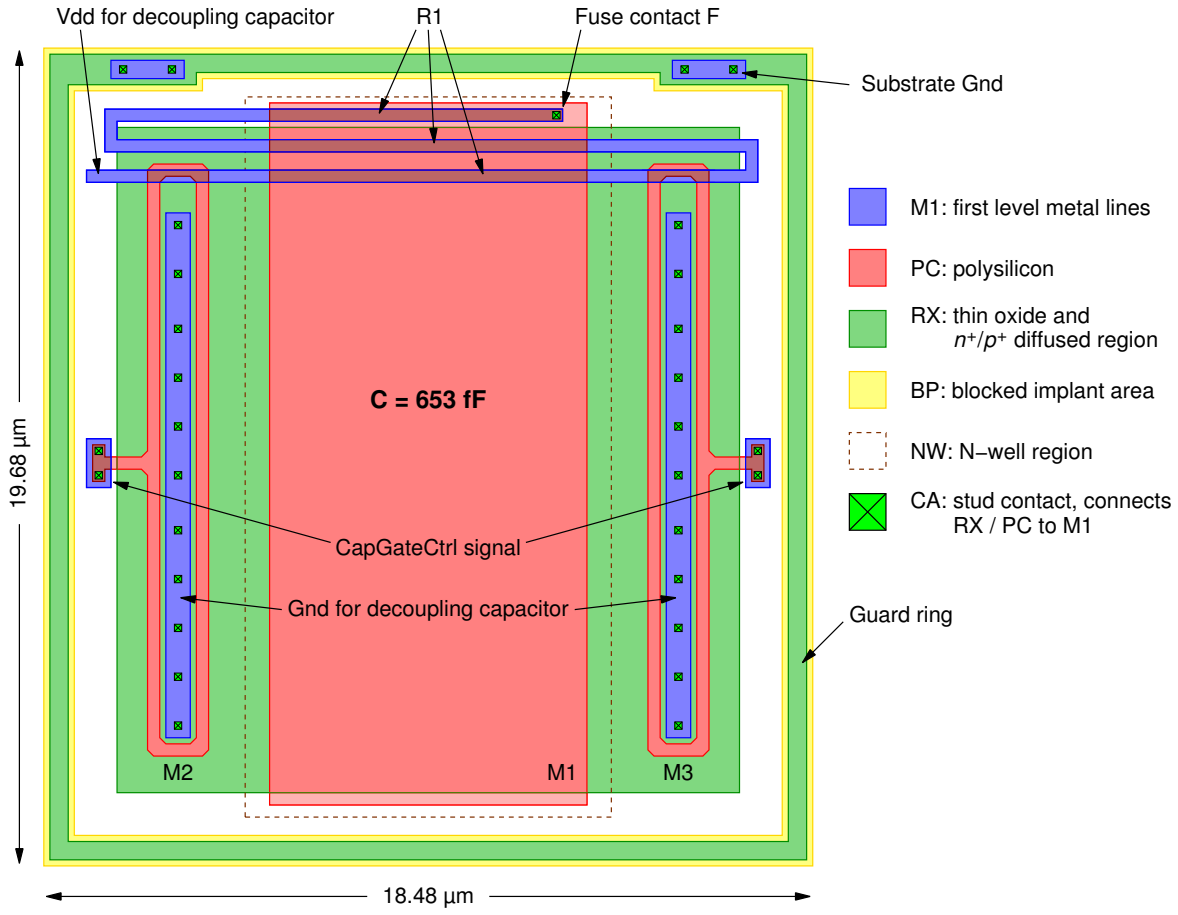


Figure 5.56: Layout of a decoupling capacitor cell. As decoupling capacitor the gate capacitance of an NFET-in-n-well transistor (`M1`) is used. A security mechanism is implemented into the design to prevent a power short-circuit in case of a defect gate oxide.

Chapter 6

Chip Characterisation and Measurement Results

A further important task of the thesis was the detailed characterisation of the *Beetle* chip. This chapter begins with the explanation of the test setup environment that was used in the laboratory. Moreover, the characterisation of the front-end (section 6.2), the complete readout chip (section 6.3) and the results of some important internal test nodes (section 6.4) are presented. A close investigation of process variations is given in the next section. Furthermore, several irradiation tests with *Beetle* chips were performed. The results of the total dose tests are shown in section 6.6. The setup and outcome of an Single Event Upset (SEU) test is presented in the following section. A long-time measurement with a silicon strip detector read out by *Beetle* chips is summarised in section 6.8. At the end of the chapter the first mass production test setup is described and first results from the routine tests are shown.

All results are obtained with *Beetle1.3* chips and confirmed quantitative for the later chip version *1.4* and *1.5*, exceptions are marked. Differences in characterisation due to special chip version features are mentioned in detail.

6.1 Experimental Test Setup

An overview of the experimental test environment is shown in fig. 6.1. All digital signals like `Clock`, `Trigger`, `Reset` and `Testpulse` as well as the voltage step signal V_{ext} of a charge injection circuit (cf. fig. 6.2) are generated by a pattern generator DG2020A from Tektronix [TEK]. The output frequency of the clock signal is set to 40 MHz, which corresponds to the nominal LHC bunch-crossing frequency. The jitter of each output signal is less than $50\,\text{ps}_{\text{p-p}}$. Further on, all outputs can be shifted in steps of 6.25 ns against the clock signal. For V_{ext} an additional delay with a maximum of 20 ns in steps of 0.1 ns can be applied. The pattern generator allows to program the upper and lower signal level of V_{ext} between $-7\,\text{V}$ and $+7\,\text{V}$ with a minimum difference of 0.5 V and a maximum of 9.0 V. The DG2020A is connected to a Personal Computer (PC) via the General Purpose Interface Bus (GPIB). The control of the DG2020A and the programming of different output sequences is done with a graphical user interface, written in LabVIEW (Laboratory Virtual Instrument Engineering Workbench) [NAT].

An experimental test board setup has been developed for the measurements of the *Beetle* readout chips in the laboratory. The setup is a combination of two different boards, which are shown in fig. 6.3.

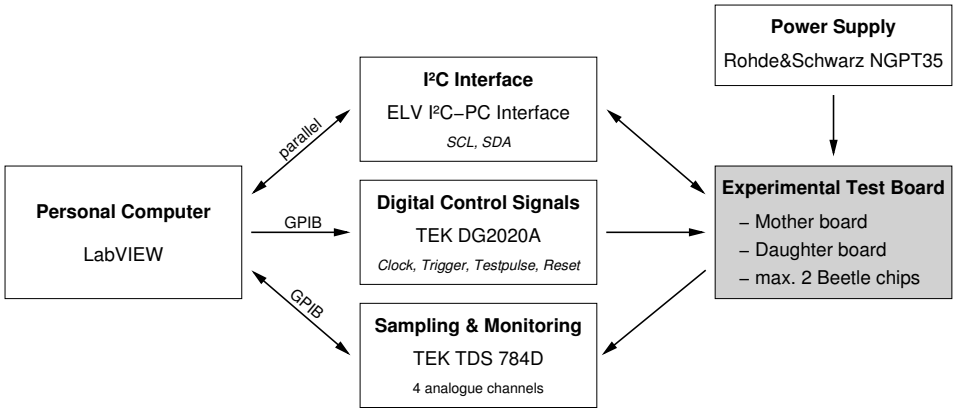


Figure 6.1: Overview of the experimental test setup: A Personal Computer with a graphical user interface (LabVIEW) controls the programming and the readout of the *Beetle* chips. The PC drives the ELV I^2C-interface (configuration register setup) and controls pattern generator (digital control signals) and oscilloscope (signal sampling & monitoring) via GPIB.

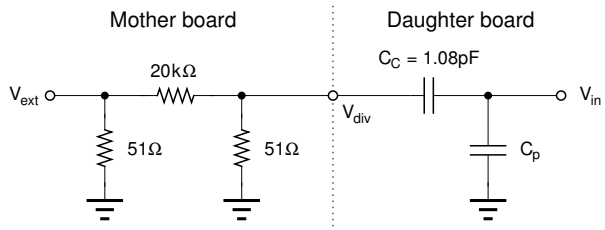


Figure 6.2: Charge injection circuit on the test board. The input signal V_{ext} is generated from a digital pattern generator DG2020A [TEK]. V_{in} is connected to the input of the *Beetle* preamplifier. The terminating resistor as well as the resistive divider is located on the mother board. To minimise the line capacitance of the routing, the coupling and load capacitances are placed very close to the inputs of the *Beetle* chips on the daughter board.

The first board is the so-called *daughter board*. It is a two-layer, gold-plated Printed Circuit Board (PCB)[1] which is designed to carry two *Beetle* chips. The size of the board is 6.4 cm × 6.6 cm with a minimum line width and a minimum gap between two lines of 57.5 µm. For bonding purposes the surface of the narrow lines has to be very flat. The *Beetle* chips are mounted with a two-component epoxy glue EPO-TEK H20S from Polytec [Poly] to the PCB. All 247 pads[2] are bonded to the board, except for the 128 analogue input pads due to geometry. Therefore the daughter board allows only a charge injection into maximum 12 out of the 128 channels. A photography of a bonded chip on a daughter board is presented in fig. 6.4.

The detailed schematic of the charge injection input circuit is shown in fig. 6.2. The injected output charge of this circuit is given by

$$Q_{\text{in}} = \frac{V_{\text{ext}}}{2} \cdot \frac{51}{20\,000} \cdot C_{\text{C}} \tag{6.1}$$

where V_{ext} is the output signal of the pattern generator. A voltage step of 2.6 V at V_{ext} and a standard capacitance of 1.08 pF at C_{C} results in an injected charge Q_{in} of 22 345 e^-. This

[1] The daughter board is produced by Häfele Leiterplattentechnik e.K.[HÄF].
[2] 248 pads are implemented on a *Beetle1.5*.

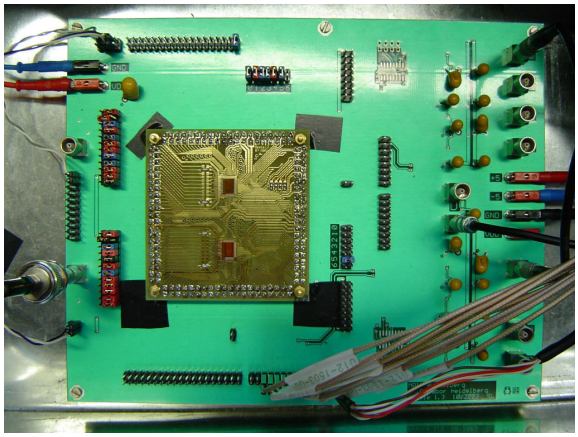


Figure 6.3: Picture of the experimental test boards. The *Beetle* chips are glued on a small PCB (*daughter board*) which is plugged on a *mother board*. The second board carries the analogue output receivers as well as level shifters and identification jumpers for the I^2C-interfaces.

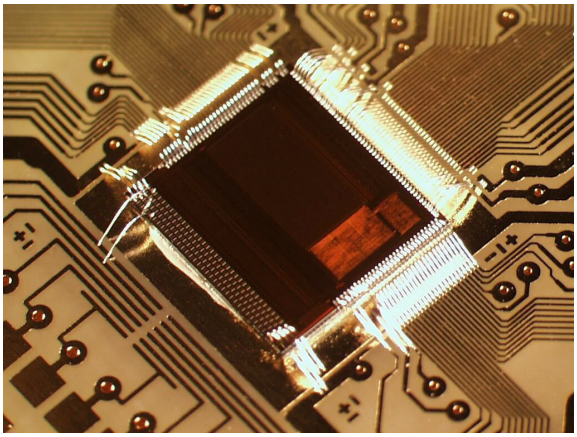


Figure 6.4: *Beetle* chip glued and bonded to the daughter board. All pads (power, communication, blocking, comparator, test structures) except for the analogue input pads are bonded. In this picture only the pads `TestInput` and `AnalogIn<12>` are connected at the input side of the chip.

input charge corresponds roughly to 1 MIP[3]. If not quoted specially in the text, this value is the standard charge for an external input signal.

In accordance to equation 6.1 the possible charge range of the input circuit is given from 4 297 e^- to 77 351 e^-. Other input charges can be generated but require the exchange of the coupling capacitance C_C on the daughter board. Furthermore, the board contains blocking components for power supply lines as well as load capacitance C_p.

The daughter board itself is mounted on a second PCB, the so-called *mother board*. It is also a two-layer board with dimensions of 19.7 cm × 15.7 cm. This board integrates 8 analogue receiver circuits [AD01] to convert the differential current outputs of the *Beetle* to a single-ended voltage signal. The differential output `DataValid` is translated with an LVDS receiver [NSC03] to a single-ended signal. Furthermore, the board contains different jumpers to define two unique I^2C chip addresses for both *Beetle* chips. The mother board allows to individually switch on or off the charge injection for each of the 12 possible input channels of a chip. A level shifter circuit that converts the I^2C-bus [Phi95, Phi97] from 5 V signals to the *Beetle* operation voltage of 2.5 V is implemented on the mother board[4]. Schematic, layout and pin-description of the test boards are attached in *The Beetle Reference Manual* in appendix C.

The output of the analogue receivers on the mother board are connected to a four-channel oscilloscope (Tektronix TDS 784D) for sampling and digitising the data. In case of a triggered readout, all four analogue receiver outputs are sampled in parallel and stored into the memory of the scope for up to 250 µs with a step size of 500 ps per sample. After the readout is finished, the stored readout information is transferred via the GPIB interface to the PC.

The internal registers of the *Beetle* chips are programmed via a computer driven I^2C-interface from ELV [ELV], which is connected to the parallel port of the PC. The imple-

[3] 1 Minimum Ionising Particle (MIP) deposits approximately 22 000 electrons in 300 µm silicon.

[4] This feature is not needed for chips of version *1.3* and newer. These chips feature 5 V tolerant I^2C-pads.

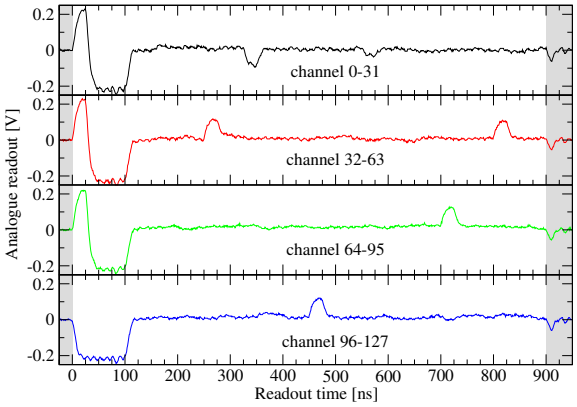


Figure 6.5: Analogue readout sequence of the *Beetle* chip. 128 channels carried on four ports in parallel. The complete readout takes 900 ns at the nominal clock frequency of 40 MHz. 5 internal and one external test pulse signal have been applied to the chip. The grey marked area shows the output signals before and after the readout sequence.

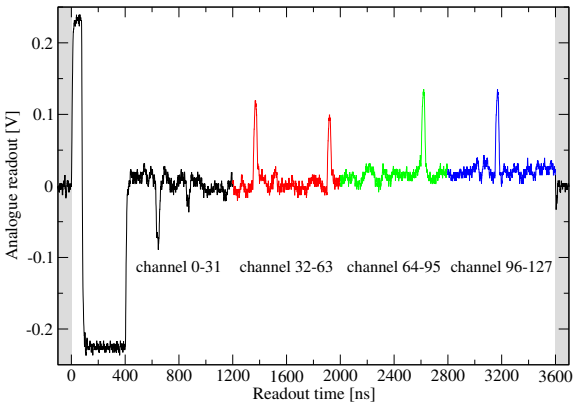


Figure 6.6: Analogue readout sequence of the *Beetle* chip. 128 channels carried on one port. This readout mode is implemented for the purpose in the laboratory. Here, the complete readout takes 3 600 ns. The test signals are applied to the same input channels as in fig. 6.5.

mentation of the interface, the development of driver software as well as the Graphical User Interface (GUI) are also a part of this thesis. For the parallel port communication to the I^2C-interface, the basic code segments are shown in appendix B.

According to the LHCb front-end electronic specifications (cf. table 2.6), all 128 channels of the *Beetle* have to be read out at a frequency of 40 MHz and within 900 ns. An example is recorded in fig. 6.5. At the beginning of the readout the status information of the *Beetle* chip and of the triggered event are transmitted via four output ports off chip. This information part is also identified as the *analogue readout header*. The readout of this header is completed after 100 ns. Within the next 800 ns, all 128 channels are read out. Therefore the channels are split into 4 groups of 32 channels. Each group is then carried by one of the four output ports. In total, 6 test signals were applied to the front-end of the chip and are observed in the readout of the *Beetle* (cf. fig. 6.5).

A special readout mode is implemented into the *Beetle* for applications, where readout speed is less important. In this mode all four output ports are multiplexed on one single readout port. This reduces the number of external devices. On the other hand the readout of the analogue data takes four times longer (3.6 µs). In fig. 6.6 the readout of the same test signals as before is presented in the one port readout mode. The readout starts again with the analogue header followed by the 128 analogue channels. The different groups of the 4 port readout mode from the previous readout figure 6.5 are marked with the same colour in figure 6.6.

6.2 Front-end Amplifier

Intense research was put into the development of the *Beetle* front-end amplifier. This section summarizes the behaviour of the front-end for different operation settings. First of all, the parameters used for the characterisation of the front-end are explained in detail.

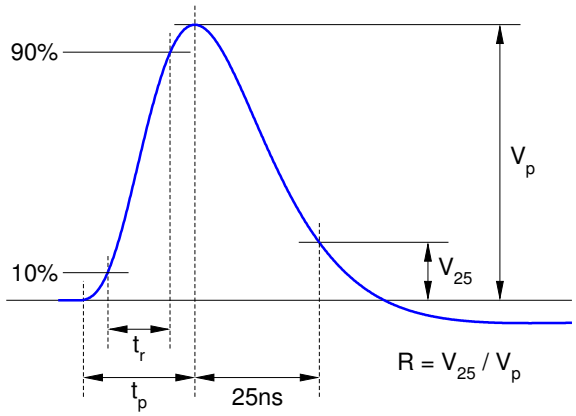


Figure 6.7: Semi-Gaussian pulse of a front-end with the corresponding parameters characterising the output shape.

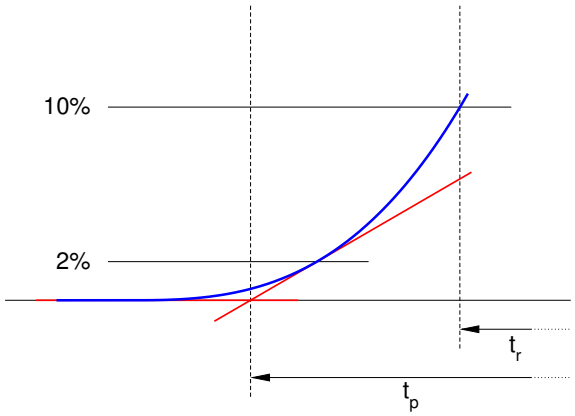


Figure 6.8: Identification of the pulse shape starting point for the peaking time measurement t_p.

Figure 6.7 shows a typical front-end output pulse with the corresponding parameters: rise time t_r $(10-90\%)$, peaking time t_p $(0-100\%)$, peaking voltage V_p and remainder R. The remainder is defined as the ratio between output signal voltage (25 ns after the peak) and peaking voltage V_p. Within this thesis the starting point of the pulse shape is defined as the intersection of the tangent taken at 2% of V_p with the baseline, as shown in fig. 6.8.

6.2.1 Pulse Shape Scan

The analogue output shapes of all 128 front-end channels are sampled in parallel every 25 ns into the pipeline (cf. section 5.7). Therefore, the output shapes are not directly measurable[5] and instead only the output signal at a certain point in time can be seen at the analogue output of the chip. However, with a more involved method the transfer curve can be reconstructed – the so called *pulse shape scan*. Here, the output response of the front-end is stored at the positive edge of the sampling clock into the pipeline, which is an analogue switched capacitor array of 130×187 cells. With a readout trigger the pipeline value is read out via an amplifier (pipeamp), a multiplexer and an analogue current output driver. The complete pulse shape is recorded by shifting the input signal with respect to the sampling clock in steps of 500 ps. For each step the average of 50 data samples is taken.

All scans are done at an average environmental temperature of the test setup between 40°C and 45°C. According to fig. 6.20, respectively equation 6.9, this corresponds to a chip temperature of 75°C to 79°C.

The output behaviour of the *Beetle* front-end can be adjusted by 3 currents and 2 voltages (cf. 5.4), all generated internally on chip. The nominal values of these front-end parameters are listed in table 6.1. All other chip parameters, that do not directly influence the behaviour of the front-end output, are explained in table C.14 of *The Beetle Reference Manual* in appendix C.

[5] Except for the *Test Channel*. There the output is routed directly off chip as a test feature.

Parameter	Description	Nominal Setting
Ipre	Preamplifier bias current	600 µA
Isha	Shaper bias current	80 µA
Ibuf	Buffer bias current	80 µA
Vfp	Preamplifier feedback voltage	0 mV
Vfs	Shaper feedback voltage	0 mV

Table 6.1: Output adjustment parameters of the front-end.

Front-end Settings

The front-end outputs, obtained from a pulse shape scan of an external input signal, are shown in fig. 6.9. Here, the gate voltage *Vfs* of the shaper feedback FET is set to 4 different values, resulting in a variation of the feedback resistances R_{fb}. This influences the large time constant $R_{\mathrm{fb}}C_{\mathrm{fb}}$ of the shaper feedback and determines the continuous reset of the integrator. The injected charge of the test signal is $Q_{\mathrm{in}} = 22\,345\,\mathrm{e}^- \pm 207\,\mathrm{e}^-$ for all measurements and the capacitive detector input load is $C_{\mathrm{p}} = 3\,\mathrm{pF}$. No absolute numbers can be given for the front-end peaking voltage V_{p} because of several other amplification factors in the readout path (e.g. pipeline amplifier, analogue current output driver, external receiver circuit, etc.). Instead all V_{p} measurements and front-end output signals are normalised to the peaking value of $Vfs = 0\,\mathrm{mV}$. An overview of all extracted parameters for this measurement is summarised in table 6.2. For all settings of $Vfs < 800\,\mathrm{mV}$ the peaking time t_{p} is less than the required 25 ns from the LHCb front-end specifications [Sch01]. Also the signal remainder R 25 ns after the pulse peak is in the limit of less than 30% for $Vfs < 800\,\mathrm{mV}$.

Vfs [mV]	Peaking time t_{p} [ns]	Rise time t_{r} [ns]	Peaking ratio $V_{\mathrm{p}}/V_{\mathrm{p,Vfs=0V}}$	Remainder [%]
0	21.0 ± 0.5	12.5 ± 0.3	1.00	2.8 ± 1.2
100	21.2 ± 0.5	12.7 ± 0.3	1.01 ± 0.03	4.6 ± 1.5
400	22.3 ± 0.5	13.2 ± 0.3	1.08 ± 0.04	15.8 ± 1.5
1 000	26.3 ± 0.6	15.3 ± 0.3	1.27 ± 0.07	42.9 ± 1.6

Table 6.2: Measured pulse shape parameters for different *Vfs* settings. The capacitive detector input load for all measurements is $C_{\mathrm{p}} = 3\,\mathrm{pF}$. The corresponding plots are shown in fig. 6.9.

Different load capacitance

Beetle chips are operating at LHCb in different subsystems with special requirements to the front-end circuit. A very important point is the different capacitive detector input load the chip has to cope with. Therefore, extensive tests are done to characterise the chip behaviour under these circumstances. Figure 6.10 shows the front-end pulse shape for different detector load capacitances between 3 pF and 51 pF[6]. The chip is programmed to the nominal settings. Especially the shaper feedback is set to $Vfs = 0\,\mathrm{mV}$ for this diagram. In table 6.3 the corre-

[6] The detector load capacitance C_{p} already includes the parasitic capacitance C_{para} of the input bond wire and line routing on the PCB. Estimations and measurements with a capacitance meter showed that a value of 3 pF is a sufficient approximation for C_{para}.

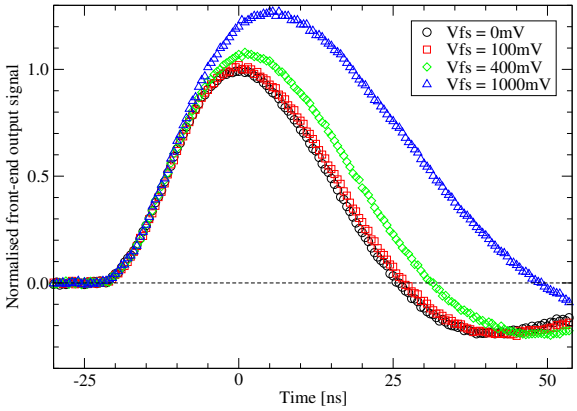


Figure 6.9: Front-end output signal obtained from a pulse shape scan for different shaper feedback settings *Vfs*. The capacitive detector input load for all measurements is $C_\mathrm{p} = 3\,\mathrm{pF}$.

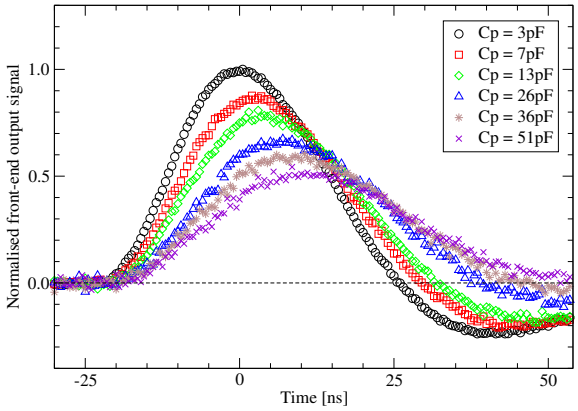


Figure 6.10: Front-end output signal for different load capacitances C_p.

C_p [pF]	Peaking time t_p [ns]	Rise time t_r [ns]	Peaking ratio $V_\mathrm{p}/V_{\mathrm{p,Vfs=0V}}$	Remainder [%]
3.0	21.0 ± 0.5	12.5 ± 0.3	1.00	2.8 ± 1.2
7.0	22.5 ± 0.5	13.8 ± 0.3	0.87 ± 0.3	5.8 ± 1.5
12.9	23.5 ± 0.5	14.7 ± 0.3	0.79 ± 0.3	10.1 ± 1.7
25.7	25.8 ± 0.6	16.3 ± 0.3	0.67 ± 0.4	23.9 ± 1.8
36.3	27.7 ± 0.6	16.8 ± 0.4	0.59 ± 0.4	31.3 ± 2.0
50.5	28.2 ± 0.7	17.7 ± 0.5	0.51 ± 0.5	33.8 ± 2.1

Table 6.3: Measured pulse shape parameters for different detector input load capacitances. All front-end settings are programmed to the nominal values (especially $Vfs = 0\,\mathrm{mV}$). The corresponding pulse shapes are shown in fig. 6.10 for all load capacitances.

sponding pulse shape parameters are listed. Even for capacitive loads of 25 pF, the peaking time is below 25 ns and the remainder stays below 30%.

Figure 6.11 shows the pulse shape parameters peaking time t_p, rise time t_r, signal peaking voltage V_p and remainder R as a function of the detector load capacitance C_p, with *Vfs* as curve parameter. All V_p measurements are normalised to the peaking value of $Vfs = 0\,\mathrm{mV}$ and $C_\mathrm{p} = 3\,\mathrm{pF}$ like before. For all extracted pulse shape parameters the formulas for the best curve fits as a function of C_p are calculated. The expressions are given in equations 6.2 to 6.5 and are valid in good approximation for $1\,\mathrm{pF} \leq C_\mathrm{p} \leq 55\,\mathrm{pF}$.

Comparison of Simulation and Measurement Results

All results in this section are based on measurements, obtained from the test setup with *Beetle* chips described before. To check the quality of the development and simulation, a simulation of the front-end circuit as well as the input circuit of the test board is done. The results from measurements are then compared with the simulations for equal settings. Figure 6.12 shows the outcome of the measurement and two different simulations of the front-end amplifier, operating at nominal settings. For the first simulation, plotted with a dashed line (red), the schematic

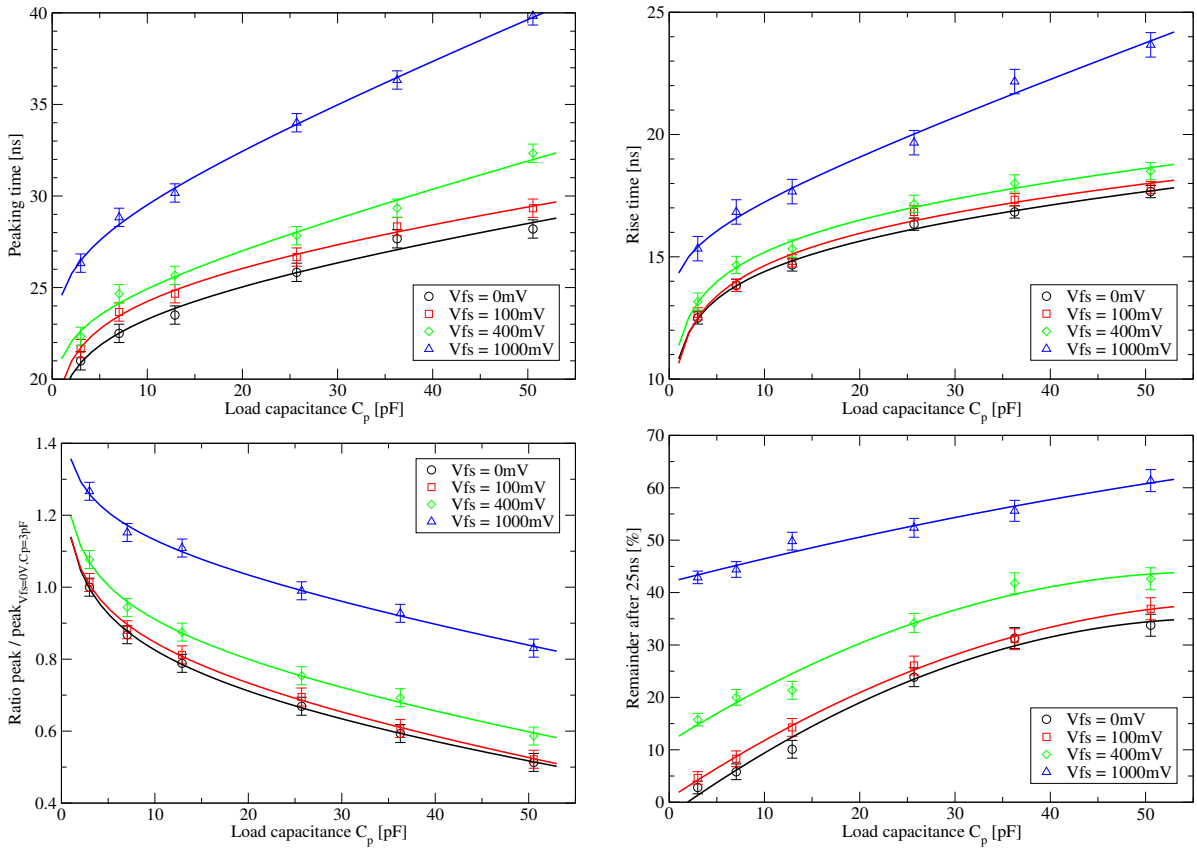


Figure 6.11: Peaking time t_p, rise time t_r, peaking voltage V_p and remainder R of the *Beetle*. All V_p measurements are normalised to the peaking value of $Vfs = 0\,\mathrm{mV}$ and $C_\mathrm{p} = 3\,\mathrm{pF}$. The calculation formulas for the best fits of the extracted parameters are depicted in (6.2) to (6.5).

$$t_{\mathrm{p,fit}}(C_\mathrm{p})[\mathrm{ns}] = \begin{cases} 6.71 \cdot 10^{-2}\, C_\mathrm{p}[\mathrm{pF}] + 1.58\, \ln(C_\mathrm{p}[\mathrm{pF}]) + 18.95 & \text{for } Vfs = 0\,\mathrm{mV} \\ 5.84 \cdot 10^{-2}\, C_\mathrm{p}[\mathrm{pF}] + 1.75\, \ln(C_\mathrm{p}[\mathrm{pF}]) + 19.62 & \text{for } Vfs = 100\,\mathrm{mV} \\ 1.28 \cdot 10^{-1}\, C_\mathrm{p}[\mathrm{pF}] + 1.16\, \ln(C_\mathrm{p}[\mathrm{pF}]) + 20.98 & \text{for } Vfs = 400\,\mathrm{mV} \\ 1.98 \cdot 10^{-1}\, C_\mathrm{p}[\mathrm{pF}] + 1.37\, \ln(C_\mathrm{p}[\mathrm{pF}]) + 24.38 & \text{for } Vfs = 1\,000\,\mathrm{mV} \end{cases} \tag{6.2}$$

$$t_{\mathrm{r,fit}}(C_\mathrm{p})[\mathrm{ns}] = \begin{cases} 2.30 \cdot 10^{-2}\, C_\mathrm{p}[\mathrm{pF}] + 1.46\, \ln(C_\mathrm{p}[\mathrm{pF}]) + 10.80 & \text{for } Vfs = 0\,\mathrm{mV} \\ 1.66 \cdot 10^{-2}\, C_\mathrm{p}[\mathrm{pF}] + 1.67\, \ln(C_\mathrm{p}[\mathrm{pF}]) + 10.63 & \text{for } Vfs = 100\,\mathrm{mV} \\ 2.28 \cdot 10^{-2}\, C_\mathrm{p}[\mathrm{pF}] + 1.57\, \ln(C_\mathrm{p}[\mathrm{pF}]) + 11.35 & \text{for } Vfs = 400\,\mathrm{mV} \\ 1.33 \cdot 10^{-1}\, C_\mathrm{p}[\mathrm{pF}] + 0.74\, \ln(C_\mathrm{p}[\mathrm{pF}]) + 14.21 & \text{for } Vfs = 1\,000\,\mathrm{mV} \end{cases} \tag{6.3}$$

$$V_\mathrm{p}/V_{\mathrm{p,Vfs=0V,fit}}(C_\mathrm{p}) = \begin{cases} -2.61 \cdot 10^{-3}\, C_\mathrm{p}[\mathrm{pF}] - 0.126\, \ln(C_\mathrm{p}[\mathrm{pF}]) + 1.14 & \text{for } Vfs = 0\,\mathrm{mV} \\ -3.46 \cdot 10^{-3}\, C_\mathrm{p}[\mathrm{pF}] - 0.113\, \ln(C_\mathrm{p}[\mathrm{pF}]) + 1.14 & \text{for } Vfs = 100\,\mathrm{mV} \\ -3.31 \cdot 10^{-3}\, C_\mathrm{p}[\mathrm{pF}] - 0.112\, \ln(C_\mathrm{p}[\mathrm{pF}]) + 1.20 & \text{for } Vfs = 400\,\mathrm{mV} \\ -3.99 \cdot 10^{-3}\, C_\mathrm{p}[\mathrm{pF}] - 0.082\, \ln(C_\mathrm{p}[\mathrm{pF}]) + 1.36 & \text{for } Vfs = 1\,000\,\mathrm{mV} \end{cases} \tag{6.4}$$

$$R_{\mathrm{fit}}(C_\mathrm{p})[\%] = \begin{cases} 1.12 \cdot 10^{-2}\, (C_\mathrm{p}[\mathrm{pF}])^2 + 1.30\, C_\mathrm{p}[\mathrm{pF}] - 2.46 & \text{for } Vfs = 0\,\mathrm{mV} \\ 9.70 \cdot 10^{-3}\, (C_\mathrm{p}[\mathrm{pF}])^2 + 1.20\, C_\mathrm{p}[\mathrm{pF}] + 0.70 & \text{for } Vfs = 100\,\mathrm{mV} \\ 1.00 \cdot 10^{-2}\, (C_\mathrm{p}[\mathrm{pF}])^2 + 1.14\, C_\mathrm{p}[\mathrm{pF}] + 11.47 & \text{for } Vfs = 400\,\mathrm{mV} \\ 1.78 \cdot 10^{-3}\, (C_\mathrm{p}[\mathrm{pF}])^2 + 0.46\, C_\mathrm{p}[\mathrm{pF}] + 42.00 & \text{for } Vfs = 1\,000\,\mathrm{mV} \end{cases} \tag{6.5}$$

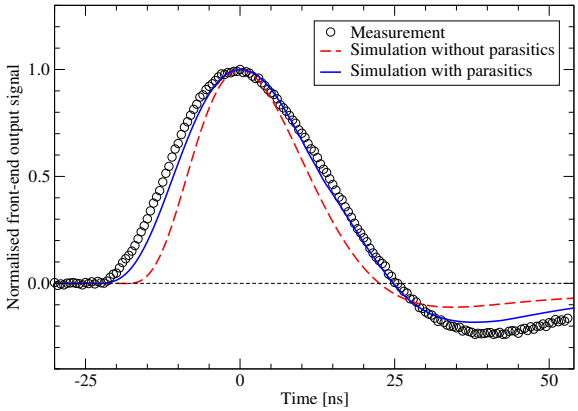


Figure 6.12: Front-end output signal comparison between measurement and simulation for nominal amplifier settings. The simulation plotted with a dashed line (red) shows the front-end circuit behaviour without any parasitic capacitances from the layout. The simulation (blue line) includes the parasitics and the resistive network, both extracted from the final chip layout.

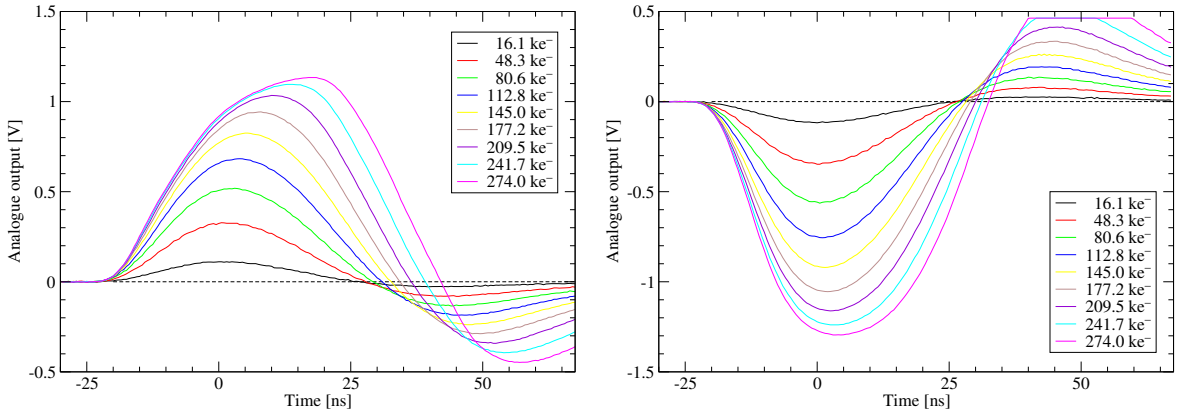
diagram of the front-end as it is implemented on the chip is used. It contains no information about parasitic capacitances or interconnecting lines coupling to neighbouring structures. As can be recognised easily from the drawing, the simulated rise and fall times are much faster than those of the measured pulse shape. Also the undershoot of the simulated pulse shape is much smaller compared to the measured signal.

For the second simulation, marked with a solid line (blue), the circuit also includes parasitic and interconnecting capacitances as well as estimations for the resistance of long routing lines. This detailed simulation can only be done at the end of the design development, when all information from the layout is available. An automatic extension of the simulation network to include parasitic components is not available for the present design kit. For the most critical parts of the front-end, the additional parasitic parameters are manually extracted from the layout or calculated by using the engineering design manual and then added to the simulation circuit. The front-end output shape of the detailed simulation is much closer to the measured pulse shape, but the signal undershoot is still smaller than for the measured shape. Additional parasitic components within the shaper feedback were identified as main contributions to the differences between measurement and simulation.

Change of Sampling Point

As described before the peaking point of the front-end output pulse is well correlated with the detector load capacitance at the input of the chip. This usually doesn't pose any challenge since the external load is constant. Therefore, the sampling clock is once aligned such that the pipeline stores the peak value of the front-end output pulse.

However, the situation is different for varying input charges. As depicted in fig. 6.13, the rise time is getting slower for larger input charges and therefore the peaking point is moving. Because the sampling point is normally fixed, this leads to the consequence that front-end output is not any more sampled at its peak value. This is also the main reason for the divergence of the front-end linearity, described in detail in section 6.3.8. Furthermore, it can be mentioned, that the *Beetle* is developed for handling charges between $-110\,\mathrm{ke}^-$ and $+110\,\mathrm{ke}^-$ in the



(a) Positive Charge (b) Negative Charge

Figure 6.13: Front-end output response from a pulse shape scan for different input charge signals Q_{in}. In the left diagram a positive test pulse signal is injected whereas a negative signal is injected in the right plot. Because of a limitation in the ADC the undershoot of the pulse shape for $Q_{\text{in}} = 241.7\,\text{ke}^-$ and $274.0\,\text{ke}^-$ is not correctly sampled.

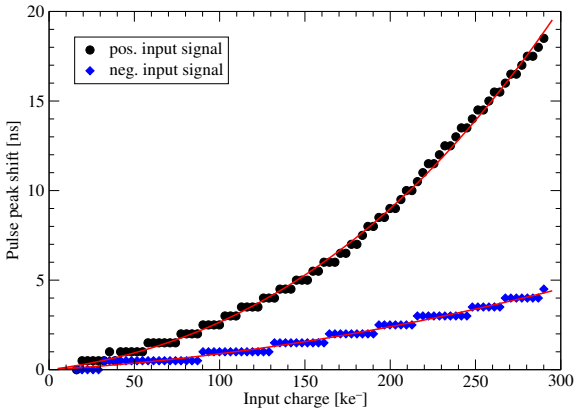


Figure 6.14: Displacement of the pulse maximum for different input charges Q_{in}.

normal operation mode. To point out the issue of the sampling point shift, the range of this measurement is expanded to $\pm 274\,\text{ke}^-$. This leads also to the compression of the pulse shape for very high input charges, because the front-end starts to saturate.

For both pulse polarities the shift of the peaking point is plotted in fig. 6.14. The nominal sampling point ($t = 0$) is set to the peaking point of the pulse shape with an equivalent input charge of $\pm 22\,\text{ke}^-$. The measurement shows an obvious difference between both polarities which can also be seen in simulations of the front-end circuit.

For a readout system with a fixed sampling clock to an input signal with a charge of $22\,\text{ke}^-$, a positive pulse of an equivalent charge of $110\,\text{ke}^-$ results in a peaking point shift of already 3 ns. This leads to the effect that the front-end output is sampled 3 ns seconds before the actual peaking point is reached, which corresponds to 98.13% of the maximum signal. Table 6.4 summarises the extracted parameters for 6 different input charges.

Pulse shape	Input charge	Peaking shift	Proportion of max. signal peak
positive	110 ke$^-$	3.0 ns	98.13%
positive	220 ke$^-$	11.0 ns	86.66%
positive	290 ke$^-$	18.5 ns	82.78%
negative	110 ke$^-$	1.0 ns	99.26%
negative	220 ke$^-$	3.0 ns	98.54%
negative	290 ke$^-$	4.5 ns	97.99%

Table 6.4: Peaking point shift of a front-end output pulse for different input charges compared to a fixed sampling point. The last column quotes the fraction of the signal peak obtained by sampling at a fixed point in time the peaking value of a 22 ke$^-$ pulse.

6.2.2 Input Charge Rate

The behaviour of the *Beetle* front-end is measured for different input charge rates. This is realised in the test setup by a constant DC current that is applied to the input V_{in} of the front-end. An input signal with a defined charge is superimposed to the DC current during the measurement. The ratio of the front-end's output with and without the DC current is calculated and plotted in fig. 6.15. The measurement is done for a positive current[7], which is equivalent to a positive input charge, that is flowing into the front-end of fig. 6.15(a). Figure 6.15(b) shows the same measurement with a negative input current, which is defined as a current that is flowing out of the chip or respectively a negative charge to the front-end input.

The maximum charge rate of the *Beetle* is defined as the value at which the front-end output degradation is 10% of the nominal signal output level. In the measurement setup this corresponds to a level of 90%, which is marked in both diagrams with a dashed red line. This results to a maximum charge rate of

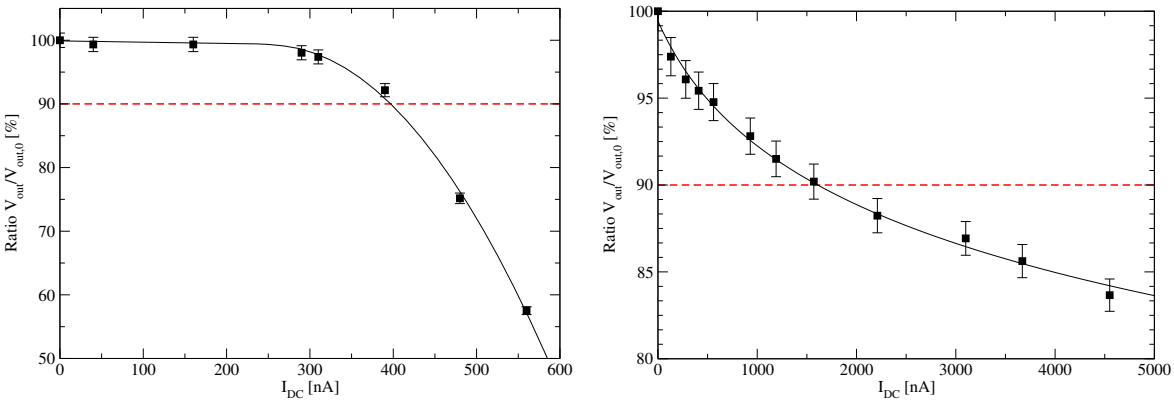
$$\dot{Q}_{\text{max}} = I_{\text{max}} = \begin{cases} 397 \ {}^{+7}_{-8} \text{ nA} & \text{for currents into the front-end } \textit{or} \text{ pos. charge} \\ 1\,609 \ {}^{+165}_{-153} \text{ nA} & \text{for currents out of the front-end } \textit{or} \text{ neg. charge} \end{cases} \tag{6.6}$$

for the front-end of a *Beetle* chip. The equivalent input charge Q_{in} at the front-end is determined from a DC input current via

$$Q_{\text{in}} = \frac{I}{f_{\text{BX}} \cdot O_{\text{CC}}} \tag{6.7}$$

with:
- Q_{in} – input charge of the analogue front-end,
- f_{BX} – bunch crossing frequency of LHC (= 40.08 MHz),
- O_{CC} – input channel strip occupancy [in %][8].

Assuming a worst case situation of 100% strip occupancy and positive charged signals, the maximum input charge according to eq. 6.7 is still 61.8 ke$^-$. For larger input charges at this high occupancy level the output degradation exceeds 10%.



(a) Positive Charge (b) Negative Charge

Figure 6.15: Front-end output behaviour as a function of different DC input currents. For all measurements a signal with a defined charge of 22 345 e^- is coupled externally into the chip. The signal ratio of the front-end output voltage with a certain DC input current (V_{out}) and without a DC current ($V_{out,0}$) is plotted on the ordinate. In diagram (a) the DC current is flowing into the front-end which corresponds to a positive charge at the front-end. Whereas on the right diagram (b) the current is flowing out of the chip which is equal to a negative charge at the front-end input.

6.2.3 Temperature Behaviour

In the final application, the *Beetle* will be used in different temperature domains. Therefore, the front-end behaviour at different temperatures is described in this section together with a brief overview of the test environment. Additional temperature test concerning all components of the *Beetle* chip (e.g. start-up, long-term operating, temperature stress tests) are discussed in section 6.3.4.

The measurement of the front-end pulse shape is performed for a constant detector load capacitance C_p of 3 pF. In a climatic exposure test cabinet the PCB with the mounted *Beetle* chips are operated at a defined environmental temperature between −44℃ and +75℃. A temperature sensitive device (PT100) is glued directly on top of the chip to measure the surface temperature of the *Beetle*. According to eq. 6.9, the ambient temperatures correspond to chip temperatures between −4℃ and +107℃.

The pulse shape parameters peaking time t_p, rise time t_r, signal peaking voltage V_p and remainder R for different feedback shaper settings *Vfs* are plotted in fig. 6.16 as a function of the chip surface temperature $T_{surface}$. All V_p measurements are normalised to the peaking value of $Vfs = 0$ mV and $T_{surface} = 60.7$℃, which is equal to an ambient temperature of 25℃.

For lower temperatures the rising of the pulse shape is faster (peaking and rise time decreases) as well as the falling of the pulse, which corresponds to a decrease of the signal remainder. Also the peak voltage is higher at lower temperatures.

[7] Definition of conventional electric current: positive current flows from positive to negative voltage drop.
[8] In case of the VELO the strip occupancy is roughly constant and below 0.5% [Muh01].

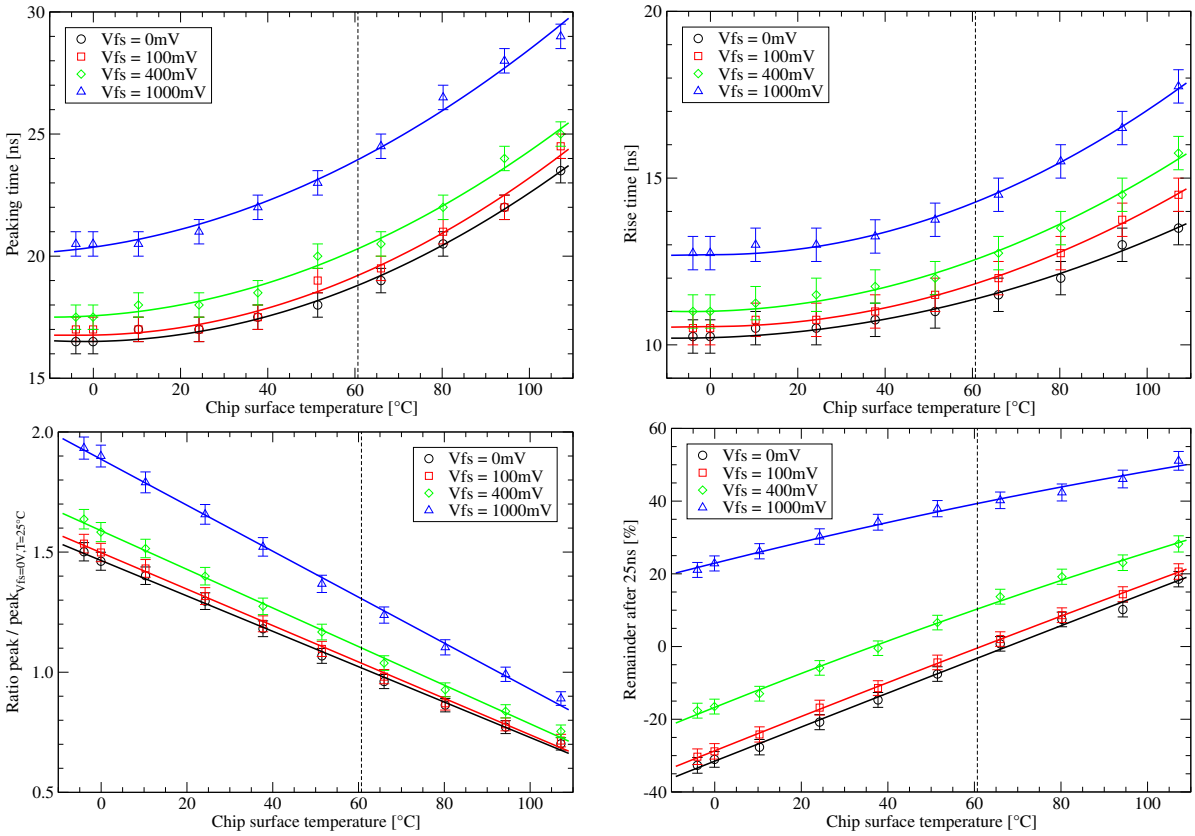


Figure 6.16: Peaking time t_p, rise time t_r, peaking voltage V_p and remainder R as a function of the chip temperature T. All V_p measurements are normalised to the peaking value of $Vfs = 0\,\text{mV}$ and an ambient temperature of $T = 25°\text{C}$, which is marked with a dashed line in all diagrams.

6.3 Complete Readout Chip

This section presents the measurement results obtained from the complete readout chip. If not especially indicated, all results were measured with a *Beetle1.3* chip and are also valid for the later chip versions *1.4* and *1.5*.

At first the power consumption of a *Beetle* and the behaviour due to variation of the power supply voltage is shown in section 6.3.1 and 6.3.2. Different functional and stress tests are summarised in section 6.3.3 to 6.3.5, followed by measurements of the analogue chip part (section 6.3.6 to 6.3.10). Finally the results of the important accessible internal test nodes are shown in section 6.4.

6.3.1 Power Consumption

An important aspect is the total power consumption of a *Beetle* chip. It is limited by the cooling capability of the VELO, where the *Beetle* operates in the secondary vacuum. Current estimates result in a required cooling capacity of 3.5 kW for the all 84 Level-0 boards [Chr05]. In detail 0.7 kW is calculated for the linear regulators and the signal repeaters require 1.4 kW.

Chip configuration			I_{supply} [mA]		P [mW/ch]	
Clock 40 MHz	Trigger 1.1 MHz	Registers	analogue readout ports			
			1	4	1	4
no	**no**	**0**	$\mathbf{24.5 \pm 0.5}$	$\mathbf{24.5 \pm 0.5}$	$\mathbf{0.48 \pm 0.01}$	$\mathbf{0.48 \pm 0.01}$
yes	no	0	64.5 ± 1.5	64.5 ± 1.5	1.26 ± 0.03	1.26 ± 0.03
yes	yes	0	64.5 ± 1.5	64.5 ± 1.5	1.26 ± 0.03	1.26 ± 0.03
no	no	nom.	192.0 ± 2.0	221.5 ± 2.0	3.75 ± 0.04	4.33 ± 0.04
yes	no	nom.	232.0 ± 2.0	261.5 ± 2.0	4.53 ± 0.04	5.11 ± 0.04
yes	**yes**	**nom.**	$\mathbf{237.0 \pm 2.0}$	$\mathbf{267.0 \pm 2.0}$	$\mathbf{4.63 \pm 0.04}$	$\mathbf{5.21 \pm 0.04}$

Table 6.5: Typical power consumption figures for different chip configurations and two different readout modes (readout of all signals via 1 respectively 4 analogue output ports). The comparator circuit and the LVDS output drivers are not powered in any of the given configurations, because they are not used in the standard mode of operation. The nominal register settings are specified in detail in table C.14.

Another 1.4 kW is reserved for the complete front-end electronic, which results in a maximum power consumption of approximately 1 W per chip (or 7.8 mW per readout channel).

In table 6.5 the typical power consumptions for different chip configurations are given. After a power-up reset is applied to the chip and no clock or trigger signals are transmitted, the basic power consumption is measured with 0.48 mW per channel. At nominal LHCb readout configuration[9] the power consumption increases to 5.21 mW per channel. A safety margin of 50% for the cooling system is strictly respected.

6.3.2 Power Supply Operation Range

A test of the power supply operation range is performed on *Beetle* chips. The aim is to prove the reliability of the chip design as well as the correct operation of the digital logic circuitry (*FastControl*)[10] and of the analogue readout path through the chip. From the technology features of the selected manufacturing process the nominal operating power supply voltage is specified as $V_{\text{dd}} = 2.5\,\text{V} \pm 8\%$. Hence, the maximum specified operating voltage is $V_{\text{dd,max}} = 2.7\,\text{V}$.

The total current consumption as a function of the applied power supply voltage is shown in fig. 6.17. All internal *Beetle* registers are programmed to the standard operating settings as defined in table C.14 of *The Beetle Reference Manual* (cf. appendix C). The system clock of 40 MHz is applied and the chip is processing triggers with a rate of 1.1 MHz. Within the measured range of V_{dd} between 1.5 V and 3.5 V, an exact linear correlation between the supply voltage and the power supply current is observed:

$$I_{\text{dd}} = (154 \pm 2)\,\text{mA/V} \cdot V_{\text{dd}} - (136 \pm 5)\,\text{mA} \tag{6.8}$$

with:
I_{dd} – power supply current [in mA],
V_{dd} – power supply voltage [in V] between 1.5 V and 3.5 V.

[9] All registers are programmed to the nominal settings of table C.14, readout is set to 4 analogue output ports, the system is clocked with 40 MHz and a mean trigger rate of 1.1 MHz is applied.

[10] The output resistance of a digital cell depends from the power supply voltage and therefore also the transition time from cell to cell.

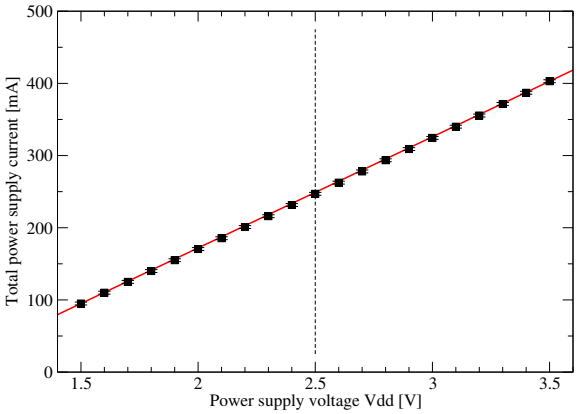


Figure 6.17: Total current consumption as a function of the *Beetle* supply voltage. The linear correlation in the measured range indicates that there are no current limitations in the design.

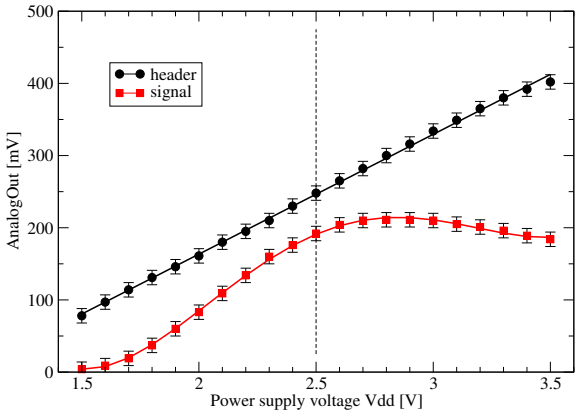


Figure 6.18: Analogue readout amplitude as a function of the supply voltage. The black curve represents the header size (baseline to header) whereas the red curve shows the analogue signal amplitude (baseline to signal peak).

This linear behaviour indicates that there is no on-chip current limitation in the measured power supply operation range.

Furthermore, the behaviour of the analogue output signals is analysed. Figure 6.18 shows the receiver output voltage for the analogue readout header and an analogue output signal, which corresponds to an input charge of 22 345 e^-. In the diagram the baseline offset is subtracted from the analogue signal. The header size is quoted as the difference between the positive *LeadingBit* of the header and the baseline before the readout.

In case of the header, the expected linear behaviour, as seen in simulation, is observed. The situation changes for the analogue output signals. Since the DC operating points of the different analogue parts on a *Beetle* exactly match each other, a variation in the power supply voltage shifts these operating points unevenly. For example, there are no signals visible for $V_{dd} < 1.5\,V$ whereas the header is already present.

6.3.3 Overclocking Test

Within this test the stability of logic circuitry (*FastControl*) which controls the event storage and readout is verified. Differing from the nominal system clock frequency of 40 MHz, the applied readout frequency is varied between 20 MHz and 100 MHz in steps of 10 MHz. The ratio between trigger and system clock frequency is kept constant at $\frac{1}{40}$ for all measurements.

In the complete tested frequency range no timing violations in the digital *FastControl* were observed. Furthermore, the processing of the analogue signals through the chip was also tested. Figure 6.19 shows the results of analogue signals at different applied system clock frequencies. The ratio of all signals normalised to the analogue output amplitude at 40 MHz are plotted for two different DAC register settings. The nominal register settings are specified in table C.14. In case of the maximum settings the registers indicated in table 6.6 are programmed with values, differing from the nominal values. Higher operating currents in the pipeline amplifier lead to a faster integration of signals. Therefore, analogue signal could be read out faster from

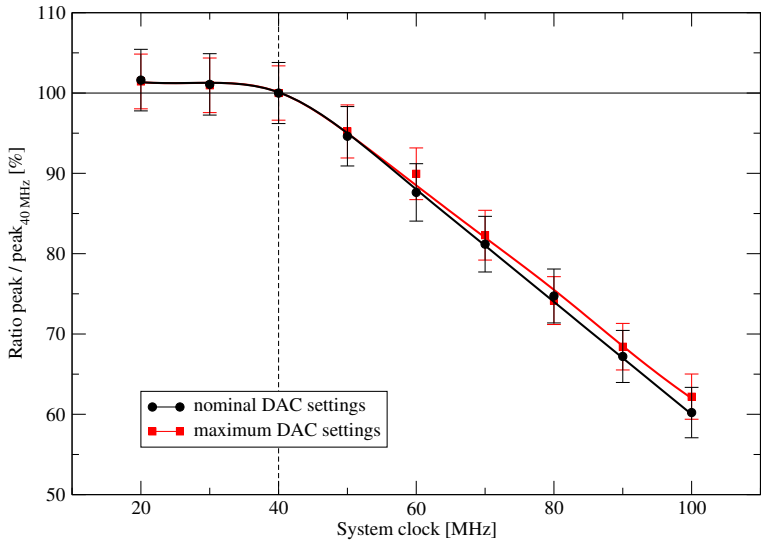


Figure 6.19: Results of a clock frequency sweep for two different DAC register settings. The output ratio is normalised to the signal peak amplitude at 40 MHz.

the pipeline. The analogue transmission of signals through the multiplexer is also faster as well as the current output driver.

Reg. no.	Reg. Name	Nominal Setting	Maximum Setting	Description
10	*Ipipe*	100 µA	1 600 µA	pipeamp bias current
13	*Ivoltbuf*	160 µA	2 000 µA	pipeamp buffer bias current
14	*Isf*	200 µA	1 000 µA	multiplexer buffer bias current
15	*Icurrbuf*	800 µA	2 000 µA	output buffer bias current

Table 6.6: Register contents for nominal and maximum overclocking DAC settings. All other not listed registers are programmed with nominal values. With a *Beetle* chip, programmed with the maximum settings, the readout of analogue signals from the pipeline is faster as well as the transmission through the multiplexer to the current output driver.

However, the measured results for both settings don't show a strong difference. This leads to the conclusion, that the analogue receiver circuitry on the external test board is too slow to keep pace with the readout of analogue signals at higher frequencies.

6.3.4 Temperature Test

The thermal properties of the LHCb VELO modules make it vital to control the operating temperature of the VELO sensors [Bow01b]. The VELO detectors will be exposed to an intense flux of particles that damage silicon, leading to heat being generated within the sensors when under bias. Additional heat is generated by the front-end readout electronics. Temperature is an important operating parameter for irradiated silicon as this directly affects the leakage current (cf. section 3.6). Thus it is necessary to construct a module that is capable of holding the sensors at the desired operating temperature of -5°C [Bow01a].

The aim of the temperature test is to prove the correct chip operation over a large ambient temperature range from −44℃ up to +75℃. Three different modes of operation are verified within this test setup – a start-up test, a long-term operation test and a maximum stress test. First of all the test environments are briefly described and afterwards the results are presented.

Test Setup

For this test a climatic exposure test cabinet[11] is used. Inside the test environment an adapter card is installed, that distributes all required signals to the Device Under Test (DUT). The adapter card receives the output signals of all *Beetle* chips and forwards it to a receiver board, that is located outside the cabinet. Because of the large temperature range, active components are not used on the adapter card. For the monitoring of the temperature inside the climatic exposure test cabinet, temperature sensitive devices (PT100) are placed at three different positions. The first one is glued on the adapter card and monitors the ambient temperature. The second one is glued on the backside of the PCB directly underneath a *Beetle* chip. The last PT100 is glued directly to the surface of the *Beetle* chip.

All analogue readout signals are sampled outside the test cabinet and stored on a PC. Other signals like `DataValid`, `FifoFull`, `WriteMon` and `TrigMon` are monitored with an oscilloscope. Temperatures of all three PT100 devices are also monitored and stored on a PC.

The correlation between ambient and chip surface temperature is plotted in fig. 6.20. For this measurement the *Beetle* chip is programmed to nominal register settings and clocked with the 40 MHz system clock. The readout is triggered with an average pseudo random trigger rate of 1.1 MHz. No active cooling system is applied to the chip. The resulting correlation fit from fig. 6.20 between chip surface and ambient temperature is quoted in eq. 6.9.

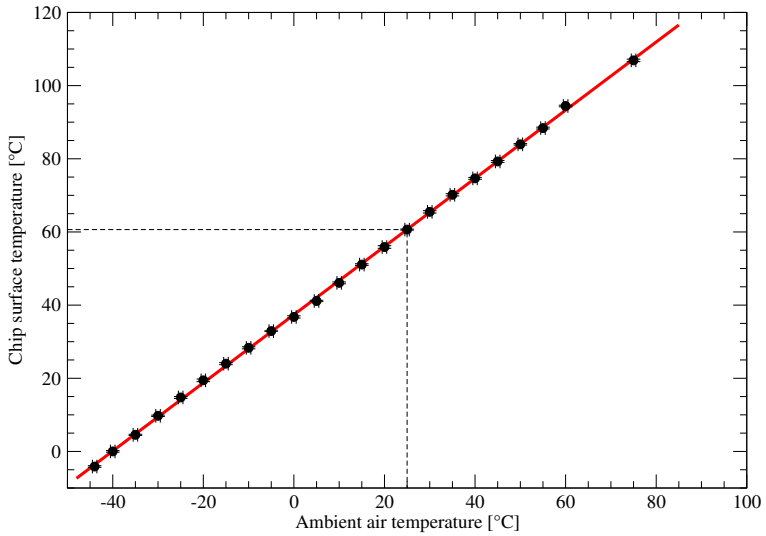


Figure 6.20: Correlation between ambient and *Beetle* chip surface temperatures. For room temperature (T= 25 ℃) the correlated chip temperature is marked with a dashed line.

$$T_{\text{surface}} = 0.93 \cdot T_{\text{ambient}} + 37.4℃ \tag{6.9}$$

[11] Model MPC AN 42/100 from MPC [MPC].

with:
T_{surface} – chip surface temperature [in ℃],
T_{ambient} – ambient air temperature [in ℃].

Start-up Tests

With this first test the start-up of two *Beetle* chips from a non-operating state is tested. After applying the power supply voltage, the chips have been reset and programmed via I^2C. Shortly after the registers are programmed to the nominal values, the chips are triggered and read out. The complete start-up test is repeated 15 times for each of the three start-up temperatures ($T_1 = -44\,℃$, $T_2 = +60\,℃$ and $T_3 = +75\,℃$). Both *Beetle* chips passed all the tests without any start-up problems.

Long-term Operating Tests

In total three long-term operating tests were performed with the *Beetle* chip, each at different ambient temperature ($T_1 = -44\,℃$, $T_2 = +60\,℃$ and $T_3 = +75\,℃$). During all three test runs (3×72 hours), the chips operated at nominal settings and consumed approximately $5.7 \cdot 10^{11}$ trigger signals. No errors have been observed.

Maximum Stress Test

A maximum stress test of a complete readout chip is performed with the *Beetle* chip. The aim of this test is to check the chip operation at very high temperatures, which can be caused by setting all *Beetle* registers to their maximum values. The ambient temperature of the climatic exposure test cabinet is set to $T = 60\,℃$ and all configuration registers are set to their maximum values. This results in a chip surface temperature of 126℃. The chip is tested under these conditions for more than 12 hours. No change in the performance could be determined within this stress test.

6.3.5 Random Trigger Test

In the context of this work several setup environments for testing the functionality and the correct operation of the pipeline control circuitry were developed. One of these verifications was done with a Random Trigger Test. The aim of such a test is to prove the correct mode of operation with an arbitrarily generated sequence of triggers. This indicates in detail that the control circuitry allocates and releases the correct pipeline column and performs the correct management of the derandomising buffer. Within this test only an evaluation of the pipeline control logic's functionality is possible, but not that of its timing behaviour. A timing check was done within an Overclocking Test (cf. section 6.3.3) and a Temperature Test (cf. section 6.3.4).

The test is performed with two *Beetle1.3* chips, running in parallel to check also the synchrony of both chips. To check as many combinations of different states as possible, the *Beetle* has to process a large number or arbitrary trigger signals. Due to setup constraints of used NIM modules, the generation of the random signal is accomplished with two noisy amplifiers. To adjust a defined trigger rate, two pulse generators with adjustable discriminator inputs are connected to the amplifier outputs. Both pulses are then combined to overcome the dead-time of the pulse generators and therefore to allow consecutive trigger signals. The setup of amplifier

Figure 6.21: Photography of the KIP ACEX board [ACEX]. It is a multi-purpose test board for experiments and exercises, originally designed for lab courses. The card can by used as a standard PCI card in a computer or as a stand-alone device. With two arbitrary external signals the FPGA on the ACEX board generates all digital signals for the random trigger test.

and discriminator is built with NIM modules. For the next signal processing steps the ACEX FPGA board is used [ACEX]. This board is a small multi-purpose test board, developed for small laboratory experiments. Figure 6.21 shows a picture of this ACEX board. It is the central processing unit of this setup and generates the 40 MHz system clock and the reset signal for the *Beetle* and it synchronises the random trigger signals from the pulse generators to the clock.

Within this test the number of generated triggers is compared to the number of *Beetle* readout frames and the number of rejected triggers. Triggers are only rejected if the derandomising buffer is full[12]. This condition is flagged with the external signal `FifoFull`. Furthermore, the synchrony of both chips is verified with the FPGA. Therefore it records and cross-checks the four signals `DataValid`, `FifoFull`, `WriteMon` and `TrigMon` of both chips.

Three test runs with different trigger rates were processed. Table 6.7 shows the number of triggers as well as the mean trigger rate. Both *Beetle1.3* chips passed the random trigger test successfully. Approximately $2 \times 2.34 \cdot 10^{12}$ triggers are processed without an error.

Test run	No. of chips	No. of triggers	Mean trigger rate
Run 1	2	$1.778 \cdot 10^{12}$	2.87 MHz
Run 2	2	$3.039 \cdot 10^{11}$	1.12 MHz
Run 3	2	$2.550 \cdot 10^{11}$	0.77 MHz

Table 6.7: Total number of processed random triggers and the mean trigger rate.

[12] Rejecting of triggers by the *Beetle* chips will not appear during data acquisition at LHCb because the Readout Supervisor (RS) will already prevent this condition. The RS will stop sending readout triggers as long as the derandomising buffers are still full.

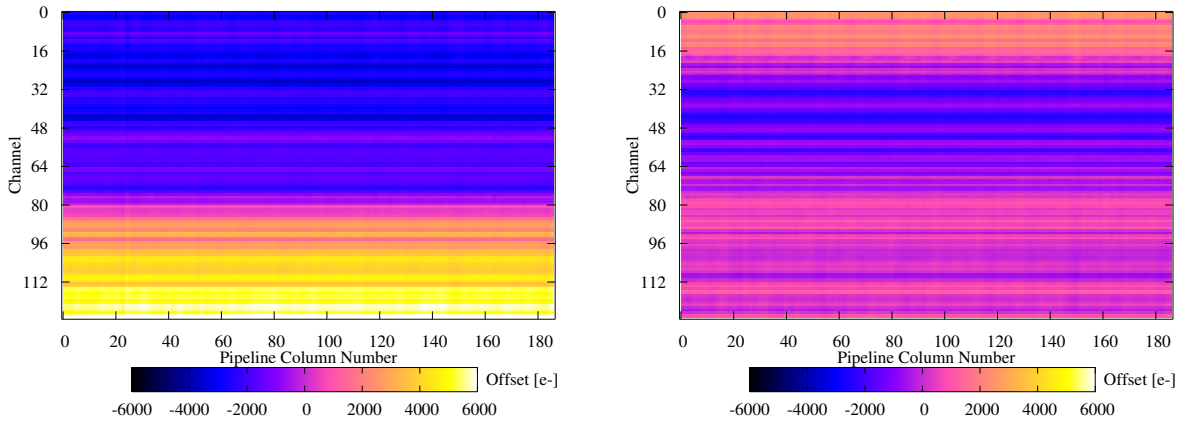


Figure 6.22: Pipeline offset of two *Beetle* chips as a function of the Pipeline Column Number (PCN) and the channel number. The left plot shows the pipeline of a *Beetle1.3* whereas the right plot shows the results of a chip version *1.5*. The common mode variations of the readout baseline is corrected in both plots. Chip version *1.5* shows less channel-to-channel variation.

6.3.6 Pipeline Homogeneity

A large part of the *Beetle* chip area is covered with the analogue pipeline. It is a switched capacitor array of 130 × 187 cells, working as a ring buffer. The rows are connected to the front-end output or to the comparator output respectively[13]. The total number of 130 rows consists of one test channel, one sense channel for common-mode subtraction and 128 detector channels (cf. figure 5.1). The number of columns is given by the maximum latency of 160 sampling intervals, 16 derandomising buffer columns and an additional logic overhead of 17 columns for the pipeline management [Bau03]. Detailed measurements are done on several *Beetle* chips to characterise the performance of the analogue pipeline concerning offset and signal voltage variations. The test and sense channels are not directly accessible on the *Beetle* chip. Therefore, the following measurement results only cover the 128 detector channels.

Pipeline Cell Offset

For the measurement of all 23 936 pipeline cell offsets, no test pulse signals were applied to the front-end inputs of the chip. A digital pattern generator provides trigger signals in a way that a defined pipeline column is read out by the PC. For each pipeline cell 5 000 measurement samples are taken. Figure 6.22 shows the results of a pipeline offset measurement from a *Beetle1.3* and a *Beetle1.5*. The data are represented in a 2D-plot. On variation the abscissae the Pipeline Column Numbers (PCNs) are outlined and on the ordinate the channel numbers are given. In both plots the common mode variations of the readout baseline are corrected. The calibration of the offset signal is taken from the gain measurement, which is described in the next section. For a better comparison between both chip versions, the mean offset of all PCNs for a defined channel number is plotted in fig. 6.23. The decrease of the offset spread across the channels is clearly visible for chip version *1.5*. This confirms the modifications in the pipeline layout.

[13] *PipelineMode* of register *CompControl* controls the input switch of the pipeline. With *PipelineMode* = 0 the output of the front-end amplifier is transferred to the pipeline, whereas with *PipelineMode* = 1 the comparator output is fed into the pipeline (cf. C.3.7).

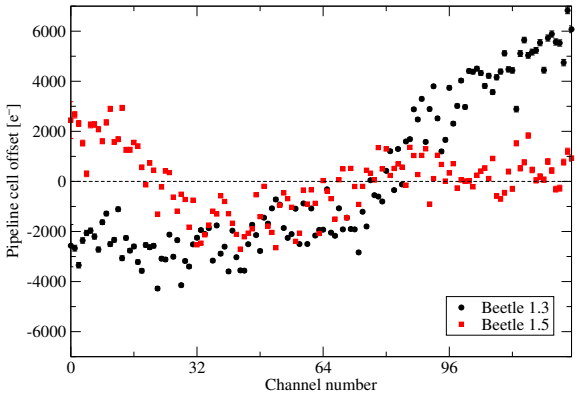


Figure 6.23: Average pipeline offset of two *Beetle* chips as a function of the channel number. The change in the average pipeline offset of chips from version *1.3* (black) is much larger compared to that of chips from version *1.5*.

Further the spread of the mean pipeline offset along the PCN respectively the channel number is shown in fig. 6.24. Both chip versions show the same behaviour of the offset variation. Across the PCN an uniform distribution has been measured. However, the offset spread of all PCNs for a defined channel shows a tub-shaped characteristic. Here the deviation is smaller in the centre of the pipeline than at the edges. No explanation has been found for this behaviour.

Gain

For a detailed characterisation of the gain distribution across the pipeline, two measurements were performed:

1. External signal source
   The pulse shape of an external signal source with a defined charge is scanned by shifting the input signal with respect to the sampling clock. The scan covers the signal range between −45 ns and +55 ns around the nominal pulse peak position with a time resolution of 500 ps. For each time step 50 samples are taken at the analogue output of the chip. To determine the gain, two positions of the shaped signal are used. One point is taken at the baseline of the pulse, the other point is the peak position itself. The difference of both values is calculated (V_p). From this the gain is given by

$$gain = \frac{Q_\mathrm{in}}{V_\mathrm{p}} \tag{6.10}$$

   where Q_in is the charge of the input signal. With this method the gain of at least 12 bonded channels was measured at the same time, limited by the layout of the test board.

2. Internal test pulse as signal source
   Once the gain is calibrated, the internal test pulse circuit is used to measure the gain uniformity of the complete pipeline. As accomplished before with an external signal, V_p is measured on the same way. With equation 6.10 the absolute charge for each pipeline cell is calculated.

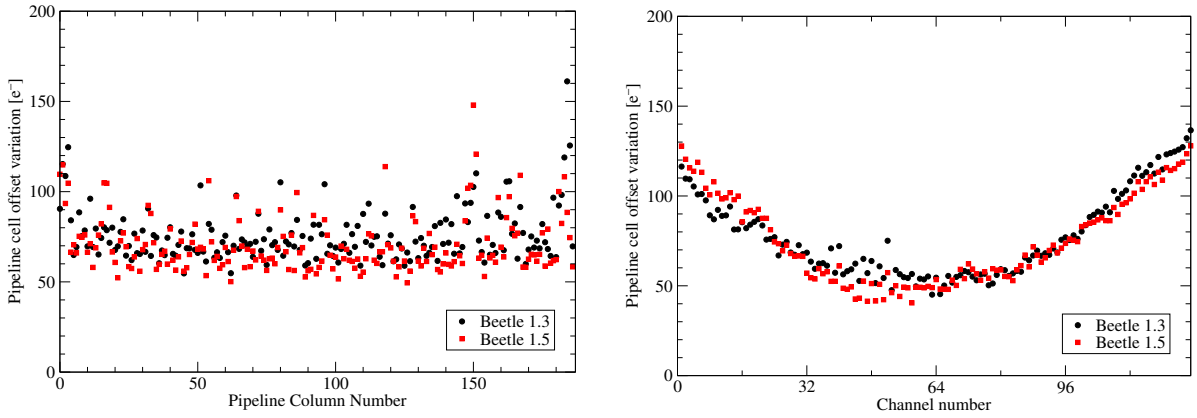


Figure 6.24: The variation of the mean pipeline cell offset is plotted in both diagrams. On the left side the variation for all channels of a given Pipeline Column Number (PCN) is plotted. The right diagram shows the variation of all PCNs for a defined channel number. In both plots the signal spread is converted into the equivalent input charge. Concerning the offset spread, no difference between a *Beetle* of version *1.3* (black) and *1.5* (red) is observed. Across the PCN there is no change of the offset variation observable. Whereas across all 128 channels the deviation is smaller to the centre than towards the edges.

Figure 6.25 shows the results of a pipeline gain measurement for an input signal of 22 345 e^-. A clear structure can be recognised in this plot – small variations along the channels whereas the gain shows no significant variations across the Pipeline Column Number. On the top diagram in fig. 6.26 the gain distribution of all 23 936 pipeline cells is plotted. The RMS value of these results is 234 e^-. It still contains the channel-to-channel variation of the front-end and pipeline amplifier. To extract only the contribution of the pipeline, the mean gain of each channel is calculated and normalised to the input charge of 22 345 e^-. The result is shown in the plot underneath. Here the RMS of the gain distribution is 125 e^-, which is 0.6% of the input charge.

6.3.7 Noise Performance

Extensive measurements of the noise performance have been done with the *Beetle* chip. First of all, the setup and the measuring procedure is described, then the results for different front-end settings are presented.

The measurement of the noise is performed on complete readout chips on the test board circuit as described before in section 6.1. If not indicated differently, all registers of the chip were programmed to the nominal values (cf. table C.14). Up to 6 arbitrarily chosen groups of two neighbouring channels, both having the same capacitive input load C_p, are connected to the external charge injection circuitry of the test board. With the component sizes given in fig. 6.2 and an external voltage step of 2.6 V at the input V_{ext}, a resulting test pulse with a charge equivalent of $Q_{in} = 22\,345\,e^-$ is injected in one of the two channels of each group. The injection circuitry of each second channel is connected to ground at node V_{div} in fig. 6.2.

Firstly the peak sampling point of the injected test pulse and the peak voltage V_p is determined. This is done by the measurement of the pulse shape with a time step resolution of 500 ps. For the following noise measurement, 10 000 samples V_{ij}^k ($(i = 1...6,\ j = 1, 2,\ k = 1...10\,000)$ at the peak position of the pulse were taken for each channel. The readout samples were distrib-

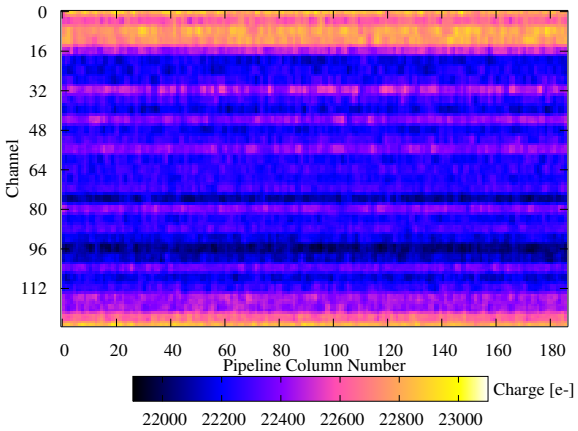


Figure 6.25: Pipeline gain distribution as a function of the channel and Pipeline Column Number. Gain variations along the channels are clearly visible.

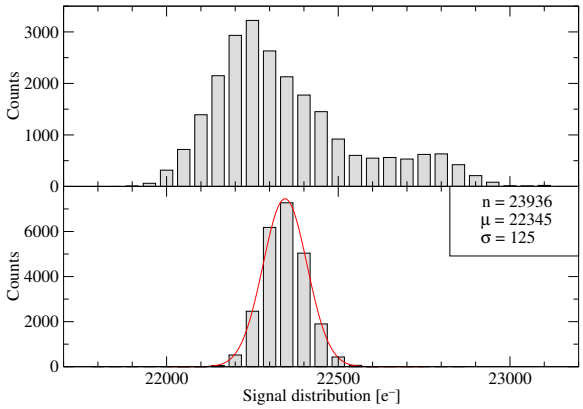


Figure 6.26: Signal distribution of the complete pipeline for an input charge of 22 345 e^-. The top plot shows the distribution without any corrections. In the bottom plot the gain distribution of the pipeline is shown. Therefore, the data was corrected for the characteristics of the individual channels' front-end and pipeline amplifier.

uted arbitrarily over all pipeline columns. To discard channel-to-channel variations the mean value per channel $\langle V_{ij} \rangle$ is subtracted from each sample V_{ij}^k. The samples of a channel with an input signal applied V_{i1} and the samples of a grounded channel V_{i2} are subtracted from each other $(\frac{1}{\sqrt{2}}(V_{i1}^k - V_{i2}^k))$ to eliminate common-mode effects. The noise voltage for each group is calculated according to eq. 6.11 [Bau03].

$$v_{n,i} = \sqrt{\frac{1}{N}\sum_{k=1}^{N}(\Delta V_i^k - \langle \Delta V_i^k \rangle)^2} \tag{6.11}$$

with:

$v_{n,i}$ – noise voltage for each group i,
ΔV_i^k – common-mode rejection ($\Delta V_i^k = 1/\sqrt{2}(V_{i1}^k - \langle V_{i1} \rangle - V_{i2}^k + \langle V_{i2} \rangle)$),
N – number of samples per channel ($N = 10\,000$).

According to equation 6.12 the Equivalent Noise Charge (ENC) is determined from the noise voltage v_n.

$$\mathrm{ENC} = \frac{v_n}{A_\mathrm{Q}} = \frac{v_n}{V_\mathrm{p}/Q_\mathrm{in}} \tag{6.12}$$

with:

v_n – noise voltage [V],
A_Q – charge gain [V/e^-],
V_p – peak voltage of test pulse [V],
Q_in – injected input charge [e^-].

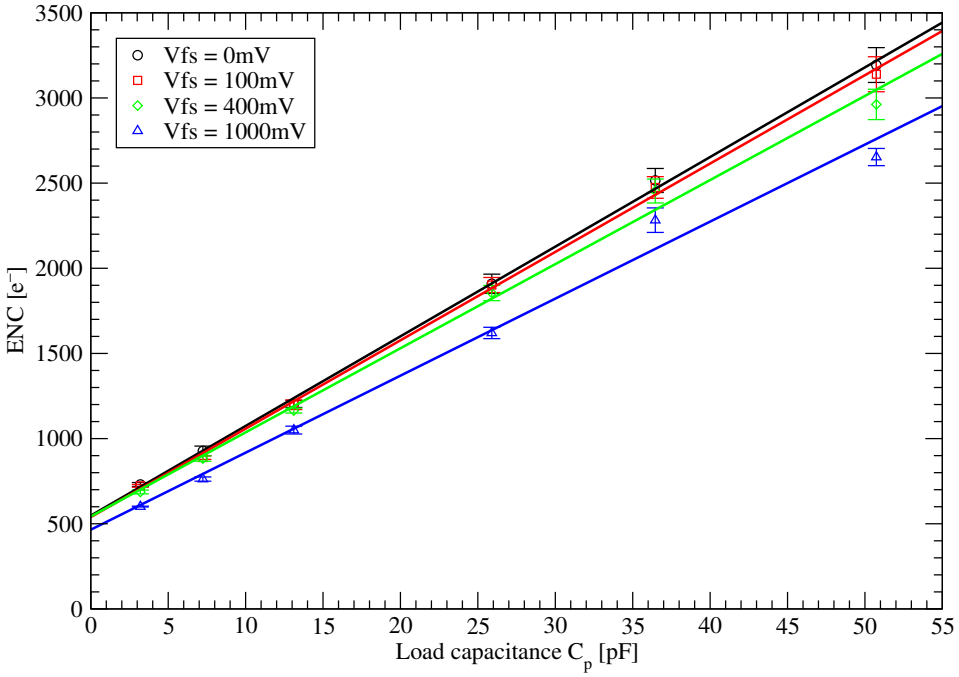


Figure 6.27: Equivalent Noise Charge of a *Beetle1.3* chip as a function of the load capacitance C_p and different feedback voltages of the front-end shaper (*Vfs*).

Vfs	Equivalent Noise Charge
0 mV	$(548 \pm 23)\,\mathrm{e}^- + (52.6 \pm 0.8)\,\mathrm{e}^-/\mathrm{pF} \cdot C_\mathrm{p}$
100 mV	$(539 \pm 24)\,\mathrm{e}^- + (51.9 \pm 0.8)\,\mathrm{e}^-/\mathrm{pF} \cdot C_\mathrm{p}$
400 mV	$(543 \pm 51)\,\mathrm{e}^- + (49.4 \pm 1.8)\,\mathrm{e}^-/\mathrm{pF} \cdot C_\mathrm{p}$
1 000 mV	$(465 \pm 70)\,\mathrm{e}^- + (45.2 \pm 2.5)\,\mathrm{e}^-/\mathrm{pF} \cdot C_\mathrm{p}$

Table 6.8: Equivalent Noise Charge of a *Beetle1.3* for different feedback voltages *Vfs* of the front-end shaper, measured at 25°C room temperature.

To determine the noise performance of a *Beetle* chip, the ENC is measured for different load capacitances C_p in the range of 3 pF to 50 pF and as well for different settings of the front-end shaper feedback (*Vfs* = 0...1 000 mV). For the data acquisition a pseudo-random trigger is applied to the *Beetle* chip to provide an arbitrary sampling over all pipeline cells. Table 6.8 lists the results for a chip from version *1.3*, the corresponding diagram of the ENC performance is shown in fig. 6.27. For increasing values of *Vfs* – and therefore a larger feedback resistance of the shaper R_fb – the slope decreases from 52.6 e^-/pF down to 45.2 e^-/pF. Simultaneously the offset of the linear equation decreases from 548 e^- down to 465 e^-.

The results of the ENC performance for different chip versions are given in table 6.9. The differences in the ENC figures originate from modifications at the pipeline structure and at the power routing of the pipeline readout amplifier between different chip versions. The modifications show a slight improvement in slope and offset for chip version *1.4* and *1.5*. This can be explained by the reduction of the parasitic capacitances C_pr of the pipeline readout path in front of the pipeline amplifier (cf. figure 5.27). A larger fraction of the stored charge in the pipeline cell C_S is now transferred to the input of the amplifier and, therefore, the gain

Chip version	Equivalent Noise Charge
Beetle1.3	$(548 \pm 23)\,\mathrm{e}^- + (52.6 \pm 0.8)\,\mathrm{e}^-/\mathrm{pF} \cdot C_\mathrm{p}$
Beetle1.4	$(543 \pm 26)\,\mathrm{e}^- + (50.6 \pm 1.2)\,\mathrm{e}^-/\mathrm{pF} \cdot C_\mathrm{p}$
Beetle1.5	$(531 \pm 10)\,\mathrm{e}^- + (49.8 \pm 0.5)\,\mathrm{e}^-/\mathrm{pF} \cdot C_\mathrm{p}$

Table 6.9: Equivalent Noise Charge of *Beetle* chips from version *1.3* to *1.5* for $Vfs = 0\,\mathrm{mV}$.

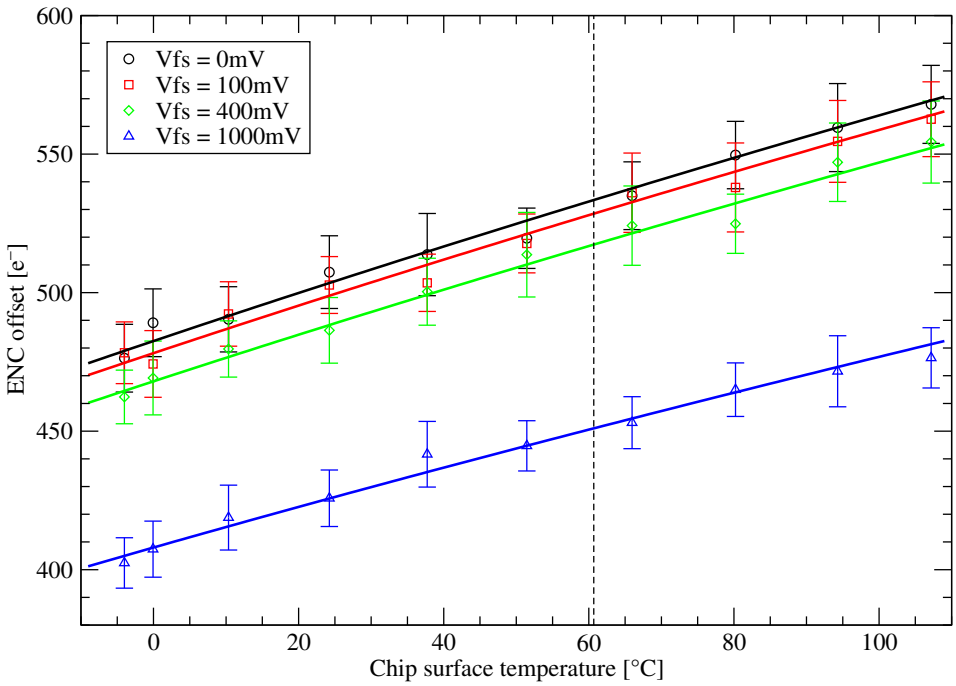


Figure 6.28: Offset of the ENC as a function of the chip temperature T and different shaper feedback voltages *Vfs*. The dashed line marks the surface temperature of the chip at 25°C room temperature.

is increased. The new uniform power routing of the pipeline amplifier additionally contributes to the reduction in noise.

Temperature Dependency of the Noise Performance

In the context of the chip characterisation, several test series were performed to measure the characteristics at different temperatures. The typical setup of such a temperature test is already described in section 6.3.4. Hereafter, the change of the noise characteristics at different temperatures is discussed.

The chip is operated in the climatic exposure test cabinet with ambient temperatures from −44°C to +75°C. According to eq. 6.9 this corresponds to a chip temperature of −4°C to +107°C. Figure 6.28 shows the offset of the ENC as a function of the chip temperature for different shaper feedback settings *Vfs*.

For the interpolation of the measurement results, the input equivalent noise formula for q_{ineq} is taken [Fal98]. It is given by the eq. 6.13, where the input noise current (i_{p}) and the input noise voltage (v_{s}) of amplifiers are defined in eq. 6.14 respectively in eq. 6.15 [Zie76].

$$ {q_{\mathrm{ineq}}}^2 = \underbrace{4kT\frac{1}{R_{\mathrm{in}}\left|j\omega\right|^2}}_{\text{thermal noise}} + \underbrace{\frac{{i_{\mathrm{p}}}^2}{\left|j\omega\right|^2}}_{\text{parallel noise}} + \underbrace{\frac{{v_{\mathrm{s}}}^2}{{R_{\mathrm{fb}}}^2\left|j\omega\right|^2} + {v_{\mathrm{s}}}^2{C_{\mathrm{in}}}^2}_{\text{series noise}} \tag{6.13} $$

$$ {i_{\mathrm{p}}}^2 = 4kT\,\frac{2(1+\eta)}{3}\cdot\frac{1}{g_{\mathrm{m}}} \tag{6.14} $$

$$ {v_{\mathrm{s}}}^2 = 4kT\,\frac{4}{15}\cdot\frac{\omega^2{C_{\mathrm{GD}}}^2}{g_{\mathrm{m}}} + 2eI_{\mathrm{leak}} \tag{6.15} $$

with:

g_{m}	–	transconductance [A/V],
η	–	Bulk Factor $= \frac{g_{\mathrm{m,BS}}}{g_{\mathrm{m}}}$,
I_{leak}	–	leakage current of the input FET [A],
R_{in}	–	signal source impedance [Ω],
R_{fb}	–	feedback resistor [Ω],
C_{in}	–	capacitive input signal source [F],
C_{GD}	–	gate-drain capacitance of the input FET [F],
k	–	Boltzmann's constant $k = 1.3807\cdot10^{-23}\ \mathrm{J\,K^{-1}}$,
T	–	absolute temperature [K].

The first term of eq. 6.13, the *thermal noise*, contributes linear to the temperature dependency. The second term, described by eq. 6.14, as well as the third term (eq. 6.15) contributes also as a factor of proportionality to the temperature behaviour. According to the square root of eq. 6.13, a $\sqrt{aT+b}$ characteristic describes the measured ENC offsets. These fits are in good agreement with the data from the measurements. In a first approximation the fit-function is nearly linear for the covered temperature range, with a slope less than $1\,e^-/\mathrm{K}$. The previous ENC equations from table 6.8 can thus be extended by a temperature dependent noise factor. The new equations are summarised in table 6.10. They are valid for chip temperatures between −20°C and +120°C.

Vfs	Equivalent Noise Charge
0 mV	$(261\pm23)\,\mathrm{e^-} + (0.8\pm0.1)\,\mathrm{e^-/K}\cdot T + (52.6\pm0.8)\,\mathrm{e^-/pF}\cdot C_{\mathrm{p}}$
100 mV	$(255\pm24)\,\mathrm{e^-} + (0.8\pm0.1)\,\mathrm{e^-/K}\cdot T + (51.9\pm0.8)\,\mathrm{e^-/pF}\cdot C_{\mathrm{p}}$
400 mV	$(265\pm51)\,\mathrm{e^-} + (0.8\pm0.1)\,\mathrm{e^-/K}\cdot T + (49.4\pm1.8)\,\mathrm{e^-/pF}\cdot C_{\mathrm{p}}$
1 000 mV	$(223\pm70)\,\mathrm{e^-} + (0.7\pm0.1)\,\mathrm{e^-/K}\cdot T + (45.2\pm2.5)\,\mathrm{e^-/pF}\cdot C_{\mathrm{p}}$

Table 6.10: Extended Equivalent Noise Charge equations of a *Beetle1.3* chip for different feedback voltages *Vfs* of the front-end shaper. C_{p} is the detector load capacitance at the input of the front-end and T is the absolute chip temperature ($253\,\mathrm{K} \le T \le 393\,\mathrm{K}$).

6.3.8 Dynamic Range, Linearity and Output Charge Calibration

Within the LHCb experiment, the dynamic charge range for the *Beetle* chip is defined between $\pm110\,\mathrm{ke^-}$. Within this region, the output has to be linear with a maximum variation of ±5%. To

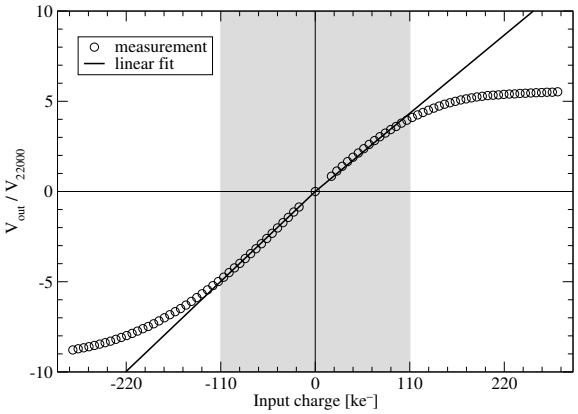


Figure 6.29: Dynamic range of a readout chip for positive and negative input charges. At the ordinate the analogue output signal V_{out} is normalised to 1 for $V_{22\,000}$, which is the corresponding voltage for an input charge of $22\,000\,\text{e}^-$. The highlighted area between $-110\,000\,\text{e}^-$ and $+110\,000\,\text{e}^-$ shows the specified range of the normal operating mode.

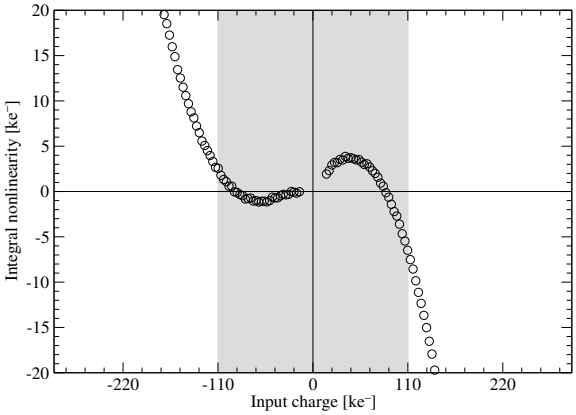


Figure 6.30: Integral Nonlinearity $\Delta Q_{\text{integral}}$ of the dynamic range as a function of the input charge for the specified operating range. The ordinate is recalculated into the corresponding charge value. The slope parameters for the optimised fit within ±5% INL are given in equation 6.16.

handle larger input charges, the standard test setup is modified. The input coupling capacitor C_{C} of the charge injection circuit on the daughter board (cf. figure 6.2 on page 114) is changed from the nominal 1.08 pF to 3.94 pF. According to equation 6.1 the possible charge at the front-end input of this setup is expanded to $\pm 282.2\,\text{ke}^-$. The analogue readout voltages of 12 different input channels are measured in parallel at the output of the receiver circuitry. The individual channel readout offset is subtracted from each output signal. All offset corrected signals are than averaged to a common value. The shift of the front-end sampling point for large input charges from section 6.2.1 is not compensated within this measurement.

In figure 6.29 the dynamic range of a *Beetle* chip is plotted for both input charge polarities. To suppress the influence of the external receiver, the measured output voltages V_{out} are normalised to 1 for $V_{22\,000}$, which is the corresponding output voltage for a defined input charge of $22\,000\,\text{e}^-$. The best fitted straight line $V_{\text{out,fit}}$ is determined for positive and negative charges in the specified operating range of the *Beetle* chip [Sch01] and is given by

$$V_{\text{out,fit}}(Q_{\text{in}}) \;=\; \begin{cases} 0.867\ \frac{Q_{\text{in}}}{+22\,000\,\text{e}^-}\ V_{+22\,000} & \text{for } Q_{\text{in}} > 0 \\ 0.997\ \frac{Q_{\text{in}}}{-22\,000\,\text{e}^-}\ V_{-22\,000} & \text{for } Q_{\text{in}} < 0 \end{cases} \tag{6.16}$$

with:

$V_{\text{out,fit}}$	–	best fitted straight line for analogue receiver output voltage [in V],
$V_{\pm 22\,000}$	–	output receiver voltage for a defined input charge of $\pm 22\,000\,\text{e}^-$ [in V],
Q_{in}	–	input charge of the analogue front-end [in e^-].

The Integral Nonlinearity (INL) of V_{out} is extracted from fig. 6.29. It shows the overall deviation from linearity by taking the difference between the best fitted straight line $V_{\text{out,fit}}$ from eq. 6.16 and the measured V_{out}. However, it is more intuitive to quote the result again as a charge

value. By multiplying the output difference with the normalisation factor $\frac{\pm 22\,000\,\mathrm{e}^-}{\pm V_{22\,000}}$, the INL is then defined as

$$\Delta Q_{\mathrm{integral}}(Q_{\mathrm{in}}) = \pm 22\,000\,\mathrm{e}^- \; \frac{V_{\mathrm{out}}(Q_{\mathrm{in}}) \; - \; V_{\mathrm{out,fit}}(Q_{\mathrm{in}})}{V_{\pm 22\,000}} \tag{6.17}$$

with:

$\Delta Q_{\mathrm{integral}}$ – INL for charge Q_{in} at the front-end input [in e^-],
V_{out} – output voltage corresponding to charge Q_{in} at the input [in V].

Figure 6.30 shows the final INL as a function of the input charge. The highlighted area represents the required dynamic range of the *Beetle*. Within this area the INL for negative input charges is between $-1.2\,\mathrm{ke}^-$ and $+2.6\,\mathrm{ke}^-$. For positive input charges the discrepancy is much larger. Here the INL is between $-6.5\,\mathrm{ke}^-$ and $+3.9\,\mathrm{ke}^-$.

Outside the specified region of $\pm 110\,\mathrm{ke}^-$, the analogue readout saturates at different input charges. For example the readout ratio in fig. 6.29 shows no further increasing for positive charges greater than $180\,\mathrm{ke}^-$, whereas for negative charges the readout still shows a small signal changing at $-286\,\mathrm{ke}^-$. The reason for this asymmetric behaviour can be explained by the analogue pipeline of the *Beetle*. By increasing the input charge at the front-end, the output voltage of the front-end buffer is decreasing. If this voltage is falling below $\approx$700 mV, the capacitance of the NMOS pipeline capacitor is starting to degrade. A simulation of the pipeline cell capacitance behaviour is shown in fig. 5.24.

In addition, the charge calibration function is extracted from the dynamic range of fig. 6.29 for both charge polarities. Assuming that the normalisation output voltage $V_{22\,000}$ for an input charge of $22\,000\,\mathrm{e}^-$ is measured once, the empiric equation 6.18 defines the front-end input charge Q_{in}. The discrepancy between the measured output and eq. 6.18 is less than 2.7% for the compelte dynamic range.

$$Q_{\mathrm{in}}(V_{\mathrm{out}}) \; = \; a0 \cdot \exp\left(a1 \cdot \frac{V_{\mathrm{out}}}{V_{\pm 22\,000}}\right) + a2 \cdot \frac{V_{\mathrm{out}}}{V_{\pm 22\,000}} + a3 \cdot \left(\frac{V_{\mathrm{out}}}{V_{\pm 22\,000}}\right)^3 \tag{6.18}$$

with:

Charge polarity	$a0$	$a1$	$a2$	$a3$
positive	$1.02 \cdot 10^{-9}$	5.83	20 971	412.8
negative	$-3.68 \cdot 10^{-1}$	−1.35	21 034	66.7

6.3.9 Channel Crosstalk

A signal crosstalk between neighbouring channels is measured on *Beetle* chips. It is not uniformly distributed over all channels. A signal applied to an even channel shows a definite crosstalk to the successor channel, whereas for an odd input channel number the crosstalk to the predecessor channel is larger.

Detailed results from the crosstalk measurement are summarised for different chip versions in table 6.11. One source of this channel depending crosstalk was found on the *Beetle1.3* in the huge parasitic capacitance between two neighbouring output lines of the analogue pipeline memory. They are routed in parallel with a distance of about 1.5 µm over a total length of nearly 2 mm to the pipeline readout amplifier (cf. fig. 5.26). By increasing the distance between both lines to 3.1 µm and modifying the pipeline cell, the channel depending crosstalk is reduced on *Beetle* chips of version *1.4* and *1.5*.

Beetle version	even input channel number		odd input channel number	
	predecessor [%]	successor [%]	predecessor [%]	successor [%]
1.3	(0.44 ± 0.42)	(3.85 ± 0.42)	(3.18 ± 0.41)	(1.86 ± 0.41)
1.4	(0.07 ± 0.45)	(1.62 ± 0.45)	(2.03 ± 0.46)	(1.97 ± 0.46)
1.5	(0.12 ± 0.51)	(1.89 ± 0.51)	(1.95 ± 0.47)	(1.93 ± 0.47)

Table 6.11: Signal crosstalk between neighboured channels on different *Beetle* chip versions.

The crosstalk in the second column (even input channel into predecessor channel) and the last column (odd input channel into successor channel) of table 6.11 indicates that there is second contribution to the crosstalk, which couples only into one direction – namely into the next channel. This can be easily associated to a crosstalk within the readout of all channels. There is still a small signal remainder in the analogue output from the previous channel (25 ns before).

6.3.10 Baseline Behaviour of Consecutive and Non-Consecutive Readouts

The *Beetle* chip has three different possible readout conditions:

- the *non-readout* is the condition where the *Beetle* is not transmitting analogue channel information off chip. In this condition, the analogue output driver is connected to a constant signal.
- a *non-consecutive readout* starts after a trigger occurs during a non-readout condition.
- *consecutive readout*: if the *Beetle* receives a trigger at least 100 ns before the last readout is completed, the next readout is send as a consecutive readout. In the consecutive readout condition, there is no gap in between two readout frames as LHCb requires a dead-time free readout [Chr01].

Figure C.13 shows the exact timing criteria which defines the non-consecutive and consecutive readout mode.

Both readout modes use different timing implementations for the pipeline amplifier and the analogue multiplexer control signals. In case of the consecutive readout mode the signal timings of the pipeline amplifier are more critical than in the non-consecutive readout mode (cf. section 5.8 and fig. 5.30). Because of the long routing lines for the control signals inside the pipeline amplifier[14], the intrinsic R-C-delay introduces a signal shift across the amplifier. Within the modifications on the *Beetle1.5*, additional signal line drivers are implemented inside the pipeline amplifier and the power routing to the pipeline amplifier channels is improved.

Figure 6.31 shows the analogue readout of two triggered events in the 128 channels on one port mode for different chip versions of the *Beetle*. The first event is read out in the non-consecutive mode, whereas the second one is transferred immediately at the end of the first frame as a consecutive readout. An increase of the channel offset to the end of each readout frame is observable for chips from version *1.3* and *1.4* whereas the baseline for a *Beetle1.5* is nearly flat. The channel offsets between the second and the first readout of fig. 6.34 are

[14] From the first to the last channel the length is ≈ 3.9 mm.

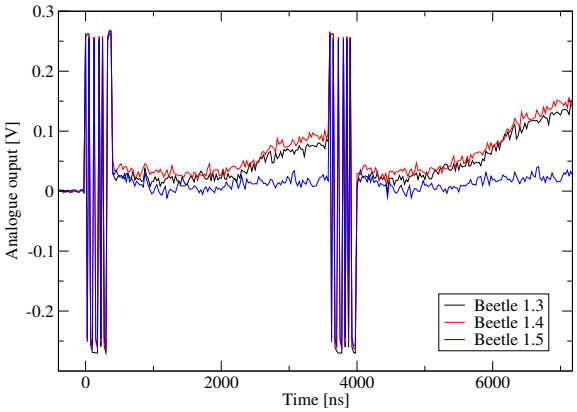


Figure 6.31: Offset behaviour of different chip versions for two triggered events. The left readout is labelled as a non-consecutive readout because there was no readout ongoing as the trigger occurred. The second trigger was received during the first readout and therefore the right readout is called a consecutive readout.

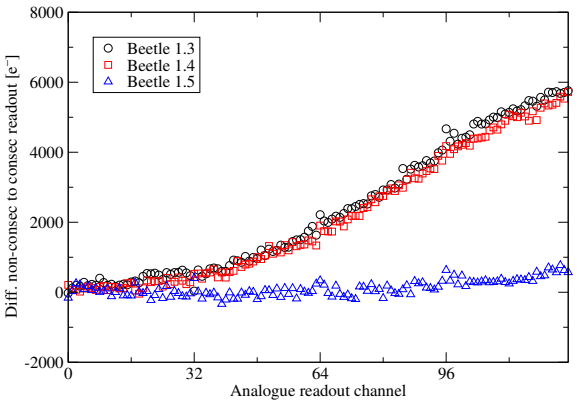


Figure 6.32: Difference of the baseline offset between a non-consecutive readout and a consecutive readout for different chip versions.

subtracted from each other and plotted in fig. 6.32. Hereby, the baseline difference is recalculated to an equivalent input charge. Between the non-consecutive and the consecutive readout of version *1.3* and *1.4* there is a significant increase of spread. At the end of the frame, the difference is comparable to an input charge signal of $\approx 5\,700\,\mathrm{e}^-$. The difference between both readout conditions is for the *Beetle1.5* less than $700\,\mathrm{e}^-$.

Further measurements are done for the study of the baseline stability between different readouts combinations. By applying random trigger sequences to *Beetle* chips of version *1.3* and *1.5*. Figure 6.33 shows the results of the offset distribution for the last channel 127, which showed the biggest difference between both chip versions (fig. 6.32. In case of version *1.3*, two different offsets are measured while for a *Beetle1.5* only one offset is found.

In addition, for each of the measured readouts the offset of channel 127 is compared with the output value 25 ns before the readout frame. In case of a consecutive readout the offset 25 ns before the frame is equal to the offset of channel 127 from the previous readout, whereas in case of a non-consecutive readout this value represents the output offset of the analogue output driver during non-readout. The results are shown in the correlation plot of fig. 6.34. For *Beetle1.3* three groups, clearly separated from each other, are observed. The first small black region on the left side of the diagram represents the non-consecutive readout (non-readout vs. non-consecutive readout). The middle group is identified as the first consecutive readout after a non-consecutive readout, followed by the group on the right side. This part combines all the consecutive readouts where the previous readout was already read out in a consecutive mode. The correlation plots confirms that there are only two different readout baselines for *Beetle1.3* – the baseline for a non-consecutive and for a consecutive readout.

In case of *Beetle1.5* only two clearly separated groups are measured. Again, the small group (red) on the left side is linked to the situation of a first, non-consecutive readout. The second

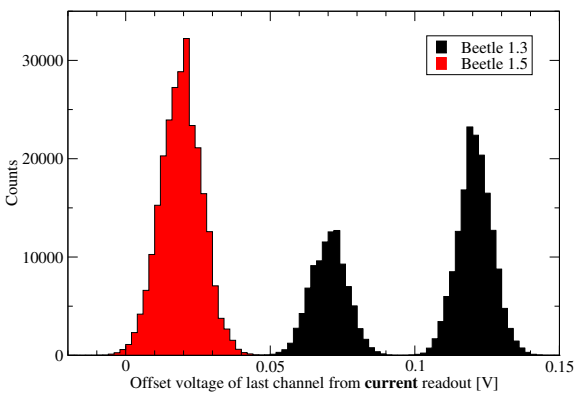


Figure 6.33: Readout offset histogram of the last channel for different chip versions. The offset for the first channel is set to 0. For a *1.3* there are two peaks observable (non-consecutive readout at $\mu = 0.0713$ and consecutive $\mu = 0.1218$) whereas for a *1.5* only one peak at $\mu = 0.0202$ is measured. This peak represents both readout conditions.

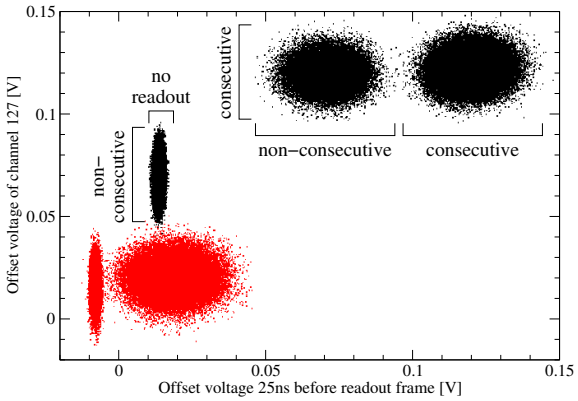


Figure 6.34: Offset voltage correlation plot of a readout and the predecessor readout. In each case the last channel 127 is plotted. The different readout combinations for a *Beetle1.3* (black dots) are labelled in the diagram. In case of a *Beetle1.5* (red) the non-consecutive and the consecutive readout are super-imposed.

group is identified as a consecutive readout. Herein, the background of the last readout is not an issue any more.

Summary of Baseline Behaviour

The modifications at the pipeline amplifier improved the baseline behaviour between the non-consecutive and the consecutive readout modes on the *Beetle1.5*. Furthermore, each readout mode on the *Beetle1.3* (and also version *1.4*) has its own defined baseline.

6.4 Test Nodes

Different test nodes are implemented on the *Beetle* chip. The test nodes allow direct access to internal circuits. Table 6.12 summarises all available test nodes for the different chip versions. For example all bias nodes of the front-end are available for direct measurements as well as the output of the analogue test channel after the front-end (`TestOutput`) and after the pipeline-amplifier (`PipeampTestOut`). For the chip version *1.5* of the *Beetle*, a special test structure for measuring the process variation is implemented. The analysis of this structure is discussed in detail in section 6.5. The measurement of the current source and the current DAC *Ibuf* are the only reported measurements here.

6.4.1 Current Source

The integrated current source provides the necessary reference current for all current DACs. On each *Beetle* chip there are two independent but identical current sources implemented. The so called *front-end current source*, which provides the current for the 7 internal DACs of the

Test node name	Description	Chip version
Front-end related test nodes:		
`Prebias`	Bias node of preamplifier current source (cf. C.7)	all
`Prebias1`	Bias node of preamplifier cascode branch (cf. C.7)	all
`Shabias`	Bias node of shaper current source (cf. C.7)	all
`Shabias1`	Bias node of shaper cascode branch (cf. C.7)	all
`Bufbias`	Bias node of buffer current source (cf. C.7)	all
`TestOutput`	Front-end output of test channel (cf. C.7)	all
`PipeampTestOut`	Pipeline-amplifier output of test channel	all
Current source related test nodes:		
`ProbeIoutBE`	Test current output of the back-end current source	all
`ProbeVrefBE`	Reference voltage of the back-end current source	all
`ProbeVrefFE`	Reference voltage of the front-end current source	only 1.2
`ProbeIDAC`	Output of current DAC (*Ibuf*)	only 1.3/1.4
Other test structures and test signals:		
`PPTout`	Output of digital Process Parameter Test structure	only 1.5
`WriteMon`	Indicates if the pipeline write pointer passes column 0	all
`TrigMon`	Indicates if the pipeline trigger pointer passes column 0	all
`FifoFull`	Signal that indicates a full derandomising buffer	all

Table 6.12: Accessible test nodes and test structures of the *Beetle* chip.

front-end and comparator part, and the *back-end current source* for the current distribution of the pipeline-amplifier, multiplexer and the analogue output driver.

The measurement access to the back-end current source is possible on all chip versions. For version *1.2* also the front-end current source is accessible for testing. Because the current source should not be influenced during chip operation, the test nodes of the current source are not routed directly to the test pads. Instead, the output current is mirrored to the test pad `ProbeIoutBE`. In case of the sensitive internal reference voltage V_{ref} the test pads `ProbeVrefBE` and `ProbeVrefFE` can be switched off. They are controlled by *ProbeEnable* (bit 7) of register *ROCtrl* and should be disabled during normal chip operation. The schematic in fig. 6.35 gives an overview of current source test nodes. A detailed overview of the current source (left box) is given in section 5.12.1. Simulation results in a nominal output current I_{out} of 126.2 µA. This corresponds to 1 283 mV at `ProbeVref` respectively 79.6 µA at `ProbeIout`[15].

To compare the results from simulation and measurement of the test node, the current source has to operate at a supply voltage of 2.5 V. The exact supply voltage at the current source is therefore also accessible in the switched off state of pad `ProbeVref` as indicated in fig. 6.35. The measured voltage drop, caused by the resistance of the power lines between the power pads and the current source, is compensated externally.

The current source output is measured for each chip version via this test node circuit. Because the circuitry and layout of the current sources have not changed between *Beetle* versions *1.2* and *1.5*, an analysis of the variations between different chips is possible. Figure 6.36

[15] The results for the test nodes are general for both current sources, if the appendix `BE` (back-end) or `FE` (front-end) are not explicit given.

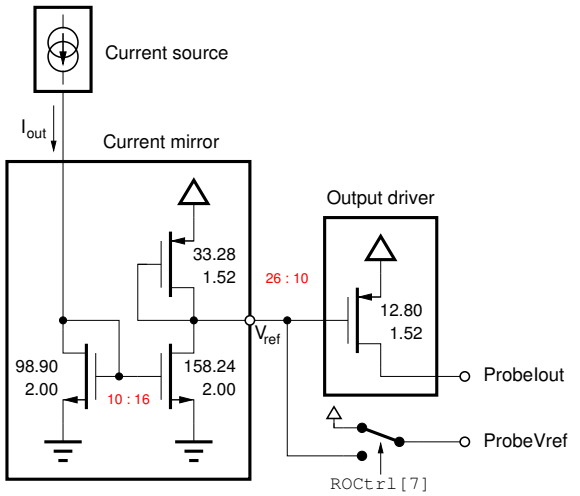


Figure 6.35: Schematic of the current source test node `ProbeIout` and `ProbeVref`. The detailed circuit of the current source block is shown in fig. 5.44.

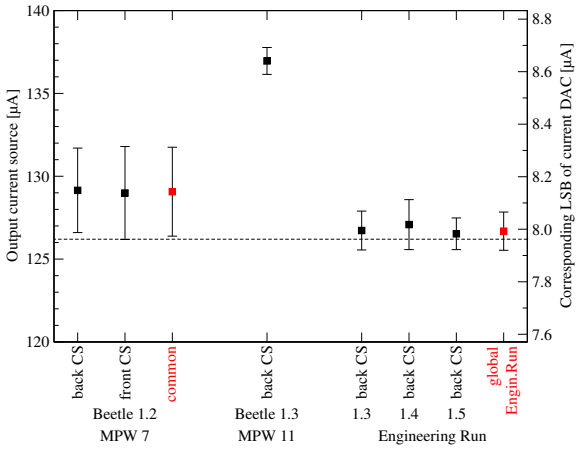


Figure 6.36: Measured output currents of the common current source for different *Beetle* versions and productions lots. The corresponding current of a LSB for the current DAC is quoted on the right ordinate.

shows the results for different chip versions and for different production lots. The dashed line illustrates the nominal output current of 126.2 µA mentioned before. Obviously, the results obtained for chips from the same production lot show similar output currents. Significant higher output currents are measured for *Beetle1.3* chips from MPW run 11. Compared to the results from the same chip version submitted on the Engineering Run, this leads to the conclusion, that this effect is caused by the manufacturer. The big deviation from the mean value of the current measurement of *1.2* chips can be explained by different corner parameters (cf. section 6.5). By a mistake during diceing chips with different corner parameters are not sorted out. By simulating the spread in corner values, the results are comparable with the measured deviation of the *1.2* chips.

Finally, there are no significant variations between the two current sources on the same chip[16], which are placed at two different positions on the chip with a distance of approximately 3.3 mm. The current output difference is calculated to 0.10 µA, which is negligible and well in between the range of the calculated deviation of ±0.36 µA. This leads to the conclusion, that the design matching between both currents sources is very good.

6.4.2 Current DAC

For the first *Beetle* prototype design a current DAC with a resolution of 10 bits and an LSB current of ≈2 µA was chosen [Sma04]. Since 10-bit resolution turned out to be not necessary and since it takes more effort to program a 10-bit DAC with an 8-bit bus protocol, all internal DACs of the *Beetle* were redesigned to 8-bit DACs. By increasing the output current of the LSB at the same time to 7.96 µA, the overall dynamic range is still 2 mA. A side effect of this modification was also the decrease of the physical size by a factor of 4 for the current DAC

[16] Measurement is only possible with chips from version *1.2* because the test nodes of both current sources are routed to pads.

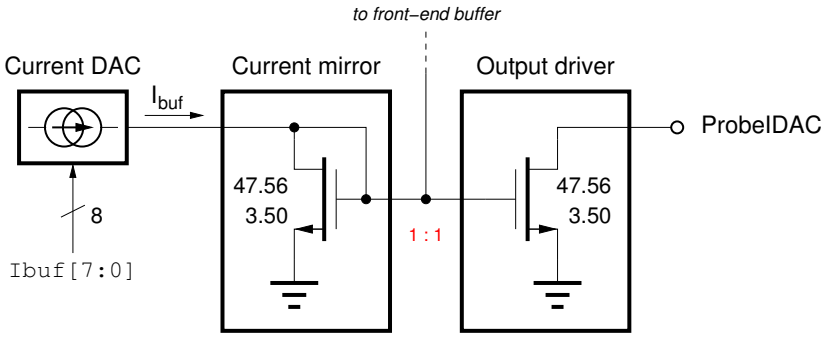


Figure 6.37: Schematic of the current DAC test node `ProbeIDAC`. The output current of the DAC is controlled by the register `Ibuf` of the front-end buffer.

layout. The new design layout was implemented for the first time on *Beetle1.2*. A drawback was, that detailed performance studies of the new design could not be done with this chip version. No DAC output currents were accessible via test nodes. Therefore, on version *1.3*, the new test node output `ProbeIDAC` was implemented in exchange of the old structure `ProbeVrefFE`.

The circuit of the current DAC test node is shown in fig. 6.37. Again the current of the test node output is not routed directly to the test pad. The test node output is generated by a 1-to-1 current mirror with two N-channel FET devices, each with a W/L ratio of 47.56 to 3.50 (4 N-channel devices in parallel). For the measurement all other registers are set to zero in order to minimise the power consumption. Also the system clock is not applied to the chip.

For a DAC test series an automatic register scan is developed. Programming of each possible register value of *Ibuf* is done via the PC connected I^2C-interface. The resulting test current is measured at pad `ProbeIDAC` with a current multimeter[17] and read back via GPIB to the PC. Both devices are controlled by LabVIEW as well as the processing of the measured data.

Test Results

Figure 6.38 shows the measured results of `ProbeIDAC` as a function of the binary register content. The simulation results from a DAC scan of the test circuitry (including the complete DAC, current mirror, output driver and all source followers of the front-end buffer) are also plotted into the diagram (red curve). The simulated current I_{buf} at the output of the current DAC is also depicted in fig. 6.38 (blue line). At register values larger than 192 the measured current already starts to saturate whereas the output of the simulation model is still linear. This discrepancy can only be caused by a mismatch in the model of the current mirror. A problem of the DAC itself can be excluded, because a failure due to switching bits should also be seen at lower register values.

For a detailed characterisation of the current DAC linearity two parameters could be extracted from figure 6.38: the Differential Nonlinearity (DNL) and the Integral Nonlinearity (INL). The DNL is the measured difference $\Delta I_{\mathrm{ProbeIDAC}}$ between the output current of register setting i and $i-1$, whereas i is the register value programmed via I^2C. The results clearly demonstrate how well each $I_{\mathrm{ProbeIDAC}}$ increment matches the last, and indicate whether the DAC is monotonic or not. INL shows the overall distortion from the linearity. Therefore, the dif-

[17] The precision of measurements with this current multimeter is 0.5 µA.

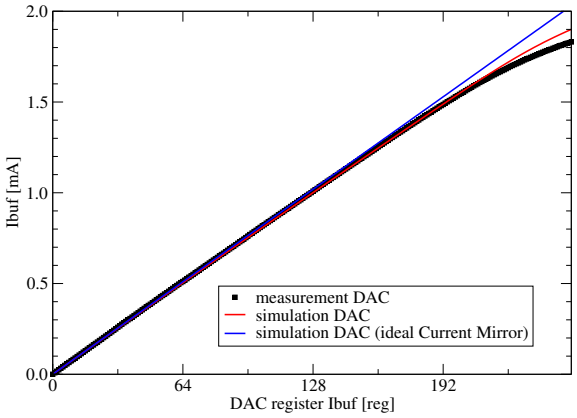


Figure 6.38: Linearity simulation and measurement results of the current DAC *Ibuf*. The results are measured at the test node output `ProbeIDAC` (black squares) whereas the red curve is the output result from a corresponding simulation. For comparison the simulation of the DAC with an ideal current mirror is also plotted (blue).

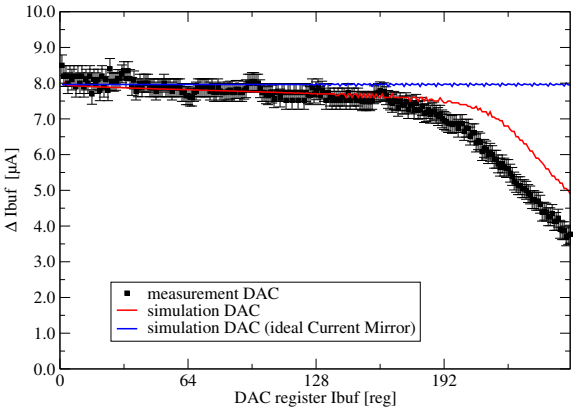


Figure 6.39: Differential Nonlinearity of the current DAC. The simulated behaviour of the DAC with the ideal current mirror (blue) shows a linear behaviour for the whole 8-bit register range. Measured (black) and simulated (red) nonlinearity shows a variation for higher register values.

ference between the measured current $I_{\text{ProbeIDAC}}$ and the best fitted straight line of $I_{\text{ProbeIDAC}}$ is calculated. A DAC is usually acceptable if both, DNL and INL, are less than $\pm 0.5\,\text{LSB}$.

The DNL of the current DAC *Ibuf*, measured at the test pad `ProbeIDAC`, is shown in fig. 6.39 as well as the corresponding simulation outputs. The DNL is within $\pm 0.5\,\text{LSB}$ or $\pm 3.98\,\mu\text{A}$ for the overall register range of the current DAC. A plot of the INL is not given, because it is obvious that there is a huge divergence due to the current mirror and output driver pad problem.

6.5 Process Parameter Variations

In the course of manufacturing Very Large Scale Integration (VLSI) devices it is possible that deviations from the nominal process parameters occur during the different production steps. Depending on the way of variation, the performance can vary from perfect to total failure. Such failures can be found during functional and/or performance tests and these chips will then be sorted out. However, the resulting number of possible good chips will decrease. Because of this, process variations are already taken into account during the development of the circuit. The possible influences are simulated, recognised and – if possible – compensated. Several data sets which contain different variations of parameters are used for the simulation, the so-called *Corner* parameters. The simulated process deviations correspond to variations of the effective gate length respectively to the speed as shown in table 6.13.

To be able to directly measure the deviation from the nominal process parameters, a test structure is implemented on a *Beetle* chip (version 1.5). Section 6.5.1 describes this feature and compares the output results from simulation with different measurements. A technique for an indirect measurement of the process parameter is shown in section 6.5.2.

Description (Gate Length)	Description (Speed)	Exposure	ΔL_{eff} (nm)	ΔL_{eff} (sigma)	Corner
Very Short	Very Fast	85% of Nominal	$-30\,\text{nm}$	$\approx -3.0\,\sigma$	+3.0
Short	Fast	92% of Nominal	$-15\,\text{nm}$	$\approx -1.5\,\sigma$	+1.5
Nominal	Nominal	100% of Nominal	$0\,\text{nm}$	0	0
Long	Slow	115% of Nominal	$+15\,\text{nm}$	$\approx +1.5\,\sigma$	−1.5
Very Long	Very Slow	125% of Nominal	$+30\,\text{nm}$	$\approx +3.0\,\sigma$	−3.0

Table 6.13: Explanation of process parameter variations. ΔL_{eff} is the difference from the nominal L_{eff} which is the effective gate length of a MOS transistor. Short L_{eff} translates into 'fast process', whilst long L_{eff} into 'slow process'. The L_{eff} variation is indicated as percent of the exposure time (85 to 125%) of the manufacturer. The correspondence between exposure and 'fast' or 'slow' process is shown. Column 'Corner' indicates the comparable settings for simulations [Fac02].

6.5.1 Process Parameter Test

The characterisation of the process parameter deviation is usually done by measuring of basic test structures like single NMOS or PMOS transistors, capacitors or resistors on a chip. To measure the characteristic output behaviour of these devices by an external setup, an enormous effort has to be applied to reduce external influences to the measurement (i.e. additional noise of the probe needles, capacitances of the readout, external amplification of the signals).

The implementation of the test structure on the *Beetle* integrates a simple and easy to use measurement possibility for the user. The Process Parameter Test (PPT) is designed as a chain of 398 inverters. With this structure the eigenfrequency of the inverter chain can be easily measured and be set into relation to the simulated values. Figure 6.40 shows the schematic of this structure, located in the upper right corner of a *Beetle1.5*. It has only one input to

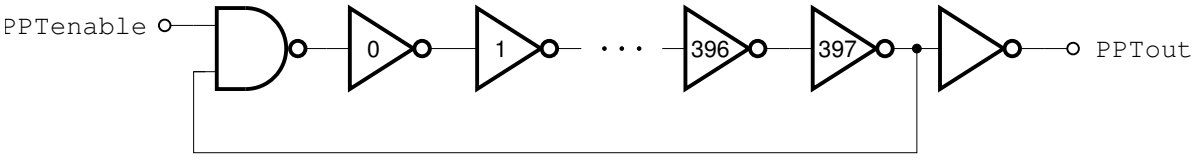


Figure 6.40: Schematic of the *Beetle1.5* Process Parameter Test.

activate the oscillation and one output to measure the frequency. The structure is powered via the LVDS comparator output driver supply `VddCPT` and `GndCPT`. For measuring of the ring oscillator output frequency (`PPTout`) pad `PPTenable` has to be set to 2.5 V.

The test structure eigenfrequency of a *Beetle1.5* chip from wafer KSMNKAT, measured at different temperatures, is shown in fig. 6.41. The variation of the chip temperature and the simultaneous readout of the test structure was performed inside a climatic exposure test cabinet. To minimise disturbing actions to the measurement only the supply voltage of the test structure was applied. All other *Beetle* components were therefore turned off. The output frequency was measured with a digital oscilloscope. Reading the data from the oscilloscope as well as the programming of the climatic chamber was done with a test program, written with LabVIEW [NAT].

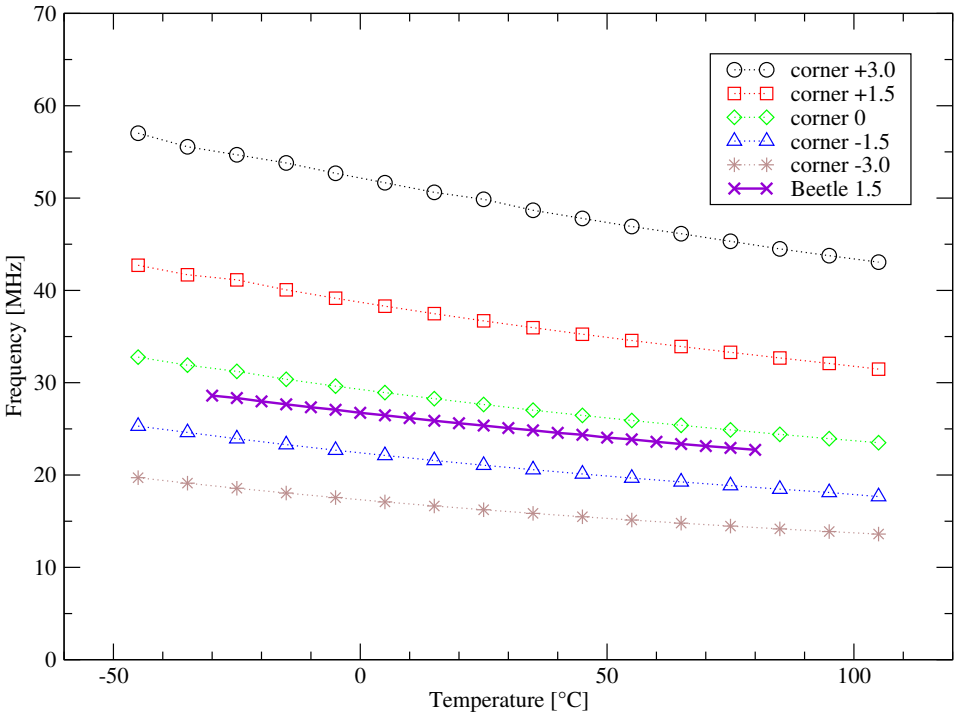


Figure 6.41: Simulation and test results of the *Beetle1.5* Process Parameter Test. The dashed lines are simulation results for different *Corner* parameters (−3.0 to +3.0) while the solid line is from a measurement of a *Beetle1.5* chip diced from wafer KSMNKAT.

To compare the measurements, the results of five simulations with different process parameters are also shown in fig. 6.41. For an exact calculation of the output frequency the following empiric function is obtained from a *Corner* and temperature simulation:

$$f = (10^{-4}T^2 - 6.95 \cdot 10^{-2}T + 29.68) \cdot e^{(-4 \cdot 10^{-7}T^2 + 10^{-4}T + 0.1834) \cdot corner} \tag{6.19}$$

with:

f	–	output frequency of Process Parameter Test [in MHz],
T	–	chip temperature [in ℃],
corner	–	process parameter variation.

The accuracy of equation 6.19 is better than 1.6% within a process parameter variation of $-3.0 \leq Corner \leq +3.0$ and a temperature range of $-45℃ \leq T \leq +105℃$.

The influence on the frequency due to process parameter fluctuations during the production of the wafers are much stronger than those due to temperature variations. Therefore the measurement of this test structure can be used to qualify the deviation of process parameters during a mass production test of different wafers. First results of process parameter deviations over whole *Beetle* wafers are presented in section 6.9.4 about the mass production tests.

6.5.2 Test Channel

Measuring the deviation of the nominal process parameters with the Process Parameter Test is only possible for chip version *1.5*. For chip versions *1.4* and before the process parameter

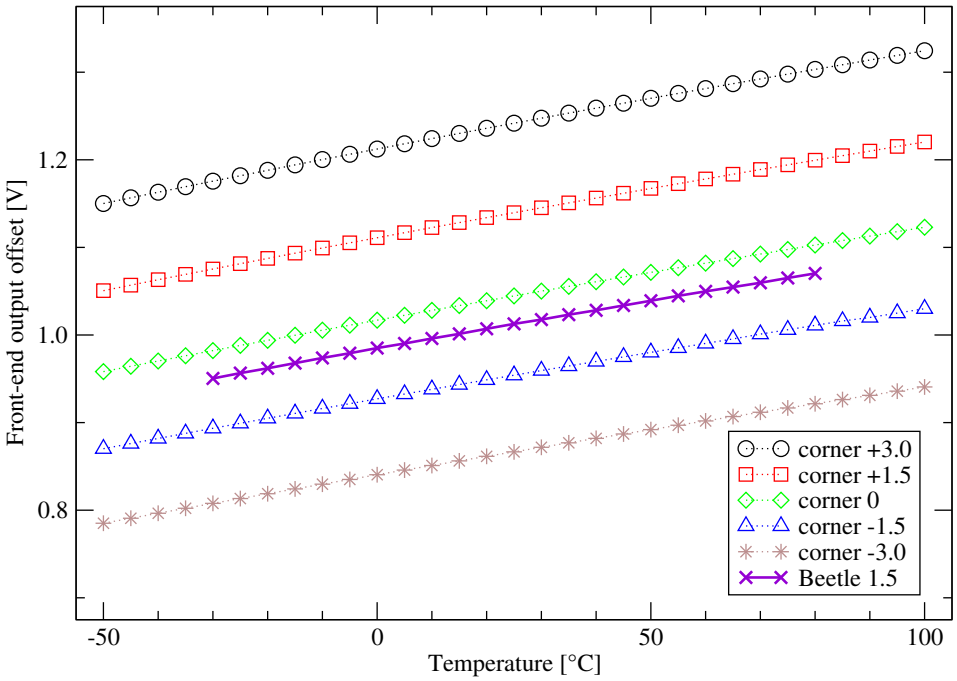


Figure 6.42: Measurement and simulation of the front-end output offset. The dashed lines are simulation results for different *Corner* parameters (from −3.0 to +3.0) and temperatures (from −50°C to +100°C) while the solid line is from a measurement of a *Beetle1.5* chip diced from wafer KSMNKAT.

can be determined by measuring the offset voltage of the analogue front-end output. But only one of the 130 front-end channels output nodes of the *Beetle* chip, namely the test channel output, is directly accessible via the pad `TestOutput` (cf. figure 5.1).

Figure 6.42 shows results from front-end simulations for different temperatures and *Corner* parameters. The output voltage shows again a smaller dependency on temperature variations and a larger offset variation due to *Corner* parameter modifications. The front-end settings for all simulations are set to the standard values[18] as described in *The Beetle Reference Manual* in appendix C. Furthermore, the output voltage, measured on the same chip from which already the data for the Process Parameter Test has been taken, are plotted into the simulation diagram. The comparison between simulation and measurement shows a tendency to a negative *Corner* value (*Corner* ≈−0.5) for wafer KSMNKAT. This result is also in good agreement with the measured shift of the *Corner* parameter from fig. 6.41.

An empiric function (eq. 6.20) describing the analogue output voltage at pad `TestOutput` can be extracted from simulation results.

$$V_{\mathrm{FE}} = (-10^{-5}\,corner - 7\cdot 10^{-4})\cdot T^2 + (2\cdot 10^{-2}\,corner + 1.1)\cdot T + (61.8\,corner + 1\,021) \quad (6.20)$$

with:

V_{FE}	–	Front-end DC output voltage [in mV], measured at test node `TestOutput`,
T	–	chip temperature [in °C],
corner	–	process parameter variation.

[18] $Ipre = 600\,\mu A$, $Isha = 80\,\mu A$, $Ibuf = 80\,\mu A$, $Vfp = 0\,V$ and $Vfs = 0\,V$

Within a temperature range of −50℃ to +100℃ and a *Corner* parameter variation between −3.0 and +3.0 the deviation of equation 6.20 is less than 0.8%.

6.6 Total Dose Irradiation Test

Between October 2001 and February 2005 three total dose irradiation tests were performed at the X-ray irradiation facility of CERN's microelectronic group [Mic01]. In total 13 readout chips and 4 front-end test chips have been irradiated. Table 6.14 summarises the different *Beetle* versions and accumulated doses. In the following the details of the experiment and measured results from February 2005 irradiation test will be presented[19].

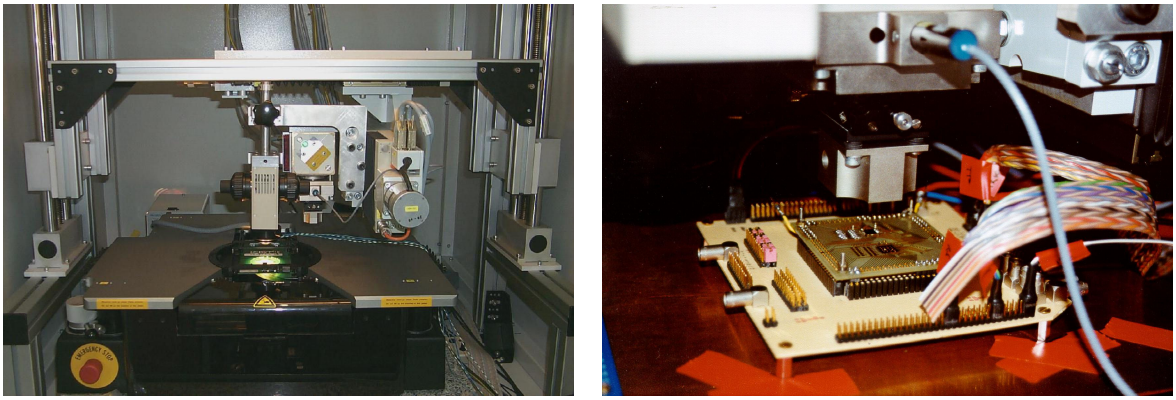
Test run	Irradiated chip version	Accumulated dose [Mrad(SiO_2)]	Annealing applied
October 2001	*Beetle1.1*	10	no
	Beetle1.1	10	yes
	Beetle1.1	30	yes
	Beetle1.1	45	no
	BeetleFE1.1	10	no
	BeetleFE1.1	10	no
	BeetleFE1.2	10	no
	BeetleFE1.2	10	no
October 2002	*Beetle1.2*	10	no
	Beetle1.2	10	no
	Beetle1.2	10	no
	Beetle1.2	30	no
February 2005	*Beetle1.3*	10	yes
	Beetle1.4	10	no
	Beetle1.5	10	yes
	Beetle1.5	12	no
	Beetle1.5	130	yes

Table 6.14: Accumulated dose for various *Beetle* chips.

6.6.1 Test Setup

An overview of the irradiation setup with the X-ray tube in the middle is shown in fig. 6.43(a). The tube is water-cooled and the power supply is adjustable from 20 kV to 60 kV. It is possible to focus the beam from up to 1 cm in diameter down to a spot of 100 µm and to vary the dose rate between 10 and 800 krad(SiO_2)/s. A detailed view of the device under test is shown in separation mode in fig. 6.43(b). The distance between collimator exit window above the chip and the surface of the chip was approximately 1 cm during irradiation and the beam diameter was 1 cm. The alignment of the beam spot to the centre of the chip was done with a laser system, installed in the irradiation cabinet.

[19] Detailed results from previous irradiation tests are published [LHC02], [Bau03] and [LHC04].



(a) Test facility (b) Device under test setup

Figure 6.43: Total dose irradiation test facility of CERN's microelectronics group (a) and the test board with a mounted *Beetle* chip positioned underneath the collimator exit window (b). The distance between collimator exit window and surface of the *Beetle* chip was approximately 1 cm during irradiation.

The characterisation of the main front-end parameters like rise and peak time, gain, remainder 25 ns after peak and undershoot were measured for each chip before irradiation. Also the chip noise, pipeline homogeneity, readout baseline and power consumption were characterised. All chips were irradiated in one step to the final dose without any further characterisation in between. Final measurements were performed after irradiation and, if the chip was also annealed, after annealing.

Each device under test was powered during irradiation and programmed with the standard settings described in table C.14. With a frequency of 1.1 MHz internal test pulses were injected into different channels, triggered and read out to control the correct operation while the chip was irradiated. Additionally the power consumption of the *Beetle* chips was monitored during irradiation.

The X-ray tube has been operated at an anode voltage of 40 kV and a tube current of 60 mA. The relation between dose rate and tube current ($5\,\mathrm{mA} \leq I_{\mathrm{tube}} \leq 60\,\mathrm{mA}$) for a distance of 1 cm and a voltage of 40 kV is given by [Mic05]:

$$\dot{D}_{40\mathrm{kV},1\mathrm{cm}}\,[\mathrm{rad(SiO_2)/min}] = 92 + 631.30 \cdot I_{\mathrm{tube}}\,[\mathrm{mA}] \tag{6.21}$$

6.6.2 Test Results

Annealing Behaviour

Three out of five chips from the February 2005 irradiation runs have been annealed inside a climatic exposure test cabinet for more than 18 days. The temperature has been kept constant at 100°C. The remaining chips were not subjected to enhanced annealing. During the annealing procedure the power consumption of the chips has been monitored as well as the frequency response of the Process Parameter Test structure (cf. section 6.5.1). Figure 6.44 shows the output frequency of two *Beetle1.5* chips as a function of the annealing time – one has been irradiated to an accumulated dose of 10 Mrad (black circles) while the other chip has been irradiated up to 130 Mrad total dose (red squares). After 10 days of heating, no further significant

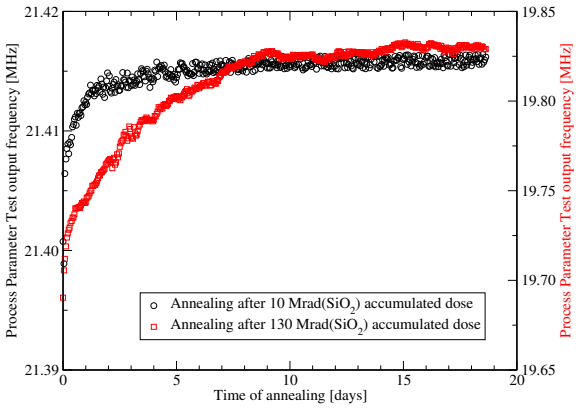


Figure 6.44: Frequency response of the Process Parameter Test while two irradiated *Beetle* chips were annealed in a climatic exposure test cabinet at a constant temperature of 100°C. One chip was irradiated up to an accumulated dose of 10 Mrad (black) whereas the second chips was irradiated up to 130 Mrad (red).

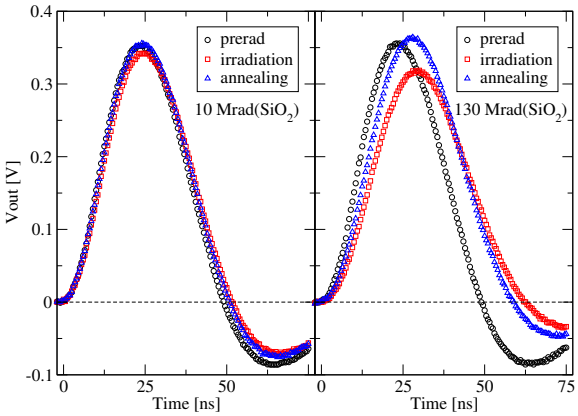


Figure 6.45: Pulse shape variation of two *Beetle1.5* chips before (black) and after (red) irradiation as well as after annealing at 100°C (blue). In the left diagram the chip was irradiated up to a total dose of 10 Mrad and up to 130 Mrad in the right plot. All measurements were done with a capacitive input load C_p of 3 pF.

changes of the output frequency were measured. A variation in the total power consumption of each chip was not observed.

Pulse Shape

Figure 6.45 shows the pulse shapes of two *Beetle1.5* chips before and after irradiation (black and red) as well as after the annealing procedure (blue). The chip in the left diagram was irradiated up to a total dose of 10 Mrad whereas the chip in the right diagram was irradiated up to 130 Mrad. The shown pulse shapes were measured at a capacitive input load C_p of 3 pF.

Up to an accumulated dose of 10 Mrad, the peaking time t_p increased by 1 ns (4.4%) and the peaking voltage V_p decreased by 3.9%. After the annealing process the pulse shape has almost regenerated to the original pulse shape before irradiation. A significant pulse shape change can be determined at the *Beetle* chip that was irradiated up to 130 Mrad. The pulse parameter t_p increased by 5 ns (22.2%) and V_p decreased by 10.7%, whereas the remainder 25 ns after peak R changed from 0.7% to 18.4%. After annealing of this chip the pulse shape is still different from the original one. Compared to the pre-irradiated pulse shape the peaking voltage has now increased slightly whereas the peaking time, respectively the rise time, is still larger than before. A detailed summary of all measured pulse shape characterisation parameters for both chips and different C_p is quoted in table 6.15.

Readout Baseline

One of the main tasks of the February irradiation run was the check of the radiation hardness of the design improvements between *Beetle* version *1.3* and *1.5*, especially the new analogue pipeline of a *Beetle1.5*. Figure 6.46 shows the analogue readout baseline of three *Beetle* chips. In the left and middle diagram the *Beetle* version *1.3* and *1.5* are shown, both irradiated up to

Pulse shape parameter	C_p [pF]	10 Mrad(SiO_2) prerad	10 Mrad(SiO_2) irrad	10 Mrad(SiO_2) anneal.	130 Mrad(SiO_2) prerad	130 Mrad(SiO_2) irrad	130 Mrad(SiO_2) anneal.
peaking time t_p [ns] $(0-100\%)$	3.00	22.5±0.5	23.5±0.5	23.0±0.5	22.5±0.5	27.5±0.5	26.0±0.5
	9.86	23.0±0.5	25.0±0.5	24.5±0.5	23.0±0.5	28.5±0.5	28.0±0.5
	18.15	25.5±0.5	26.0±0.5	26.0±0.5	25.5±0.5	31.5±0.5	29.5±0.5
	36.08	26.5±0.5	28.5±0.5	27.5±0.5	26.5±0.5	33.5±0.5	32.5±0.5
rise time t_r [ns] $(10-90\%)$	3.00	13.3±0.3	14.5±0.3	14.3±0.3	13.0±0.3	16.5±0.3	15.7±0.3
	9.86	14.0±0.3	15.5±0.3	15.3±0.3	14.0±0.3	17.5±0.3	17.0±0.3
	18.15	15.8±0.3	16.0±0.3	16.0±0.3	15.0±0.3	18.5±0.3	18.0±0.3
	36.08	16.0±0.3	17.5±0.3	17.3±0.3	16.0±0.3	20.0±0.3	19.5±0.3
peaking voltage V_p [mV]	3.00	351±19	337±17	349±17	351±18	313±21	358±19
	9.86	318±17	309±17	317±21	317±21	278±16	318±18
	18.15	284±21	271±23	282±26	281±23	243±22	275±24
	36.08	224±28	215±26	223±26	221±27	187±26	215±31
remainder R [%] 25 ns after peak	3.00	0.7±1.2	5.9±1.3	4.7±1.2	0.7±1.2	18.4±1.4	15.5±2.1
	9.86	3.0±1.5	11.0±1.5	11.4±1.7	3.1±1.8	23.9±2.3	21.1±2.1
	18.15	11.8±2.2	17.8±2.1	16.5±2.2	12.0±2.3	31.1±3.5	25.5±3.1
	36.08	22.8±3.1	27.8±3.0	28.8±3.4	22.9±3.0	40.5±4.5	36.8±3.9

Table 6.15: Pulse shape characterisation parameters peaking time t_p, rise time t_r, peaking voltage V_p and pulse remainder R for different capacitive input loads C_p and two different *Beetle1.5* chips. One chips was irradiated up to an accumulated dose of 10 Mrad(SiO_2), the other up to an accumulated dose of 130 Mrad(SiO_2). For each chip all parameters are quoted before irradiation (left column), after irradiation (middle column) and after 18 days of annealing at 100°C (right column).

a total dose of 10 Mrad. The right diagram shows again a chip version *1.5*, this time irradiated up to an accumulated dose of 130 Mrad. In each diagram the pedestal shift before and after irradiation is quoted for each readout channel (black circles) together with the offset shift before irradiation and after annealing (red squares). It is obvious that there is an enormous variation of the *Beetle1.3* pipeline under irradiation, even more than for the *1.5* chip at a total dose of 130 Mrad. This is a clear confirmation that the gate capacitance of an n-FET over n-well shows less performance degradation under irradiation compared to an n-FET without an n-well underneath (as used in *Beetle* version *1.3*).

Noise

The goal of this test is the characterisation of the Equivalent Noise Charge behaviour under irradiation. Therefore, the measurement procedure is set-up and implemented in the same way as already described in section 6.3.7. The data acquisition is done for a fixed pipeline column number. Table 6.16 lists the results from a *Beetle1.3* chip, irradiated up to a total dose of 10 Mrad whereas table 6.17 lists the results of two version *1.5* chips with a total dose of 10 Mrad and 130 Mrad. For each chip the ENC is quoted before and after irradiation as well as after annealing. The corresponding ENC plots for both *Beetle1.5* chips are shown in fig. 6.47.

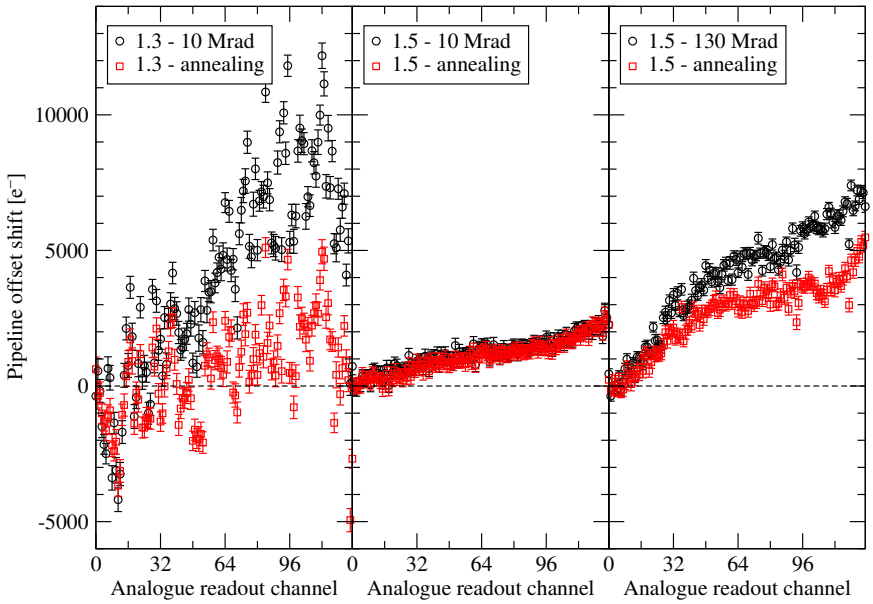


Figure 6.46: Analogue readout offset after irradiation and annealing of three different *Beetle* chips. In each diagram the difference of the readout baseline before and after irradiation is shown (black) as well as the difference of the baseline before irradiation and after annealing (red). The left and middle diagram shows a *Beetle1.3* and *Beetle1.5* with an accumulated dose of 10 Mrad(SiO_2) each, on the right there is again a *Beetle1.5* but with an accumulated dose of 130 Mrad(SiO_2).

Integral dose	Equivalent Noise Charge
prerad	$(541 \pm 25)\,e^- + (50.8 \pm 1.2)\,e^-/pF \cdot C_p$
10 Mrad(SiO_2)	$(563 \pm 28)\,e^- + (51.2 \pm 1.3)\,e^-/pF \cdot C_p$
annealing	$(553 \pm 27)\,e^- + (51.0 \pm 1.3)\,e^-/pF \cdot C_p$

Table 6.16: Measured Equivalent Noise Charge of a *Beetle1.3* chip under irradiation.

Integral dose	Equivalent Noise Charge
prerad	$(523 \pm 10)\,e^- + (50.0 \pm 0.5)\,e^-/pF \cdot C_p$
10 Mrad(SiO_2)	$(548 \pm 12)\,e^- + (50.4 \pm 0.7)\,e^-/pF \cdot C_p$
annealing	$(532 \pm 12)\,e^- + (50.2 \pm 0.7)\,e^-/pF \cdot C_p$
prerad	$(527 \pm 10)\,e^- + (50.2 \pm 0.6)\,e^-/pF \cdot C_p$
130 Mrad(SiO_2)	$(598 \pm 21)\,e^- + (51.8 \pm 1.2)\,e^-/pF \cdot C_p$
annealing	$(582 \pm 20)\,e^- + (51.1 \pm 0.9)\,e^-/pF \cdot C_p$

Table 6.17: Measured Equivalent Noise Charge of two *Beetle1.5* chips for different dose levels.

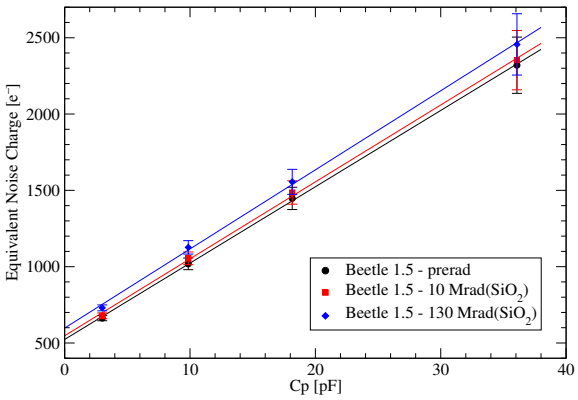


Figure 6.47: Equivalent noise charge as function of load capacitance and dose.

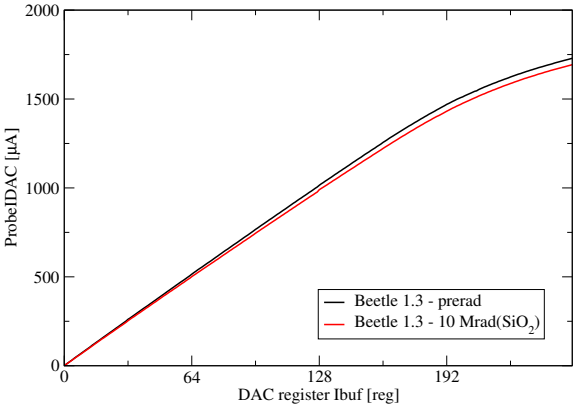


Figure 6.48: Output of a *Beetle1.3* current DAC (*Ibuf*) before and after irradiation.

Within the error of the measurement, the ENC slope is unchanged for both chip versions and dose levels. An increase of the ENC offset of approximately 25 e^- has been observed after 10 Mrad which decreased again after annealing. For the *Beetle* with a total dose of 130 Mrad the ENC offset is significantly higher (+70 e^- or 13.4%) but showed only a slight improvement after annealing (still 55 e^- or 10.4% higher than the initial offset).

Test Structure

The goal of this measurement was the characterisation of the internal current DAC before and after irradiation. With the aid of the test structure output `ProbeIDAC` of a *Beetle1.3* chip the output current of the internal DAC *Ibuf* is mirrored to a test pad for external measurements (cf. section 6.4.2). For this test all internal control and bias registers are set to zero and no clock or trigger signals were applied. The output is measured for all 256 register values with a sensitive current meter.

Figure 6.48 shows the results for the DAC scan before (black) and after irradiation (red) with an accumulated dose of 10 Mrad. The measurement results after the irradiation procedure expose a slightly slope of the DAC current output characteristic than before. No significant changes can be determined for the Differential Nonlinearity. A possible explanation is a degradation of the common current source (cf 5.12.1), that provides a constant reference current for all current DACs. With that assumption a decrease of 2.5% ± 0.2% after 10 Mrad accumulated dose from the nominal value of the current source output (126.2 µA) is calculated.

Input Charge Rate

A change of the preamplifier feedback resistor *Vfp* under irradiation would strongly influence the charge rate behaviour of the chip. Therefore the front-end behaviour for high input charge rates has been measured for different accumulated doses. Test setup and measurement method are the same as described in section 6.2.2. All measurements were performed with *Beetle* chips of version *1.5*. The measured results are also valid for chip versions *1.3* and *1.4* since the same front-ends are implemented on these chips.

The front-end output ratio of an external test charge (22 345 e^-) with and without the DC current is plotted in fig. 6.49 for 0, 10 and 130 Mrad accumulated dose and for positive

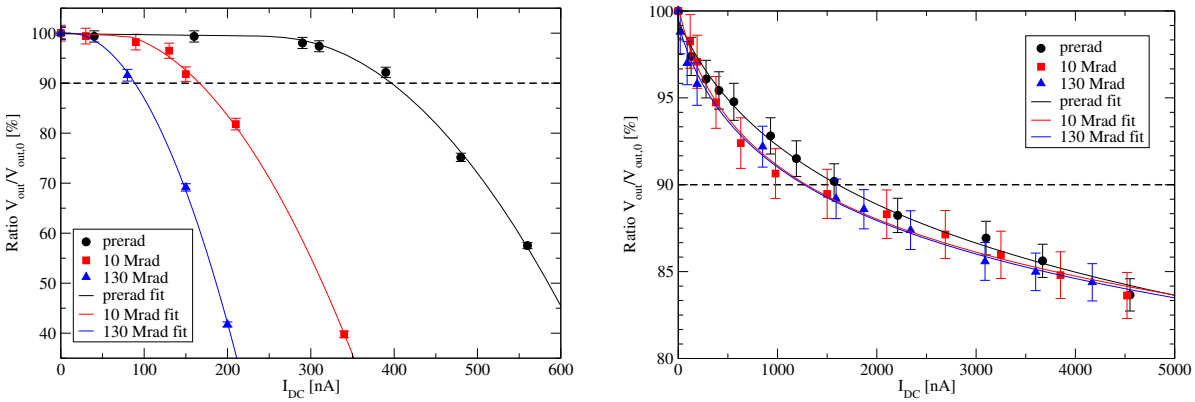


Figure 6.49: Front-end output under irradiation as a function of different input DC currents. For all measurements a signal with a defined charge of 22 345 e^- is coupled into the chip. The signal ratio of the front-end output voltage with a certain DC input current (V_{out}) and without a DC current ($V_{out,0}$) is plotted on the ordinate axis. In the left diagram the DC current is flowing into the front-end which corresponds to a positive input charge. In the right diagram the current is flowing out of the chip which is equal to a negative input charge at the front-end input. The accumulated dose rates for this measurement are 0, 10 and 130 Mrad.

Integral dose	Maximum DC input current [nA]	
	positive charge	negative charge
prerad	$397\ ^{+7}_{-8}$	$1\,609\ ^{+165}_{-153}$
10 Mrad(SiO_2)	$166\ ^{+6}_{-6}$	$1\,290\ ^{+154}_{-140}$
130 Mrad(SiO_2)	$89\ ^{+4}_{-4}$	$1\,268\ ^{+153}_{-139}$

Table 6.18: Maximum DC input current of the *Beetle* for three different accumulated doses.

respectively negative charges. Again, the maximum charge rate is defined as the value at which the front-end output degradation is more than 10% of the nominal signal output level. In the measurement setup this corresponds to a ratio level of 90% (marked as dashed red lines).

The predicted degradation of the maximum charge rate under irradiation is clearly visible in both diagrams. This is a direct indication that the feedback FET of the preamplifier, which acts as variable resistor in the high ohmic region[20], is very sensitive to defects from irradiation.

Table 6.18 summarises the maximum DC currents, which are extracted from the best fitted values of fig. 6.49. The maximum input charges for these currents are calculated with equation 6.7. Assuming the worst case chip operation parameters at LHCb (10 Mrad accumulated dose after 10 years of operation and a channel strip occupancy of 10%), this leads to a maximum positive input charge of 259 ke^-. This is still two times higher than the required maximum input charge of the *Beetle* chip [Sch01] and will not induce any restrictions to the use of the *Beetle* chip in the LHCb experiment.

[20] The specification of an exact resistance value is not possible, because the feedback resistor is not constant. It depends strongly on the voltage difference between front-end input and output. The normal value is in the order of 200 kΩ to 600 kΩ for *Vfp*=0 V.

6.7 Single Event Upset Irradiation Test

Due to the proximity of the Vertex Locator and the Silicon Tracker to the interaction point and the beam pipe, the readout chips are subjected to high fluences of ionising particles. Radiation induced effects may temporarily or permanently affect or inhibit the normal operation mode of the electronics (cf. chapter 4). In this section a test of the robustness against Single Event Upsets (SEU) of the *Beetle* chip as well as the results of this test are described.

The SEU irradiation test was performed at the Proton Irradiation Facility (PIF) of the Paul Scherrer Institute [PSI] in February 2004. Three *Beetle1.3* chips were irradiated with 65 MeV protons with an average particle flux of $1.5 \cdot 10^9\,\mathrm{p/(cm^2 \cdot s)}$, which corresponds to a dose rate of approximately 102 rad/s. The SEU testability of the *Beetle* chip is described briefly, whereas the test results and the summary are discussed afterwards.

6.7.1 SEU Testability of the *Beetle*

In case of an SEU the deposited charge was sufficient to flip the value of a digital memory. SEUs normally refer to bit flips in static or dynamic RAM circuits or flip-flops. In some rare cases an SEU may also directly affect digital signals in logic circuits. The SEU is particularly dangerous for the configuration registers and the state machine of the control logic. In worst case will lead to the complete loss of the functionality of the chip. Although it does not prevent the generation of an SEU, introducing redundancy into the design of the digital circuits, the sensitivity to SEU is drastically decreased. The possible effects to the digital logic are greatly suppressed by implementing triple-redundancy with majority voting elements into the circuitry.

The parts on the *Beetle* chip, which are sensitive to SEUs, are the digital memory devices realised as D-type flip-flops. These parts can be classified into three groups (see table 6.19):

Quasi-static, non-redundant devices
: They are used as mask registers for the test pulse and the comparator to define individual channel settings. There is no built-in redundancy for these devices. Instead the parity of all mask registers is encoded and flagged in the analogue readout header of a triggered event. In case of a bit-flip in these registers, the registers have to be reprogrammed manually via the I^2C-interface to correct the wrong settings.

Quasi-static, redundant devices
: They are used in all DAC registers and form the *Beetle* configuration registers. The redundancy is implemented in majority voting flip-flops with a self-triggered correction mechanism, also called *self-triggered triple-redundant flip-flops* (cf. section 5.11.3). They are programmed only when a register is addressed by the I^2C-interface. In case of inconsistency due to an SEU between one of the three sub-flip-flops of the device in fig. 5.42 the correction mechanism automatically reprograms all three sub-flip-flops with the correct information within less than 2 ns.

Clocked devices
: They are used within the pipeline control logic and I^2C-interface to form the state registers of finite state machines, the derandomising buffer, the shift-registers and counters as well as the shift-registers of the analogue readout multiplexer. Except for the multiplexer, the redundancy is again done by *triple-redundant flip-flops* (cf. section 5.11.3)

Position of flip-flop	Standard flip-flop	Triple redun-dant	Self-triggered correct.	SEU counter	Parity-Flag
Quasi-static, non-redundant devices:					
Comparator *CompChTh*	640	—	—	640	ParCompChTh
Comparator *CompMask*	128	—	—	128	ParCompMask
Test pulse *TpSelect*	129	—	—	129	ParTpSelect
Test pulse pad	1	—	—	—	
Bias (FE)	1	—	—	1	
Quasi-static, redundant devices:					
Configuration registers	—	32	32	96	
Front-end DACs	—	80	80	240	
Back-end DACs	—	48	48	144	
Clocked devices:					
Digital logic circuitry	—	521	—	—	
Comparator	—	256	—	—	
Multiplexer	138	—	—	—	
Total Sum	1 037	937	160	1 378	

Table 6.19: Overview of all flip-flops of a *Beetle* chip. The first column gives the position of the flip-flops on the *Beetle*. Column two to four give the number of flip-flops, which form these building blocks. Here, the triple-redundant flip-flops are counted as one device. The column SEUcounter depicts the number of flip-flops contributing to the SEU counter. The last column indicates if the flip-flops are encoding a parity bit in the analogue header.

which are clocked with the sampling clock or a fraction[21] of it. Again, the status of each of the three sub-flip-flops is automatically refreshed.

The shift-registers of the multiplexer are automatically reset at the beginning of each readout. Therefore an SEU flip affects only one readout event.

For monitoring purpose and SEU cross section calculation an internal 8-bit triple-redundant counter is integrated in the *Beetle*. It indicates the number of occurred SEUs during operation. The output is readable via the read-only register *SEUcoutner*. In addition, the two Least Significant Bits (LSBs) are flagged in the header of each analogue readout, which allows a fast monitoring of SEUs during readout. All DAC, configuration settings and mask registers are contributing to the counter. The flip-flops used in the logic control circuitry are not taken into account. Table 6.19 summarizes the numbers of flip-flops in the *Beetle* chip. In total, there are 3 848 ($= 1\,037 + 3 \times 937$) flip-flops integrated in the chip. 1 378 out of these contribute to the SEU counter. Thus, for 36% of the total amount of flip-flops, an unexpected output change due to an SEU can be detected by monitoring the status of the *SEUcount* register.

[21] We can assume that after 16 consecutive readouts and 36 clock cycles per readout event the derandomising buffer is completely refreshed. This corresponds to 1/576 of the nominal clock frequency.

Information about a change in the mask registers content *TpSelect*, *CompChTh* and *CompMask* can be obtained in two ways: either by detecting a change of the parity bit information in the analogue readout header or by reading back the register information via the I^2C-interface. For all other DAC and configuration registers, an SEU induced bit flip can only be detected by the change of the content of register *SEUcount*.

6.7.2 SEU Test Setup

A certain charge has to be deposited in order to create an SEU in the sensitive volume[22] of a flip-flop (cf. section 4.3.1). Since in silicon 3.6 eV are needed to create an electron-hole pair, the minimum charge relates to the energy by $Q_{\text{crit}} = e \cdot E_{\text{crit}}/3.6\,\text{eV}$, which yields with eq. 4.11 to

$$Q_{\text{crit}} = \frac{e \cdot \text{LET}_{\text{crit}} \cdot \rho_{\text{Si}}\, d}{3.6\,\text{eV}} \tag{6.22}$$

with:

LET_{crit} – critical Linear Energy Transfer [in $\text{eV}\,\text{cm}^2\,\text{mg}^{-1}$],
d – SEU sensitive depth for a flip-flop [in µm],
ρ – density of the material [in g/cm^3], for silicon $\rho_{\text{Si}} = 2.33\,\text{g/cm}^3$,

For a depth d of 0.5 µm [Fac99a] and a critical LET of $5.4\,\text{MeV}\,\text{cm}^2\,\text{mg}^{-1}$ [Fac99a], the minimum charge Q_{crit} is $175\,\text{ke}^- = 28\,\text{fC}$ and the critical energy $E_{\text{crit}} = 0.63\,\text{MeV}$.

To create an Single Event Upset, potential candidates are *heavy ions* or *hadrons* such as protons, pions or neutrons (cf. section 4.3.1). This Single Event Upset test has been performed at the NE-B[23] line of the 'Injector 1' cyclotron of the Paul Scherrer Institute, using 65 MeV protons[24]. The irradiation took place in air and at an ambient temperature of ≈ 30°C. Figure 6.50 shows an overview of the test setup at the irradiation facility. Inside the experimental area (right to the shielding wall), an Inner Tracker hybrid with three *Beetle1.3* chips is mounted in front of the exit window of the proton beam. The beam spot has a circular profile with a diameter of up to 9 cm and an uniformity of >90% for the inner 5 cm diameter, which covers therefore all three *Beetle* chips on the hybrid (distance from left to right *Beetle* chip is ≈ 4 cm). A picture that images the DUTs is shown in fig. 6.51. A side view photography of the setup inside the radiation area is depicted in fig. 6.52.

As the readout hybrid is located directly in the beam, only radiation hard components are allowed here. Therefore, the *Beetle* chips are the only active devices on the hybrid. Other components are the passive signal line termination resistors and blocking capacitors that stabilize the power supply voltages and the bias nodes of the *Beetle*. All chips are biased with the nominal operating settings (cf. table C.14). A 40 MHz system clock is applied to the chips during irradiation and internal test pulse signals are injected to the front-end. The chips are triggered and then read out. All analogue readout ports of the three chips are connected via an adapter card to a digital oscilloscope outside the shielding wall. Via the same adapter card all digital service signals are routed to the *Beetle* chips. *Clock*, *Trigger*, *Testpulse* and *Reset* are generated by the digital pattern generator DG2020A [TEK], whereas the I^2C-interface of the *Beetle* is controlled by a Laptop. As the adapter card is located close to the proton beam

[22] $1 \times 1 \times 0.5\,\mu\text{m}^3$ [Fac99a]
[23] The NE-B line and the experimental area is also known as Proton Irradiation Facility (PIF).
[24] The SEU cross section for high-energy hadrons is roughly energy-independent above some 30 MeV and drops rapidly below that energy. For a suitable test, protons with an energy of 60-200 MeV have to be used to irradiate devices [Huh00].

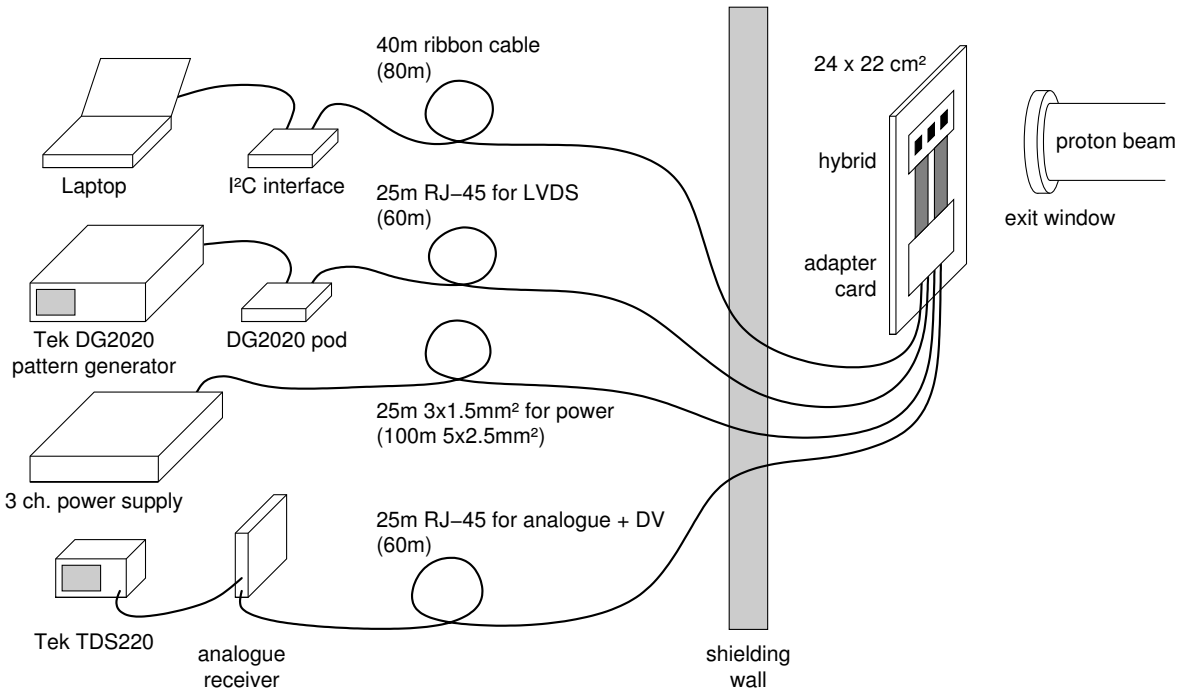


Figure 6.50: Scheme of the SEU irradiation setup at the Proton Irradiation Facility (PIF). The hybrid with all *Beetle* chips and the cable adapter card are behind the shielding wall inside the radiation facility. All other components are located outside the wall. All cable lengths for the setup are indicated. The maximum lengths tested in the laboratory are quoted in brackets.

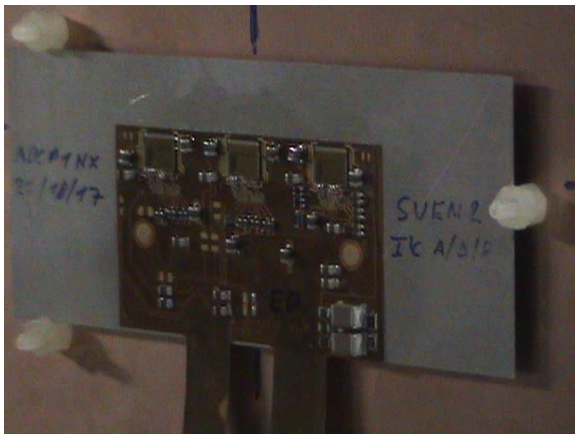


Figure 6.51: Target hybrid with 3 *Beetle* chips for SEU irradiation test.

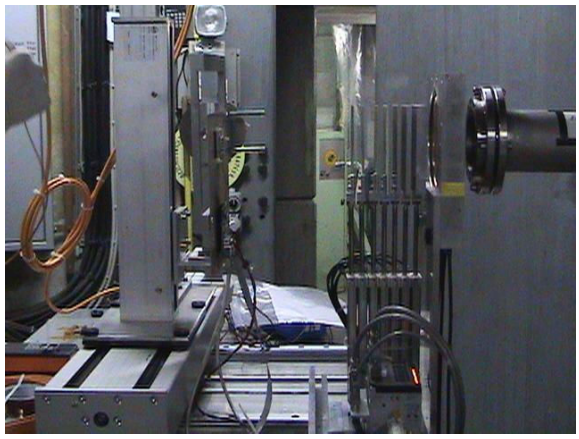


Figure 6.52: Setup of the SEU test inside the radiation facility. From right to left it shows the exit window of the proton beam, followed by an ionisation chamber and the beam degraders. The hybrid with the *Beetle* chips is mounted to the sample frame on the left side.

and thus high flux of ionising radiation are encountered, no active components are mounted here. Hence, all signals are routed one-to-one from the flexible capton cable of the hybrid to the long-distance cables. As a result the *Beetle* chips have to drive the analogue readout signals plus the digital signal *DataValid* over a distance of 25 m to the monitoring devices.

The measurement procedure foresaw a readout of the *SEUcounter* register of all three chips every 15 seconds. The register content can be interpreted directly as the total number of SEUs occurred in the $3 \times 1\,378 = 4\,134$ monitored static flip-flops of the three *Beetle* chips. Additionally, all non-triple-redundant flip-flops of the mask registers are read out every minute and are compared with the original data set. A discrepancy is interpreted as an SEU in the mask registers. With both on-line monitoring possibilities an upset can be localised to one of the two groups of quasi-static devices.

6.7.3 Results

The three *Beetle* chips were irradiated with 64.52 MeV protons for nearly 11 hours, except for a short time period of 40 minutes, where the energy of the protons was 20.24 MeV. The achieved accumulated dose was (7.7 ± 0.3) Mrad which corresponds to an accumulated fluence of $(5.3 \pm 0.2) \cdot 10^{13}\,\mathrm{p/cm^2}$. Figure 6.53 shows the accumulated dose respectively the fluence as a function of the irradiation time.

Single Event Upset Measurement and Cross Section Results

In total 4 upsets in the registers of the three chips were detected by the SEU counters. They all appeared in a time window of 75 minutes. Within this period the chips accumulated a dose of (0.923 ± 0.033) Mrad. Three flips were found in the mask registers, the fourth was detected in one of the triple-redundant self-triggered DAC or configuration registers. At least one SEU was found on each chip. For better understanding of the distribution, the moment of the four SEU detections are marked into fig. 6.53, too.

To calculate the probability of this SEU distribution a Monte Carlo simulation has been set up. For this simulation it is assumed that only protons with an energy of 65 MeV contributed to the creation of SEUs. Therefore, the accumulated dose for the simulated irradiation run is only 6.647 Mrad. Further it is assumed that the SEUs have an exponential distribution for the accumulated dose between two independent events. The result of the simulation is shown in fig. 6.55. It shows the probability of a burst of exact 4 SEUs (respectively more than 4) within an irradiation window of 0.923 Mrad as a function of the mean accumulated dose between two SEUs, if the total dose is 6.647 Mrad. The maximum probability is – as expected – at $6.647/4 = 1.662$ Mrad. For the measured SEU distribution the probability to detect exact 4 SEU in this small windows is only 0.25%. This small likelihood can not be explained by variation of the beam profile nor by a chip failure. The beam current was permanently monitored during irradiation as well as the beam profile was measured several times by the accelerator shift leaders.

The small probability value, together with the observation of a continuously rising current (cf. 6.7.3 *Current Consumption Measurement Results* and fig. 6.54), is an indication that the SEU cross section was time-dependent, i.e. during the irradiation the three *Beetle* chips passed through a phase of enhanced SEU probability. Therefore, restricting the analysis to

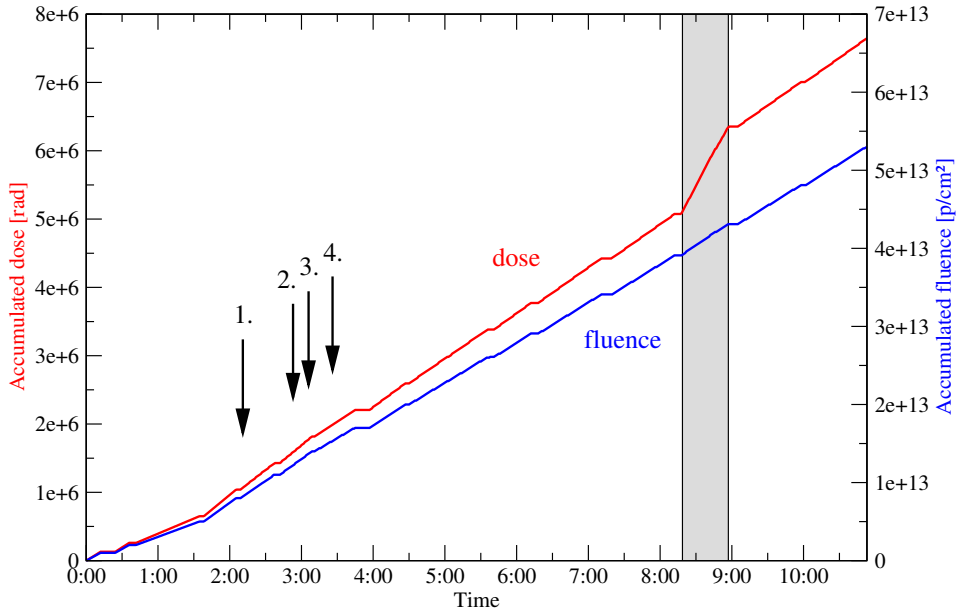


Figure 6.53: Accumulated dose (red) and fluence (blue) as a function of irradiation time. The irradiation is done with 65 MeV protons, except for the marked area. Here the chips are irradiated with 20 MeV protons for approximately 40 minutes. The time of the SEU detection is marked in the diagram.

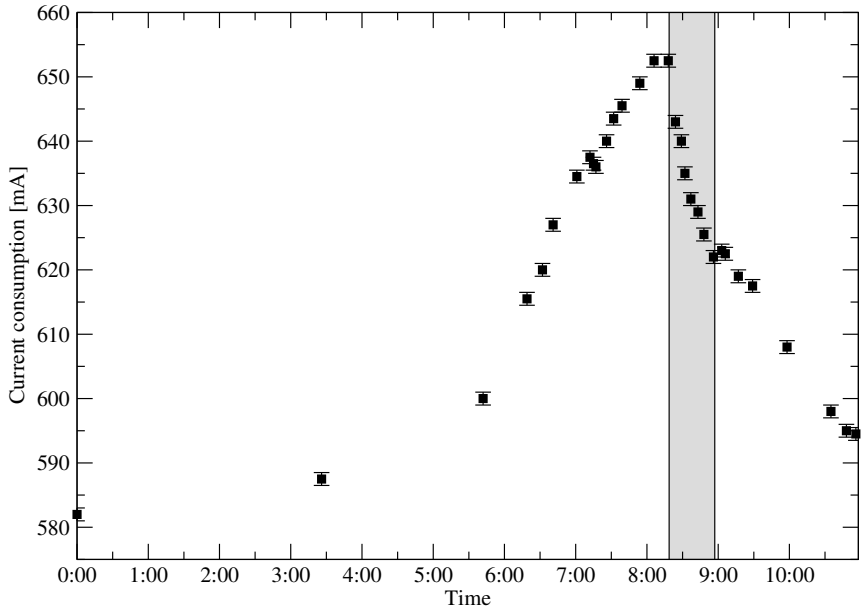


Figure 6.54: Current consumption of all three *Beetle* chips as a function of irradiation time.

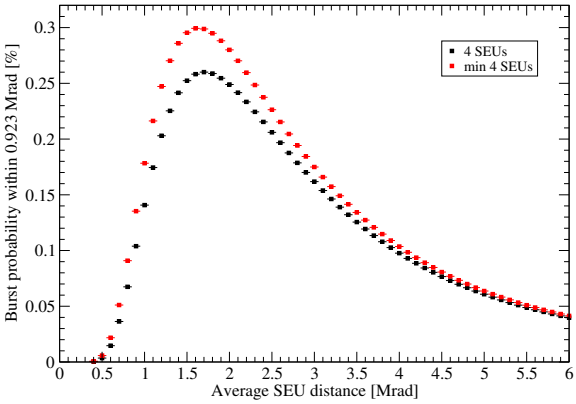


Figure 6.55: Monte Carlo simulation of a burst of 4 (black) or 4 and more (red) SEUs within 0.923 Mrad as a function of the average SEU distance. The total irradiation dose with 65 MeV protons is 6.647 Mrad.

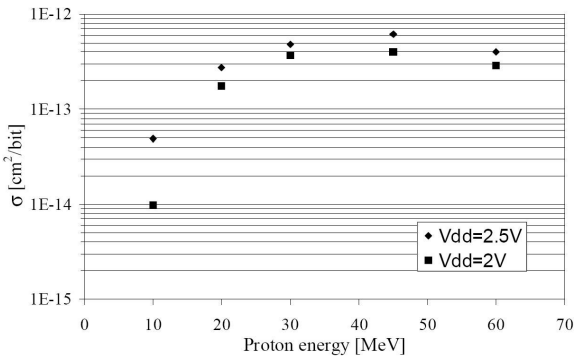


Figure 6.56: Measured cross section of a dynamic flip-flop, irradiated with a proton beam at different power supply voltages in the clocked mode [Fac99a].

the 0.923 Mrad window and taking the mean accumulated fluence between two SEUs, an SEU cross section per bit is calculated to

$$\sigma_{\text{unclocked static FF}} = (1.36 \pm 0.05) \cdot 10^{-16}\,\text{cm}^2/\text{bit} \tag{6.23}$$

for an unclocked static flip-flop (D-flip-flop with an asynchronous reset), irradiated with protons.

Figure 6.56 shows measurement results of the SEU cross section for clocked dynamic flip-flops as a function of the proton energy [Fac99a]. The test was performed at the nominal power supply voltage of 2.5 V and a reduced voltage of 2 V. The cross section gets lower when the power supply is decreased to 2 V, in contrast to the common idea that the SEU sensitivity is higher at lower supply voltages.

Comparing the cross section result for an unclocked static flip-flop (eq. 6.23) with the SEU cross section $\sigma_{\text{clocked dynamic FF}} = 4 \cdot 10^{-13}\,\text{cm}^2/\text{bit}$ for a clocked dynamic flip-flop at a proton energy of 60 MeV (from fig. 6.56), it can be observed that the dynamic D-flip-flop architecture is about four orders of magnitude more sensitive to SEUs than the static ones. This conclusion is in good agreement with the measurement results described in [Fac99a].

The absolute number of Single Event Upsets can be calculated by

$$SEUs = \sigma \cdot Fluence \cdot N \tag{6.24}$$

Taking the SEU cross section of a dynamic flip-flop, the total number of dynamic flip-flops of the three irradiated chips $N = 3 \times 2\,469 = 7\,407$ and a fluence of $5.3 \cdot 10^{13}\,\text{p/cm}^2$, the absolute number of SEUs created by 65 MeV protons during the irradiation test in the clocked logic circuitry of the *Beetle* chips is estimated to $\approx 1.73 \cdot 10^5$. This corresponds to a rate of SEUs of ≈ 4.4 Hz.

With the use of equation 6.24 and the given cross section for dynamic and static flip-flops, an estimation for the expected SEUs of *Beetle* chips at LHCb is also possible. The results are quoted in table 6.20 for all different sub-detectors which will be read out by the *Beetle* chip.

Detector	Chips	Flip-flops static/ dynamic	Rad. level over 10 years[25]	total numbers of SEUs in 10 years	number of SEUs
VELO	1 344	611	5.8 Mrad	$5.01 \cdot 10^3$	1.37 / day
		1 701	5.8 Mrad	$4.50 \cdot 10^7$	8.56 / minute
PUS	64	1 379	5.8 Mrad	$5.38 \cdot 10^2$	0.15 / day
		2 469	5.8 Mrad	$3.11 \cdot 10^6$	35.48 / hour
IT	1 008	611	7.0 Mrad	$4.54 \cdot 10^3$	1.24 / day
		1 701	7.0 Mrad	$4.07 \cdot 10^7$	7.74 / minute
TT	1 410	611	7.0 Mrad	$6.34 \cdot 10^3$	1.74 / day
		1 701	7.0 Mrad	$5.69 \cdot 10^7$	10.83 / minute
in total	3 826			$1.46 \cdot 10^8$	27.73 / minute

Table 6.20: Expected *Beetle* SEUs in 10 years of LHCb operation for different sub-detectors. The radiation levels are taken from [Chr05]. For the static used flip-flops a cross section of $\sigma_{\text{unclocked static FF}} = (1.36 \pm 0.05) \cdot 10^{-16}\,\text{cm}^2/\text{bit}$ (cf. eq. 6.23) is assumed, respectively for dynamic flip-flops $\sigma_{\text{clocked dynamic FF}} = 4 \cdot 10^{-13}\,\text{cm}^2/\text{bit}$ [Fac99a].

Pulse Shape Measurement Results

In addition to the SEU cross section measurement, pulse shape scans of the *Beetle* front-end were measured before, in between and after proton irradiation. Figure 6.57 shows these pulse shapes. In the plot the offset variation is corrected for each pulse shape. All front-end outputs are referred to the pre-irradiated pulse, whose peak is normalised to one. A 7.8% decrease of the amplitude is observed for the front-end output after an accumulated dose of 7.7 Mrad. Signal remainder 25 ns after the pulse maximum as well as peaking and rise time showed no variations.

Current Consumption Measurement Results

The measured total current consumption for all three *Beetle* chips during the proton irradiation is shown in fig. 6.54. It increased slowly from 580 to 600 mA in the first five hours of irradiation ($\approx$ 3 mA/h) and by another 55 mA in the next $2\frac{1}{2}$ hours ($\approx$ 22 mA/h). After this current increase the chips were irradiated for 40 minutes with 20 MeV protons instead of 65 MeV. The current consumption dropped during the irradiation and continued to decrease after the proton energy was set back to 65 MeV. There is no explanation of this current variation during the irradiation test. The analogue readout as well as the pipeline control logic and the I^2C-interface showed no failures.

6.7.4 Summary

Three chips were irradiated with 65 MeV protons for nearly 11 hours. The accumulated dose for all chips during this period was measured to 7.7 Mrad, which is more than the expected dose at LHCb after ten years of operation [Chr05]. After irradiation, the pipeline control logic of the three *Beetle* chips still run synchronously which leads to the conclusion that no malfunctions

[25] 1 Mrad is equivalent to $7.708 \cdot 10^{12}\,\text{p/cm}^2$ for 65 MeV protons.

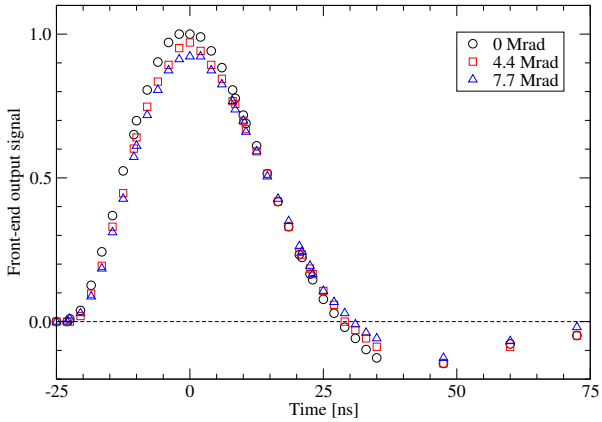


Figure 6.57: Pulse shape variation of a proton irradiated *Beetle* chip at different accumulated dose levels.

were introduced to the logic circuitry by SEUs. It was possible to detect SEUs by the internal SEU counter and to quote a cross section for static, unclocked D-flip-flops. A test of the self-triggering correction process of the triple-redundant flip-flops was not possible because of the low statistic of detected SEUs. The unexpected increase of the power consumption by 12% and the continious decrease of the current afterwards can not be explained.

6.8 Cosmic System Test

The concept of the cosmic system test was to set up a simple, stand-alone system for the long-term analysis of a complete readout system. The main task was verification of the processing of real detector signals. Furthermore, the logic circuitry, which controls the event storage and readout, the processing of arbitrary triggers and the synchronise readout of all chips, were tested.

6.8.1 Test Setup

Figure 6.58 shows a photography of the test setup in the ASIC laboratory. It consists of two scintillators with photomultiplier tubes and a silicon detector in between (left photography). A detailed view of the detector is shown on the right. The detector consists of three silicon strip sensors connected in series. Each of them is an OB2-type CMS silicon sensor designed for silicon tracker of the Compact Muon Solenoid (CMS) experiment [CMS]. Each sensor is a p-on-n type single-sided AC coupled silicon strip detector with a physical dimension of $96 \times 94\,\mathrm{mm}^2$ [Gas03a]. The nominal thickness of the n-type substrate is 500 µm, the p^+ strip pitch is 183 µm and the implant width is 46 µm. On each sensor there are 512 strips in total. The mean strip capacitance of a single sensor is given as $12.8 \pm 0.3\,\mathrm{pF}$ or normalised by the strip length to $1.39 \pm 0.04\,\mathrm{pF/cm}$. The sensor was operated in full depletion mode at an applied voltage of $V_\mathrm{d} = 200\,\mathrm{V}$.

The middle part of the detector strips (384 out of 512) is bonded to a ceramic pitch adapter and connected to three *Beetle1.2* chips on a hybrid of the Trigger Tracker. All analogue signals are connected via an adapter card to a digital scope. In case of a trigger the data is read out and stored on a PC. Via the same adapter card all digital service signals are routed to the *Beetle*

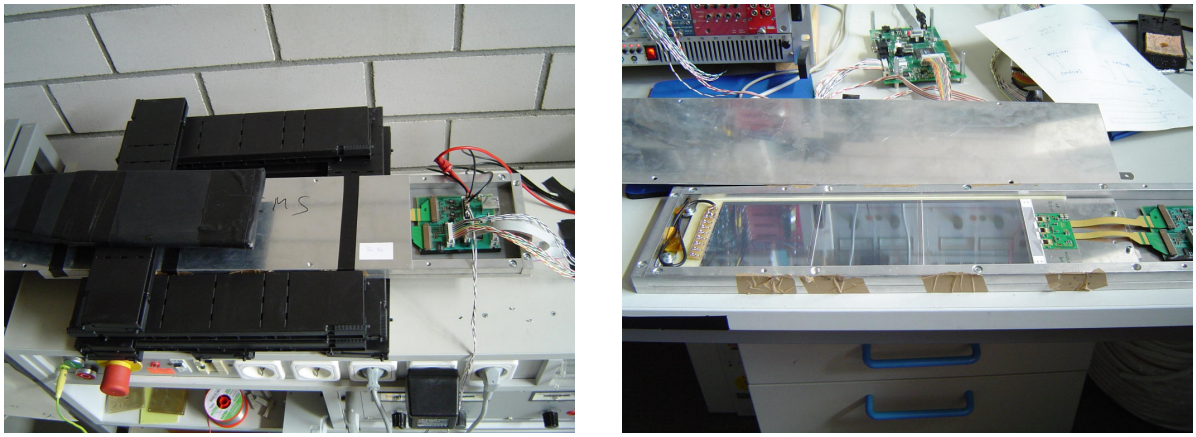


Figure 6.58: Photography of the *Beetle* system test setup with cosmic rays in the ASIC laboratory. The setup consists of two scintillators with photomultiplier tubes and a silicon detector in between (left). A detailed view of the detector is shown on the right photography. It is built-up from three smaller silicon detectors bonded together to one long detector and connected via a ceramic fan-in to a hybrid with three *Beetle1.2* chips.

chips. *Clock*, *Trigger*, *Testpulse* and *Reset* are generated by an FPGA on an ACEX board (cf. section 6.3.5). The I^2C-interface of the *Beetle* is controlled by the PC. NIM modules were employed for readout and coincidence detection of the photomultiplier signals. The coincidence signal is then connected to the ACEX FPGA. There the signal is synchronised to the 40 MHz system clock and delayed by 4 µs to match the latency of 160 clock cycles of the *Beetle*.

6.8.2 Test Results

The setup operated continuously for more then 3 months. Over this period of time no loss of the synchronisation between all three chips was seen, more exactly the Pipeline Column Numbers (PCNs) for all three chips are identical. Furthermore, no malfunction or hiccup of logic circuitry (*FastControl*) could be observed. In total, $1.4 \cdot 10^6$ events have been recorded to disk.

Beyond the long term test and functional test of the chips, the analogue signals are analysed, too. First of all, channels with a detector hit are classified by the off-line analysis software. A common mode baseline subtraction for all events and for each readout chip is applied. After this a pedestal of each channel and PCN is calculated from the data of all events. However, this value differs from the real offset value because there are still detector signals included. Therefore, a re-calculation of the average readout offset is done by ignoring all measurement values that differ more than 5σ from the first offset calculation. The results from the new calculation defines a precise offset value for each channel and PCN. In addition, the average noise value (N) for each pipeline cell is specified by the deviation from the previous calculation. Each readout signal (S) that exceeds more than 5σ is defined as a detector hit. The calibration of the noise amplitude to an Equivalent Noise Charge (ENC) is done with an external test pulse injection.

Figure 6.59 shows the Signal-to-Noise (S/N) distribution of all measured events. Data set entries with a S/N ratio of less than 5 are not taken into account. From the distribution a mean S/N of 16.44 and a deviation of 8.38 is calculated.

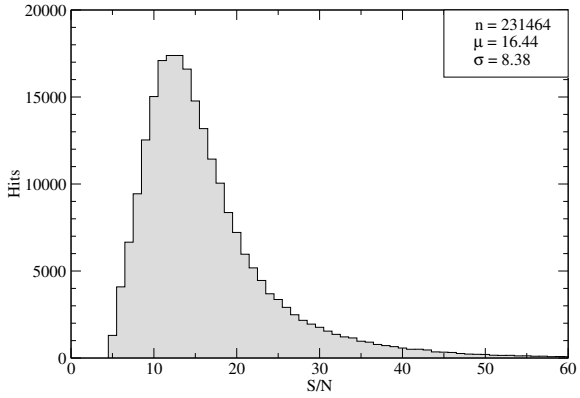


Figure 6.59: Signal-to-Noise (S/N) distribution of the measured events.

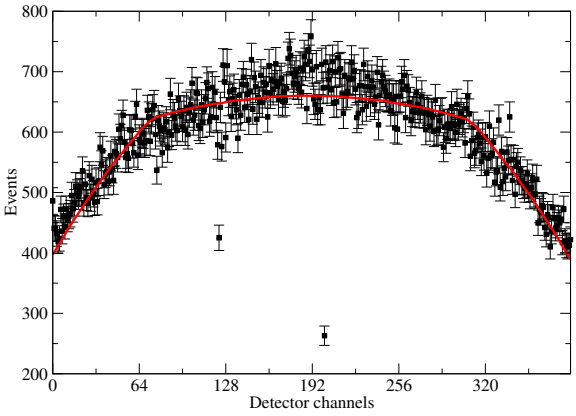


Figure 6.60: Number of measured hits for each detector readout channel (black) and the mean expected number (red), given by the position and size of the scintillators and the geometry of the detector.

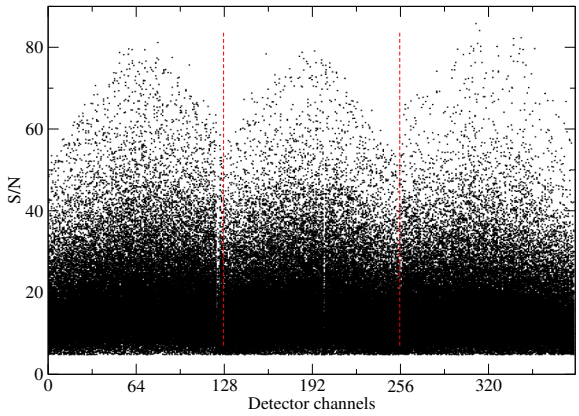


Figure 6.61: S/N value and detector channel position for each measured hit. Each group of 128 channels is connected and read out by a *Beetle* chip.

The total number of hits for each readout channel is plotted in fig. 6.60 (black). The readout channels are counted from 0 to 383. Each group of 128 channels is connected to one of the three *Beetle* chips. For comparison purposes the expected distribution from a simulation, given by the position and size of the scintillators and the geometry of the detector, is plotted in the same diagram (red). Two small outliers could be seen at channel 123 and 201. This can be explained by a broken bond wire between the single sensors. For channel 123 the bond wire between the last and the middle sensor is broken and therefore only two-thirds of the expected signals are transferred to the *Beetle*. In case of channel 201 only one sensor is connected to the readout chip (one-third of the expected signal amplitude is measured).

In the diagram of fig. 6.61 the S/N versus channel correlation is shown. The boundaries between different chips are marked with a dashed red line to clarify the different readout groups. A distinct rise of the maximum S/N ratio to the channels in the middle of a readout chip can be seen. This phenomenon is consistent with the results from the baseline offset

variation (fig. 6.62) and the noise variation (fig. 6.63) across the detector channels. A higher

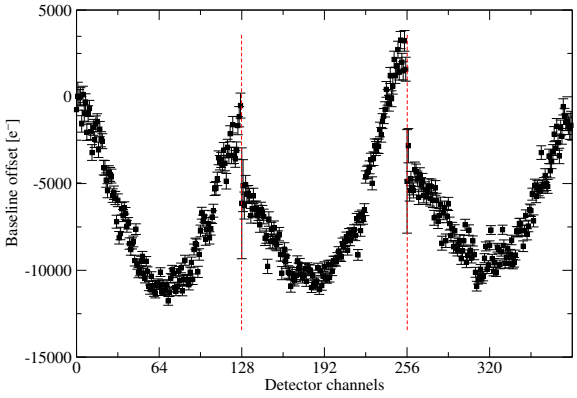


Figure 6.62: Baseline offset of all three detector readout chips.

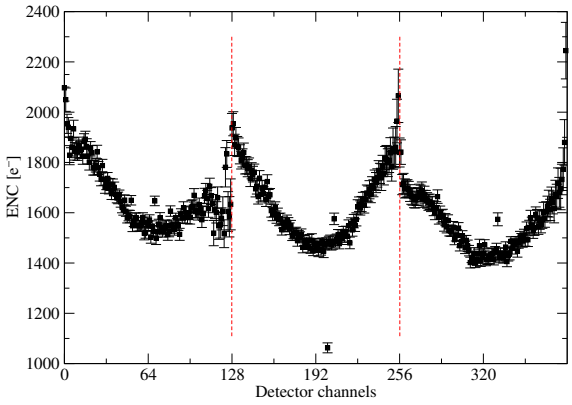


Figure 6.63: Equivalent Noise Charge (ENC) variation for all detector channels.

offset of the baseline at the edge of the readout chip leads to a smaller signal maximum due to the dynamic range limitation. Therefore, the S/N is smaller outside than in the middle part of a chip. The Equivalent Noise Charge distribution drops towards the centre and thus the ratio between Signal-to-Noise increases. The huge variation of the baseline offset and the dip in the middle is a typical feature of a *Beetle1.2* chip and solved at chips of version *1.5*.

The distribution of the ENC is strongly related to the input load capacitance (C_p) of the *Beetle*. From precise calibration measurements of the Equivalent Noise Charge (cf. section 6.3.7) the results of fig. 6.63 are converted to an equivalent capacitance. The maximum $C_\mathrm{p,max}$ at the edge of each chip results to $\approx 28\,\mathrm{pF}$, the minimum $C_\mathrm{p,min}$ in the centre is $\approx 21\,\mathrm{pF}$. Part of this inhomogeneity is caused by the different routing lengths on the ceramic adapter. The remaining part can not be explained.

Figure 6.64 shows the signal width distribution. The mean width is quoted with 1.93 channels and a deviation of 0.54. The large spread of the signal width is caused by the detector thickness of 500 µm and the maximum zenith angle of 55°, which produces in the most unfavourable case a signal in already 3.8 channels.

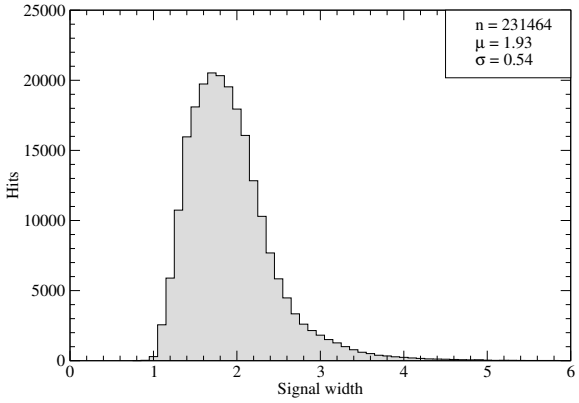


Figure 6.64: Signal width distribution.

6.9 Mass Production Tests

To ensure the complete functionality of a complex hybrid after assembly of a large number of *Beetle* chips, all individual chips have to be tested before. Because of this several hundreds of dies were tested manually in a clean room between July and October 2004 to guarantee the full analogue and digital performance of each single chip. In the following the details of the test setup, the measurement procedure and the test results are described.

6.9.1 Test Setup

It is not possible to test single chips for a future assembly with a hard wired connection. Therefore, a possibility is to connect chips temporarily with a so-called probe card. On such a card hundreds of small needles made of tungsten are attached. The order of the needles corresponds exactly to the pad order of the chip that has to be tested. In case of the *Beetle* chip these are 129 needles with a lateral distance of around 115 µm or less. The tips of all needles on such a card are exact at the same level. By moving down the complete card with all probe needles to the pad surface an electrical contact can be established. In case of a bad connection, this contact procedure can be theoretically repeated many times on the same chip. But due to the problem that each probe needle scratches the pad surface during contact phase, this process should be repeated only three to four times per chip.

Main part of the first mass production test setup is the combination of two different boards, so called mother and daughter boards. The daughter board contains only the probe needles as well as passive components (i.e. voltage blocking and signal termination). The board itself is a common two layer PCB that was developed in the ASIC laboratory for the use in different test environments. Geometry and size of the PCB was chosen so that it fits exactly into the mounts of both wafer probe stations[26] that are available in the clean room of the ASIC laboratory. Attaching and soldering the probe needles to the PCB was done by the company Uwe Electronics [UWE]. The final assembly of the probe card is shown in fig. 6.65 whereas fig. 6.66 shows the manual probe station PM5 with the probe card already installed.

In cooperation with the electronics workshop of Max-Planck-Institute for Nuclear Physics the mother board of the test setup was developed. It contains all active components like four analogue receivers, LVDS line drivers and receivers for the digital signals of a *Beetle*, I^2C-level shifters, etc.

The advantage of such a sandwich solution is the fast exchange of the sensitive probe card for the purpose of cleaning or repair.

For programming and testing of all *Beetle* registers a computer with an I^2C-interface is used. The communication via I^2C is done with a graphical user interface programmed in LabVIEW [NAT]. All digital sequences were generated with a pattern generator DG2020A from Tektronix [TEK], operating at the nominal LHCb frequency of 40 MHz. The important digital control signals (`WriteMon`, `TrigMon`, `FifoFull` and `DataValid`) and the four analogue readout links of the tested *Beetle* chip are controlled visually with two four-channels oscilloscopes.

6.9.2 Measurement Procedure

At first a single test chip is put directly under the probe card. The next step is then the alignment of the chip with respect to the probe needles. After the touchdown of the needles

[26] PM5 (manual) and PA200 (automatic) wafer probe station, both are from SÜSS MicroTec [SÜS]

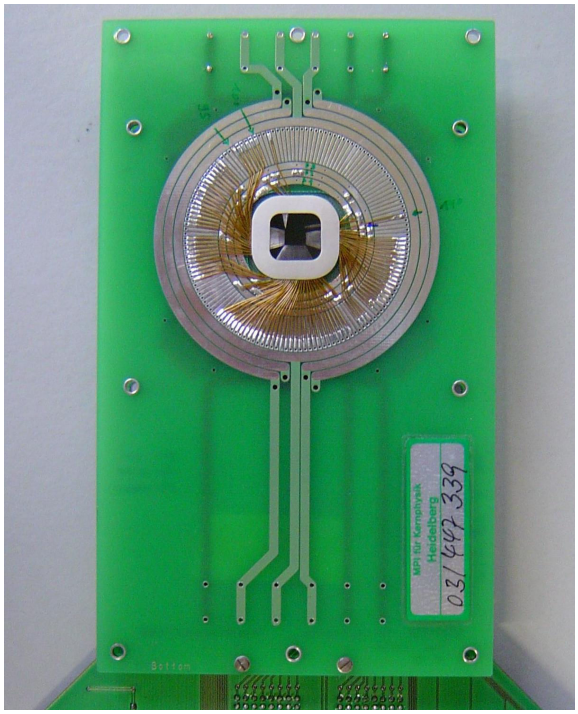


Figure 6.65: Bottom view of the *Beetle* probe card. The 129 needles can be recognised in the middle of the white ring.

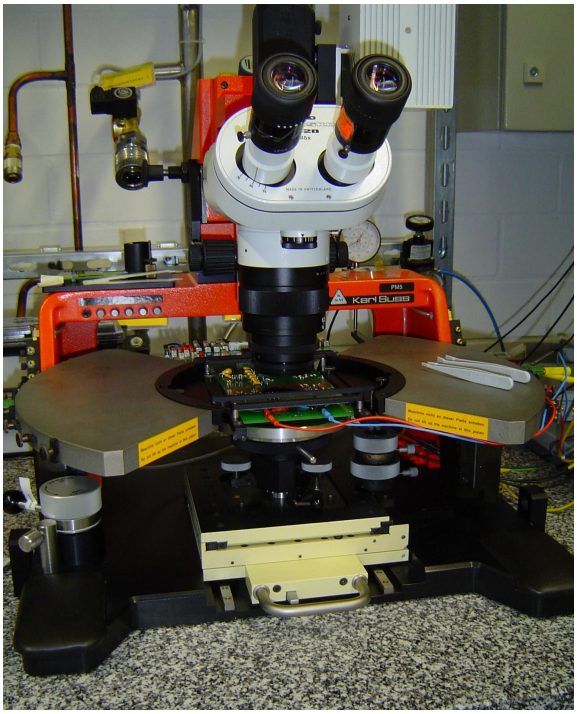


Figure 6.66: Manual wafer probe station PM5 from SÜSS MicroTec. The maximum possible wafer size of this prober is 6 inches.

to the pads of the *Beetle* chip, the power supply is switched on and the power consumption is measured. If this is smaller than the nominal value, the reason is mostly a bad power contact between chip and probe needles. In this case the power supply is turned off and the probe card is separated again. The repetition of the contact procedure solves contact problems in most cases. The power consumption of the chips then is in the expected range.

Then the following listed items are measured on each *Beetle* chip:

- power consumption without clock and programming of all registers.
- check of I^2C-identification number
- write and read of all internal *Beetle* registers, comparison of these values
- test of I^2C-general call access to the registers
- power consumption with clock and nominal operation parameters
- operation of all four analogue readout links
- application of positive and negative internal test pulses, readout of sampled test pulse data
- scan of the analogue pipeline for dead cells
- application of special trigger sequences, check for consecutive readouts

- test of different readout links:
  - 32 channels on four readout links (standard LHCb readout mode)
  - 128 channels on one readout link (lab mode)
- readout frequency less than sampling frequency (`Rclk` $\neq$ `Sclk`)
- consistency checks:
  - latency (`WriteMon` and `TrigMon`)
  - readout length (`DataValid`)
  - trigger handling (`FifoFull`)

To summarise the variety of the possible defects on a chip, nine groups listed in table 6.21 are introduced. A *Beetle* chip that passed all tested components is classified into the group 'Good', otherwise it is classified in one of the other groups according to the test results.

Group	Description	Possible examples
Good	All measured components showed no defects	
No power	Total power consumption (analogue and digital) is zero	• Skipped exposure during manufacturing
Power problems	Total power consumption is more than 10 percent lower/higher than expected	• Gate rupture • Short circuit
Analogue defect	Defects located somewhere in the analogue readout	• Defect readout driver • Wrong baseline • No internal test pulse
Channel defect	Defect related to a front-end channel	• Wrong signal on each PCN
Cell defect	A single cell defect in the pipelined memory	• Different signal for a single PCN
Digital defect	Defect located in the digital control system	• Pipeline control logic • Digital test signals • Wrong `DataValid` signal
I^2C defect	Communication problems with I^2C-interface	• Wrong identification number • Acknowledge problems
Register defect	Defect registers	• Write/read values are different

Table 6.21: Classification of chip defects, effects and possible sources of defects.

A special group is 'No Power'. Chips belonging to this group are normally located at the edge of a wafer. Because of production reasons the manufacturer has left out the exposure of some masks. However, it is possible to find these chips with a microscope by examining a revision block area on a *Beetle*. This will occur to all chips at the same position on different tested wafers. Once this position is known it is possible to skip the test of this position on all other wafers. The number of these chips has to be excluded from the yield calculation as well.

6.9.3 Test Results

Beetle1.3

Within this thesis the first mass production test setup for the *Beetle* was developed and assembled in the first half of 2004. The first tests with chips started in July. A large part of the first chip alignment and measuring program was done by Dr. Christian Bauer and Dr. Johan Blouw, both members of MPIK. This first lot of chips consisted of the remaining 181 *Beetle1.3* of the MPW run 11 (submitted in June 2003). Table 6.22 summarise the defects found during these tests. The high fraction of bad chips from wafer ACCP1PX and ADCP1NX can be explained

Wafer	ACCP1PX	ADCP1NX	ANCP1DX	AMCP1EX	total
Tested no. of chips	18	22	62	79	181
Good chips	13	19	59	73	164
Bad chips	5	4	3	6	18
Power problems		2	2	2	6
Analogue defect	1		1	1	3
Channel defect	1				1
Cell defect	3	1		2	6
Digital defect		1			1
I^2C defect				1	1
Register defect					0
No power					0

Table 6.22: *Beetle1.3* manual wafer test results from MPW 11

by the fact that nearly all of these chips are from the edge of the wafers. In case of wafer ANCP1DX and AMCP1EX the situation is different. At the time of the test no information about the original chip location were available. Therefore, there was no preselection of good chips before the wafer test.

***Beetle1.3*, *1.4* and *1.5* (Engineering Run)**

End of July 2004 the first 6 wafers from the *Beetle* engineering run, a pre-production run, were delivered to Heidelberg. On each wafer there are three different versions produced, ordered in rows over the complete wafer. In total there are 265 (263/262) chips from *Beetle1.3* (*1.4*/*1.5*) on each wafer. Because of laboratory and hybrid tests a quarter of one wafer was diced into single chips. *Beetle* version *1.3* and *1.4* could be tested with the same test setup from July. Before the test of a *Beetle1.5* could start a small modification at the probe card had to be done.

Altogether 213 chips from wafer KSMNKAT were tested manually in August and October 2004. These chips are from the second quadrant on the wafer. Measurement result of all chips are shown in table 6.23. The numbering of these chips as well as the distribution of the version

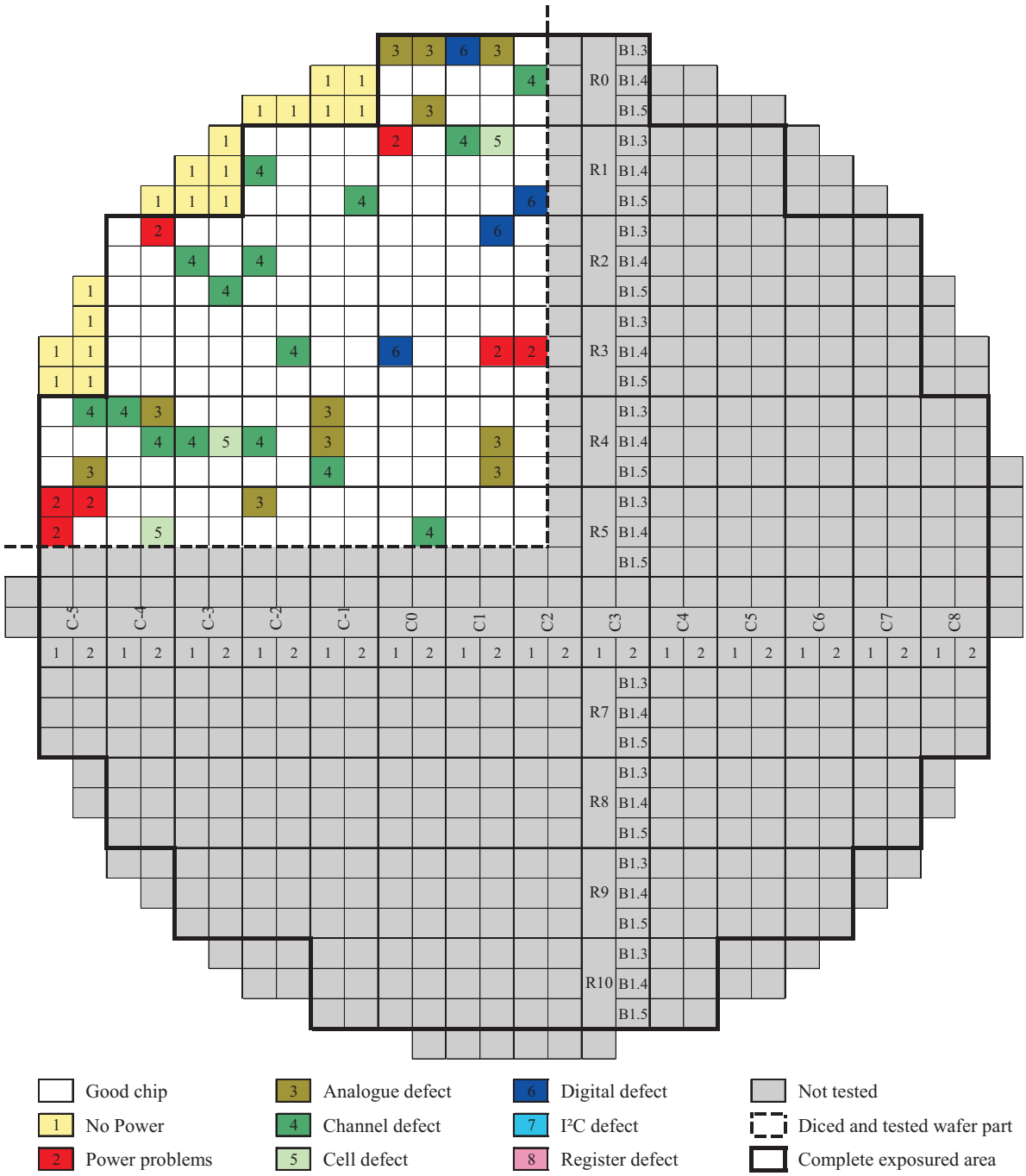


Figure 6.67: Wafer map of a *Beetle* engineering run wafer. Shown is the whole wafer with 790 dies. Different chip versions are ordered in rows. Framed chips in groups of up to six chips are from the same reticle and so exposed simultaneously during wafer production. The upper left quarter represents the tested area of wafer KSMNKAT. Defects are marked with different colours. Obviously chips with no power consumption (inked yellow) are from the same exposure step. 'No Power' defects are restricted to exposure steps that touch the wafer edge. Here the manufacturer intentionally skips production steps to avoid defective chips. The same problem with chips from the wafer edge is expected for each fabrication run.

Chip version	*Beetle1.3*	*Beetle1.4*	*Beetle1.5*	total
Tested no. of chips	72	76	65	213
Good chips	54	53	48	155
Bad chips	16	17	7	40
Power problems	4	3		7
Analogue defect	6	2	3	11
Channel defect	3	9	3	15
Cell defect	1	2		3
Digital defect	2	1	1	4
I^2C defect				0
Register defect				0
No power	2	6	10	18

Table 6.23: *Beetle1.3*, *1.4* and *1.5* wafer test results from engineering run

numbers on the wafer are printed in figure 6.67. Furthermore, the common exposure area is shown in this overview as well as the defect classification of the measured chips. In case of 'No Power' it is clearly visible that this effects the complete exposure area, and thus different chip versions. This effect occurs only at the edge of a wafer. It is caused by the manufacturer. The position of these chips is well known and the chips are not taken into account for the yield calculation below. So this will reduce the total number of possible good chips of each version on a wafer to 240. Figure 6.68 shows a detailed view of the emphasised reticle structure.

Yield Calculation

With the results of all measurements the yield of the production can be calculated. It is of interest, whether there is a deviation in the chip quality between wafers from the same production lot or between different lots, since there is a gap of nearly one year between these runs. An overview of all yield values is plotted in figure 6.69 as well as a global value for each single production lot. Furthermore, for reasons of comparison, a yield result from the former *Beetle* version *1.2* is also plotted in this diagram. In total, the overall yield of all good *Beetle1.3* chips from the MPW run is calculated to

$$Yield_{Beetle1.3(MPW)} = 90.6\% \pm 2.2\% \ .$$

The engineering run in contrast added up to the following yield numbers, quoted for each chip version separately:

$$Yield_{Beetle1.3} = 77.1\% \pm 5.0\%$$
$$Yield_{Beetle1.4} = 75.7\% \pm 5.1\%$$
$$Yield_{Beetle1.5} = 87.3\% \pm 4.5\%$$

Compared to the 2002 results of the *Beetle1.2* tests ($91.2\% \pm 3.4\%$) more defects are found on chips from the engineering run wafer.

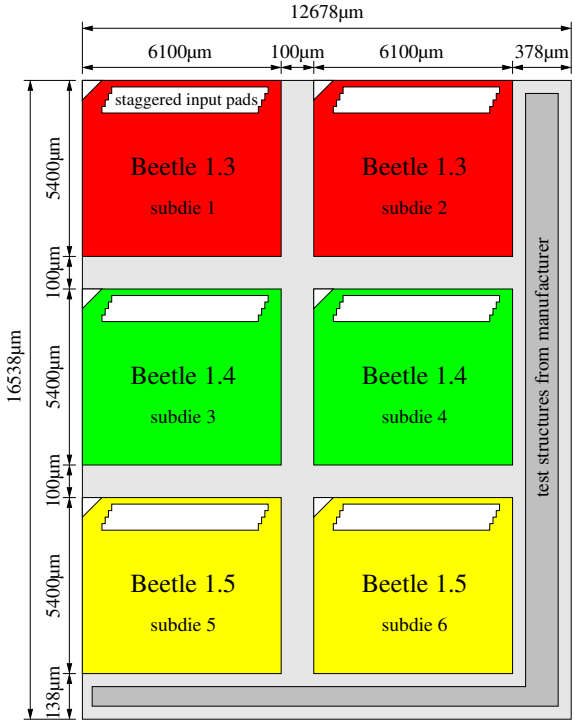


Figure 6.68: Final layout of the *Beetle* engineering and production run reticle. In total six chips are arranged on one reticle, containing two chips from each *Beetle* version *1.3*, *1.4* and *1.5*. The single chips are labelled from 'subdie 1' (upper left) to 'subdie 6' (lower right). Chips of the same version number are marked with the same colour.

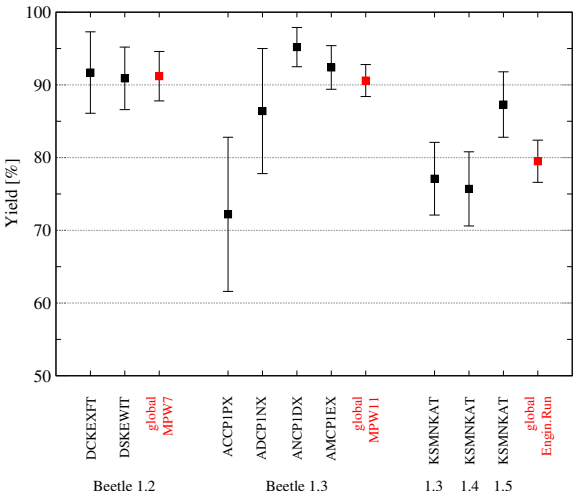


Figure 6.69: Yield summary of all mass production test results. For comparison reasons two results from a former chip test are included (*Beetle1.2* chips from MPW 7). A global value is added to the diagram for each different production lot (red dots).

6.9.4 Process Variations

The delivery of complete wafers from the engineering run for the first time allowed to measure process parameter deviations across single wafers. The distribution was measured by means of the test structure on *Beetle1.5* chips, already described in section 6.5.1.

Test Setup

The measurement of the Process Parameter Test structure was done on an automatic wafer probe station PA200 from SÜSS MicroTec [SÜS]. Four manipulators were used to place and connect probe needles to the four pads of the test structure (`VddCPT`, `GndCPT`, `PPTenable` and frequency output pad `PPTout`). Once aligned, the chip positioning and the contact procedure were controlled by the probe station software. The power supply voltage was set to the nominal process voltage of 2.5 volts and the digital signal `PPTenable` needed for activating the Process Parameter Test was generated by a pattern generator DG2020A from Tektronix [TEK]. To minimise the influence of the temperature on the measurement, the temperature of the complete wafer was regulated automatically by the probe station to a constant value of 25°C.

The internally generated frequency was measured at the output pad `PPTout`. To compare the measured deviation with results from simulation, the frequency was recalculated to a *Corner* parameter according to equation 6.19.

Test Results

First of all, the distribution of the process parameters on a complete wafer was determined. For the measurement the wafer no. K2MNG2T was chosen and the output frequencies of all 240 *Beetle1.5* chips on this wafer were measured. Altogether measurement of the frequency was repeated three times to minimise the error. Figure 6.70 shows the resulting distribution, diagrammed in a coloured, two-dimensional wafer map. Black and blue colours represent re-

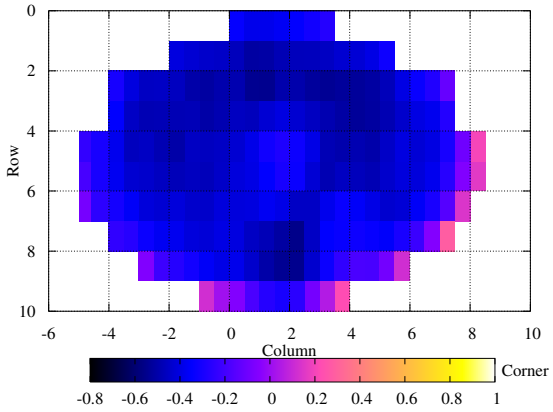


Figure 6.70: Distribution of measured *Corner* parameters across wafer K2MNG2T.

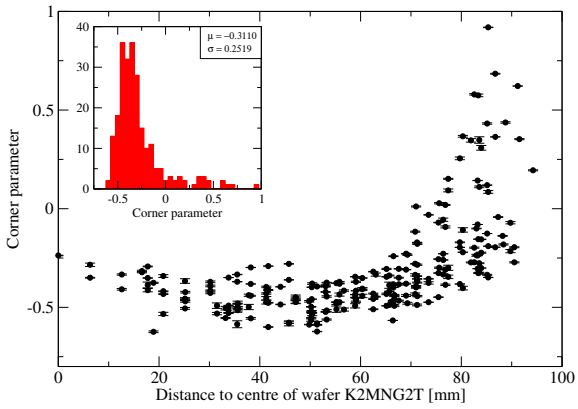


Figure 6.71: *Corner* parameter distribution as a function from the distance to the centre of the wafer. The histogram of the *Corner* distribution is also shown in the diagram.

gions with negative *Corner* values whereas regions with positive values are plotted in pink and yellow. In fig. 6.71 the results are plotted against the distance from the centre of the

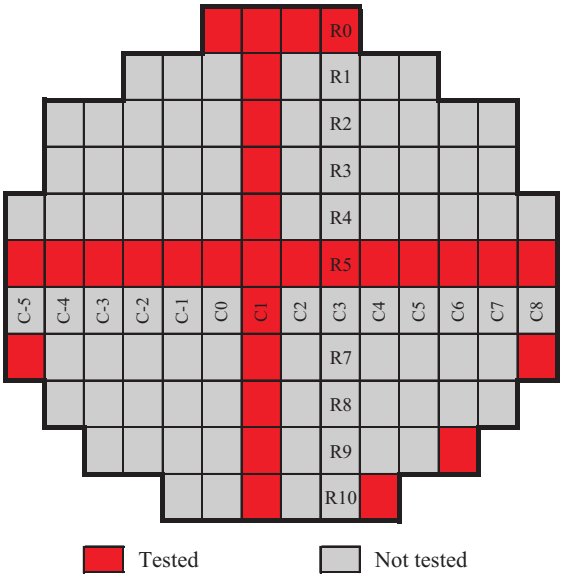


Figure 6.72: Position of selected reticles for the *Corner* measurements for different engineering run wafers. On each reticle there are two *Beetle1.5* chips with a Process Parameter Test structure.

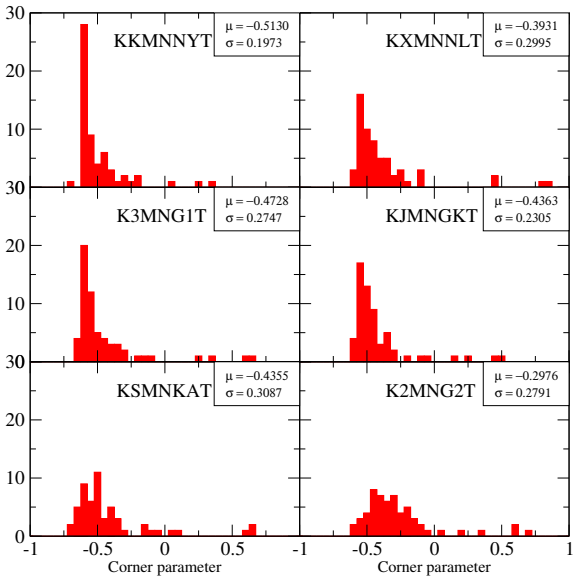


Figure 6.73: Histogram of the *Corner* parameter variation for all wafers of the engineering run. The mean value and the standard deviation of the process parameters for each wafer number is quoted in the diagram.

wafer together with the histogram of this distribution. It can be recognised easily, that the *Corner* parameter considerably rises towards the edge of the wafer. The mean displacement from the nominal process parameter for the complete wafer K2MNG2T was measured to be $\mu = -0.3110$ with a standard deviation of $\sigma = 0.2519$.

To give an estimation on the deviation between different wafers, the process parameter was also measured on six more wafers of the engineering run. Because of limited access to the wafer probe station, a reduction of the number of measurements had to be accepted. Therefore, a sample of 62 chips was chosen. The arrangement on the wafer is depicted in fig. 6.72. The distribution for each single wafer is plotted in the histograms of fig. 6.73. There is a clear variation from the nominal design value recognisable for all six wafers from the engineering run.

Chapter 7

Summary

Conclusion

The *Beetle* readout chip is designed for the readout of the approximately 450 000 silicon strip detector channels of the Vertex Locator (VELO), Pile-Up System (PUS), Trigger Tracker (TT) and Inner Tracker (IT) at LHCb. It is also designed as a backup option for the Ring-Imaging Cherenkov (RICH) detector in case of multi-anode photomultiplier readout is used.

Each chip provides an analogue or binary pipelined readout of 128 input channels as well as a prompt binary information of the front-end pulse discrimination. The analogue pipeline enables a maximum trigger latency of 4 µs (160 LHCb sampling clock intervals). Up to 16 consecutive events can be read out dead-time free. The implementation of the circuitry in a deep-submicron process technology and the use of enclosed NMOS transistors establishes the radiation hardness against total dose effects. Robustness against Single Event Upsets is achieved by the consistent use if triple-redundant logic in the highly sensitive parts of the pipeline control logic and in the Digital-to-Analogue-Converter and configuration registers.

In the context of this work, the following contributions have been made:

- five iterations of complete *Beetle* readout chips (*Beetle1.0* - *Beetle1.5*) as well as the preparation of the Engineering and Production Run ($\approx$ 40 000 chips),
- two test-chips have been developed, which were intended to characterise discrete chip components like the analogue pipeline memory, the pipeline amplifier, the I^2C-interface and a bidirectional LVDS driver and receiver (*BeetlePA1.0*) and the test and characterisation of the front-end modifications (*BeetleFE1.1*),
- the implementation of 8-bit current and voltage DACs which use a triple-redundant logic and a self-correction mechanism to ensure the robustness against Single Event Upsets,
- the modification of the low-noise charge-sensitive amplifier, to keep the LHCb specifications,
- the internal test-pulse circuitry, which allows the injection of well defined test signals to the front-end channels,
- the new pipeline schema, to reduce the channel-to-channel crosstalk as well as the increase of the radiation hardness,

- the improvement of the pipeline amplifier, to suppress baseline variations of the different readout modes,
- the analogue multiplexer together with the differential current output driver stage,
- increase of the overall performance of the *Beetle* chip in terms of noise, analogue-digital crosstalk, power consumption, testability and chip yield,
- irradiation of several chips up to 130 Mrad and characterised concerning pulse parameters, noise and function,
- a proton irradiation test to qualify the robustness against Single Event Upsets and to determine the SEU cross section of the digital memory cells,
- the development of the PC-based programming interface and assembly of the laboratory test environment,
- initial start-up of the different *Beetle* chip versions as well as the detailed characterisation of these chips,
- development of a mass production test setup.

The latest versions of the *Beetle* readout chips (*Beetle1.3* to *Beetle1.5*) fulfil all the requirements of the VELO, PUS, TT and IT detectors of LHCb as well as the front-end electronics specifications. Furthermore a irradiation test approved the radiation hardness in excess of 130 Mrad and the logic circuitry operated successfully in a 65 MeV proton beam without any malfunction due to SEUs. The Equivalent Noise Charge (ENC) of the latest *Beetle* chip version is measured to

$$\mathrm{ENC} = (530.64 \pm 9.97)\,\mathrm{e}^- + (49.76 \pm 0.46)\,\mathrm{e}^-/\mathrm{pF} \cdot C_\mathrm{p}.$$

The *Beetle* chips have been successfully operated in different test beam campaigns that included the final detector module design.

Outlook

A chip test setup for a semi-automatic wafer probe station has been developed for the use of the final testing and characterisation of the mass production chips (*Beetle1.3* to *1.5*). Until end of Q3/2005 in total 29 520 out of the existing 44 640 chips have been tested. An average yield of 82.8% has been measured with the automatic wafer test. This is six times more chips than needed by the LHCb sub-detectors. In Q1/2006 the remaining chips will be tested and diced for their possible use in future experiments. The test result summary of the single chip analogue performance on a wafer is shown in fig. 7.1 exemplarily. The overall distribution of the classified chips across the wafers is given in fig. 7.2.

The next steps in the *Beetle* project include the start of the series production for the Vertex Locator, Pile-Up System and the Silicon Tracker. They will be ready for installation into the LHCb detector in 2006. After successful commissioning the first data-taking of LHCb is expected for late 2007.

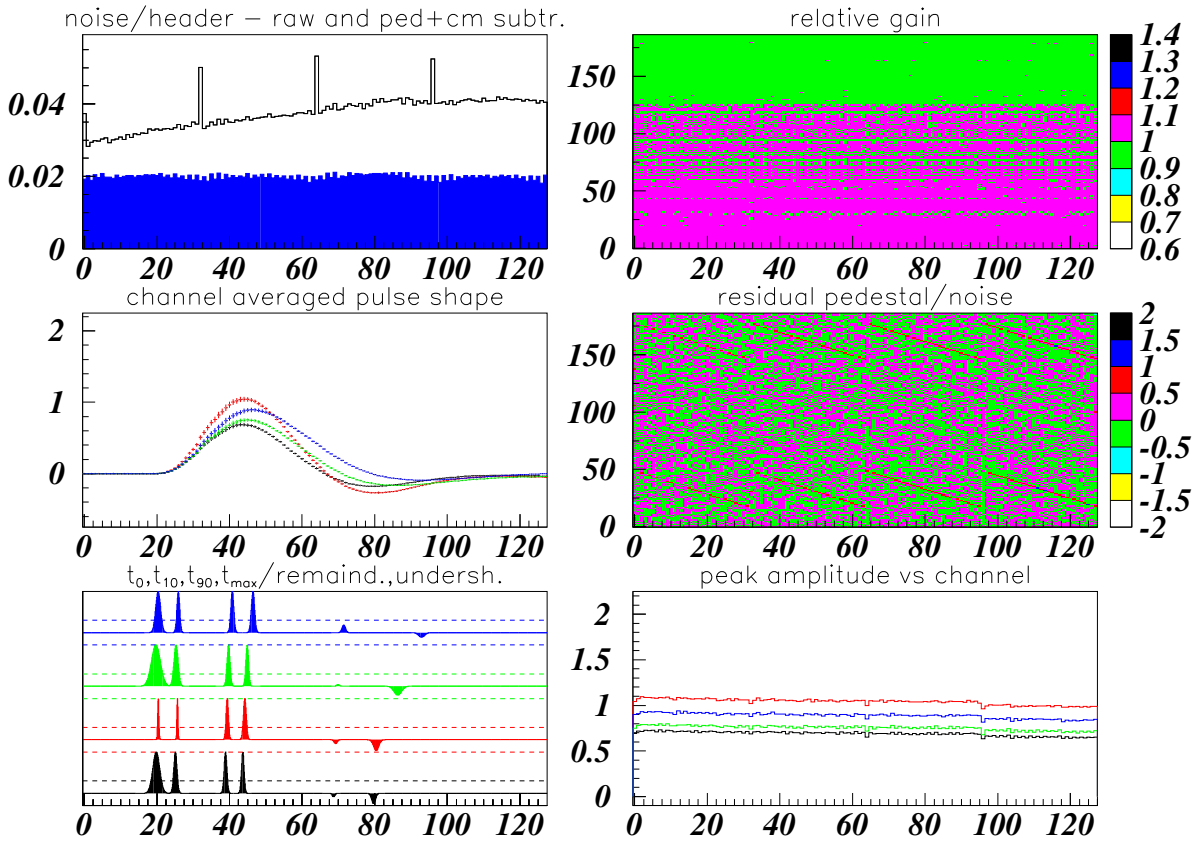


Figure 7.1: Overview of the analogue test results for a single *Beetle* chip, measured at the semi-automatic wafer probe station. In the left column from top to bottom the results of a noise scan, the pulse shapes for different bias settings and the distribution of characteristic timing points t(start), t(10%), t(90%), t(peak), t(remainder) and t(undershoot) of the pulse shapes are shown. On the right hand side the gain across the pipeline, the pipeline pedestal and the peak amplitude versus the channel number for different front-end bias settings are plotted [Sch05].

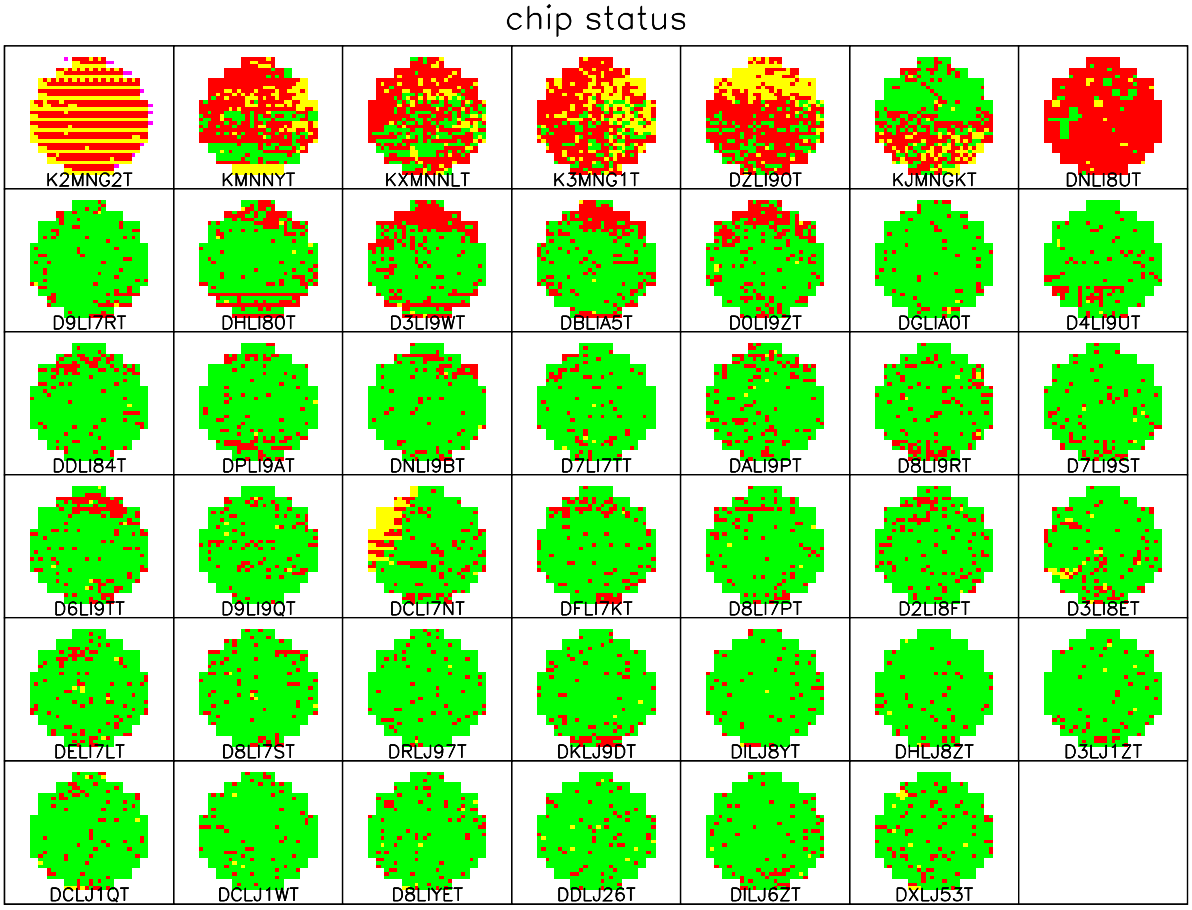


Figure 7.2: Graphical overview of all wafer test results. Underneath each plot the internal wafer number is given. Numbers starting with a 'K' are from the Engineering Run, 'D' numbers are from the final mass production. On each wafer 720 chips are placed. The different colours represents the final test results of these chips: green – good chip, all tests have been passed; yellow – no data has been taken; red – bad chip, some analogue or digital tests have not been passed. The wafers were tested in the order from left to right and top to bottom. At the beginning of the routine wafer test, chips were marked more often as failed because of bad chip contacts [Sch05].

List of Abbreviations

AC	Alternating Current
ADC	Analogue-to-Digital-Converter
ALICE	A Large Ion Collider Experiment
ASIC	Application Specific Integrated Circuit
ATLAS	A Toroidal LHC AparatuS
CCE	Charge Collection Efficiency
CERN	European Organisation for Nuclear Research
CKM	Cabbibo-Kobayashi-Maskawa
CMOS	Complementary Metal Oxide Semiconductor
CMS	Compact Muon Solenoid
CSA	Charge-Sensitive Amplifier
DAC	Digital-to-Analogue-Converter
DC	Direct Current
DELPHI	DEtector with Lepton Photon and Hadron Identification
DFF	Dynamic Flip-Flop
DNL	Differential Nonlinearity
DTMF	Dual Tone Multiple Frequency
DUT	Device Under Test
ECAL	Electromagnetic Calorimeter
ECS	Experiment Control System
EDAC	Error Detection and Correction
EEPROM	Electrically Erasable Programmable Read-Only Memory
ELT	Edgeless Transistor

ENC Equivalent Noise Charge

ESD Electro-Static Discharge

FET Field Effect Transistor

FIB Focused Ion Beam

FIFO First In, First Out

FPGA Field Programmable Gate Array

GBW Gain-Bandwidth

GEM Gas Electron Multiplier

GPIB General Purpose Interface Bus

GUI Graphical User Interface

HCAL Hadronic Calorimeter

HDL Hardware Description Language

HLT High Level Trigger

HPD Hybrid Photo Detector

IC Integrated Circuit

INL Integral Nonlinearity

IP Interaction Point

IT Inner Tracker

JTAG Joint Test Action Group

KIP Kirchhoff Institute for Physics

LabVIEW Laboratory Virtual Instrument Engineering Workbench

LEP Large Electron Positron

LET Linear Energy Transfer

LHC Large Hadron Collider

LHCb Large Hadron Collider beauty

LOCOS Local Oxidation of Silicon

LSB Least Significant Bit

LVDS Low Voltage Differential Signals

MaPMT Multianode Photomultiplier Tube

MBU Multiple Bit Upset

MIMCAP Metal-Insulator-Metal Capacitor

MIP Minimum Ionising Particle

MOS Metal Oxide Semiconductor

MOSCAP Metal Oxide Semiconductor Capacitor

MOSFET Metal Oxide Semiconductor Field Effect Transistor

MPIK Max-Planck-Institute for Nuclear Physics

MPW Multi-Project Wafer

MSB Most Significant Bit

MWPC Multi Wire Proportional Chamber

NIM Nuclear Instrumentation Module

NMOS N-channel Metal Oxide Semiconductor

NFET N-channel Field Effect Transistor

OT Outer Tracker

OTA Operational Transconductance Amplifier

OTIS Outer tracker Time Information System

PC Personal Computer

PCB Printed Circuit Board

PCI Peripheral Component Interconnect/Interface

PCN Pipeline Column Number

PIF Proton Irradiation Facility

PMOS P-channel Metal Oxide Semiconductor

PPT Process Parameter Test

PS Preshower

PSI Paul Scherrer Institute

PUS Pile-Up System

RAM Random Access Memory

RICH Ring-Imaging Cherenkov

RMS Root Mean Square

RS Readout Supervisor

S/N Signal-to-Noise

SCL Serial Clock

SCR Silicon Controlled Rectifier

SDA Serial Data

SEBO Single Event Burn Out

SED Single Event Disturb

SEE Single Event Effect

SEFI Single Event Functional Interrupt

SEGR Single Event Gate Rupture

SEL Single Event Latch-up

SES Single Event Snapback

SET Single Event Transient

SEU Single Event Upset

SHE Single Hard Error

SM Standard Model

SPD Scintillating Pad Detector

SRAM Static Random Access Memory

ST Silicon Tracker

STI Shallow-Trench Isolation

TDC Time to Digital Converter

TOTEM TOTal cross section and Elastic scattering Measurement

TRDFF Triple-Redundant D-type Flip-Flop

TRFDFF Triple-Redundant Flip-indicating D-type Flip-Flop

TT Trigger Tracker

VELO Vertex Locator

VLSI Very Large Scale Integration

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Appendix A

The *Beetle* Family

The development of the *Beetle* chip started in late 1998 with the specification and the choice of the technology. In the following years, 8 test chips and 7 complete readout chips are developed successfully.

In this appendix a short summary for each developed chip is given. The chronological order of the fabrication of the chips is shown in fig. A.1.

A.1 The *Beetle* Test Chips

In total 8 test chips, all with a dimension of $2 \times 2\,\mathrm{mm}^2$, are developed.

A.1.1 *BeetleFE1.0*

The *BeetleFE1.0* is the first prototype chip for the preamplifier/shaper circuitry of the *Beetle* chip. It contains three different sets of preamplifier and shapers (each set consists of 4 identical channels). It follows the basic RD20 approach of a folded cascode charge sensitive preamplifier, followed by an active CR-RC shaper and an output buffer.

The three sets differ as follows:

- Set 1 and 2 use PMOS input transistors but differ in the feedback network of the shaper.
- Set 3 uses an NMOS input transistor.

A.1.2 *BeetleFE1.1*

BeetleFE1.1 implements an improved preamplifier/shaper circuitry of the *Beetle* chip. All front-end channels of the *BeetleFE1.1* use as NMOS input transistor and a PMOS feedback transistor in the preamplifier. Design goal for this chip was the development of a front-end with a faster shaping and an increased rate capability than the former *BeetleFE1.0* to cope with higher detector occupancies.

The three blocks differ as follows

- Block 1 consists of two channels from the *Beetle1.0* readout chip. It has additional substrate contacts in the front-end, which were not present on the original *BeetleFE1.0*.
- Block 2 consists of 5 front-end channels with different preamplifier and shaper feedback circuits.
- Block 3 is identical to Block 2, except for a modified bias circuitry.

A.1.3 *BeetleFE1.2*

BeetleFE1.2 implements an improved preamplifier/shaper circuitry of the *Beetle* chip. Design goal for this chip was the development of a front-end with faster shaping and an increased rate capability than the *BeetleFE1.0*.

The three sets differ as follows

- Set 2 consists of a single channel as implemented on the original *BeetleFE1.0*. It uses a PMOS input preamplifier with a PMOS feedback transistor.

- Set 5 consists of 9 front-end channels with different preamplifier input transistors and shaper feedback circuits. It uses a PMOS input preamplifier with a PMOS feedback transistor.

- Set 6 is the original Set 2 from *BeetleFE1.0*, except that the preamplifier feedback has been changed: the 2nd channel uses an NMOS input preamplifier with an NMOS feedback transistor.

A.1.4 *BeetleBG1.0*

BeetleBG1.0 is the first prototype chip for the bias generators to be integrated into the *Beetle* readout chip. It integrates voltage and current Digital-to-Analogue-Converter (DAC) and a current source.

A.1.5 *BeetlePA1.0*

BeetlePA1.0 implements components from the *Beetle1.0* with special access possibilities to some internal notes. These components are: a small fraction of the pipeline memory, the pipeline readout amplifier, I^2C-interface and some LVDS input/output pads.

A.1.6 *BeetleCO1.0*

BeetleCO1.0 implements different comparator versions for the *Beetle* chip. To improve the threshold uniformity, each comparator has a 3-bit DAC. The comparator can handle positive and negative input signals. A polarity signal changes the polarity of the threshold level and makes the output signal always active high. The output signal is latched by an external 40 MHz clock.

A.1.7 *BeetleMA1.0*

BeetleMA1.0 is a front-end test chip for the RICH backup solution. It is a copy of the *BeetleFE1.0* with some modifications before the preamplifier stage to reduce the input signal.

A.1.8 *BeetleSR1.0*

BeetleSR1.0 integrates two types of I^2C-interfaces – a standard and an SEU robust one using triple redundant logic. Further there are two memory blocks implemented, consisting of 34 8-bit registers each.

A.2 The *Beetle* Readout Chips

In total 7 readout chips are developed and manufactured within this project. The height of all chips were 6.1 mm and the width varied between 5.1 mm and 5.5 mm.

A.2.1 *Beetle1.0*

Beetle1.0 was the first prototype of the complete readout chip for the LHCb experiment. Its main purpose was the evaluation of the concept and enabling first system tests. Hence, while featuring the basic fast readout mode for LHCb (16 multi-event buffers, output of analogue data via 4 ports at 40 MHz speed) many other features were not implemented, especially the logic was not robust against SEU.

A layout error in a tristate buffer of the control circuitry prevents the programming of the chip via the I^2C-bus. The internal data bus of the *Beetle1.0* was permanently forced to logic 0. Due to a bug in the extraction software, this error was not found by the available checking tools. A Focused Ion Beam (FIB) patch has been applied to a single die [FEI].

A.2.2 *Beetle1.1*

Beetle1.1 is an improved version of the first complete readout chip *Beetle1.0*. Its main purpose was again the evaluation of the concept and enabling system tests.

The main improvements are:

- working tristate buffers which enable the read-back of setup registers,
- improved biasing of pipeline readout amplifier,
- fixed dummy transistors in transmission gates of the multiplexer and the pipeline readout amplifier,
- missing ground connections are removed,
- correct Pipeline Column Number (PCN) levels in the analogue output header,
- binary readout now available,
- analogue delay circuit for I^2C-interface permits the programming independent from 40 MHz clock,
- implementation of the pipeline readout amplifier test node,
- new structure of pipeline.

A.2.3 *Beetle1.2*

Beetle1.2 is an improved version of the *Beetle1.1* chip. All missing features are implemented, especially the logic robustness against SEU.

The brief improvements and new features are:

- Single Event Upset (SEU) robustness of all digital parts,
- hard wired *Beetle* chip identification number (defined via bond pads),
- consecutive readout within 900 ns (without any gap in between two readouts),
- status information is added to the analogue output header,

- improved daisy chain concept,
- fixed crazy readout at very low trigger rates,
- new analogue front-end (taken from *BeetleFE1.1*),
- new reset concept (external reset + power-up reset),
- modified comparator (disable of individual channels, SEU robust logic),
- new test pulse circuit (test pulse on individual channels now possible),
- elongated analogue input pads,
- fully differential output drivers (analogue and LVDS operation mode),
- added Schmitt-Triggers to I^2C-pads,
- improved power routing (additional pads),
- smaller die size: $5.1 \times 6.1\,mm^2$
- modified biasing of LVDS transmitters (reduced power consumption),
- on-chip trigger synchronisation,
- new I^2C-interface (taken from *BeetleSR1.0*),
- implementation of a counter for SEU events.

A.2.4 *Beetle1.2 MA0*

Beetle1.2 MA0 is a copy from the readout chip *Beetle1.2* with some modifications in the front-end amplifier. The modifications were tested before on the *BeetleMA1.0* test chip.

A.2.5 *Beetle1.3*

Beetle1.3 is an improved version of the former *Beetle1.2* chip. It was first manufactured on a Multi-Project Wafer (MPW) run. After detailed characterisations the chip was accepted as a possible readout chip version for the LHCb experiment. Hence it is the first of the three versions, submitted on the final *Beetle* engineering run in May 2004. More details can be found in the appendix C.

A quick summary of improvements are:

- resize of chip dimension to $5.4 \times 6.1\,mm^2$,
- modifications in comparator design, 5-bit channel resolution,
- power net improvements to reduce digital crosstalk:
  - new power pads to the analogue input part,
  - power routing changed in front-end (especially shaper), additional power blocking in output buffer stage,

  - improved pipeline readout amplifier power routing,
  - merged pad openings of adjacent power pads (more bond wires are possible),
  - separation of digital multiplexer power and digital logic core power,
  - separation of comparator power (digital core) and power of the comparator LVDS pads,
  - 2 new power pads for digital logic core,

- all current mirrors in the layout of the front-end are moved from top to bottom,
- new current output driver,
- fixed over voltage problem,
- implementation of 5 V tolerant I^2C-pads,
- reduced number of Dynamic Flip-Flop in multiplexer,
- removed switching spikes in analogue readout header,
- fixed crosstalk from analogue readout header into first readout channel,
- fixed sticky charge problem,
- fixed baseline problem in consecutive readouts (run-away of baseline),
- changed test pulse pattern,
- new probe pads for current DAC measurements,
- fixed daisy chain bug,
- fixed limitation of `Rclk` divider ratio,
- reduced number of clock buffers in the logic core of the *Beetle*Beetle.

A.2.6 *Beetle1.4*

Beetle1.4 is the second of the three versions, submitted on the final *Beetle* engineering run in May 2004.

A quick summary of improvements on *Beetle1.4* are:

- fixed parity bit of the Pipeline Column Number (PCN) in the analogue readout header,
- fixed even/odd crosstalk in pipeline,
- new, modified comparator circuit,
- additional optical alignment markers.

A.2.7 *Beetle1.5*

Beetle1.5 is the third of the three versions, submitted on the final *Beetle* engineering run in May 2004.

A quick summary of improvements on *Beetle1.5* are:

- new, separated analogue power net for the comparator,
- new layout of the analogue pipeline memory,
- modified multiplexer timing,
- new test structures (Process Parameter Test).

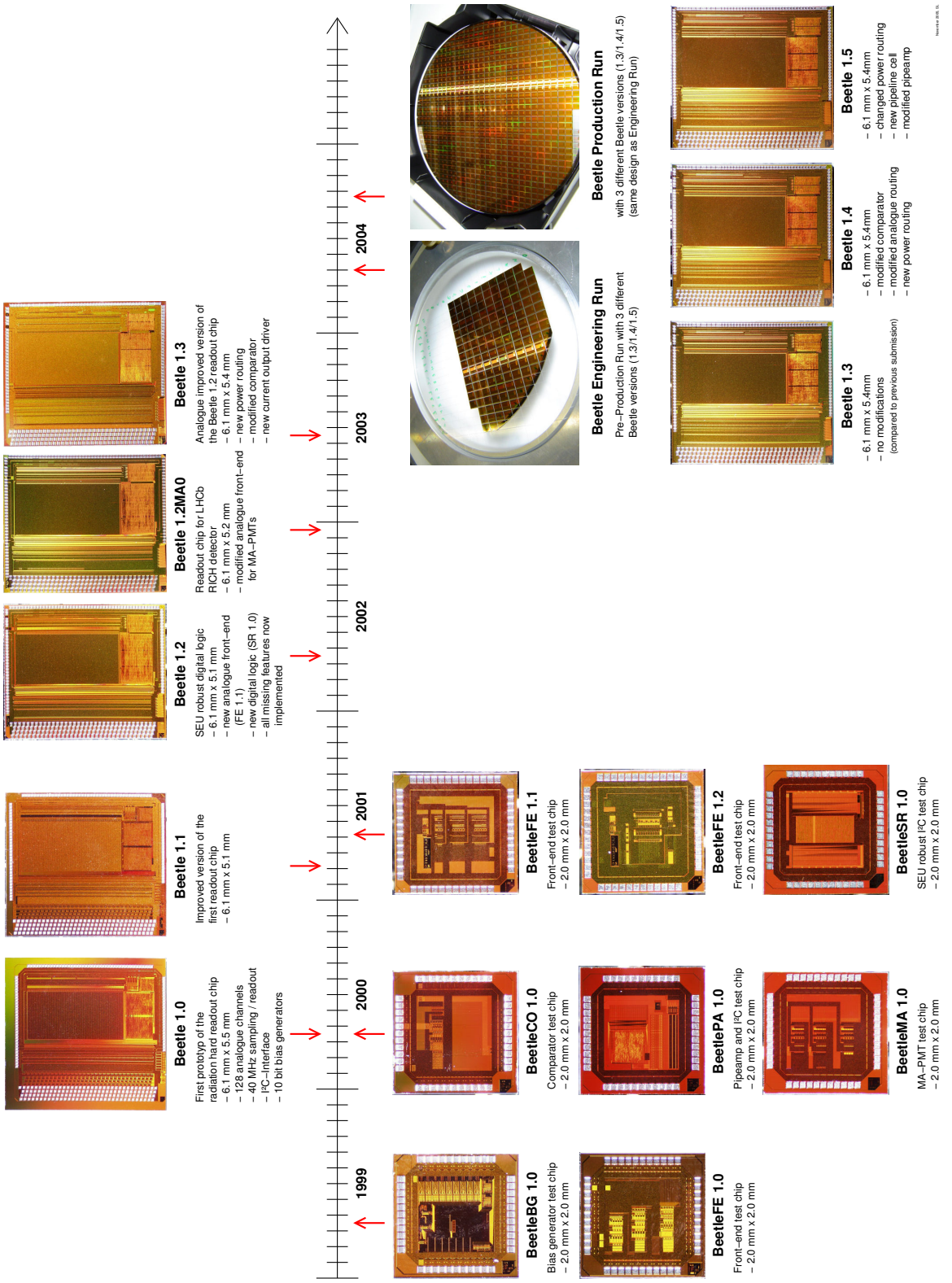

Figure A.1: Chronological overview of the fabrication of the different test and readout chips of the *Beetle* project.

Appendix B

I^2C-Software

B.1 ELV I²C Parallel Port Adapter Software

The I²C-bus is a simple 2-wire bus that allows micro-controllers and computers to connect to specialised IC's like videotex-decoders, Dual Tone Multiple Frequency (DTMF) generators, and many others. There is also a wide range of other I²C-bus chips that offer a more wide-range application like ADCs and DACs, switches, digital potentiometers, etc.

The ELV I²C-interface is not designed as an stand-alone I²C-master. Quite contrary, it operates only as a repeater board and converts the signal levels to the I²C standards. The real I²C-sequence is generated at the parallel port of a standard PC. The I²C software implementation is written in *C* (cf. listing B.1) and consists of two parts. In the first part (code line 17 to 100) all basic communication functions of the parallel port are shown. From code line 101 to 320 the functions for I²C-signal generation are printed.

Listing B.1: `i2c.c`: *C* code of ELV I²C parallel port adapter software

```
1  /*****************************************************************/
2  /*  I2C-ELV-PC-interface                                         */
3  /*                                                               */
4  /*  name               : i2c.c                                   */
5  /*  created from ELV   : 06.06.01   Sven Loechner                */
6  /*                       12.06.01   Sven Loechner  (waitPort)    */
7  /*****************************************************************/
8
9  #include <conio.h>
10 #include "i2c.h"
11
12 unsigned char data;      /* global variable  = parallel port output */
13
14 /* definition for all routines:                                  */
15 /*   portDelay: number of cycles to wait                         */
16 /*   portAdr:   address of LPT-port (LPT1: 0x378, LPT2: 0x37a)    */
```

```
17 /*****************************************************************/
18 /* basic routines for SDA and SCL bit manipulation               */
19 /*****************************************************************/
20
21 void waitPort (unsigned short portAdr, unsigned char portDelay)
22 /* wait max. portDelay operations cycles for an input */
23 /* input: portDelay, portAdr */
24 {
25     while (portDelay)
26     {
27         portDelay--;
28         _inp(portAdr);
29     }
30 }
31
32 void sda_high (unsigned short portAdr, unsigned char portDelay)
33 /* set SDA output to high    */
34 /* input: portDelay, portAdr */
35 {
36     data &= 0xfd;                    /* line D1=0 --> SHA high */
37     _outp (portAdr, data);           /* send data              */
38     waitPort(portAdr, portDelay);    /* NOP - wait             */
39 }
40
41 void sda_low (unsigned short portAdr, unsigned char portDelay)
42 /* set SDA output to low     */
43 /* input: portDelay, portAdr */
44 {
45     data |= 0x02;                    /* line D1=1 --> SDA low  */
46     _outp (portAdr, data);           /* send data              */
```

```
47      waitPort(portAdr, portDelay);        /* NOP - wait              */
48  }
49
50  void scl_high (unsigned short portAdr, unsigned char portDelay)
51  /* set SCL output to high    */
52  /* input: portDelay, portAdr */
53  {
54      data &= 0xfe;                        /* line D0=0 --> SCL high */
55      _outp (portAdr, data);               /* send data               */
56      waitPort(portAdr, portDelay);        /* NOP - wait              */
57  }
58
59  void scl_low (unsigned short portAdr, unsigned char portDelay)
60  /* set SCL output to low     */
61  /* input: portDelay, portAdr */
62  {
63      data |= 0x01;                        /* line D0=1 --> SCL low  */
64      _outp (portAdr, data);               /* send data               */
65      waitPort(portAdr, portDelay);        /* NOP - wait              */
66  }
67
68  unsigned char read_sda (unsigned short portAdr)
69  /* readout of SDA-line       */
70  /* input: portAdr            */
71  /* output: 0 = low, 1 = high */
72  {
73      if (_inp((unsigned short)(portAdr+1)) & 0x40)   /* read ACK   */
74          return (0);
75      else
76          return (1);
77  }
78
79  unsigned char read_scl (unsigned short portAdr)
80  /* readout of SCL-line       */
81  /* input: portAdr            */
82  /* output: 0 = low, 1 = high */
83  {
84      if (_inp((unsigned short)(portAdr+1)) & 0x08)   /* read ERROR */
85          return (0);
86      else
87          return (1);
88  }
89
90  unsigned char read_int (unsigned short portAdr)
91  /* readout of INT-line       */
92  /* input: portAdr            */
93  /* output: 0 = no interrupt  */
94  /*         1 = interrupt     */
95  {
96      if (_inp((unsigned short)(portAdr+1)) & 0x20)   /* read PE    */
97          return (1);         /* signal is low  */
98      else
99          return (0);         /* signal is high */
100 }
```

```
101 /*****************************************************************/
102 /* common I2C-sub-programs:                                      */
103 /*****************************************************************/
104
105 unsigned char i2c_write_byte (unsigned short portAdr,
106                               unsigned char portDelay,
107                               unsigned char w)
108 /* send a byte via I2C-bus                                  */
109 /* after sending MASTER is waiting for an ACK from SLAVE */
110 /* input: portDelay, portAdr                               */
111 /*        w: byte to send                                  */
```

```
112 /* output: 0 = no ACK (time-out), 1 = received ACK       */
113 {
114     unsigned char mask;
115     unsigned char flag;
116
117     mask = 0x80;                            /* mask byte            */
118     do
119     {
120         if (w & mask)                       /* selected bit is 1 ?  */
121             sda_high(portAdr, portDelay);   /* write 1 on SDA       */
122       else
123             sda_low(portAdr, portDelay);    /* write 0 on SDA       */
124
125         scl_high(portAdr, portDelay);       /* SCL to high          */
126         while (!read_scl(portAdr));         /* wait for high SCL    */
127         scl_low(portAdr, portDelay);        /* SCL to low           */
128
129         mask /= 2;                          /* shift mask-bit right */
130     }
131     while (mask);                           /* repeat writing 8x    */
132
133     waitPort(portAdr, portDelay);
134
135     sda_high(portAdr, portDelay);           /* SDA to high          */
136     scl_high(portAdr, portDelay);           /* SCL to high          */
137     while (!read_scl(portAdr));             /* wait for high SCL    */
138
139     if (read_sda(portAdr))                  /* read SDA             */
140         flag = 0;                           /* no ACK               */
141     else
142         flag = 1;                           /* ACK                  */
143
144     scl_low(portAdr, portDelay);            /* SCL to low           */
145
146     return(flag);                           /* return SLAVE answer  */
147 }
148
149 unsigned char i2c_read_byte(unsigned short portAdr,
150                             unsigned char portDelay,
151                             unsigned char ack)
152 /* read a byte via I2C-bus                                  */
153 /* input: portDelay, portAdr                                */
154 /*        ack <> 0, MASTER is sending an ACK                */
155 /* output: 0 = no ACK (time-out), 1 = received ACK          */
156 {
157     unsigned char b, q;
158
159     sda_high(portAdr, portDelay);           /* SDA to high          */
160     b = 0;                                  /* clear byte           */
161     for (q = 0; q < 8; q++)
162     {
163         scl_high(portAdr, portDelay);       /* SCL to high          */
164         while (!read_scl(portAdr));         /* wait for high SCL    */
165
166         b <<= 1;                            /* shift b to left      */
167         if (read_sda(portAdr))              /* if SDA is high       */
168             b |= 1;                         /* set LSB of b to 1    */
169
170         scl_low(portAdr, portDelay);        /* SCL to low           */
171     }
172
173     if (ack)                                /* should send ACK ?    */
174         sda_low(portAdr, portDelay);        /* SDA to low (=>ACK)   */
175     else
176         sda_high(portAdr, portDelay);       /* SDA to high (no ACK) */
177
```

```
178     scl_high(portAdr, portDelay);           /* SCL to high          */
179     while (!read_scl(portAdr));             /* wait for high SCL    */
180
181     waitPort(portAdr, portDelay);
182
183     scl_low(portAdr, portDelay);            /* SCL to low           */
184     sda_high(portAdr, portDelay);           /* SDA to high          */
185
186     return(b);                              /* return byte          */
187 }
188
189 void i2c_start(unsigned short portAdr, unsigned char portDelay)
190 /* send a start condition                                  */
191 /*   a high to low transition on the SDA line              */
192 /*   while SCL is high                                     */
193 /* input: portDelay, portAdr                               */
194 {
195     sda_high(portAdr, portDelay);           /* SDA to high          */
196     scl_high(portAdr, portDelay);           /* SCL to high          */
197     while (!read_scl(portAdr));             /* wait for high SCL    */
198
199     waitPort(portAdr, portDelay);           /* wait                 */
200     sda_low(portAdr, portDelay);            /* SDA to low           */
201     waitPort(portAdr, portDelay);           /* wait                 */
202     scl_low(portAdr, portDelay);            /* SCL to low           */
203 }
204
205 void i2c_stop(unsigned short portAdr, unsigned char portDelay)
206 /* send a stop condition                                   */
207 /*   a low to high transition on the SDA line              */
208 /*   while SCL is high                                     */
209 /* input: portDelay, portAdr                               */
210 {
211     sda_low(portAdr, portDelay);            /* SDA to low           */
212     scl_high(portAdr, portDelay);           /* SCL to high          */
213     while (!read_scl(portAdr));             /* wait for high SCL    */
214
215     waitPort(portAdr, portDelay);           /* wait                 */
216     sda_high(portAdr, portDelay);           /* SDA to high          */
217 }
218
219 int i2c_ok (unsigned short portAdr, unsigned char portDelay)
220 /* testing the I2C-interface on a given port               */
221 /* input: portDelay, portAdr                               */
222 /* output: 0=not found, 1=found                            */
223 {
224     char ret;
225     ret = 1;
226
227     if (_inp((unsigned short)(portAdr+1)) & 0x80)
228                                             /* control BUSY line    */
229         ret = 0;                            /* BUSY is not high     */
230
231     if (ret)                                /* if BUSY is high      */
232     {
233         _outp((unsigned short)(portAdr+2), 0x0c);
234                                             /* SLCT to low          */
235         waitPort(portAdr, portDelay);       /*wait                  */
236         waitPort(portAdr, portDelay);       /*wait                  */
237
238         if (!(_inp((unsigned short)(portAdr+1)) & 0x10))
239                                             /* control ONLINE       */
240             ret = 0;                        /* ONLINE is not high   */
241
242         if (ret)                            /* ONLINE is also high? */
243         {
```

```
244             _outp((unsigned short)(portAdr+2), 0x04);
245                                             /* SLCT to high         */
246             waitPort(portAdr, portDelay);   /*wait                  */
247             waitPort(portAdr, portDelay);   /*wait                  */
248                                             /* control ONLINE       */
249             if (_inp((unsigned short)(portAdr+1)) & 0x10)
250             {                               /* ONLINE is not low    */
251                 ret = 0;
252                 _outp((unsigned short)(portAdr+2), 0x0c);
253             }
254         }
255     }
256     data = 0x00;                            /* clear parallel output*/
257     _outp (portAdr, data);                  /* send data            */
258
259     return (ret);                           /* return status        */
260 }
261
262 unsigned short i2c_init (unsigned char portNr,
263                          unsigned char portDelay)
264 /* init I2C interface                                   */
265 /* input portNr : 0 : search interface on LPT 1..2      */
266 /*                1 : LPT 1                             */
267 /*                2 : LPT 2                             */
268 /*       portDelay                                      */
269 /* output : >0 : adr>0 of LPT-port                      */
270 /*           0 : no I2C interface found                 */
271 {
272     char ok;
273     unsigned short portAdr;                 /* define portAdr local */
274
275     ok = 0;
276     portAdr = 0;
277
278     if (portNr==0)                          /* automat. port-search */
279     {
280         portAdr = 0x378;                    /* set portAdr for LPT1 */
281
282         if (i2c_ok(portAdr, portDelay))     /* look for I2C on LPT1 */
283             ok = 1;                         /* I2C found on LPT1    */
284
285         if (!ok)                            /* no I2C found */
286         {
287             portAdr = 0x37a;                /* set portAdr for LPT2 */
288
289             if (i2c_ok(portAdr, portDelay)) /* look for I2C on LPT2 */
290                 ok = 1;                     /* I2C found on LPT2    */
291         }
292     }
293     else                                    /* I2C on a given LPT   */
294     {
295         switch (portNr)
296         {
297         case 1 : portAdr = 0x378;           /* set portAdr for LPT1 */
298             break;
299         case 2 : portAdr = 0x37a;           /* set portAdr for LPT2 */
300             break;
301         }
302
303         if (i2c_ok(portAdr, portDelay))     /* look for I2C on port */
304             ok = 1;                         /* I2C found            */
305     }
306
307     if (!ok)                                /* no I2C found         */
308         portAdr = 0;                        /* clear portAdr        */
309
```

```
310     return portAdr;                          /* return found address */
311 }
312
313 void i2c_deinit (unsigned short portAdr)
314 /* I2C-interface de-initialising                          */
315 /* input portAdr                                          */
316 {
317     _outp (portAdr, 0);
318     _outp ((unsigned short)(portAdr+2), 0xc);
319 }
```

B.2 LabVIEW to ELV I²C Parallel Port Adapter

Listing B.2 represents the *C* code for a *write*-access interface between LabVIEW and parallel port of a PC. The interface code for a I²C-*read*-access via LabVIEW is shown in listing B.3.

Listing B.2: `write_data.c`: *write* interface code between ELV adapter and LabVIEW

```
1  /* CIN source file */
2
3  #include "extcode.h"
4  #include "i2c.h"
5
6  /* typedefs */
7
8  typedef struct {
9      int32 dimSize;
10     uInt8 data[255];
11     } TD1;
12 typedef TD1 **TD1Hdl;
13
14 CIN MgErr CINRun(uInt16 *portAdr, uInt8 *portDelay, uInt8 *id,
15                  uInt8 *startReg, uInt8 *noReg, TD1Hdl var4,
16                  uInt8 *ack);
17 CIN MgErr CINRun(uInt16 *portAdr, uInt8 *portDelay, uInt8 *id,
18                  uInt8 *startReg, uInt8 *noReg, TD1Hdl var4,
19                  uInt8 *ack)
20 {   TD1   reg;
21     uInt8 count;
22
23     reg = **var4;
24
25     if (*portAdr)
26     {
27         i2c_start(*portAdr, *portDelay);            /* send a START */
28         if (*id)                                    /* Chip Id > 0  */
29             *ack = i2c_write_byte(*portAdr, *portDelay, *id<<1);
30                                                     /* send id      */
31         else                                        /* general call */
32         {
33             *ack = i2c_write_byte(*portAdr, *portDelay, 0);
34                                                     /* first byte   */
35             if (*ack)                               /* no error ?   */
36                 *ack = i2c_write_byte(*portAdr, *portDelay, 1);
37                                                     /* second byte  */
38                                                     /* master adr=0 */
39         }
40
41         if (*ack)                                   /* no error ?   */
42         {
43             *ack = i2c_write_byte(*portAdr, *portDelay, *startReg);
44                                                     /* send reg.    */
45
```

```
46              count = 0;                                  /* start counter*/
47              do
48              {
49                  *ack = i2c_write_byte(*portAdr, *portDelay,
50                              reg.data[count]);           /* send data    */
51
52                  count++;                                /* inc counter  */
53
54              }
55              while (*ack && (count<*noReg));
56
57              if (*ack)                                   /* no error ?   */
58                  i2c_stop(*portAdr, *portDelay);
59          }
60      }
61      else
62          *ack = 0;
63
64      return noErr;
65  }
```

Listing B.3: `read_data.c`: *read* interface code between ELV adapter and LabVIEW

```
1  /* CIN source file */
2
3  #include "extcode.h"
4  #include "i2c.h"
5
6  /* typedefs */
7
8  typedef struct {
9      int32 dimSize;
10     uInt8 data[255];
11     } TD1;
12 typedef TD1 **TD1Hdl;
13
14 CIN MgErr CINRun(uInt16 *portAdr, uInt8 *portDelay, uInt8 *id,
15                  uInt8 *startReg, uInt8 *noReg, TD1Hdl var4,
16                  uInt8 *ack);
17 CIN MgErr CINRun(uInt16 *portAdr, uInt8 *portDelay, uInt8 *id,
18                  uInt8 *startReg, uInt8 *noReg, TD1Hdl var4,
19                  uInt8 *ack)
20 {
21     TD1   reg;
22     uInt8 count;
23
24     reg = **var4;
25
26     if (*portAdr)
27     {
28         i2c_start(*portAdr, *portDelay);            /* send a START */
29
30         *ack = i2c_write_byte(*portAdr, *portDelay, *id<<1);
31                                                     /* send id      */
32         if (*ack)                                   /* no error ?   */
33         {
34             *ack = i2c_write_byte(*portAdr, *portDelay, *startReg);
35                                                     /* send reg.    */
36             if (*ack)                               /* no error ?   */
37             {
38                 i2c_start(*portAdr, *portDelay);    /* send a START */
39                 *ack=i2c_write_byte(*portAdr, *portDelay, (*id<<1)|1);
40             }                                       /* send id.     */
41         }
42
43         if (*ack)                                   /* no error ?   */
```

```
44          {                                                   /* start readout*/
45              count = 0;                                      /* start counter*/
46
47              do
48              {
49                  reg.data[count] = i2c_read_byte(*portAdr, *portDelay,
50                                  count+1<*noReg);            /* read data    */
51                  count++;                                    /* inc counter  */
52              }
53              while (count<*noReg);
54
55              if (*ack)                                       /* no error ?   */
56                  i2c_stop(*portAdr, *portDelay);
57          }
58
59          **var4 = reg;
60      }
61      else
62          *ack = 0;
63
64      return noErr;
65  }
```

Appendix C

The Beetle Reference Manual

The Beetle Reference Manual

— chip version 1.3, 1.4 and 1.5 —

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document version: 1.73

Abstract

This paper details the electrical specifications, operating conditions and port definitions of the readout chips *Beetle1.3*, *1.4* and *1.5*. The chip is developed for the LHCb experiment and fulfils the requirements of the silicon vertex detector (VELO, PUS[1]), the silicon tracker and the RICH detectors in case of multi-anode photomultiplier readout.

It integrates 128 channels with low-noise charge-sensitive preamplifiers and shapers. The pulse shape can be chosen such that it complies with LHCb specifications: a peaking time of 25 ns with a remainder of the peak voltage after 25 ns of less than 30%. A comparator per channel with configurable polarity provides a binary signal. Four adjacent comparator channels are being ORed and brought off chip via LVDS ports. Either the shaper or comparator output is sampled with the LHC bunch-crossing frequency of 40 MHz into an analogue pipeline. This ring buffer has a programmable latency of max. 160 sampling intervals and an integrated derandomising buffer of 16 stages. For analogue readout data is multiplexed with up to 40 MHz onto 1 or 4 ports. A binary readout mode operates at up to 80 MHz output rate on two ports. Current drivers bring the serialised data off chip. The chip can accept trigger rates up to 1.1 MHz to perform a dead-timeless readout within 900 ns per trigger. For testability and calibration purposes, a charge injector with adjustable pulse height is implemented. The bias settings and various other parameters can be controlled via a standard I^2C-interface.

Appropriate design measures have been taken to ensure the radiation hardness against total dose effects in excess of 100 Mrad. Robustness against Single Event Upset is achieved by redundant logic.

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Contents

Document Edition History

This manual describes the three *Beetle* chip versions 1.3, 1.4 and 1.5.
For *Beetle* versions 1.0 and 1.1 please refer to the corresponding version of this manual (LHCb-note 2001-046), for *Beetle1.2* to the corresponding manual "The *Beetle* Reference Manual - version 1.2".

Version	Date	Author	Description
1.0	11.03.2004	DB, SL	document created
1.1	04.04.2004	SL	updated missing measurement values
1.2	12.04.2004	SL	pulse-parameters
1.3	16.04.2004	SL	modified chap. C.4.2, Rclk divider
1.4	03.05.2004	SL	new table C.10 (*Ipipe* / *Ivoltbuf*), modified standard settings table C.14
1.5	16.06.2004	SL	add modifications for *Beetle1.4* and *Beetle1.5*
1.51	23.06.2004	SL	modified first page (new coordinates for N. Bakel)
1.52	06.10.2004	SL	modified chap. C.7.2 and chap. C.7.4 (corrected *Beetle* version numbers)
1.53	24.11.2004	SL	modified wrong link in history table
1.54	05.01.2005	SL	revised document
1.55	03.03.2005	SL	add remarks to power-up reset (C.3.4) and `EnableEDC` pad (C.4.3)
1.6	09.04.2005	SL	changed description of *Beetle* Revision Id., modified organisation and programming of shift registers, modified section C.3.7, add default values for *ROCtrl* in table C.11
1.61	19.05.2005	SL	revised document
1.62	09.07.2005	SL	revised table C.14
1.63	10.07.2005	SL	fixed an error in table C.1 (DC characteristics), additional comment to the programming of shift registers in chapter C.5
1.64	15.07.2005	SL	add layout of mother board (fig. C.27 and C.28)
1.65	01.08.2005	SL	fixed wrong reference
1.66	23.09.2005	SL	minor modifications
1.67	15.11.2005	SL	minor modifications, changed VETO to PUS
1.68	23.11.2005	SL	modified comparator description (cf. section C.3.7)
1.69	07.03.2006	SL	modified description of comparator low-pass filter (cf. section C.3.7)
1.70	07.04.2006	SL	revised document
1.71	05.05.2006	SL	revised document
1.72	15.05.2006	SL	revised document
1.73	05.06.2006	SL	add *Beetle* chip version bug description (cf. section C.6)

Chip Version History

Version	Submission Date	Changes relating to previous version
Beetle1.0	April 2000	
Beetle1.1	March 2001	extended test channel including pipeamp output, modified pipeline layout analogue delay element for I^2C-SDA line added modified pipeamp, modified bias network of pipeamp modified multiplexer modified tristate buffer in control circuit
Beetle1.2	April 2002	implementation of a new front-end (set 2c of *BeetleFE1.1*) modified analogue input pad geometry (elongated pad opening) introduction of SEU robustness scheme restriction of readout time to 900 ns introduction of 8 additional status bits in data header introduction of a power-up reset introduction of comparator mask and test pulse selection bit per channel on-chip trigger synchronisation hard-wired I^2C-chip address (defined via bond pads) introduction of SCHMITT-triggers in the I^2C-pads reduced DAC resolution from 10 to 8 bits, increased max. bias current to 2 mA
Beetle1.3	June 2003	fix of sticky charge effect: analogue delay of `MuxTrack` signal increased comparator channel threshold resolution (5 bits) improved output buffer: fully diff. current buffer, increased gain bug fixes in control logic: daisy chain operation, reduced Rclk frequency new I^2C-pads: 5 V compatible reduced number of flip-flops in multiplexer (from 414 to 138) reduced number of clock buffers in logic core (from 275 to 104) on-chip blocking of power nets (total blocking capacitance: $\mathcal{O}(1\,\text{nF})$) modified front-end power pad distribution improved shaper power routing, improved front-end biasing scheme separation of comparator core power from comparator LVDS power improved pipeamp power routing split power supply of multiplexer and logic core, improved multiplexer timing implementation of two new power pads for logic core merged pad openings of adjacent power pads improved guard-ring structures (n-well and substrate contacts) increased overall chip size by 300 µm in x: $5\,400 \times 6\,100\,\mu\text{m}^2$
Beetle1.4	May 2004	fixed parity bit of Pipeline Column Number (PCN) fixed even/odd crosstalk in pipeline new modified comparator changed *Beetle* revision number, add optical alignment markers
Beetle1.5	May 2004	split analogue power of front-end and comparator into two nets new pipeline cell new multiplexer timing (to reduce the header crosstalk) modified pipeamp, improved power routing changed *Beetle* revision number new test structure

C.1 Chip Architecture

The *Beetle* can be operated as analogue or alternatively as binary pipelined readout chip. It implements the basic RD20 front-end electronics architecture [1, 2, 3]. Figure C.1 shows a schematic block diagram of the chip.

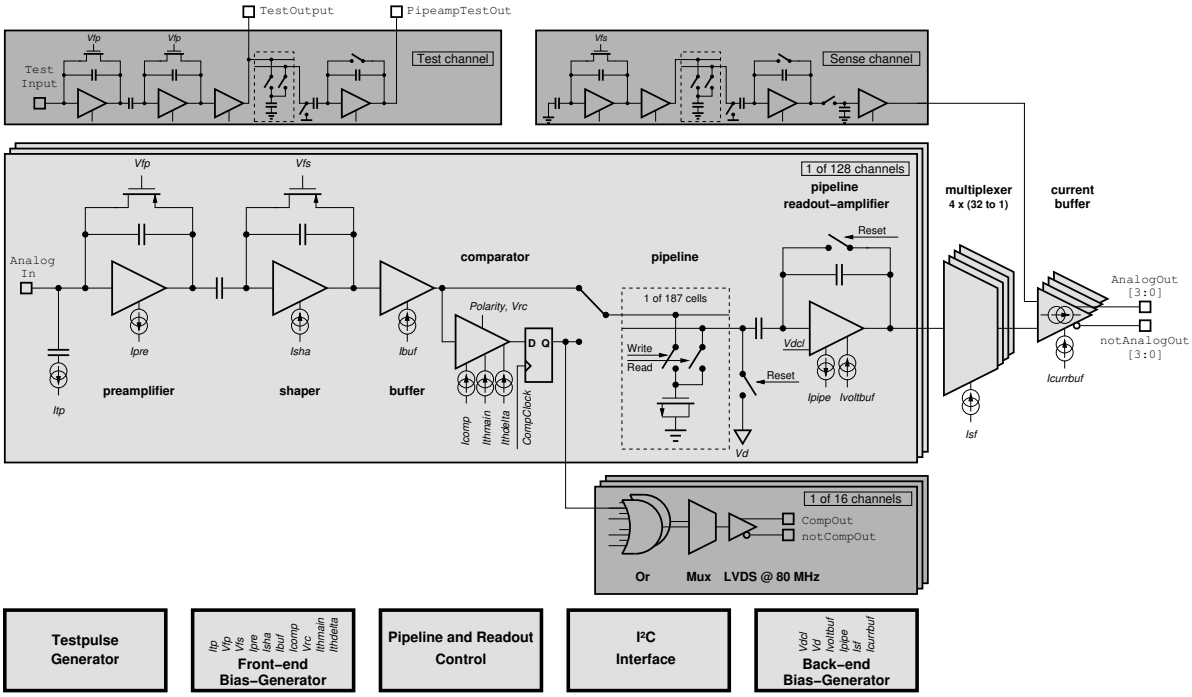


Figure C.1: Schematic block diagram of the *Beetle* readout chip.

The chip integrates 128 channels, each consisting of a low-noise charge-sensitive preamplifier, an active CR-RC pulse shaper and a buffer. They form the analogue front-end. The equivalent noise charge (ENC) of the front-end has been measured as $\mathrm{ENC} = 497\,\mathrm{e}^- + 48.3\,\mathrm{e}^-/\mathrm{pF} \cdot C_{\mathrm{in}}$. The shape of the front-end pulse can be chosen according to the specific requirements of the application. The minimum rise time (10-90%) is well below 25 ns, the remainder of the peak voltage after 25 ns can be adjusted to less than 30% for load capacitances $C_{\mathrm{in}} \leq 35\,pF$. A comparator discriminates the front-end's output pulse. The threshold is adjustable per channel and input signals of both polarities can be processed. Four adjacent comparator channels are grouped by a logic OR, latched, multiplexed by a factor of 2 and routed off the chip via low voltage differential signalling (LVDS) ports at 80 MHz. Either the shaper- or the comparator output is sampled with the LHC bunch-crossing frequency of 40 MHz into an analogue pipeline which has a programmable latency of max. 160 sampling intervals and an integrated multi-event buffer of 16 stages. The signal stored in the pipeline is transfered to the multiplexer via a resettable charge-sensitive amplifier (pipeamp). Within a readout time of 900 ns current drivers bring the serialised data off chip. The output of a dummy channel is subtracted from the analogue data to compensate common mode effects. All amplifier stages are biased by forced currents. On-chip digital-to-analogue converters (DACs) with 8 bit resolution generate the bias currents and voltages. For test and calibration purposes a charge injector with adjustable pulse height is implemented on each channel. The bias settings and various other parameters like the trigger latency can be controlled via a standard $\mathrm{I}^2\mathrm{C}$-interface [6]. All digital control and data signals, except those for the $\mathrm{I}^2\mathrm{C}$-ports, are routed via LVDS ports.

The choice of a deep-submicron process technology (0.25 µm standard CMOS) with a thin gate oxide ($t_{ox} \approx 62$ Å) and the consistent use of enclosed NMOS transistors reduces a shift in the transistor threshold voltage and eliminates "end-around" leakage current paths. This establishes a total dose radiation hardness in excess of 130 Mrad. Single Event Latch-up (SEL) is suppressed by means of guard-rings. The continuous use of triple-redundant logic ensures a robustness against Single Event Upset (SEU).

C.2 Electrical Specifications

C.2.1 DC Characteristics

Table C.1: DC characteristics of *Beetle*

Supply	Min. [V]	Nom. [V]	Max. [V]	Description
Vdda	2.3	2.5	2.7	Positive analogue supply (back-end)
Gnda	-0.2	0.0	0.2	Negative analogue supply (back-end)
Vddd	2.3	2.5	2.7	Positive digital supply
Gndd	-0.2	0.0	0.2	Negative digital supply
VddPre	2.3	2.5	2.7	Positive analogue preamplifier supply
GndPre	-0.2	0.0	0.2	Negative analogue preamplifier supply (detector ground)
VddaComp	2.3	2.5	2.7	Positive analogue comparator supply (*only Beetle1.5*)
GndaComp	-0.2	0.0	0.2	Negative analogue comparator supply (*only Beetle1.5*)
VdddComp	2.3	2.5	2.7	Positive digital comparator supply
GnddComp	-0.2	0.0	0.2	Negative digital comparator supply
VddCPB	2.3	2.5	2.7	Positive comparator pad supply at bottom side
GndCPB	-0.2	0.0	0.2	Negative comparator pad supply at bottom side
VddCPT	2.3	2.5	2.7	Positive comparator pad supply at top side
GndCPT	-0.2	0.0	0.2	Negative comparator pad supply at top side
VddMux	2.3	2.5	2.7	Positive multiplexer supply
GndMux	-0.2	0.0	0.2	Negative multiplexer supply
VddTX	2.3	2.5	2.7	Positive output driver supply
GndTX	-0.2	0.0	0.2	Negative output driver supply

Power Consumption Typical values for the power consumption of a *Beetle* chip are given in table C.2 for various setup configurations. Nominal register settings refer to table C.14.

Table C.2: Typical power consumption.

Chip configuration					I_{supply} [mA]		P [mW/ch]	
Comparator		Clock	Trigger		analogue readout ports			
LVDS term.	digital	40 MHz	1.1 MHz	Registers	1	4	1	4
open	disabled	no	no	0	24.5	24.5	0.48	0.48
open	disabled	yes	no	0	64.5	64.5	1.26	1.26
open	disabled	yes	yes	0	64.5	64.5	1.26	1.26
open	disabled	no	no	nom.	192.0	221.5	3.75	4.33
open	disabled	yes	no	nom.	232.0	261.5	4.53	5.11
open	disabled	yes	yes	nom.	237.0	267.0	4.63	5.21

C.2.2 Signal Levels

The *Beetle* chip has 3 different kind of I/O pads. The signal levels for these pads are given in table C.3.

Table C.3: Specification of signal levels.

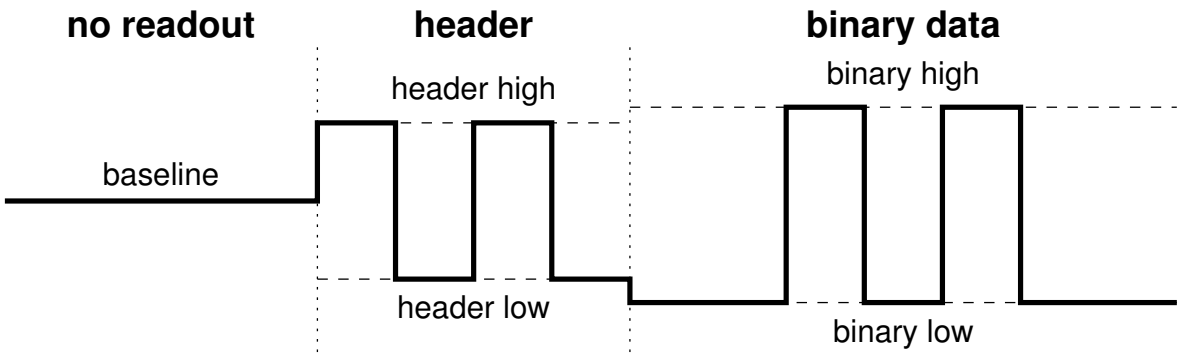
I^2C							
	logic 0			logic 1			Unit
	Min.	Max.	Typ.	Min.	Max.	Typ.	
input	-0.7	1.1	0.0	1.5	7.0	2.5	V
output	—	—	0.0	—	—	2.5	V
CMOS							
	logic 0			logic 1			Unit
	Min.	Max.	Typ.	Min.	Max.	Typ.	
input	-0.7	1.1	0.0	1.4	3.3	2.5	V
output	—	—	0.0	—	—	2.5	V
LVDS (100 Ω termination)							
	offset voltage			differential voltage			Unit
	Min.	Max.	Typ.	Min.	Max.	Typ.	
input	0.0	2.5	1.2	0.1	2.5	0.2	V
output	—	—	1.02	—	—	1.38	V

C.2.3 Output Characteristics

The *Beetle* chip provides an *analogue* as well as a *binary* output mode. A differential current is transmitted in each case by the *Beetle* current output driver.

Figure C.2 specify the signal levels of the *Beetle* current output driver for different modes of operation. All levels were measured with a 100 Ω termination resistor between `AnalogOut<X>` and `notAnalogOut<X>`. The internal current of the output driver was programmed to the nominal value given in table C.3.

Figure C.3 gives an example of a receiver circuit for analogue signals using the AD8130 transimpedance amplifier [4] and binary signals using the DS90C032 [5] LVDS receiver.



		BinaryHeader: ON CompDisable: OFF PipelineMode: ON			BinaryHeader: OFF CompDisable: OFF PipelineMode: ON			BinaryHeader: OFF CompDisable: ON PipelineMode: ON			BinaryHeader: OFF CompDisable: ON PipelineMode: OFF		
		V_{AO} [mV]	$V_{\overline{AO}}$ [mV]	I_{out} [mA]	V_{AO} [mV]	$V_{\overline{AO}}$ [mV]	I_{out} [mA]	V_{AO} [mV]	$V_{\overline{AO}}$ [mV]	I_{out} [mA]	V_{AO} [mV]	$V_{\overline{AO}}$ [mV]	I_{out} [mA]
baseline		1152	824	3.28	973	978	-0.05	973	978	-0.05	973	978	-0.05
header	high	840	1184	-3.44	916	1058	-1.42	916	1058	-1.42	916	1058	-1.42
	low	1152	824	3.28	1014	912	1.29	1014	912	1.29	1014	912	1.29
binary	high	760	1432	-6.72	760	1432	-6.72	1121	842	2.79	analogue readout		
	low	1164	816	3.48	1164	816	3.48						

Figure C.2: Current output driver levels, measured over a 100 Ω resistor

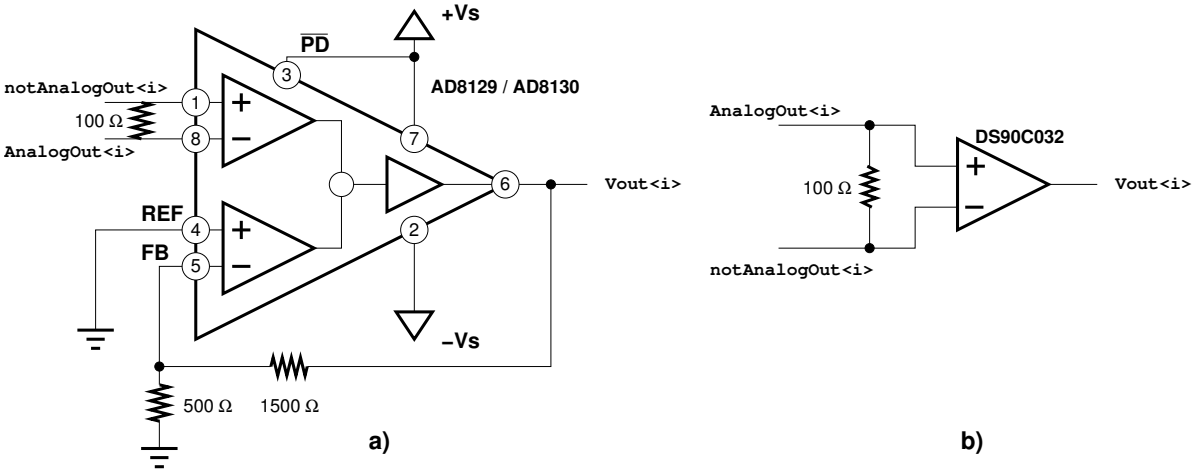


Figure C.3: Example of a receiver circuit for the analogue (a) and binary (b) output signals. In case of analogue signals the AD8130 amplifier is used, in case of binary signals the DS90C032 LVDS receiver.

C.3 Operating the *Beetle* Chip

C.3.1 Front-end Pulse Shape

The front-end output signal is a semi-Gaussian pulse which can be characterised by three parameters:

- peaking time t_p $(0-100\%)$ or rise time t_r $(10-90\%)$,
- peaking voltage V_p and
- remainder R, which is the ratio between the signal voltage 25 ns after the peak (V_{25+}) and V_p.

The peaking time is sometimes hard to measure since the starting point of the pulse is not well defined, so the rise time t_r $(10-90\%)$ is usually quoted. Figure C.4 explains the various parameters.

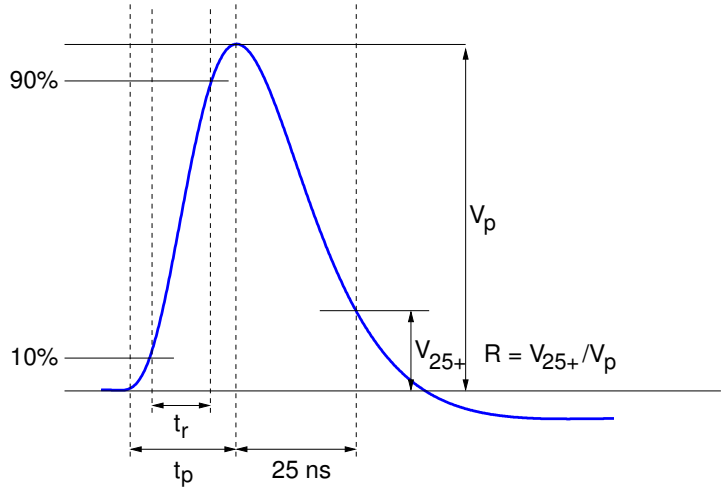


Figure C.4: Semi-Gaussian pulse with the corresponding parameters characterising the shape.

Information about the front-end's pulse shape can be obtained on a *Beetle* readout chip from either the test channel output (`TestOutput`, pad no. 242) or from a *pulse shape scan*. Here, the front-end's output is read out via the pipelined path while the preamplifier input signal is shifted w. r. t. the sampling clock.

The pulse shape can be varied by 5 bias parameters:

Ipre sets the preamplifier bias current. Higher currents decrease the rise time and the remainder and increase the pulse undershoot.

Isha defines the shaper bias current. Increasing currents shift the DC-offset to lower values and result in a slightly decreasing rise time, remainder and undershoot.

Ibuf sets the buffer bias current. It does not affect the shape of the pulse, but the DC-offset.

Vfp determines the preamplifier feedback resistance. It defines the time constant for discharging the preamplifier's integration capacitor and therefore the tolerable input charge rate.

Vfs controls the shaper feedback resistance. Increasing *Vfs* values enlarge the peaking time, the peaking voltage as well as the remainder (cf. figure C.6).

Figure C.5 depicts the variation of the pulse shape for four example bias parameter settings. For the nominal settings listed in table C.14, i.e. Ipre = 600 µA, Isha = Ibuf = 80 µA, Vfp = Vfs = 0 V, the front-end sensitivity $A_Q = V_{FEout}/Q_{in} = 38\,\text{mV}/22\,000\,\text{e}^- = 38\,\text{mV/MIP}$.

The behaviour of the front-end pulse parameters is strongly coupled to the detector load capacitances. Figure C.6 shows the variation of

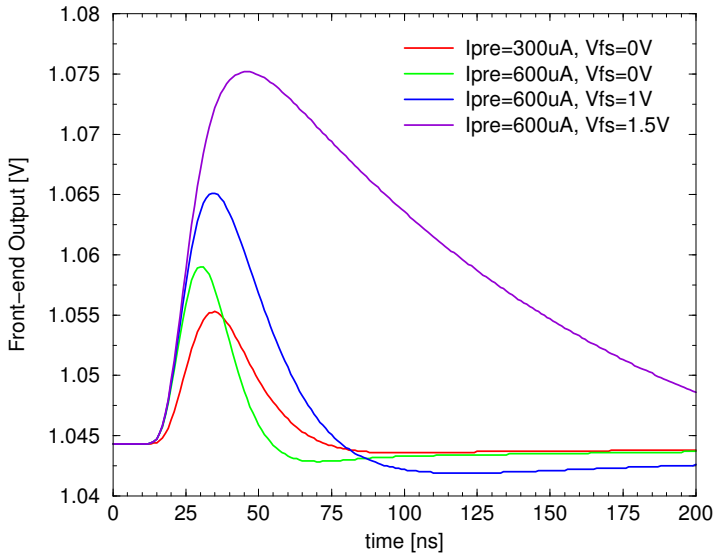


Figure C.5: Variation of simulated front-end pulse shapes for settings (Isha = Ibuf = 80 µA, Vfp = 0 V).

- peaking time t_{p} $(0-100\%)$ [upper left plot],
- rise time t_{r} $(10-90\%)$ [upper right plot],
- peaking voltage V_{p} [lower left plot] and
- remainder R [lower right plot]

for different detector capacitances and for four different shaper feedback settings *Vfs*.

C.3.2 Equivalent Noise Charge

The equivalent noise charge (ENC) of a complete *Beetle1.3* readout chip has been measured for different front-end settings. ENC values are given in table C.4 for different shaper feedback settings *Vfs*. Nominal register settings refer to table C.14. For *Beetle1.4* and *Beetle1.5* one expects roughly the same results, because all three chip versions have the same front-end.

Table C.4: Measured equivalent noise charge of *Beetle1.3* for different shaper feedback settings *Vfs*.

Vfs [mV]	Equivalent noise charge
0	$\mathrm{ENC} = 547.7\,\mathrm{e}^- + 52.64\,\mathrm{e}^-/\mathrm{pF} \cdot C_{\mathrm{in}}$
100	$\mathrm{ENC} = 539.1\,\mathrm{e}^- + 51.89\,\mathrm{e}^-/\mathrm{pF} \cdot C_{\mathrm{in}}$
400	$\mathrm{ENC} = 542.8\,\mathrm{e}^- + 49.38\,\mathrm{e}^-/\mathrm{pF} \cdot C_{\mathrm{in}}$
1000	$\mathrm{ENC} = 465.1\,\mathrm{e}^- + 45.22\,\mathrm{e}^-/\mathrm{pF} \cdot C_{\mathrm{in}}$

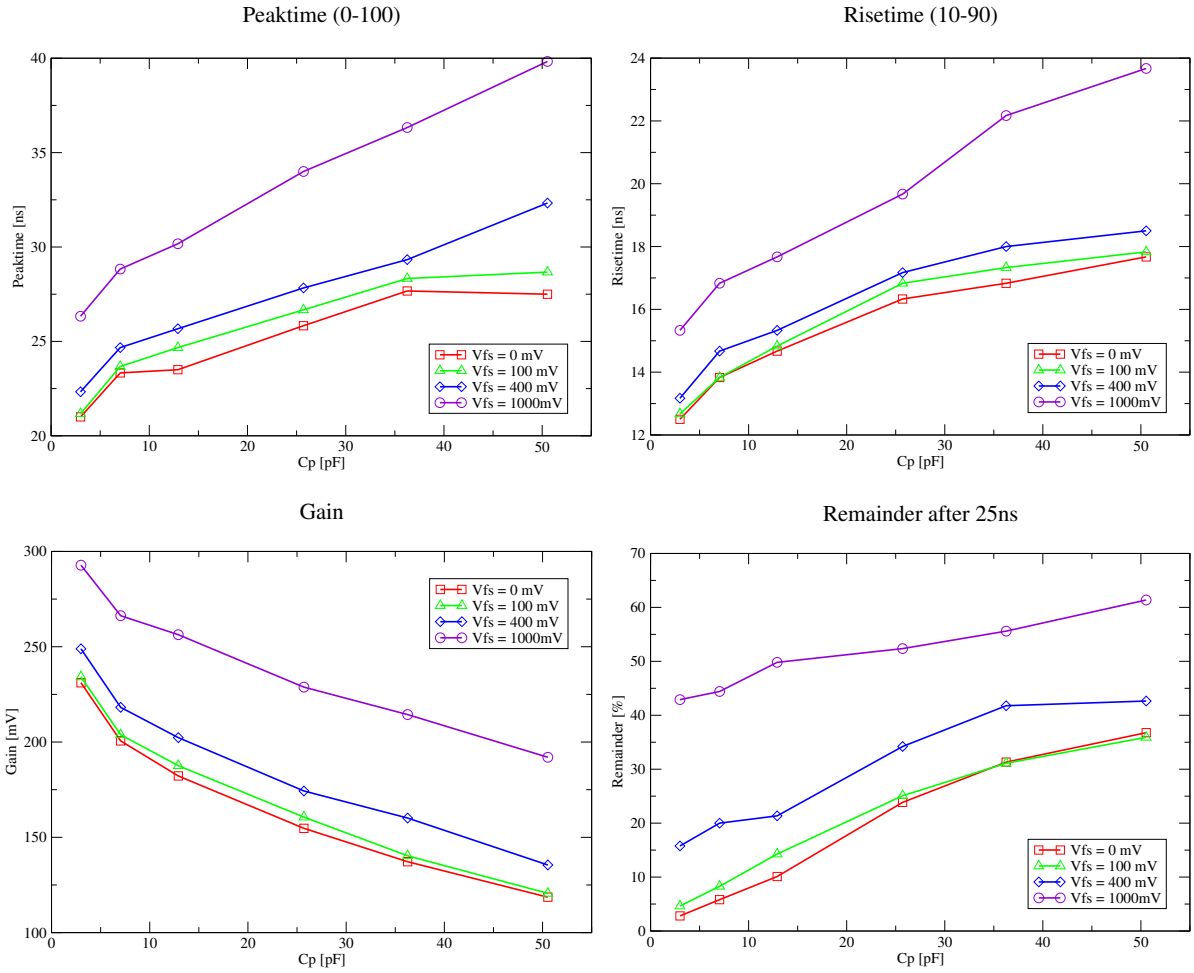


Figure C.6: Front-end pulse parameters for different shaper settings *Vfs* and different detector load capacitances C_p

C.3.3 Test Channel

The *Beetle* chip integrates beside the 128 channels a *test channel* with direct access to the front-end output (`TestOutput`, pad no. 242 on *Beetle1.3* and *1.4* resp. pad no. 243 on *Beetle1.5*) as well as the pipeamp output (`PipeampTestOut`, pad no. 218 (*1.3* and *1.4*) resp. 217 (*1.5*)). An input charge can be injected either via the `TestInput` port (pad no. 6) or via the internal test pulse generator (+1 step, cf. C.3.6). Additionally, 5 internal voltage nodes of the test channel's front-end are accessible on test pads: `Prebias`, `Prebias1`, `Shabias`, `Shabias1` and `Bufbias`. Figure C.7 illustrates the various bias nodes, which are common for all *Beetle* front-ends.

C.3.4 Reset Modes

Two different types of reset exist on *Beetle*.

- *Power-up reset* is activated immediately when the power of the chip is switched on. The reset's time-constant, i.e. the time between "power-on" and the reset becoming inactive, can be adjusted via an external capacitance connected to the `PowerupReset` pad no. 192. For typical capacitance values like $C_\mathrm{ext} = 10\,\mathrm{nF}$ (100 nF), the time constant τ results in $\tau = 28\,\mathrm{ms}$ (280 ms). All *Beetle*

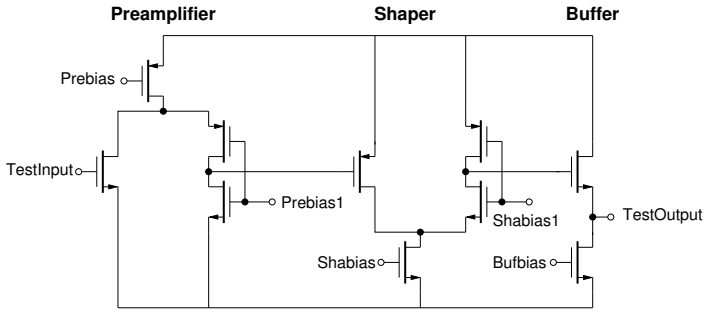


Figure C.7: Test channel bias nodes.

registers are reset to 0 and the I^2C-interface is initialised.
Manual access to the power-up reset control is also possible via the `PowerupReset` pad. The reset is enabled by switching this pad to Gnd and accordingly set the chip back to operation mode by connecting the pad to Vdd[2].

- *External reset* is controlled by the `Reset` port (see section C.7.3). It resets the pipeline write and trigger pointer to column number 0 and initialises the control logic's state machines. The rising edge of `Reset` re-initialises also the I^2C-interface. The minimum reset width is 25 ns, i.e. one sampling clock cycle.

C.3.5 Readout Modes

The readout of the *Beetle* chip is synchronous to the readout clock *Rclk*, which is generated on-chip from the sampling clock *Sclk* (`Clk` port). For operation at LHC, sampling and readout clock have the same frequency. For other applications, the readout clock frequency can be reduced to a fraction of *Sclk* (cf. C.4.2).

The *Beetle* readout chip provides three different readout modes[3]:

Analogue readout on 4 ports Each port carries 4 header bits plus 32 channels. Data transmission is synchronous to the rising edge of the readout clock and takes 900 ns per trigger.

Binary readout on 2 ports Each port carries 8 header bits plus 64 channels. Data transmission is synchronous to both edges of *Rclk*. The readout takes 900 ns per trigger.

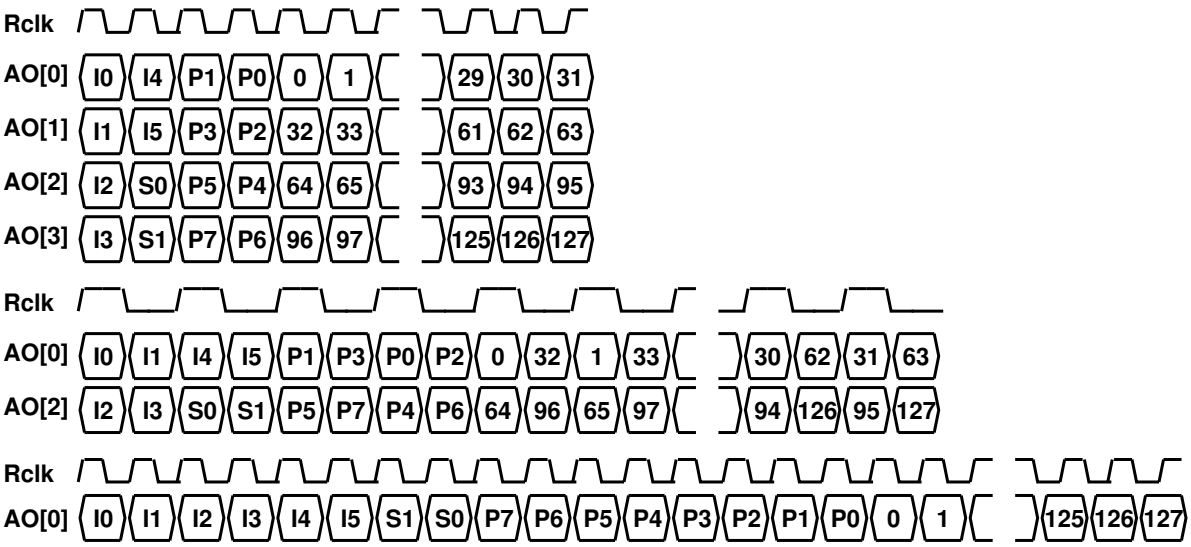
Analogue readout on 1 port This is for applications with less demanding readout speed requirements. The readout lasts 3.6 µs per trigger.

Figure C.8 shows the assignment of the header bits and analogue input channels to the output channels in the different modes. The meaning of the various header bits is described beneath the assignment.

C.3.6 Internal Test Pulses

Test pulses can be injected into the preamplifier with an on-chip generator. A step like pattern corresponding to +1 and −1 times a reference signal amplitude is coupled to the 129 channels (table C.5). Its amplitude alternates with the channel number and can be adjusted with the *Itp* bias register (cf. table C.14). A test pulse is triggered via the rising edge of `Testpulse` signal (pad no. 177, 178) and can be enabled per channel by the *TpSelect* register (cf. C.4.2). Figure C.9 shows the correlation between the `Testpulse` port and the internal test pulse trigger. The test pulse is independent from `Clk`.

[2] reset enable: signal level of `PowerupReset` < 0.410 V; reset disable: signal level > 1.950 V
[3] The specification of the readout time assumes $Rclk = Sclk = 40$ MHz.



From top to bottom: Analogue readout mode: 32 analogue channels are multiplexed onto 4 ports with up to 40 MHz. Binary readout mode: 64 binary channels are multiplexed onto 2 ports with up to 80 MHz. Readout mode for less demanding readout speed requirements: 128 analogue channels are multiplexed onto 1 port with up to 40 MHz.

Bit		Description
I0	LeadingBit	always active (= 1)
I2	ActiveEDC	1 indicates active error detection and correction (EDC) logic
I3	ParCompChTh	(even) parity of register *CompChTh* (reg. no. 20, cf. table C.14)
I4	ParCompMask	(even) parity of register *CompMask* (reg. no. 21, cf. table C.14)
S0		LSB of register *SEUcounter* (reg. no. 23, cf. table C.14)
S1		bit 1 of register *SEUcounter* (reg. no. 23, cf. table C.14)
P0		LSB of pipeline column number
P1		bit 1 of pipeline column number
P2		bit 2 of pipeline column number
P3		bit 3 of pipeline column number
P4		bit 4 of pipeline column number
P5		bit 5 of pipeline column number
P6		bit 6 of pipeline column number
P7		MSB of pipeline column number
special for ***Beetle1.3***:		
I1	ParPCN	(even) parity of pipeline column number (PCN)
I5	ParTpSelect	(even) parity of register *TpSelect* (reg. no. 22, cf. table C.14)
special for ***Beetle1.4* and *Beetle1.5***:		
I1	ParTpSelect	(even) parity of register *TpSelect* (reg. no. 22, cf. table C.14)
I5	ParPCN	(even) parity of pipeline column number (PCN)

Figure C.8: *Beetle* readout data formats and definition of the header bits. I1 and I5 are swapped between *Beetle1.3* and *Beetle1.4 / 1.5*.

Table C.5: Mapping of test pulse amplitudes to analogue channels.

Channel no.	Test channel	0	1	2	3	...	124	125	126	127
Test pulse step height	∓ 1	± 1	∓ 1	± 1	∓ 1	...	± 1	∓ 1	± 1	∓ 1

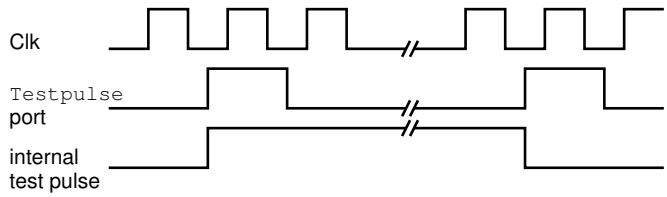


Figure C.9: Test pulse triggering.

Calibration The relation between *Itp* and the injected charge Q_{in} is given:

- $Q_{\text{in}} = 131.2\,\text{e}^-/\mu\text{A} \cdot I_{\text{tp}}$

or

- $Q_{\text{in}} = 1\,025\,\text{e}^-/[\text{regbit}] \cdot I_{\text{tp}}\,[\text{regbit}]$

C.3.7 Comparator Operation

The comparator circuit consists of an integrator, a threshold generator and a discriminator. The integrator tracks the DC-offset of the shaped pulse with a variable time constant τ between 16 µs and 10 ms, which can be adjusted via the *Vrc* register (cf. table C.14). The programmable range of *Vrc* is between 0 and 1.25 V, but only values up to 330 mV will have an influence to the time constant of the low-pass filter. A more detailed view of the correlation between *Vrc* and τ is shown in table C.6. The DC-offset vary from channel to channel and is added to the threshold voltage. The threshold level is adjustable with a resolution of 5 bits per channel. With the rising edge of the comparator's own `CompClock` (pad no. 146, 147) the discriminator output is sampled.

Comparator Configuration

The comparator is configured via the register *CompControl* (see table C.12 and table C.14). *PipelineMode* defines the mode of operation of the comparator. *PipelineMode* = 0 selects the analogue mode, in which the output of the front-end amplifier is transferred to the pipeline. In binary mode (*PipelineMode* = 1) the comparator output is fed into the pipeline. *CompDisable* = 1 turns off the comparator's bias current. *CompPolarity* selects between an inverting (0) or non-inverting (1) comparator operation. *CompMode* switches between two different kinds of output signal. With *CompMode* = 0 the output is active as long as the comparator input signal is above the threshold level. With *CompMode* = 1 the output is only active for one `CompClock` cycle, independent from the time the input signal is above the threshold.

Table C.6: Correlation between *Vrc* and the time constant τ of the comparator low-pass filter.

Vrc	τ	*Vrc*	τ
0 mV	16.3 µs	200 mV	375.8 µs
20 mV	18.0 µs	220 mV	558.1 µs
40 mV	24.7 µs	240 mV	920.8 µs
60 mV	31.6 µs	280 mV	1.4 ms
80 mV	41.6 µs	300 mV	4.6 ms
100 mV	56.3 µs	320 mV	9.2 ms
120 mV	78.7 µs	340 mV	>10.0 ms
140 mV	112.3 µs		
160 mV	164.4 µs		
180 mV	245.5 µs		

Threshold Adjustment

The threshold level is generated from two programmable currents. *Ithmain* (register address 8) determines the global threshold, which is common to all channels. *Ithdelta* (register address 7) defines an additional delta threshold.

The comparator threshold register (*CompChTh*, address 20) selects the number of delta thresholds which are being subtracted from the global threshold. This register is operated as a shift register. The bits *CompChTh[4:0]* are being assigned to channel *k*. To define the delta threshold of all channels, the *CompChTh* register has to be programmed 128 times consecutively. A shift mechanism provides the bits to the channels in the order Ch[0], Ch[1], Ch[2],..., Ch[126], Ch[127].

Comparator Masking

The comparator mask register (*CompMask*, address 21) deactivates the operation of a single comparator channel. Eight adjacent channel mask bits are combined to one group and can be programmed via the shift register *CompMask*.

A detailed description of the mapping and programming of the shift register is explained in chapter C.4 and especially in fig. C.16.

Comparator Channel Mapping

The comparator outputs are LVDS drivers. Each driver sends data of two combined comparator groups, the first group of ORed channels during the high phase of `CompClock`, the second during the low phase. The mapping of the channels to the comparator outputs is shown in table C.7.

C.3.8 Timing Specifications

Reset, Trigger, Testpulse The timing relation between *Reset* and *Trigger* in order to trigger on pipeline column number n can be depicted from fig. C.10, whereas $n = k$ modulo 187. k must be equal or greater than 1, *Latency* refers to the content of the Latency register (no. 16). **The external *Reset* and *Trigger* signals are sampled internally to the negative edge of *Clk*.**

Figure C.11 depicts the timing relation between *Testpulse* and *Trigger*. *Latency* refers again to the content of the Latency register.

Table C.7: Mapping of analogue input channels to comparator output channels.

Output port	High phase of `CompClock`	Low phase of `CompClock`
CompOut[15]	Ch[127]∨Ch[126]∨Ch[125]∨Ch[124]	Ch[123]∨Ch[122]∨Ch[121]∨Ch[120]
CompOut[14]	Ch[119]∨Ch[118]∨Ch[117]∨Ch[116]	Ch[115]∨Ch[114]∨Ch[113]∨Ch[112]
CompOut[13]	Ch[111]∨Ch[110]∨Ch[109]∨Ch[108]	Ch[107]∨Ch[106]∨Ch[105]∨Ch[104]
CompOut[12]	Ch[103]∨Ch[102]∨Ch[101]∨Ch[100]	Ch[99]∨Ch[98]∨Ch[97]∨Ch[96]
CompOut[11]	Ch[95]∨Ch[94]∨Ch[93]∨Ch[92]	Ch[91]∨Ch[90]∨Ch[89]∨Ch[88]
CompOut[10]	Ch[87]∨Ch[86]∨Ch[85]∨Ch[84]	Ch[83]∨Ch[82]∨Ch[81]∨Ch[80]
CompOut[9]	Ch[79]∨Ch[78]∨Ch[77]∨Ch[76]	Ch[75]∨Ch[74]∨Ch[73]∨Ch[72]
CompOut[8]	Ch[71]∨Ch[70]∨Ch[69]∨Ch[68]	Ch[67]∨Ch[66]∨Ch[65]∨Ch[64]
CompOut[7]	Ch[63]∨Ch[62]∨Ch[61]∨Ch[60]	Ch[59]∨Ch[58]∨Ch[57]∨Ch[56]
CompOut[6]	Ch[55]∨Ch[54]∨Ch[53]∨Ch[52]	Ch[51]∨Ch[50]∨Ch[49]∨Ch[48]
CompOut[5]	Ch[47]∨Ch[46]∨Ch[45]∨Ch[44]	Ch[43]∨Ch[42]∨Ch[41]∨Ch[40]
CompOut[4]	Ch[39]∨Ch[38]∨Ch[37]∨Ch[36]	Ch[35]∨Ch[34]∨Ch[33]∨Ch[32]
CompOut[3]	Ch[31]∨Ch[30]∨Ch[29]∨Ch[28]	Ch[27]∨Ch[26]∨Ch[25]∨Ch[24]
CompOut[2]	Ch[23]∨Ch[22]∨Ch[21]∨Ch[20]	Ch[19]∨Ch[18]∨Ch[17]∨Ch[16]
CompOut[1]	Ch[15]∨Ch[14]∨Ch[13]∨Ch[12]	Ch[11]∨Ch[10]∨Ch[9]∨Ch[8]
CompOut[0]	Ch[7]∨Ch[6]∨Ch[5]∨Ch[4]	Ch[3]∨Ch[2]∨Ch[1]∨Ch[0]

Readout Timing The *Beetle* chip has two different possible readout timings called *non-consecutive* and *consecutive* readout. A non-consecutive readout starts after a trigger occurs during a non-readout. If the *Beetle* receives a second trigger before a last readout is completed, the next readout is send as a consecutive readout. Figure C.13 depicts the timing condition where the next readout starts as a consecutive readout (upper scheme) respectively the first condition where the next readout starts as a non-consecutive readout (lower scheme).

Figure C.12 describe the readout timing of *Trigger*, *DataValid* and *AnalogOut* of the analogue readout mode on 4 ports. The upper plot shows a single readout burst (non-consecutive readout), the lower the case of a consecutive readout.

C.3.9 Diagnostic Signals

The *Beetle* chip provides several signals for monitoring or diagnostics purposes which are explained briefly in table C.8.

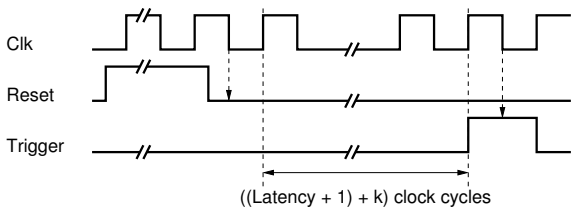


Figure C.10: Timing relation between *Reset* and *Trigger* in order to trigger on a defined pipeline column number.

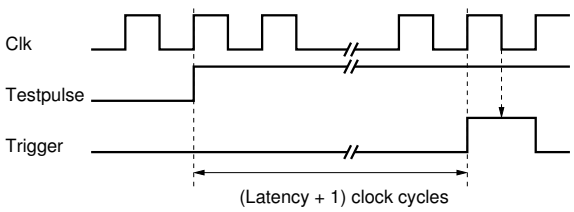


Figure C.11: Timing relation between *Testpulse* and *Trigger*. *Latency* refers to the content of the latency register.

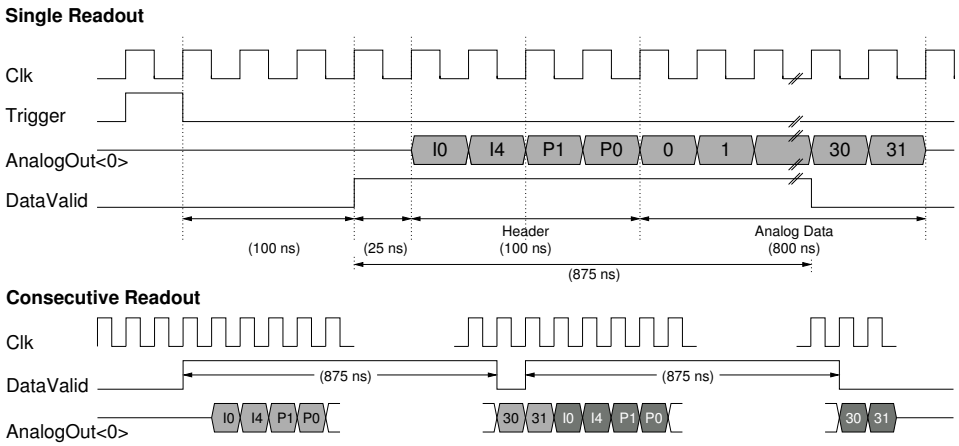


Figure C.12: Readout timing schemes of the analogue readout mode on 4 ports. Only channel 0 is depicted. The upper plot shows a single readout burst, the lower the case of consecutive readout.

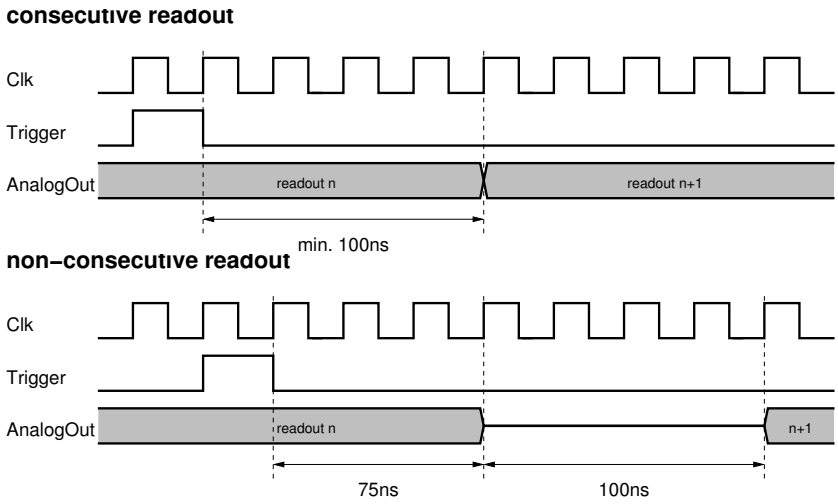


Figure C.13: Non-consecutive and consecutive readout condition. The upper timing plot shows the last possible timing condition of a trigger where the next readout starts as a consecutive readout. The lower plot shows the first condition where the next readout starts as a non-consecutive readout.

Table C.8: Signals for monitoring or diagnostics purposes. First column shows the signal name. The pad no. for chip version *1.3* and *1.4* are quoted in the second column, resp. for *1.5* in the third column. The last column describes briefly the function of the signal.

Signal name	Pad no. 1.3 / 1.4	Pad. no. 1.5	Description
Digital signals (all signals are active-high):			
`FifoFull`	166	166	indicates full derandomising trigger buffer; with 15 occupied FIFO entries, the next trigger activates `FifoFull`
`TrigMon`	171	171	indicates if pipeline trigger pointer passes column no. 0
`WriteMon`	172	172	indicates if pipeline write pointer passes column no. 0
`DataValid`	181, 182	181, 182	indicates presence of valid data on the `AnalogOut` ports; see fig. C.12 for timing specifications
`PPTout`	—	218	output of internal test structure, that shifts with different temperature and/or different process parameter settings
Analogue signals:			
`ProbeIDAC`	139	—	internal current of front-end current DAC Ibuf
`ProbeVrefBE`	216	215	reference voltage of the internal back-end current source
`ProbeIoutBE`	217	216	control current to measure the internal back-end current source
`PipeampTestOut`	218	217	test channel output after pipeline-amplifier
`TestOutput`	242	243	front-end output of test channel (cf. C.3.6)
`Bufbias`	243	244	internal bias node of front-end (cf. C.3.6)
`Shabias1`	244	245	internal bias node of front-end (cf. C.3.6)
`Shabias`	245	246	internal bias node of front-end (cf. C.3.6)
`Prebias1`	246	247	internal bias node of front-end (cf. C.3.6)
`Prebias`	247	248	internal bias node of front-end (cf. C.3.6)

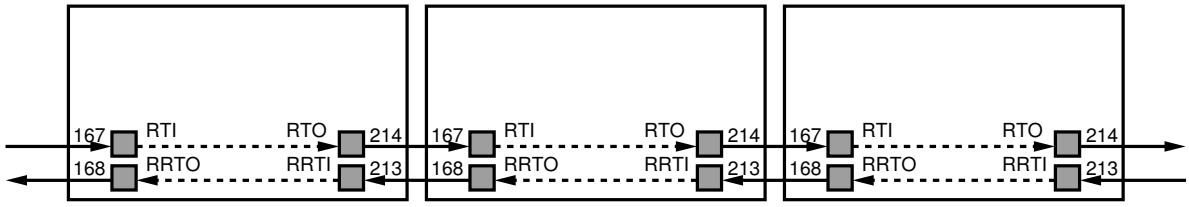


Figure C.14: Daisy chain composition. The figures indicate the pad reference numbers (RTI = RoTokenIn, RRTO = RoReTokenOut, RTO = RoTokenOut, RRTI = RoReTokenIn).

`WriteMon` and `TrigMon` allow to check the physical latency of the chip. They are pulses with a width of one sampling clock cycle and a period of 187 cycles in case of an empty pipeline. Their relative distance is (*Latency + 1*) clock cycles. `WriteMon` and

`PPTout` is the output of an internal test structure on *Beetle1.5* that is switched on/off via the pad `PPTenable` (pad no. 219). If `PPTenable` is not connected, the default setting is off. The output oscillates with a certain frequency that depends on the temperature and the process parameters of the chip. To activate `PPTout` the power pads `VddCPT` (pad no. 221) and `GndCPT` (pad no. 220) have also to be bonded.

C.3.10 Daisy Chain

The daisy chain allows several chips to share one, two or four output lines. It consists of two signal paths, a *token* and a *return token* path. They are built up by connecting the `RoTokenOut` (`RoReTokenIn`) pad of one chip with the `RoTokenIn` (`RoReTokenOut`) of the neighbouring chip (see fig. C.14). The chip position in the chain has to be configured in the *ROCtrl* register (bits 3 and 4). A chip can be the first (`DaisyFirst` = 1), an intermediate or the last (`DaisyLast` = 1) in the daisy chain.

In case of single chip operation, `DaisyFirst` and `DaisyLast` have to be set to 1. As well the bonding of the token pads can be skipped in this mode.

C.4 Slow Control

C.4.1 I²C-Interface

The chip's slow control interface is a standard mode I²C-slave device featuring a transfer rate of 100 kbit/s. The chip address, necessary to access a single device via the I²C-bus, is 7 bits wide and assigned via the address pads `I2CAddr[6:0]` (cf. section C.7.3). The *Beetle* chip responds to addresses in the range $8 - 119$. The addresses `0000XXX` and `1111XXX` are reserved in the I²C-standard for other purposes [6].

The internal registers are being accessed via a *pointer register*. It contains the address of the register to be written or read first. The pointer is internally incremented by 1 after each transferred data frame. In this way registers with adjacent addresses can be accessed consecutively. The pointer register itself remains unchanged, i.e. a new transfer will start at the original pointer position. Figure C.15 explains the transfer sequences in write and read mode. Data is always transferred with the most significant bit (MSB) first. In write mode the chip address is transmitted after initialising the transfer, followed by the pointer byte and the data. After the transmission of one data frame, the pointer addresses the subsequent register because of its auto-incrementing function. The registers with addresses $20 - 23$ are excepted. Registers $20-22$ are implemented as 128-bit shift-registers (cf. C.4.2), register 23 is the output of the SEU counter. A write access to this register resets it to 0. Hence, the auto-incrementing of the address pointer is only performed for addresses ≤ 19. To access the addresses $20 - 23$ the corresponding register has to be addressed directly.

The transfer of the pointer byte is obligatory in write mode. In read mode there are two versions:

- Preset pointer
  After initialising the transfer and sending the chip address data is immediately read out. The pointer has been set in a previous transfer.
- Pointer set followed by immediate read-out
  After initialising the transfer and sending the chip address the pointer byte is transferred. The I²C-bus is re-initialised, the chip address is sent and data is read out.

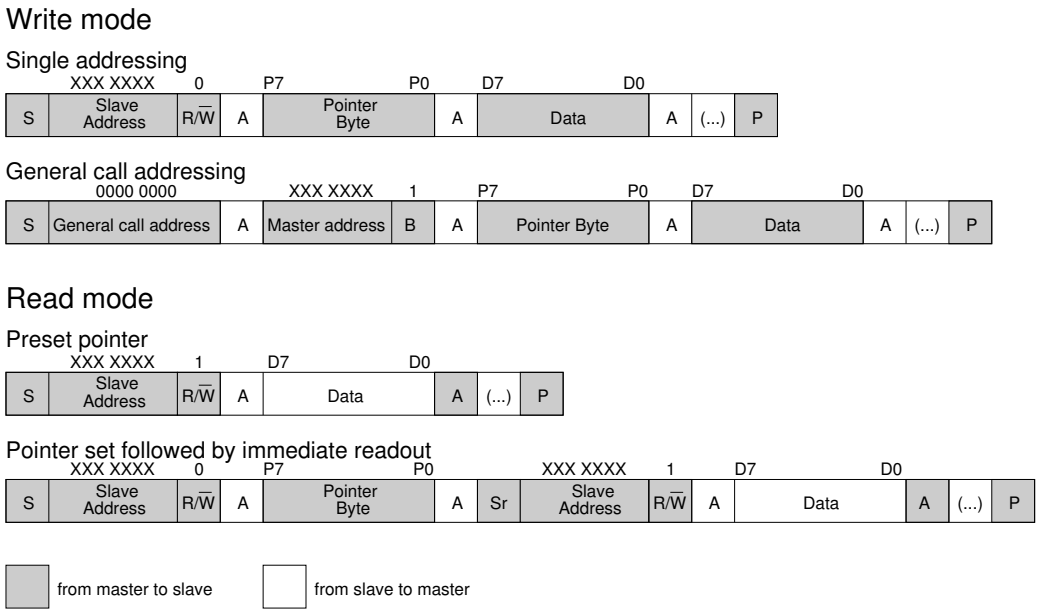


Figure C.15: I²C-bus write and read sequences for accessing registers on the *Beetle*.

Commercially available I^2C-devices usually operate at 3.3 V or 5 V. With version 1.3 or higher, such external devices can be directly connected to the *Beetle* I^2C-interface.

C.4.2 Bias and Configuration Registers

Beetle contains 24 8-bit registers with the addresses $0-23$. Table C.14 lists all registers with physical range, resolution and nominal setting. Registers $0-15$ are bias registers for the analogue stages.

Pipeamp reset potential: *Vd* Register 11 determines the potential to which the pipeamp is reset. This voltage should correspond to the DC output level of the front-end and is therefore depending on *Isha* and *Ibuf* (cf. C.3.1). Table C.9 gives typical values of *Vd* for *Isha* = 80 µA and various *Ibuf* settings.

Table C.9: Corresponding bias settings of *Ibuf* and *Vd* for *Isha* = 80 µA.

Ibuf		*Vd*	
Value	Reg. content	Value	Reg. content
39 µA	0x05	1.314 mV	0x86
47 µA	0x06	1.304 mV	0x85
55 µA	0x07	1.294 mV	0x84
63 µA	0x08	1.284 mV	0x83
71 µA	0x09	1.284 mV	0x83
78 µA	0x0A	1.275 mV	0x82
86 µA	0x0B	1.275 mV	0x82
94 µA	0x0C	1.275 mV	0x82
102 µA	0x0D	1.265 mV	0x81
110 µA	0x0E	1.265 mV	0x81
118 µA	0x0F	1.265 mV	0x81
125 µA	0x10	1.255 mV	0x80
251 µA	0x20	1.216 mV	0x7C

Pipeamp reference potential: *Vdcl* Register 12 adjusts the potential of the non-inverting input of the pipeamp.

Pipeamp bias currents: *Ipipe* and *Ivoltbuf* Register 10 (*Ipipe*) adjusts the bias of the pipeamp, whereas register 13 (*Ivoltbuf*) controls the bias of the *Vdcl*-buffer. Both bias nodes depend strongly on each other. Table C.10 gives typical values of *Ivoltbuf* for various *Ipipe* settings.

Latency Register 16 defines the latency which has to be ≥ 10 and ≤ 160 for reliable chip operation.
$\rightsquigarrow$ A change of the latency register is only made effective by applying a reset.

Rclk divider: *RclkDiv* Register 18 defines the ratio between the readout clock `Rclk` and the sampling clock `Sclk`. The ratio $\nu_{\texttt{Rclk}}/\nu_{\texttt{Sclk}}$ is defined as

$$\frac{\nu_{\texttt{Rclk}}}{\nu_{\texttt{Sclk}}} = \begin{cases} 1 & \text{for } \mathit{RclkDiv} = 0 \\ \frac{1}{2 \cdot \mathit{RclkDiv}} & \text{for } \mathit{RclkDiv} > 0 \end{cases}$$

Table C.10: Corresponding bias settings of *Ivoltbuf* and *Ipipe*

Ipipe		*Ivoltbuf*	
Value	Reg. content	Value	Reg. content
78 µA	0x0A	149 µA	0x13
86 µA	0x0B	149 µA	0x13
94 µA	0x0C	149 µA	0x13
102 µA	0x0D	157 µA	0x14
110 µA	0x0E	157 µA	0x14
118 µA	0x0F	157 µA	0x14
125 µA	0x10	165 µA	0x15
133 µA	0x11	173 µA	0x16
141 µA	0x12	180 µA	0x17
149 µA	0x13	180 µA	0x17
157 µA	0x14	188 µA	0x18
165 µA	0x15	196 µA	0x19
173 µA	0x16	196 µA	0x19
180 µA	0x17	204 µA	0x1A
188 µA	0x18	212 µA	0x1B
196 µA	0x19	212 µA	0x1B
204 µA	0x1A	220 µA	0x1C

and allows `Rclk` frequencies from 40 MHz down to $\approx$ 78 kHz. *RclkDiv* = 0 means, that `Sclk` and `Rclk` have the same frequency.

$\rightsquigarrow$ A change of the *RclkDiv* register requires a following reset for proper chip operation.

Mode of operation: *ROCtrl*, *CompCtrl* The registers 17 and 19 select the chip's mode of operation (readout mode, daisy chain configuration) and define the comparator configuration. Tables C.11 and C.12 show the detailed bit assignment of the registers *ROControl* and *CompControl*. Note, that the three *ModeSelect* bits (*BinRO2*, *AnaRO1* and *AnaRO4*) are exclusive, i.e. only one bit is allowed to be set.

$\rightsquigarrow$ A change of the *ROCtrl* register bit $4-0$ requires a following reset for proper chip operation.

Shift registers Registers $20-22$ (*CompChTh*, *CompMask*, *TpSelect*) are operated as shift-registers: *CompMask* and *TpSelect* form a 128-bit register each, segmented in 16 8-bit registers, *CompChTh* establishes a 1024 ($= 128 \times 8$) bit register, whereas only 5 of the 8 bits per frame are assigned (cf. section C.3.7). A consecutive write access to the corresponding register address shifts the data in 8-bit frames starting from the largest channel number (see fig. C.16).

An unusual feature is the programming of the internal test pulse mask bit of the test channel. With a 17th consecutive write access to the *TpSelect* register, the value of *TpSelect* channel 7 is shifted into *TpSelect* of the test channel.

A read access to one of the shift registers returns the bits corresponding to channels $7-0$ in case of *CompMask* and *TpSelect* and channel 0 in case of *CompChTh*. This allows a verification of the shifted data. In addition the unused bits (7 to 5) of *CompChTh* are used for reading back the *Beetle* chip version number (*RevId*). An overview of the register as well as the possible values for *RevId* are given in table C.13.

Table C.11: Bit assignment of the configuration register *ROCtrl*.

Bit	Function	Description	Nominal
0	BinRO2	binary readout on 2 ports	0
1	AnaRO1	analogue readout on 1 port	0
2	AnaRO4	analogue readout on 4 ports	1
3	DaisyFirst	first chip in daisy chain	1
4	DaisyLast	last chip in daisy chain	1
5	BinaryHeader	readout header levels of current driver	0
6	*not used*	—	0
7	ProbeEnable	enables probe pads `ProbeVrefBE` (pad no. 216)	0

All switches are active-high. 1 enables the switch, 0 disables it.
Nominal settings are defined for LHCb readout mode

Table C.12: Bit assignment of the configuration register *CompCtrl*.

Bit	Function	Description
0	DisableCompLVDS	0: enable comparator LVDS output ports 1: disable comparator LVDS output ports
1	CompPolarity	0: inverting 1: non-inverting
2	PipelineMode	0: analogue readout 1: binary readout
3	CompDisable	0: enable comparator 1: disable comparator
4	CompMode	0: track mode 1: pulse mode
5-7	*not used*	—

SEU counter Register 23 is the output of the SEU counter (cf. C.4.3). A write access to this register resets the content to 0. Note, that the two LSBs of the register *SEUcounts* are transmitted in the header (`S[1:0]`) of the analogue output stream (cf. C.3.5).

C.4.3 Single Event Upset Robustness

Beetle continuously uses triple-redundant logic in order to assure the robustness against Single Event Upset (SEU), i.e. the change of the state of a memory device induced by ionisation. A logic bit is represented by the majority of the outputs of three flip-flops. The flip-flops on *Beetle* can be categorised into two groups:

Clocked flip-flops They are used in the control logic which operates with the sampling clock frequency of 40 MHz in case of the *FastControl* and the I^2C-clock of 100 kHz in case of the *Slow Control*.

Static flip-flops They form the bias and configuration registers. These flip-flops use triple-redundant majority voting in combination with a self-triggered correction mechanism. The correction mech-

Table C.13: Bit assignment of a read access to the comparator threshold register *CompChTh*.

Bit	Function	Description
4-0	CompChTh	Comparator channel threshold number
7-5	RevId	*Beetle* chip version number 111: *Beetle1.3* 100: *Beetle1.4* 101: *Beetle1.5* (cf. section C.6)

anism is controlled by the pad `EnableEDC` and in default mode (enable) a single bit errors will be automatically corrected.

An 8-bit counter is integrated in *Beetle* to indicate the number of Single Event Upsets in the bias and configuration registers. All registers, including the shift-registers *CompChTh*, *CompMask* and *TpSelect*, can increment the SEU counter. The bits used in the logic control circuits (clocked flip-flops) are *not* taken into account. The counter output is readable via the I^2C-bus (cf. C.4.2). The two least significant bits are additionally transferred in the header of the analogue output stream (fig. C.8, S0 and S1). This allows a fast monitoring of SEUs during readout. An I^2C-write access to the counter register resets it.

Table C.14: Bias and configuration registers of *Beetle*.

Reg. no.	Reg. Name	Range	Res. of LSB	Nominal Setting		Description
				Value	Reg. content	
0	*Itp*	0 - 2 mA	7.8 µA	0 µA	`0x00`	test pulse bias current
1	*Ipre*	0 - 2 mA	7.8 µA	600 µA	`0x4C`	preamplifier bias current
2	*Isha*	0 - 2 mA	7.8 µA	80 µA	`0x0A`	shaper bias current
3	*Ibuf*	0 - 2 mA	7.8 µA	80 µA	`0x0A`	front-end buffer bias current
4	*Vfp*	0 - 2.5 V	9.8 mV	0 mV	`0x00`	preamplifier feedback voltage
5	*Vfs*	0 - 2.5 V	9.8 mV	0 mV	`0x00`	shaper feedback voltage
6	*Icomp*	0 - 2 mA	7.8 µA	40 µA	`0x05`	comparator bias current
7	*Ithdelta*	0 - 2 mA	7.8 µA	—	—	current defining incremental comparator threshold
8	*Ithmain*	0 - 2 mA	7.8 µA	—	—	current defining common comparator threshold
9	*Vrc*	0 - 1.25 V	4.9 mV	0 mV	`0x00`	comparator RC time constant
10	*Ipipe*	0 - 2 mA	7.8 µA	100 µA	`0x0D`	pipeamp bias current
11	*Vd*	0 - 2.5 V	9.8 mV	1 275 mV	`0x82`	pipeamp reset potential
12	*Vdcl*	0 - 2.5 V	9.8 mV	1 030 mV	`0x69`	pipeamp reference voltage
13	*Ivoltbuf*	0 - 2 mA	7.8 µA	160 µA	`0x14`	pipeamp buffer bias current
14	*Isf*	0 - 2 mA	7.8 µA	200 µA	`0x1A`	multiplexer buffer bias current
15	*Icurrbuf*	0 - 2 mA	7.8 µA	800 µA	`0x66`	output buffer bias current
16	*Latency*	10 - 160	—	160	`0xA0`	trigger latency
17	*ROCtrl*	—	—	cf. table C.11		readout control
18	*RclkDiv*	0 - 255	—	0	`0x00`	ratio between `Rclk` and `Sclk`
19	*CompCtrl*	—	—	cf. table C.12		comparator control
20	*CompChTh*	0 - 31	—	—	—	comparator channel threshold shift register implementation and *Beetle* revision Id. (cf. table C.13)
21	*CompMask*	—	—	0	`0x00`	comparator mask shift register implementation
22	*TpSelect*	—	—	0	`0x00`	test pulse selection shift register implementation
23	*SEUcounts*	0 - 255	—	—	—	sum of Single Event Upsets

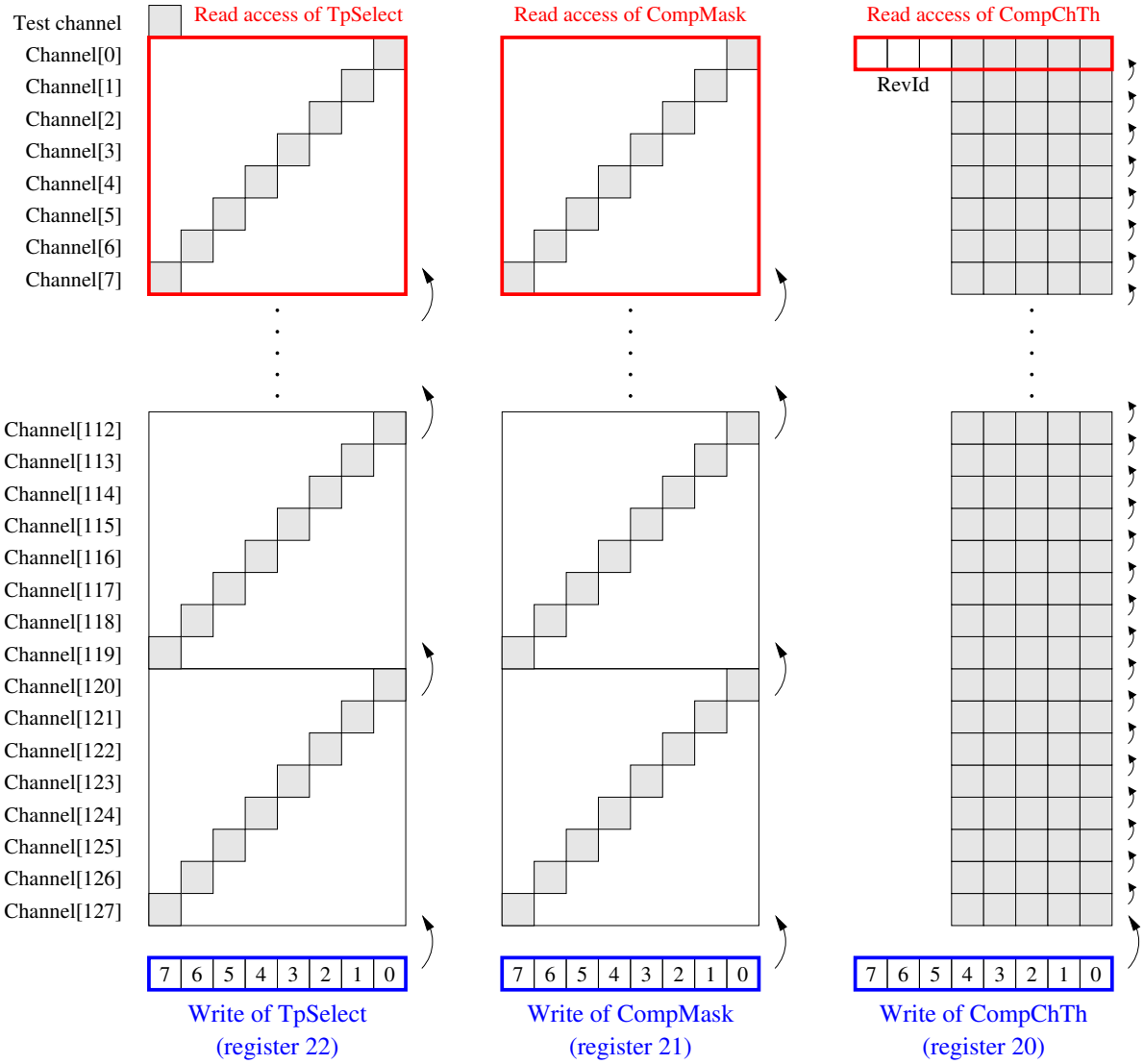


Figure C.16: Mapping of shift register *TpSelect*, *CompMask* and *CompChTh*. Write access via I^2C starting from the largest channel number, whereas a read access returns the data content of the lowest channel.

C.5 How to get the *Beetle* Chip working

This section describes important steps to get the *Beetle* chip working. Some may be trivial, but ignoring them can cause lengthy trouble in debugging the setup.

Power and Blocking

- Power the chip:
  - for analogue operation (like VELO, ST):
    connect to Vdd: pad no.: 3, 4, 135, 136, 169, 205 – 207. In case of *Beetle1.3/1.4* also 141, 240 resp. 140, 241 for *Beetle1.5*
    connect to Gnd: pad no.: 1, 2, 5, 137, 138, 170, 202 – 204. In case of *1.3/1.4* also 140, 241
  - for binary/comparator operation (like PUS, RICH) connect *additionally* to the above listed pads:
    to Vdd: pad no.: 142, 164, 221, 239. In case of *Beetle1.5* also 141, 240
    to Gnd: pad no.: 143, 165, 220, 238. In case of *1.5* also 139, 242

  In case of non-operating in binary/comparator mode, it is recommended to connect all power pads of this mode to Gnd.
- Block the following pads with $\mathcal{O}(100\,\mathrm{nF})$ to ground:
  - `Icurrbuf` (pad no. 208)
  - `Isf` (pad no. 209)
  - `Ipipe` (pad no. 210)
  - `Vdclbuf` (pad no. 211)
  - `Vdbuf` (pad no. 212)

Minimum number of pads to be bonded

The following list specifies the minimum number of *input ports* to be bonded for proper chip operation in addition to power and blocking pads:

- `Trigger` (pad no. 173, 174),
- `Clock` (pad no. 175, 176),
- `Reset` (pad no. 179, 180),
- `SCL, SDA` (pad no. 190, 191).

Besides the analogue output ports `AnalogOut<i>` (pad no. 194 – 201) or the comparator output ports `CompOut<i>` (pad no. 149 – 164, 222 – 237), it is recommended to bond the *digital output pads* listed in C.3.9.

LVDS ports

Apply defined levels to all LVDS input ports, e.g. *Clock*, *Trigger*, *Reset*, *Testpulse*, i.e. do not leave any input pads floating.
Keep in mind that *Reset* and *Trigger* are sampled internally to the negative edge of *Clock*.

Power-up reset

Connect the `PowerupReset` port (pad no. 192) with $\mathcal{O}(100\,\mathrm{nF})$ to ground.

If after powering up the chip the power consumption decreases after programming all bias registers via I^2C-interface then it is obvious that the `PowerupReset` doesn't work. Possible reasons:

- Time constant and therefore the capacitance of `Powerupreset` is to small
- Capacitance `PowerupReset` is still loaded from a previous powering. Perhaps implement a high ohmic path $\mathcal{O}(10\,\mathrm{M\Omega})$ parallel to the capacitance to Gnd.

I^2C-bus

- Define the chip ID via the pads `I2CAddr[6:0]` for individual chip access, or use general call mode. The chip responds to addresses in the range $8 - 119$.
- Assure, that different chips sharing one I^2C-bus line have unique addresses.
- Assure, that the `Reset` port has a defined logic level and does not change while programming the chip via I^2C-bus.

FastControl

- Define the chip as *DaisyFirst* as well as *DaisyLast* (*ROCtrl* register is `XXX11XXX`).
- A change of the content of the *Latency* register (register ID 16) is taken over by the logic circuit only after applying an external reset via the `Reset` port. To check the *physical* latency, determine the time distance of the `WriteMon` (pad no. 171) and `TrigMon` (pad no. 170) signals, which is *Latency + 1*.

  $\rightsquigarrow$ *Latency* has to be in the range $10 - 160$ for proper chip operation.

Shift registers

For a correct programming of all single bits, grouped together to a shift registers, the following number of I^2C-write cycles are necessary:

- *CompChTh* (reg. no. 20): 128
- *CompMask* (reg. no. 21): 16
- *TpSelect* (reg. no. 22): 17 (16 for all 128 channels and 1 for the test channel)

Of course the same number of cycles has to be applied for clearing all bits. (cf. section C.4.2 and especially fig. C.16)

C.6 Known Problems and Limitations

Problem Parity of pipeline column number **(only in *Beetle1.3*)**
In case of operating the *Beetle* in readout mode *Analogue readout on 4 ports* (cf. C.3.5) and *Rclk divider* ratio of 1 (cf. C.4.2, $RclDiv = 0$), the parity bit in the header of a consecutive readout is encoded incorrect.

Limitation Daisy chain
The readout of a second chip in a daisy chain starts to early.

Limitation *Rclk divider* ratio unequal 1
The last channels of each analogue readout sequence on each readout port is only valid for one `Sclk` cycle. For the remaining readout time the value is undefined.

Problem Even/Odd channel crosstalk
There is a signal crosstalk in the order of 2.5% of an odd channel into the predecessor channel, and from an even channel into the successor channel on *Beetle1.3*. On *Beetle1.4* and *1.5* this crosstalk is suppressed to less than 1%.
Since the *dummy channel* of the *Beetle* is the successor channel of the *test channel*, this leads also to a baseline jump if a signal is coupled into the *test channel*.

Problem *Beetle* chip version number
In case of operating a *Beetle1.5* chip without powering the comparator (especially `VddaComp`), the read back of the *Beetle* chip version number (register 20 – *CompChTh*) via I^2C will show a wrong version number.

C.7 Pad Description

A reference number has been assigned to each pad.The numbering starts in the upper left corner of the die (with the analogue input pads left) and runs counter-clockwise (cf. figure C.17 for *Beetle1.3 / 1.4* or figure C.18 for *Beetle1.5)*. The following tables summarise the signals and explain them. The pad coordinates refer to the lower left corner of the pad opening, which is 120 µm×95 µm in case of the front pads and 95 µm×95 µm for all others with exception of the backside power pads. Their enlarged pad windows are listed in section C.7.3. The origin of the coordinate system is defined by the lower left chip corner $(0, 0)$. The dimensions of the chip die are 5 400 µm×6 100 µm[4]. The analogue input pads have a pitch of 40.24 µm, all others 115 µm.

[4] Note, that this are the dimensions of the chip's scribe line, i.e. not including cutting margins. They could add some 100 µm to the chip dimensions.

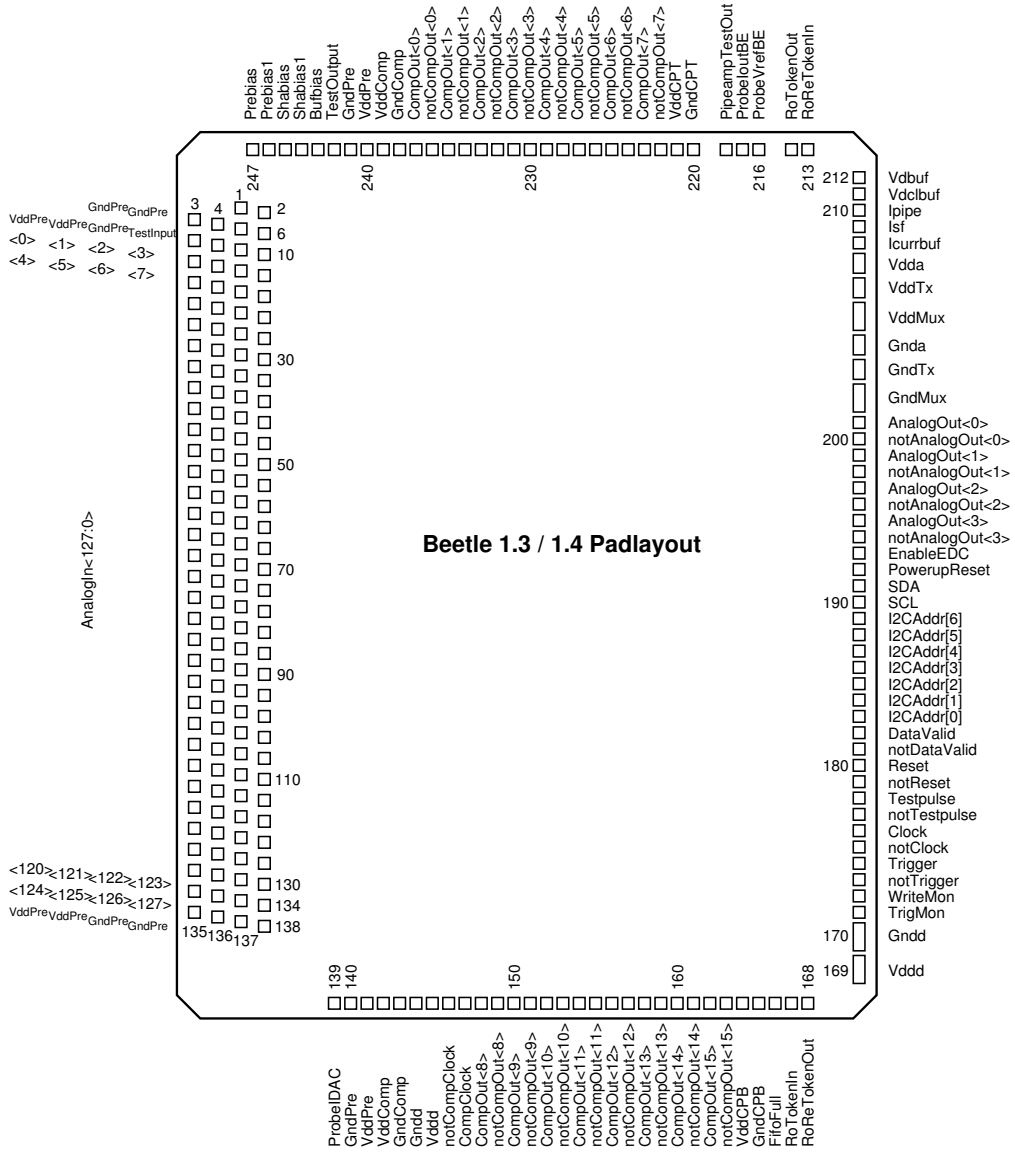


Figure C.17: Pad layout of *Beetle1.3* and *Beetle1.4*. The die size is $(5.4 \times 6.1)\,\mathrm{mm}^2$.

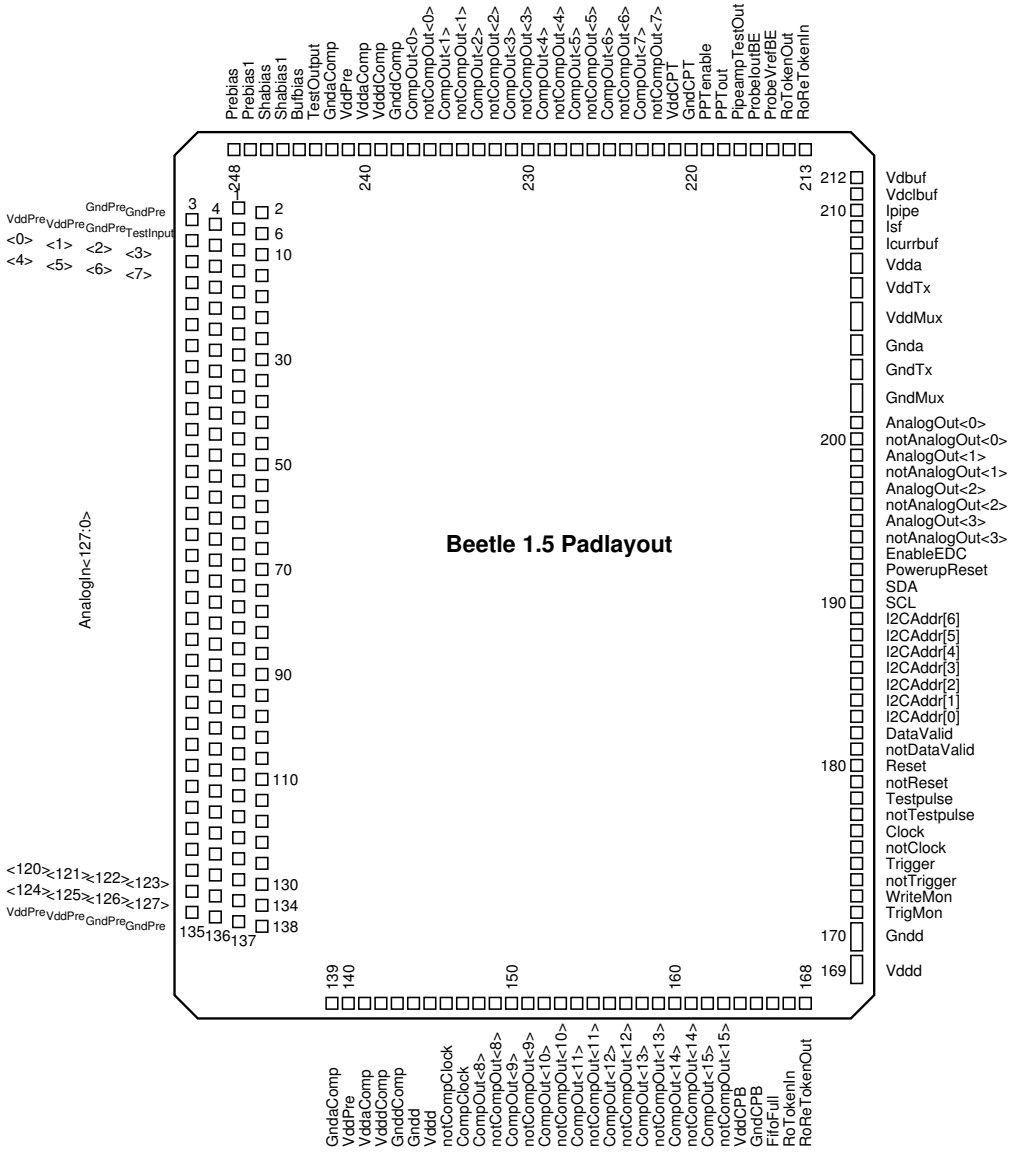


Figure C.18: Pad layout of *Beetle1.5*. The die size is $(5.4 \times 6.1)\,\mathrm{mm}^2$.

C.7.1 Front Pads

Ref. no	Pin name	Coordinates x [µm]	Coordinates y [µm]	Type	Description
1	GndPre	335.00	5876.54	power input	neg. analogue preamplifier supply (detector gnd)
2	GndPre	490.00	5836.30	power input	neg. analogue preamplifier supply (detector gnd)
3	VddPre	25.00	5796.06	power input	pos. analogue preamplifier supply
4	VddPre	180.00	5755.82	power input	pos. analogue preamplifier supply
5	GndPre	335.00	5715.58	power input	neg. analogue preamplifier supply (detector gnd)
6	TestInput	490.00	5675.34	input	input of test channel
7	AnalogIn<0>	25.00	5635.10	input	input of channel 0
8	AnalogIn<1>	180.00	5594.86	input	input of channel 1
9	AnalogIn<2>	335.00	5554.62	input	input of channel 2
10	AnalogIn<3>	490.00	5514.38	input	input of channel 3
11	AnalogIn<4>	25.00	5474.14	input	input of channel 4
12	AnalogIn<5>	180.00	5433.90	input	input of channel 5
13	AnalogIn<6>	335.00	5393.66	input	input of channel 6
14	AnalogIn<7>	490.00	5353.42	input	input of channel 7
15	AnalogIn<8>	25.00	5313.18	input	input of channel 8
16	AnalogIn<9>	180.00	5272.94	input	input of channel 9
17	AnalogIn<10>	335.00	5232.70	input	input of channel 10
18	AnalogIn<11>	490.00	5192.46	input	input of channel 11
19	AnalogIn<12>	25.00	5152.22	input	input of channel 12
20	AnalogIn<13>	180.00	5111.98	input	input of channel 13
21	AnalogIn<14>	335.00	5071.74	input	input of channel 14
22	AnalogIn<15>	490.00	5031.50	input	input of channel 15
23	AnalogIn<16>	25.00	4991.26	input	input of channel 16
24	AnalogIn<17>	180.00	4951.02	input	input of channel 17
25	AnalogIn<18>	335.00	4910.78	input	input of channel 18
26	AnalogIn<19>	490.00	4870.54	input	input of channel 19
27	AnalogIn<20>	25.00	4830.30	input	input of channel 20
28	AnalogIn<21>	180.00	4790.06	input	input of channel 21
29	AnalogIn<22>	335.00	4749.82	input	input of channel 22
30	AnalogIn<23>	490.00	4709.58	input	input of channel 23
31	AnalogIn<24>	25.00	4669.34	input	input of channel 24
32	AnalogIn<25>	180.00	4629.10	input	input of channel 25
33	AnalogIn<26>	335.00	4588.86	input	input of channel 26
34	AnalogIn<27>	490.00	4548.62	input	input of channel 27
35	AnalogIn<28>	25.00	4508.38	input	input of channel 28
36	AnalogIn<29>	180.00	4468.14	input	input of channel 29
37	AnalogIn<30>	335.00	4427.90	input	input of channel 30
38	AnalogIn<31>	490.00	4387.66	input	input of channel 31
39	AnalogIn<32>	25.00	4347.42	input	input of channel 32
40	AnalogIn<33>	180.00	4307.18	input	input of channel 33
41	AnalogIn<34>	335.00	4266.94	input	input of channel 34
42	AnalogIn<35>	490.00	4226.70	input	input of channel 35
43	AnalogIn<36>	25.00	4186.46	input	input of channel 36
44	AnalogIn<37>	180.00	4146.22	input	input of channel 37
45	AnalogIn<38>	335.00	4105.98	input	input of channel 38
46	AnalogIn<39>	490.00	4065.74	input	input of channel 39
47	AnalogIn<40>	25.00	4025.50	input	input of channel 40
48	AnalogIn<41>	180.00	3985.26	input	input of channel 41

Ref. no	Pin name	Coordinates x [µm]	Coordinates y [µm]	Type	Description
49	AnalogIn<42>	335.00	3945.02	input	input of channel 42
50	AnalogIn<43>	490.00	3904.78	input	input of channel 43
51	AnalogIn<44>	25.00	3864.54	input	input of channel 44
52	AnalogIn<45>	180.00	3824.30	input	input of channel 45
53	AnalogIn<46>	335.00	3784.06	input	input of channel 46
54	AnalogIn<47>	490.00	3743.82	input	input of channel 47
55	AnalogIn<48>	25.00	3703.58	input	input of channel 48
56	AnalogIn<49>	180.00	3663.34	input	input of channel 49
57	AnalogIn<50>	335.00	3623.10	input	input of channel 50
58	AnalogIn<51>	490.00	3582.86	input	input of channel 51
59	AnalogIn<52>	25.00	3542.62	input	input of channel 52
60	AnalogIn<53>	180.00	3502.38	input	input of channel 53
61	AnalogIn<54>	335.00	3462.14	input	input of channel 54
62	AnalogIn<55>	490.00	3421.90	input	input of channel 55
63	AnalogIn<56>	25.00	3381.66	input	input of channel 56
64	AnalogIn<57>	180.00	3341.42	input	input of channel 57
65	AnalogIn<58>	335.00	3301.18	input	input of channel 58
66	AnalogIn<59>	490.00	3260.94	input	input of channel 59
67	AnalogIn<60>	25.00	3220.70	input	input of channel 60
68	AnalogIn<61>	180.00	3180.46	input	input of channel 61
69	AnalogIn<62>	335.00	3140.22	input	input of channel 62
70	AnalogIn<63>	490.00	3099.98	input	input of channel 63
71	AnalogIn<64>	25.00	3059.74	input	input of channel 64
72	AnalogIn<65>	180.00	3019.50	input	input of channel 65
73	AnalogIn<66>	335.00	2979.26	input	input of channel 66
74	AnalogIn<67>	490.00	2939.02	input	input of channel 67
75	AnalogIn<68>	25.00	2898.78	input	input of channel 68
76	AnalogIn<69>	180.00	2858.54	input	input of channel 69
77	AnalogIn<70>	335.00	2818.30	input	input of channel 70
78	AnalogIn<71>	490.00	2778.06	input	input of channel 71
79	AnalogIn<72>	25.00	2737.82	input	input of channel 72
80	AnalogIn<73>	180.00	2697.58	input	input of channel 73
81	AnalogIn<74>	335.00	2657.34	input	input of channel 74
82	AnalogIn<75>	490.00	2617.10	input	input of channel 75
83	AnalogIn<76>	25.00	2576.86	input	input of channel 76
84	AnalogIn<77>	180.00	2536.62	input	input of channel 77
85	AnalogIn<78>	335.00	2496.38	input	input of channel 78
86	AnalogIn<79>	490.00	2456.14	input	input of channel 79
87	AnalogIn<80>	25.00	2415.90	input	input of channel 80
88	AnalogIn<81>	180.00	2375.66	input	input of channel 81
89	AnalogIn<82>	335.00	2335.42	input	input of channel 82
90	AnalogIn<83>	490.00	2295.18	input	input of channel 83
91	AnalogIn<84>	25.00	2254.94	input	input of channel 84
92	AnalogIn<85>	180.00	2214.70	input	input of channel 85
93	AnalogIn<86>	335.00	2174.46	input	input of channel 86
94	AnalogIn<87>	490.00	2134.22	input	input of channel 87
95	AnalogIn<88>	25.00	2093.98	input	input of channel 88
96	AnalogIn<89>	180.00	2053.74	input	input of channel 89
97	AnalogIn<90>	335.00	2013.50	input	input of channel 90
98	AnalogIn<91>	490.00	1973.26	input	input of channel 91
99	AnalogIn<92>	25.00	1933.02	input	input of channel 92
100	AnalogIn<93>	180.00	1892.78	input	input of channel 93
101	AnalogIn<94>	335.00	1852.54	input	input of channel 94

Ref. no	Pin name	Coordinates x [µm]	Coordinates y [µm]	Type	Description
102	AnalogIn<95>	490.00	1812.30	input	input of channel 95
103	AnalogIn<96>	25.00	1772.06	input	input of channel 96
104	AnalogIn<97>	180.00	1731.82	input	input of channel 97
105	AnalogIn<98>	335.00	1691.58	input	input of channel 98
106	AnalogIn<99>	490.00	1651.34	input	input of channel 99
107	AnalogIn<100>	25.00	1611.10	input	input of channel 100
108	AnalogIn<101>	180.00	1570.86	input	input of channel 101
109	AnalogIn<102>	335.00	1530.62	input	input of channel 102
110	AnalogIn<103>	490.00	1490.38	input	input of channel 103
111	AnalogIn<104>	25.00	1450.14	input	input of channel 104
112	AnalogIn<105>	180.00	1409.90	input	input of channel 105
113	AnalogIn<106>	335.00	1369.66	input	input of channel 106
114	AnalogIn<107>	490.00	1329.42	input	input of channel 107
115	AnalogIn<108>	25.00	1289.18	input	input of channel 108
116	AnalogIn<109>	180.00	1248.94	input	input of channel 109
117	AnalogIn<110>	335.00	1208.70	input	input of channel 110
118	AnalogIn<111>	490.00	1168.46	input	input of channel 111
119	AnalogIn<112>	25.00	1128.22	input	input of channel 112
120	AnalogIn<113>	180.00	1087.98	input	input of channel 113
121	AnalogIn<114>	335.00	1047.74	input	input of channel 114
122	AnalogIn<115>	490.00	1007.50	input	input of channel 115
123	AnalogIn<116>	25.00	967.26	input	input of channel 116
124	AnalogIn<117>	180.00	927.02	input	input of channel 117
125	AnalogIn<118>	335.00	886.78	input	input of channel 118
126	AnalogIn<119>	490.00	846.54	input	input of channel 119
127	AnalogIn<120>	25.00	806.30	input	input of channel 120
128	AnalogIn<121>	180.00	766.06	input	input of channel 121
129	AnalogIn<122>	335.00	725.82	input	input of channel 122
130	AnalogIn<123>	490.00	685.58	input	input of channel 123
131	AnalogIn<124>	25.00	645.34	input	input of channel 124
132	AnalogIn<125>	180.00	605.10	input	input of channel 125
133	AnalogIn<126>	335.00	564.86	input	input of channel 126
134	AnalogIn<127>	490.00	524.62	input	input of channel 127
135	VddPre	25.00	484.38	power input	pos. analogue preamplifier supply
136	VddPre	180.00	444.14	power input	pos. analogue preamplifier supply
137	GndPre	335.00	403.90	power input	neg. analogue preamplifier supply (detector gnd)
138	GndPre	490.00	363.66	power input	neg. analogue preamplifier supply (detector gnd)

C.7.2 Bottom Pads

Ref. no	Pin name	Coordinates x [µm]	Coordinates y [µm]	Type	Description
139					
1.3/1.4	ProbeIDAC	1824.12	37.50	output	current DAC (*Ibuf*) probe pad
1.5	GndaComp	1824.12	37.50	power input	neg. analogue comparator supply
140					
1.3/1.4	GndPre	1939.12	37.50	power input	neg. analogue preamplifier (detector gnd) and comparator supply
1.5	VddPre	1939.12	37.50	power input	pos. analogue preamplifier supply
141					
1.3/1.4	VddPre	2054.12	37.50	power input	pos. analogue preamplifier and comparator supply
1.5	VddaComp	2054.12	37.50	power input	pos. analogue comparator supply
142	VdddComp	2169.12	37.50	power input	pos. digital comparator supply
143	GnddComp	2284.12	37.50	power input	neg. digital comparator supply
144	Gndd	2399.12	37.50	power input	neg. digital supply
145	Vddd	2514.12	37.50	power input	pos. digital supply
146	notCompClock	2629.12	37.50	LVDS input	comparator clock
147	CompClock	2744.12	37.50	LVDS input	comparator clock
148	CompOut<8>	2859.12	37.50	LVDS output	comparator output channel 8
149	notCompOut<8>	2974.12	37.50	LVDS output	comparator output channel 8
150	CompOut<9>	3089.12	37.50	LVDS output	comparator output channel 9
151	notCompOut<9>	3204.12	37.50	LVDS output	comparator output channel 9
152	CompOut<10>	3319.12	37.50	LVDS output	comparator output channel 10
153	notCompOut<10>	3434.12	37.50	LVDS output	comparator output channel 10
154	CompOut<11>	3549.12	37.50	LVDS output	comparator output channel 11
155	notCompOut<11>	3664.12	37.50	LVDS output	comparator output channel 11
156	CompOut<12>	3779.12	37.50	LVDS output	comparator output channel 12
157	notCompOut<12>	3894.12	37.50	LVDS output	comparator output channel 12
158	CompOut<13>	4009.12	37.50	LVDS output	comparator output channel 13
159	notCompOut<13>	4124.12	37.50	LVDS output	comparator output channel 13
160	CompOut<14>	4239.12	37.50	LVDS output	comparator output channel 14
161	notCompOut<14>	4354.12	37.50	LVDS output	comparator output channel 14
162	CompOut<15>	4469.12	37.50	LVDS output	comparator output channel 15
163	notCompOut<15>	4584.12	37.50	LVDS output	comparator output channel 15
164	VddCPB	4699.12	37.50	power input	pos. comparator LVFS supply
165	GndCPB	4814.12	37.50	power input	neg. comparator LVDS supply
166	FifoFull	4929.12	37.50	CMOS output	indicates a full derandomising buffer
167	RoTokenIn	5044.12	37.50	CMOS input (pull-down)	readout start token in daisy-chain mode
168	RoReTokenOut	5159.12	37.50	CMOS output	return token in daisy-chain mode

C.7.3 Backside Pads

Ref. no	Pin name	Coordinates x [µm]	Coordinates y [µm]	Type	Description
169	Vddd	5274.62	184.72	power input	pos. digital supply (pad window: (95×210) µm^2)
170	Gndd	5274.62	414.72	power input	neg. digital supply (pad window: (95×210) µm^2)
171	TrigMon	5274.62	644.72	CMOS output	indicates if trigger pointer passes column 0
172	WriteMon	5274.62	759.72	CMOS output	indicates if write pointer passes column 0
173	notTrigger	5274.62	874.72	LVDS input	trigger
174	Trigger	5274.62	989.72	LVDS input	trigger
175	notClock	5274.62	1104.72	LVDS input	system clock
176	Clock	5274.62	1219.72	LVDS input	system clock
177	notTestpulse	5274.62	1334.72	LVDS input	test pulse
178	Testpulse	5274.62	1449.72	LVDS input	test pulse
179	notReset	5274.62	1564.72	LVDS input	system reset
180	Reset	5274.62	1679.72	LVDS input	system reset
181	notDataValid	5274.62	1794.72	LVDS output	indicates presence of valid data
182	DataValid	5274.62	1909.72	LVDS output	indicates presence of valid data
183	I2CAddr<0>	5274.62	2024.72	CMOS input (pull-down)	*Beetle* chip id. bit 0
184	I2CAddr<1>	5274.62	2139.72	CMOS input (pull-down)	*Beetle* chip id. bit 1
185	I2CAddr<2>	5274.62	2254.72	CMOS input (pull-down)	*Beetle* chip id. bit 2
186	I2CAddr<3>	5274.62	2369.72	CMOS input (pull-down)	*Beetle* chip id. bit 3
187	I2CAddr<4>	5274.62	2484.72	CMOS input (pull-down)	*Beetle* chip id. bit 4
188	I2CAddr<5>	5274.62	2599.72	CMOS input (pull-down)	*Beetle* chip id. bit 5
189	I2CAddr<6>	5274.62	2714.72	CMOS input (pull-down)	*Beetle* chip id. bit 6
190	SCL	5274.62	2829.72	CMOS input (5V)	I^{2}C-bus clock port
191	SDA	5274.62	2944.72	CMOS inout (5V)	I^{2}C-bus data port
192	PowerupReset	5274.62	3059.72	block output	block pad for powerup Reset
193	EnableEDC	5274.62	3174.72	CMOS input (pull-up)	enable Error Detection and Correction
194	notAnalogOut<3>	5274.62	3289.72	output	analogue output channel 3
195	AnalogOut<3>	5274.62	3404.72	output	analogue output channel 3
196	notAnalogOut<2>	5274.62	3519.72	output	analogue output channel 2
197	AnalogOut<2>	5274.62	3634.72	output	analogue output channel 2
198	notAnalogOut<1>	5274.62	3749.72	output	analogue output channel 1
199	AnalogOut<1>	5274.62	3864.72	output	analogue output channel 1
200	notAnalogOut<0>	5274.62	3979.72	output	analogue output channel 0
201	AnalogOut<0>	5274.62	4094.72	output	analogue output channel 0
202	GnddMux	5274.62	4209.72	power input	neg. digital MUX supply (pad window: (95×210) µm^2)
203	GndaTx	5274.62	4439.72	power input	neg. supply output driver (pad window: (95×152.5) µm^2)

Ref. no	Pin name	Coordinates x [µm]	Coordinates y [µm]	Type	Description
204	`Gnda`	5274.62	4612.22	power input	neg. analogue supply (pad window: (95×152.5) µm^2)
205	`VdddMux`	5274.62	4784.72	power input	pos. digital MUX supply (pad window: (95×210) µm^2)
206	`VddaTx`	5274.62	5014.72	power input	pos. supply output driver (pad window: (95×152.5) µm^2)
207	`Vdda`	5274.62	5187.22	power input	pos. analogue supply (pad window: (95×152.5) µm^2)
208	`Icurrbuf`	5274.62	5359.72	block output	analogue probe pad (to be blocked)
209	`Isf`	5274.62	5474.72	block output	analogue probe pad (to be blocked)
210	`Ipipe`	5274.62	5589.72	block output	analogue probe pad (to be blocked)
211	`Vdclbuf`	5274.62	5704.72	block output	analogue probe pad (to be blocked)
212	`Vdbuf`	5274.62	5819.72	block output	analogue probe pad (to be blocked)

C.7.4 Top Pads

Ref. no	Pin name	Coordinates x [µm]	Coordinates y [µm]	Type	Description
213	RoReTokenIn	5159.12	5967.52	CMOS input (pull-down)	return token in daisy-chain mode
214	RoTokenOut	5044.12	5967.52	CMOS output	readout start token in daisy-chain mode
215					
1.3/1.4	—	—	—	—	—
1.5	ProbeVrefBE	4929.12	5967.52	output	current source BE probe pad
216					
1.3/1.4	ProbeVrefBE	4814.12	5967.52	output	current source BE probe pad
1.5	ProbeIoutBE	4814.12	5967.52	output	current source BE probe pad
217					
1.3/1.4	ProbeIoutBE	4699.12	5967.52	output	current source BE probe pad
1.5	PipeampTestOut	4699.12	5967.52	output	pipeline-amplifier probe pad
218					
1.3/1.4	PipeampTestOut	4584.12	5967.52	output	pipeline-amplifier probe pad
1.5	PPTout	4584.12	5967.52	output	digital PPT test structure probe pad
219					
1.3/1.4	—	—	—	—	—
1.5	PPTenable	4469.12	5967.52	CMOS input (pull-down)	enable pad for PPT test structure
220	GndCPT	4354.12	5967.52	power input	neg. comparator LVDS supply
221	VddCPT	4239.12	5967.52	power input	pos. comparator LVDS supply
222	notCompOut<7>	4124.12	5967.52	LVDS output	comparator output channel 7
223	CompOut<7>	4009.12	5967.52	LVDS output	comparator output channel 7
224	notCompOut<6>	3894.12	5967.52	LVDS output	comparator output channel 6
225	CompOut<6>	3779.12	5967.52	LVDS output	comparator output channel 6
226	notCompOut<5>	3664.12	5967.52	LVDS output	comparator output channel 5
227	CompOut<5>	3549.12	5967.52	LVDS output	comparator output channel 5
228	notCompOut<4>	3434.12	5967.52	LVDS output	comparator output channel 4
229	CompOut<4>	3319.12	5967.52	LVDS output	comparator output channel 4
230	notCompOut<3>	3204.12	5967.52	LVDS output	comparator output channel 3
231	CompOut<3>	3089.12	5967.52	LVDS output	comparator output channel 3
232	notCompOut<2>	2974.12	5967.52	LVDS output	comparator output channel 2
233	CompOut<2>	2859.12	5967.52	LVDS output	comparator output channel 2
234	notCompOut<1>	2744.12	5967.52	LVDS output	comparator output channel 1
235	CompOut<1>	2629.12	5967.52	LVDS output	comparator output channel 1
236	notCompOut<0>	2514.12	5967.52	LVDS output	comparator output channel 0
237	CompOut<0>	2399.12	5967.52	LVDS output	comparator output channel 0
238	GnddComp	2284.12	5967.52	power input	neg. digital comparator supply
239	VdddComp	2169.12	5967.52	power input	pos. digital comparator supply
240					
1.3/1.4	VddPre	2054.12	5967.52	power input	pos. analogue preamplifier and comparator supply
1.5	VddaComp	2054.12	5967.52	power input	pos. analogue comparator
241					
1.3/1.4	GndPre	1939.12	5967.52	power input	neg. analogue preamplifier (detector gnd) and comparator supply
1.5	VddPre	1939.12	5967.52	power input	pos. analogue preamplifier
242					
1.3/1.4	TestOutput	1824.12	5967.52	output	front-end output of test channel
1.5	GndaComp	1824.12	5967.52	power input	neg. analogue comparator supply

Ref. no	Pin name	Coordinates x [µm]	Coordinates y [µm]	Type	Description
243					
1.3/1.4	`Bufbias`	1709.12	5967.52	output	analogue probe pad
1.5	`TestOutput`	1709.12	5967.52	output	front-end output of test channel
244					
1.3/1.4	`Shabias1`	1594.12	5967.52	output	analogue probe pad
1.5	`Bufbias`	1594.12	5967.52	output	analogue probe pad
245					
1.3/1.4	`Shabias`	1479.12	5967.52	output	analogue probe pad
1.5	`Shabias1`	1479.12	5967.52	output	analogue probe pad
246					
1.3/1.4	`Prebias1`	1364.12	5967.52	output	analogue probe pad
1.5	`Shabias`	1364.12	5967.52	output	analogue probe pad
247					
1.3/1.4	`Prebias`	1249.12	5967.52	output	analogue probe pad
1.5	`Prebias1`	1249.12	5967.52	output	analogue probe pad
248					
1.3/1.4	—	—	—	—	—
1.5	`Prebias`	1134.12	5967.52	output	analogue probe pad

C.8 Optical Alignment Markers

For an easier chip alignment on *Beetle1.4* and *Beetle1.5* two optical alignment markers were implemented on the top metal layer. Figure C.19 shows the layout and the sizes of the alignment structure. The overall position of the lower left alignment corner on the *Beetle* chip (referred to the coordinate system defined in section C.7) are:

- 697.92 µm×56.64 µm
- 995.98 µm×5 964.32 µm

On *Beetle1.3* this alignment structure is not available.

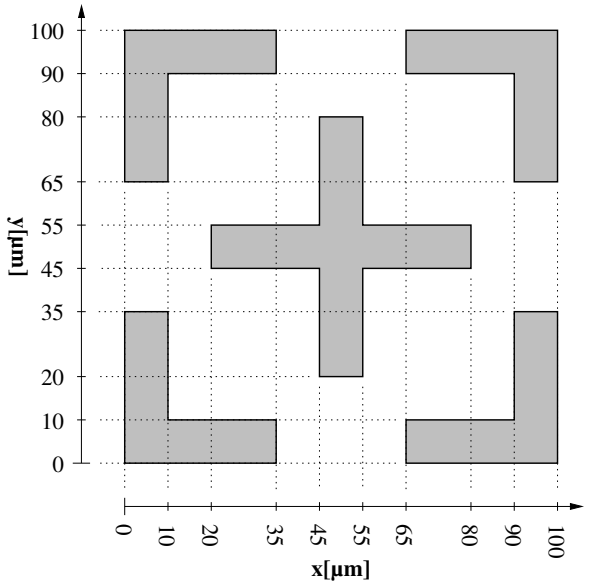


Figure C.19: Optical alignment makers, available on *Beetle1.4* and *Beetle1.5*. The origin of the coordinate system is defined by the lower left alignment corner.

C.9 Heidelberg Test Boards

For a standalone characterisation of the *Beetle* chip, i.e. without a silicon sensor connected to it's inputs, a test setup consisting of two printed circuit boards has been developed in Heidelberg. This section summarises the pin configurations and bonding schemes of the two boards. The *daughter board* can carry two *Beetle* chips and is mounted on a second board, called *mother board*, which integrates the receiver circuits for the analogue output stages (fig. C.3) as well as a LVDS receiver. The set-up allows the charge injection to 12 input channels per chip via a resistive voltage divider (located on the mother board) and a series capacitance. Parallel capacitances can be applied as load. Series and parallel capacitances are located on the daughter board.

Figure C.20 shows the pin configuration of the daughter board, fig. C.21 the layout of the top side and fig. C.22 the layout of the bottom side. Figs. C.23 and C.24 shows the corresponding bonding schemes with and without comparator operation for a *Beetle1.3 / 1.4*, resp. figs. C.25 and C.26 for a *Beetle1.5*. The pin configuration of the mother board is depicted in fig. C.29. A schematic diagram of the mother board is specified in fig. C.30.

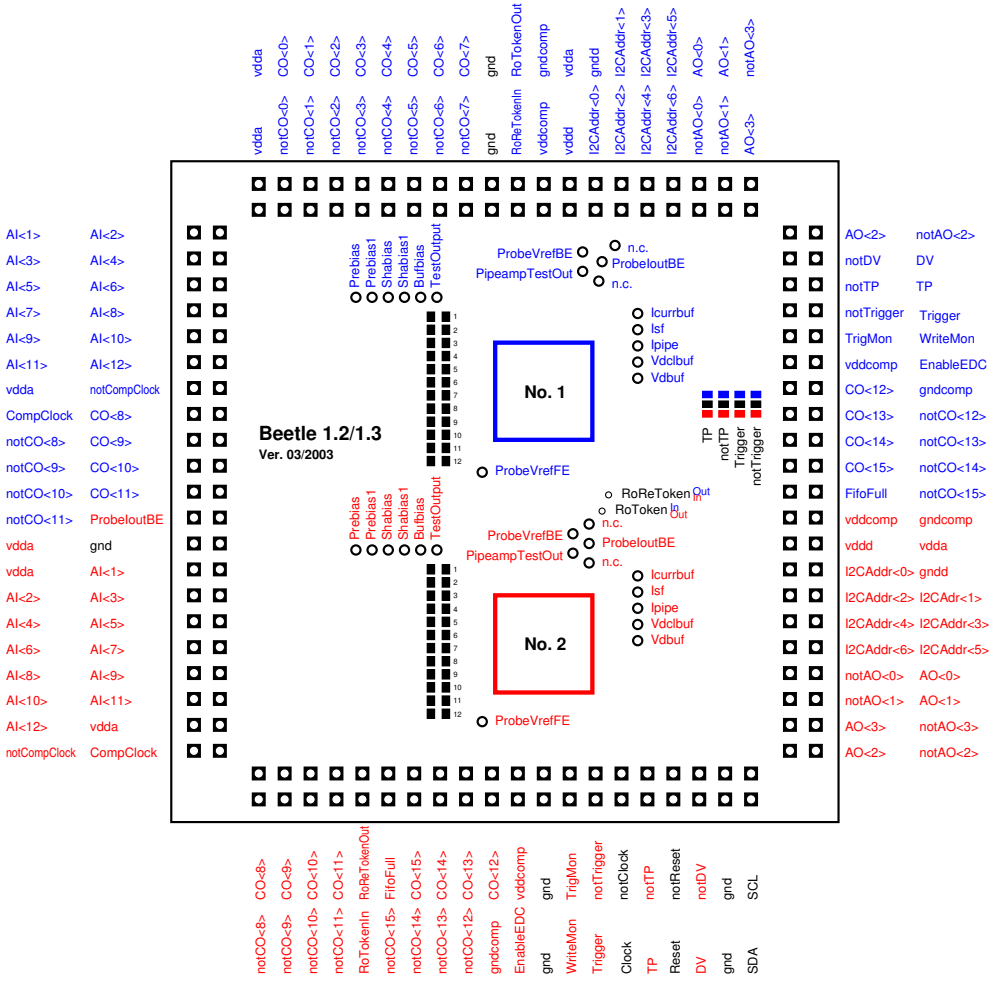


Figure C.20: Pin configuration of the daughter board. The four jumper rows labelled *TP, notTP, Trigger, notTrigger* refer to chip no. 1 and select between the signal pins on the right side (upper position) and on the bottom side (lower position). Using the lower jumper positions, both chips receive *Trigger* and *TP* signals via the bottom side pins.

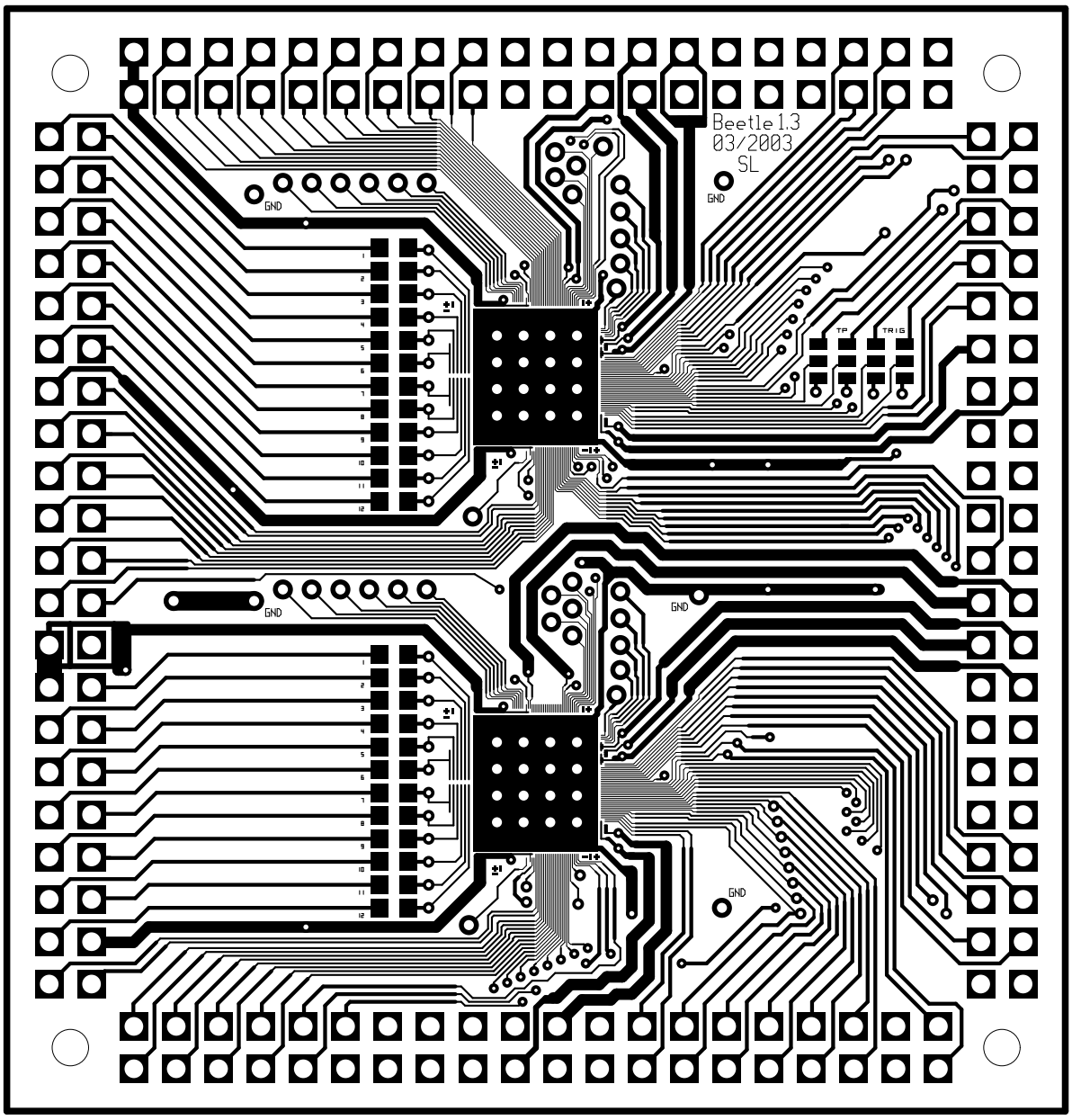


Figure C.21: Top layer of the Heidelberg daughter PCB (version 03/2003).

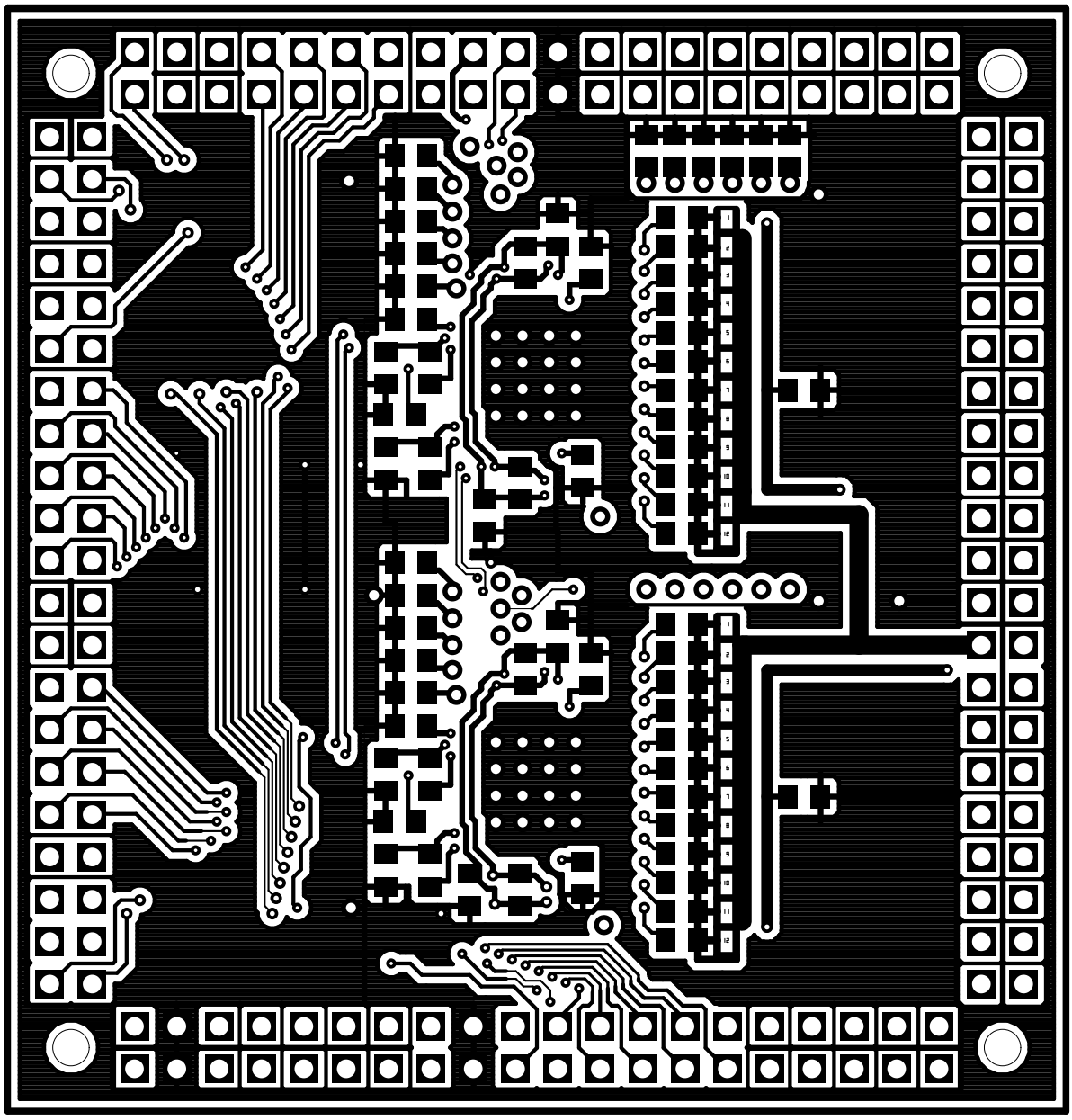


Figure C.22: Bottom layer of the Heidelberg daughter PCB (version 03/2003).

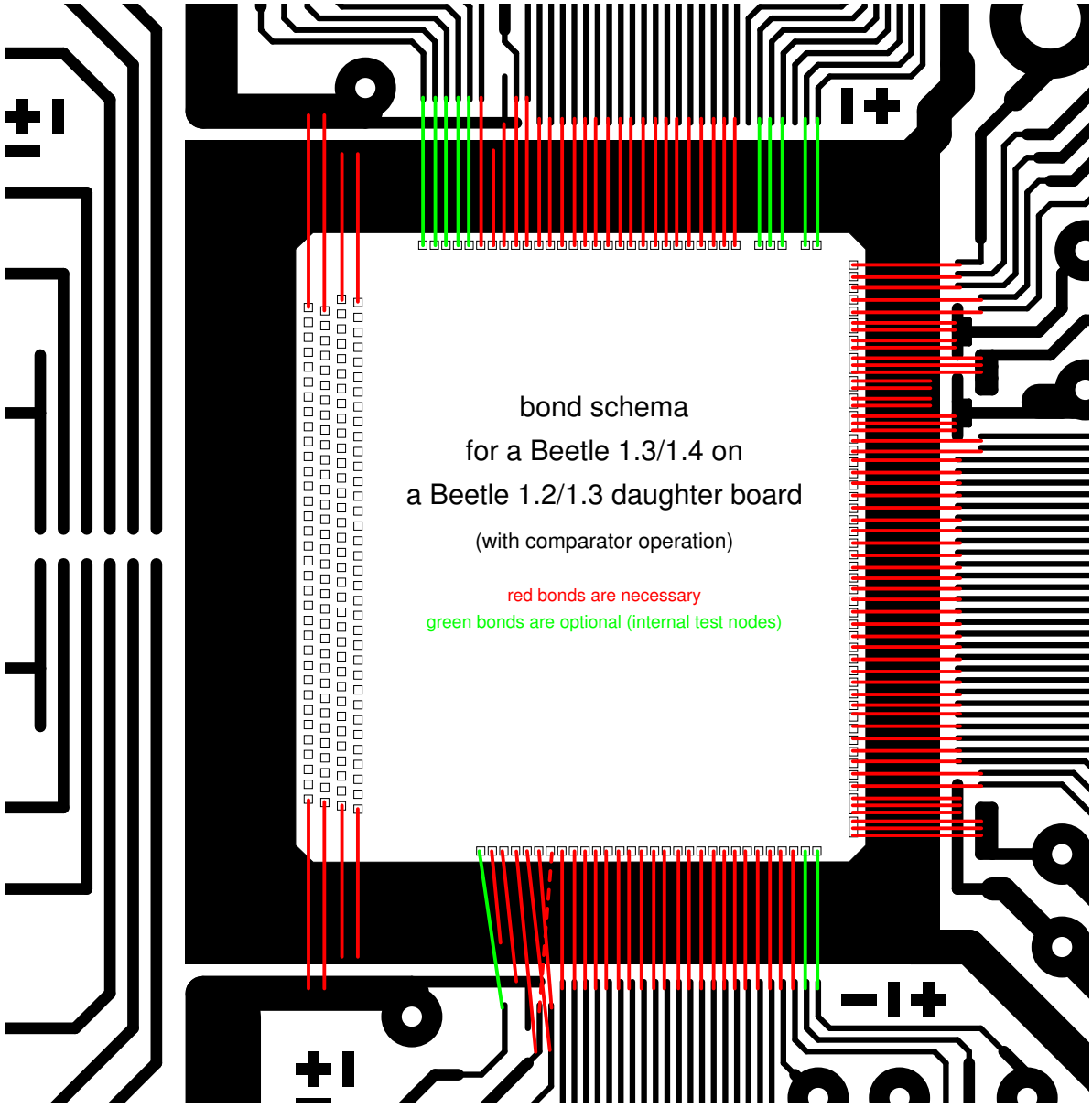


Figure C.23: Bonding diagram for *Beetle1.3* and *Beetle1.4* with comparator operation.

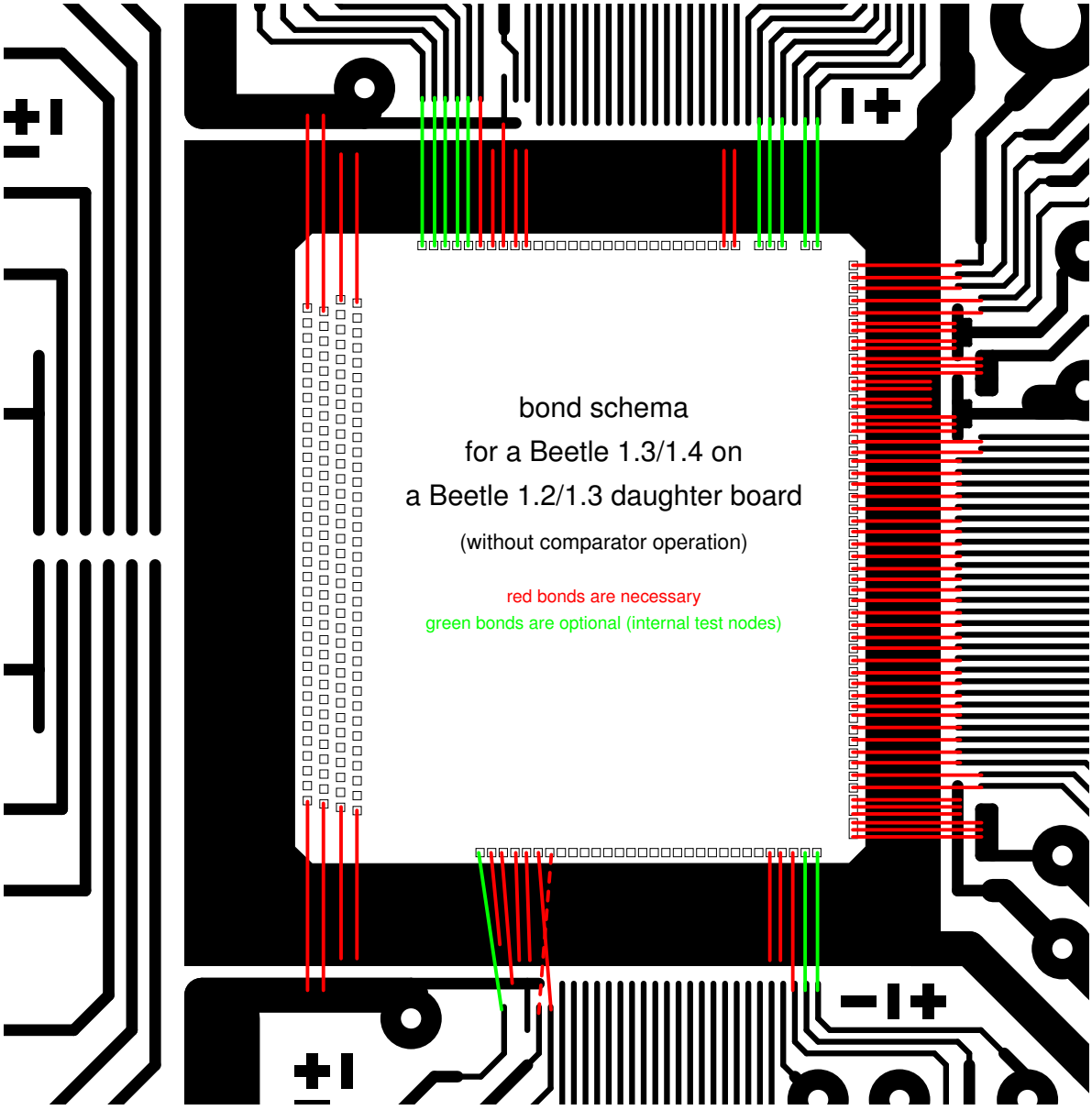


Figure C.24: Bonding diagram for *Beetle1.3* and *Beetle1.4* without comparator operation.

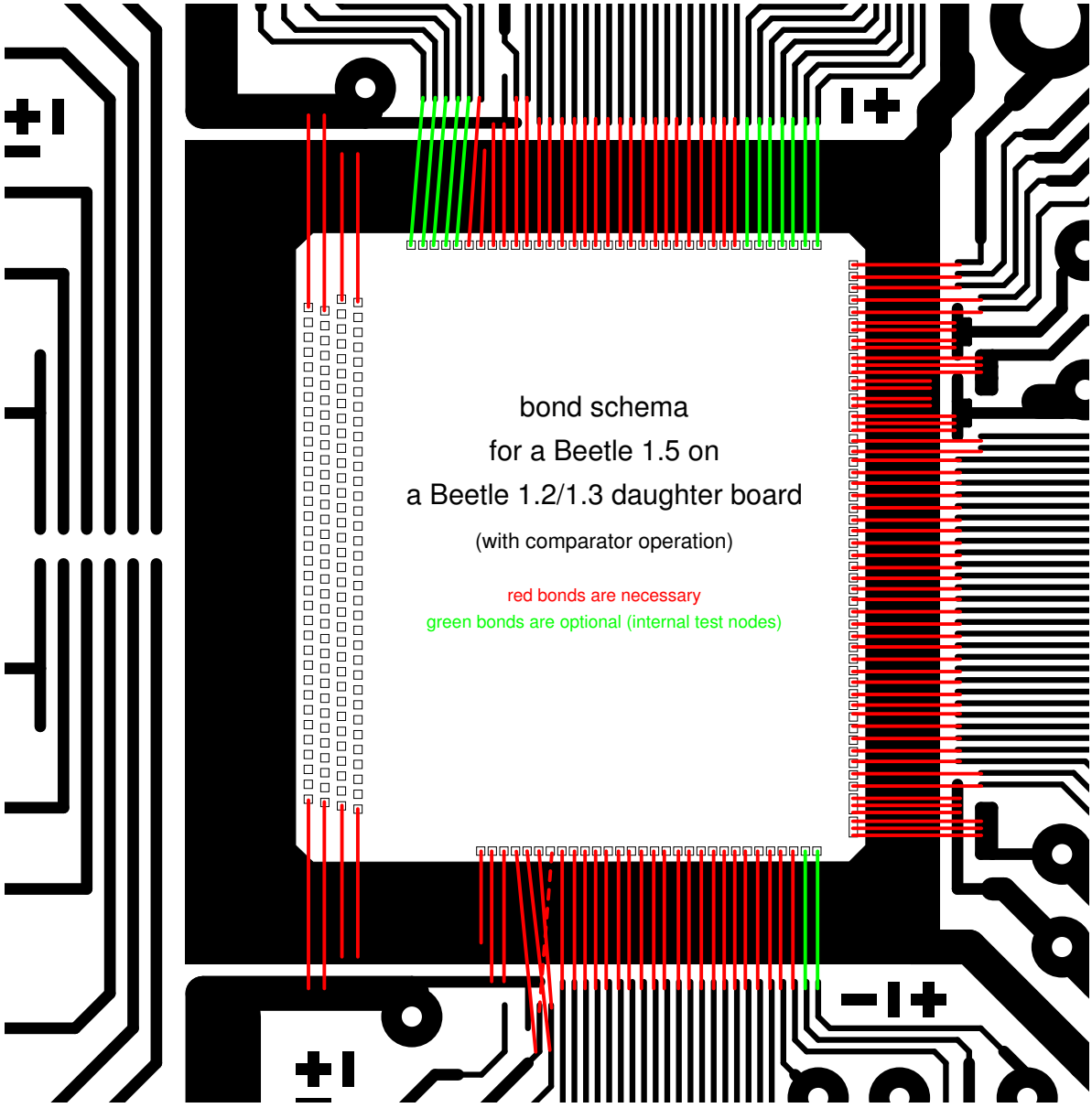


Figure C.25: Bonding diagram for *Beetle1.5* with comparator operation.

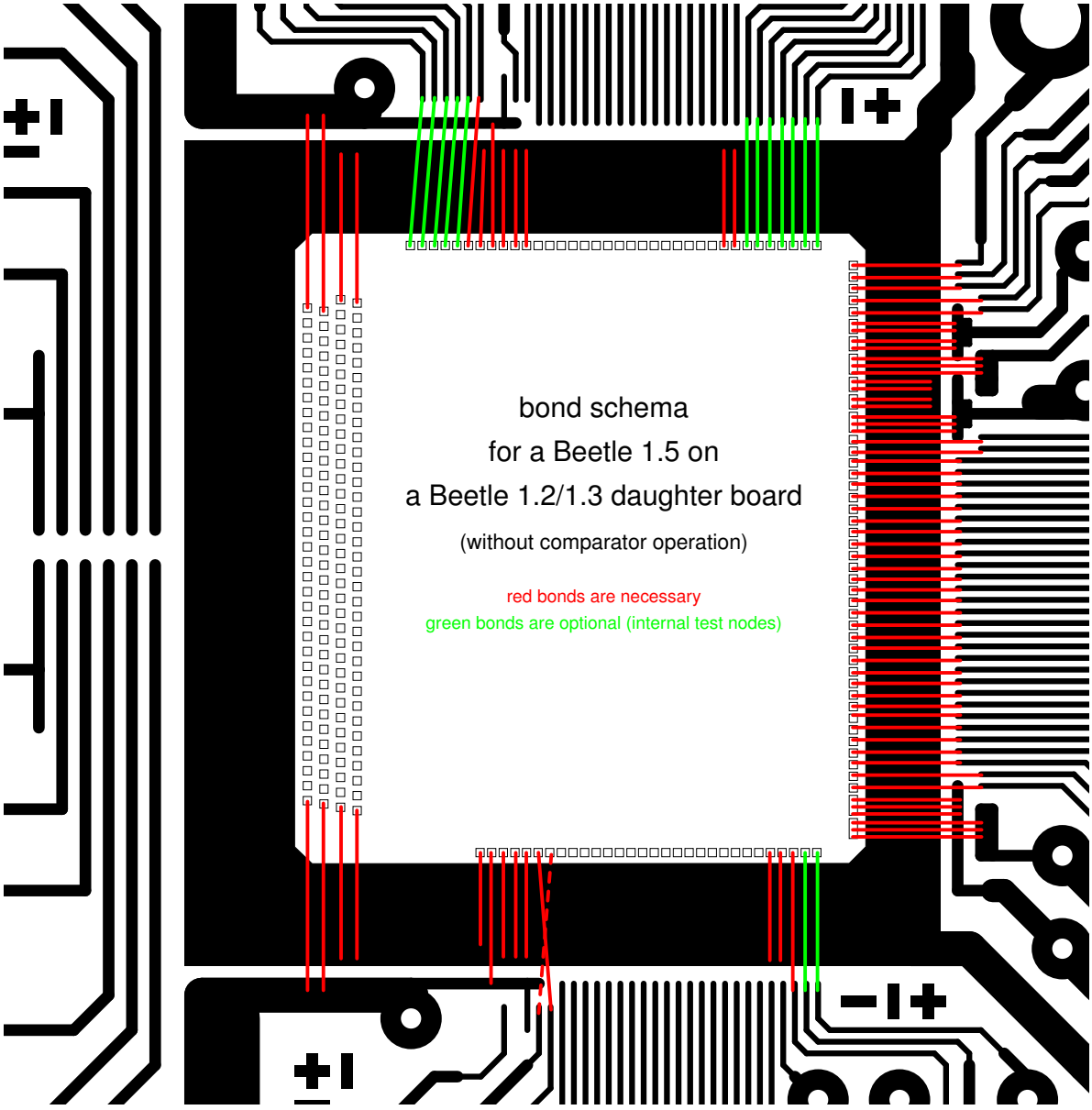


Figure C.26: Bonding diagram for *Beetle1.5* without comparator operation.

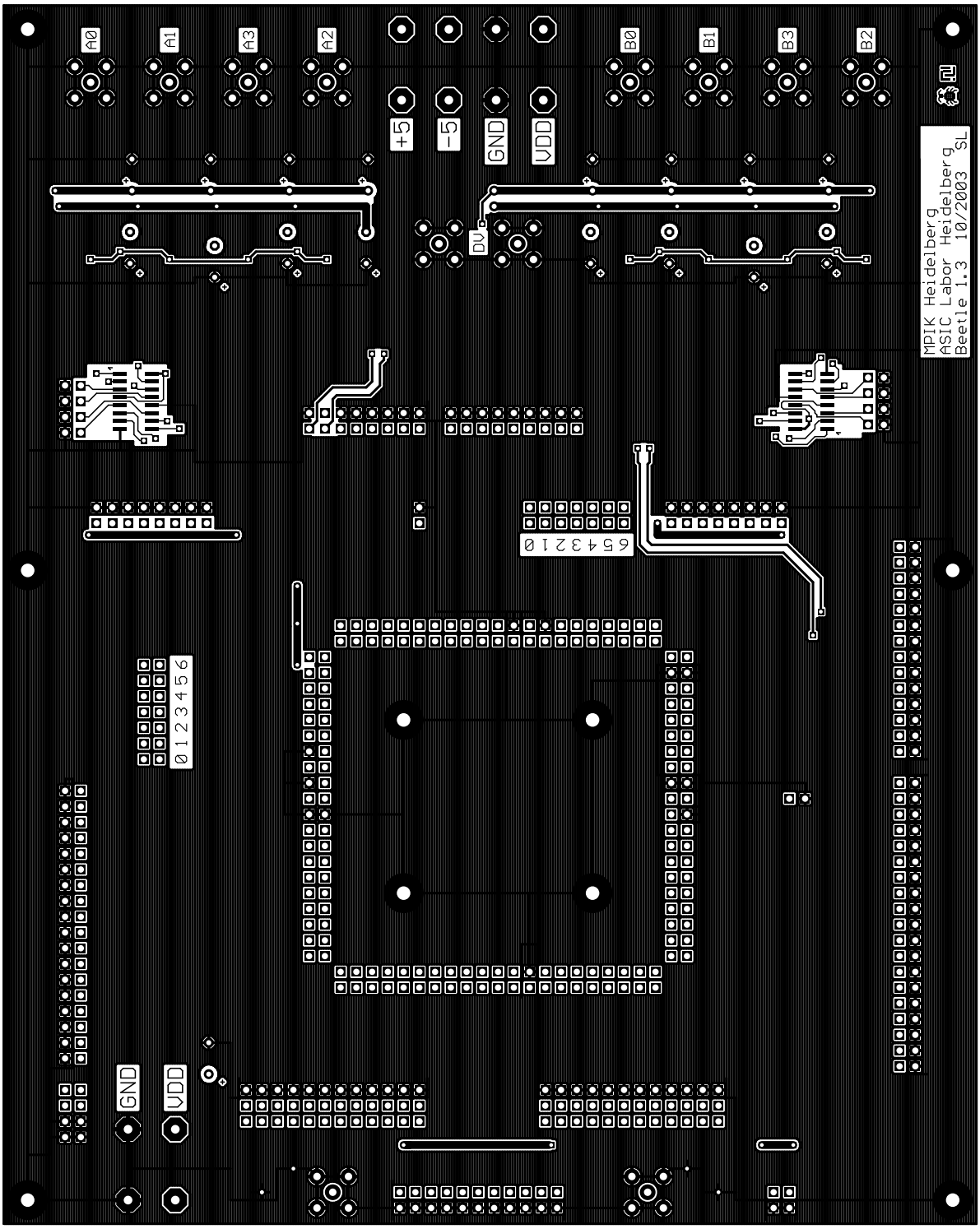


Figure C.27: Top side layout of the Heidelberg mother board.

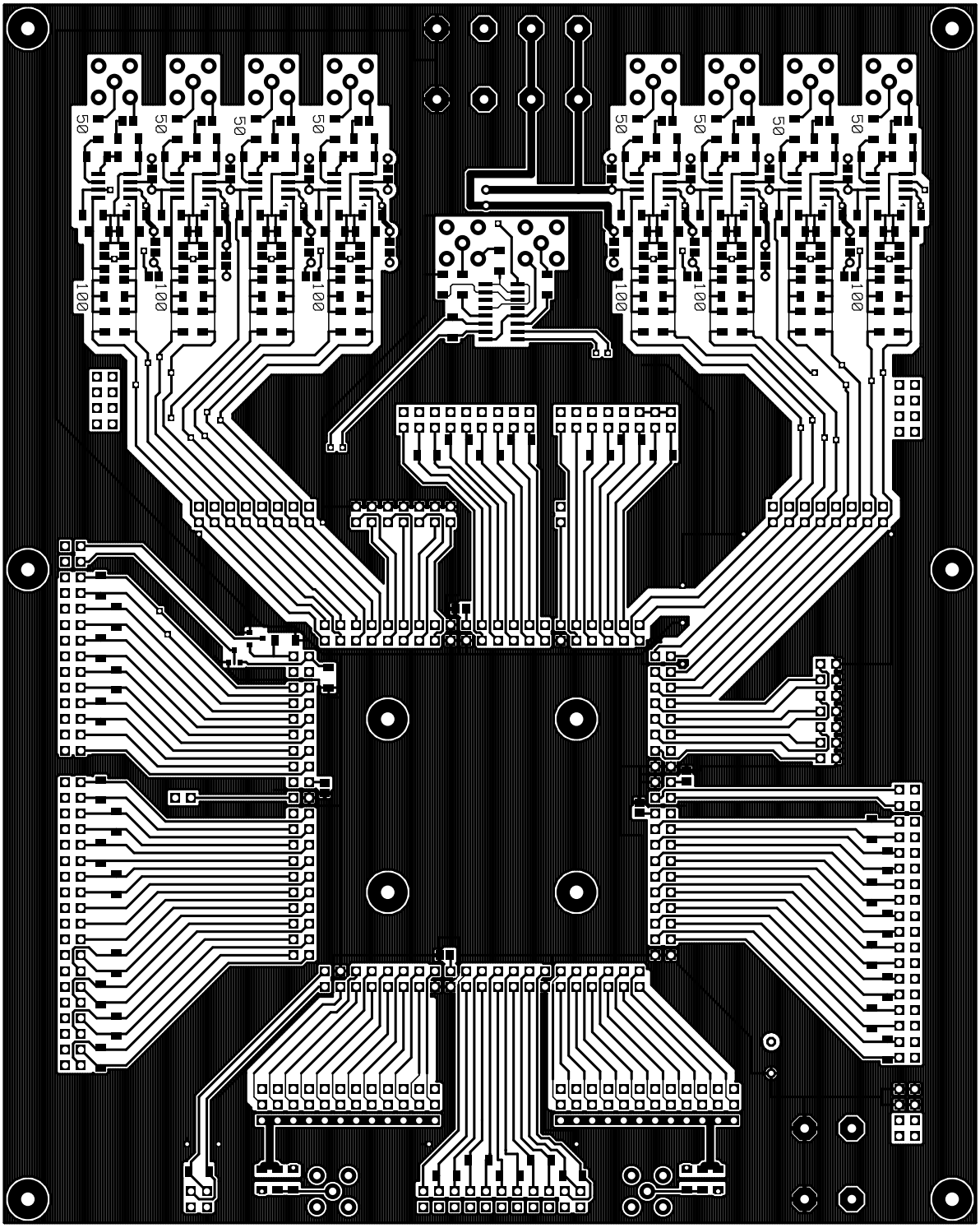


Figure C.28: Bottom side layout of the Heidelberg mother board.

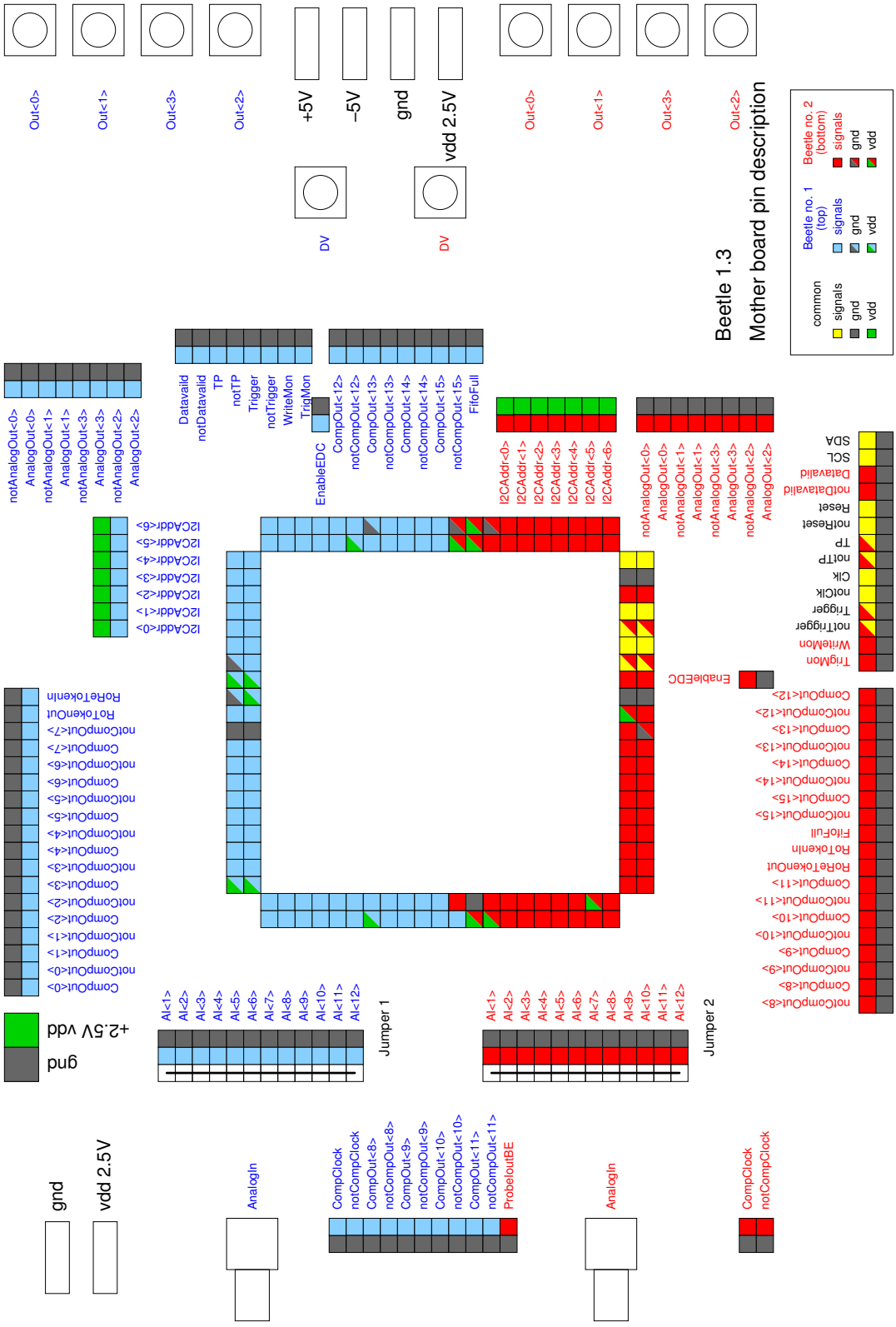


Figure C.29: Pin configuration of the Heidelberg mother board.

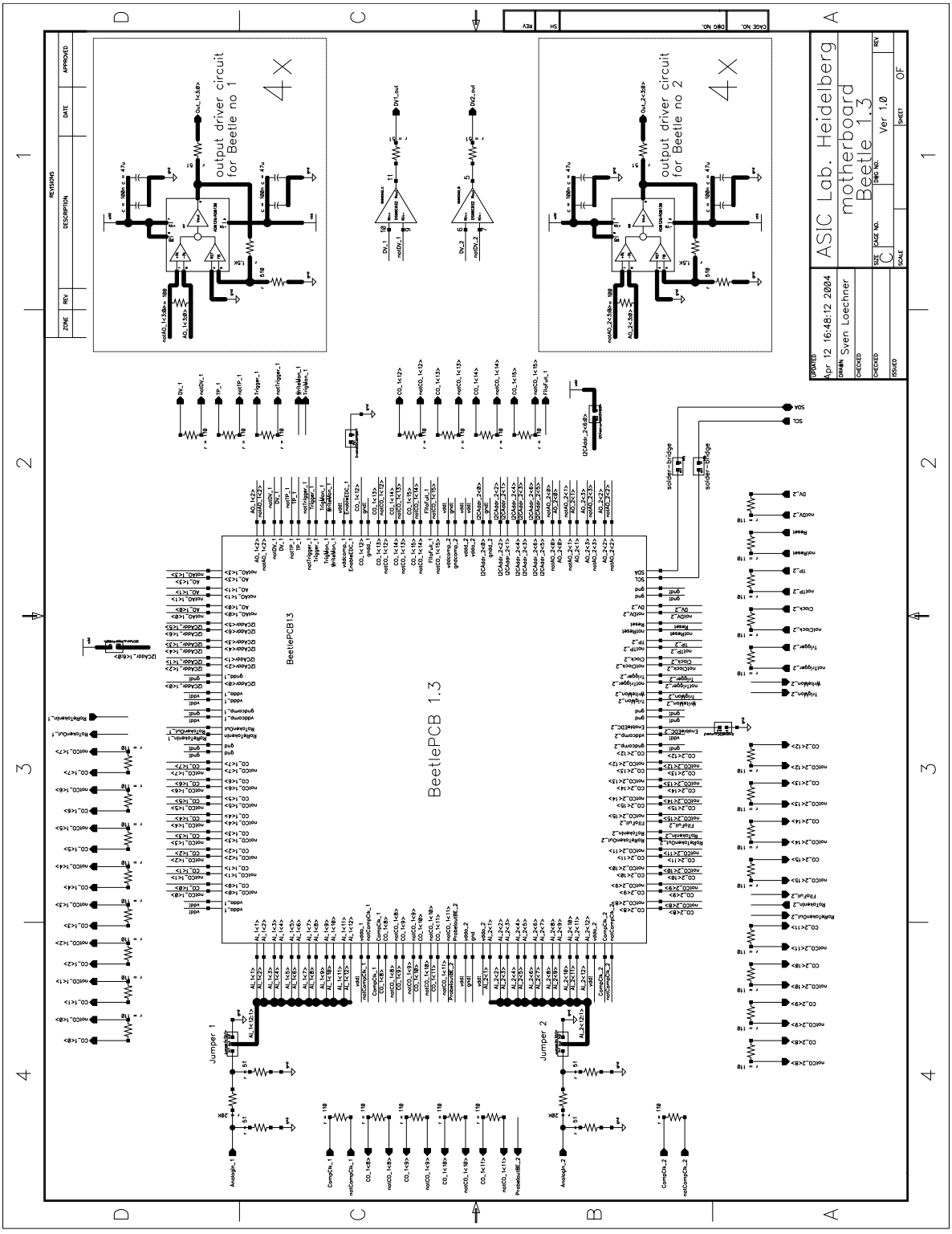


Figure C.30: Schematic diagram of the Heidelberg mother board.

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