Custom integrated circuit development for LHC Experiments

The Beetle Readout Chip

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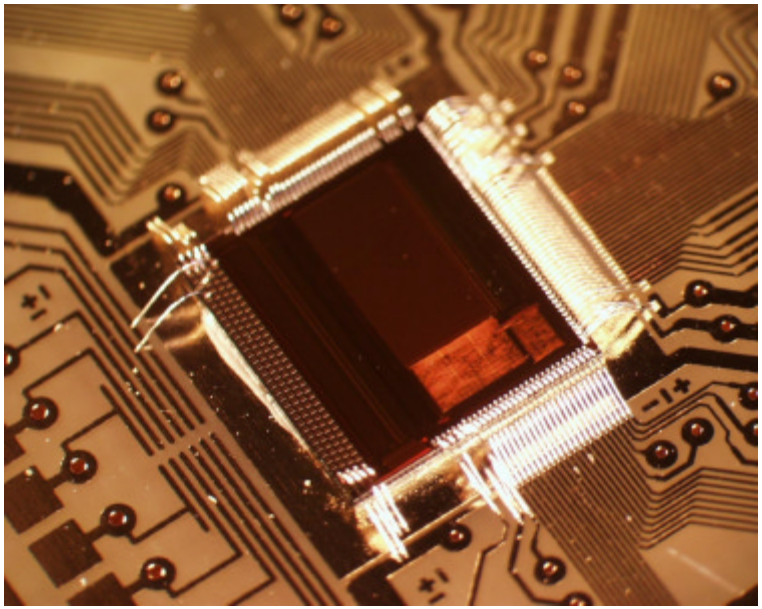
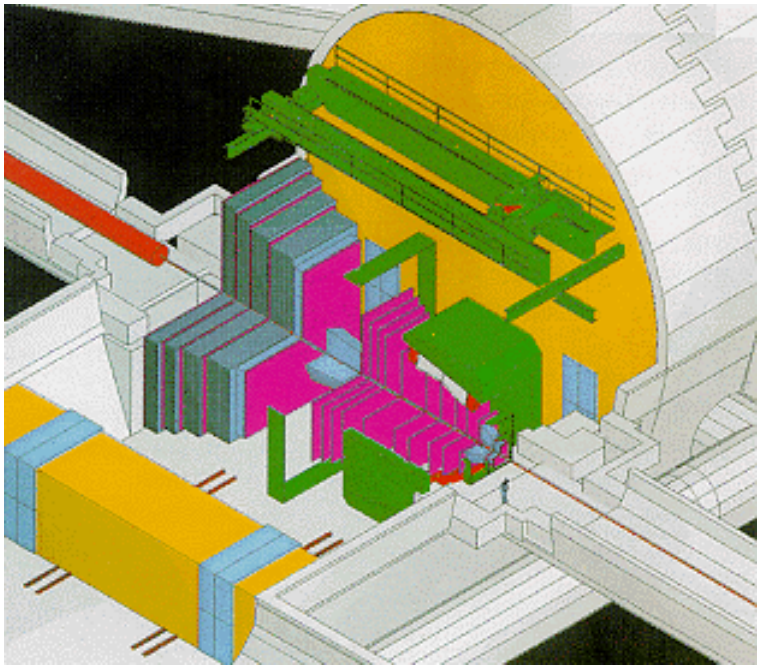
Outline

- LHCb experiment
  - requirements
- Beetle development
  - chip architecture / floor plan
  - key measurements
- Subdetectors
- Outlook



Integrated circuit “Beetle”

LHCb experiment

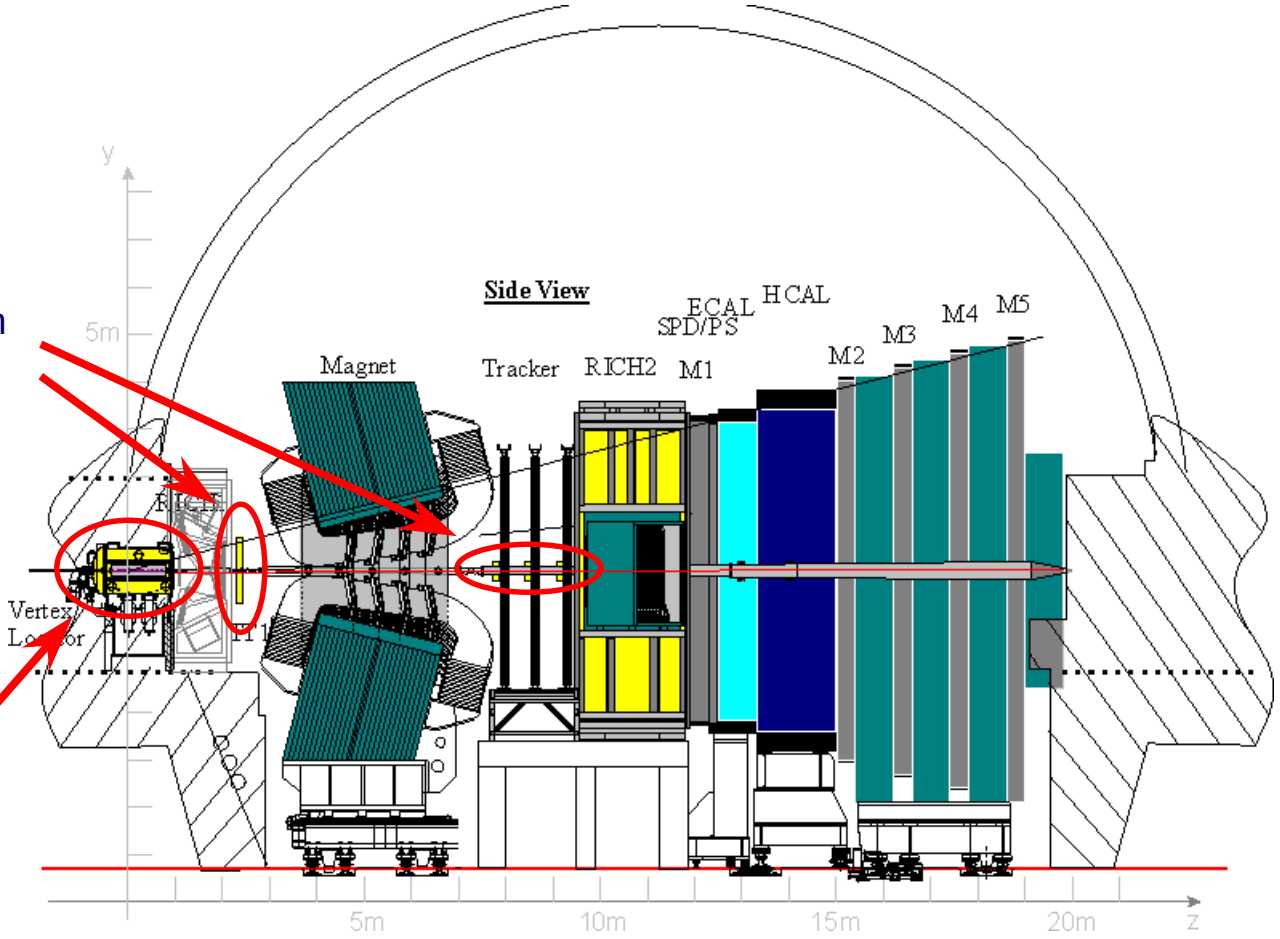


- **Next-generation experiment to study CP-violation and rare decays in the B-meson system at LHC**
- **40 MHz *pp*-collision rate**
- **B-mesons every 200 collisions**
- **Key specifications of front-end readout:**
  - fast shaping ($t_{rise} \leq 25$ ns)
  - low noise (S/N > 12)
  - large bandwidth (~20 TByte/s)
  - radiation hardness (^{3} 10 Mrad)

LHCb detector

- **Si**licon **T**racker **(ST):**
  - silicon-strip detector
  - ~ 200 µm pitch
  - strip length up to 33 cm
  - Input load up to 50 pF
  - **300.000** channels
  - 11 m²

- **Ve**rtex **Lo**cator **(VeLo):**
  - silicon-strip sensor
  - 37 µm to 92 µm pitch
  - Input load < 10 pF
  - **200.000** channels



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Requirements

Summary of the major requirements for the readout electronics:

- **large number of detector channels (~500.000 channels)**
- **huge amount of sampling data (~20 TB/s)**
- **radiation hardness of electronic devices**

not possible to use discrete components

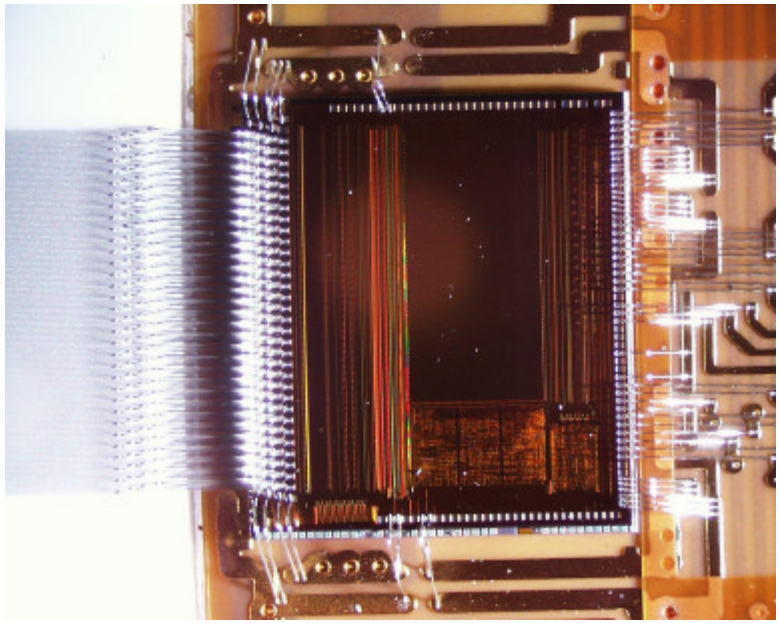
no commercial devices are available

Solution: Development of an Application-Specific Integrated Circuit (ASIC)
Þ Beetle readout chip

in the ASIC-Lab, founded 1994 by MPI and University of Heidelberg

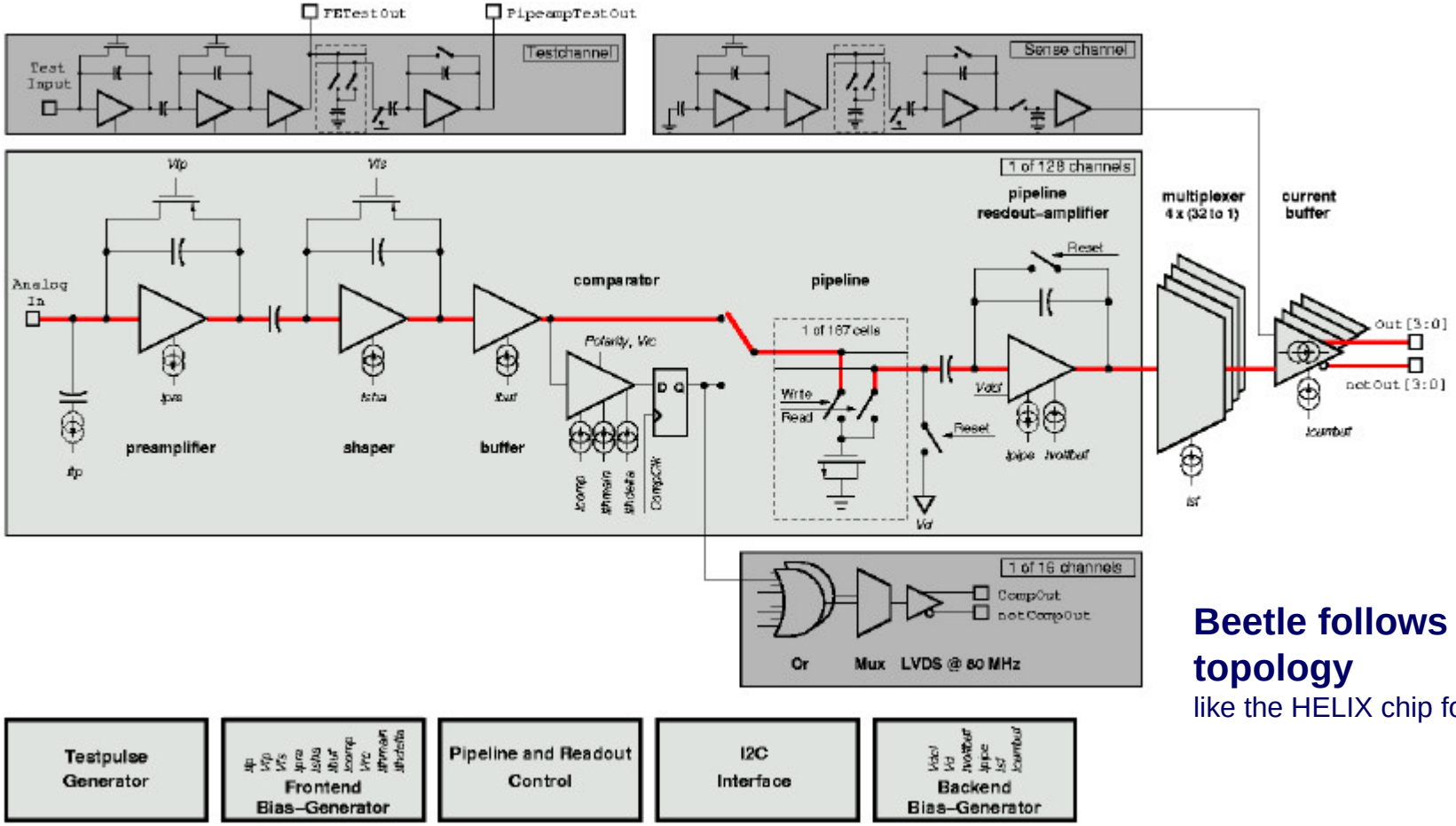
Beetle development

- LHCb experiment
  - requirements
- **Beetle development**
  - **chip architecture / floor plan**
  - **key measurements**
- Subdetectors
- Outlook



Beetle on a IT hybrid

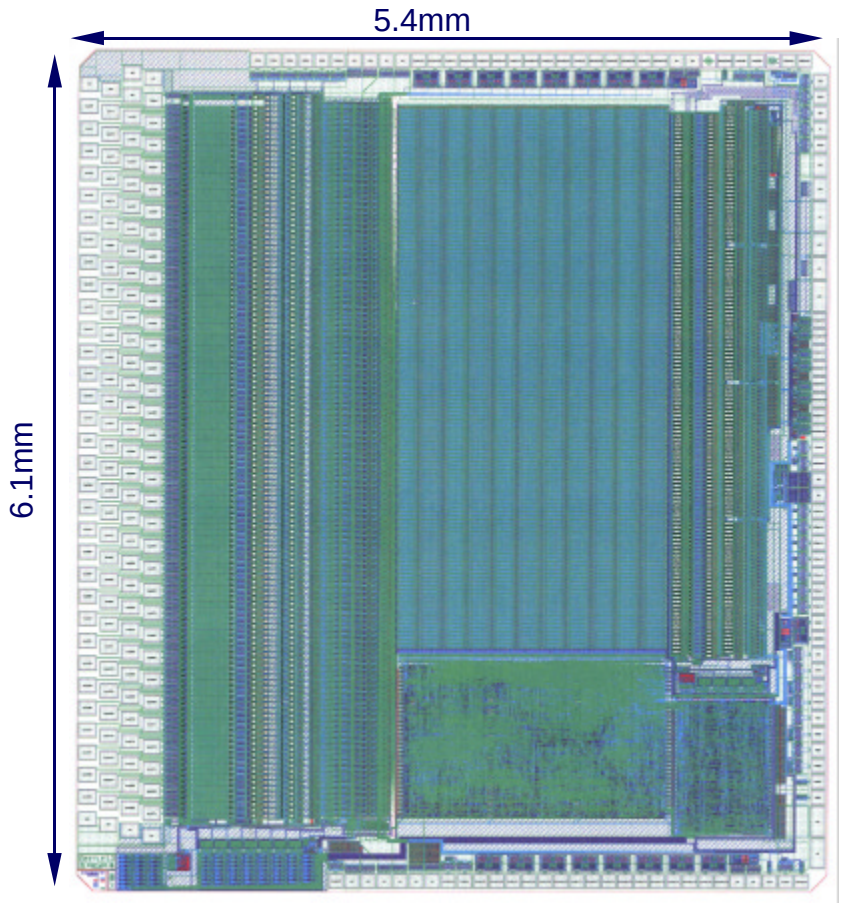
Beetle: Architecture

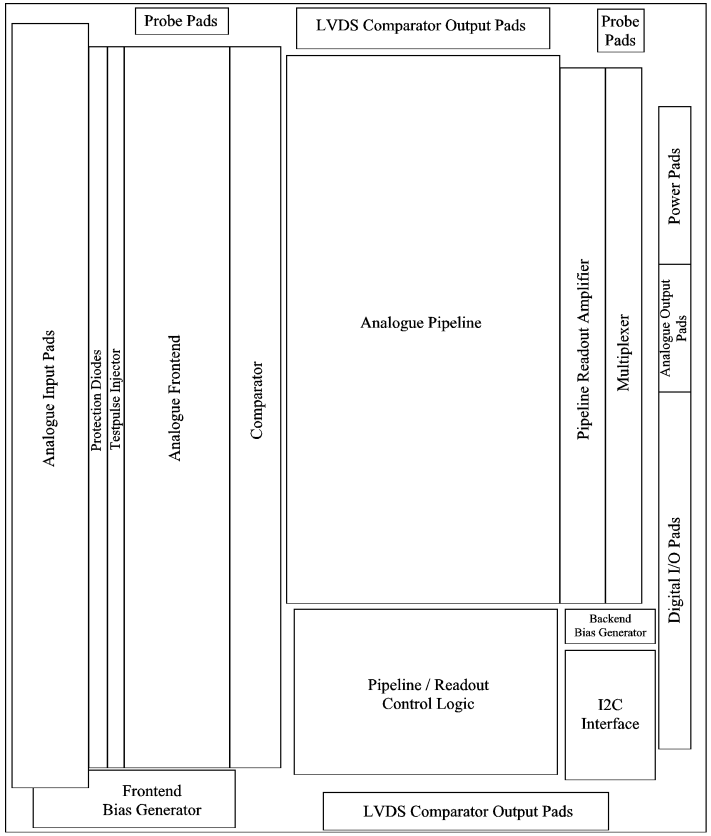


Beetle follows RD 20 topology

like the HELIX chip for HERA-B

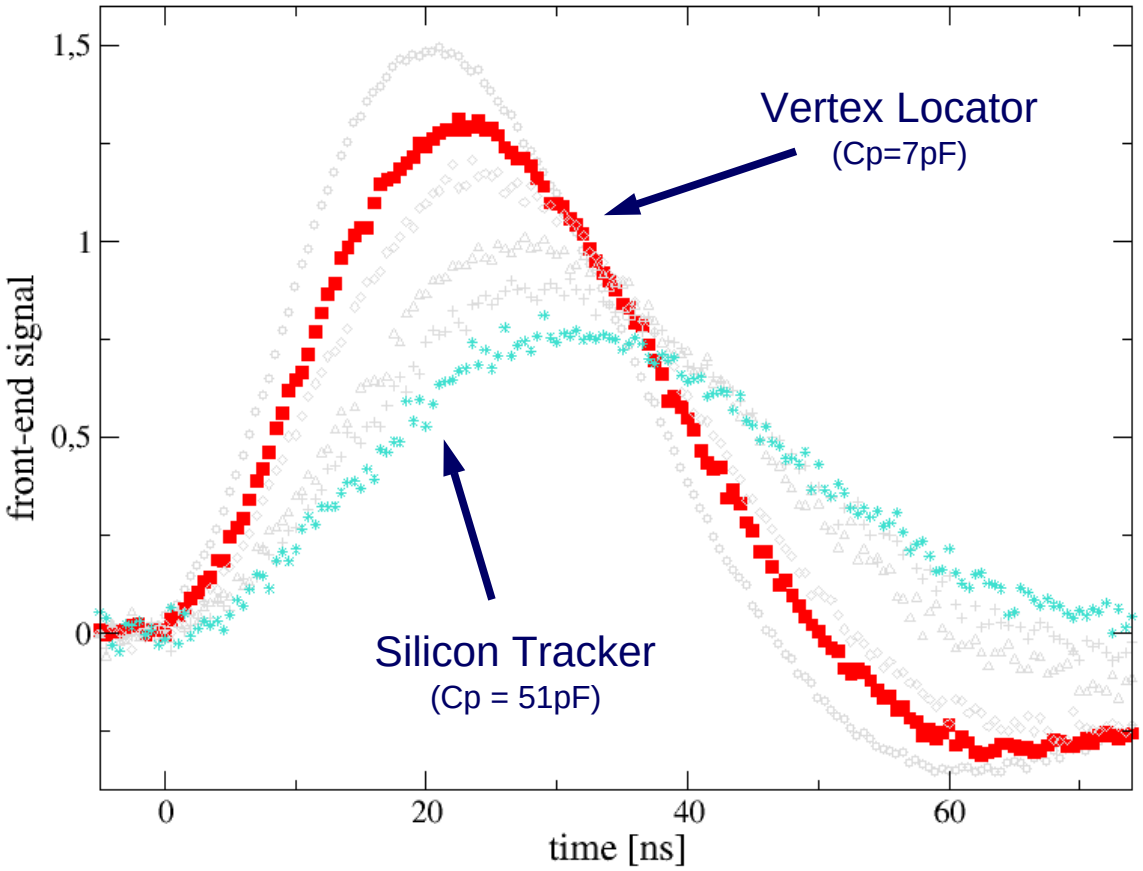
Beetle: Layout / Floor plan





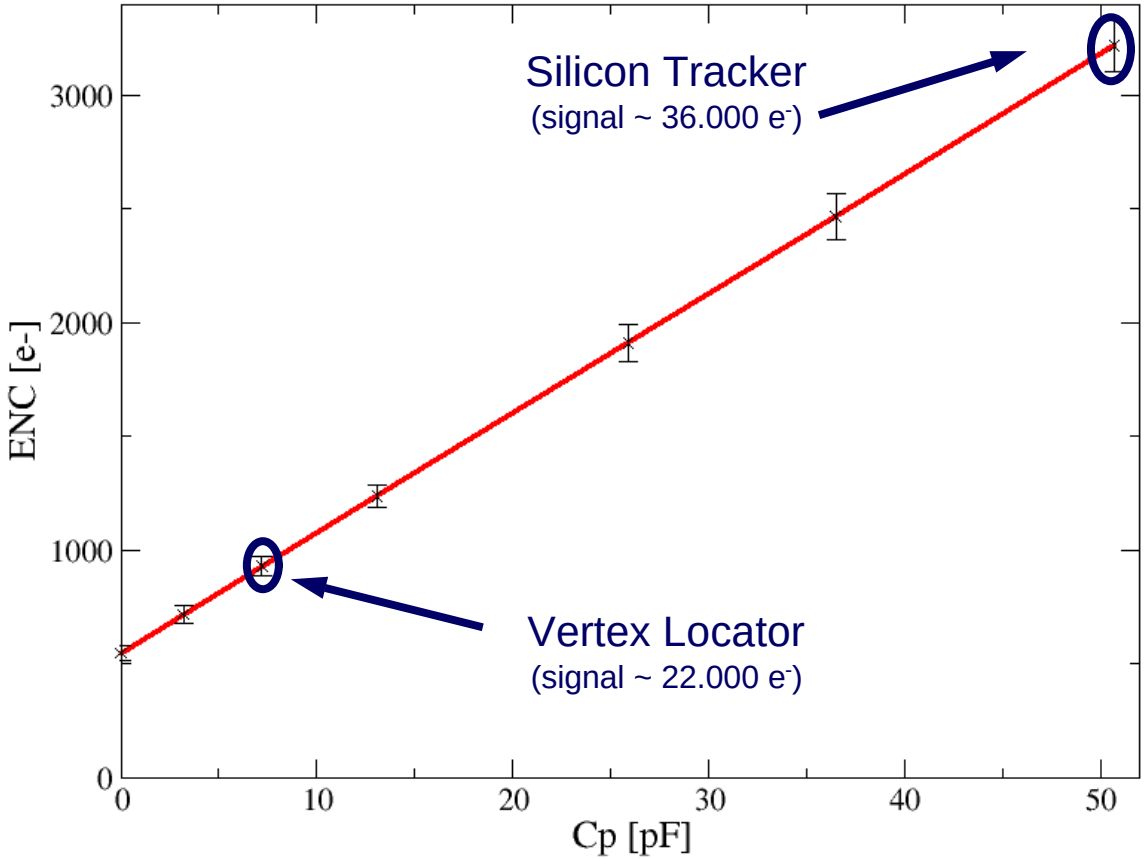
Layout of the final Beetle chip and its corresponding floor plan.

Front end: Pulseshape



Front end behaviour for different detector capacitances C_p

Equivalent Noise Charge



Equivalent Noise Charge (ENC) of a Beetle chip

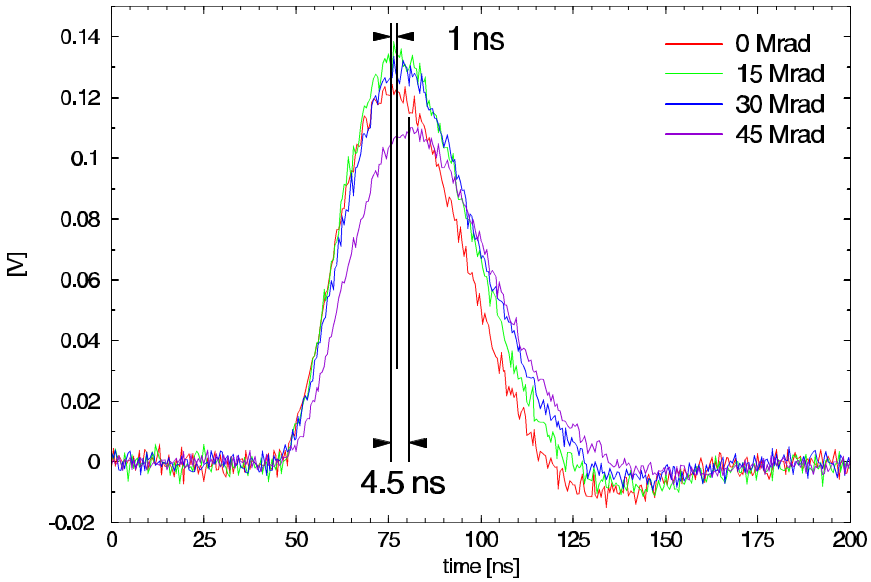
Front end, Pipeline, Pipeamp, Readout

ENC = 547.7 e^- + 52.6 e^-/pF

Radiation hardness (I)

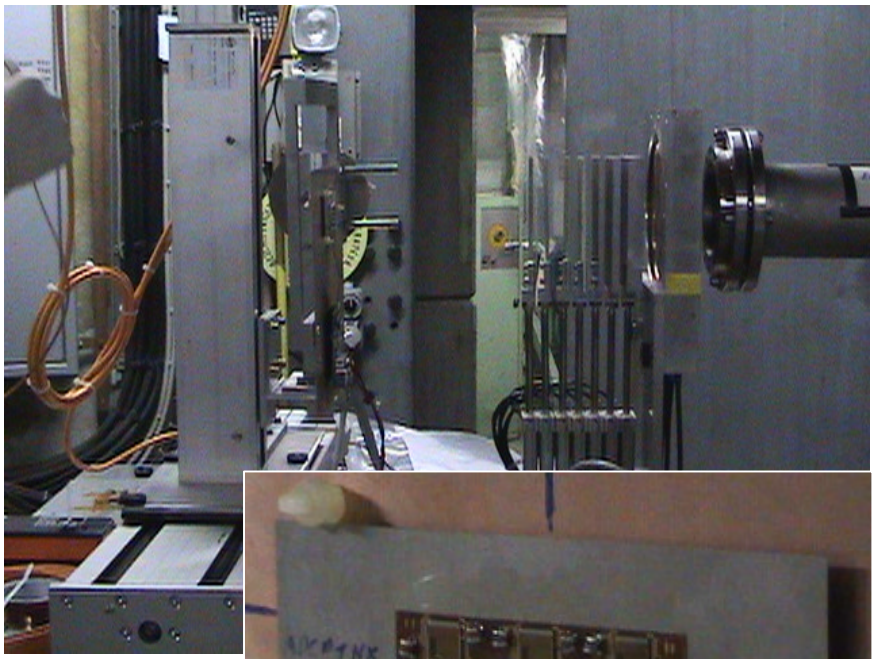
- **Total Ionizing Dose (TID) irradiation at CERN's X-ray facility**
- **Irradiated up to 45 Mrad total dose**
- **Beetle shows**
  - full trigger and readout functionality
  - full read/write access via I²C
- **Performance degradations are small**
  - peaktime: up to 30 Mrad: $\Delta t \leq 1$ ns
    up to 45 Mrad: $\Delta t \leq 4{,}5$ ns
  - gain: up to 45 Mrad: $\Delta \leq 10\%$

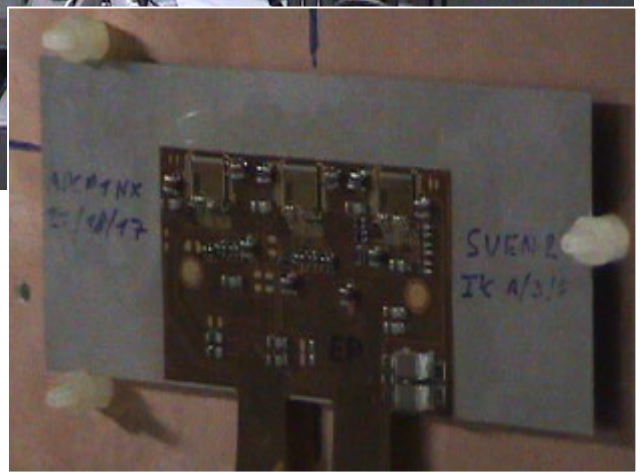
Predecessor chip (HELIX) died already at 400 krad



Radiation hardness (II)

- **Single Event Upset (SEU): bit-flips in registers by large localised ionising particles**
- **Irradiation:**
  - **65 MeV protons**
  - **accumulated dose: 7.93 Mrad**
    (mean flux: 1.56 x 10^9 p/cm²/s)





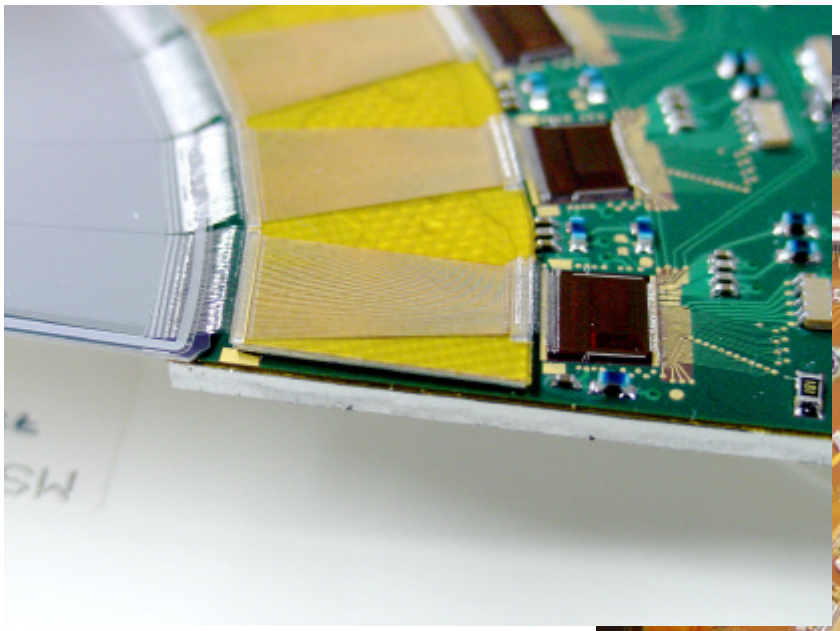
SEU cross section for a std. flip flop

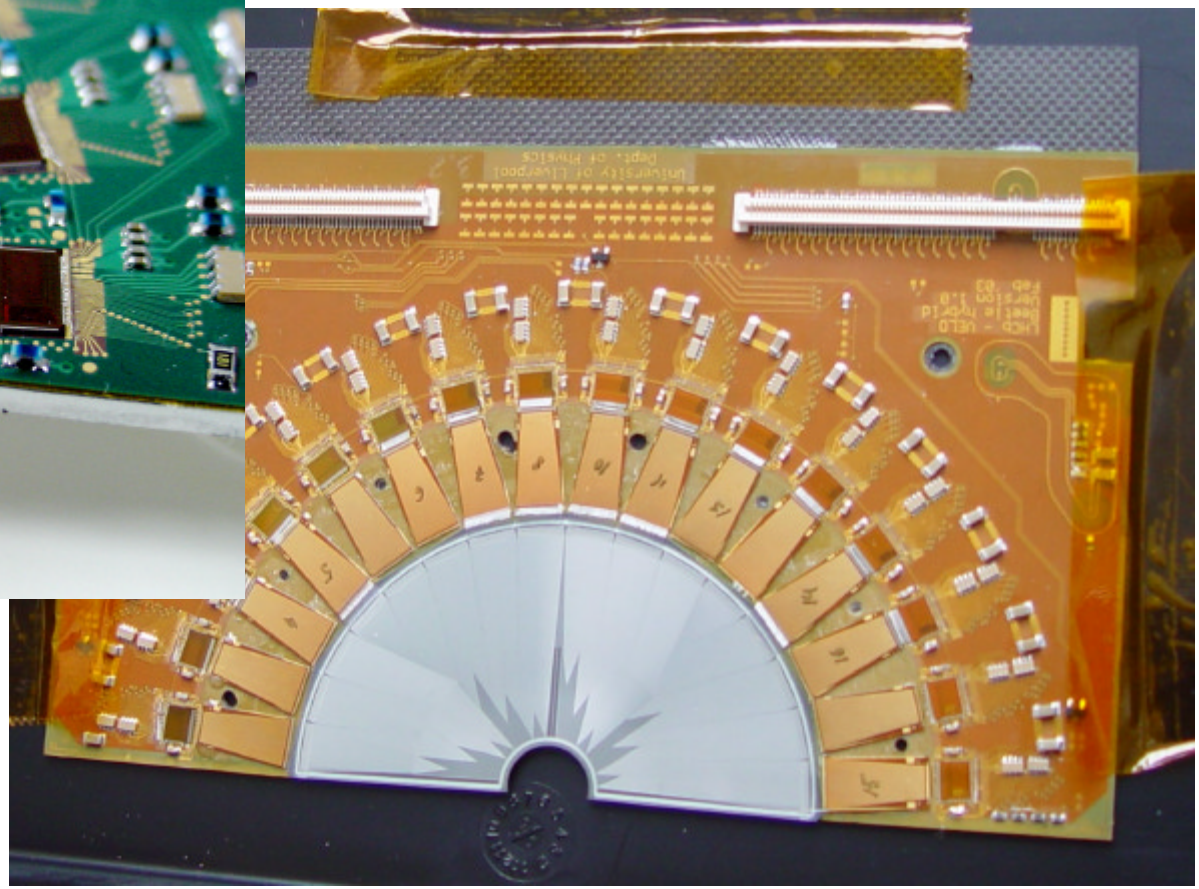
σ **= (1.12 ± 0.56) · 10^{-16} cm²** (for 65 MeV protons)

or 1 SEU per 25 minutes (VELO)

SEUs in registers are corrected by the Beetle

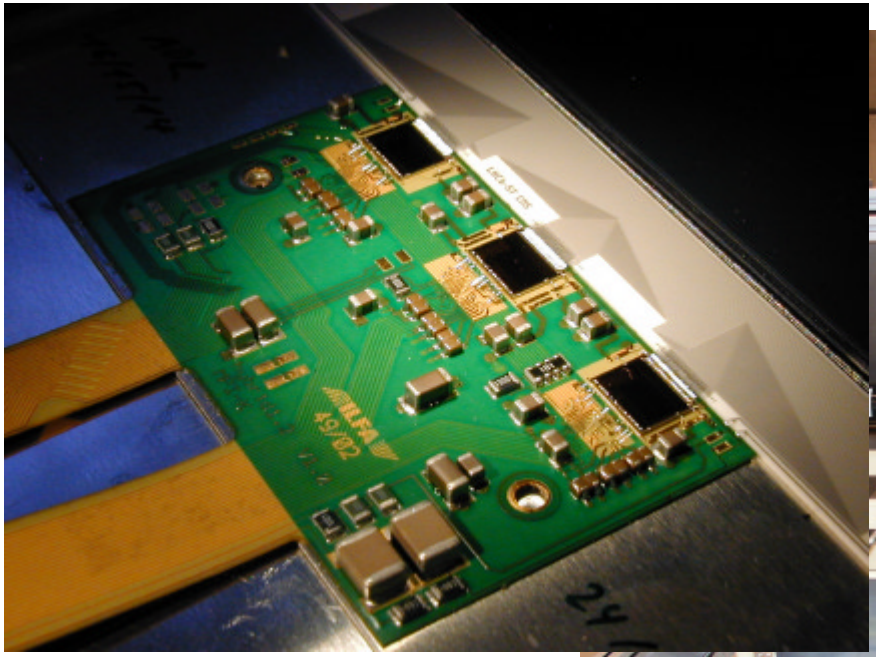
Vertex Locator

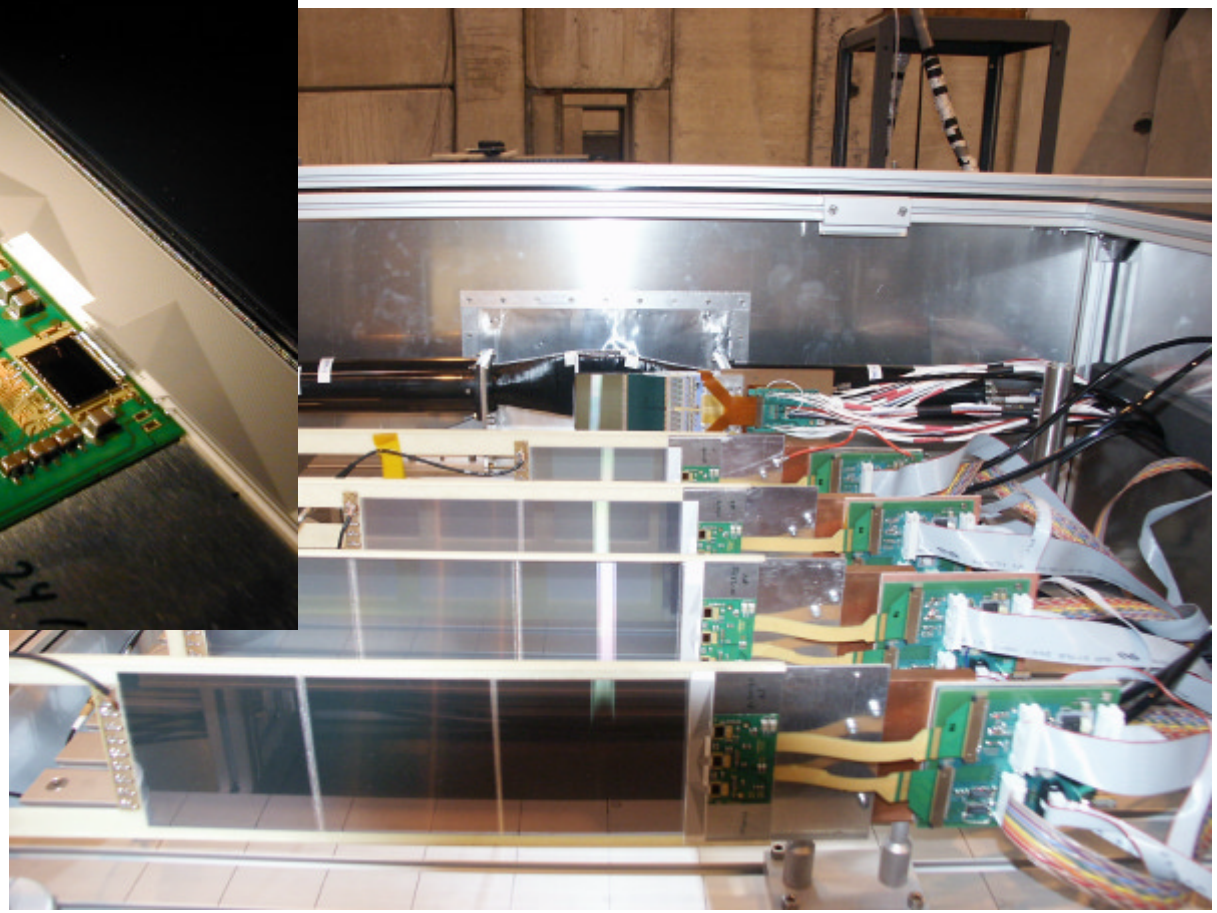




First prototype of a Vertex Locator hybrid

Silicon Tracker





Silicon Tracker hybrid

Summary / Outlook

- **Beetle was tested and characterised thoroughly in the lab and testbeams**
- **Fulfills all specifications**
  - **no defects were found on the chip which would prevent a use in LHCb.**
- **Start of mass-production: May 2004**
  - **in total 54 wafer (8”) will be produced**
  - **with an expected yield of 85% production results in 30.000 chips**
- **MPI is responsible for the mass-production tests**
- **Start of LHCb is planned for 2007**