ASIC-Labor Heidelberg

Beetle 1.0 Tests

25 Beetle 1.0 arrived at the ASIC Lab on September 7th.

2 Beetle 1.0 chips glued and bonded on the test-pcb

General

- total current: 50mA
- current source: OK
- output signal of LVDS: OK

Slowcontrol

- I2C: - Acknowledge: OK
  - from BeetlePA10 test-chip: I2C completely tested: OK
- internal reset-generator: OK

Fastcontrol

- control signals for pipeline latency: OK

Beetle 1.0 Tests

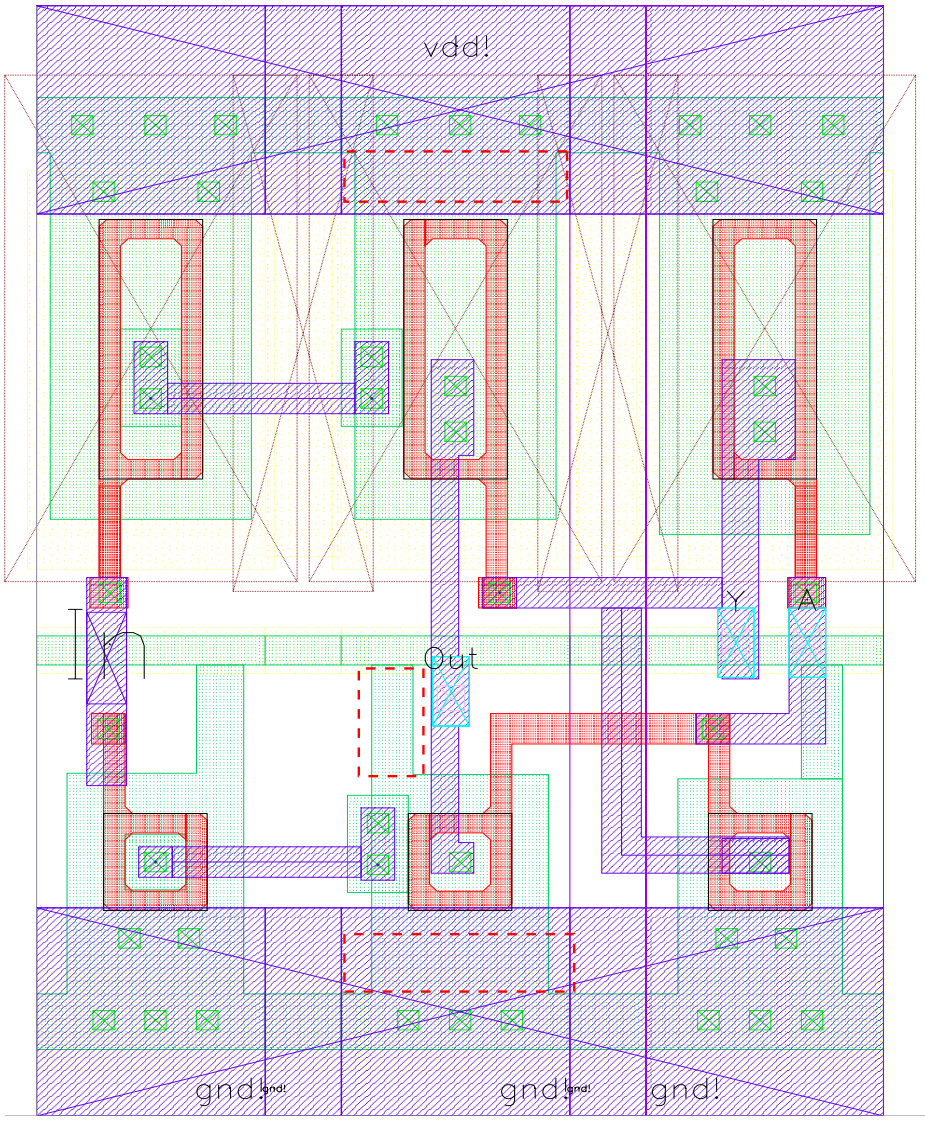
Problems:

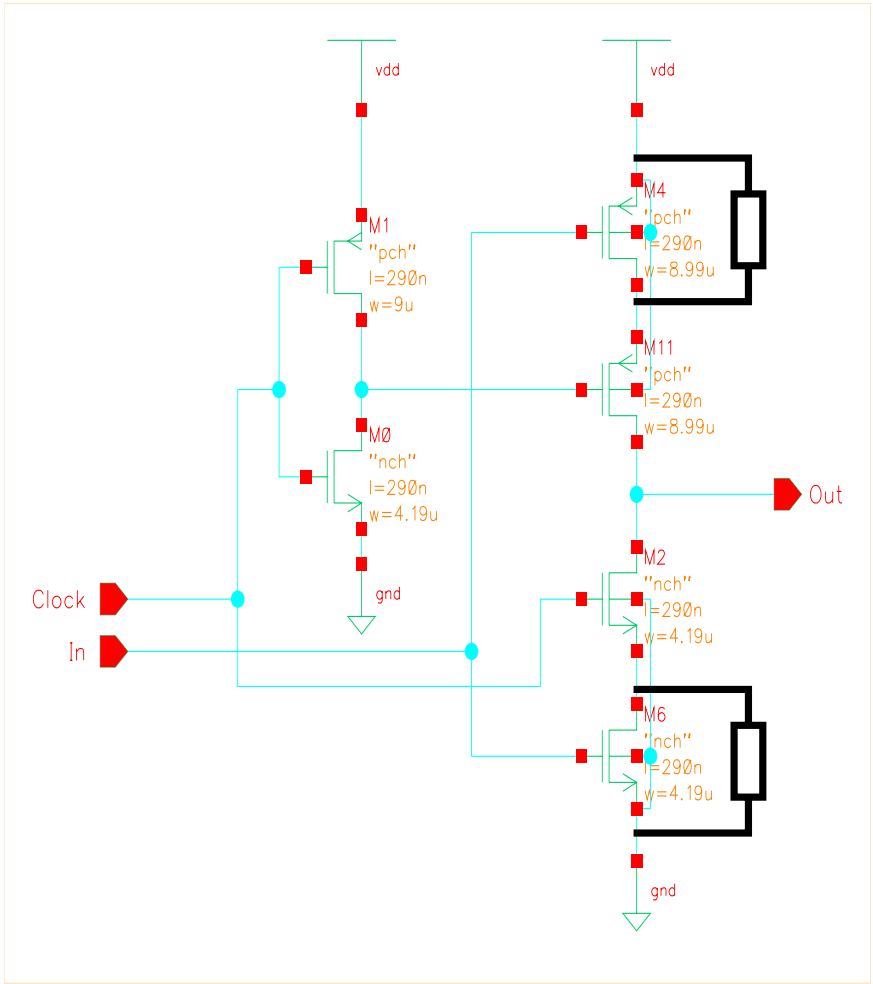
- internal databus between slowcontrol and registers is always zero
  -> registers are always zero -> Beetle isn't programmable

Reason for databus-problem:

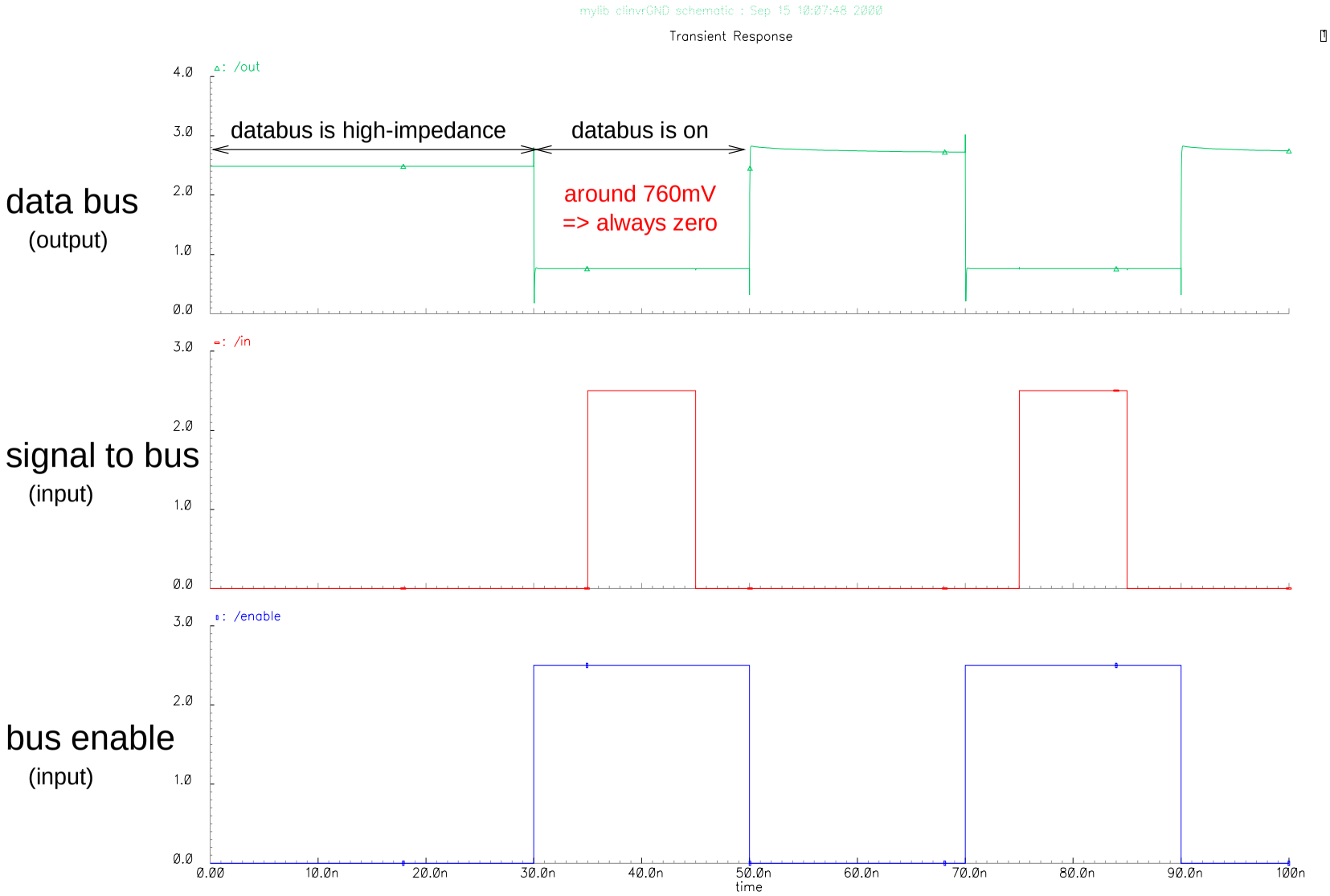
an error in the extraction rules causes that a diffusion shortcut wasn't seen in the LVS check.

Tristate Error

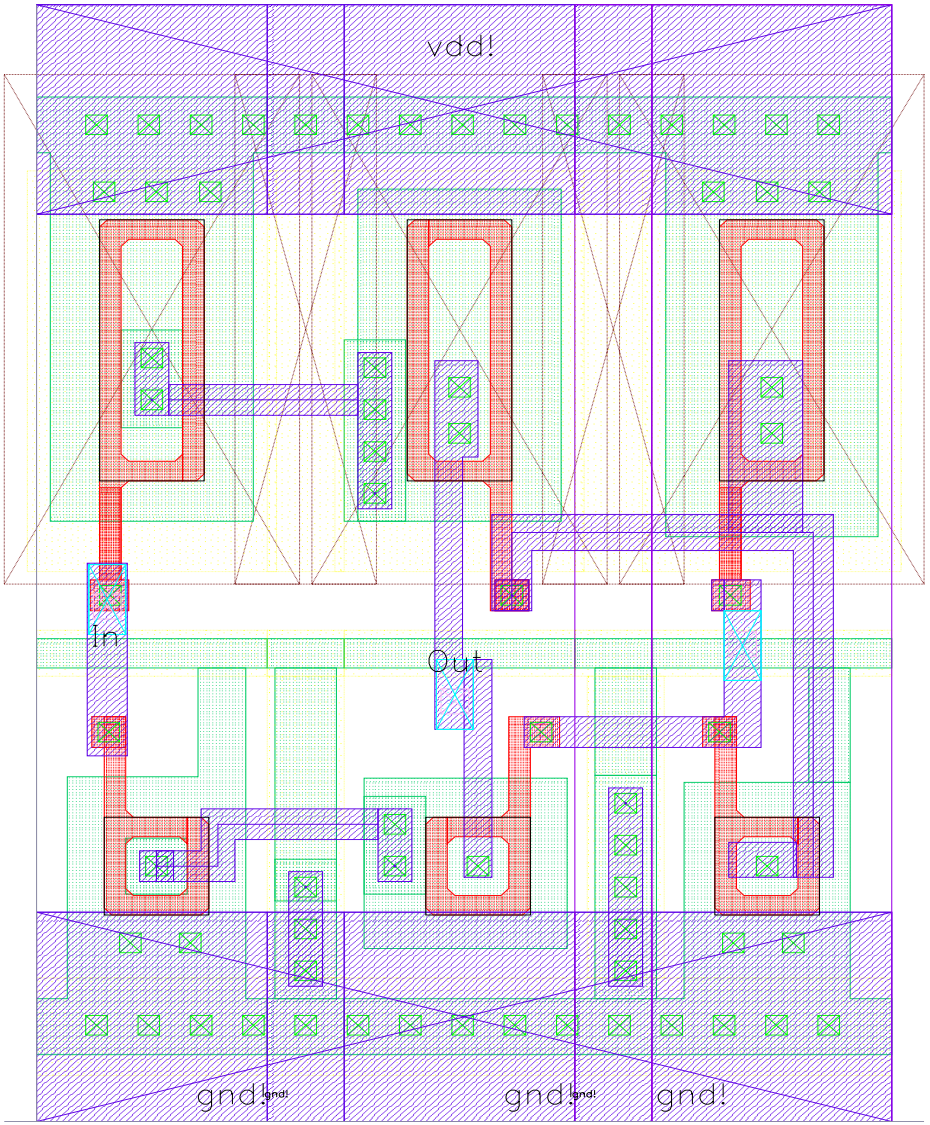




Bad Tristate Simulation



New Tristate Layout



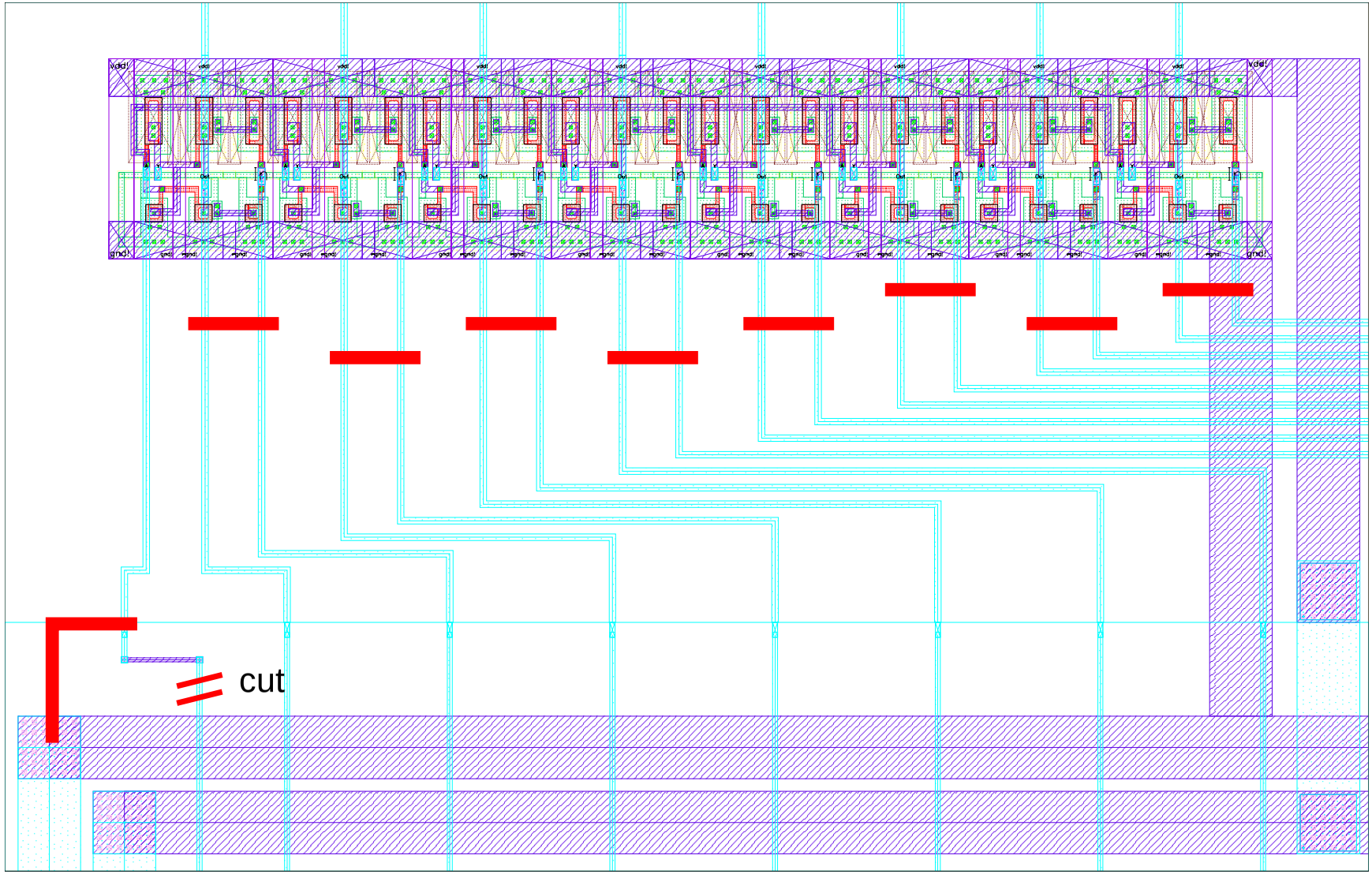
- diffusions of pmos separated from vdd
- diffusions of nmos separated from gnd
- another guardring around nmos

Way out for Beetle 1.0 problem?

Tristate-Patch with a FIB at Micrion, Munich

=> all register can hopefully be programmed

Micrion-Patch



Further measurements on testchips

BeetleCO

- frontend and comparator
- analog output driver

BeetlePA

- pipeline
- pipeline-amplifier
- LVDS-pads

BeetleMA

- modified frontend for MAPMT