ASIC-Labor Heidelberg

Beetle 1.0

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Status report on the Beetle development

Testchips (2mm x 2mm)

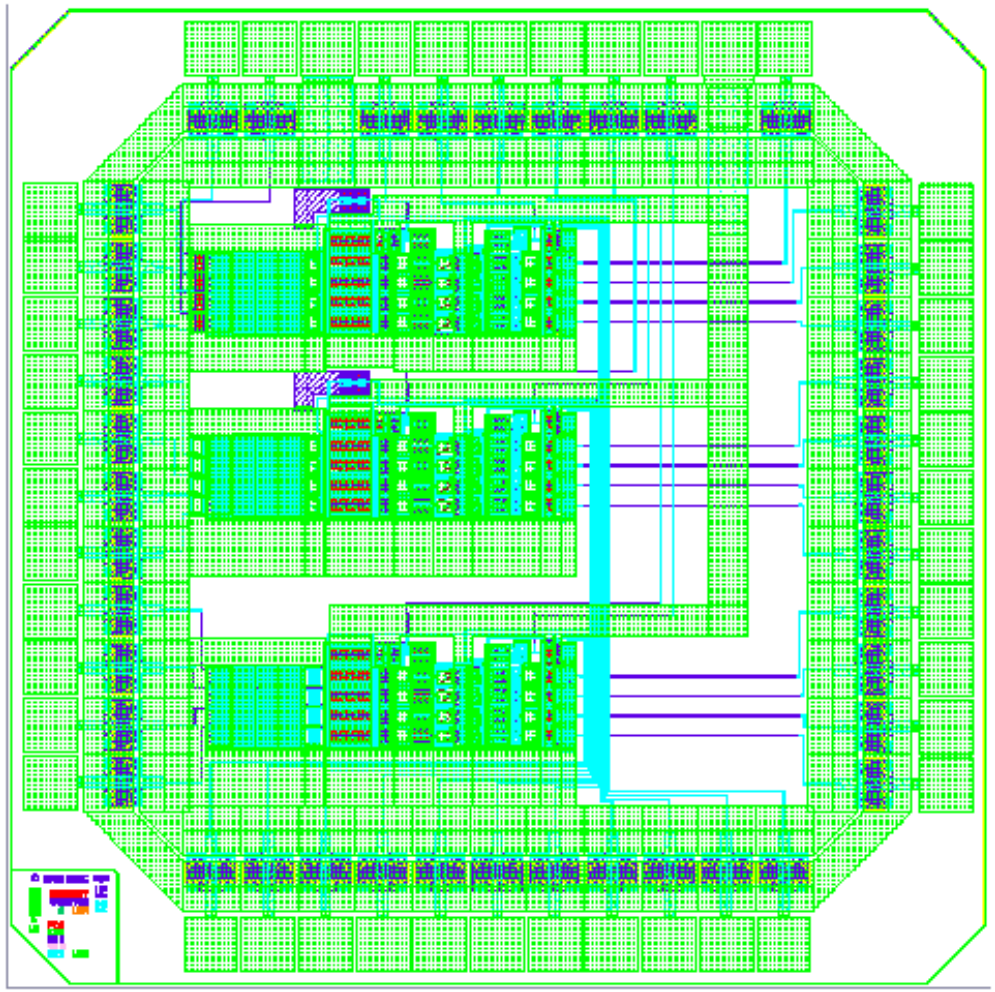
- BeetleMA (frontend for multianode-readout)
- BeetleCO (comparator)
- BeetlePA (pipeline amplifier)

First prototyp readout chip

- Beetle 1.0

all submitted to CERN in april 2000

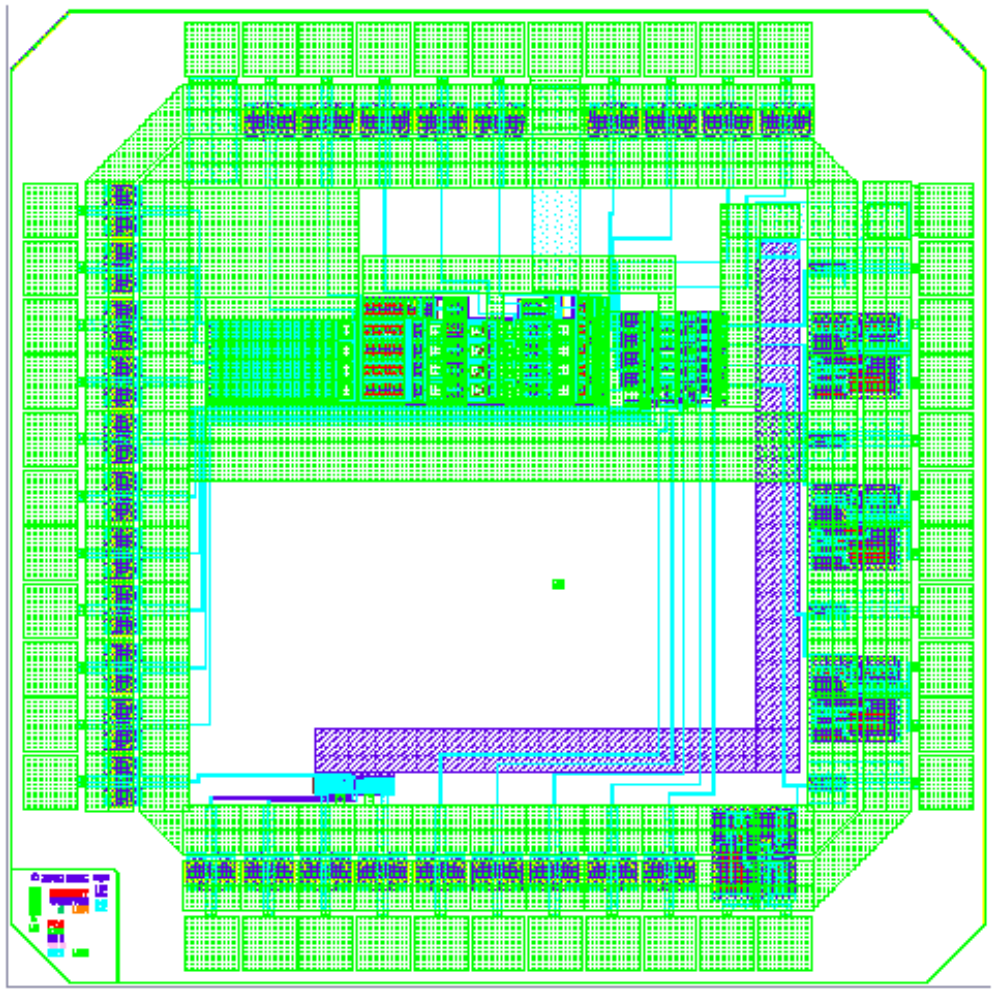
BeetleMA - Frontend for MAPMT



Modification of BeetleFE (submitted in july 1999) different voltage divider in front of the input of the frontend

Designed by Nigel Smale, University of Oxford

BeetleCO - Comparator

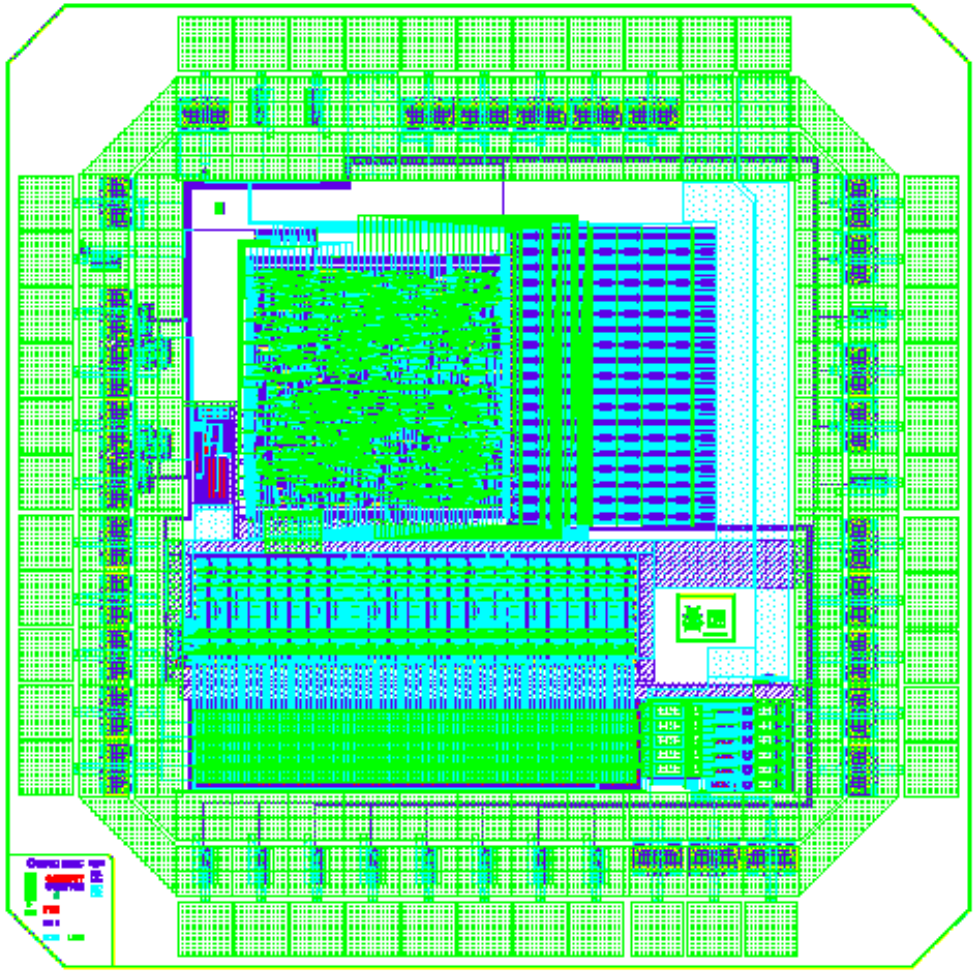


Relevant for Pileup veto and RICH binary option

Chip for comparator-tests
- frontend
- comparators
- analog output driver

Designed by Hans Verkoijen, NIKHEF Amsterdam

BeetlePA - Backup for Beetle 1.0



Pipeline-amplifier testchip
- 88 cells deep pipeline
- pipeline-amplifier
- I2C-Interface
- pads

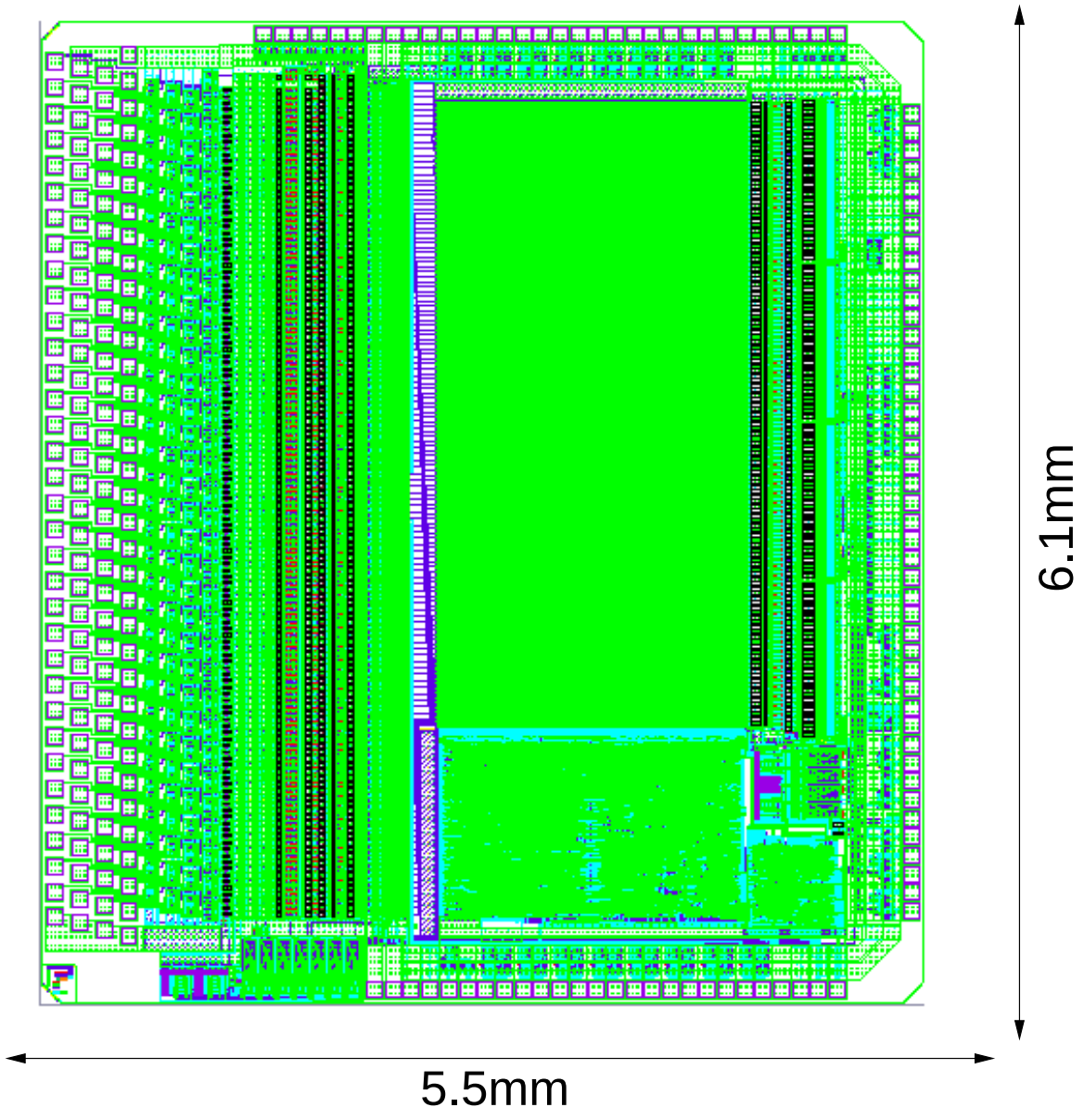
only used as a backup-chip

Designed in ASIC-Lab, Heidelberg

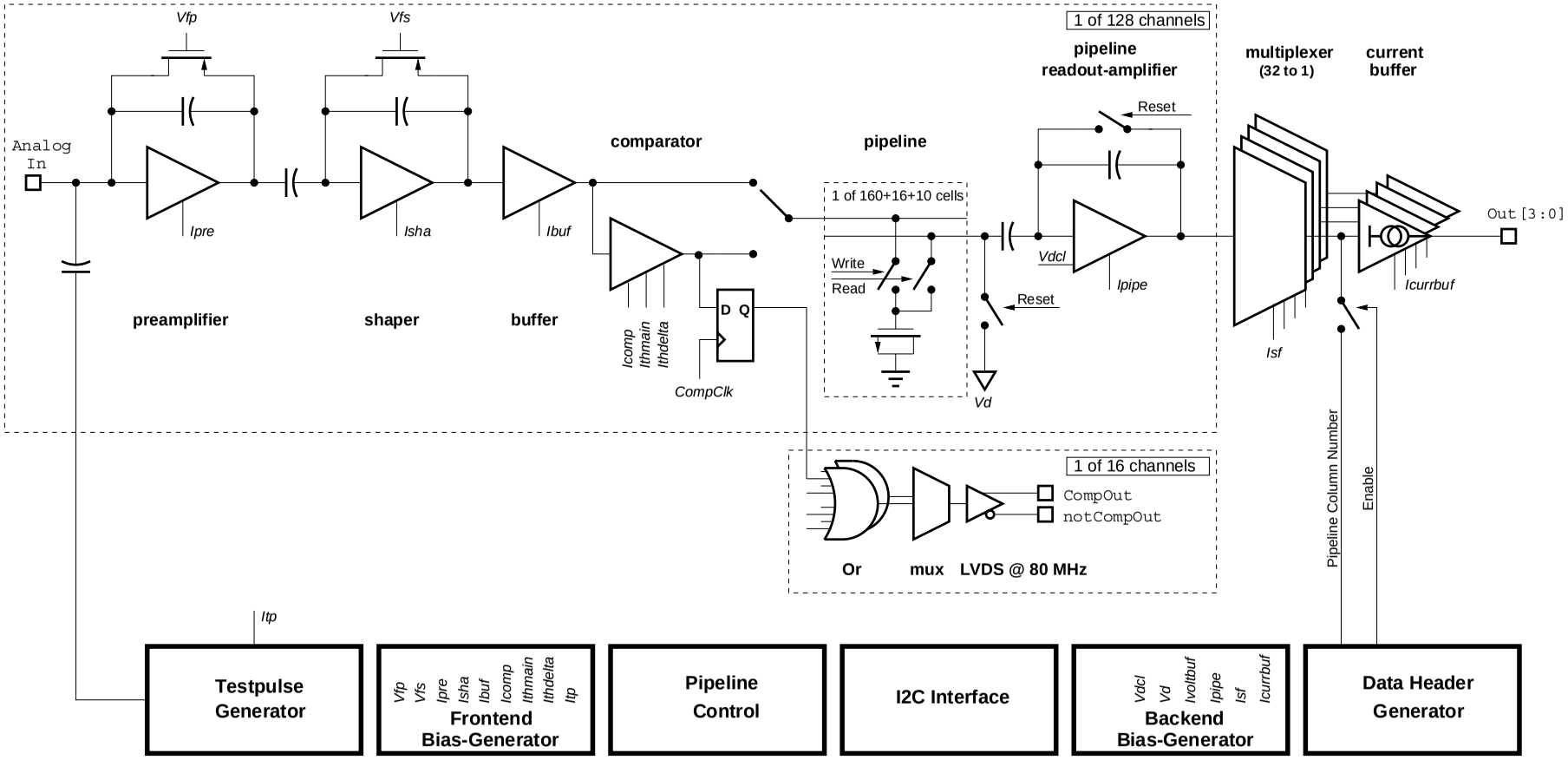
Beetle 1.0

input pitch: 41um

-> overall pitch: 50um
(chips in daisy-chain)

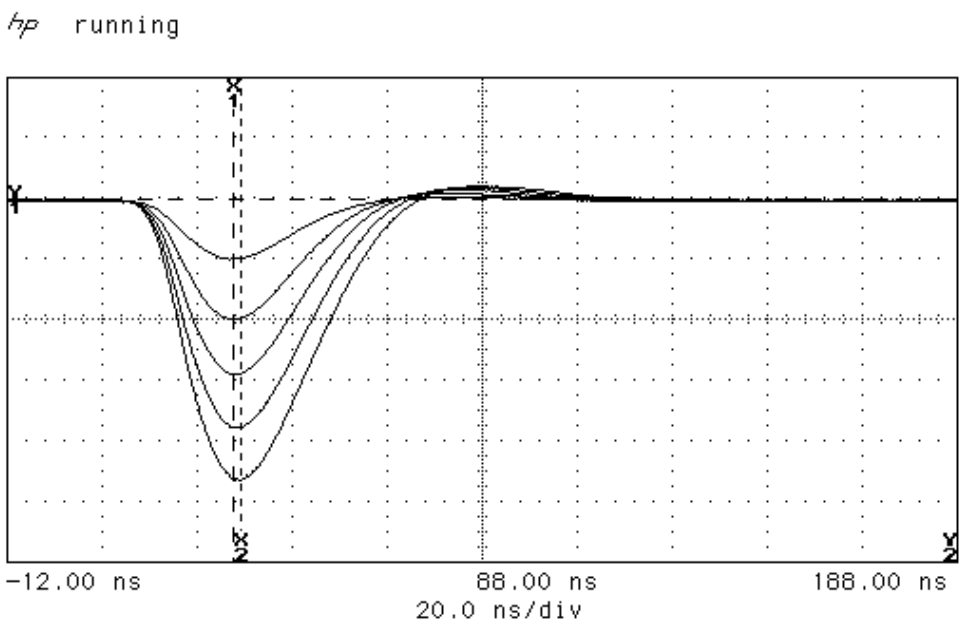


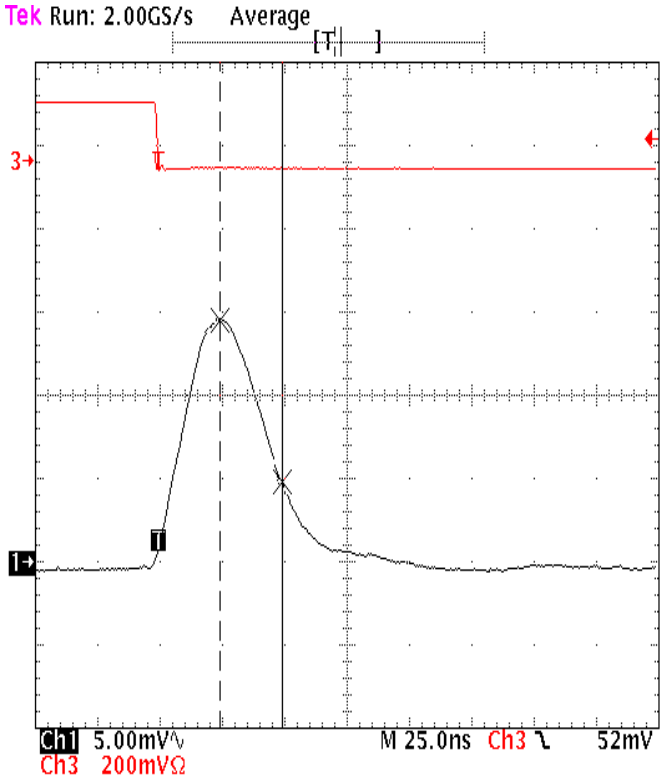
Block Diagram of the Beetle 1.0



Beetle 1.0 Frontend Amplifier

Same like on BeetleFE testchip





measured noise = 303e$^-$+ 33.6e$^-$/pF

dynamic range: +- 10 MIP = +- 110.000e$^-$

no peakshift for higher signals

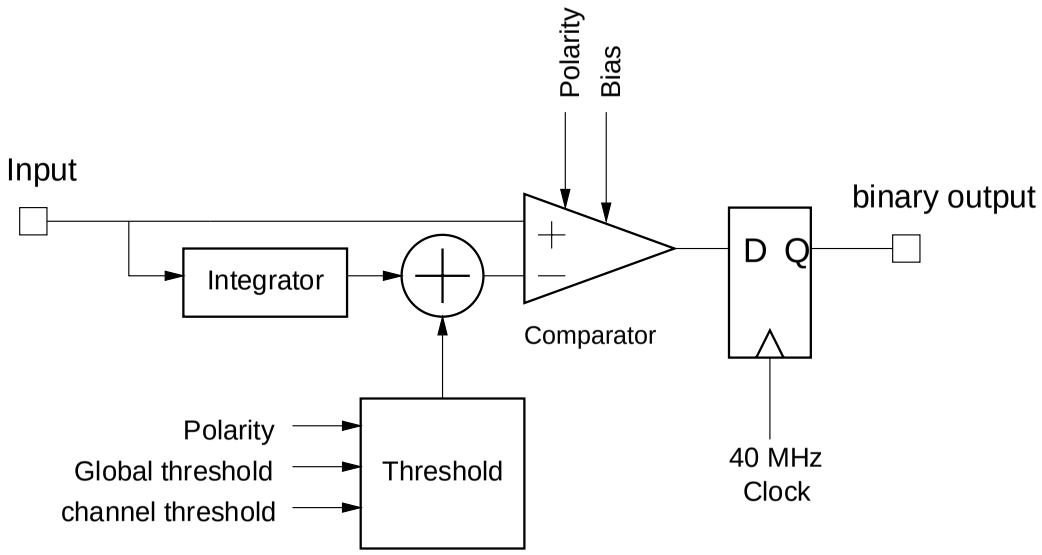
power consumption: 1.88mW / channel

risetime = 25ns

gain = 14.5 mV / 11.000e$^-$

remainder after 25ns = 30%

Comparator



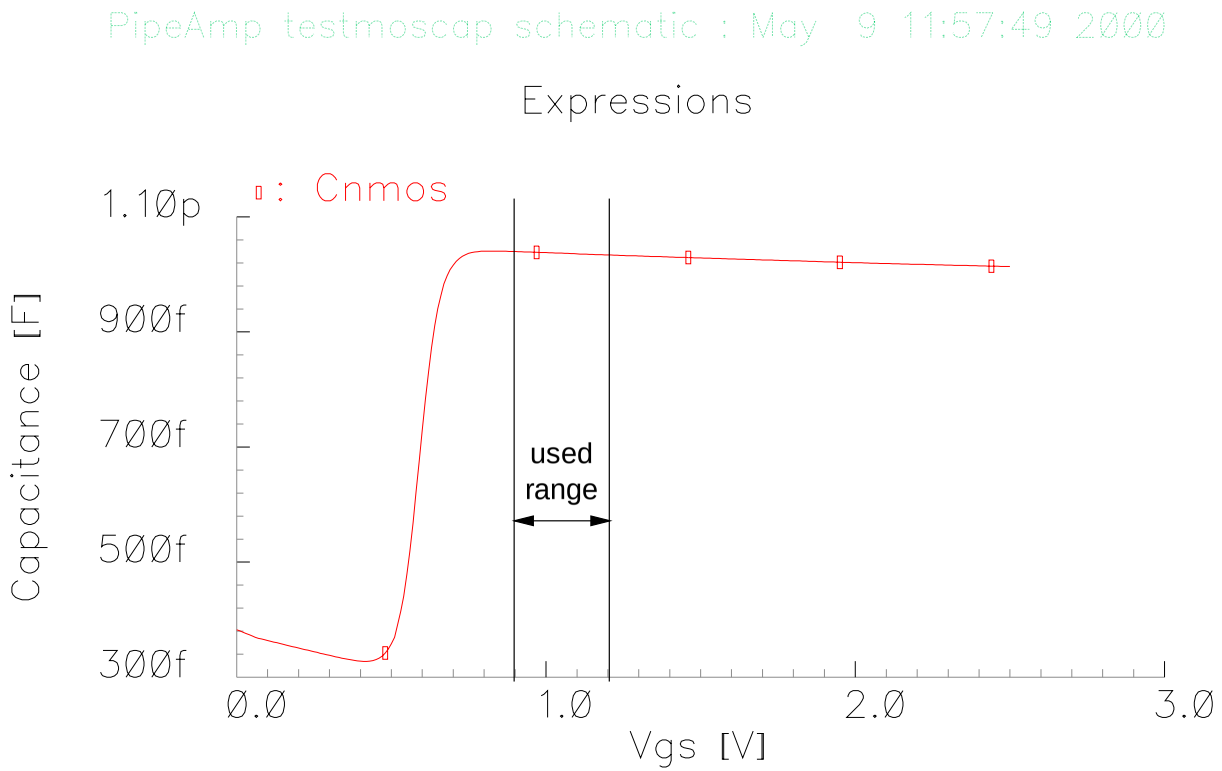
Relevant for Pileup veto and RICH binary option

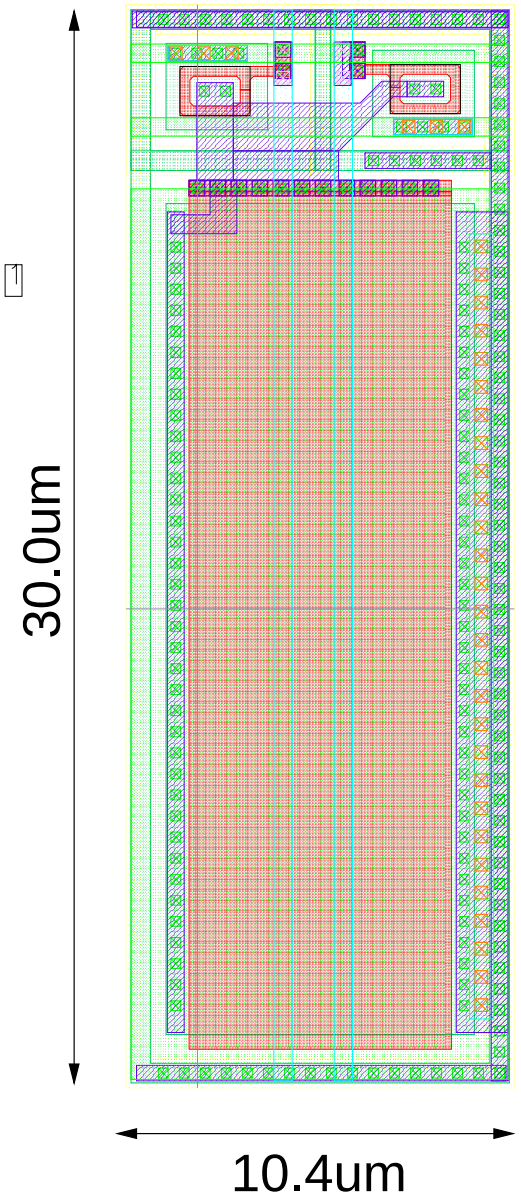
Adjustable threshold for each channel

Binary output:
- stored in pipeline instead of analog data (optional)
- imediately brought off chip via LVDS (optional)

Time constant of integrator: 5us

Analog Pipeline





- 129 x 186 n-mos gate capacitors
- capacitance 1pF
- 2 enclosed n-mos as read/write switch

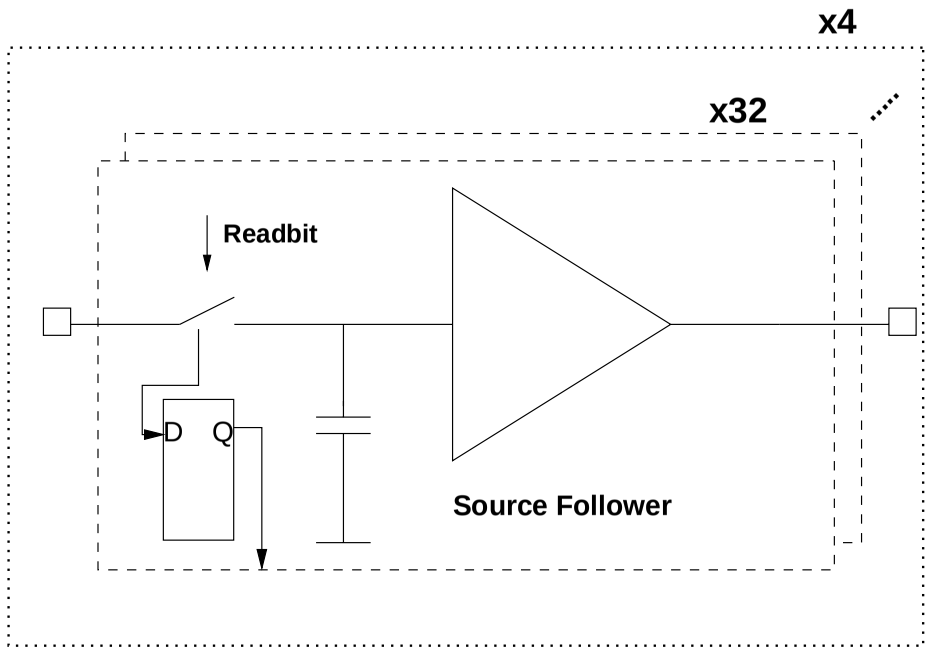
Multiplexer

- Sample / Hold stage with source follower
- different multiplexing modes by switching of "Readbit"

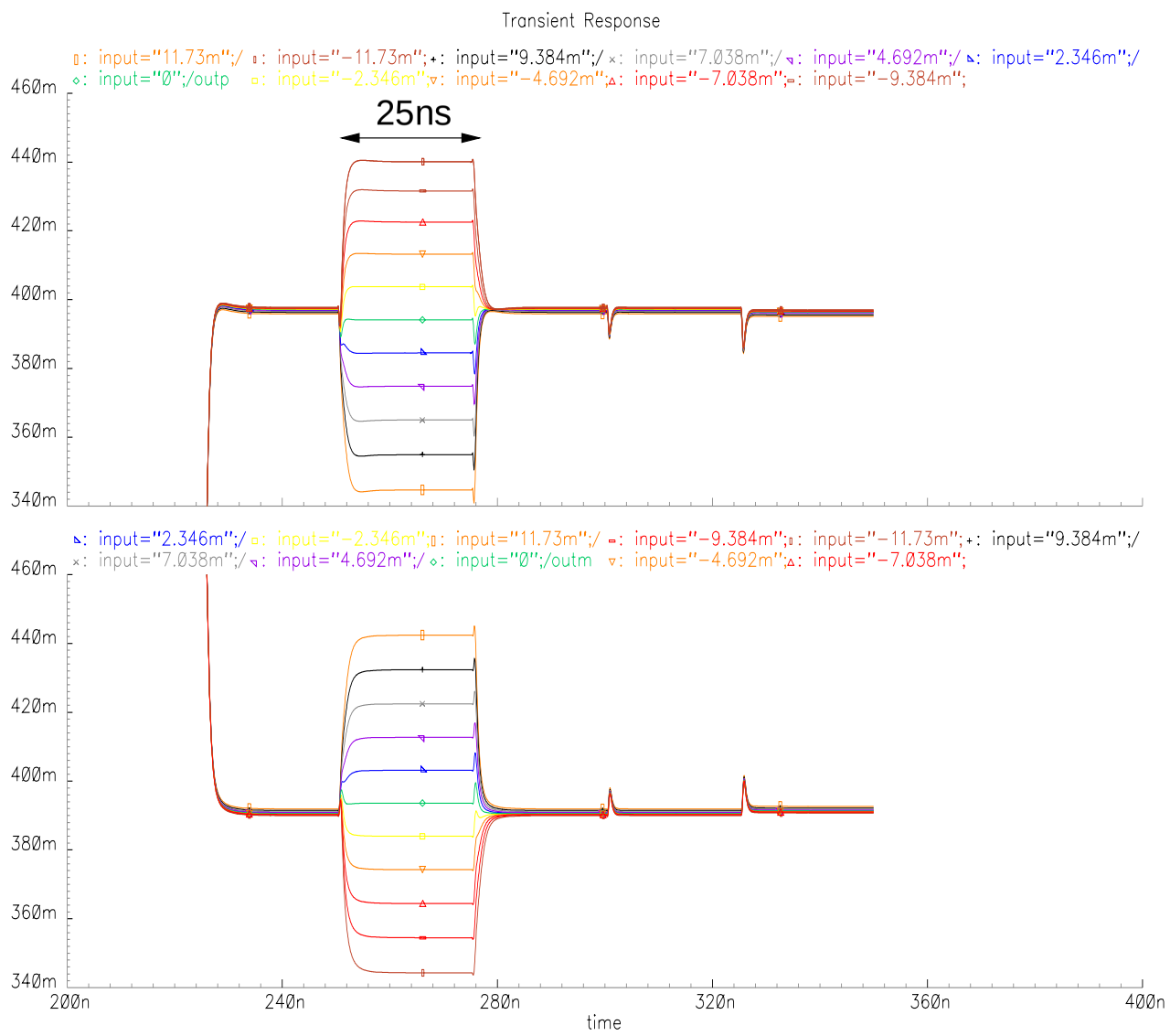
1.) 4 output pads (LHCb-mode):
32 channels to 1 output pad
for analog readout at 40MHz
=> 900ns readout time per event

2.) 2 output pads (LHCb-RICH):
64 channels to 1 output pad
for binary readout at 80MHz
=> 900ns readout time per event

3.) 1 output pad (economy-mode):
128 channels to 1 output pad
for analog readout at 40MHz
=> slow readout for test setups



Simulation of the complete analog chain



total gain of the analog readout chain:

90uA / 11.000e⁻

Digital Part

- functional description in Verilog
- synthesis with Synopsys

Slow Control

- standard I2C-Interface (ported from CIPix 1.1)
- assignment of chip address in a self-programming procedure on powerup
- different internal resets possible (controlled by length of external reset)
- 38 registers (read/write/powerup-resetted)

Fast Control (Pipeline and Readout Control logic)

- control logic ported from HELIX128-3.1 readout chip

Future plans for Beetle 1.0

- first measurements will be done at the ASIC-Lab in Heidelberg
  - assure basic functionality
  - assert fast random trigger and readout the Beetle to look for hiccups

    need ODE in Heidelberg
- detailed characterization of the chip
- detector specific measurements

  beta-tester?
- irradiation tests with Beetle 1.0

  Co60 source (20kRad/h) at FZ Karlsruhe is available

  other options are needed

  also a particle beam for SEU measurements

Submission of Beetle 1.1

Submission planned for end 2000 / start 2001

Additional features:

- JTAG protocol to enable boundary scan
- parity check of all registers to enable SEU detection
- modification of output current buffer
- mask register for testpulse and comparator

Nearer future: detailed specification meeting