Performance of the Beetle Readout Chip for LHCb

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The Beetle1.3 Chip Version

Chip Architecture

The *Beetle* ASIC is a 128 channel pipelined readout chip which will be used in the silicon vertex detector and the silicon tracker of the LHCb experiment at the future LHC collider. It is also an option for the ring imaging Cherenkov counters in case of multi-anode photomultiplier readout.

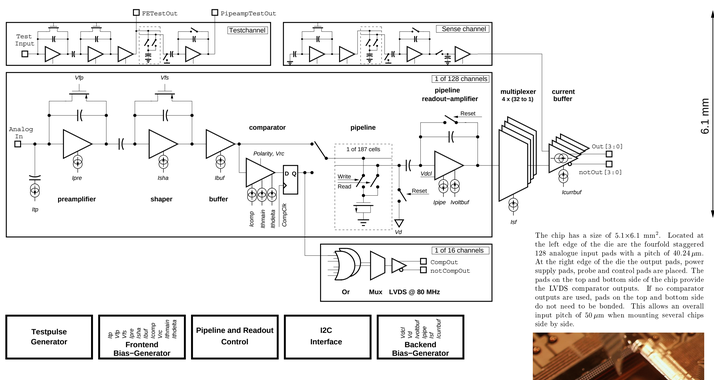
The chip can be operated as an analogue or alternatively as a binary pipelined readout chip and provides in addition prompt binary information of the front-end pulse discrimination. It implements the basic RD20 front-end electronics architecture [1, 2, 3]. Each channel consists of a low-noise charge-sensitive preamplifier, an active CR-RC pulse shaper and a buffer. They form the analogue front-end.

A comparator discriminates the front-end's output pulse. The threshold is adjustable per channel with a resolution of 5 bits and input signals of both polarities can be processed. Four adjacent comparator channels are grouped by a logic OR, latched, multiplexed by a factor of 2 and routed off the chip via low voltage differential signalling (LVDS) ports at 80 MHz.

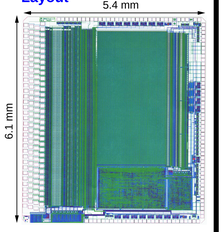
The memory for intermediate storage (pipeline) is realized as a switched-capacitor array of 130 × 187 cells, using the gate oxide capacitance of a transistor. Either the shaper- or the comparator output is sampled with the LHC bunch-crossing frequency at 40 MHz into the pipeline. The memory provides a programmable latency of maximum 160 clock periods (4 µs at 40 MHz sampling frequency) and integrates a derandomising trigger buffer of 16 stages which enables the readout of 16 consecutive events without dead time.

A resetable charge-sensitive amplifier (pipeamp) retrieves the stored signal from the pipeline and transfers it to an (analogue) multiplexer for serialisation. The multiplexer can operate in three different modes carrying the 128 channels on either 1, 2 or 4 output ports. Within a readout time of minimum 900 ns, differential current drivers bring the serialised data off chip. The output of a sense channel is subtracted from the analogue data to compensate common mode effects.

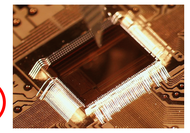
All amplifier stages are biased by forced currents. On-chip digital-to-analog converters (DACs) with 8 bit resolution generate the bias currents and voltages. For test and calibration purposes a charge injector with adjustable pulse height is implemented on each channel. The bias settings and various other parameters like the trigger latency can be controlled via a standard I^2C-interface [4]. All digital control and data signals, except those for the I^2C-ports, are routed via LVDS ports.



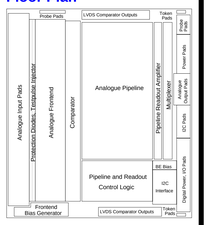
Layout



The chip has a size of 5.1×6.1 mm^2. Located at the left edge of the die are the fourfold staggered 128 analogue input pads with a pitch of 40.24 µm. At the right edge of the die the output pads, power supply pads, probe and control pads are placed. The pads on the top and bottom side of the chip provide the LVDS comparator outputs. If no comparator outputs are used, pads on the top and bottom side do not need to be bonded. This allows an overall input pitch of 50 µm when mounting several chips side by side.



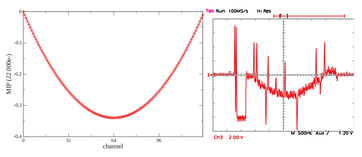
Floor Plan

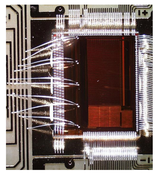


Beetle1.3: Front−End

The schematic of the front-end implemented on Beetle 1.2 was not changed, since it fulfills all requirements and exhibited the performance expected from simulation and earlier test chips. However, some changes were applied to its layout and peripheral circuits:

- Test pulse circuit: The original 4-level (staircase) pattern was abandoned in favour of a single level pattern with alternating polarity. The idea is to simplify chip testing and gain checks on single channels, since no corrections for the test pulse amplitude have to be applied.
- Power Routing: On Beetle 1.2MA0 a slight improvement of the readout figure, regarding its bent shape, was observed. This improvement resulted from changes of the power supply lines in the pipeline readout amplifier. Triggered by this observation, the power routing of the front-end was also investigated. One Beetle 1.2 was patched such, that wires could be bonded to the front-end power supply as shown in the figure beside. Interestingly the voltage drop measured across the 128 channels closely resembled the bent shape of the readout baseline. In turn a simulation of all 128 front-end channels, connected by resistive power nets was done. Adding resistors representing the connections to the power pads led to the results shown in the figure below. This simulation also confirmed, that the power supply of the shaper's folded cascode was the sole source of the baseline sag: The DC-offset of the preamplifier is removed by the AC-coupling to the shaper, while the buffer stage is a source follower, which is greatly independent from the power supply voltage. In consequence, the power bars connecting the 128 channels were widened and additional pads for both power nets were placed on bottom and top of the chip. Along with this measures, blocking capacitors were placed between the power nets for reasons described later.
- Bias networks: The investigations on the front-end's power supply also revealed a minor design flaw in the biasing of the front-end. While the DAC generating the bias current was located at the bottom side of the chip, the diode-connected transistor of the current mirror sinking it was located on the top side, generating a considerable voltage drop across the interconnection. In turn the gate voltages of the current sources of the different channels varied, predicting a gain drop towards the higher channel. This was experimentally confirmed in test beam data taken with a NIKHEF hybrid. On Beetle 1.3 the diode connected transistor of the current mirror was moved to the bottom side of the chip to eliminate this effect.

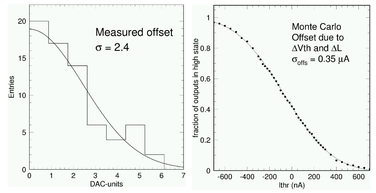


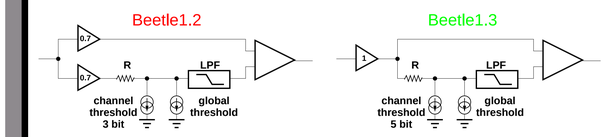


Beetle1.3: Discriminator

Measurements of the discriminator done at NIKHEF resulted in a measured threshold spread equivalent to $\sigma = 2.4$ DAC counts (or 4800e−).

This meant that the bipolar spread is of the same magnitude as the range of the unipolar 3 bit local DACs intended for its compensation. The measured spread was also found in good agreement with the spread expected from process parameter variations, which resulted in $\sigma = 2.8$ DAC counts (or 5600e$^-$). A major culprit for this spread was found to be the split input buffer of the comparator, which was in turn replaced by a single one with an increased gain (1 instead of 0.7) on Beetle 1.3. To provide a sufficient safety margin, the channel's local DACs intended for offset compensation were improved with a bipolar range of 14400e− and 5 bit resolution.





Beetle1.3: Control Core

The Beetle's control circuit was re-synthesized for Beetle 1.2, especially to include SEU protection/correction circuits. This was done by using triple redundant Flip-Flops for all registers, enhanced by self-triggered reprogramming circuits for the static ones.

Regarding the digital functionality, the control circuit of Beetle 1.2 worked as expected. But its operation affected almost all other circuits by coupling switching spikes to the chip's outputs and power lines. Suspiciously these spikes appeared on both clock edges (and were attributed as "40 MHz X-talk"), which pointed to the clock tree. The latter had grown from 21 buffers on 1.1 to 275 on 1.2 and was consequently considered as the primary source of the effect. A further increase of the crosstalk was probably due to a guard ring, which was moved from the analogue supply on 1.1 to the digital one on 1.2.

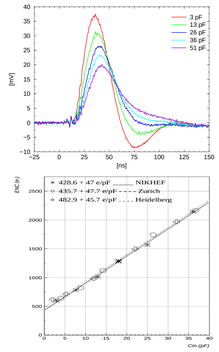
Another feature of the 1.2 core was the absence of a multiplexer at the return-token inputs used for daisy-chained readout. It required that these pads were pulled to ground, if unused. For the core of Beetle 1.3 special care was taken for the clock tree, which was reduced to 104 buffers. In addition the offending guard ring was moved back to the analogue supply and the missing multiplexers were added. Targeted on a further reduction of crosstalk, the digital power supply of the multiplexer was separated from the core supply and both were blocked with gate capacitors on chip.

Front−end

The analogue front-end is formed by a charge-sensitive preamplifier, an active CR-RC shaper and a source-follower as buffer. Preamplifier and shaper use folded-cascode amplifier cores with an NMOS input transistor ($W/L = 3744/0.42$) in case of the preamplifier and a PMOS input transistor in case of the shaper.

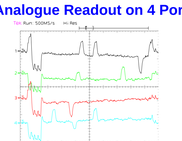
The shape of the front-end pulse can be chosen according to the specific requirements of the application. The minimum risetime (10-90[%]) is well below 25 ns, the remainder of the peak voltage after 25 ns can be adjusted to less than 30% for load capacitances ≤ 35 pF.

The equivalent noise charge (ENC) of the front-end has been measured as $\mathrm{ENC} = 497\,e^- + (48.3\,e^-/\mathrm{pF}) \cdot C_{in}$.

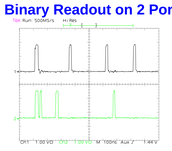


Readout Modes

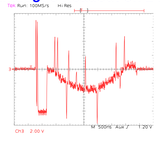
Analogue Readout on 4 Ports



Binary Readout on 2 Ports



Analogue Readout on 1 Port



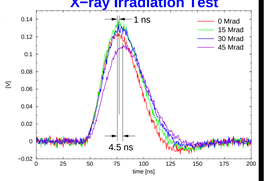
Radiation Hard VLSI Design

The requirements on the *Beetle* chip concerning radiation hardness are defined by it's use in the silicon vertex detector. The expected dose rate is 2 Mrad per year. Several measures have been taken to assure the resistance against total ionising dose (TID) as well as single event effects.

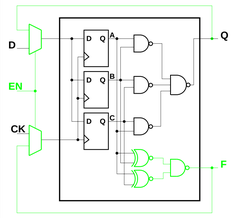
The chip is fabricated in a standard CMOS deep-submicron technology featuring a 0.25 µm lithography. The thin gate oxide of ≈ 62 Å reduces a shift in the transistor threshold voltage under irradiation. The consistent use of enclosed NMOS transistors eliminates "end-around" leakage currents. Analogue stages are biased with constant currents instead of voltages. This establishes a total ionising dose radiation hardness in excess of 10 Mrad. An X-ray irradiation test up to an accumulated dose of 45 Mrad showed only minor degradations in the analogue performance and no functional failure of the chip.

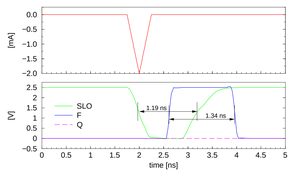
Single Event Latch-up (SEL) is suppressed due to the implementation of guard-rings. The continuous use of triple-redundant logic ensures a robustness against Single Event Upset (SEU), which is expected to occur at a rate of 1 µHz per chip in the vertex detector of LHCb. Static parts of the logic, i.e. bias and configuration registers, implement a self-correction mechanism against SEU-induced errors.

X−ray Irradiation Test



SEU Protection: Triple−Redundancy





Simulation result of a self-triggered correction process. A total charge of 500 fC has been injected as a triangular pulse to a sensitive node (SLO). The disturbance takes 1.2 ns. The clock (F) triggering the self-correction has a width of 1.34 ns. The flip-flop output Q remains unchanged all the time.

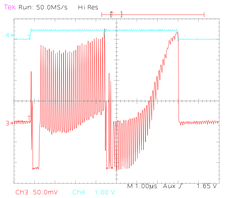
self−triggered correction

Beetle1.3: Pipeline Readout Amplifier

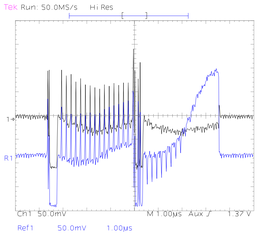
The decrease of a readout cycle to the LHCb-required 900 ns on Beetle 1.2 caused the activation of two switches at the same time. Besides some charge injection, this also lead to the back-transfer of the charge present on the multiplexer's hold capacitor to the pipeamp. As a result, a 60% remainder with opposite polarity and a strong distortion of the readout baseline in the next data frame was visible. A simulation, in which the relative timing of the two switching signals was swept is shown below. It revealed that the simultaneous timing on Beetle 1.2 was almost the worst case and delaying either signal would result in a considerable improvement. On Beetle 1.3 the `MuxTrack` signal is delayed by 5ns, which removes the sticky charge. This was also proven in advance by a patch applied to a Beetle 1.2: An external *mux track* signal was coupled to the corresponding line, overriding the internal signal.

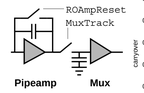
A further modification of the Beetle 1.3 Pipeamp are widened power lines, already present on Beetle 1.2MA0.

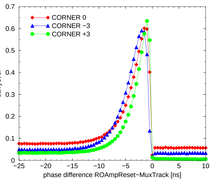
Sticky Charge Effect



Fix of Sticky Charge Effect:





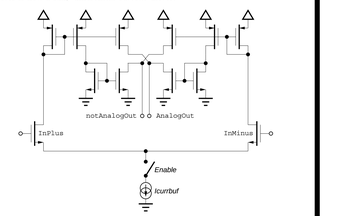


Beetle1.3: Multiplexer

Three changes were applied to the multiplexer of Beetle 1.3: The number of reference channels used for DC level subtraction was increased to 4 – one for each block of 32 channels. This modification is intended to remove spikes at the start and end of a data frame, originating from block to block crosstalk via the reference channel. Also the balance of the switch operation was improved, again targeting on the suppression of spikes. The biggest modification was in the digital part: It received its own power supply and the triple redundant Flip-Flops were removed. This was motivated by the lower switching noise, which was considered more important than SEU robustness in this part. In this place it should be denoted, that an SEU can at maximum corrupt 2 data frames by injecting an additional token, since the multiplexer token is discarded after leaving the last channel.

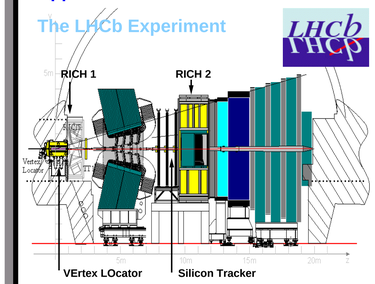
Beetle1.3: Output Driver

The output driver underwent a major redesign, primarily driven by an excessive current density in some part of the circuit. In case of an increased power supply voltage, the latter also caused a failure of the circuit. On Beetle 1.3 the output driver is now a fully differential *current* driver.



Applications

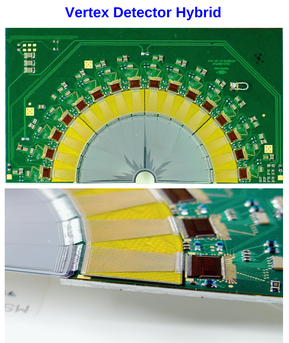
The LHCb Experiment



LHCb is a next-generation experiment to study B-physics in pp-collisions at LHC. It is a precision measurement experiment for $\mathcal{CP}$-violation and rare decays in the B-meson system, being able to perform redundant measurements of all angles in the unitarity triangle and to test the Standard Model of electroweak interaction with unprecedeondated precision.

The *LHCb*-experiment plans to operated at a pp centre-of-mass energy of 14 TeV and a bunch crossing frequency of 40 MHz with an average luminosity of $\mathcal{L} = 2 \times 10^{32}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$. The $b\bar{b}$-production cross section $\sigma_{b\bar{b}}$ is ≈ 500 µb, which is far larger than at any existing machines. From the total inelastic cross section $\sigma_{tot} = 100$ mb the ratio of events with b quarks is 5×10^{-2}. Hence, at *LHCb* 100,000 B-mesons/s are produced at an interaction rate of 40 MHz. They are hidden in 200 times more non-B events.

Vertex Detector Hybrid



Vertex Detector

The silicon sensors of the vertex detector use n-strips on n-bulk material with AC coupling to the electronics and polysilicon biasing. Due to radiation damage it is expected, that they have to be replaced every 3 years. The sensors have a half-disc shape with azimuthal (r-measuring) or radial (φ-measuring) strips. This layout has been chosen to optimise the speed of the pattern recognition in the L1 trigger. The number of strips per half-disc is 2,048 with varying length to restrict the occupancy below 1% everywhere.

Silicon Tracker

The Silicon Tracker uses rectangular sensors with p-strips on an n-bulk. In order to minimise the number of readout channels, a large strip pitch of ∼ 200 µm together with long readout strips of 22 cm has been chosen. A ladder is formed by two silicon sensors, which are read out by 3 *Beetle* chips. For one station of the tracking system, even ladders consisting of 3 silicon sensors with a total strip length of 33 cm are being constructed.

Silicon Tracker Ladders (Testbeam Setup)

Beetle1.2 Readout Chips

Silicon Tracker Hybrid

References

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[4] The I^2-bus and how to use it, Philips Semiconductors, 1995