Performance and Future Development of the Beetle Chip

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Beetle: Outline

What is *"Beetle"*?

- 128 channels analogue/binary pipelined readout chip
- additional immediate binary readout for trigger applications
- manufactured in commercial 0.25 μm CMOS technology

Where in LHCb will it be used?

- Silicon Vertex Detector (VELO)
- Pile-up Veto Counters
- Inner Tracker
- RICH (if MAPMTs are used)

Beetle 1.1:

- Architecture
- Layout
- Test Results

BeetleFE 1.1, BeetleFE 1.2:

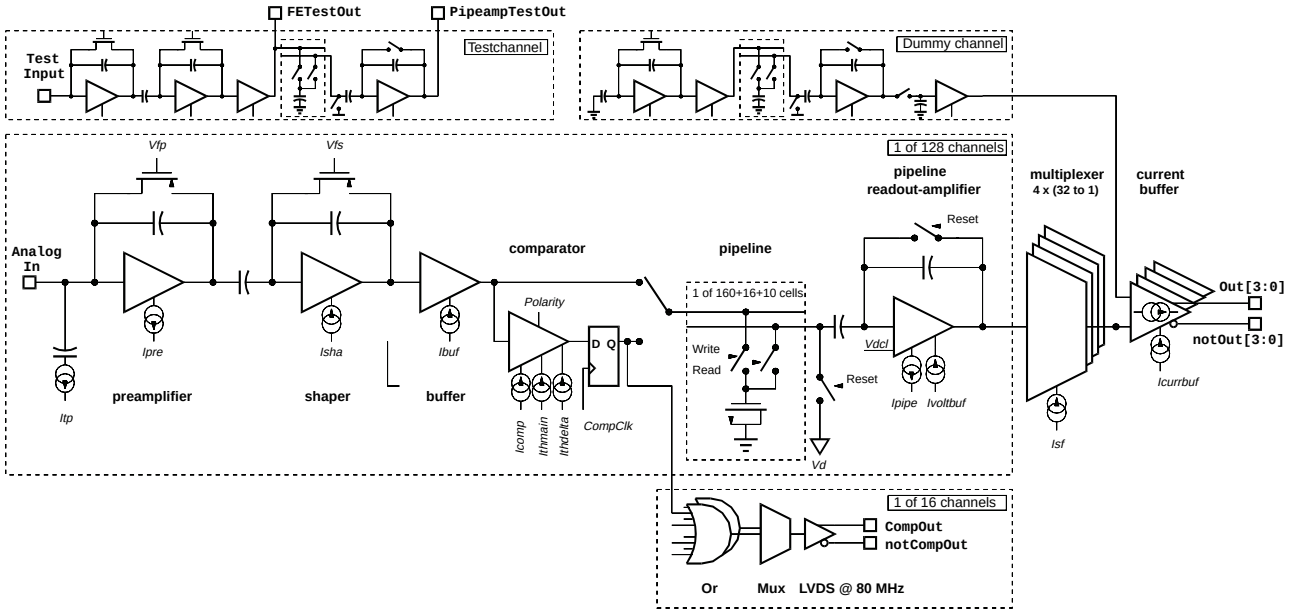
- Schematics and Layout
- Expected Improvements

BeetleSR 1.0:

- Schematics
- planned Measurements

Outlook

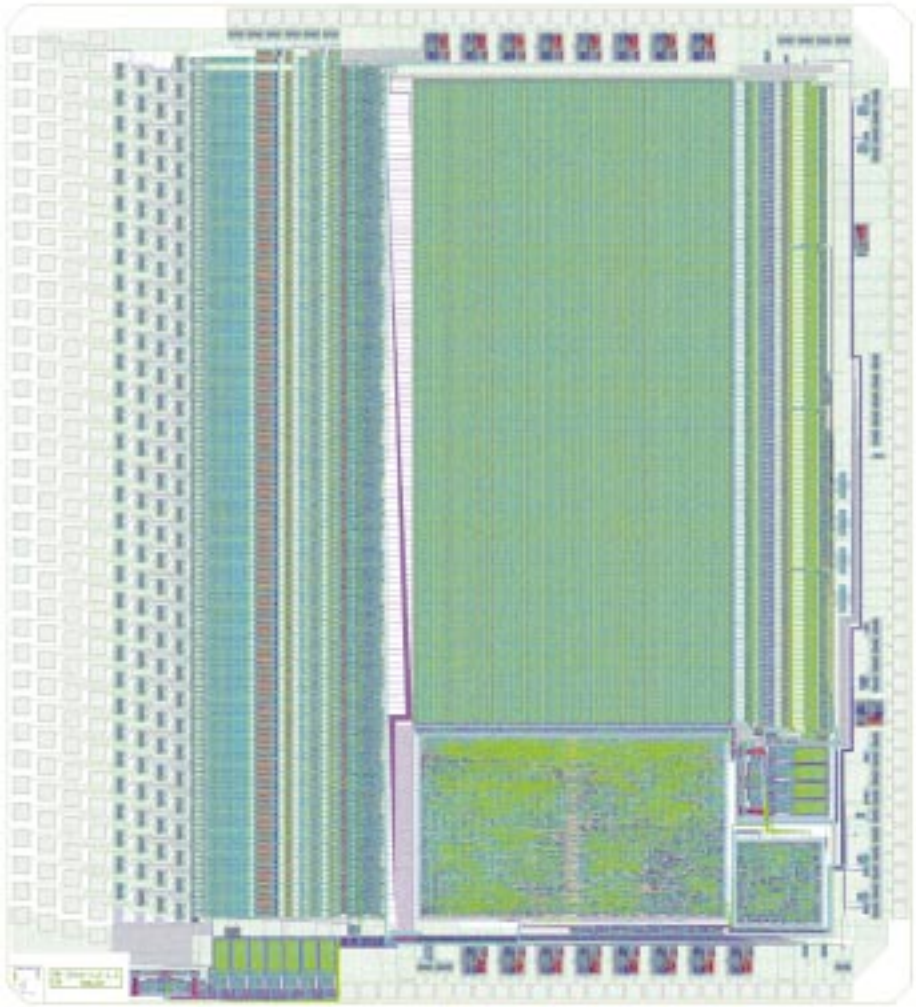
Beetle: Architecture

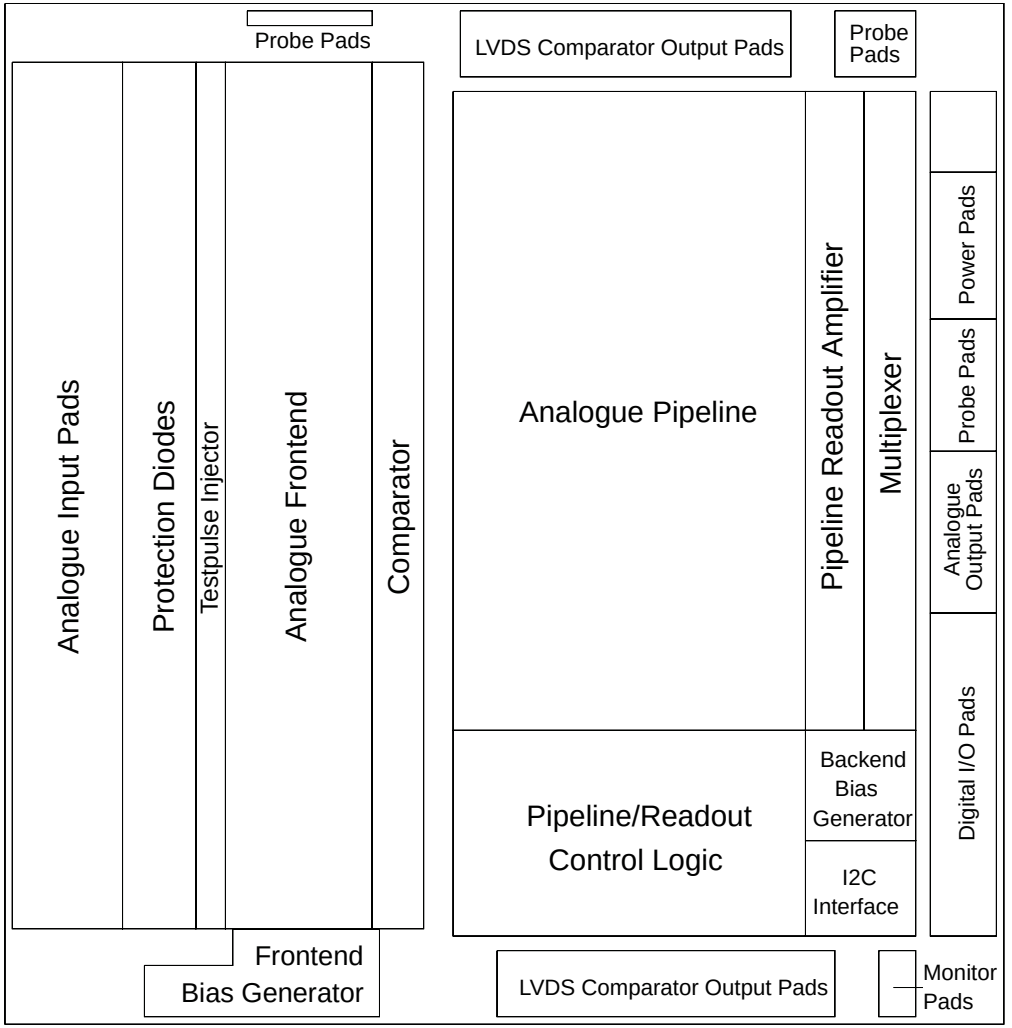


Features:

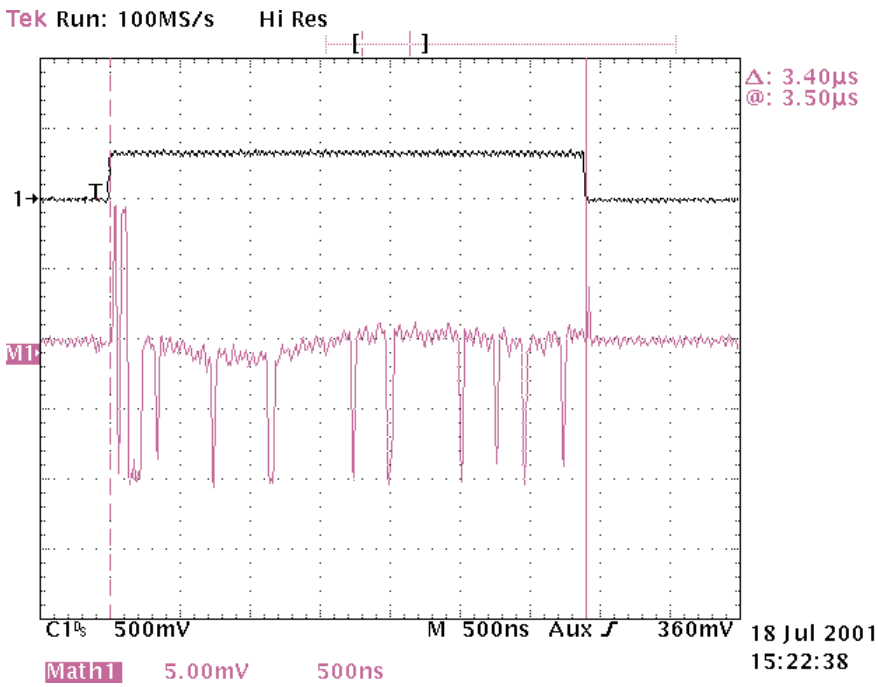
- 128 input channels
- CSA/Shaper with 25ns peaking time
- 40 MHz sampling (LHC clock)
- 128 discriminators with switchable polarity
- analogue memory for 160 sampling steps
- buffer for 16 triggered events
- ➔ 4 µs max. latency
- ➔ 900ns/event readout speed
- internal DACs for bias settings
- test pulse injector with adjustable amplitude
- setup/slow control via I^2C interface

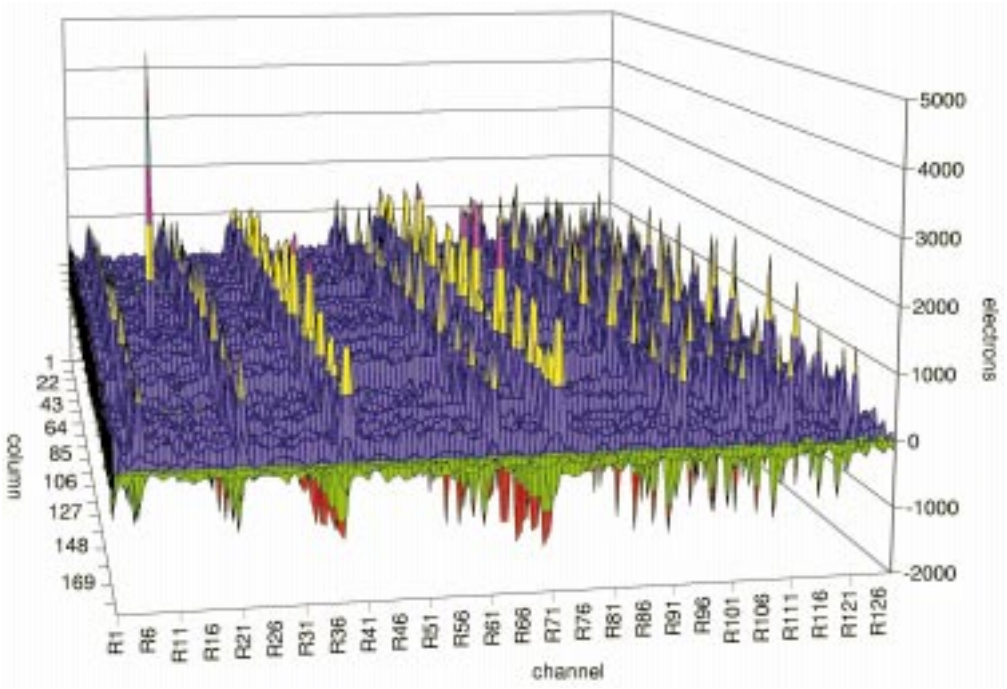
Beetle: Layout and Floorplan





Beetle: Analog Readout

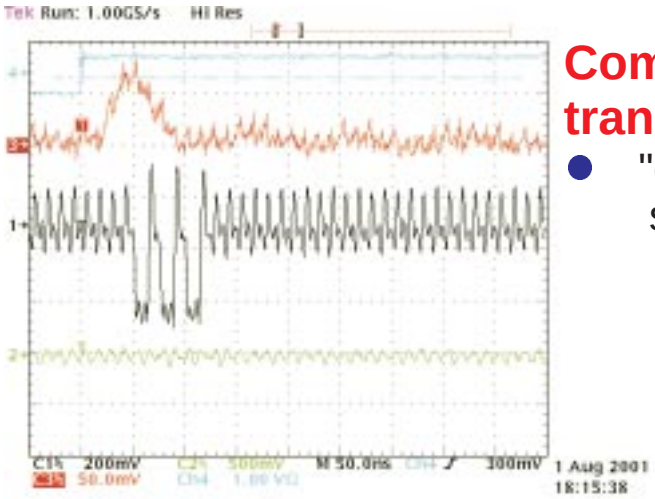




Analogue Readout shows the expected behaviour:

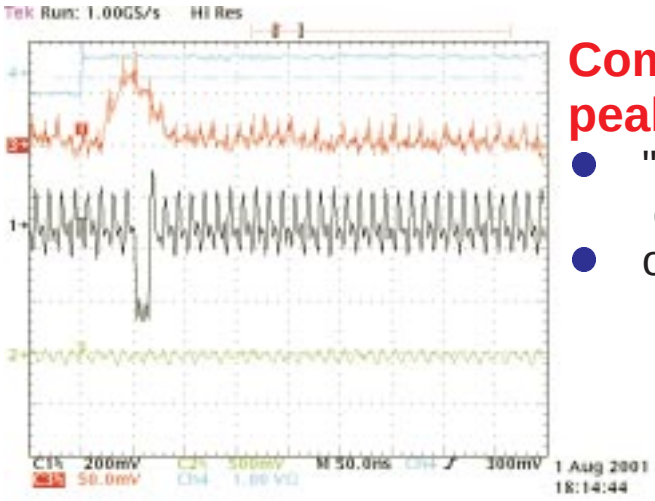
- flat baseline
- correct levels of encoded pipeline address
- expected gain
- pipeline homogenity better than 1000e$^-$

Beetle: Binary Readout



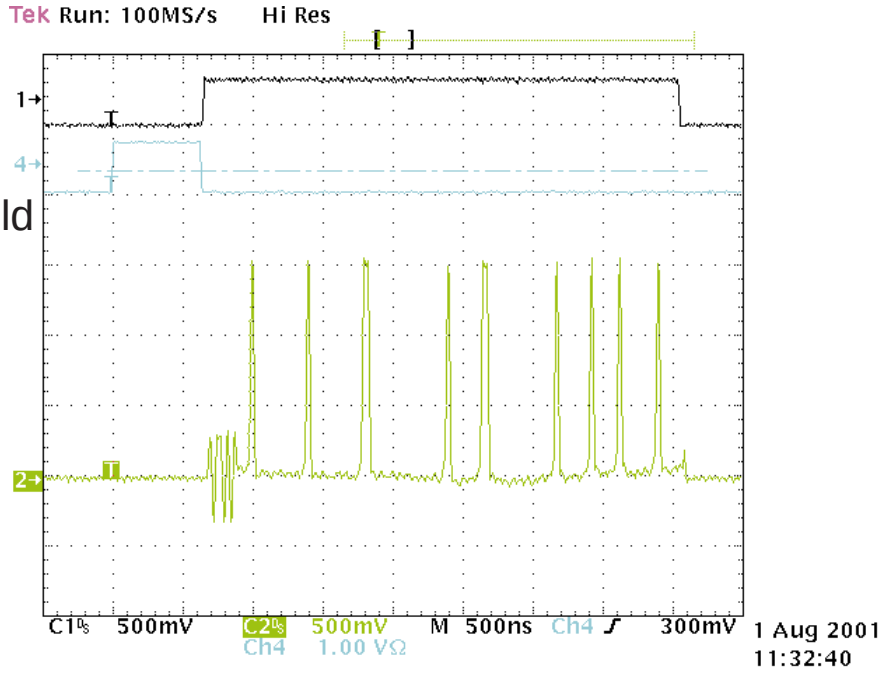
Comparator in transient mode:

- "on" as long as signal is over threshold



Comparator in peak mode:

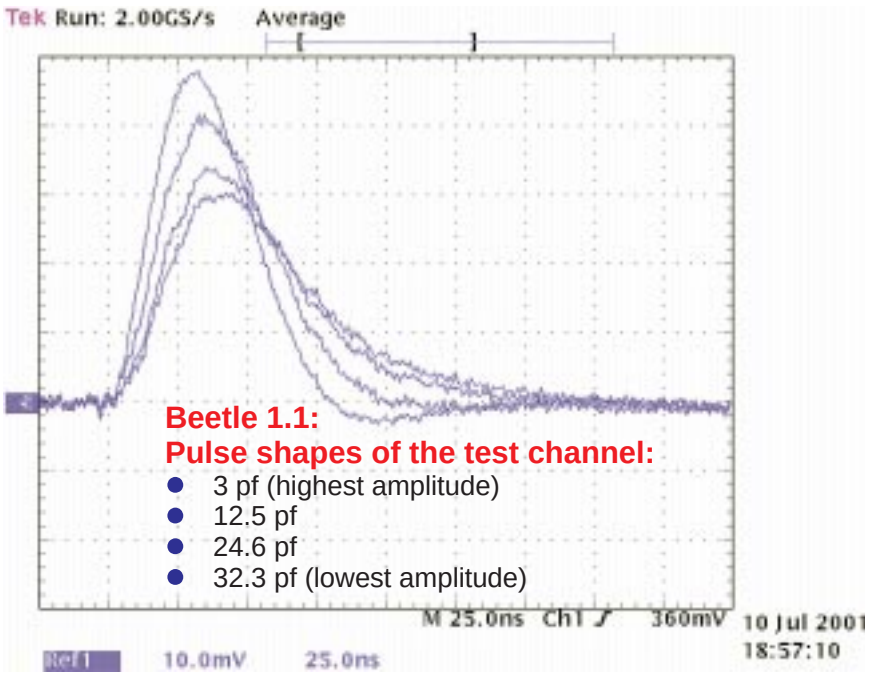
- "on" only for one one bunch crossing
- one BX dead time to rearm comparator



Binary readout mode:

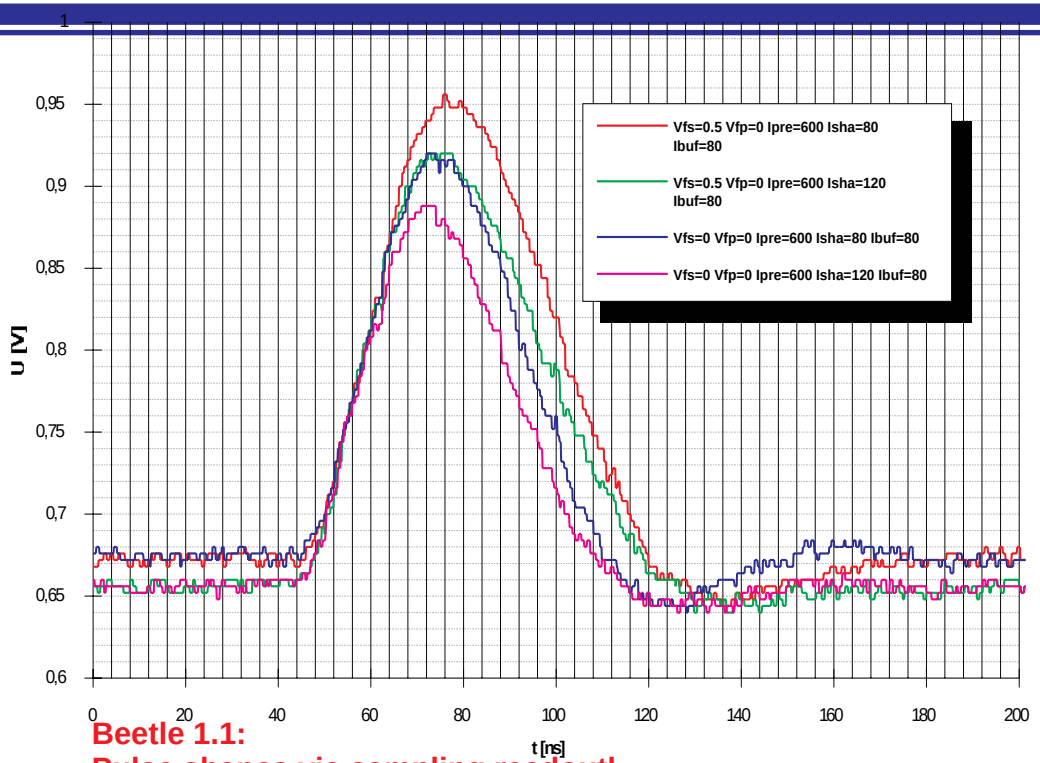
- "on"-level =120000 e^- as designed (PC# = 24000e^-)
- flat baseline

Beetle: Pulse Shape and Charge Rate



Beetle 1.1:
Pulse shapes of the test channel:

- 3 pf (highest amplitude)
- 12.5 pf
- 24.6 pf
- 32.3 pf (lowest amplitude)



Beetle 1.1:
Pulse shapes via sampling readoutl:

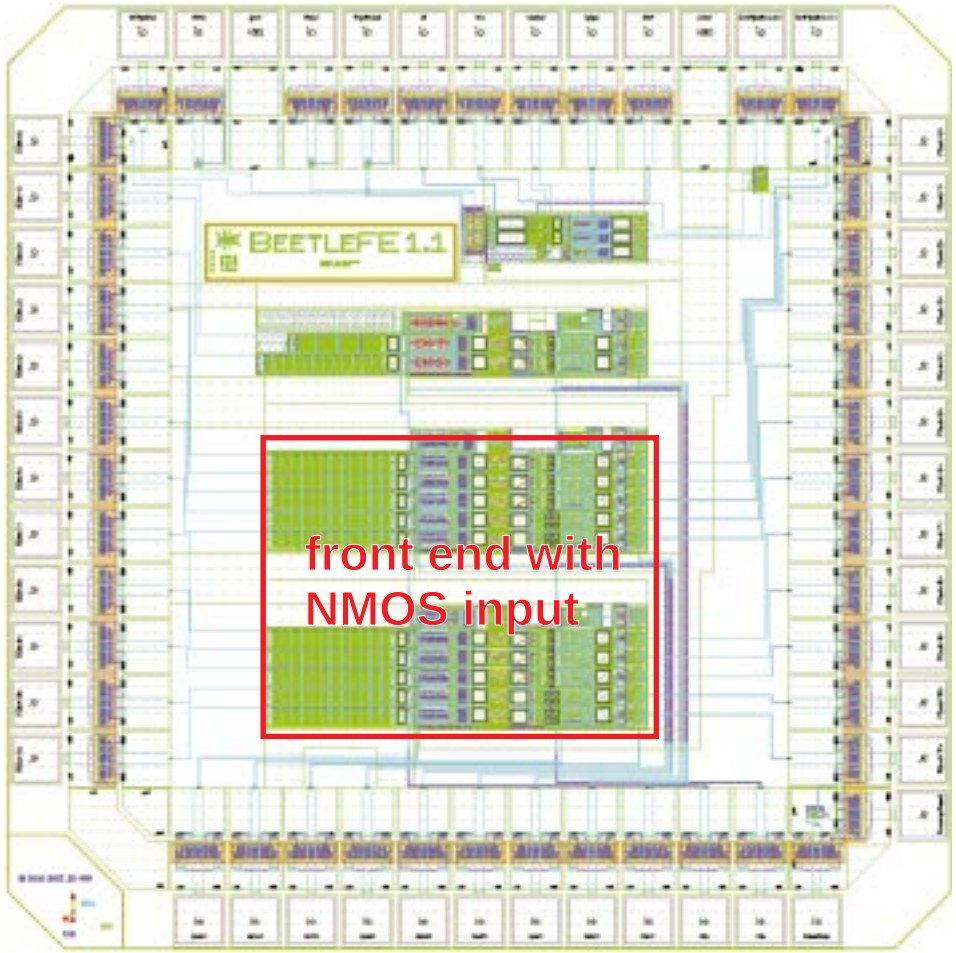
- good agreement with test channel

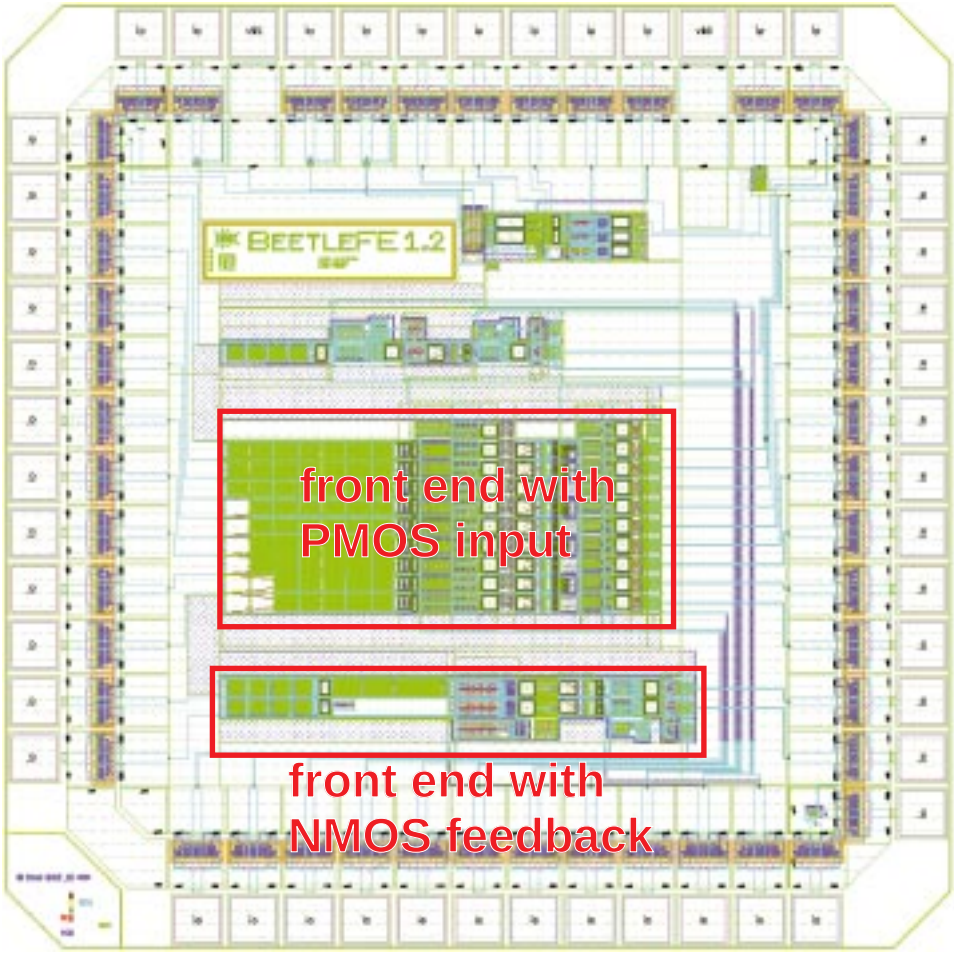
Analogue Characteristics:

- peaking time of $t_{peak} \approx 27$ ns and
- remainder in next BX of $t_r \approx 30\%$ in good agreement with simulation
- problems to keep up with LHC*b* specifications at higher C_p
- higher C_p expected especially for Inner Tracker
- input charge rate limited to 2 nA (≈ 0.32% strip occupancy) due to feedback transistor

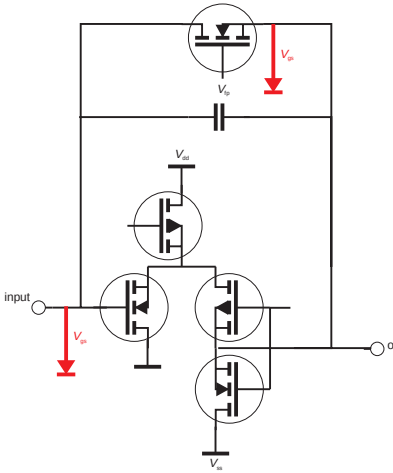
➔ development of new front ends

BeetleFE 1.1 & 1.2: Layout





BeetleFE 1.1 & 1.2: Schematics



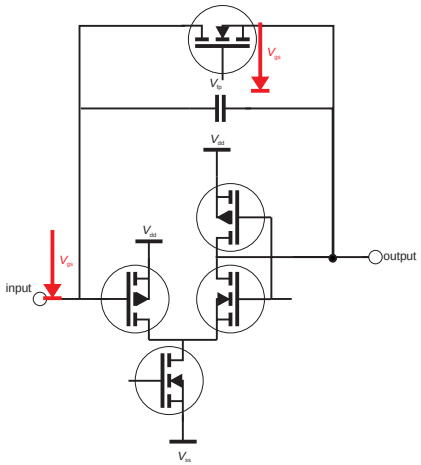
NMOS input,
PMOS feedback:

- high g_m/area of input transistor
- feedback control voltage limited by power supply rail

Beetle 1.0 and 1.1,
BeetleFE 1.0 and 1.1

Designed for 25 ns peaking time @ 40 pF:

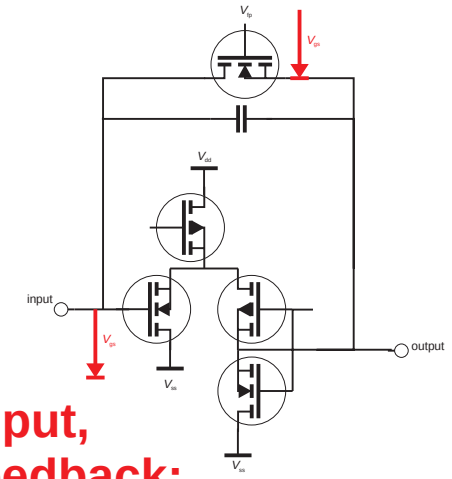
- reduced impedance of the load branch



PMOS input,
PMOS feedback:

- no limitations for feedback transistor design
- low g_m/area of input transistor

BeetleFE 1.0 and 1.2



NMOS input,
NMOS feedback:

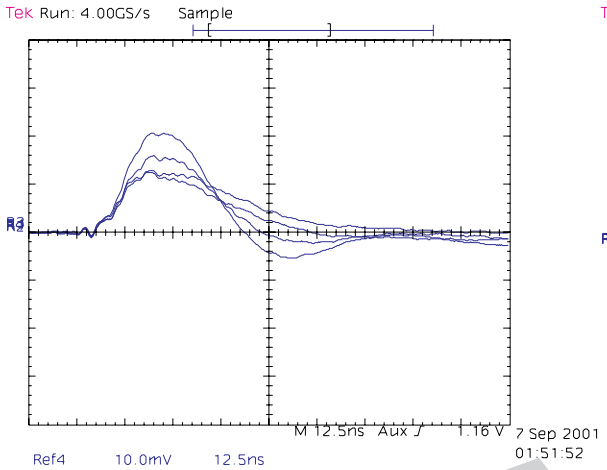
- high g_m/area of input transistor
- large parasitics resulting from huge number of enclosed feedback transistors

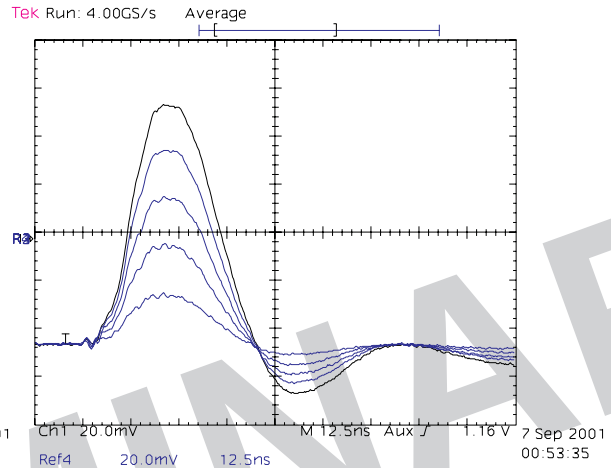
BeetleFE 1.2

BeetleFE 1.1 & 1.2: Comparison

Set	input transistor	W	L	feedback	shaper feedback
2a..c	NMOS rectangular	3744 um	0.42 um	PMOS	48.8 fF
2d..e	NMOS rectangular	3744 um	0.42 um	PMOS	20.5 fF
5a	PMOS waffle	8310 um	0.28 um	PMOS	15 fF
5b	PMOS waffle	8310 um	0.28 um	PMOS	18.75 fF
5c	PMOS waffle	8310 um	0.28 um	PMOS	37.5 fF
5d	PMOS waffle	7123 um	0.28 um	PMOS	18.75 fF
5e	PMOS waffle	7123 um	0.28 um	PMOS	37.5 fF
5f	PMOS rectangular	5852 um	0.28 um	PMOS	18.75 fF
5g	PMOS rectangular	5852 um	0.28 um	PMOS	37.5 fF
5h	PMOS waffle	5936 um	0.28 um	PMOS	18.75 fF
5i	PMOS waffle	5936 um	0.28 um	PMOS	37.5 fF
6a	NMOS rectangular	3744 um	0.42 um	NMOS	48.8 fF

BeetleFE 1.1: First Results





Different front end channels:

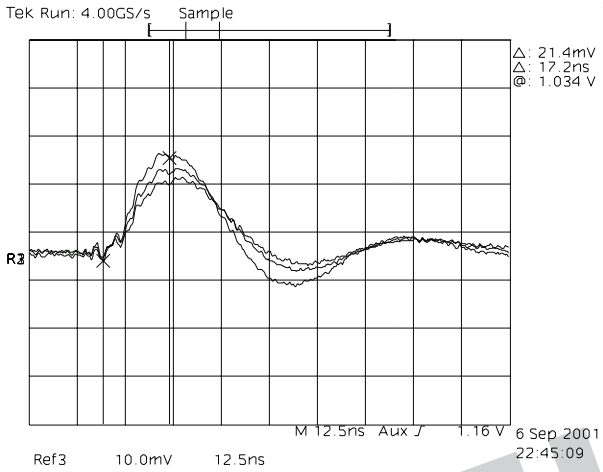
- different preamp feedback transistor
- different shaper feedback capacitances

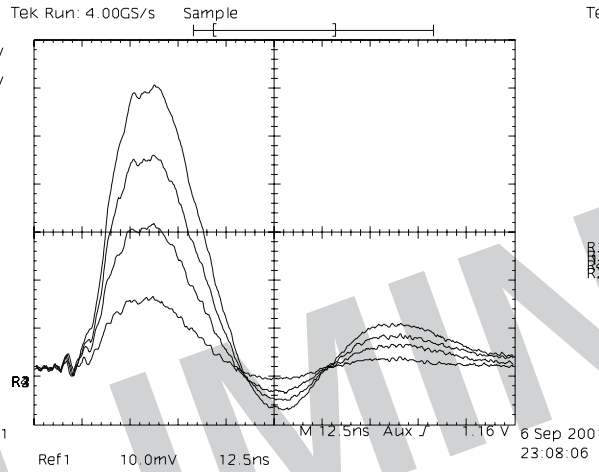
Different input charges:

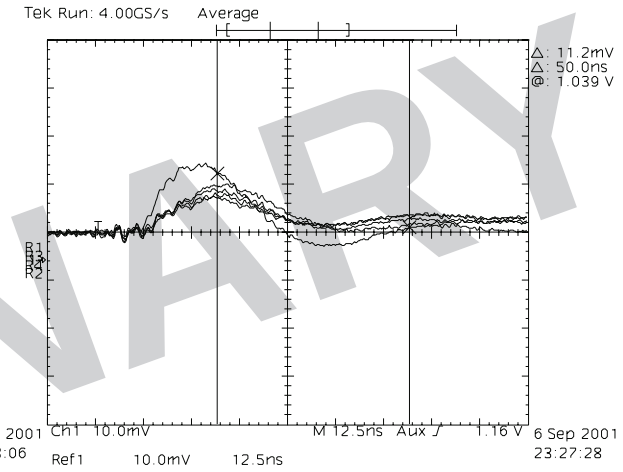
- 55000e^- (top)
- 44000e^-
- 33000e^-
- 22000e^-
- 11000e^- (bottom)

➔ peaking time below 25 ns
➔ maximum charge rate to be tested

BeetleFE 1.2: First Results







Different front end channels:

- different W of input transistor
- different shaper feedback capacitances

Different input charges:

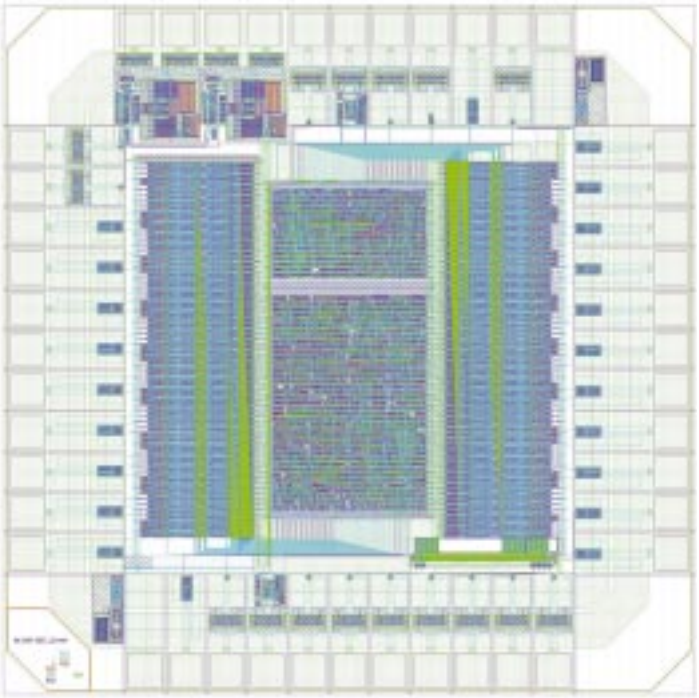
- 44000e$^-$ (top)
- 33000e$^-$
- 22000e$^-$
- 11000e$^-$ (bottom)

Different load capacitances:

- 3 pF
- 10 pF
- 20 pF
- 30 pF
- 40 pF

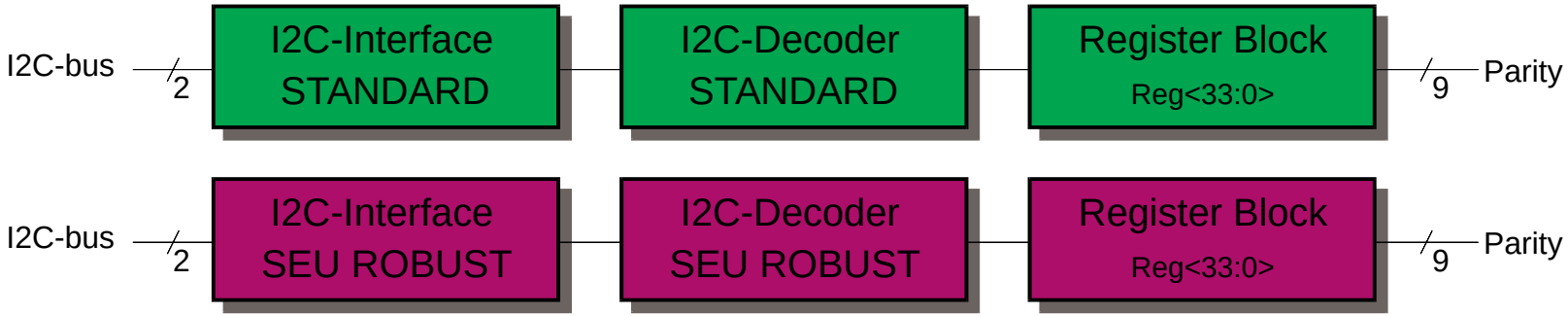
➔ peaking time below 25 ns
➔ maximum charge rate not an issue by design

BeetleSR 1.0: Overview



BeetleSR 1.0 consists of:

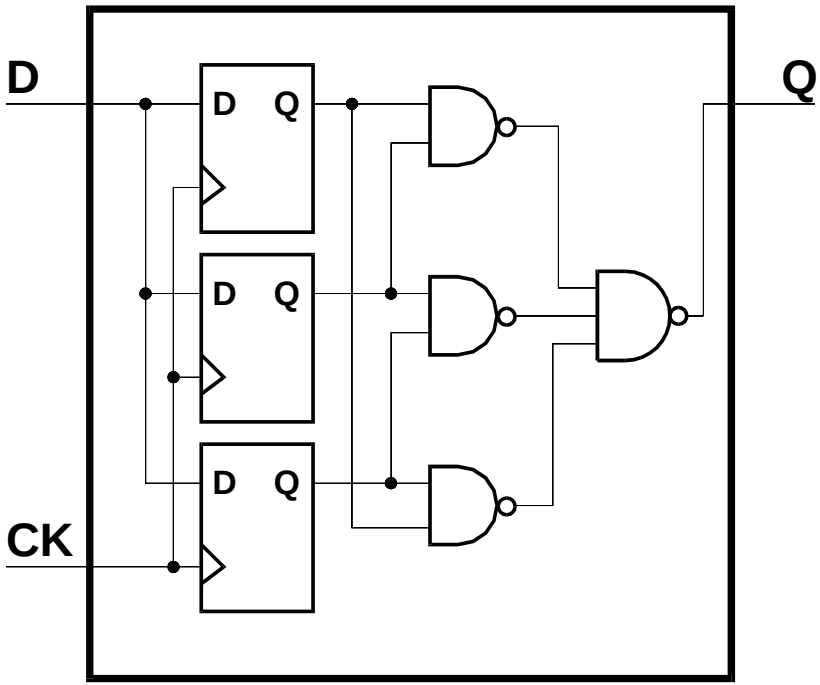
- standard I^2C-interface and decoder
- SEU hardened I^2C-interface and decoder
- 2 blocks of 34 registers
- 2×9 pads indicating the parity of 32 register bits each



BeetleSR: Principle & Planned Tests

Principle of SEU-hardened logic on BeetleSR 1.0:

- triple redundant flipflops
- majority decoder



Measurements with BeetleSR 1.0:

- SEU rate vs. Flux from register banks
- SEU supression factor from triple redundant logic

SEU-hardened logic on future Beetle chips:

- triple-redundant registers in switching parts of the circuit (e.g. state machines)
- ECC with hamming codes for static circuits (e.g. configuration registers)

Beetle: Future Plans and Outlook

Beetle 1.1:

- system test with detectors is under preparation
- test for 10 Mrad radiation hardness planned for October
- test beam planned for October

Beetle 1.2:

- Tape-Out scheduled for April 2001

Beetle 1.2 will include:

- one of the front ends from BeetleFE 1.1 or 1.2
- SEU robust logic circuits with
  - triple-redundant flipflops in state machines etc.
  - ECC for static registers
- differential output driver with bipolar current
- minor improvements on discriminators