Enhanced Radiation Hardness and Faster Front Ends for the Beetle Readout Chip

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Abstract

This paper summarizes the recent progress in the development of the 128 channel pipelined readout chip *Beetle*, which is intended for the silicon vertex detector, the inner tracker, the pile-up veto trigger and the RICH detectors[1] of LHC*b*.

Deficiencies found in the front end of the *Beetle* Version *1.0* and *1.1* chips resulted in the submissions of *BeetleFE 1.1* and *BeetleFE 1.2*, while *BeetleSR 1.0* implements test circuits to provide future *Beetle* chips with logic circuits hardened against single event upset (SEU).

Section I. motivates the development of new front ends for the *Beetle* chip, and section II. summarizes their concepts and construction. Section III. reports preliminary results from the *BeetleFE 1.1* and *BeetleFE 1.2* chips, while section IV. describes the *BeetleSR 1.0* chip. An outlook on future test and development of the *Beetle* chip is given in section V.

I. Introduction

The development of the *Beetle* readout chip started in late 1998. It implements the basic RD20 architecture [4], augmented with a prompt binary readout path like it was implemented on the HELIX128 chip [5] and a pipelined binary operation mode. Besides several (2×2) mm^2 chips with test structures and components, two complete readout chips (*Beetle1.0* and *Beetle1.1*) have been manufactured in commercial 0.25 µm CMOS technology. A detailed description of these chips, their architecture and performance can be found in [1] [2] [3].

Beetle1.0, the first complete pipelined readout chip had to be patched with a focused ion beam to become functional. In turn the second one, *Beetle1.1* included all fixes to correct the errors found on its predecessor. However, a few problems still remained:

- Peaking time of the front end $t_{\mathrm{peak}}(0\ldots100\%) \geq 27$ ns,
- Decay time of the pulse has a remainder above 30% after 25 ns, too long for the operation of the LHC*b* vertex detector,
- Maximum input current of ≈ 2 nA, too small for the expected occupancies at LHC*b*
- Digital circuits not robust against SEU.

To overcome these problems, which are primarily related to the actual requirements of LHC*b*, test chips implementing the necessary circuits were submitted. This allows the test of the circuit's functionality prior to its implementation on a complete readout chip. Furthermore different approaches to solve the same problem can be evaluated to find the optimum solution.

II. New front ends

The front end implemented on *Beetle1.1* was developed with an early version of the 0.25 µm CMOS design kit in 1998 and submitted on the first test chip *BeetleFE 1.0*. It consists of a charge sensitive preamplifier, a $CR-RC$ pulse shaper and a buffer. The first two stages use *folded cascode* amplifier cores, while the buffer is a source follower. Measurements of its characteristics showed that it was considerably slower than

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[1] in case of multianode photomultiplier tube readout

expected from simulation. This discrepancy, however, diminished with the evolution of the design kit and nearly vanished with the last version. A further impetus to develop a faster front end arose from the increasing detector capacitances. While values around 10 pF were assumed for the strip capacitance of the LHC*b* vertex detector during the development of the *BeetleFE 1.0*, the current designs predict capacitances of up to 35 pF for the inner tracker detectors of LHC*b*. Fig. 1 shows the pulse shape of the *Beetle1.1* front end for different input capacitances.

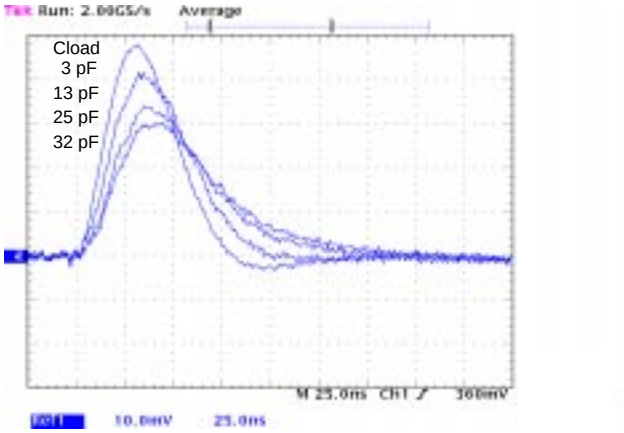

Figure 1: Pulse Shapes of the *Beetle1.1*'s test channel at indicated capacitances.

To decrease the peaking time and fall time of the shaped signal, the following provisions have been taken:

- Decreased resistance of the preamplifier's *folded cascode* load branch to decrease the peaking time of the pulse. This also required an increase of the input transistor's transconductance g_m in order to maintain the same open loop gain A_0.
- Decreased integration time constant τ_{sha} of the shaper in order to decrease the fall time of the pulse. The shaper's amplifier core was in principle not affected by this change.

DC input currents showed up as another problem of *Beetle1.1*. A thorough investigation of the problem and subsequent simulations revealed that the front end was able to cope with average input currents only below 2 nA, which is too low for the expected occupancies at LHC*b*.

The cause for this behaviour is inherent to the concept of the *Beetle1.1*'s front end depicted in fig. 2: The gate potential of the NMOS input transistor is on a potential of around the threshold voltage V_{th}(NMOS) of the input transistor above V_{ss}. This potential is also the source voltage of the PMOS feedback transistor. In turn the gate potential of this transistor has to be

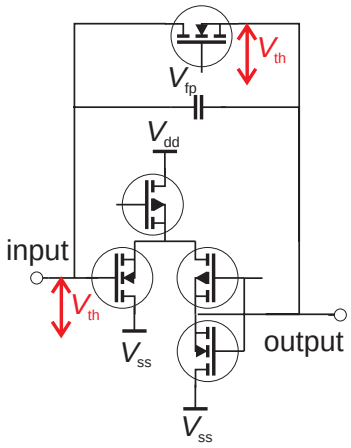

Figure 2: Schematic of the front ends implemented on *Beetle1.1* and *BeetleFE 1.1*: The threshold voltages V_{th} of the NMOS input transistor and PMOS feedback transistor are indicated by arrows.

V_{th}(NMOS)+V_{th}(PMOS)[2] in order to become conductive. Since the absolute value of the threshold voltage is a bit higher for a PMOS than for an NMOS transistor and since V_{th} is lower for short transistors like the NMOS input FET, the situation is worsened. Nevertheless, the circuit reaches a stable operating point, since the feedback transistor is usually operated in the linear (sub threshold) region, where the resistance was still about 15 MΩ when the gate of the feedback transistor was tied to the V_{ss} potential.

A first approach to overcome the problem was implemented on the *BeetleFE 1.1* chip shown in fig. 3: The length of the feedback transistor was decreased in order to reduce its resistance and threshold voltage.

For the *BeetleFE 1.2* (fig. 4) two different concepts were realised: Front ends with PMOS input and feedback transistors and one channel with an NMOS input and feedback transistor.

In case of the PMOS input and feedback configuration (fig. 5), the threshold voltages point away from the power supply rails and thus do not restrict the range of useful voltages V_{fp} on the feedback transistor's gate. The biggest disadvantage of this circuit is the by a factor of 3 lower g_m/area ratio of the input transistor. On the *BeetleFE 1.2* this was partly compensated by the reduction of the channel length and the enclosed waffle geometry of the input transistor.

The solution with NMOS input and feedback transistors shown in fig. 6 is spoiled by the constraints of radiation hard layout techniques: The enclosed geometry limits the W/L ratio to about 4, which together with the minimum W of $\approx 12\,\mu m$ calls for a series of more than 100 transistors to form the feedback resistance.

[2] since V_{th}(PMOS) ≤ 0

Table 1: Design parameters of the front ends of the *BeetleFE 1.1* (Set 2) and *BeetleFE 1.2* (Set 5 and Set 6) test chips.

Set	input transistor	W	L	feedback	shaper feedback
2a...c	NMOS rectangular	3744 µm	0.42µm	PMOS	48.8fF
2d...e	NMOS rectangular	3744 µm	0.42µm	PMOS	20.5fF
5a	PMOS waffle	8310 µm	0.28 µm	PMOS	15 fF
5b	PMOS waffle	8310 µm	0.28 µm	PMOS	18.75 fF
5c	PMOS waffle	8310 µm	0.28 µm	PMOS	37.5 fF
5d	PMOS waffle	7123 µm	0.28 µm	PMOS	18.75 fF
5e	PMOS waffle	7123 µm	0.28 µm	PMOS	37.5 fF
5f	PMOS rectangular	5852 µm	0.28 µm	PMOS	18.75 fF
5g	PMOS rectangular	5852 µm	0.28 µm	PMOS	37.5 fF
5h	PMOS waffle	5936 µm	0.28 µm	PMOS	18.75 fF
5i	PMOS waffle	5936 µm	0.28 µm	PMOS	37.5 fF
6a	NMOS rectangular	3744 µm	0.42 µm	NMOS	48.8 fF

Figure 3: Layout of the *BeetleFE 1.1*: The new front end channels are indicated

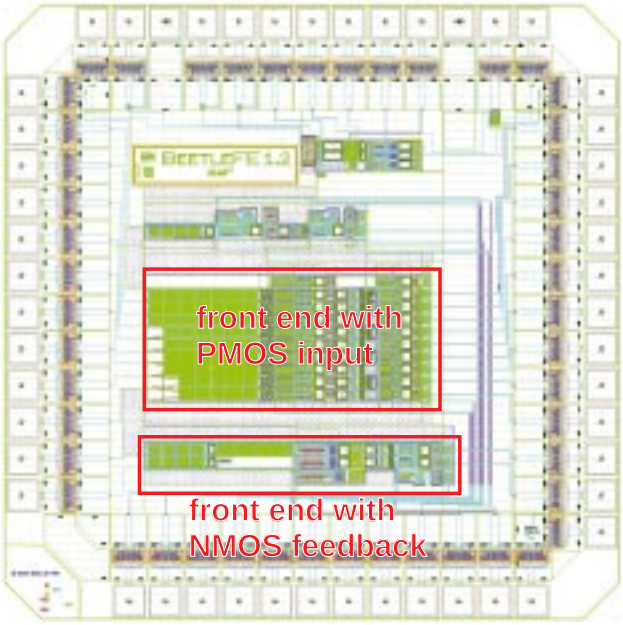

Figure 4: Layout of the *BeetleFE 1.2*: The new front end channels are indicated

III. First results from new front ends

Measurements on the *BeetleFE 1.1* and *BeetleFE 1.2* (figs. 7 and 8) showed that one of the design goals, a rise time well below 25 ns has been reached with both chips. For the *BeetleFE 1.2* it was also found, that the front end could achieve a rise time of ≤ 24 ns with an input capacitance as high as 40 pF. Measurements of the maximum input current, as well as noise measurements are still in progress.

IV. The *BeetleSR 1.0* chip

The *BeetleSR 1.0* chip implements two blocks of 34 registers, each 8 bits wide. Combinatorial logic calculates the parity of these registers, which is available on two groups of 9 pads. Read and write access to these register blocks is accomplished via two independent I^2C interfaces: One is implemented in conventional circuitry, while the other one uses triple redundant flip-flops with majority encoding. The block schematic of the chip is shown in fig. 9, while a triple redundant flip-flop with majority encoder is illustrated in fig. 11.

This chip will permit to measure SEU rates by means of the register blocks, it also allows the calcu-

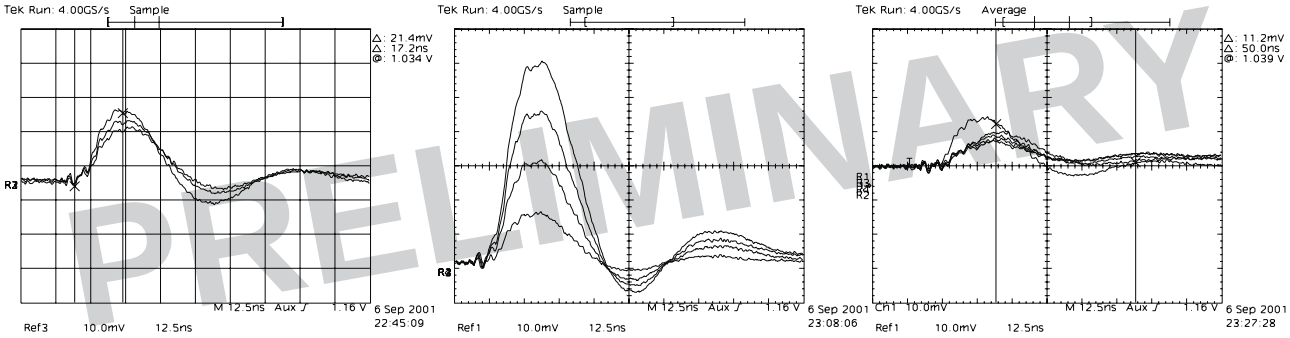

Figure 8: Pulse shapes of the *BeetleFE 1.2* test chip. The left graph shows pulse shapes from different modifications of the "Set 5" (c.f. tab. 1) front end, The middle one shows the response for different input charges, and the right graph depicts the response for input capacitances of 3 pF,10 pF,20 pF,30 pF and 40 pF.

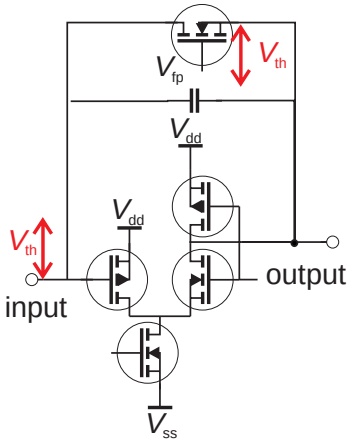

Figure 5: Schematic of the PMOS front ends implemented on *BeetleFE 1.2*: The threshold voltages V_{th} of the PMOS input transistor and PMOS feedback transistor are indicated by arrows.

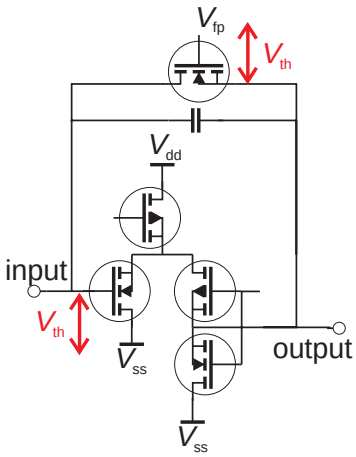

Figure 6: Schematic of the NMOS front ends implemented on *BeetleFE 1.2*: The threshold voltages V_{th} of the NMOS input transistor and NMOS feedback transistor are indicated by arrows.

lation of the SEU suppression arising from the usage of triple redundant flip-flops in state machines.

V. Future plans

Beetle1.1 chips will be irradiated up to 10 Mrad (100 kGy) with the X-ray irradiation facility of the CERN micro electronics group. They will also be used in a test beam with prototype detectors of the LHC*b* inner tracker in October 2001. Studies with the chip bonded to a detector are under way.

The submission of the final version (1.2) of the *Beetle* chip is planned for spring 2002. This chip will implement:

- a modified frontend with a faster shaping and a higher maximum input charge rate, chosen from the front ends on the *BeetleFE 1.1* and *BeetleFE 1.2* chips.
- two single event upset (SEU) detection and correction mechanisms:
  (I) triple redundant flip-flops with majority encoding in state machines and other frequently changed registers, and
  (ii) ECC[3] based on hamming encoding for more static registers.

Status reports and further test results will be available at [6].

[3] Error correction circuit

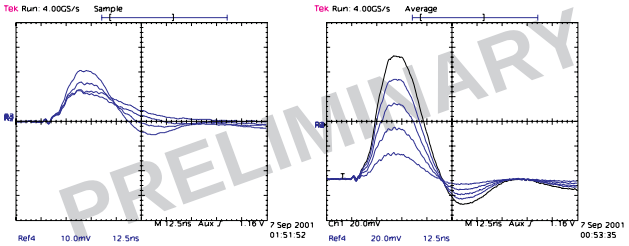

Figure 7: Pulse shapes of the *BeetleFE 1.1* test chip. The left graph shows pulse shapes from different modifications of the "Set 2" (c.f. tab. 1) front end, the right one shows the response for different input charges.

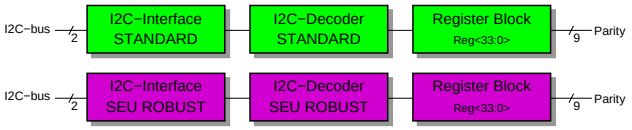

Figure 9: Block schematic of the *BeetleSR 1.0* test chip. Two register blocks with parity encoding are controlled via a standard or a SEU robust I^2C interface respectively.

References

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[4] R. Brenner et al., Nucl. Instr. and Meth. A339 (1994) 564

[5] U. Trunk, Development and Characterisation of the Radiation Tolerant HELIX128-2 Readout Chip for the HERA-*B* Microstrip Detectors, PhD thesis, Heidelberg (2000)

[6] http://wwwasic.kip.uni-heidelberg.de/lhcb/

Figure 10: Layout of the *BeetleSR 1.0* test chip. The two register blocks are located on the right and left hand side of the chip. The I^2C interfaces are the blocks in the centre, the SEU robust one being the larger block.

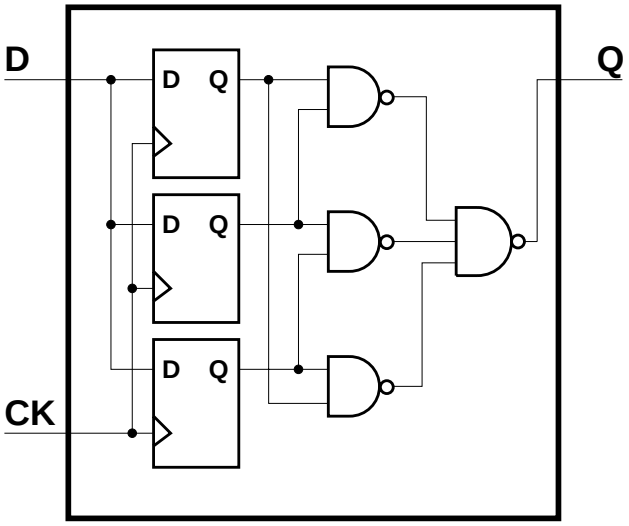

Figure 11: Triple redundant flip-flop with majority encoder used in the SEU robust I^2C interface of the *BeetleSR 1.0* test chip.