Performance of the Beetle Readout Chip for LHCb

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Abstract

This paper details the development steps of the 128 channel pipelined readout chip *Beetle*, which is being designed for the silicon vertex detector, the inner tracker, the pile-up veto trigger and the RICH detectors[1] of LHCb.

Section II. summarizes the *Beetle* chip architecture. Section III. shows the key measurements on the first chip version (*Beetle1.0*) which drove the design changes for the *Beetle1.1*. First performance data of the new chip is presented in section IV., while an outlook on the future test and development of the chip are given in section V.

I. Introduction

Since the beginning of the development of the *Beetle* chip in late 1998 the chip family has grown to 2 members of complete readout chips (*Beetle1.0* and *Beetle1.1*) and 8 (2×2) mm^2 chips implementing test-structures and prototype components.

Due to a layout error in the control circuitry, the first prototype of a complete readout chip (*Beetle1.0*) is only functional with a patch. The successor version *Beetle1.1* fixes this bug among others.

II. Chip Architecture

The *Beetle* [1][2] can be operated as an analogue or alternatively as a binary pipelined readout chip. It implements the basic RD20 frontend electronics architecture [3]. Figure 1 shows a schematic block diagram of the chip.

The chip integrates 128 channels. Each channel consists of a low-noise charge-sensitive preamplifier, an active CR-RC pulse shaper and a buffer. The risetime of the shaped pulse is ≤ 25 ns, the spill-over left 25 ns after the peak is below 30%. The chip provides two different readout paths. For the *prompt binary readout* the frontend's output couples to a comparator which features a configurable polarity (to detect input signals of both polarities) and an individual threshold level. Four adjacent comparator channels are logically ORed, latched, multiplexed by a factor of 2 and routed off the chip via low voltage differential signaling (LVDS) ports at 80 MHz. The *pipelined readout path* can operate in either a *binary* mode by using the comparator outputs or an *analogue* mode by sampling the frontend's buffer output with the LHC bunch-crossing frequency at 40 MHz. The sampled amplitudes are stored in an analogue memory (pipeline) with a programmable latency of max. 160 sampling intervals and an integrated trigger buffer (fifo) of 16 stages. The signal stored in the pipeline is transfered to the multiplexer via a resetable charge-sensitive amplifier. Within a readout time of 900 ns current drivers bring the serialized data off chip. The output of a dummy channel is subtracted from the analogue data to compensate common mode effects. All amplifier stages are biased by forced currents. On-chip digital-to-analogue converters (DACs) with 10 bit resolution generate the bias currents and voltages. For test and calibration purposes a charge injector with adjustable pulse height is implemented on each channel. The bias settings and various other parameters like the trigger latency can be controlled via a standard I^{2}C-interface [4]. All digital control and data signals, except those for the I^{2}C-ports, are routed via LVDS ports.

The chip is fabricated in 0.25 μm standard CMOS technology and has a die size of 6.1×5.5 mm^2. The

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[1] in case multianode photomultiplier tubes are used

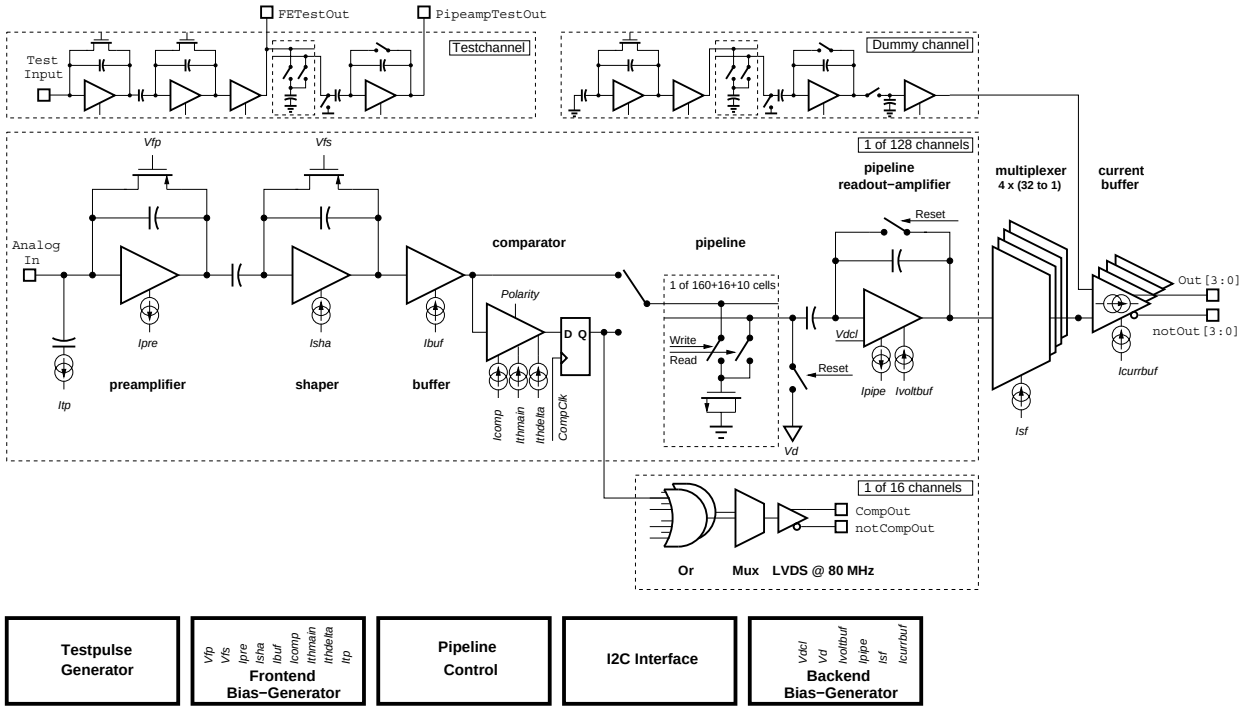

Figure 1: Schematic block diagram of the *Beetle* readout chip.

layout with the corresponding floor plan is depicted in fig. 2.

The chip is designed to withstand a total dose in excess of 10 Mrad (100 kGy) taking the following design measures [5]: Enclosed gate structures for NMOS transistors suppress an increase in leakage current under irradiation; a consistent use of guard rings minimizes the rate of single event effects [6]. Forced bias currents are used in all analogue stages instead of fixed node voltages.

III. The Beetle1.0 Chip

Beetle1.0 is the first prototype of a complete readout chip. It was submitted in April 2000. This chip version has to be patched, e.g. with a focused ion beam, to be functional. A layout error in a tristate buffer of the control circuitry prevents programming the chip via the I^2C-bus. The chip's internal data bus is permanently forced to logic 0. Due to a bug in the extraction software, this error was not discovered by the available checking tools. A focused ion beam patch has been applied to a single die. The patch however enables only a write access to the chip. The chip registers cannot be read back. Fig. 3 shows the output signal of the patched die using the analogue pipelined readout path. All 128 channels are multiplexed on one port. The figure is an overlay of different events with input signals corresponding to 1, 2, 3, 4 and 7 MIPs[2] applied to 7 single and a group of 4 adjacent channels of the chip. On the figure the different input levels are clearly visible on the group of 4 channels. The baseline shift is due to a voltage drop on the `Vdcl`-bias line of the pipeline readout amplifier (cf. fig.1). The header is correctly encoded but has wrong voltage levels due to a bug in the multplexer.

Investigations on the *BeetlePA10* testchip which implements the pipeline readout amplifier with access to all internal nodes revealed a bug in the layout of the transmission gate used to reset the amplifier. The same error is present in the switches of the multiplexer: A shorted transistor which is used as dummy device in the transmission gate is incorrectly wired. This causes the injection of charge into the amplifier's input which results in shifting it's operating point. This error was not detected by the layout versus schematic (LVS) check, because edgless shorted transistors are not extracted as physical devices.

IV. The Beetle1.1 Chip

The *Beetle1.1* chip version was submitted in March 2001 with the intention to fix all known bugs and to avoid the implementation of new features unless they are critical for the complete design.

[2] Minimum Ionizing Particle, 1 MIP = 11,000 electrons in 150 μm silicon

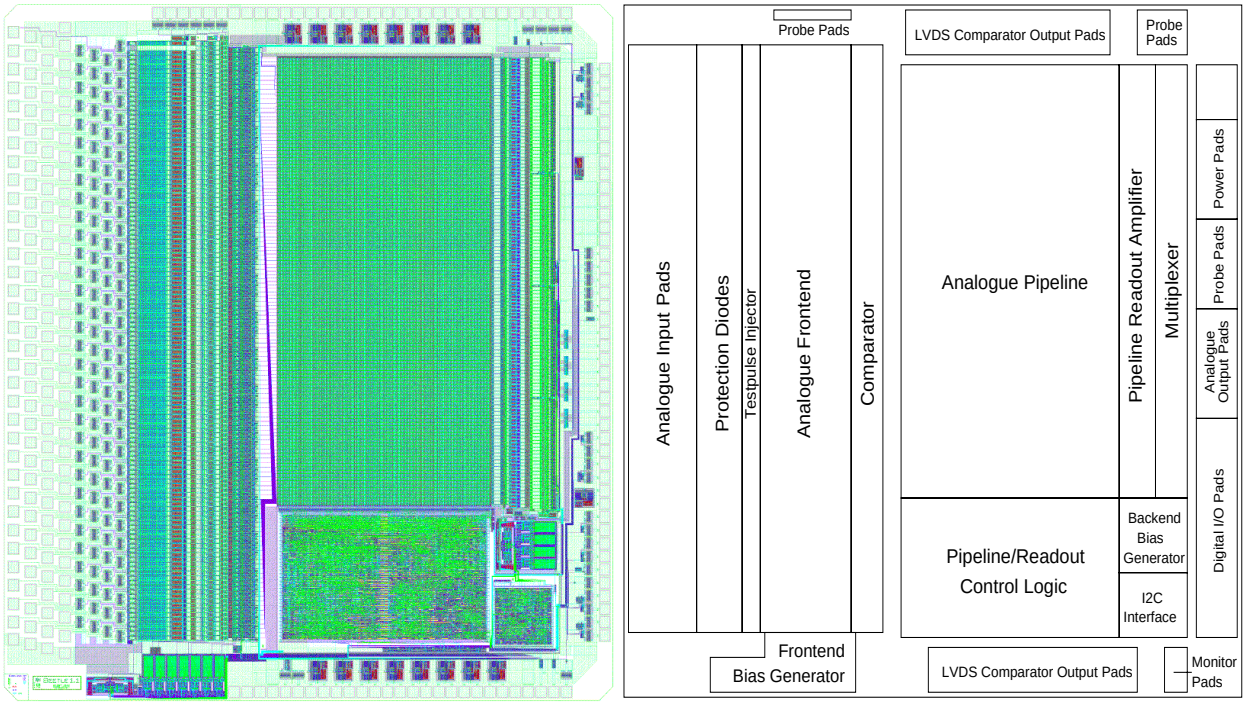

Figure 2: Layout of the *Beetle1.1* chip version and its corresponding floor plan. The die size is $(6.1 \times 5.5)\text{mm}^2$.

A. *Design Changes*

The following design changes have been applied:

- The layout of the tristate buffers in the control circuit has been modified.
- A source follower has been added to each pipeamp channel to buffer the `Vdcl` bias node.
- The layout of the transmission gate used in the pipeamp and multiplexer has been modified.
- A wiring error in the multiplexer has been resolved.

In addition to the above mentioned bug fixes some minor changes have been done: The digital delay element[3] for the I^{2}C-SDA line has been replaced by an analogue one. The layout of the pipeline has been modified to reduce crosstalk. The test channel has been extended down to the pipeamp's output.

B. *First Measurement Results*

1). *Pipelined Readout*

The output signal of the complete analogue chain is shown in fig. 4. All 128 channels are multiplexed on one port. Input signals corresponding to 2 MIPs are applied to 7 single and two groups of 2 adjacent channels of the chip. The first eight bits of the data stream encode the pipeline column number. Column number 176 has been triggered in this plot which is clearly visible in the data header. The voltage levels of the header correspond to ±2 MIPs. The slight variation of the baseline of approx. 1/3 MIP is not yet understood.

Fig. 5 depicts the *binary* pipelined readout path where the comparator outputs are sampled into the pipeline. Again all 128 channels are multiplexed on one port. As in the analogue pipelined readout path the header is encoded with ±2 MIPs. The logic levels of the binary channels are represented with 0 and 10 MIPs respectively.

2). *Frontend Pulse Shape*

Information about the frontend's pulse shape can be obtained from either the test channel output `FETestOut` (cf. fig. 1) or from a pulse shape scan. Here, the frontend's output is read out via the pipelined path while the preamplifier input signal is shifted w. r. t. the sampling clock. Fig. 6 shows the shaped pulse measured at the output node of the test channel. The load capacitance at the preamplier's input has been varied in four steps (3 pF, 13 pF, 23 pF, 32 pF). Fig. 7 depicts the result of a pulse shape scan with a capacitive input load of 3 pF. For the chosen bias settings the peaking time in both plots exceeds 30 ns which is in disagreement with simulation results. New frontend developments (cf. sect. V.) will overcome this problem.

[3] used to assure timing constraints of the I^{2}C-protocol

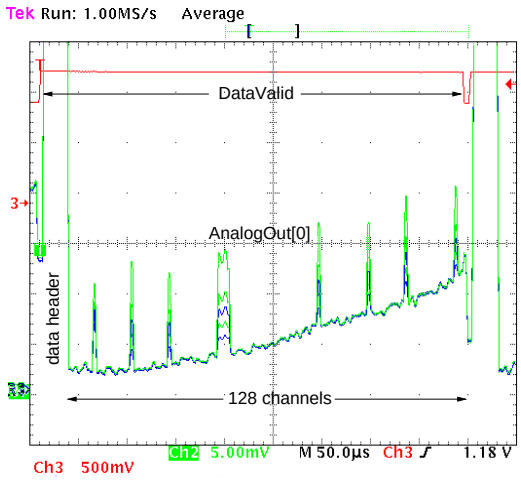

Figure 3: Analogue output signal of a *Beetle1.0* chip. All 128 channels are multiplexed on one port. Input signals corresponding to 1, 2, 3, 4 and 7 MIPs have been applied to 7 single and a group of 4 adjacent channels of the chip. The readout speed is set to 1.25 MHz.

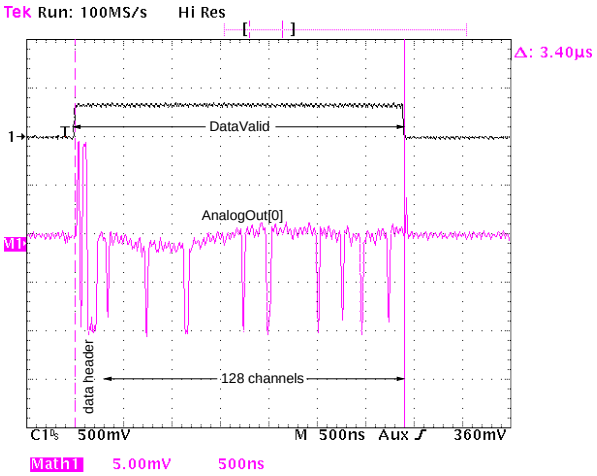

Figure 4: Analogue output signal of a *Beetle1.1* chip. All 128 channels are multiplexed with 40 MHz on one port. Input signals corresponding to 2 MIPs have been applied to 7 single and two groups of 2 adjacent channels of the chip.

V. Future plans

It is planned to irradiate the *Beetle1.1* chips in October 2001 at the X-ray irradiation facility of the CERN microelectronics group up to 10 Mrad.

The submission of version 1.2 of the *Beetle* chip is intended in spring 2002. This new chip version will implement the following:

- A modified frontend with a faster shaping and a higher tolerable maximum input charge rate.
  Two (2×2) mm^2 testchips have been submitted in May 2001 implementing in total 17 different frontends. A detailed description can be found in [7]. After intensive testing of these structures a decision for the frontend modification will be made.

- Two single event upset (SEU) detection and correction mechanisms.
  First investigations on SEU hardened logic will be made with the testchip *BeetleSR10*. An error correction mechanism based on hamming encoding is under development.

Status reports and further test results will be available at [8].

References

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[6] F. Faccio et al., Total Dose and Single Event Effects (SEE) in a 0.25 μm CMOS Technology, CERN/LHCC/98-36 (1998)

[7] U. Trunk et al., Enhanced radiation hardness and faster front ends for the Beetle readout chip, to be published in: Proceedings of the 7th Workshop on Electronics for LHC Experiments

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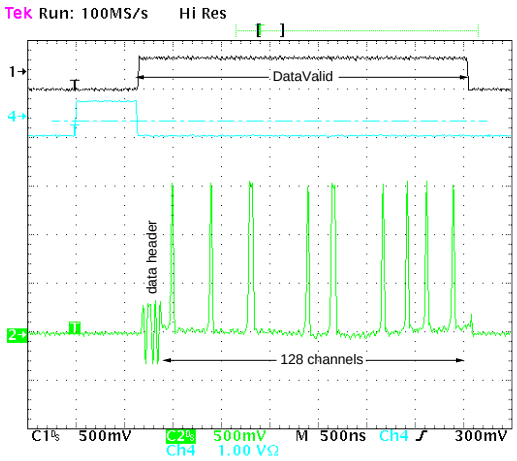

Figure 5: Output signal of the binary pipelined readout path. All 128 channels are multiplexed on one port. The header is encoded with ±2 MIPs. The logic levels of the binary channels are represented by 0 and 10 MIPs respectively.

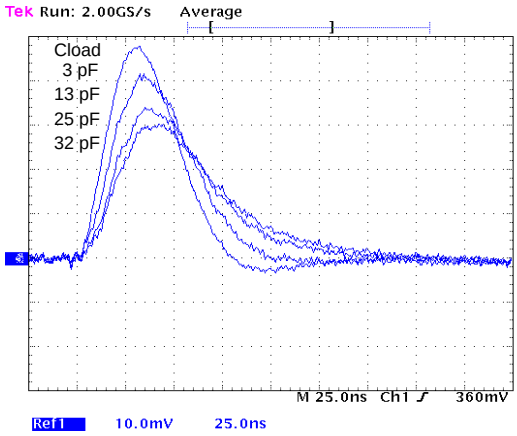

Figure 6: Transient response on a delta-shaped input signal of 38,000 electrons ($3\frac{1}{2}$ MIP) measured at the *Beetle's* test channel. Load capacitances of 3 pF, 13 pF, 25 pF and 32 pF have been applied to the preamplifier's input.

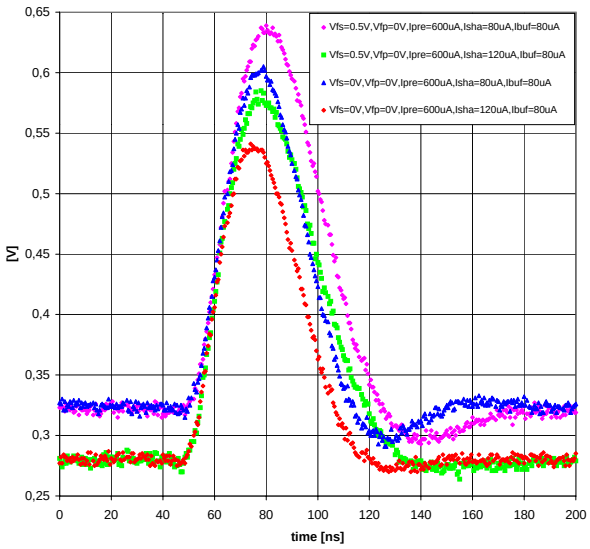

Figure 7: Frontend output signal with varying bias settings obtained from a pulse shape scan. The capacitive input load is 3 pF.