Design of a Prototype Frontend and Bias Generator for a new Readout Chip for LHCb

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Readout Chip for LHCb:

Silicon Vertex Detector
Inner Tracker
Pile-Up Veto Trigger
RICH (Multi Anode Photo multiplier tube or Pad Hybrid Photo Diode)

- chosen technology: standard 0.25um CMOS process
- 128 channels with analog input stages / 50um overall pitch
- capacitor array used as analogue pipeline
- 3 readout modes: 40 MHz via 4 ports analog
  80 MHz via 2 ports binary
  40 MHz via 1 port + daisy chaining
  } readout per event < 900 ns
- fast trigger output via adjustable comparator threshold
- programmable latency up to 160 clock cycles
- 16 multi event buffer
- I2C programming interface
- intensive test and monitoring facilities

Requirements on radiation hardness (driven by vertex detector)

vertex detector FE-electronics:

2 MRad / year -> 10 MRad total dose

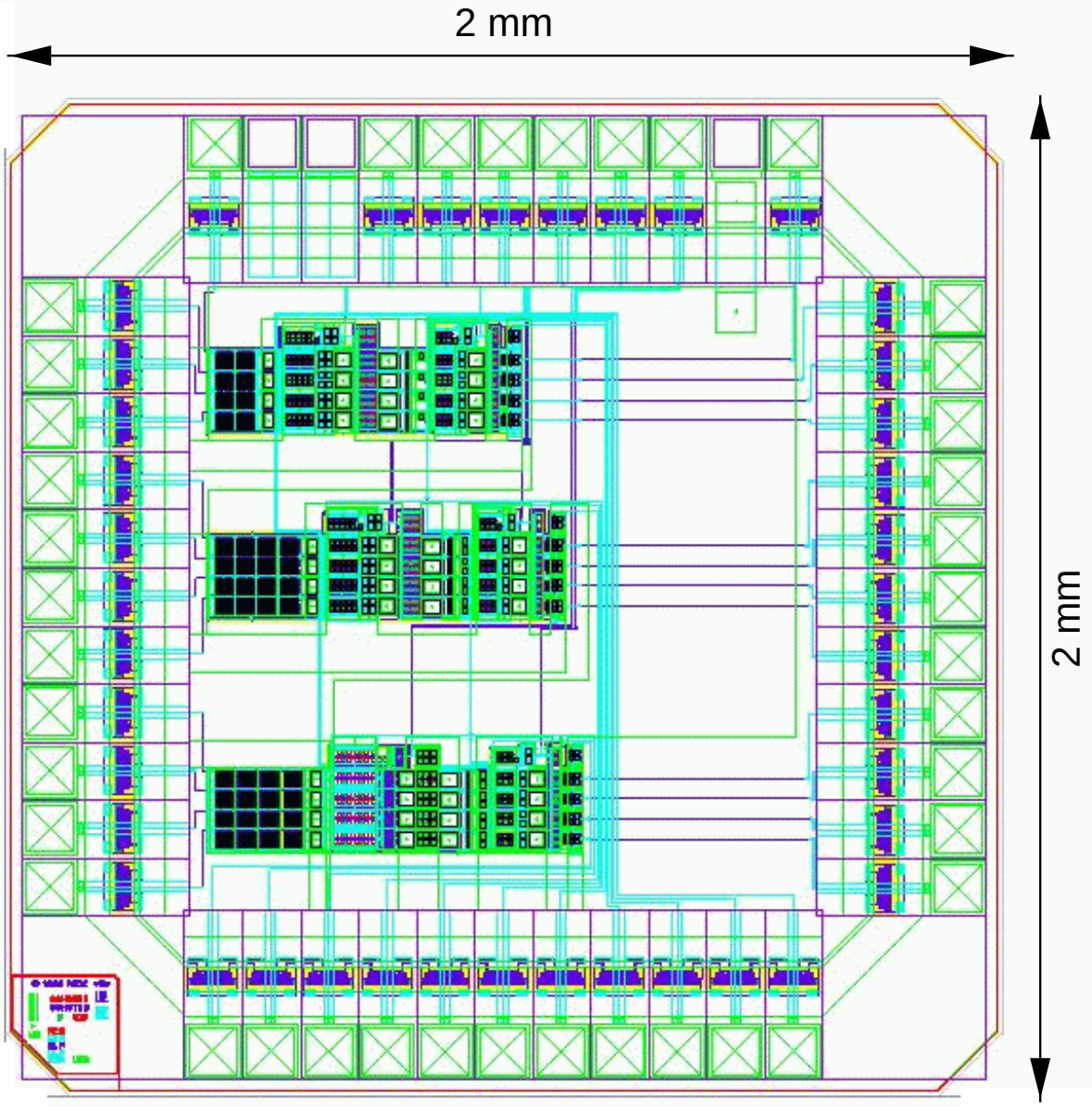
Design techniques to enhance radiation resistance:

- minimize threshold voltage shift by choice of technology
- edgeless n-mos transistor layout to reduce leakage current
- systematic use of guardrings to minimize SEE rate

(Total Dose and Single Event Effects (SEE) in a 0.25um CMOS Technology, F.Faccio et al. in CERN/LHCC/98-36)

- forced bias currents / node voltages not fixed
- passive components used as negative feedback

(e.g. RD20 or HELIX128, W. Fallot-Burghardt et al. in HD-ASIC-33-0697)



Chip1:

BeetleFE-1.0

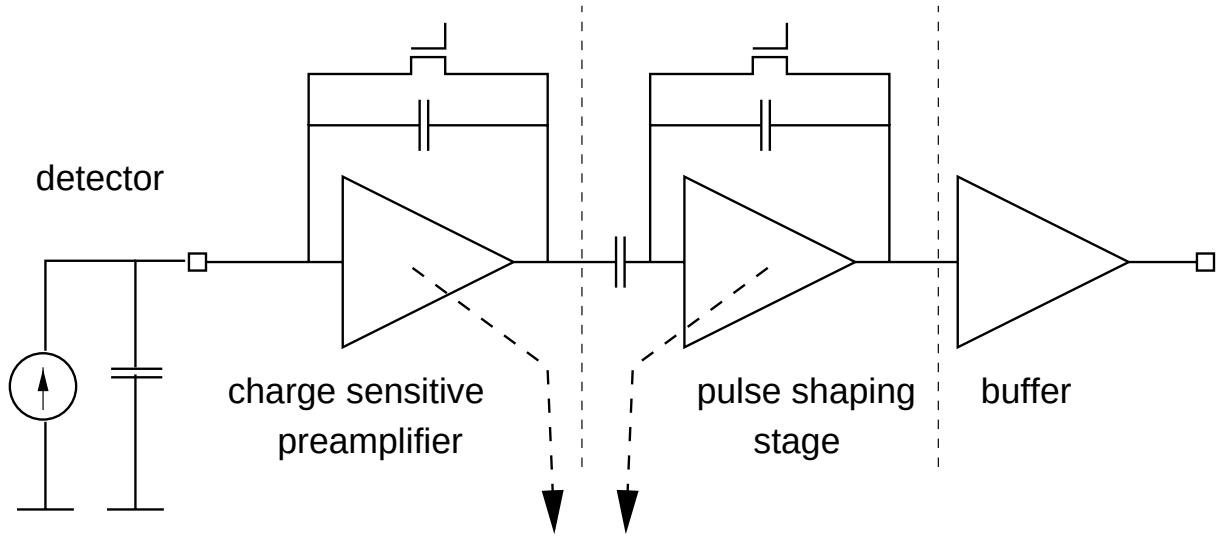
3 different types of frontend
(each as block of 4 channels

Set 1:
input transistor : pmos
slow shaping

Set 2:
input transistor : pmos
fast shaping

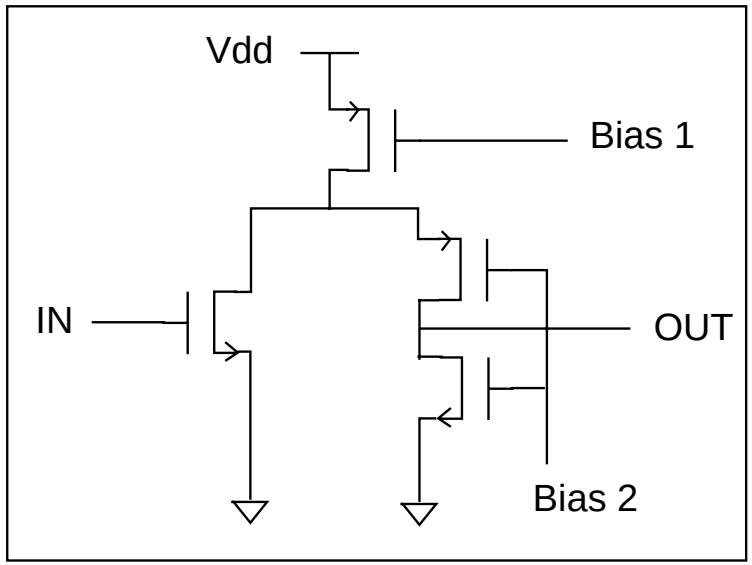
Set 3:
input transistor : nmos
fast shaping

Frontend Building Blocks



- charge sensitive preamplifier with adjustable feedback resistance

- active RC-CR shaper time constant adjustable by feedback resistance



- preamplifier and shaper use a folded cascode configuration as an opamp cell

Noise of the Frontend:

- noise of frontend determined by noise of input transistor

$$\frac{ENC_{thermal}}{C_{input}} = e\sqrt{\frac{(1+\eta)\cdot kT}{3\cdot T_{peak}\cdot g_m}}$$

g_m transconductance of input transistor

T_{peak} peaking time

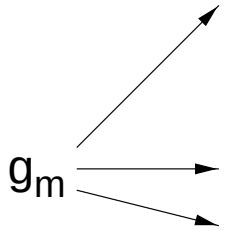
η bulk-source transconductance

(1/f noise can be neglected)

values simulated for third set

slope of noise function	power per channel
46.5 e/pF	0.88 mW
41.4 e/pF	1.13 mW
37.5 e/pF	1.38 mW
35.5 e/pF	1.63 mW
33.6 e/pF	1.88 mW

degress of freedom:



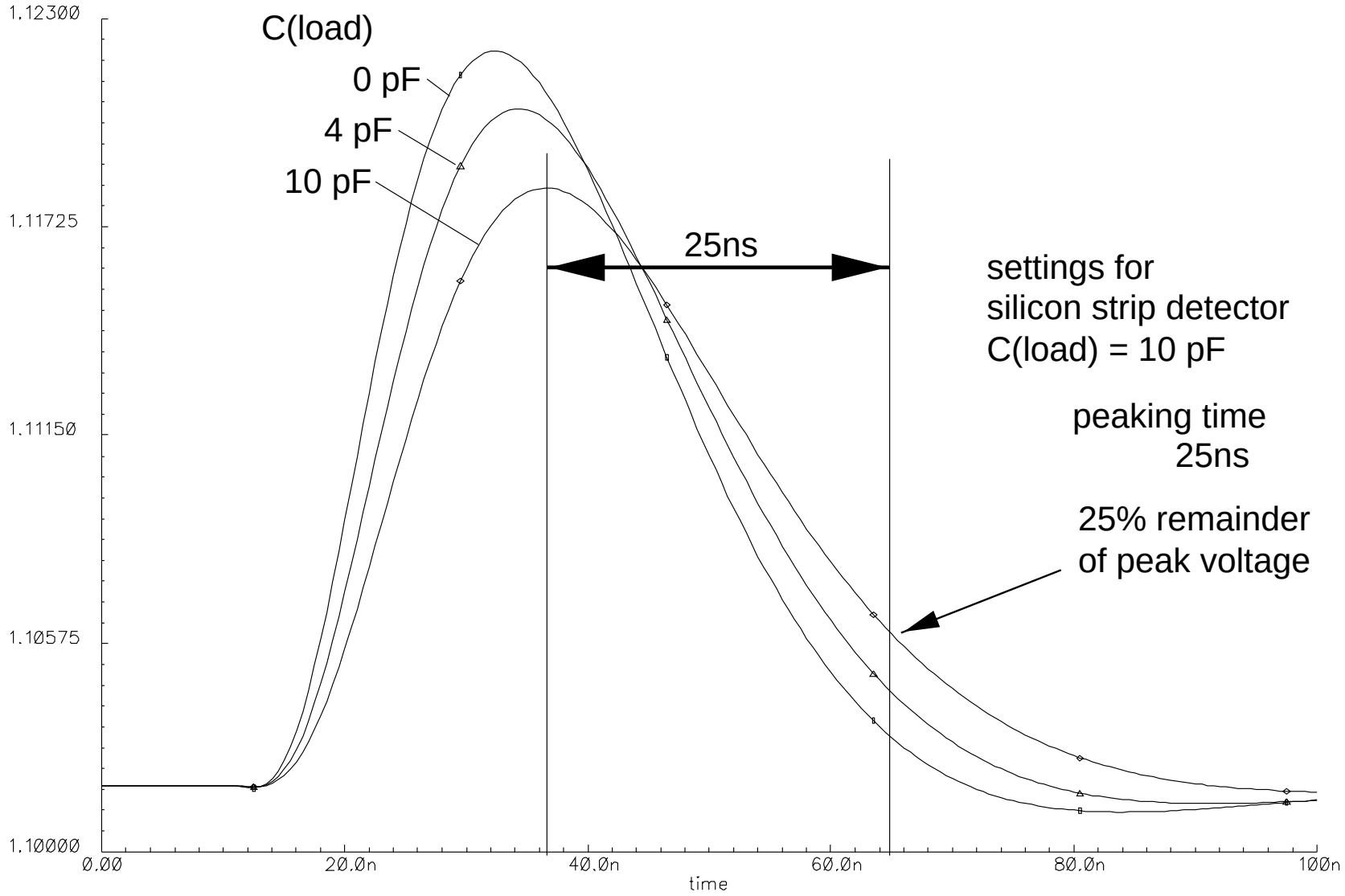
I_{ds} drain-source current, limited by subsystem specification (e.g. silicon vertex detector 4 mW/channel)

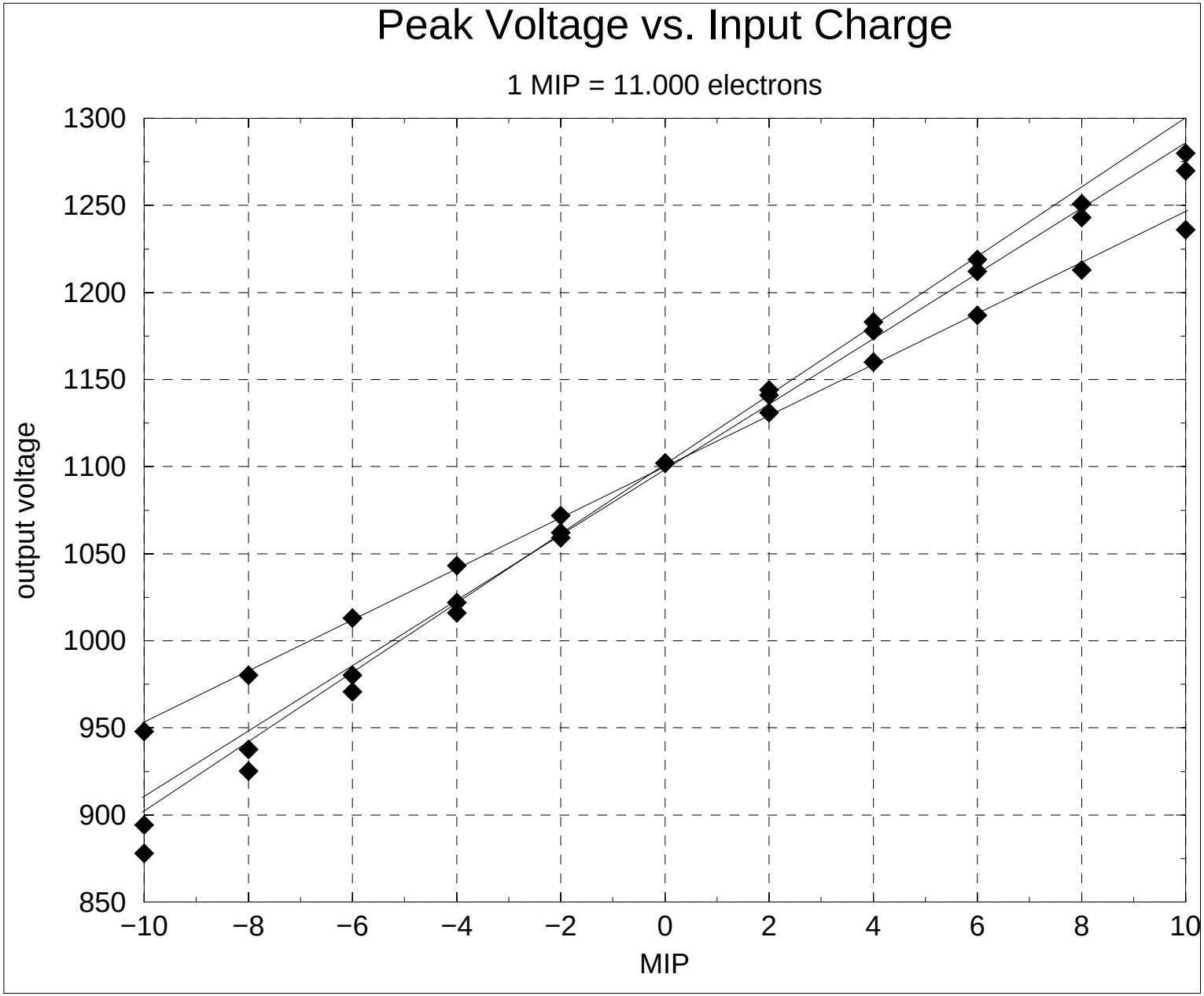
W optimum value to be chosen

L optimum value to minimize η

T_{peak} specified by subdetector system

Simulation Results



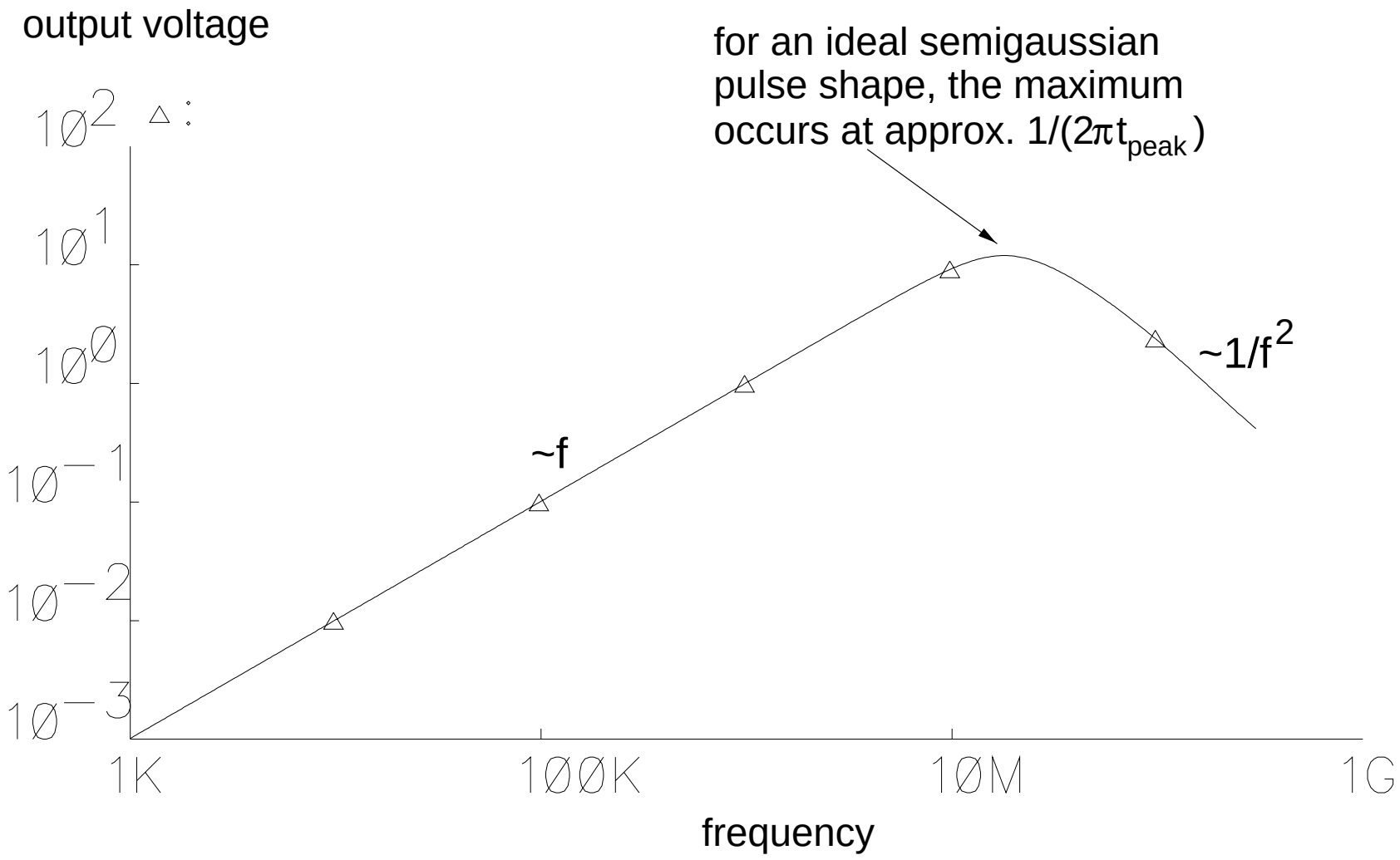


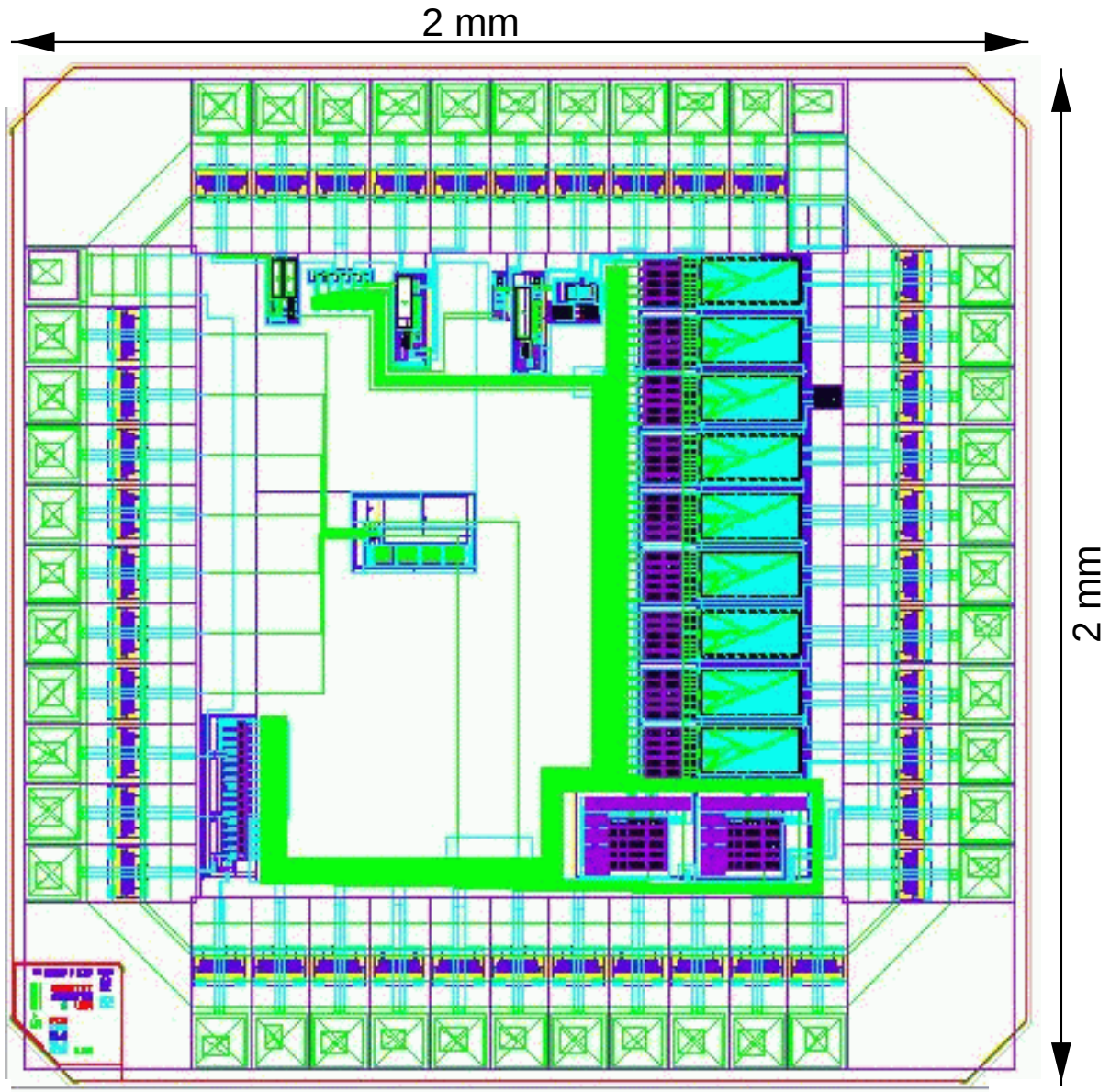
Simulated dynamic range

-10 MIP to +10 MIP

load capacitance	gain
0pF	20.4 mV/MIP
4pF	19.0 mV/MIP
10pF	14.5 mV/MIP

Frequency response of the pulse shaper





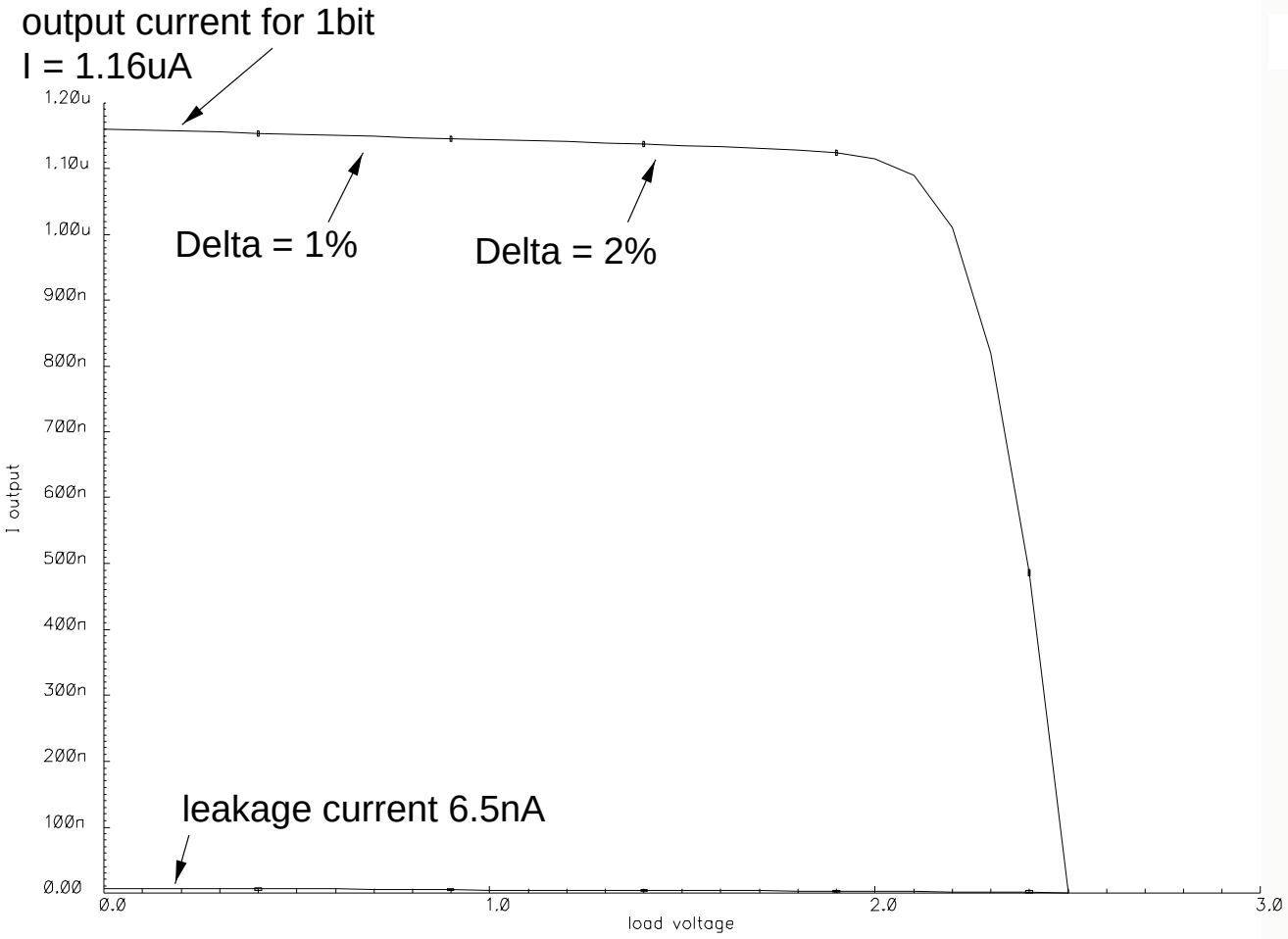
BeetleBG-1.0

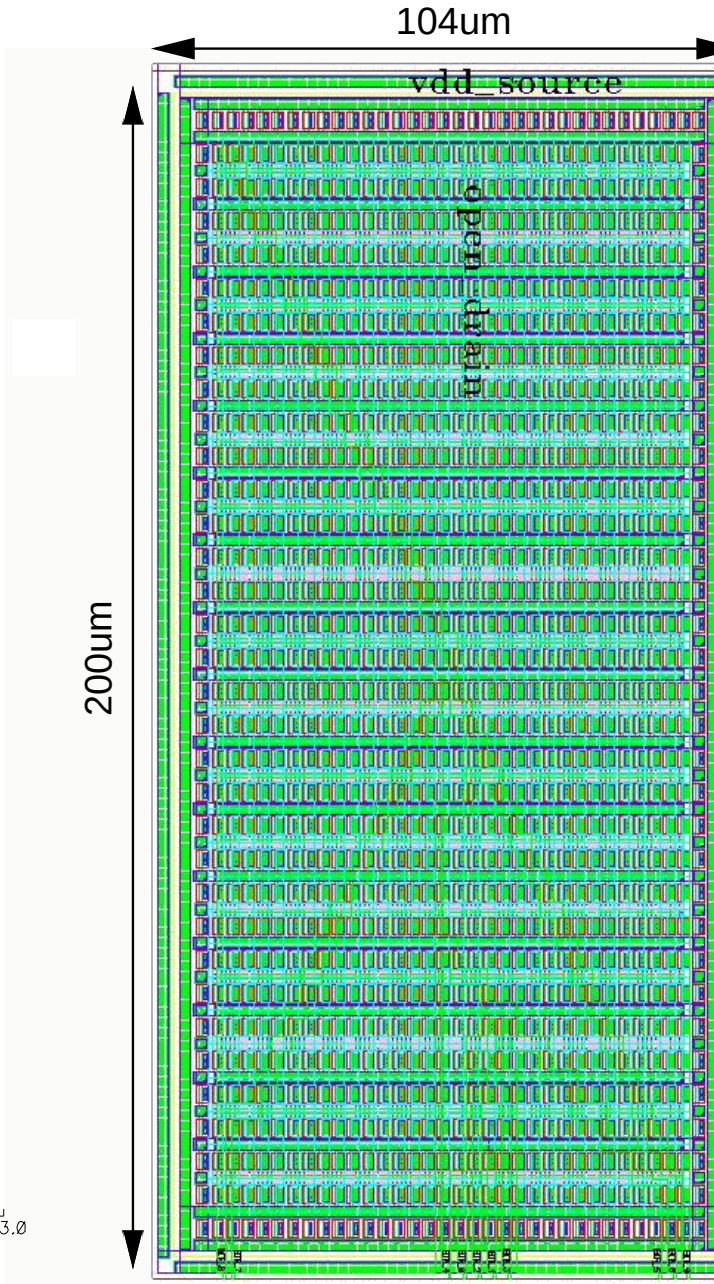
- 3 different types of current sources
- 10bit R2R ladder voltage DAC
- 10 bit current DAC
- teststructures to study transistor parameters under irradiation

to be bonded to the FE chip

current DAC with a resolution of 10 bit

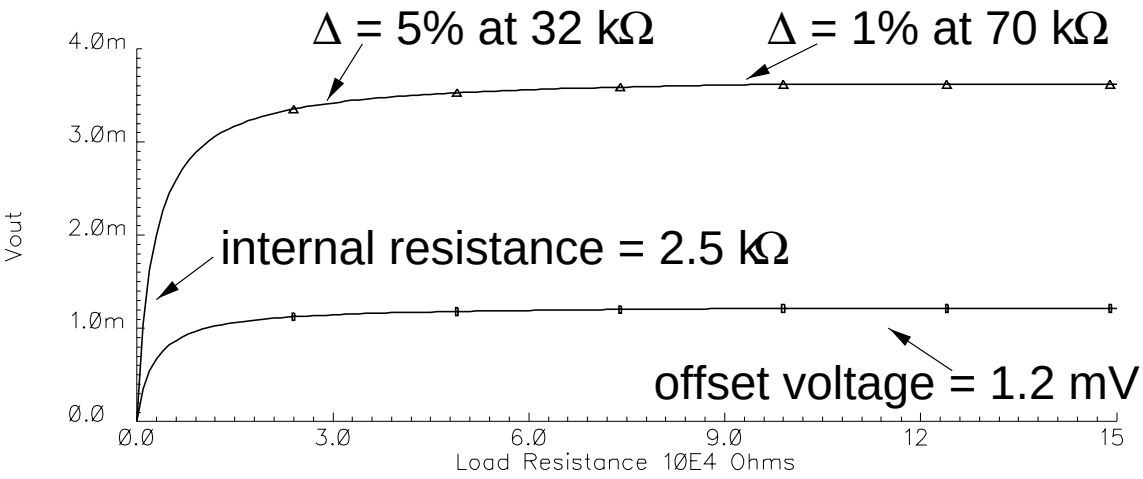
- 1024 conventional pmos
  W/L = 0.6 um / 3 um
- 132 dummy pmos for matching

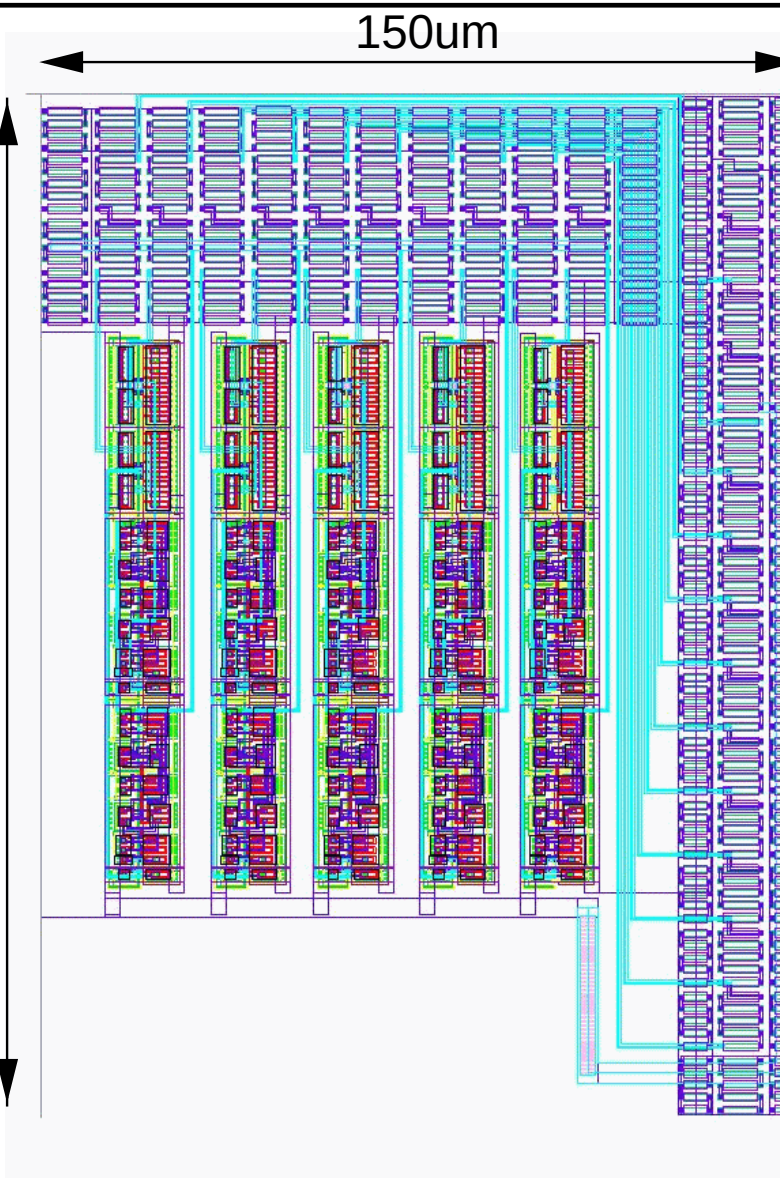




R2R voltage DAC with a resolution of 10bit

- 34 N+ diffusion resistors each 3.0kΩ
- output range 0 to 2.5 V
- power consumption 690 uW





3 different types of current sources

type of current source	maximum load (Δ I = 1%)	small signal resistance	power	size
100 uA current source with opamp feedback	1.06 V	4 MΩ	2.35 mW	164 x 61 um^2
100 uA current source with opamp feedback and regular cascode output	1.94 V	14 MΩ	2.5 mW	189 x 61 um^2
100 uA regular cascode	1.93 V	17 MΩ	599 uW	84 x 23 um^2

future milestones:

- end of ’99: submission of further components
  - second iteration of frontend
  - calibration pulse generator
  - comparator
  - pipeline capacitor array
  - pipeline readout amplifier
  - control logic
  - multiplexer
  - readout buffer

- october 2000: first iteration of readout chip
- october 2001: final readout chip

(plus additional test runs)

see status on: http://wwwasic.ihep.uni-heidelberg.de/lhcb