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Beetle Specification

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1 Revision history

Table 1: Revision history

Date	Author	Modification
22.06.2001	U.T.	Original document created from Beetle *Reference Manual* [1]

2 Overview

The *Beetle* is a low noise 128 channel pipelined readout chip for silicon microstrip detectors and MAPMTs[1]. It is intended for various detector components of the LHCb experiment:

- The vertex detector (VELO)
- The pileup veto counters (VETO)
- The inner tracker (IT)
- The RICH[2] (in case of MAPMT readout)

Subsequent to the charge sensitive preamplifier/shaper frontends, the *Beetle* implements two independent sampling readout paths: A prompt binary one for trigger applications and a pipelined path with analog or digital output for tracking applications.

The analog stages of the chip are optimized for operation at 40MHz.

Full remote control of the chip is accomplished via a standard I^2C interface.

The *Beetle* is manufactured in commercial 0.25µm CMOS technology and withstands a total dose of 10Mrad (100kGy).

2.1 Architecture

A block schematic of the *Beetle* is shown in fig. 1

Each of the *Beetle*'s 128 input channels consists of a protected input pad connecting to a charge sensitive preamplifier, an active $CR-RC$ pulse shaper and a buffer.

[1]Multi anodede photomultiplier tube
[2]Ring image Čherenkov counter

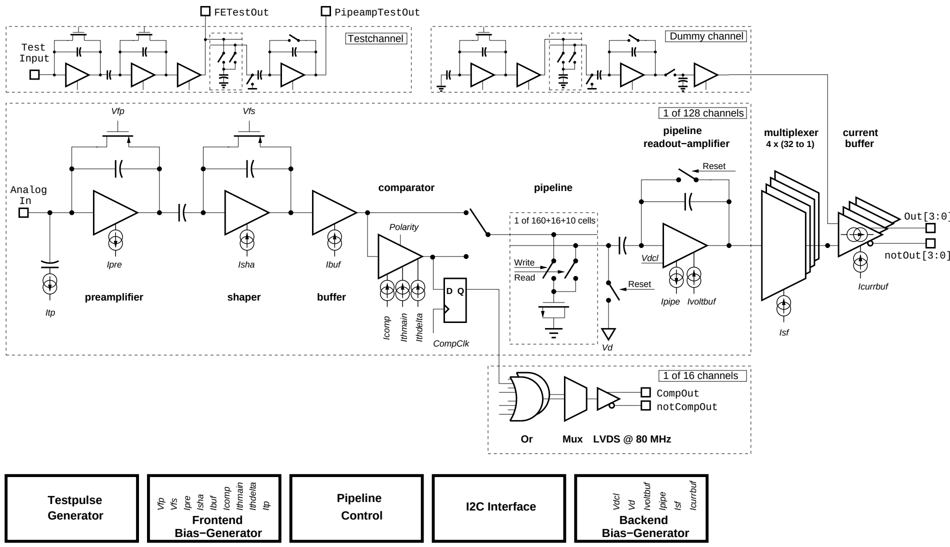


Figure 1: Schematic block diagram of the *Beetle* readout chip.

Key specifications for the front end are:

Detector (parallel) capacitance C_{p} at amplifier input	≤ 40pF
Rise time $t_{\mathrm{rise}}(0\ldots100\%)$	≤ 25ns
Amplitude @ $t_{\mathrm{rise}} + 25$ns i.e. 25ns after the peak	$\leq 25\%$ i.e. a spill-over of $\leq 25\%$ into the next sample @ 40MHz is permitted
Noise @ $C_{\mathrm{p}} = 10$pF	$\leq 785e^{-}$
Noise @ $C_{\mathrm{p}} = 30$pF	$\leq ???e^{-}$

For the **prompt binary readout path** , the front end's output couples to a comparator with invertible output polarity (to detect input signals of both polarities). The outputs of four adjacent channel's comparators are logically *or*ed and latched with `CompClk`. The outputs of these latches are then multiplexed to 16 LVDS[3] ports synchronous to the `CompClk` signal.

Key specifications for the comparator are:

[3] Low voltage differential signaling

Polarity	both, globally selectable
Threshold	globally and locally adjustable
Offset subtraction	yes
Maskable outputs	yes
Resolution @ $C_\mathrm{p} = 10\mathrm{pF}$	$\leq ??? e^-$
Resolution @ $C_\mathrm{p} = 30\mathrm{pF}$	$\leq ??? e^-$
Time over threshold t_min	$\leq$???ns
Sampling frequency $f_\texttt{CompClk}$	$\geq$ 40MHz
Output data rate f_out	$= 2 f_\texttt{CompClk}$

The **pipelined readout path** can operate in either a *binary* mode by using the comparator outputs or an *analog* mode by using the front end's buffer output. The architecture of this readout path follows the concept of the CERN RD20 frontend electronics: With each cycle of the `Clock` signal the amplitudes of all 128 channels are sampled on a *column* of an analog memory (*pipeline*). A `trigger` signal arriving *latency* (c.f. tab. 6) `Clock` cycles later will mark this column for readout. Otherwise the data of this column is discarded. The oldest data marked for readout is read out of the pipeline and multiplexed onto 1, 2 or 4 ports. The analog data is preceeded by a header encoding the pipeline column of the data or some error information in case of malfunction. The data is driven off chip by differential current drivers. Presence of valid readout data is indicated by the `DataValid` signal.
Key specifications for pipeline and readout are:

Max. latency	160 samples
Max. pending readouts (derandomizer depth)	16 triggers
Max. consecutive triggers	16
Number of output ports	1, 2 or 4 (selectable)
Readout speed	$2 \cdot$ `Clock` or `Clock`$/n$, $n = 1 \ldots 256$
Readout time $t_\mathrm{read} \leq 900\mathrm{ns}$	4 ports @ 40MHz (`Clock`) 2 ports @ 80MHz ($2 \cdot$ `Clock`)

Setup and slow control of the *Beetle* is accomplished via a standard $\mathrm{I}^2\mathrm{C}$-interface. **Key specifications** for setup and slow control are:

Interface & protocol	$\mathrm{I}^2\mathrm{C}$
Address mode	7bit $\mathrm{I}^2\mathrm{C}$ address mode
Setup	register based

2.1.1 Input pads

The input pads are arranged in a fourfold staggered arrangement. Attached to each input is a pair of diodes, which connect to the power supply and thus form an overvoltage protection. The protection is sufficient for the handling of the chips. It can be extended by an external series resistor $R_{\mathrm{prot}} \geq \frac{t_{\mathrm{ondiode}}}{C_{\mathrm{g}} \ln(\frac{2.5\mathrm{V}}{U_{\mathrm{det}}})}$ (with $t_{\mathrm{ondiode}} \approx XXX$ps the turn-on time of the protection diodes, $C_{\mathrm{g}} \approx 2$pF the gate capacitance of the input transistor and U_{det} the peak voltage of the spark, i.e. the detector's operating voltage) in order to provide spark protection for e.g. gaseous detectors.

2.1.2 Test pulse circuit

Further information required

2.1.3 Charge sensitive preamplifier

The input stage is formed by a folded cascode amplifier core, which uses a $C_{\mathrm{fb}} = 400$fF feedback capacitor to form a charge sensitive amplifier. The discharge of the C_{fb} is accomplished with a parallel transistor.

Adjustable parameters (c.f. sect. 6):
preamplifier bias current *Ipre*
gate voltage of the feedback transistor *Vfp*
Dependencies:
Ipre primarily affects the noise behavior of the preamp and in conjunction with the capacitance at the amp's input the undershoot of the shaped signal.
Vfp affects noise and rate capability of the preamplifier.

2.1.4 Active $CR - RC$ pulse shaper

The CR part is formed by a *MIMCAP* capacitor, connecting to an active integrator, which contributes the R by its input impedance. The integrator itself uses a folded cascode amplifier core and provides the RC part of the shaping.

Adjustable parameters (c.f. sect. 6):
shaper bias current *Isha*
gate voltage of the feedback transistor *Vfs*
Dependencies:
Isha has only a very faint influence on the rise time of the shaped pulse.
Vfs in conjunction with the capacitance at the preamp's input affects the length and amplitude of the shaped pulse.

2.1.5 Frontend buffer

The buffer is a simple source follower, which provides the low impedance to drive the comparator and the analog memory (*pipeline*), depending on the selected readout mode.

Adjustable parameters (c.f. sect. 6):
buffer bias current *Ibuf*
Dependencies:
Ibuf has only a very faint influence on the amplitude of the shaped pulse.

2.1.6 Comparator

A comparator for each channel indicates that the frontend's output exceeded the *threshold level*. This *t*hreshold level is the sum of

- the channel's signal itself, averaged by a $\tau = 5\mu$s low pass filter for offset compensation
- a *common* threshold level for all 128 channels
- an additional *channel* threshold, which has a resolution of 3 bits

The comparator outputs' polarity can be switched (c.f. tab. 6 and fig. 5) and their signals are are combined (i.e. logically *or*ed) together in groups of four channels. These signals are latched and multiplexed to 16 LVDS[4] ports synchronous to the `CompClk` signal. The assignment of the channels to the `CompOut` ports is shown in tab. 7.

Adjustable parameters (c.f. sect. 6):
Global threshold *Ithmain* Local threshold LSB *Ithdelta* Local threshold (bits $5 \ldots 7$ in *CompControl*) Latching (bit 4 in *CompControl*) Operation(on/off)(bit 3 in *CompControl*) Signal polarity (bit 1 in *CompControl*)
Dependencies:
The threshold of an individual channel is given by $(Ithmain + Ithdelta \cdot CompControl < 7,5 >) \cdot ???e^{-}$
$CompControl < 4 >= 1$ switches the prompt binary path to transient transmission mode, i.e. outputs immediatelly follow transitions of the comparator.
$CompControl) < 3 >= 1$ disables the comparator.

[4]Low voltage differential signaling

$CompControl) < 1 >= 1$ inverts the polarity of the comparator to detect negative signals.

2.1.7 *Pipeline* read/write control

This digital circuit coordinates the read and write operations to the analog memory.

Adjustable parameters (c.f. sect. 6):
Operation mode (bit 2 of *CompControl*)
Trigger latency *Latency*
Dependencies:
Binary readout mode is selected by setting $CompControl) < 2 >= 1$, i.e. the comparator outputs are sampled into the *pipeline*.
For $CompControl) < 2 >= 0$ the front end's analog output is sampled.
Latency adjusts the time (in `clock` cycles) between sampling and trigger for certain data.

2.1.8 *Pipeline* readout amplifier (*pipeamp*)

The *pipeamp* is a sampling charge sensitive amplifier used to retrieve the information sored in the analog memory. It consists of a *folded cascode* amplifier core with a resetable feedback capacitor and a subsequent s&H stage.
Adjustable parameters (c.f. sect. 6):
Readout line reset voltage *Vd*
Source voltage of the pipeline readout amplifier's input transistor *Vdcl*
Pipeline readout amplifier bias *Ipipe*
Voltage buffer bias *Ivoltbuf*
Dependencies:
Vd, *Vdcl* and *Ivoltbuf* affect the stability of the readout baseline.
Ipipe affects speed and gain of the pipeline readout amp.

2.1.9 Multiplexer and current buffer

The multiplexer consists of four parts, which can operate sequentially or in paralell. This way the signal can be switched to 1, 2 or 4 mux output lines. An additional switch in front of the subsequent current buffer allows the transmission of the data with the speed of the mux (when the switch is static) or at *double data rate* (DDR), i.e. $2 \cdot$ `Clock` frequency on 1 or 2 ports (when the switch is operated with *Clock*). Operation of the multiplexer

slower than the sampling *Clock* and daisy-chained readout of two or more chips is also possible.
Adjustable parameters (c.f. sect. 6):
Multiplexer bias current *Isf*
Current buffer bias current *Icurrbuf*
Readout mode and speed *ROControl*
Readout speed *ClockDiv*
Dependencies:
Isf affects the speed and gain of the multiplexer.
Icurrbuf affects the DC offset of the current output buffer.
ROControl selects the readout mode and speed according to figs. 5 and 7.
ClockDiv adjusts the base clock of the multiplexer: $f_{\mathrm{mux}} = \mathtt{Clock}/(ClockDiv+1))$.

2.1.10 Other circuits

The *Beetle* actually has 2 additional channels:
A *test channel* which implements the complete signal chain from the input to the *pipeamp's* output. It can be accessed via several test pads (c.f. tab. 2 and is intended for diagnostic issues.
A *dummy channel* lacking the preamp's input transistor. It is used for on-chip offset compensation by the current buffer.

2.2 Signal definition

A reference number has been assigned to each pad. The numbering starts in the upper left corner of the die (with the analog input pads left) and runs counterclockwise (cf. fig.2). The following tables summarize the signals and explain them. Definition of the different signal classes can be found in sect. 4

Table 2: Signal definition of *Beetle*

Pad No.	Name	Class	Description
		Front Pads	
1	`TestInput`	input	input of testchannel
2 - 5	`VddPre`	pwr input	positive preamplifier supply
6	`AnalogIn<0>`	input	input of channel 0
7	`AnalogIn<1>`	input	input of channel 1
⋮	⋮	⋮	⋮
133	`AnalogIn<127>`	input	input of channel 127
134 - 137	`Gnd`	pwr input	detector ground

Signal definition of *Beetle* – cont. –

Pad No.	Name	Class	Description
Top Pads			
241	`Prebias`	test output	analog probe pad
240	`Prebias1`	test output	analog probe pad
239	`Shabias`	test output	analog probe pad
238	`Shabias1`	test output	analog probe pad
237	`Bufbias`	test output	analog probe pad
236	`TestOutput`	output	frontend output of testchannel
235	`Gnda`	pwr input	negative analog supply
234	`Vdda`	pwr input	positive analog supply
233	`VddComp`	pwr input	positive comparator supply
232	`GndComp`	pwr input	negative comparator supply
231	notCompOut<0>	LVDS output	comparator output channel 0
230	CompOut<0>	LVDS output	comparator output channel 0
229	notCompOut<1>	LVDS output	comparator output channel 1
228	CompOut<1>	LVDS output	comparator output channel 1
227	notCompOut<2>	LVDS output	comparator output channel 2
226	CompOut<2>	LVDS output	comparator output channel 2
225	notCompOut<3>	LVDS output	comparator output channel 3
224	CompOut<3>	LVDS output	comparator output channel 3
223	notCompOut<4>	LVDS output	comparator output channel 4
222	CompOut<4>	LVDS output	comparator output channel 4
221	notCompOut<5>	LVDS output	comparator output channel 5
220	CompOut<5>	LVDS output	comparator output channel 5
219	notCompOut<6>	LVDS output	comparator output channel 6
218	CompOut<6>	LVDS output	comparator output channel 6
217	notCompOut<7>	LVDS output	comparator output channel 7
216	CompOut<7>	LVDS output	comparator output channel 7
215	`VddComp`	pwr input	positive comparator supply
214	`GndComp`	pwr input	negative comparator supply
213	`FifoFull`	CMOS output	indicates full derandomizing buffer
212	`PipeampTestOut`	output	analog probe pad pipeamp output of testchannel
211	`I2CAddrMode`	CMOS input (internal pull-down)	selects between 7-bit and 10-bit I^2C-address (default: 7-bit address)
210	`IOut`	test output	analog probe pad
209	`IRef`	test input	reference current for current source
Bottom Pads			
138	`Gnda`	pwr input	negative analog supply
139	`Vdda`	pwr input	positive analog supply
140	`VddComp`	pwr input	positive comparator supply
141	`GndComp`	pwr input	negative comparator supply
142	`notCompClock`	LVDS input	comparator clock
143	`CompClock`	LVDS input	comparator clock

Signal definition of *Beetle* – cont. –

Pad No.	Name	Class	Description
144	notCompOut<15>	LVDS output	comparator output channel 15
145	CompOut<15>	LVDS output	comparator output channel 15
146	notCompOut<14>	LVDS output	comparator output channel 14
147	CompOut<14>	LVDS output	comparator output channel 14
148	notCompOut<13>	LVDS output	comparator output channel 13
149	CompOut<13>	LVDS output	comparator output channel 13
150	notCompOut<12>	LVDS output	comparator output channel 12
151	CompOut<12>	LVDS output	comparator output channel 12
152	notCompOut<11>	LVDS output	comparator output channel 11
153	CompOut<11>	LVDS output	comparator output channel 11
154	notCompOut<10>	LVDS output	comparator output channel 10
155	CompOut<10>	LVDS output	comparator output channel 10
156	notCompOut<9>	LVDS output	comparator output channel 9
157	CompOut<9>	LVDS output	comparator output channel 9
158	notCompOut<8>	LVDS output	comparator output channel 8
159	CompOut<8>	LVDS output	comparator output channel 8
160	VddComp	pwr input	positive comparator supply
161	GndComp	pwr input	negative comparator supply
162	TrigMon	CMOS output	indicates if pipeline trigger pointer passes column 0
163	WriteMon	CMOS output	indicates if pipeline write pointer passas column 0
164	SDAoutputMode	CMOS input (internal pull-up)	selects between an analog or digital SDA-line delay stage (default: analog stage)
Rear Pads			
208	notT1A	LVDS input/output	Token for address/readout daisy-chain
207	T1A	LVDS input/output	Token for address/readout daisy-chain
206	notT1B	LVDS input/output	Token for address/readout daisy-chain
205	T1B	LVDS input/output	Token for address/readout daisy-chain
204	Vdda	pwr input	positive analog supply
203	Vdda	pwr input	positive analog supply
202	Vdda	pwr input	positive analog supply
201	Vddd	pwr input	positive digital supply
200	Vddd	pwr input	positive digital supply
199	Gnda	pwr input	negative analog supply
198	Gnda	pwr input	negative analog supply
197	Gnda	pwr input	negative analog supply
196	Gndd	pwr input	negative digital supply
195	Gndd	pwr input	negative digital supply

Signal definition of *Beetle* – cont. –

Pad No.	Name	Class	Description
194	`Icurrbuf`	block output	analog probe pad (to be blocked)
193	`Isf`	block output	analog probe pad (to be blocked)
192	`Vdcl`	block output	analog probe pad (to be blocked)
191	`Vd`	block output	analog probe pad (to be blocked)
190	`Ipipe`	block output	analog probe pad (to be blocked)
189	`notError`	CMOS output	on chip error signal
188	`notAnalogOut<0>`	output	analog output channel 0
187	`AnalogOut<0>`	output	analog output channel 0
186	`notAnalogOut<1>`	output	analog output channel 1
185	`AnalogOut<1>`	output	analog output channel 1
184	`notAnalogOut<2>`	output	analog output channel 2
183	`AnalogOut<2>`	output	analog output channel 2
182	`notAnalogOut<3>`	output	analog output channel 3
181	`AnalogOut<3>`	output	analog output channel 3
180	`Reset`	LVDS input	system reset
179	`notReset`	LVDS input	system reset
178	`Testpulse`	LVDS input	test pulse
177	`notTestpulse`	LVDS input	test pulse
176	`DataValid`	LVDS input	indicates presence of valid data on AnalogOut/notAnalogOut
175	`notDataValid`	LVDS input	indicates presence of valid data on AnalogOut/notAnalogOut
174	`Trigger`	LVDS input	trigger
173	`notTrigger`	LVDS input	trigger
172	`Clock`	LVDS input	system clock
171	`notClock`	LVDS input	system clock
170	`SDA`	CMOS input/output (open-drain)	I^2C-bus data port
169	`SCL`	CMOS input	I^2C-bus clock port
168	`T2B`	LVDS input/output	Token for address/readout daisy-chain
167	`notT2B`	LVDS input/output	Token for address/readout daisy-chain
166	`T2A`	LVDS input/output	Token for address/readout daisy-chain
165	`notT2A`	LVDS input/output	Token for address/readout daisy-chain

3 Geometrical specification

The *Beetle*1.1's die size is $(6.1 \times 5.5)\,\mathrm{mm}^2$. It is shown in fig. 2, which also includes the positions and names of the pads. The analog input pads have a pitch of $41.2\,\mu\mathrm{m}$. If no comparator outputs are used, pads on the sides of the chip do not need to be bonded. This allows an overall pitch of 50 µm when mounting the chips side by side. Table 3 gives the exact coordinates of all pads.

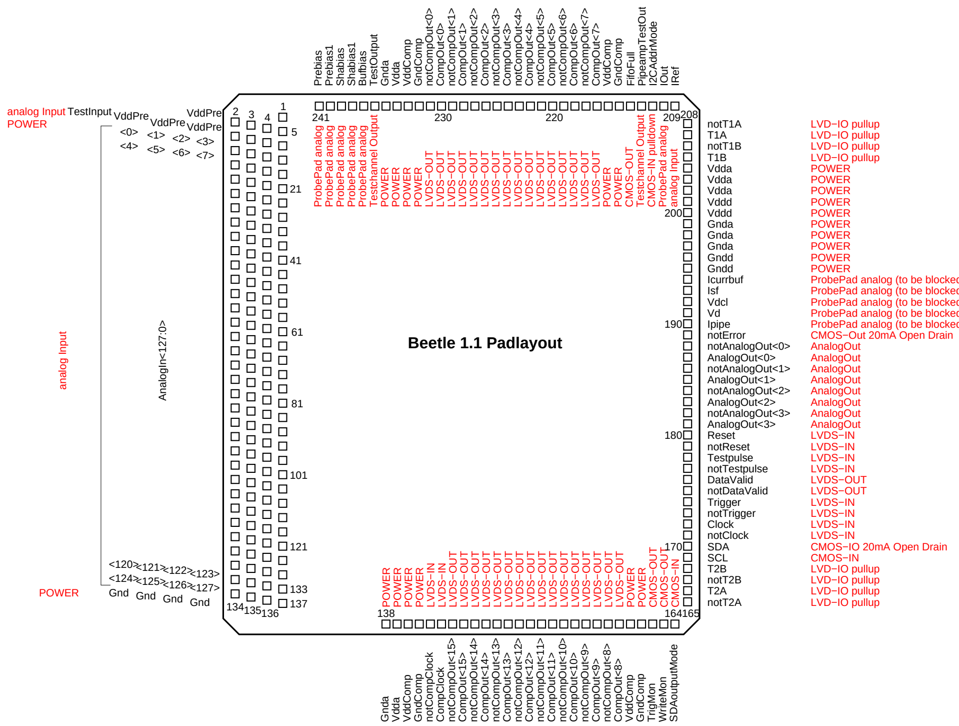


Figure 2: Pad layout of the *Beetle*1.1.

Table 3: *Beetle*1.1 pad positions (top left corner) wrt. to the `TestInput` (top left) pad.

		x [µm]	y [µm]
Pad window		+100	+100
Pad No.	Name	x [µm]	y [µm]
1	`TestInput`	0	0

4 DC characteristics

Tables 4 and 5 specify the DC characteristics *Beetle*'s signal and power connections.

Table 4: DC characteristics of *Beetle1.1*: Signal class *pwr input*

Supply	Min.[V]	Nom.[V]	Max. [V]	Max. [mA]	Description
Vdda	2.2	2.5	2.7	???	Positive analog supply
Gnda	0	0	0	???	Negative analog supply
Vddd	2.2	2.5	2.7	???	Positive digital supply
Gndd	0	0	0	???	Negative digital supply
VddPre	2.2	2.5	2.7	???	Positive preamplifier supply
Gnd	0	0	0	???	Detector ground
VddComp	2.2	2.5	2.7	???	Positive comparator output supply
GndComp	0	0	0	???	Negative comparator output supply

Table 5: DC characteristics of *Beetle1.1*: Other classes

Class	Min.	Nom.	Max.	Description
input	0	n.a.	Vdd	Preamplifier input, it should not carry a DC-current (leakage currents of a few nA are premitted)
test input	0	0	???	Test input to override the 100µA current of the internal reference current source
output	0	920µA	n.a.	Analog output of the chip. It delivers a current to Vss
test output	0	n.a.	Vdd	Test outputs of various stages, usually $Z \gg 10\mathrm{k}\Omega$
block output	0	n.a.	Vdd	Outputs of various stages. To be individually blocked to Vssa with about 100nF
LVDS input	???	1.2V	???	Differential voltage input. sensitivity $\leq$ 100mV. No 150Ω termination
LVDS output	???	1.2V	???	Signal is a differential current of 2mA
LVDS input/output	???	1.2V	???	Bidirectional signal as specified for LVDS input and LVDS output
CMOS input	0	n.a.	Vdd	High-Z voltage input. transition levels are $\approx$ 2/3 Vdd (L$\rightarrow$H) and $\approx$ 1/3 Vdd (H$\rightarrow$L). Internal pull-ups or pull-downs are $\geq$ 10kΩ towards Vdd or Vss respectively.
CMOS output	0	n.a.	Vdd	Voltage output with 4mA maximum driving capability
CMOS input/output	0	n.a.	Vdd	CMOS-input (w/o pull-up or pull-down) with open drain transistor output capable of sinking 4mA

5 AC characteristics

The readout timing behaviour is depicted in fig. 3.

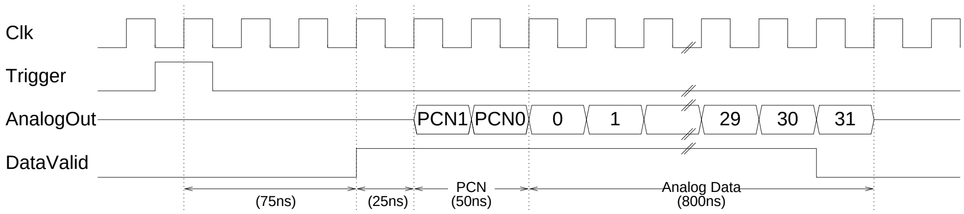


Figure 3: Readout timing scheme.

The AC characteristics define the timing of all signals.

6 Setup and slow control

The *Beetle*'s setup and slow control is completely register based. Access to these registers is via a standard I^2C-interface.

6.1 Programming interface

The chip's slow control interface is a standard mode I^2C-slave device performing a transfer rate of 100kbit/s. The chip address, necessary to access a single device via the I^2C-bus, is assigned in a self-programming procedure on power-up using a daisy-chain of several chips (cf. section 6.3.1).

The internal registers are being accessed via a *pointer register*. This contains the address of the register to be written or read first. The pointer is internally incremented by 1 after each transferred data frame. In this way registers with adjacent addresses can be accessed consecutively. The pointer register itself remains unchanged, i.e. a new transfer will start at the same pointer position. Fig. 4 explains the transfer sequences in write and read mode. Data is always transferred with the most significant bit (MSB) first. In write mode the chip address is transmitted after initializing the transfer, followed by the pointer byte and the data. After the transmission of one data frame, the pointer addresses the successive register because of its auto-incrementing function. A 10 bit register allocates 2 addresses in the address space. The MSBs (D[9:2]) occupy the lower address (cf. table 6). The transfer of the pointer byte is obligatory in write mode. In read mode there are two versions:

- Preset pointer
  After initializing the transfer and sending the chip address data is immediately read out. The pointer has been set in a previous transfer.

- Pointer set followed by immediate read-out
  After initializing the transfer and sending the chip address the pointer byte is transferred. The I^2C-bus is re-initialized, the chip address is sent and data is read out.

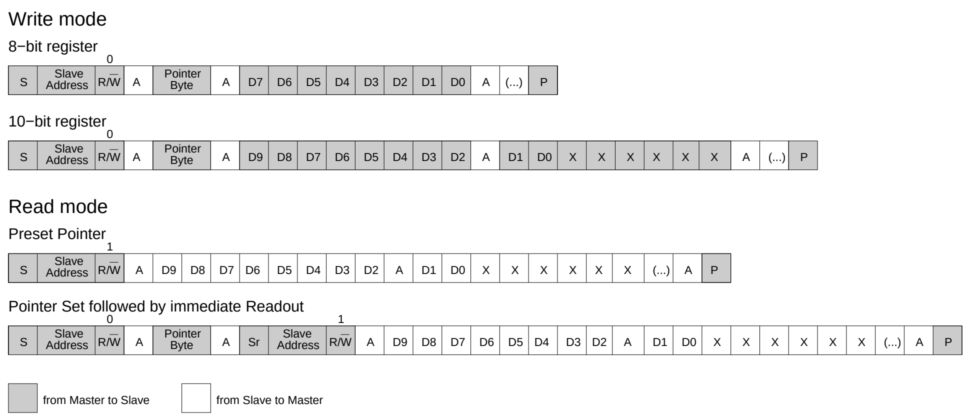
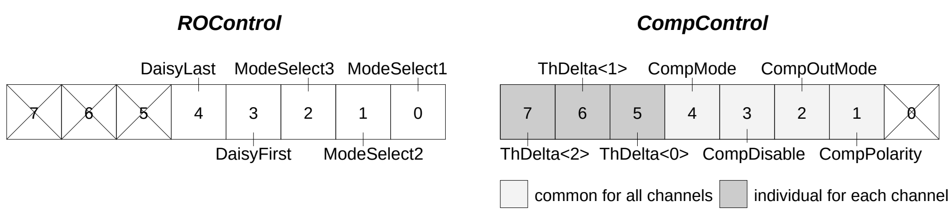


Figure 4: I^2C-bus write and read sequences for accessing registers on the *Beetle*.

6.2 Register map

*Beetle*1.1 contains 34 8-bit registers with the addresses 0-32 and 37. The register addresses 33-36 are presently not used but reserved for future purposes. Table 6 lists all registers with their nominal value and register content. A LSB corresponds to 0.977 µA for currents and 2.44 mV for voltages. Registers 0-29 are bias registers for the analog stages. Register 30 defines the latency, register 32 the ratio between the readout clock `Rclk` and the sampling clock `Sclk`. Each LSB reduces the frequency of `Rclk` with respect to `Sclk` by a factor of 2. The register value is modulo 8, a 0 means, that `Sclk` and `Rclk` have the same frequency. The registers 31 and 37 select the chip's mode of operation (readout mode, daisy-chain configuration) and define the comparator configuration. Fig. 5 shows the detailed bit assignment of the registers *ROControl* and *CompControl*.



DaisyFirst: first in daisychain
DaisyLast: last in daisychain
ModeSelect1: analog readout on 4 ports
ModeSelect2: analog readout on 1 port
ModeSelect3: binary readout on 2 ports

ThDelta<2:0>: delta threshold
CompMode: 1: pulse mode 0: track mode
CompDisable: 1: disables comparator
CompOutMode: 1: binary readout 0: analog readout
CompPolarity: 1: inverting 0: non−inverting

Figure 5: Bit assignment of the configuration registers *ROControl* and *CompControl*. All switches are active-high. 1 enables the switch, 0 disables it.

Table 6: Bias and configuration registers of *Beetle*1.1. Register addresses 33-36 are presently not used but reserved for future purposes.

Register Address	Register Name	Nominal Value	Register content
0	Ithdelta MSBs		0x00
1	Ithdelta LSBs	3.2 µA	0xC0
2	Ithmain MSBs		0x01
3	Ithmain LSBs	4 µA	0x00
4	Icomp MSBs		0x0A
5	Icomp LSBs	40 µA	0x80
6	Ibuf MSBs		0x14
7	Ibuf LSBs	80 µA	0x80
8	Isha MSBs		0x14
9	Isha LSBs	80 µA	0x80
10	Ipre MSBs		0x99
11	Ipre LSBs	600 µA	0x80
12	Itp MSBs		0x00
13	Itp LSBs	0 µA	0x00
14	Vfs MSBs		0x33
15	Vfs LSBs	500 mV	0x40
16	Vfp MSBs		0x00
17	Vfp LSBs	0 V	0x00
18	Icurrbuf MSBs		0x19
19	Icurrbuf LSBs	100 µA	0x80
20	Isf MSBs		0x33
21	Isf LSBs	200 µA	0x40
22	Ipipe MSBs		0x19
23	Ipipe LSBs	100 µA	0x80
24	Ivoltbuf MSBs		0x99
25	Ivoltbuf LSBs	600 µA	0x80
26	Vdcl MSBs		0x66
27	Vdcl LSBs	1 V	0x80
28	Vd MSBs		0x70
29	Vd LSBs	1.1 V	0xC0
30	Latency	160	0xA0
31	ROControl	cf. fig 5	0x19
32	RclkDivider	0	0x00
37	CompControl	cf. fig 5	0x04

6.3 Operation of sampling and readout

6.3.1 Daisy-chain connection

The token ports `T1A`, `T1B`, `T2A`, and `T2B` handle two tasks:

1. They form a daisy chain for generating the chip address for programming via the I^2C-interface.

2. They form a daisy chain for the read-out.

The daisy chain is built by connecting the `T1A` port to the `T2A` port of the neighbouring chip and connecting the `T1B` port to the `T2B` port of the next but the neighbouring chip (see fig. 6). The latter is used to overcome non-adjacent dead chips. Address generation is initiated by with the `Reset` signal and to `Clock`(i.e. `Clock` should not be active during power-on).

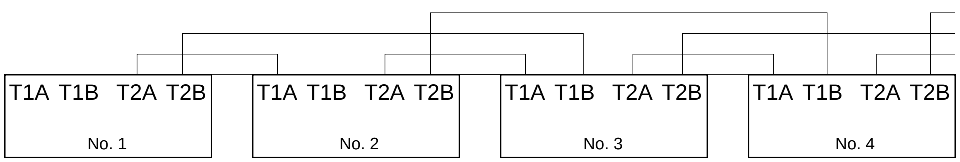


Figure 6: Connection scheme of *Beetle* chips in a daisy-chain.

6.4 Setup and readout modes

Now the bias and configuration registers must be set to the desired values. Especially *CompControl, ROControl, Latency and ClockDiv* registers must be set to the appropriate values to ensure the correct operation of the *Beetle*'s control circuits.

6.5 Comparator operation

Enabling the comparators ($CompControl< 3 >= 0$) in transient mode ($CompControl< 4 >= 0$) will immediately switch the `Compout`$< 0,16 >$ (and `notCompout`$< 0,16 >$) LVDS pads to the channel's comparator outputs according to tab. 7. If $CompControl< 4 >= 0$, the output of the channel comparators is sampled upon the rising edge of `CompClock`. Again the signals are present at the `Compout`$< 0,16 >$ (and `notCompout`$< 0,16 >$) outputs according to tab. 7.

Table 7: Mapping of analog input channels to comparator output channels on *Beetle*

CompOut No.	High phase of Clk	Low phase of Clk
CompOut[15]	Ch[127], Ch[126], Ch[125], Ch[124]	Ch[123], Ch[122], Ch[121], Ch[120]
CompOut[14]	Ch[119], Ch[118], Ch[117], Ch[116]	Ch[115], Ch[114], Ch[113], Ch[112]
CompOut[13]	Ch[111], Ch[110], Ch[109], Ch[108]	Ch[107], Ch[106], Ch[105], Ch[104]
CompOut[12]	Ch[103], Ch[102], Ch[101], Ch[100]	Ch[99], Ch[98], Ch[97], Ch[96]
CompOut[11]	Ch[95], Ch[94], Ch[93], Ch[92]	Ch[91], Ch[90], Ch[89], Ch[88]
CompOut[10]	Ch[87], Ch[86], Ch[85], Ch[84]	Ch[83], Ch[82], Ch[81], Ch[80]
CompOut[9]	Ch[79], Ch[78], Ch[77], Ch[76]	Ch[75], Ch[74], Ch[73], Ch[72]
CompOut[8]	Ch[71], Ch[70], Ch[69], Ch[68]	Ch[67], Ch[66], Ch[65], Ch[64]
CompOut[7]	Ch[63], Ch[62], Ch[61], Ch[60]	Ch[59], Ch[58], Ch[57], Ch[56]
CompOut[6]	Ch[55], Ch[54], Ch[53], Ch[52]	Ch[51], Ch[50], Ch[49], Ch[48]
CompOut[5]	Ch[47], Ch[46], Ch[45], Ch[44]	Ch[43], Ch[42], Ch[41], Ch[40]
CompOut[4]	Ch[39], Ch[38], Ch[37], Ch[36]	Ch[35], Ch[34], Ch[33], Ch[32]
CompOut[3]	Ch[31], Ch[30], Ch[29], Ch[28]	Ch[27], Ch[26], Ch[25], Ch[24]
CompOut[2]	Ch[23], Ch[22], Ch[21], Ch[20]	Ch[19], Ch[18], Ch[17], Ch[16]
CompOut[1]	Ch[15], Ch[14], Ch[13], Ch[12]	Ch[11], Ch[10], Ch[9], Ch[8]
CompOut[0]	Ch[7], Ch[6], Ch[5], Ch[4]	Ch[3], Ch[2], Ch[1], Ch[0]

6.6 Pipelined readout operation

Either binary data from the comparator outputs (in case of $CompControl< 2 >= 1$) or the frontend's analog output ($CompControl< 2 >= 0$) is sampled for pipelined readout. The sampling of channel data into the analog memory occurs on the rising edge of `clock`. To initialize this operation and to adjust the chips *latency*, `Reset` has to be activated for at least one `Clock` cycle. `Reset` will invalidate all entries of the analog memory as well as of the derandomizer buffer for pending readouts. It also terminates any readout in progress. Upon release of `Reset`, data is written into column 0 of the pipeline. *Latency* `Clock` cycles after a certain data has been sampled, a high `trigger` input during the rising edge of `Clock` will mark this data for readout. If there are no pending triggers, the readout burst will start 5 (???)`Clock` cycles later. Readout clock speed and data format will depend on the choosen readout mode ($ROControl< 2, 0 >$), as shown in fig. 7. If daisy-chained readout is selected ($ROControl< 4, 3 >= 0b01$ for the first, $ROControl< 4, 3 >= 0b10$ for the last chip in the chain and $ROControl< 4, 3 >= 0b00$ for all chips in between), the data burst of the subsequent chip in the chain will immediatelly start after the preceeding one has finished. Under certain circumstances, it can take up to 186 (???)

`Clock` cycles after the readout of a certain data started, until it is discarded from the buffer for pending readouts.

7 Application notes

7.0.1 I^2C level shifter

Commercially available I^2C-devices usually operate at 3.3 V or 5 V. To interconnect these devices with a *Beetle* I^2C-interface a bidirectional level shifter is necessary. A simple solution to this problem is the use of a discete MOS-FET for each bus line [4]. Fig. 8 illustrates the level shifter circuit. An example for a single MOS-FET device is type BSN20 from Philips Semiconductors.

7.0.2 Analog current receiver

The output level of the analog output driver is 46 mV $\pm$ 2.8 mV/MIP measured over 56 Ω to ground. Fig. 9 gives an example of a receiver circuit.

References

[1] N. van Bakel, D. Baumeister et al., The *Beetle* Reference Manual, CERN LHCb 2001-046

[2] R. Brenner et al., Nucl. Instr. and Meth. A339 (1994) 564

[3] The I^2C-bus and how to use it, Philips Semiconductors, 1995

[4] Bi-directional level shifter for I^2C-bus and other systems, Application Note AN97055, Philips Semiconductors, 1998

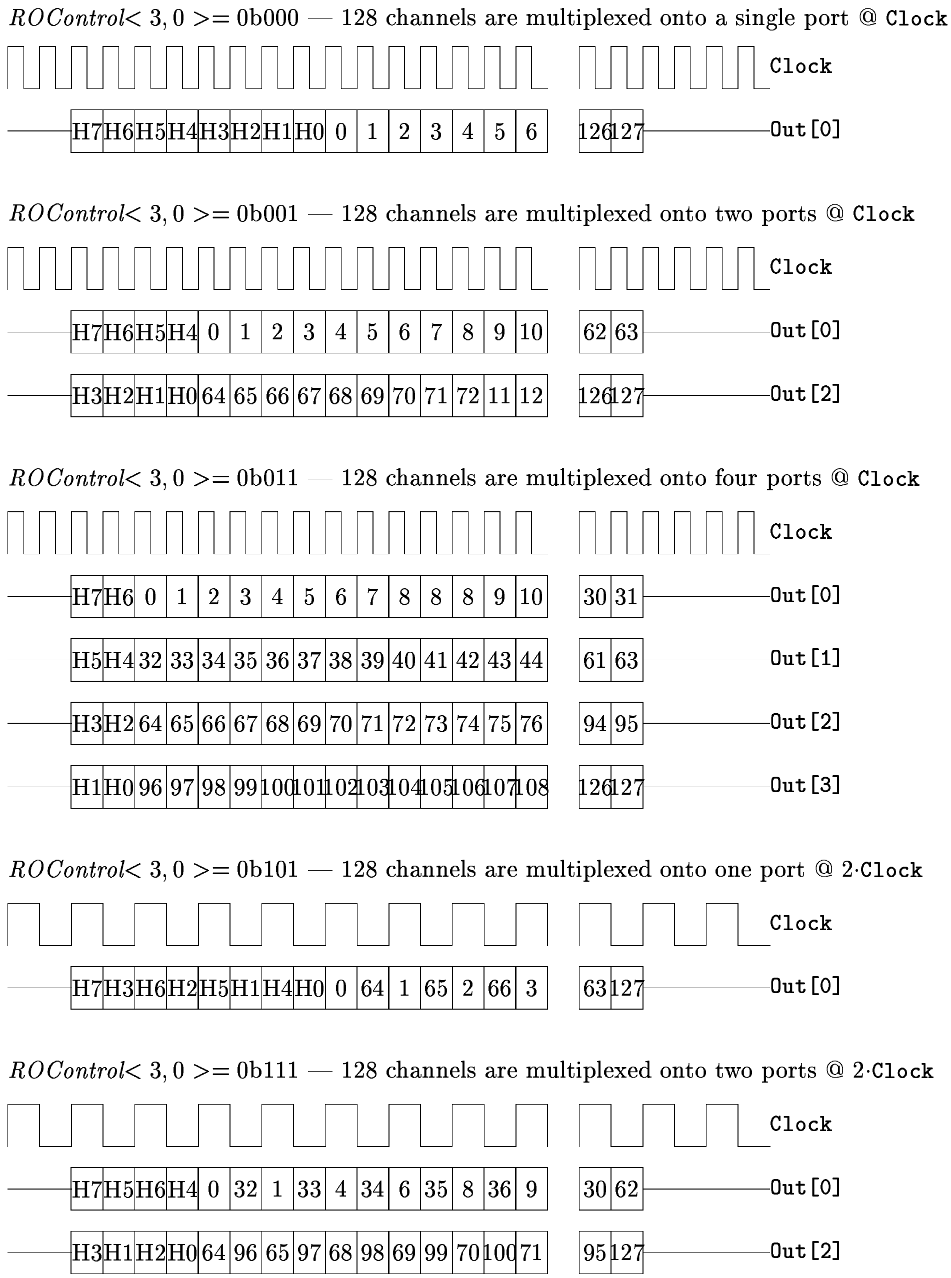


Figure 7: Readout modes of the *Beetle*

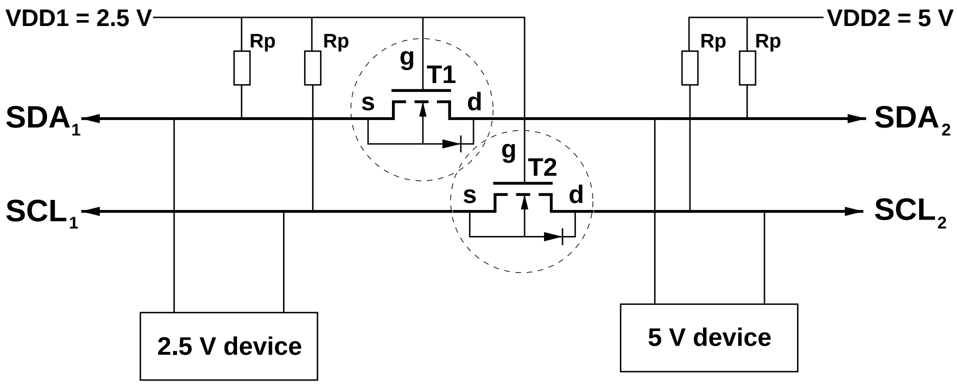


Figure 8: Bidirectional level shifter circuit to connect two different voltage level sections of an I^{2}C-bus system. An example for a single MOS-FET device is type BSN20 from Philips Semiconductors.

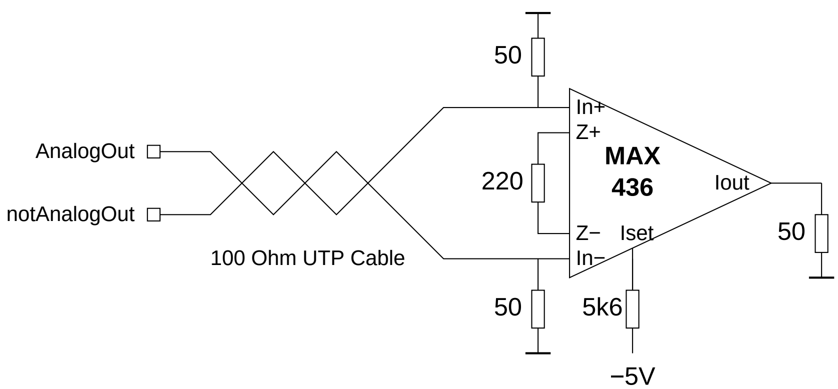


Figure 9: Example of a receiver circuit for the analog output signals.