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The Beetle Reference Manual

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v1.0

Abstract

This paper details the port definitions, electrical specifications, modes of operation and programming sequences of the 128 channel readout chip *Beetle*. The chip is developed for the LHCb experiment and fulfills the requirements of the silicon vertex detector, the inner tracker, the pile-up veto trigger and the RICH detector in case of multianode photomultiplier readout. It integrates 128 channels with low-noise charge-sensitive preamplifiers and shapers. The risetime of the shaped pulse is 25 ns with a 30% remainder of the peak voltage after 25 ns. A comparator per channel with configurable polarity provides a binary signal. Four adjacent comparator channels are being ORed and brought off chip via LVDS ports. Either the shaper or comparator output is sampled with the LHC-bunch-crossing frequency of 40 MHz into an analogue pipeline with a programmable latency of max. 160 sampling intervalls and an integrated derandomizing buffer of 16 stages. For analog readout data is multiplexed with up to 40 MHz onto 1 or 4 ports. A binary readout mode operates at up to 80 MHz output rate on two ports. Current drivers bring the serialized data off chip. The chip can accept trigger rates of up to 1 MHz to perform a deadtimeless readout within 900 ns per sample. For testability and calibration purposes, a charge injector with adjustable pulse height is implemented. The bias settings and various other parameters can be controlled via a standard I^2C-interface.

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1 Document Edition History

This manual describes the chip versions 1.0 and 1.1. It refers to *Beetle1.1* unless otherwise noted.

Version	Date	Author	Description
1.0	22.04.2001	DB, SL	document created

2 Chip Version History

Version	Submission Date	Changes relating to previous version
Beetle1.0	April 2000	
Beetle1.1	March 2001	testchannel extended till pipeline readout amplifier (pipeamp) output modified pipline layout analog delay element for I^2C-SDA line added modified pipeamp modified bias network of pipeamp modified multiplexer modified tristate buffer in control circuit

3 Chip Architecture

The *Beetle* can be operated as analogue or alternatively as binary pipelined readout chip. It implements the basic RD20 frontend electronics architecture [1]. Figure 1 shows a schematic block diagram of the chip.

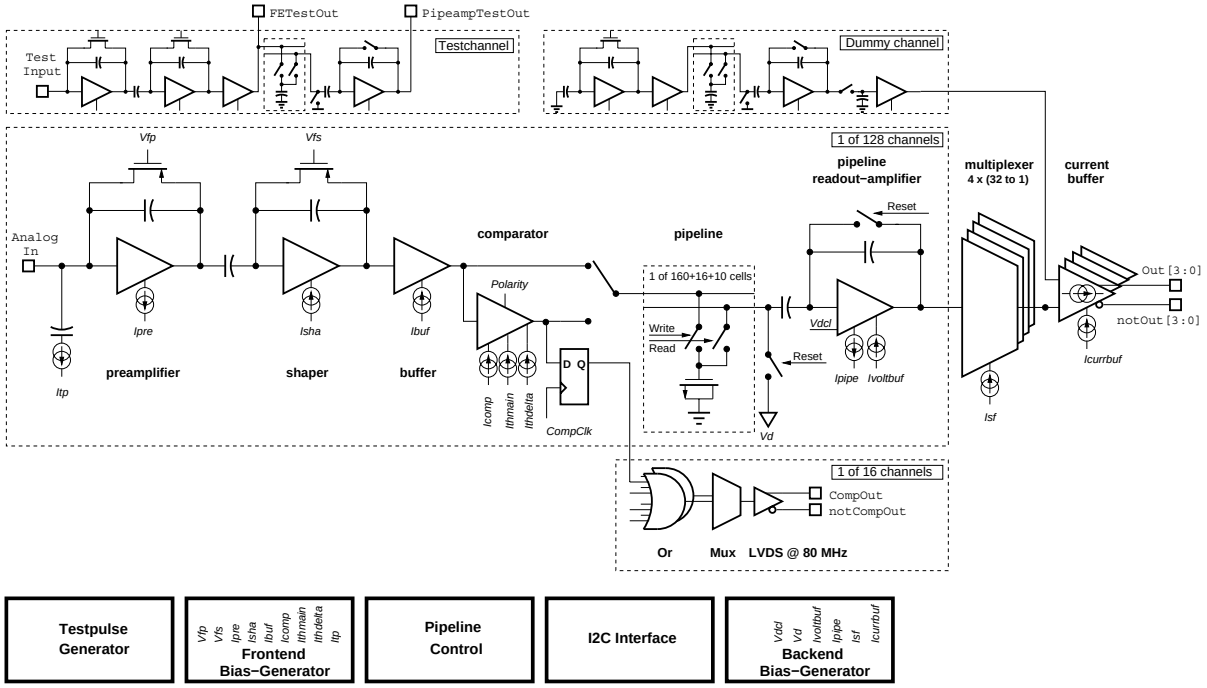

Figure 1: Schematic block diagram of the *Beetle* readout chip.

The chip integrates 128 channels. Each channel consists of a low-noise charge-sensitive preamplifier and an active CR-RC pulse shaper. The risetime of the shaped pulse is ≤ 25 ns, the spill-over left 25 ns after the peak at most 30%. A comparator per channel provides a binary signal. It features a configurable polarity and an individual threshold level. Four adjacent comparator channels are ORed together, latched, multiplexed by a factor of 2 and routed off the chip via low voltage differential signaling (LVDS) ports at 80 MHz. Either the shaper- or the comparator output is sampled with the LHC bunch-crossing frequency at 40 MHz into an analogue pipeline with a programmable latency of max. 160 sampling intervals and an integrated multi-event buffer of 16 stages. The signal stored in the pipeline is transfered to the multiplexer via a resetable charge-sensitive amplifier. Within a readout time of 900 ns current drivers

bring the serialized data off chip. The output of a dummy channel is subtracted from the analogue data to compensate common mode effects. All amplifier stages are biased by forced currents. On-chip digital-to-analogue converters (DACs) with 10 bit resolution generate the bias currents and voltages. For test and calibration purposes a charge injector with adjustable pulse height is implemented on each channel. The bias settings and various other parameters like the trigger latency can be controlled via a standard I^2C-interface [2]. All digital control and data signals, except those for the I^2C-ports, are routed via LVDS ports.

The chip is fabricated in 0.25 μm standard CMOS technology and has a die size of 6.1×5.5 mm^2. The analogue input pads have a pitch of 41.2 μm. If no comparator outputs are used, pads on the sides of the chip do not need to be bonded. This allows an overall pitch of 50 μm when mounting the chips side by side.

4 Electrical specifications

4.1 DC characteristics

Supply	Min.[V]	Nom.[V]	Max. [V]	Description
Vdda	2.2	2.5	2.7	Positive analogue supply
Gnda	0	0	0	Negative analogue supply
Vddd	2.2	2.5	2.7	Positive digital supply
Gndd	0	0	0	Negative digital supply
VddPre	2.2	2.5	2.7	Positive preamplifier supply
Gnd	0	0	0	Detector ground
VddComp	2.2	2.5	2.7	Positive comparator output supply
GndComp	0	0	0	Negative comparator output supply

Table 1: DC characteristics of *Beetle1.1*

4.2 Analog output characteristics

The output level of the analog output driver is 46 mV ± 2.8 mV/MIP measured over 56 Ω to ground. Fig. 2 gives an example of a receiver circuit.

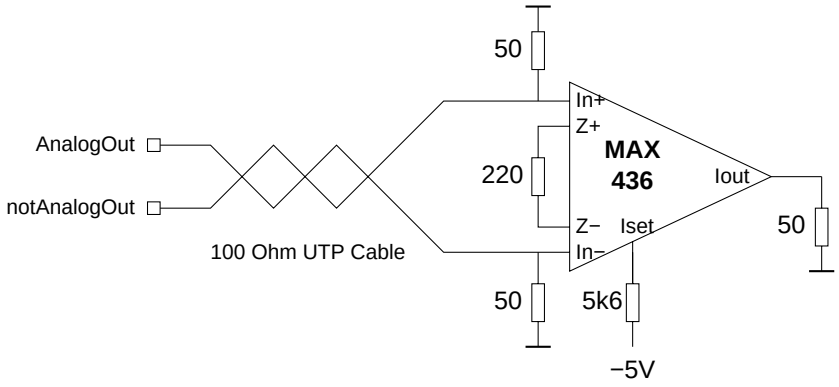

Figure 2: Example of a receiver circuit for the analog output signals.

5 Modes of operation

5.1 Reset modes

Two different types of reset exist on *Beetle1.0* and *Beetle1.1*, which are differentiated by the duration of the active external reset with respect to the system clock.

- Readout reset (cf. fig.3 a))
  It is generated by activating `Reset` for exactly 2 `Clock` cycles. It resets the Write- and Trigger pointers of the pipeline, removes all entries from the read-out fifo and stops any running read-out process immediately. The data currently submitted is lost.

- Power up reset (cf. fig.3 b))
  It is generated by activating `Reset` for 4 `Clock` cycles or longer. It resets all internal registers to default values. E. g. the DAC registers for the bias currents are set to 0 (no current). This is mainly to reduce power consumption during power up. Power up reset also switches the Beetle into the "Idle" state, i. e. the write pointer and the trigger pointer do not circulate and no triggers are accepted.

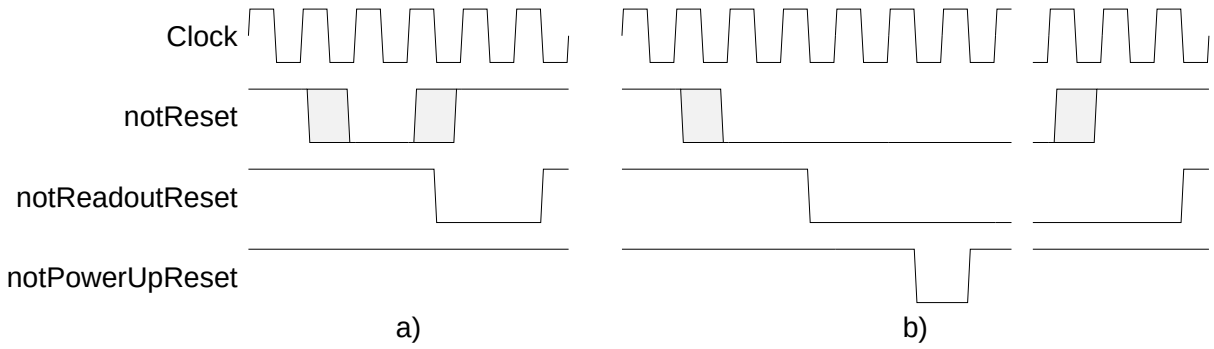

Figure 3: Types of reset on *Beetle1.1*: a) Readout reset, b) Power up reset

5.2 Readout modes

Beetle1.1 provides three different readout modes:

1. Analogue readout in 900 ns on 4 ports
2. Binary readout in 900 ns on 2 ports
3. Analogue readout on 1 port (for applications with less demanding readout speed requirements).

Fig. 4 - 6 show the assignment of the header bits and analog input channels to the output channels in the different modes.

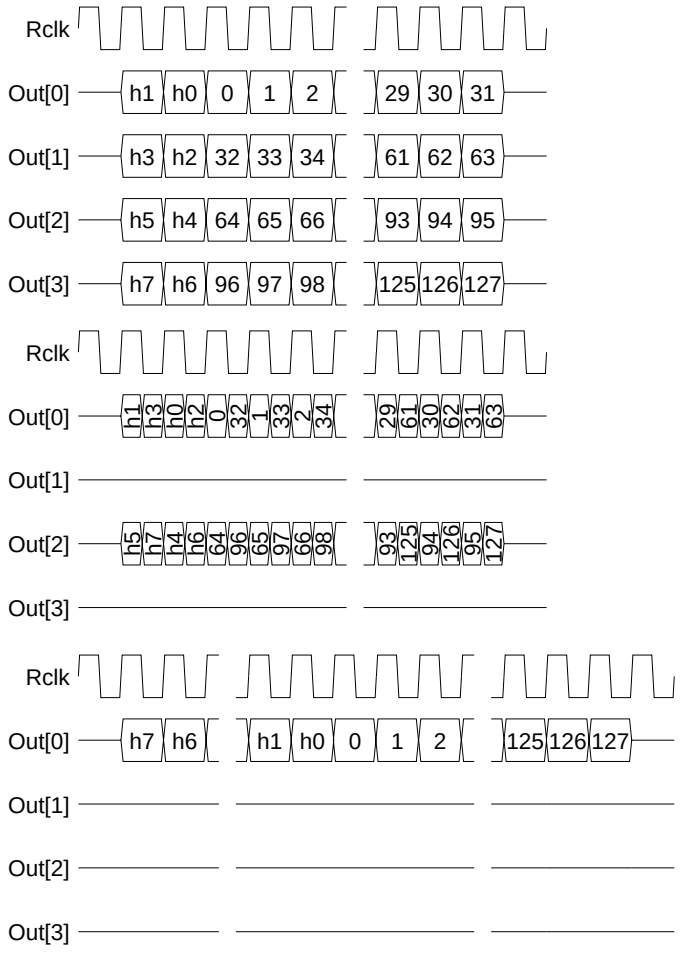

Figure 4: Analog readout mode: 32 analog channels are multiplexed onto 4 ports with up to 40 MHz.

Figure 5: Binary readout mode: 64 binary channels are multiplexed onto 2 ports with up to 80 MHz.

Figure 6: Readout mode for less demanding readout speed requirements: 128 analog channels are multiplexed onto 1 port with up to 40 MHz.

The readout timing behaviour is depicted in fig. 7.

5.3 Operation in daisychain

The token ports `T1A`, `T1B`, `T2A`, and `T2B` handle two tasks:

1. They form a daisy chain for generating the chip address for programming via the I^2C-interface.
2. They form a daisy chain for the read-out.

The daisy chain is built by connecting the `T1A` port to the `T2A` port of the neighbouring chip and connecting the `T1B` port to the `T2B` port of the next but the neighbouring chip (see fig. 8).

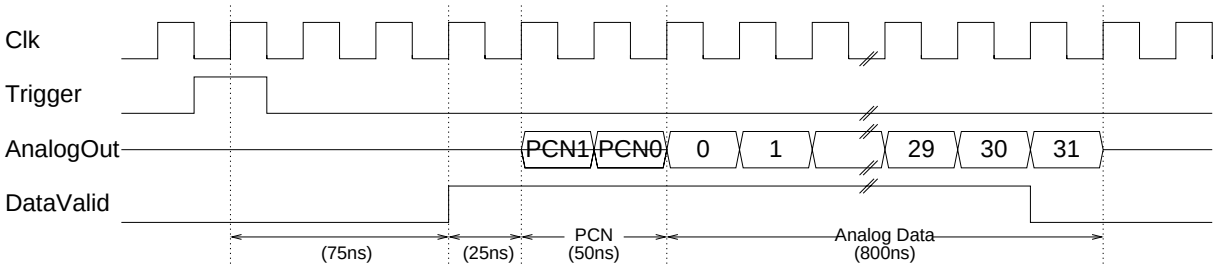

Figure 7: Readout timing scheme.

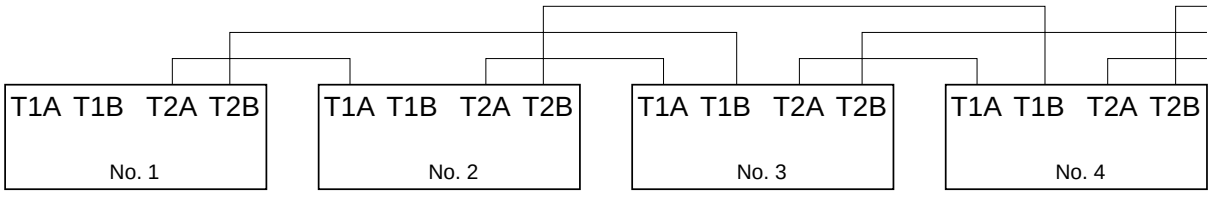

Figure 8: Connection scheme of *Beetle* chips in a daisychain.

5.4 Comparator operation

The comparator circuit consists of an integrator, a threshold generator and a discriminator. The integrator extracts the DC-offset of the shaped pulse with a time constant of 5 μs. This offset varies from channel to channel and is added to the threshold voltage. The threshold level is adjustable per channel with a resolution of 3 bits.

5.4.1 Comparator configuration

The comparator is configured via the register *CompControl* (see table 3 and fig. 11). *CompOutMode* defines the mode of operation of the comparator. *CompOutMode*=0 selects the analog mode, in which the output of the frontend amplfier is transferred to the pipeline. In binray mode (*CompOutMode*=1) the comparator output is fed into the pipeline. *CompDisable*=1 turns off the comparator's bias current. *CompPolarity* selects between an inverting (1) or non-inverting (0) comperator operation. *CompMode* switches between two different kinds of output signal. With *CompMode*=0 the output is as long active as the comparator input signal is above the threshold level. With *CompMode*=1 the output is only one CompClk cycle active, independent of the time, which the input signal is above the threshold.

5.4.2 Threshold adjustment

The threshold level is generated from two programmable currents. *Ithmain* (register addresses 2 and 3) determines the global threshold, which is common to all channels. *Ithdelta* (register addresses 0 and 1) defines an additional delta voltage. The 3 MSBs of the configuration register *CompControl* ThDelta[2:0] (fig. 11) select the number of delta voltages which are being added to the global threshold voltage.

5.4.3 Comparator channel mapping

The comparator outputs are LVDS drivers. Each driver sends data of two combined comparator groups, the first group during the high phase of `Clk`, the second during the low phase. The mapping of the channels to the comparator outputs is shown in table 2.

CompOut No.	High phase of Clk	Low phase of Clk
CompOut[15]	Ch[127], Ch[126], Ch[125], Ch[124]	Ch[123], Ch[122], Ch[121], Ch[120]
CompOut[14]	Ch[119], Ch[118], Ch[117], Ch[116]	Ch[115], Ch[114], Ch[113], Ch[112]
CompOut[13]	Ch[111], Ch[110], Ch[109], Ch[108]	Ch[107], Ch[106], Ch[105], Ch[104]
CompOut[12]	Ch[103], Ch[102], Ch[101], Ch[100]	Ch[99], Ch[98], Ch[97], Ch[96]
CompOut[11]	Ch[95], Ch[94], Ch[93], Ch[92]	Ch[91], Ch[90], Ch[89], Ch[88]
CompOut[10]	Ch[87], Ch[86], Ch[85], Ch[84]	Ch[83], Ch[82], Ch[81], Ch[80]
CompOut[9]	Ch[79], Ch[78], Ch[77], Ch[76]	Ch[75], Ch[74], Ch[73], Ch[72]
CompOut[8]	Ch[71], Ch[70], Ch[69], Ch[68]	Ch[67], Ch[66], Ch[65], Ch[64]
CompOut[7]	Ch[63], Ch[62], Ch[61], Ch[60]	Ch[59], Ch[58], Ch[57], Ch[56]
CompOut[6]	Ch[55], Ch[54], Ch[53], Ch[52]	Ch[51], Ch[50], Ch[49], Ch[48]
CompOut[5]	Ch[47], Ch[46], Ch[45], Ch[44]	Ch[43], Ch[42], Ch[41], Ch[40]
CompOut[4]	Ch[39], Ch[38], Ch[37], Ch[36]	Ch[35], Ch[34], Ch[33], Ch[32]
CompOut[3]	Ch[31], Ch[30], Ch[29], Ch[28]	Ch[27], Ch[26], Ch[25], Ch[24]
CompOut[2]	Ch[23], Ch[22], Ch[21], Ch[20]	Ch[19], Ch[18], Ch[17], Ch[16]
CompOut[1]	Ch[15], Ch[14], Ch[13], Ch[12]	Ch[11], Ch[10], Ch[9], Ch[8]
CompOut[0]	Ch[7], Ch[6], Ch[5], Ch[4]	Ch[3], Ch[2], Ch[1], Ch[0]

Table 2: Mapping of analog input channels to comparator output channels on *Beetle1.1*

6 Slow Control

6.1 I²C-Interface

The chip's slow control interface is a standard mode I²C-slave device performing a transfer rate of 100 kbit/s. The chip address, necessary to access a single device via the I²C-bus, is assigned in a self-programming procedure on power-up using a daisychain of several chips (cf. section 5.3).

The internal registers are being accessed via a *pointer register*. This contains the address of the register to be written or read first. The pointer is internally incremented by 1 after each transferred data frame. In this way registers with adjacent addresses can be accessed consecutively. The pointer register itself remains unchanged, i.e. a new transfer will start at the same pointer position. Fig. 9 explains the transfer sequences in write and read mode. Data is always transferred with the most significant bit (MSB) first. In write mode the chip address is transmitted after initializing the transfer, followed by the pointer byte and the data. After the transmission of one data frame, the pointer addresses the successive register because of its auto-incrementing function. A 10 bit register allocates 2 addresses in the address space. The MSBs (D[9:2]) occupy the lower address (cf. table 3). The transfer of the pointer byte is obligatory in write mode. In read mode there are two versions:

- Preset pointer
  After initializing the transfer and sending the chip address data is immediately read out. The pointer has been set in a previous transfer.
- Pointer set followed by immediate read-out
  After initializing the transfer and sending the chip address the pointer byte is transferred. The I²C-bus is re-initialized, the chip address is sent and data is read out.

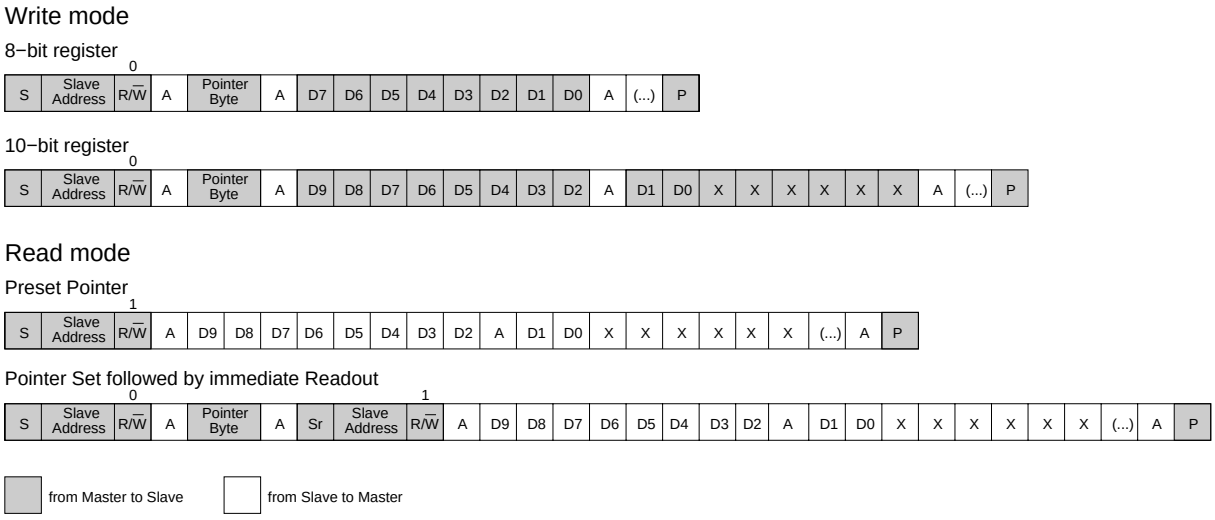

Figure 9: I²C-bus write and read sequences for accessing registers on the *Beetle*.

Commercially available I²C-devices usually operate at 3.3 V or 5 V. To interconnect these devices with a *Beetle* I²C-interface a bidirectional level shifter is necessary. A simple solution to this problem is the use of a discete MOS-FET for each bus line [3]. Fig. 10 illustrates the level shifter circuit. An example for a single MOS-FET device is type BSN20 from Philips Semiconductors.

6.2 Bias and configuration registers

Beetle1.0 and *Beetle1.1* contain 34 8-bit registers with the addresses 0-32 and 37. The register addresses 33-36 are presently not used but reserved for future purposes. Table 3 lists all registers with their nominal

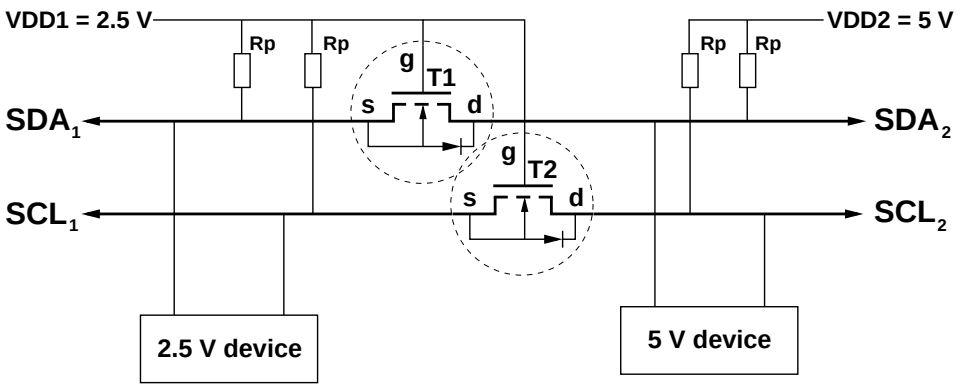

Figure 10: Bidirectional level shifter circuit to connect two different voltage level sections of an I^2C-bus system. An example for a single MOS-FET device is type BSN20 from Philips Semiconductors.

value and register content. A LSB corresponds to 0.977 μA for currents and 2.44 mV for voltages. Registers 0-29 are bias registers for the analog stages. Register 30 defines the latency, register 32 the ratio between the readout clock `Rclk` and the sampling clock `Sclk`. Each LSB reduces the frequency of `Rclk` with respect to `Sclk` by a factor of 2. The register value is modulo 8, a 0 means, that `Sclk` and `Rclk` have the same frequency. The registers 31 and 37 select the chip's mode of operation (readout mode, daisychain configuration) and define the comparator configuration. Fig. 11 shows the detailed bit assignment of the registers *ROControl* and *CompControl*.

DaisyFirst: first in daisychain
DaisyLast: last in daisychain
ModeSelect1: analog readout on 4 ports
ModeSelect2: analog readout on 1 port
ModeSelect3: binary readout on 2 ports

ThDelta<2:0>: delta threshold
CompMode: 1: pulse mode 0: track mode
CompDisable: 1: disables comparator
CompOutMode: 1: binary readout 0: analog readout
CompPolarity: 1: inverting 0: non−inverting

Figure 11: Bit assignment of the configuration registers *ROControl* and *CompControl*. All switches are active-high. 1 enables the switch, 0 disables it.

Register Address	Register Name	Nominal Value	Register content
0	Ithdelta MSBs		0x00
1	Ithdelta LSBs	3.2 μA	0xC0
2	Ithmain MSBs		0x01
3	Ithmain LSBs	4 μA	0x00
4	Icomp MSBs		0x0A
5	Icomp LSBs	40 μA	0x80
6	Ibuf MSBs		0x14
7	Ibuf LSBs	80 μA	0x80
8	Isha MSBs		0x14
9	Isha LSBs	80 μA	0x80
10	Ipre MSBs		0x99
11	Ipre LSBs	600 μA	0x80
12	Itp MSBs		0x00
13	Itp LSBs	0 μA	0x00
14	Vfs MSBs		0x33
15	Vfs LSBs	500 mV	0x40
16	Vfp MSBs		0x00
17	Vfp LSBs	0 V	0x00
18	Icurrbuf MSBs		0x19
19	Icurrbuf LSBs	100 μA	0x80
20	Isf MSBs		0x33
21	Isf LSBs	200 μA	0x40
22	Ipipe MSBs		0x19
23	Ipipe LSBs	100 μA	0x80
24	Ivoltbuf MSBs		0x99
25	Ivoltbuf LSBs	600 μA	0x80
26	Vdcl MSBs		0x66
27	Vdcl LSBs	1 V	0x80
28	Vd MSBs		0x70
29	Vd LSBs	1.1 V	0xC0
30	Latency	160	0xA0
31	ROControl	cf. fig 11	0x19
32	RclkDivider	0	0x00
37	CompControl	cf. fig 11	0x04

Table 3: Bias and configuration registers of *Beetle1.1*. Register addresses 33-36 are presently not used but reserved for future purposes.

7 Pad Description

A reference number has been assigned to each pad. The numbering starts in the upper left corner of the die (with the analog input pads left) and runs counterclockwise (cf. fig.12). The following tables summarize the signals and explain them.

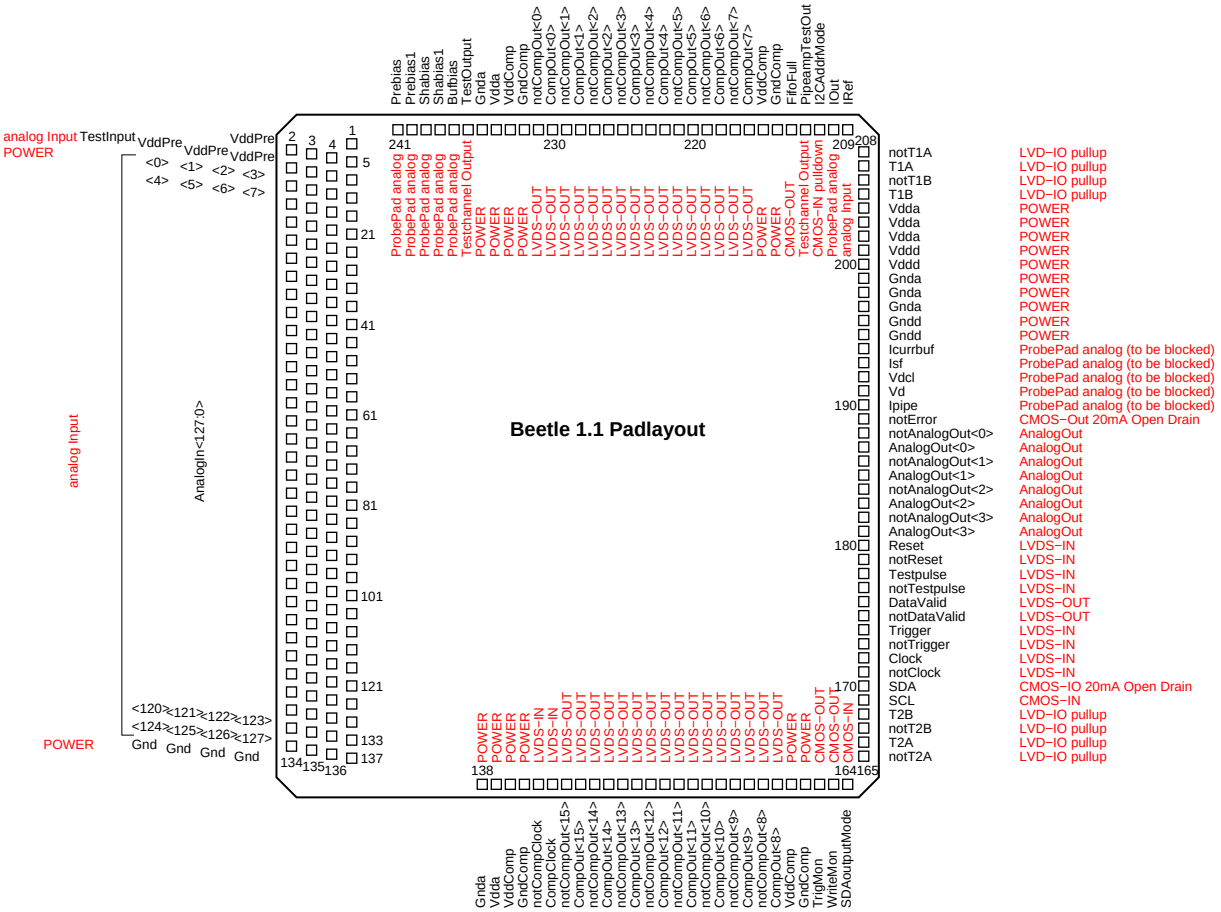

Figure 12: Padlayout of the *Beetle1.1*. The die size is $(6.1 \times 5.5)\,\mathrm{mm}^2$.

7.1 Front pads

Ref.no.	Pin name	Type	Description
1	`TestInput`	input	input of testchannel
2 - 5	`VddPre`	input	positiv preamplifier supply
6	`AnalogIn<0>`	input	input of channel 0
7	`AnalogIn<1>`	input	input of channel 1
⋮	⋮	⋮	⋮
133	`AnalogIn<127>`	input	input of channel 127
134 - 137	`Gnd`	input	detector ground

7.2 Top pads

Ref.no.	Pin name	Type	Description
241	Prebias	output	analog probe pad
240	Prebias1	output	analog probe pad
239	Shabias	output	analog probe pad
238	Shabias1	output	analog probe pad
237	Bufbias	output	analog probe pad
236	TestOutput	output	frontend output of testchannel
235	Gnda	input	negativ analog supply
234	Vdda	input	positiv analog supply
233	VddComp	input	positiv comparator supply
232	GndComp	input	negativ comparator supply
231	notCompOut<0>	LVDS output	comparator output channel 0
230	CompOut<0>	LVDS output	comparator output channel 0
229	notCompOut<1>	LVDS output	comparator output channel 1
228	CompOut<1>	LVDS output	comparator output channel 1
227	notCompOut<2>	LVDS output	comparator output channel 2
226	CompOut<2>	LVDS output	comparator output channel 2
225	notCompOut<3>	LVDS output	comparator output channel 3
224	CompOut<3>	LVDS output	comparator output channel 3
223	notCompOut<4>	LVDS output	comparator output channel 4
222	CompOut<4>	LVDS output	comparator output channel 4
221	notCompOut<5>	LVDS output	comparator output channel 5
220	CompOut<5>	LVDS output	comparator output channel 5
219	notCompOut<6>	LVDS output	comparator output channel 6
218	CompOut<6>	LVDS output	comparator output channel 6
217	notCompOut<7>	LVDS output	comparator output channel 7
216	CompOut<7>	LVDS output	comparator output channel 7
215	VddComp	input	positiv comparator supply
214	GndComp	input	negativ comparator supply
213	FifoFull	CMOS output	indicates full derandomizing buffer
212	PipeampTestOut	output	analog probe pad pipeamp output of testchannel
211	I2CAddrMode	CMOS input (internal pull-down)	selects between 7-bit and 10-bit I^2C-address (default: 7-bit address)
210	IOut	output	analog probe pad
209	IRef	input	reference current for current source

7.3 Bottom pads

Ref.no.	Pin name	Type	Description
138	Gnda	input	negativ analog supply
139	Vdda	input	positiv analog supply
140	VddComp	input	positiv comparator supply
141	GndComp	input	negativ comparator supply
142	notCompClock	LVDS input	comparator clock
143	CompClock	LVDS input	comparator clock
144	notCompOut<15>	LVDS output	comparator output channel 15
145	CompOut<15>	LVDS output	comparator output channel 15
146	notCompOut<14>	LVDS output	comparator output channel 14
147	CompOut<14>	LVDS output	comparator output channel 14
148	notCompOut<13>	LVDS output	comparator output channel 13
149	CompOut<13>	LVDS output	comparator output channel 13
150	notCompOut<12>	LVDS output	comparator output channel 12
151	CompOut<12>	LVDS output	comparator output channel 12
152	notCompOut<11>	LVDS output	comparator output channel 11
153	CompOut<11>	LVDS output	comparator output channel 11
154	notCompOut<10>	LVDS output	comparator output channel 10
155	CompOut<10>	LVDS output	comparator output channel 10
156	notCompOut<9>	LVDS output	comparator output channel 9
157	CompOut<9>	LVDS output	comparator output channel 9
158	notCompOut<8>	LVDS output	comparator output channel 8
159	CompOut<8>	LVDS output	comparator output channel 8
160	VddComp	input	positiv comparator supply
161	GndComp	input	negativ comparator supply
162	TrigMon	CMOS output	indicates if pipeline trigger pointer passas column 0
163	WriteMon	CMOS output	indicates if pipeline write pointer passas column 0
164	SDAoutputMode	CMOS input (internal pull-up)	selects between an analog or digital SDA-line delay stage (default: analog stage)

7.4 Backside pads

Ref.no.	Pin name	Type	Description
208	notT1A	LVDS input/output	Token for address/readout daisychain
207	T1A	LVDS input/output	Token for address/readout daisychain
206	notT1B	LVDS input/output	Token for address/readout daisychain
205	T1B	LVDS input/output	Token for address/readout daisychain
204	Vdda	input	positiv analog supply
203	Vdda	input	positiv analog supply
202	Vdda	input	positiv analog supply
201	Vddd	input	positiv digital supply
200	Vddd	input	positiv digital supply
199	Gnda	input	negativ analog supply
198	Gnda	input	negativ analog supply
197	Gnda	input	negativ analog supply
196	Gndd	input	negativ digital supply
195	Gndd	input	negativ digital supply
194	Icurrbuf	output	analog probe pad (to be blocked)
193	Isf	output	analog probe pad (to be blocked)
192	Vdcl	output	analog probe pad (to be blocked)
191	Vd	output	analog probe pad (to be blocked)
190	Ipipe	output	analog probe pad (to be blocked)
189	notError	CMOS output	on chip error signal
188	notAnalogOut<0>	output	analog output channel 0
187	AnalogOut<0>	output	analog output channel 0
186	notAnalogOut<1>	output	analog output channel 1
185	AnalogOut<1>	output	analog output channel 1
184	notAnalogOut<2>	output	analog output channel 2
183	AnalogOut<2>	output	analog output channel 2
182	notAnalogOut<3>	input	analog output channel 3
181	AnalogOut<3>	input	analog output channel 3
180	Reset	LVDS input	system reset
179	notReset	LVDS input	system reset
178	Testpulse	LVDS input	test pulse
177	notTestpulse	LVDS input	test pulse
176	DataValid	LVDS input	indicates presence of valid data on AnalogOut/notAnalogOut
175	notDataValid	LVDS input	indicates presence of valid data on AnalogOut/notAnalogOut
174	Trigger	LVDS input	trigger
173	notTrigger	LVDS input	trigger
172	Clock	LVDS input	system clock
171	notClock	LVDS input	system clock
170	SDA	CMOS input/output (open-drain)	I^2C-bus data port
169	SCL	CMOS input	I^2C-bus clock port
168	T2B	LVDS input/output	Token for address/readout daisychain
167	notT2B	LVDS input/output	Token for address/readout daisychain
166	T2A	LVDS input/output	Token for address/readout daisychain
165	notT2A	LVDS input/output	Token for address/readout daisychain

8 List of known problems and bugs

8.1 Beetle1.0

The chip has to be patched e.g. with a focused ion beam to be functional. This is due to an error in the tristate buffers inside the control circuit. In addition the following errors occured:

- Transmission gate inside pipeline readout amplifier and multiplexer
- Bias network of pipeline readout amplifier
- Connection error inside multiplexer
- Readout daisychain not correctly implemented

8.2 Beetle1.1

Readout daisychain not correctly implemented (unchanged retained from *Beetle1.0*).

References

[1] R. Brenner et al., Nucl. Instr. and Meth. A339 (1994) 564

[2] The I^2C-bus and how to use it, Philips Semiconductors, 1995

[3] Bi-directional level shifter for I^2C-bus and other systems, Application Note AN97055, Philips Semiconductors, 1998