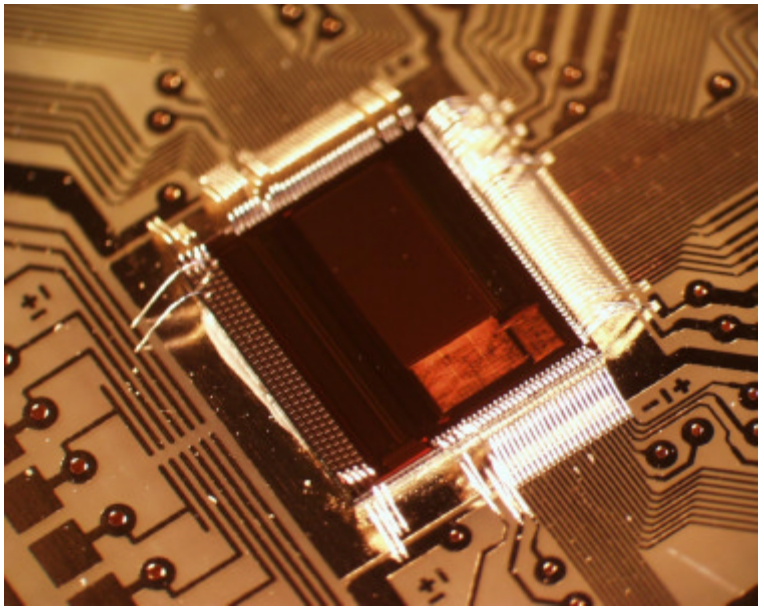
Beetle – A radiation hard readout chip for LHCb

Sven Löchner

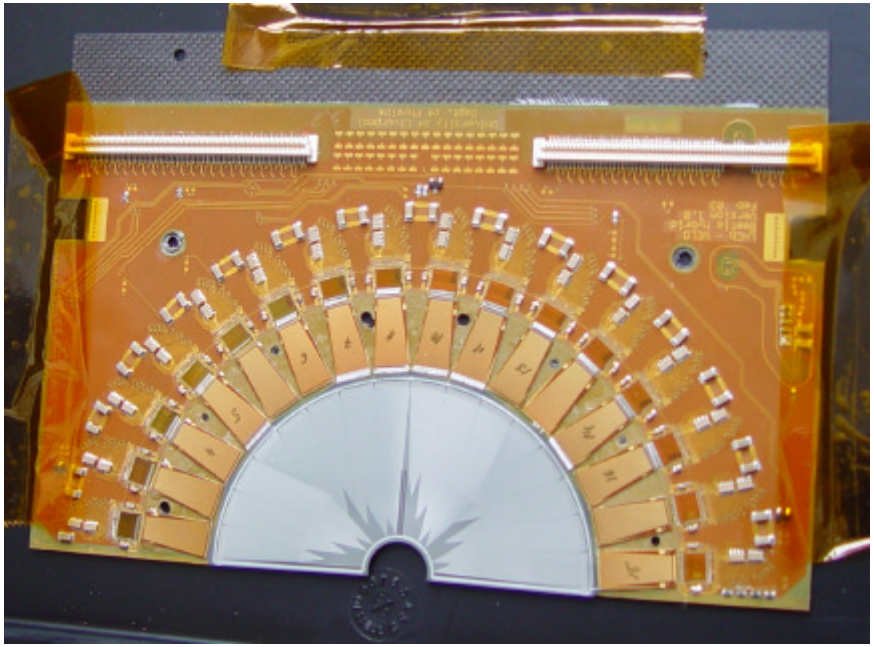
(Max-Planck-Institute for Nuclear Physics, Heidelberg)



Beetle 1.3 on a test PCB

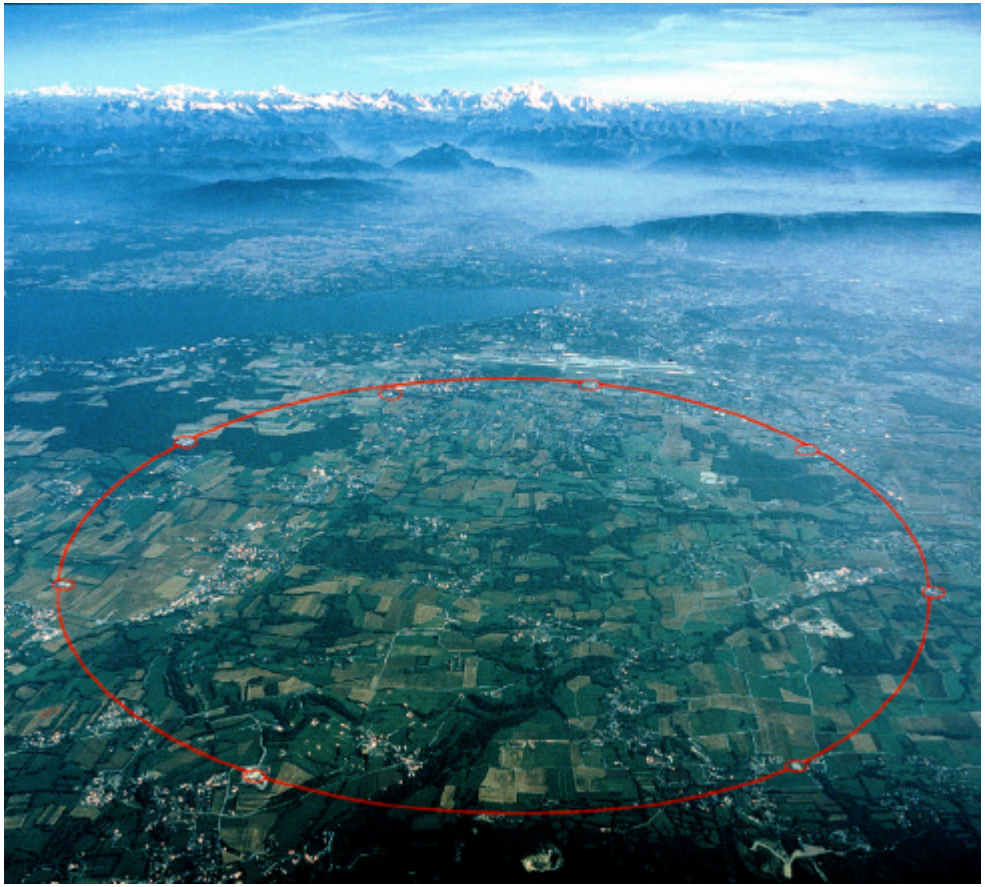
Outline

- **LHC accelerator / LHCb experiment**
- Beetle 1.3
  - Overview / Architecture
  - Lab measurements
  - Test beam
- “Unsightly” behaviours
  - patches and workaround
- Outlook



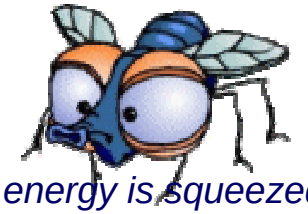
16 Beetle 1.3 on a VELO hybrid attached to Si-sensor

LHC accelerator at CERN



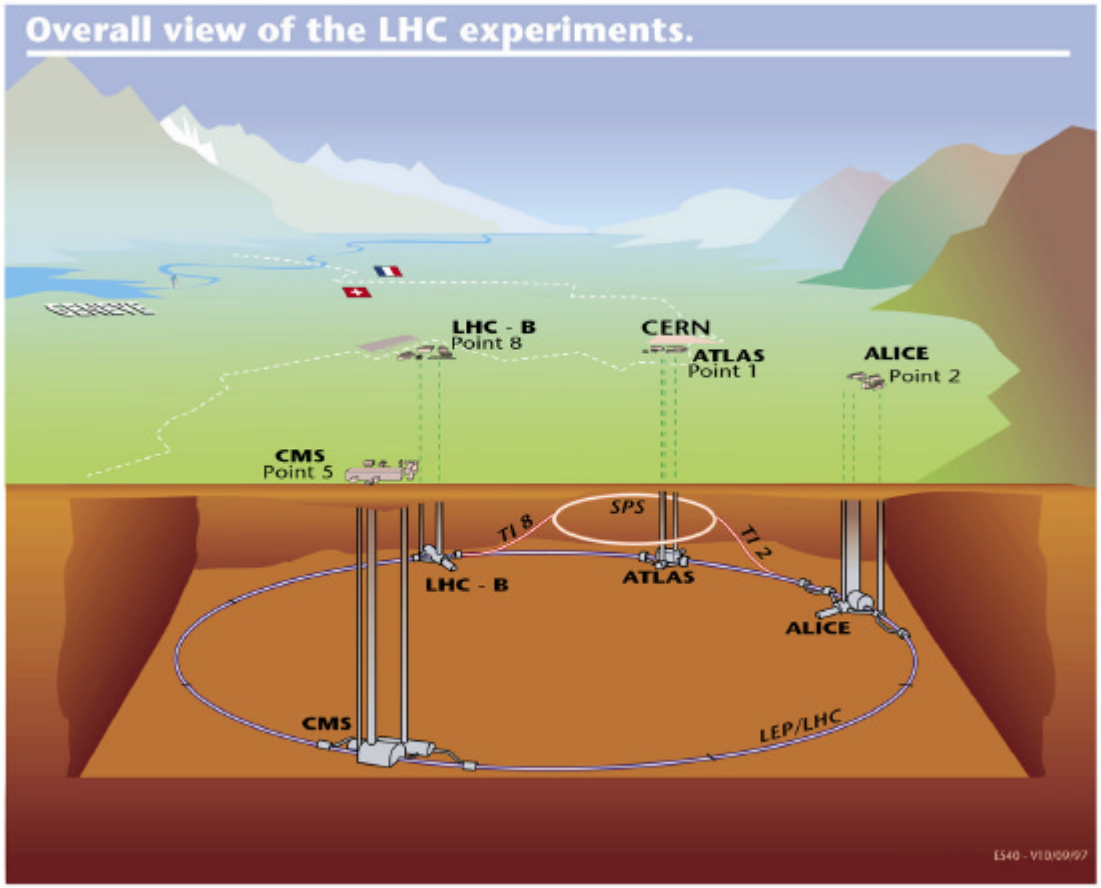
- **L**arge **H**adron **C**ollider **(LHC)**
- 27 km circumference
- switch on 2007
- collide beams of protons at an energy of 14 TeV,
  lead nuclei smashing together with a collision energy of 1150 TeV

1 TeV = energy of a flying mosquito,



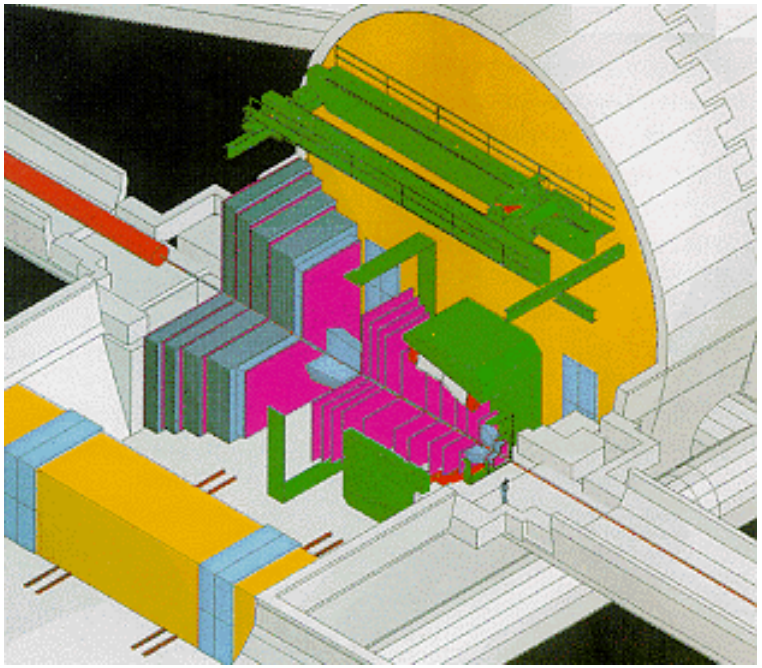
but energy is squeezed into a space about million million times smaller than a mosquito.

LHC experiments



- **5 LHC experiments:**
  - **ATLAS**
  - **CMS**
  - **TOTEM**
  - **ALICE**
  - **LHC*b***

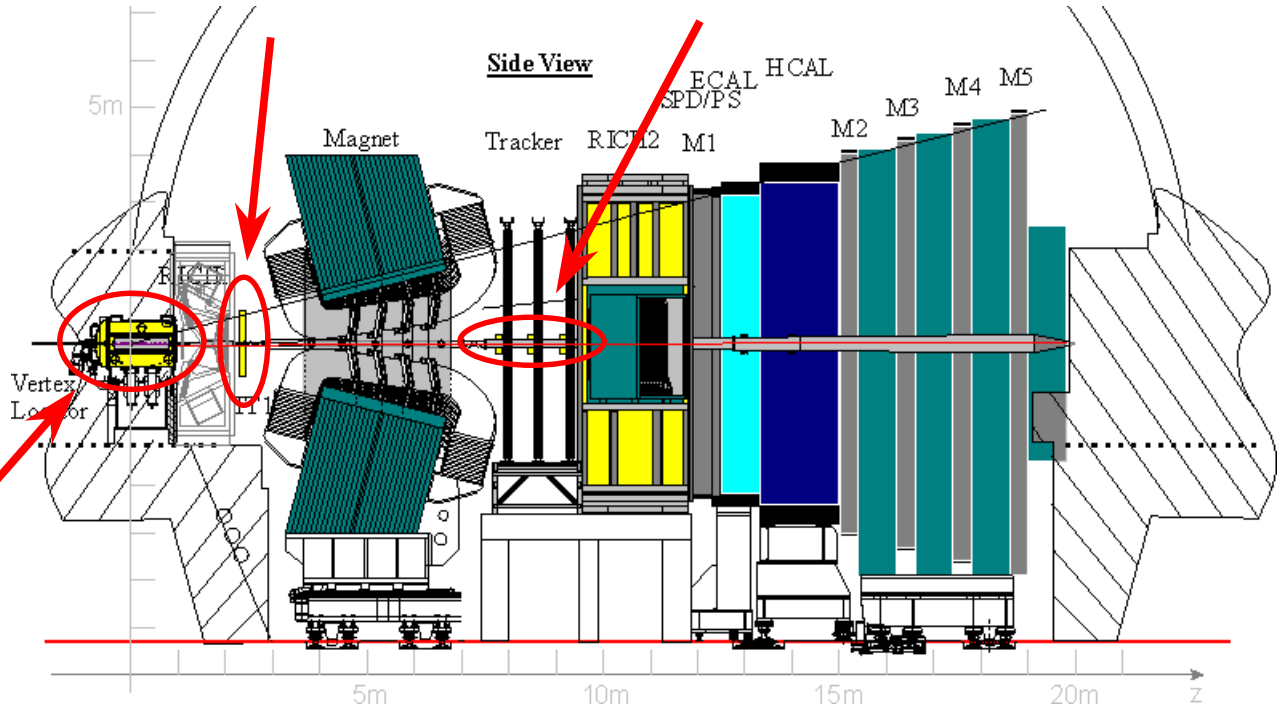
LHCb experiment



- **Single-arm spectrometer, *pp*-collisions**
- **precision measurement experiment for CP-violation and rare decays in B-meson system**
- **100.000 B-mesons/s at an interaction rate of 40 MHz, hidden in 200 times more non-B events**
- **Key Specifications:**
  - 40 MHz sampling / 40 MHz analog readout
  - max. latency 4 µs
  - fast shaping:
    $t_{rise} \leq 25$ ns
    remainder 25 ns after peak ≤ 30%
  - accept up to 16 consecutive triggers
  - readout time £ 900 ns
  - radiation hard ³ 10 Mrad

LHCb detector

- **Silicon Tracker (ST):**
  - silicon-strip detector
  - ~ 200 µm pitch
  - 350.000 channels
  - 11 m²
- **Vertex Locator (VeLo):**
  - R-Ö-silicon sensor
  - 37 µm to 92 µm pitch
  - Input load < 10 pF
  - 205.000 channels
- **Trigger Tracker (TT):**
  - Input load up to 50 pF
  - 22 to 33 cm strip length
- **Inner Tracker (IT):**
  - Input load ~ 33 pF
  - up to 22 cm strip length



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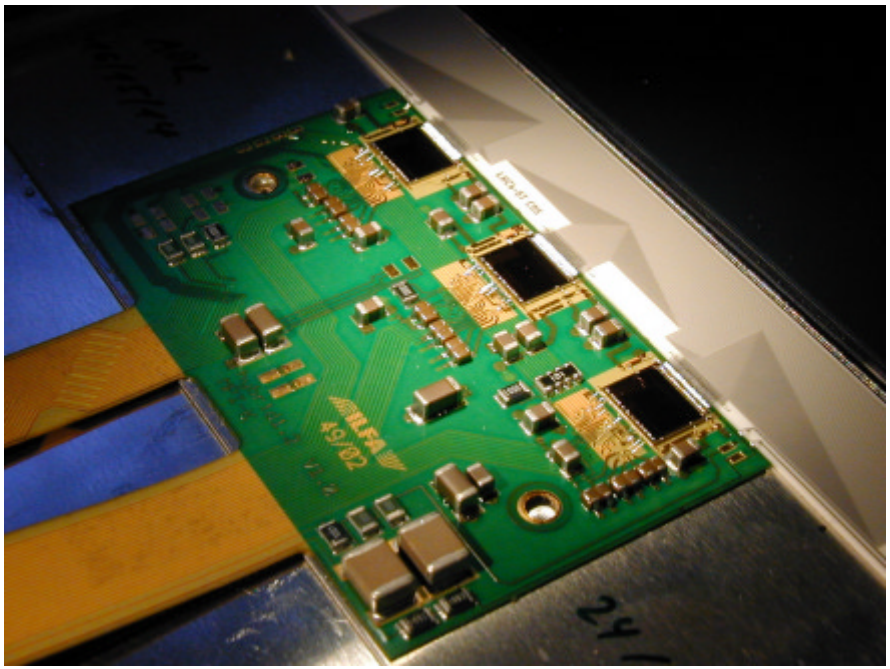
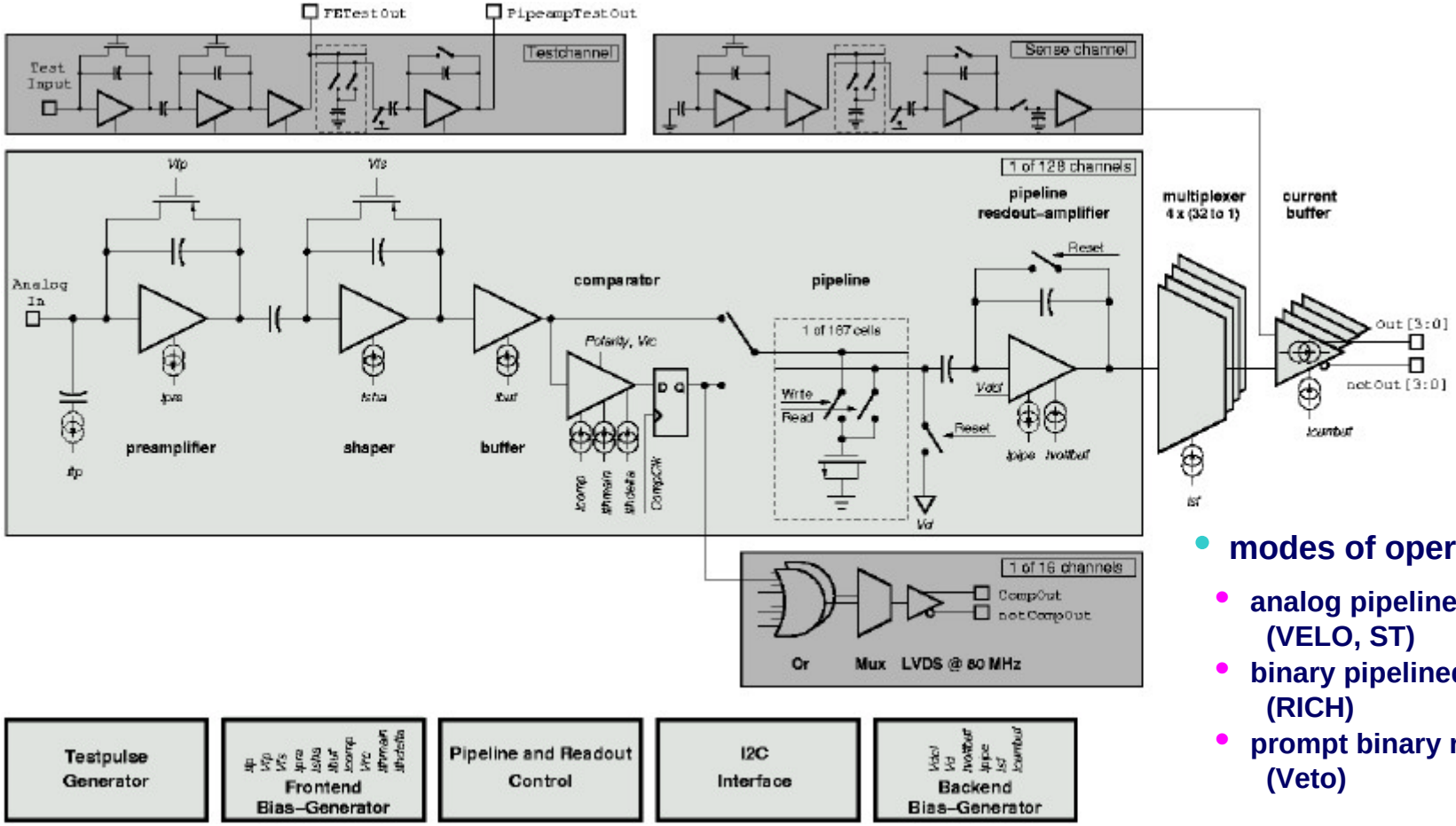


3 Beetle 1.2 on a TT prototype hybrid attached to Si-ladder

Beetle: Architecture



- **modes of operation:**
  - **analog pipelined readout (VELO, ST)**
  - **binary pipelined readout (RICH)**
  - **prompt binary readout (Veto)**

History

chip name	submission	size [mm²]	desciption
BeetleFE 1.0	May 1999	2 x 2	front-end test chip
BeetleBG 1.0	May 1999	2 x 2	bias generator test chip
Beetle 1.0	April 2000	5.5 x 6.1	readout chip
BeetleCO 1.0	April 2000	2 x 2	comparator test chip
BeetlePA 1.0	April 2000	2 x 2	pipeamp and I²C-interface test chip
BeetleMA 1.0	April 2000	2 x 2	front-end test chip for RICH option
Beetle 1.1	March 2001	5.5 x 6.1	readout chip
BeetleFE 1.1	May 2001	2 x 2	front-end test chip
BeetleFE 1.2	May 2001	2 x 2	front-end test chip
BeetleSR 1.0	May 2001	2 x 2	SEU robust I²C-interface test chip
Beetle 1.2	April 2002	5.1 x 6.1	readout chip (now SEU robust)
Beetle 1.2 MA0	December 2002	5.2 x 6.1	readout chip (RICH)
Beetle 1.3	June 2003	5.4 x 6.1	readout chip
Beetle 1.4	May 2004	5.4 x 6.1	readout chip

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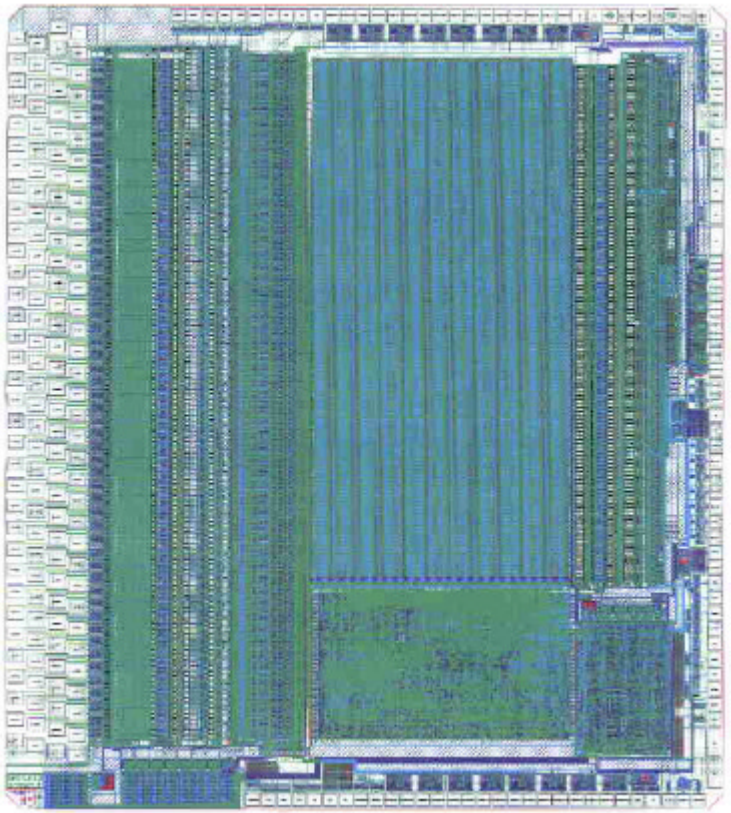
Layout

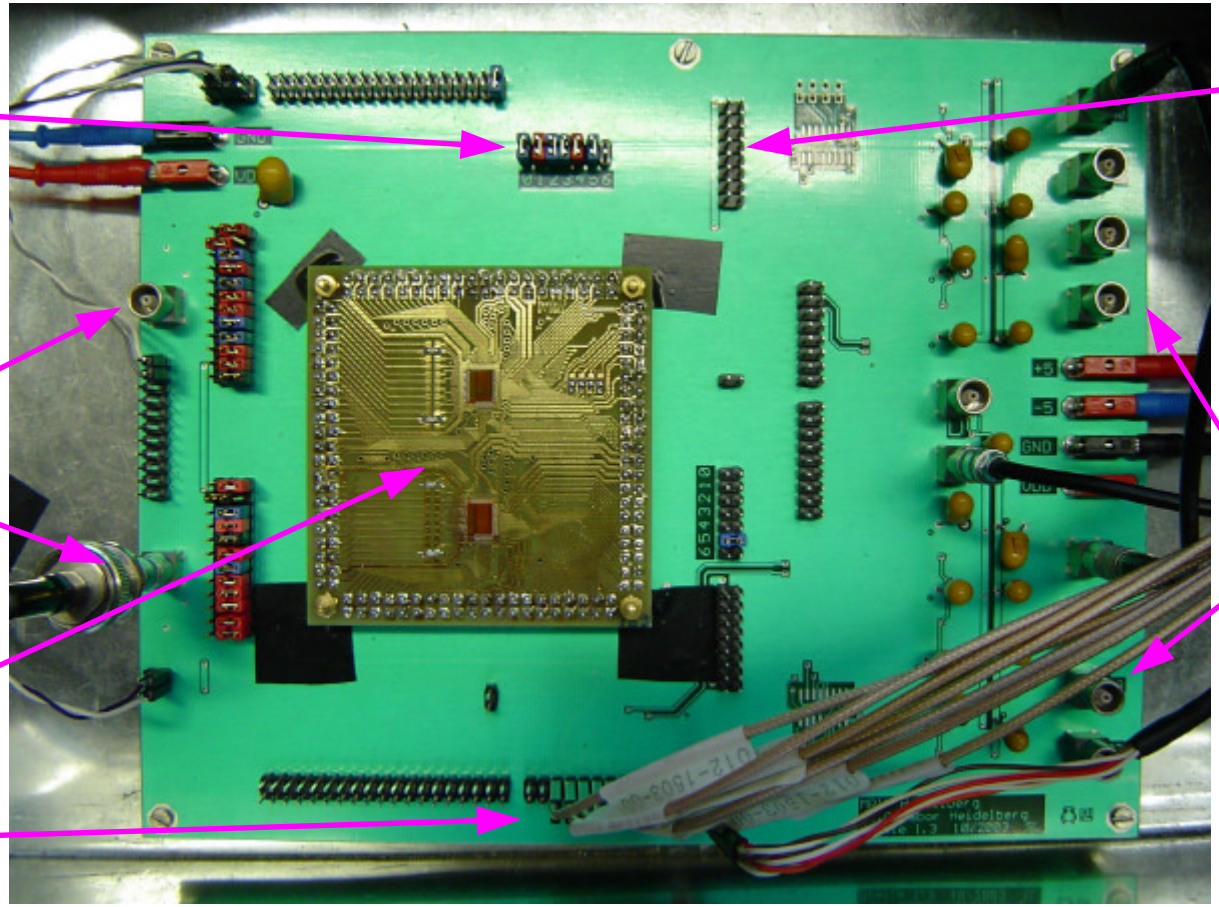
- **0.25 µm standard CMOS technology**
  - **3 metal layers**
  - **with MIMCAP and ZeroVt option**

- **30.06.2003 Submission of Beetle 1.3**
- **22.09.2003 Beetle arrived in Heidelberg**



Beetle 1.3 layout

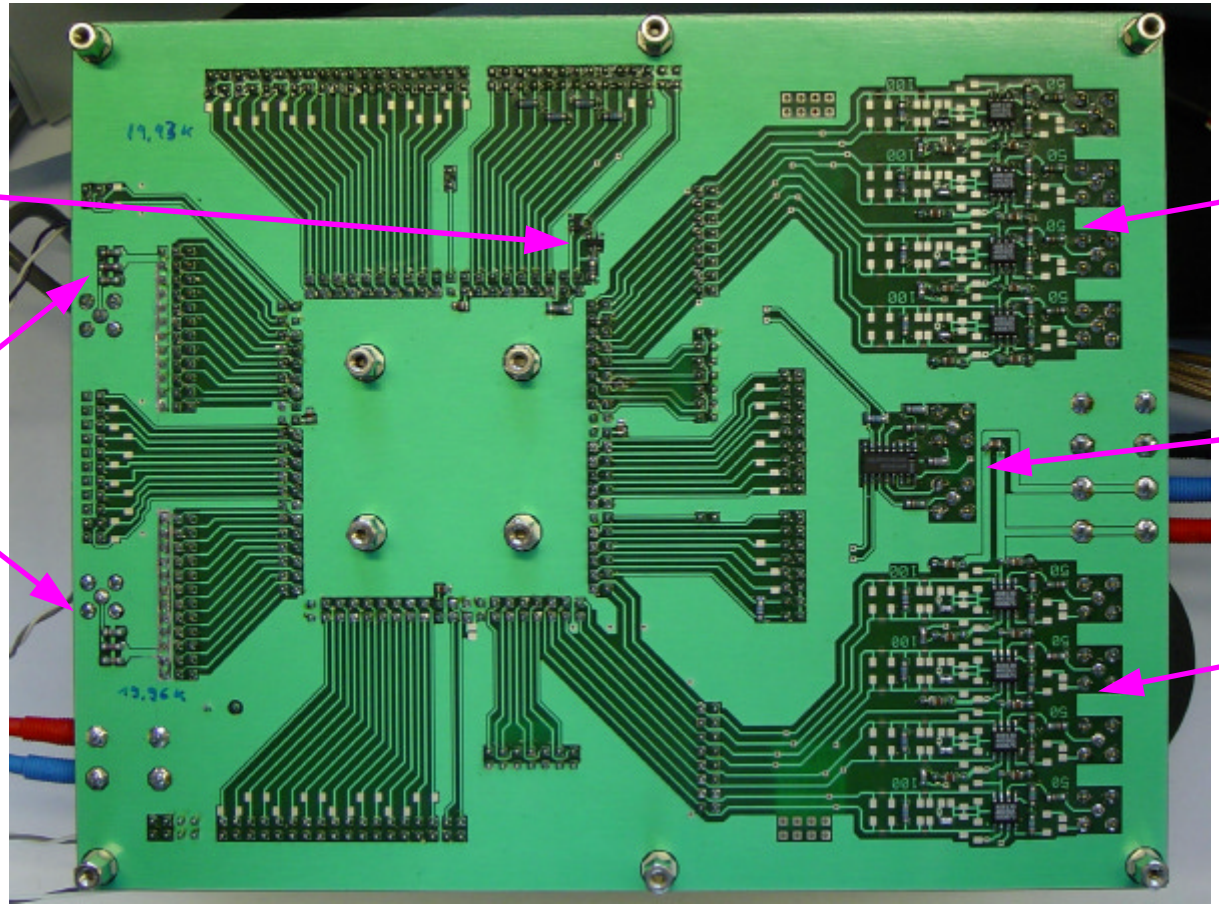
Beetle 1.3 Lab Setup (1)



Beetle 1.3 Lab Setup (2)

I²C level shifter
(unnecessary for Beetle 1.3)

Analog In
Voltage divider



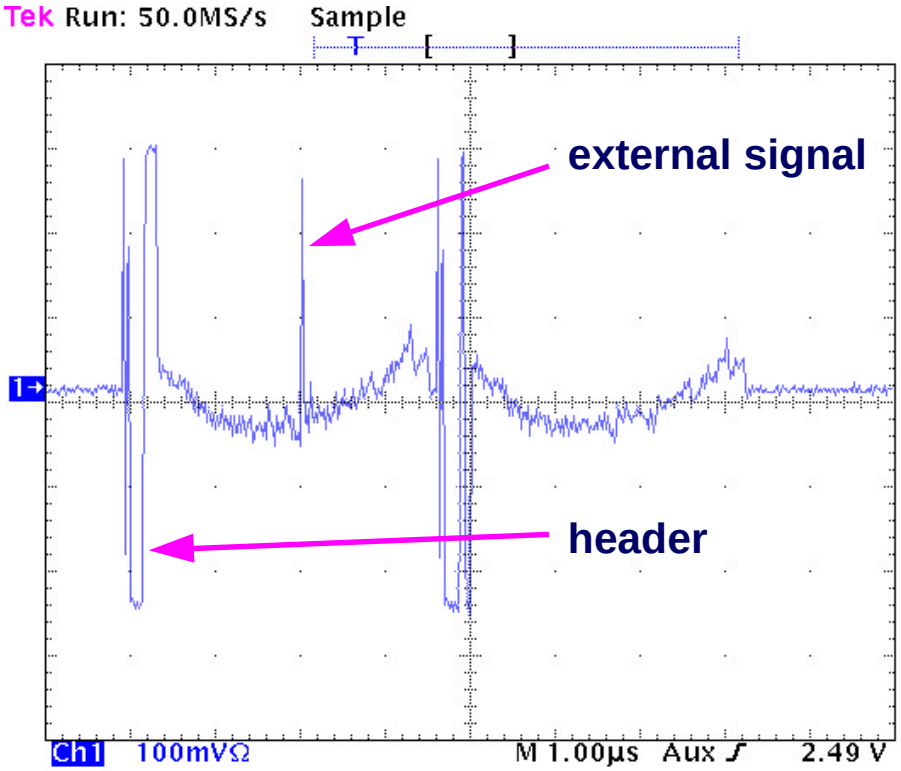
4 Analog Receiver for 2nd Beetle
(AD8130)

LVDS receiver
(DS90C032)

4 Analog receiver for 1st Beetle
(AD8130)

bottom view

First readout



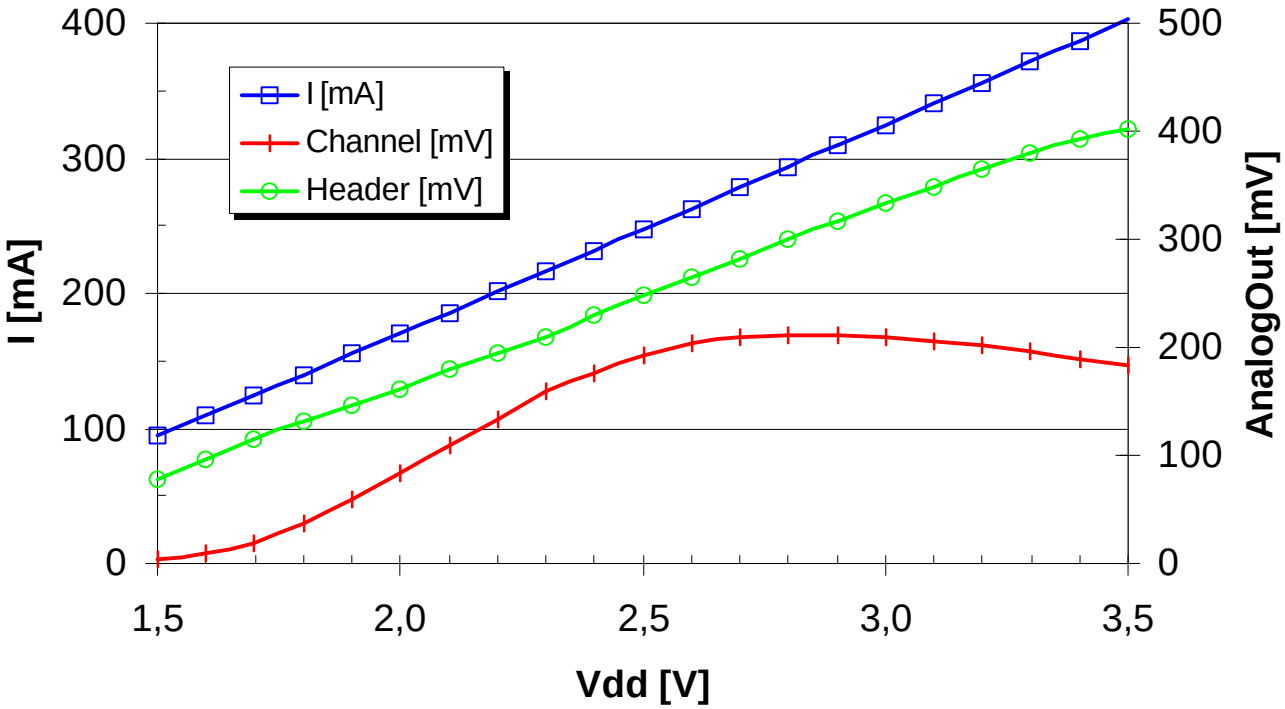
non-consecutive readout

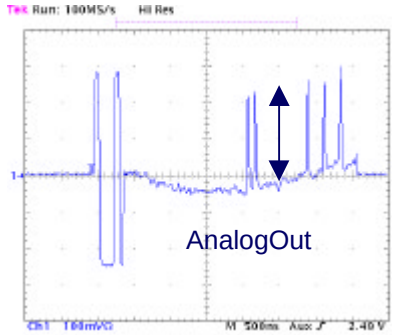
- analog readout with 40 MHz
- all 128 channels
- 2 readout frames
  - 1. readout with external signal
  - 2. readout without external signal

Total Power Consumption

Power consumption [mW/ch.]	Minimal	Nominal			Max. operation			Max. DAC
#AO drivers	0	0	1	4	0	1	4	4
without clock	**0,48**	3,49	3,68	**4,25**	4,76	5,02	**5,83**	**14,21**
only 40 MHz clock	**1,26**	4,28	4,46	**5,03**	5,54	5,81	**6,61**	**14,95**
clocked + 1.1 MHz trigger	**1,26**	4,36	4,56	**5,14**	5,62	5,90	**6,70**	**15,12**

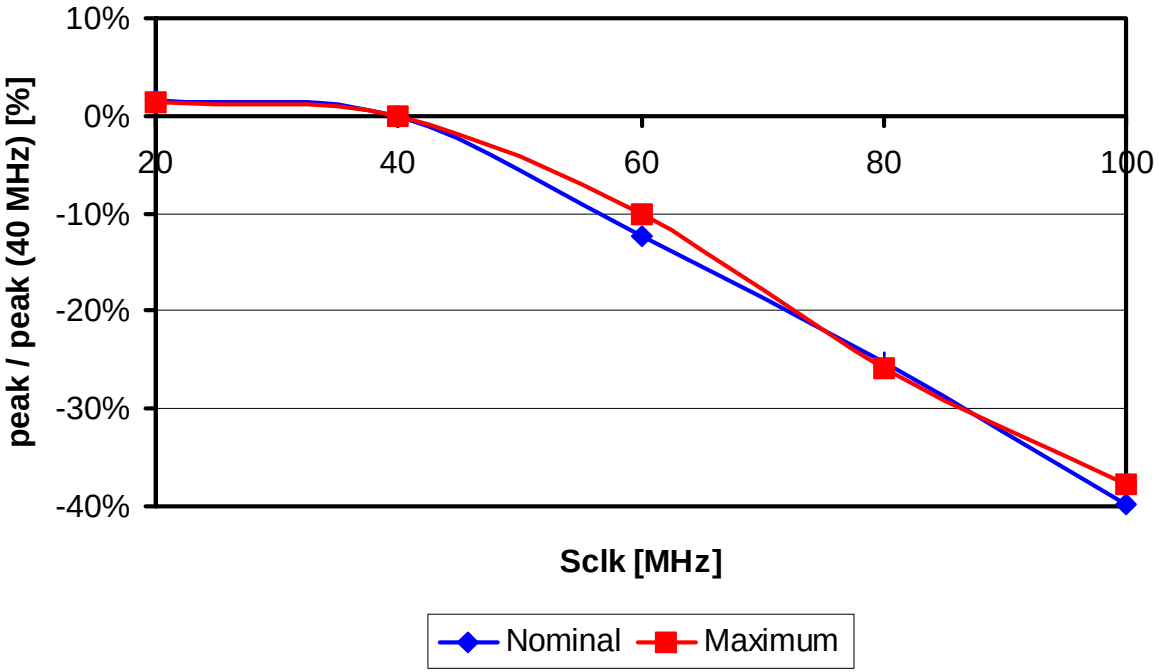
Power Supply Operation





- **Analog / Digital: 1.5V to 3.5V**

Overclocking Test

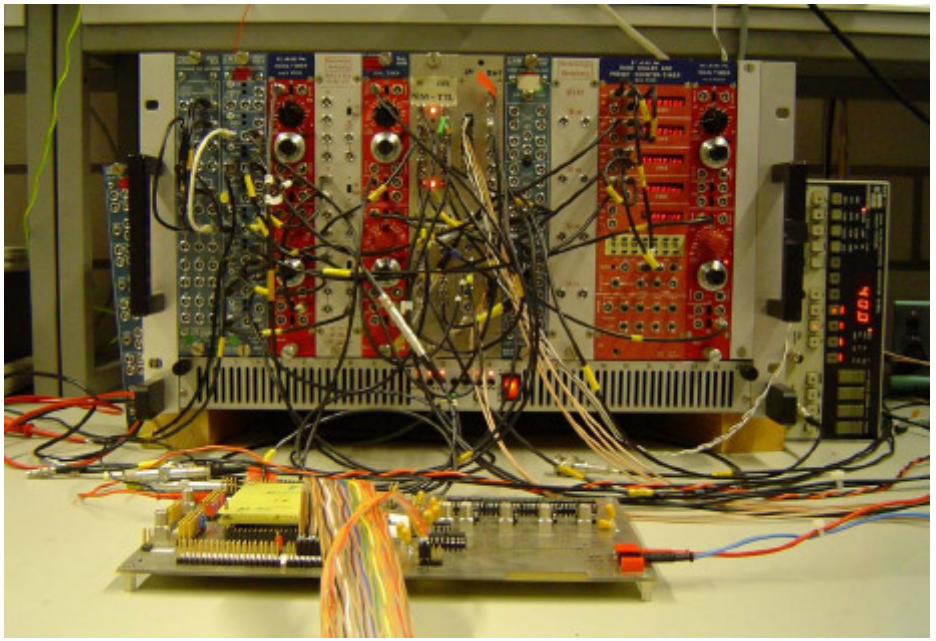


frequency test

- **Digital: perfect operation up to 100 MHz**
- **Analog: nearly 40% gain loss @ 100 MHz**

Random Trigger Test

- 2 Beetle 1.3 @ 40 MHz
- 2 x 2.34 · 10^{12} random triggers
  - 172h (1.778 · 10^{12}, Þ 2.87 MHz)
  - 75h (3.039 · 10^{11}, Þ 1.12 MHz)
  - 92h (2.550 · 10^{11}, Þ 0.77 MHz)
- no triggers lost



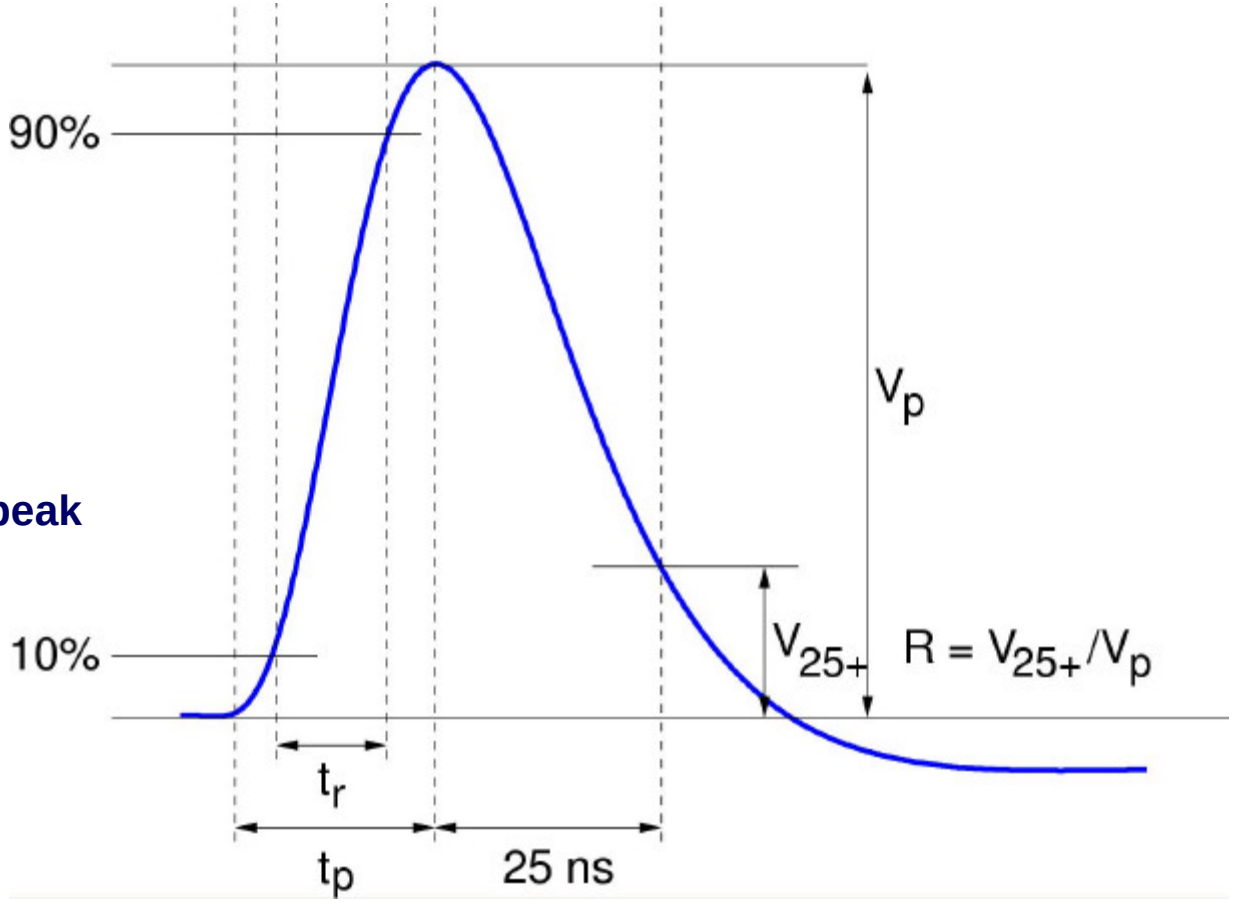
Beetle 1.3 random trigger test setup

Temperature Test

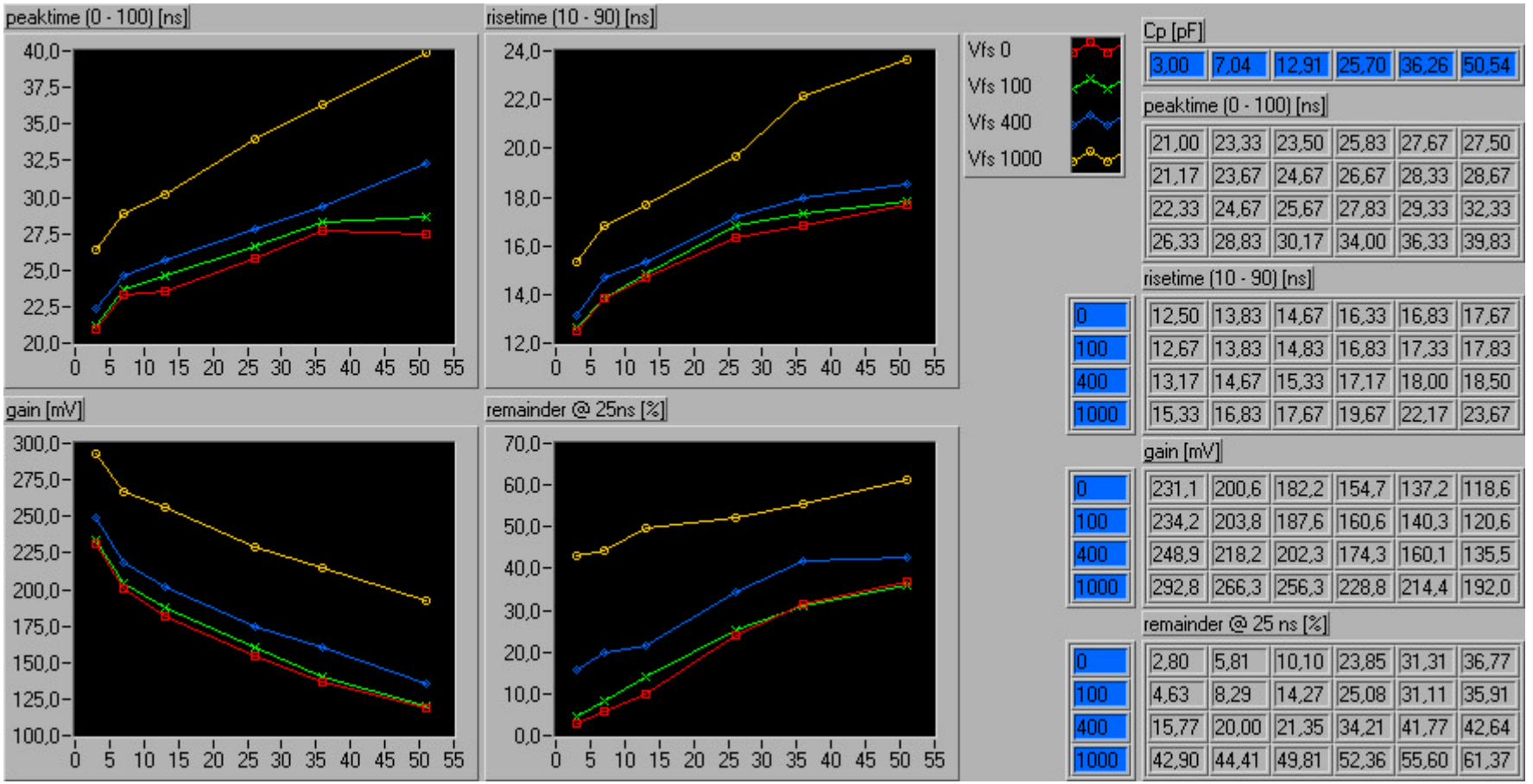
- **Start-up tests (~ 15 times each chip):**
  - **2 Beetle 1.3**
  - **@ T= -44°C, 60°C, 75°C** (facility temperature)
  - **Programming (I^2C)**
  - **1.1 MHz trigger + analog readout**
- **Longtime operating tests (~3 days):**
  - **1 Beetle 1.3**
  - **@ T= -44°C, 60°C, 75°C ($T_{surface}$= -4°C, 94°C, 107°C)**
  - **1.1 MHz + analog readout**
- **Max. stress test:**
  - **1 Beetle 1.3**
  - **max. DAC settings**
  - **@ T= 60°C (Þ $T_{surface}$= 126°C)**
  - **Operating over ~ 12 hour**

Front end: Pulse-Parameter (1)

- **Front-end pulse characterization:**
  - **peaking time t_p (0-100)**
  - **rise time t_r (10-90)**
  - **gain V_p**
  - **remainder 25 ns after peak**
    $R = V_{25+} / V_p$



Front end: Pulse-Parameter (2)



Cp [pF]

3,00	7,04	12,91	25,70	36,26	50,54

peaktime (0 - 100) [ns]

21,00	23,33	23,50	25,83	27,67	27,50
21,17	23,67	24,67	26,67	28,33	28,67
22,33	24,67	25,67	27,83	29,33	32,33
26,33	28,83	30,17	34,00	36,33	39,83

risetime (10 - 90) [ns]

0	12,50	13,83	14,67	16,33	16,83	17,67
100	12,67	13,83	14,83	16,83	17,33	17,83
400	13,17	14,67	15,33	17,17	18,00	18,50
1000	15,33	16,83	17,67	19,67	22,17	23,67

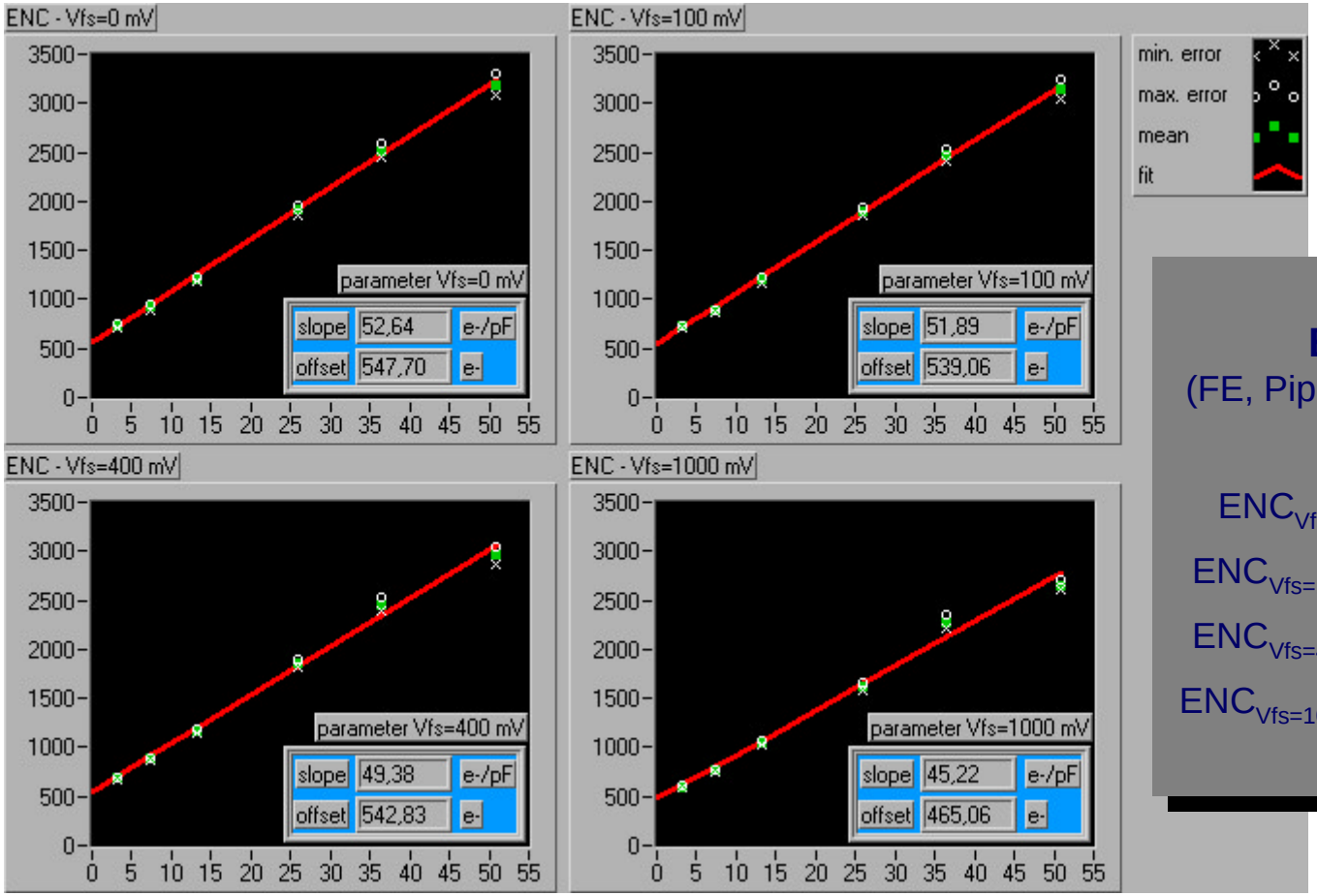
gain [mV]

0	231,1	200,6	182,2	154,7	137,2	118,6
100	234,2	203,8	187,6	160,6	140,3	120,6
400	248,9	218,2	202,3	174,3	160,1	135,5
1000	292,8	266,3	256,3	228,8	214,4	192,0

remainder @ 25 ns [%]

0	2,80	5,81	10,10	23,85	31,31	36,77
100	4,63	8,29	14,27	25,08	31,11	35,91
400	15,77	20,00	21,35	34,21	41,77	42,64
1000	42,90	44,41	49,81	52,36	55,60	61,37

Front end: ENC - Beetle 1.3



Beetle 1.3 ENC
(FE, Pipeline, Pipeamp, Readout)

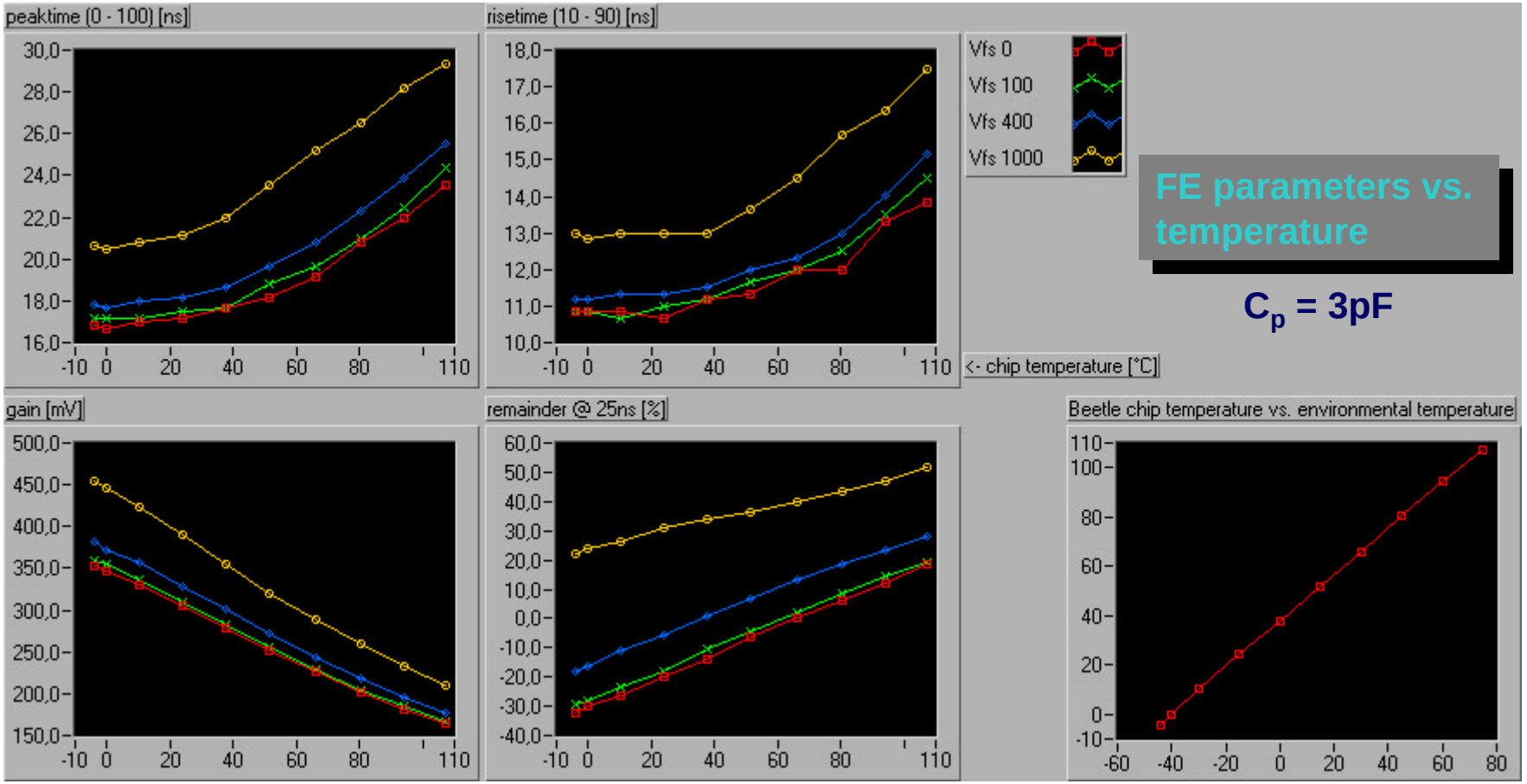
$ENC_{Vfs=0}$: 547.7 e^- + 52.6 e^-/pF

$ENC_{Vfs=100}$: 539.1 e^- + 51.9 e^-/pF

$ENC_{Vfs=400}$: 542.8 e^- + 49.9 e^-/pF

$ENC_{Vfs=1000}$: 465.1 e^- + 45.2 e^-/pF

Front end: Temperature



FE parameters vs. temperature

C_p = 3pF

I²C - Input Pads

New 5V tolerant I²C-Pads for Beetle 1.3

- **SCL / SDA input level tested:**
  min. HIGH: 1.5V
  max. HIGH: 7.0V (only tested up to 7.0V)

  min. LOW: -0.7V
  max. LOW: 1.1V @ 2.5V HIGH level
  1.2V @ 3.3V
  1.3V @ 5.0V

- **SDA output delay (ACK): 500ns** (I²C specification: delay > 300ns)

Total Ionizing Dose irradiation

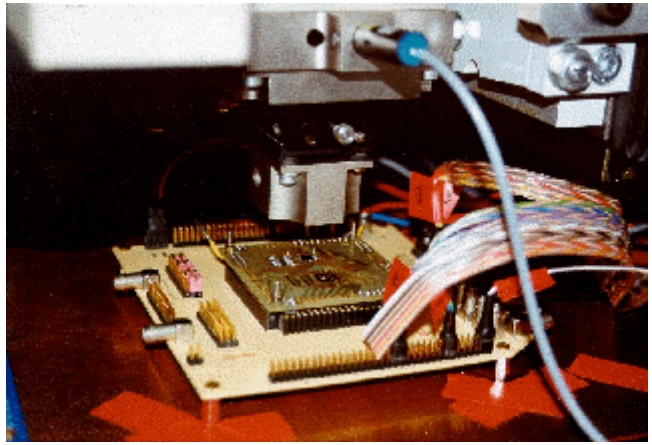
Done at the X-ray facility of CERN's Microelectronic Group

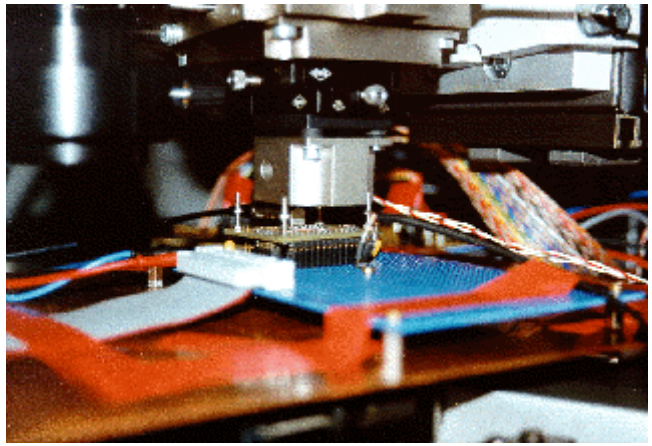
Irradiated Chips:

- **4 Beetle 1.1 chips**
  - 2 chips being kept at room temperature
  - 2 chips being annealed at 100 °C
- **2 BeetleFE 1.1 chips**
  containing FE prototypes with a NMOS input transistor
- **2 BeetleFE 1.2 chips**
  containing FE prototypes with a PMOS input transistor

Accumulated Dose:

- **Beetle 1.1:** 10 Mrad, 10 Mrad, 30 Mrad, 45 Mrad
- **BeetleFE 1.1:** 10 Mrad
- **BeetleFE 1.2:** 10 Mrad



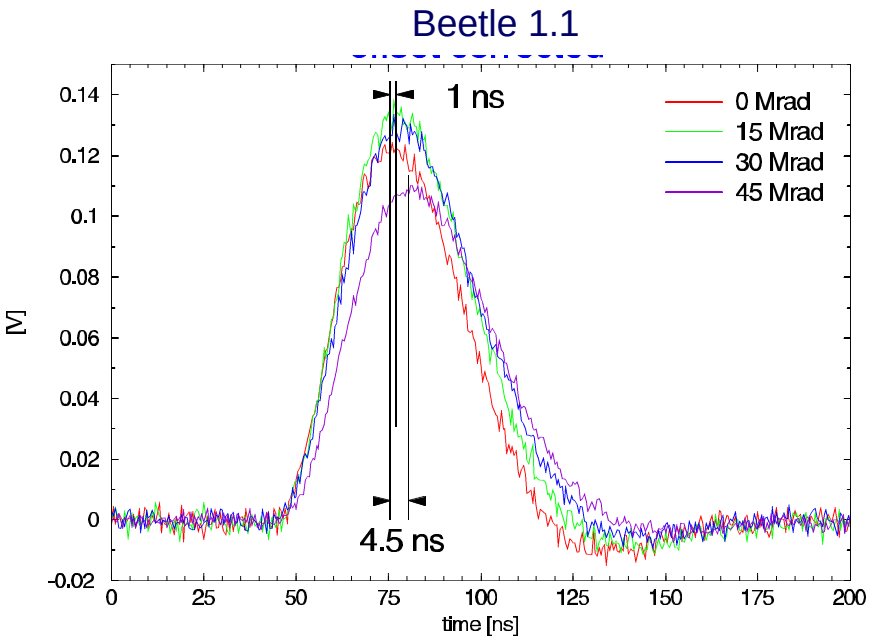


Total Ionizing Dose results

Beetle showed full functionality beyond 45 Mrad

- full trigger and readout functionality
- full slow control functionality
- performance degradations are small
  - peaktime: up to 30 Mrad: ≤ 1 ns
    up to 45 Mrad: ≤ 4,5 ns
  - gain: up to 45 Mrad: ≤ 10%

no tuning of bias settings



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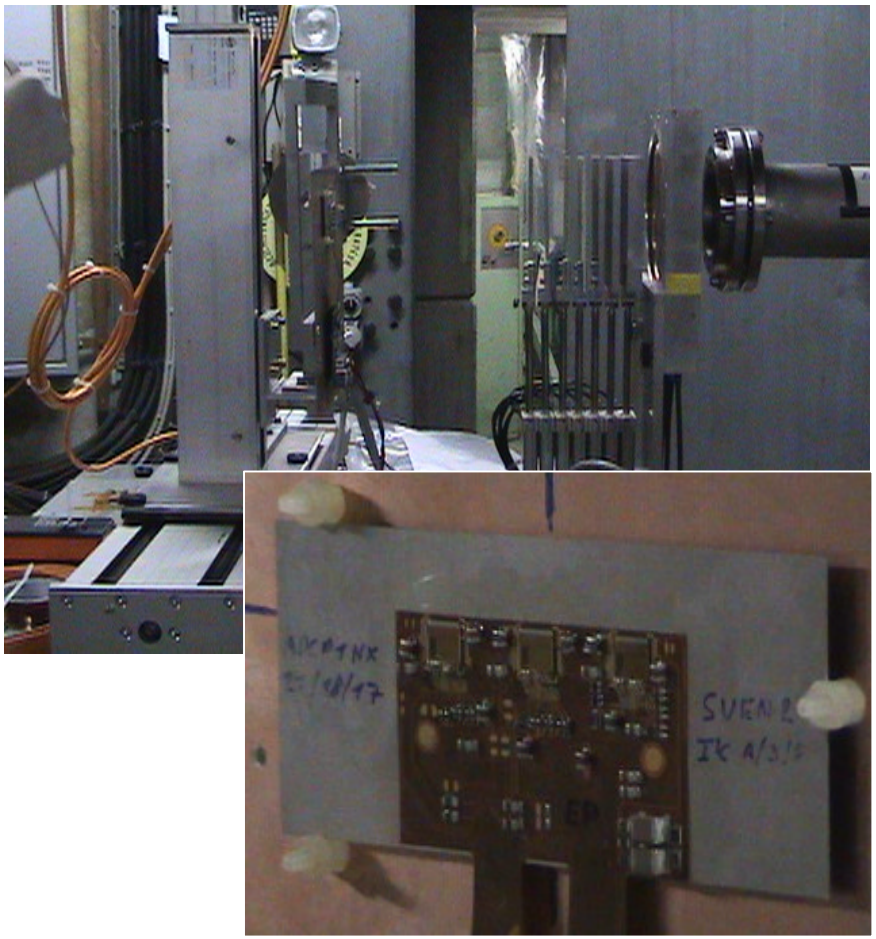
SEU beam test (1)

- **SEU beam test at**
  Proton Irradiation Facility (PIF)
  Paul-Scherrer Institute, Swizerland

- **Irradiate of 3 chips:**
  - **65 MeV protons**
  - **mean flux: 1.56 x 10^9 p/cm²/s**
  - **fluence: 5.51 x 10^{13} p/cm²**
  - **accumulated dose: 7.93 Mrad**

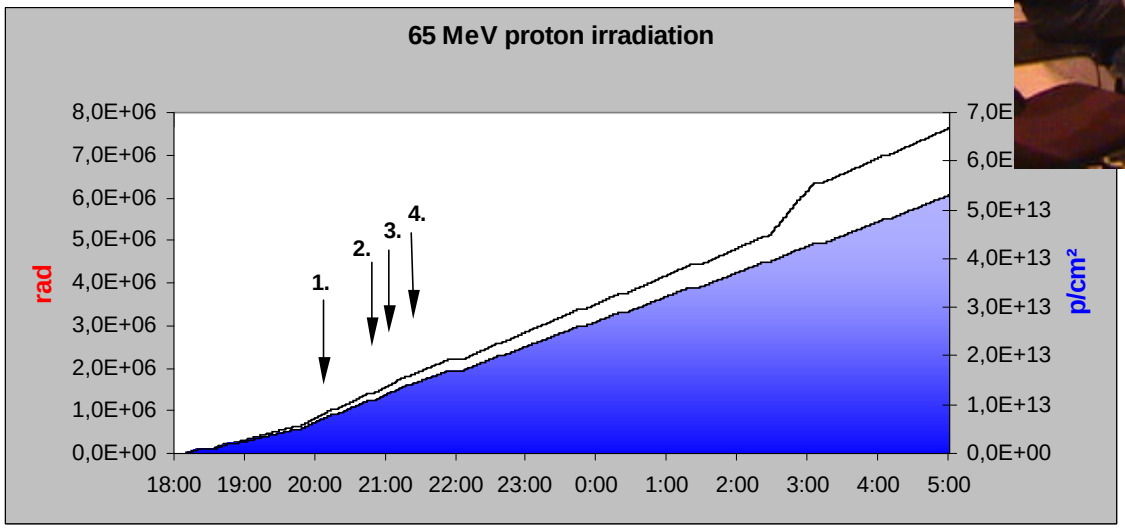
- **Check for bit-flips in Beetle registers**



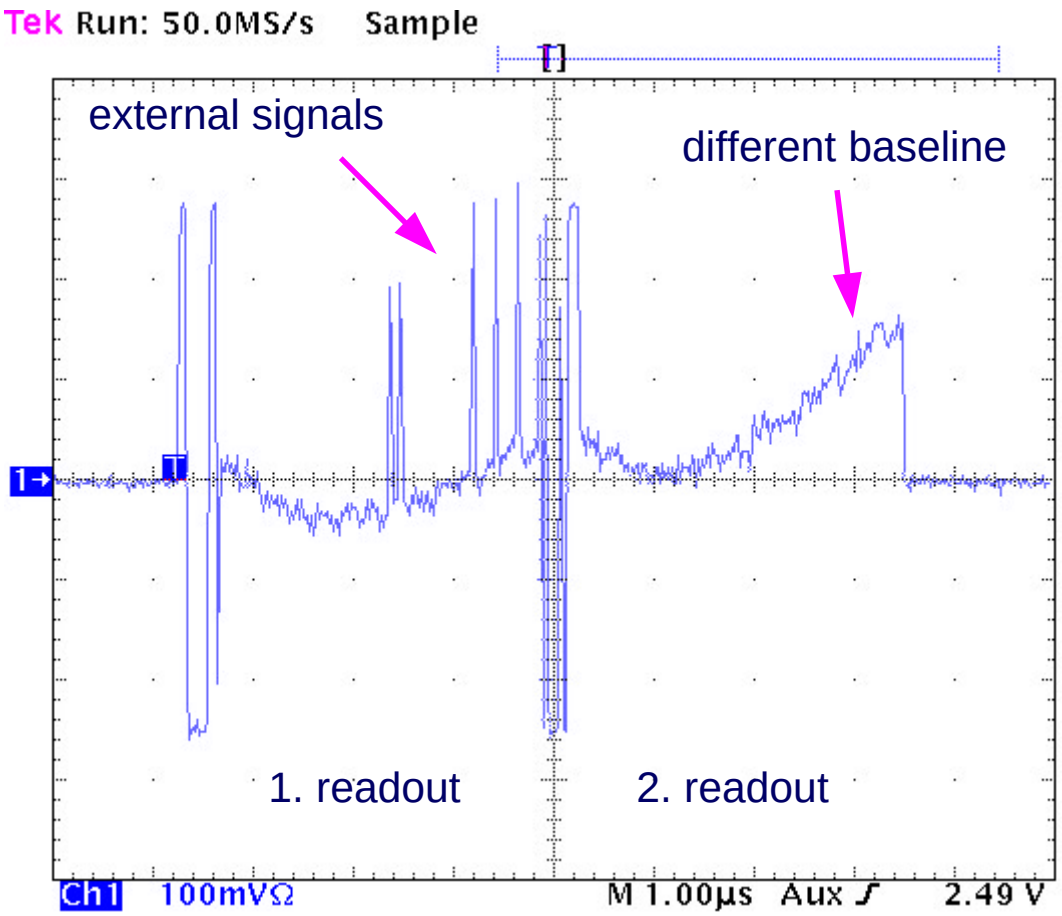
SEU beam test (2)

- **4 SEU flips found**
- **time distribution not yet understood, but**
  SEU cross section is not a problem !!!

setup on top of the irradiation facility



Sticky Charge



Consecutive readout

- **External signals on 5 channel in 1st readout frame**
- **No sticky charge in 2nd readout frame**

  but still a different baseline

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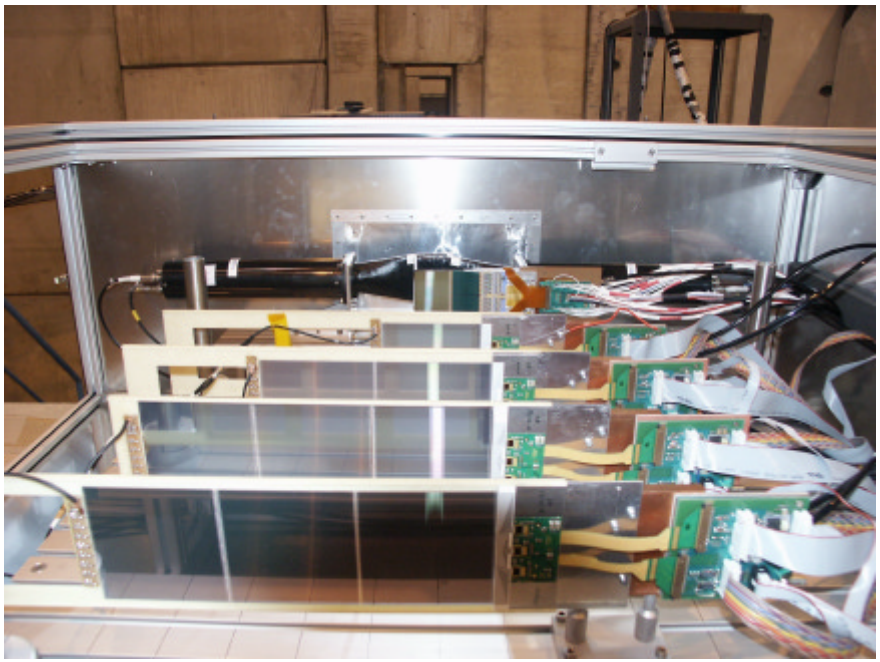
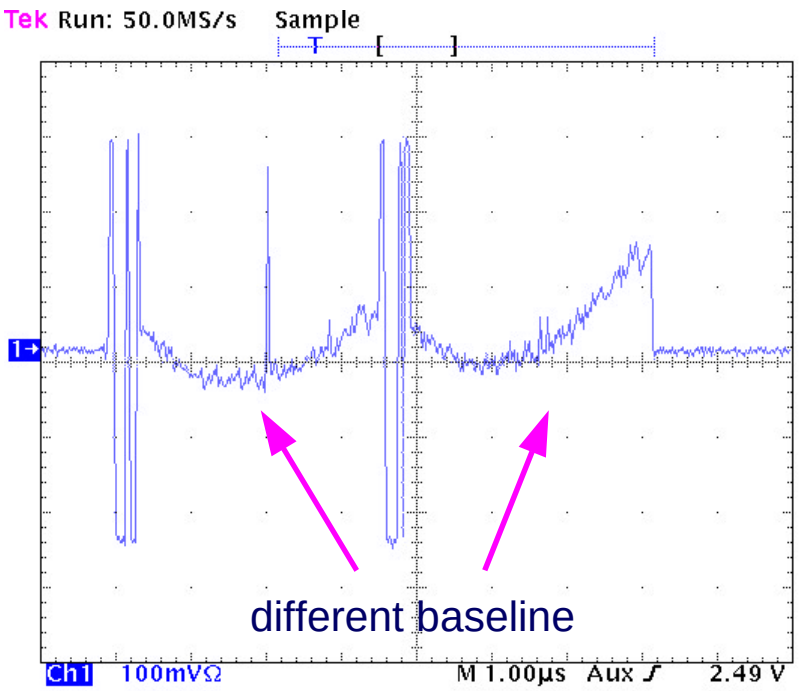
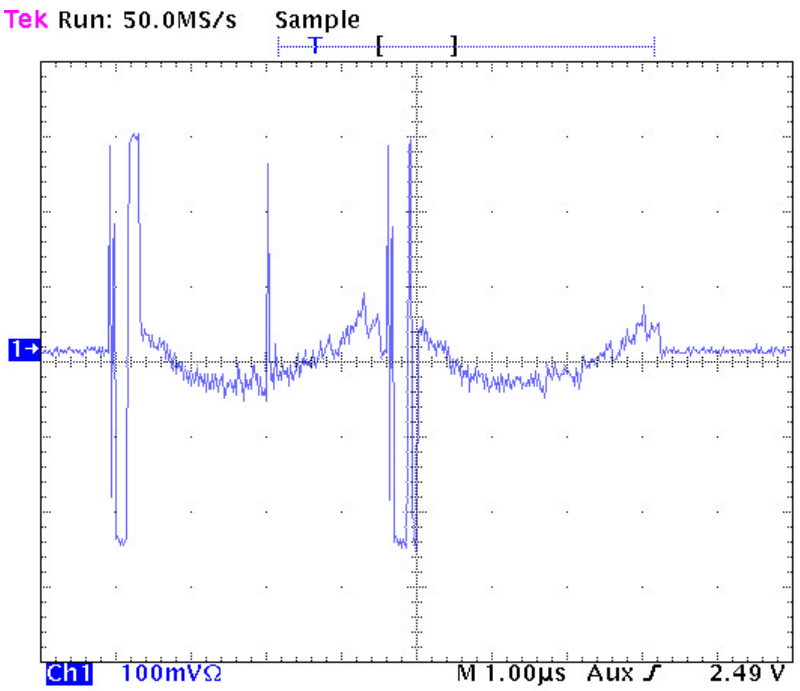


X7 beam test with different sensors, attached to Beetle 1.2 chips

Readout (Baseline) (1)

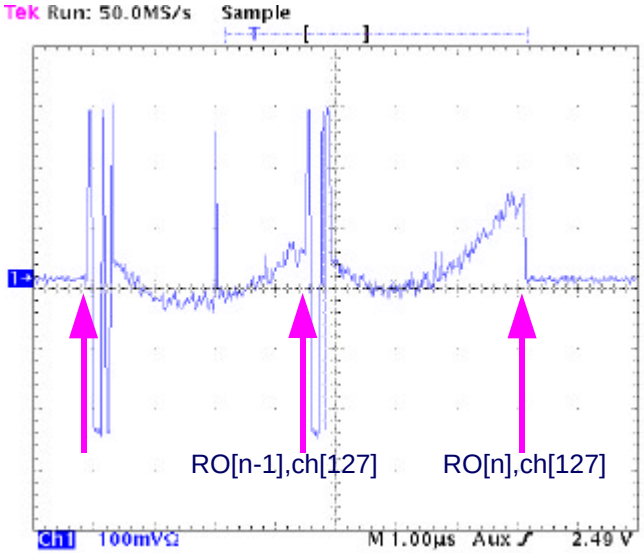


consecutive readout



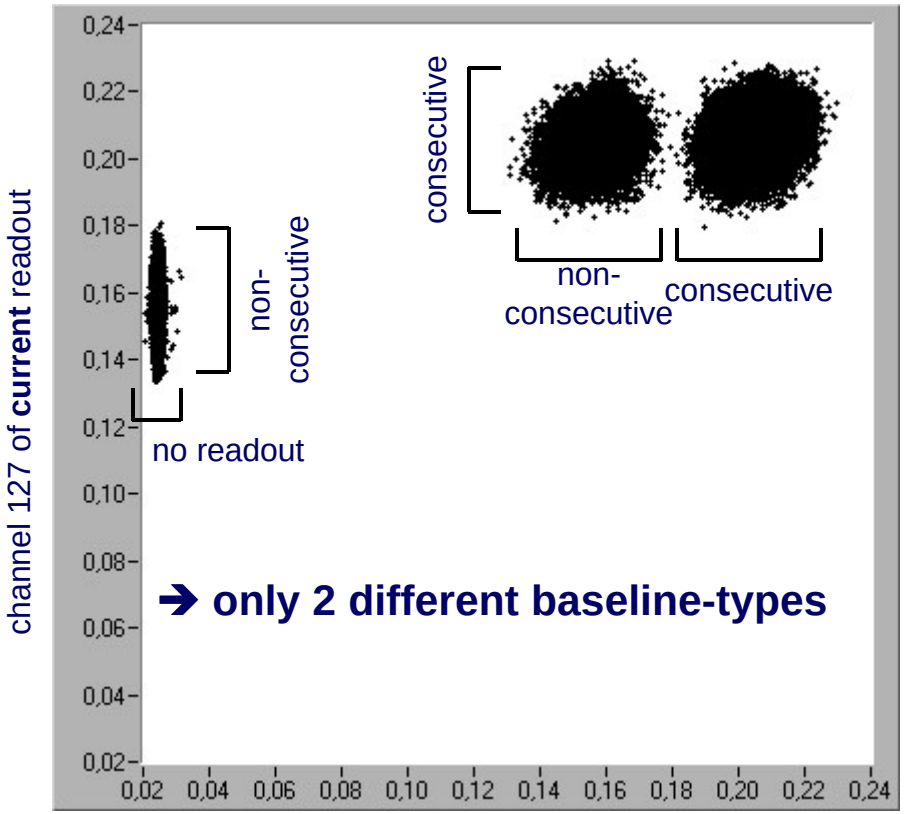
non-consecutive readout

Readout (Baseline) (2)

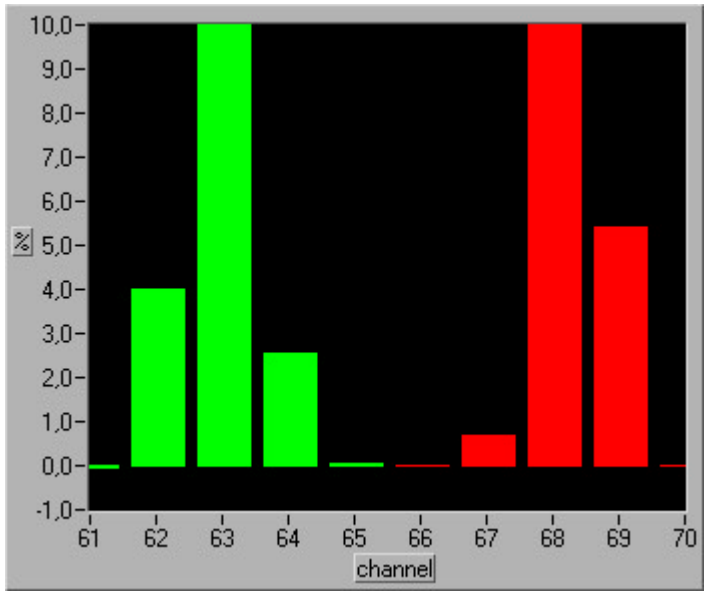


- **correlation plot of RO[n-1], ch[127] vs. RO[n], ch[127]**

previous readout vs. current readout



Channel Crosstalk (1)



Testpulse (63. & 68) is standardised to 100%

Channel crosstalk

- **measured a even/odd dependency**
- **this effect is also present in 1.2**

Clarification of crosstalk:

typical Testpulse for a odd channel (e.g. 63):
crosstalk into predecessor channel is larger than into successor channel

typical Testpulse for a even channel (e.g. 68):
crosstalk into successor channel is larger than into predecessor channel

Channel Crosstalk (2)

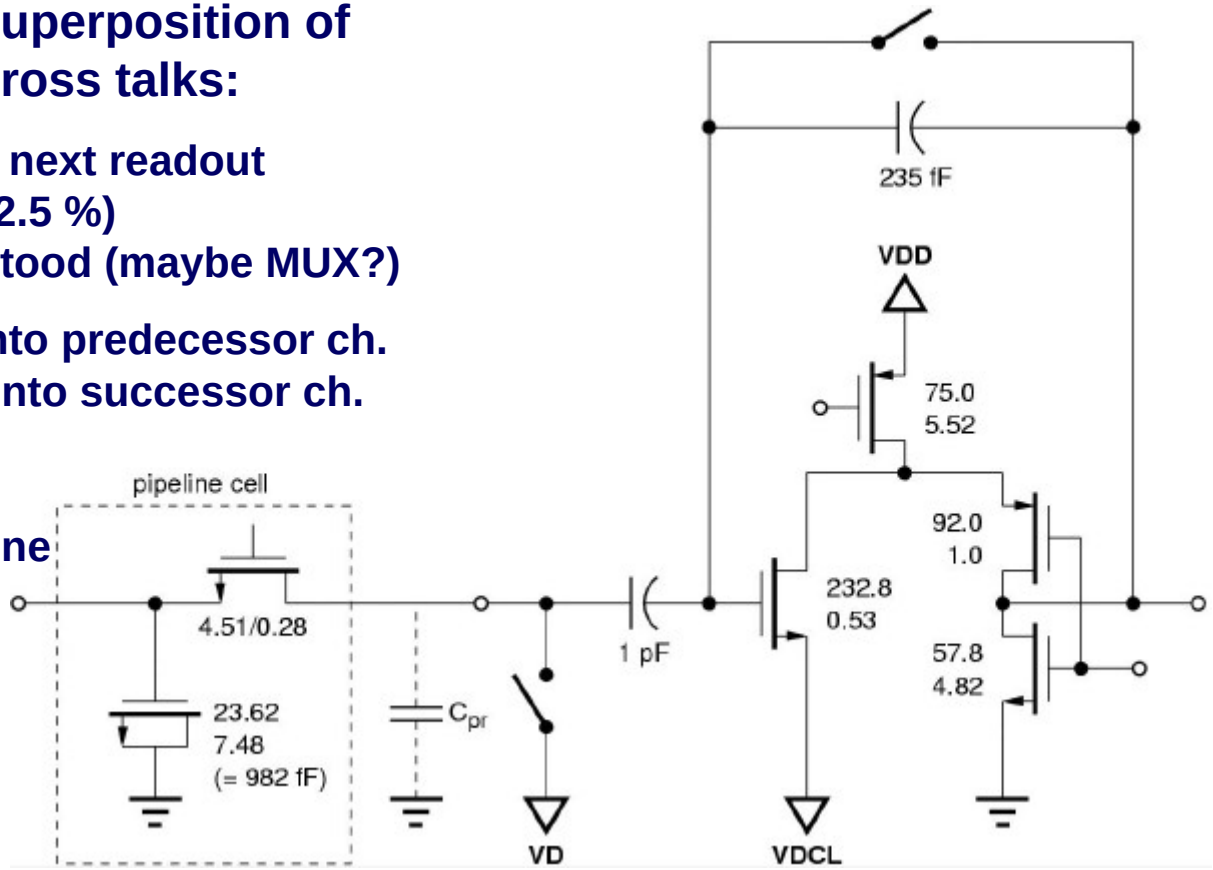
Channel crosstalk is a superposition of at least two different cross talks:

- **general “remainder” into next readout channel (order of 2 % to 2.5 %)**
  ➔ reason yet not understood (maybe MUX?)
- **odd channel: crosstalk into predecessor ch. even channel: crosstalk into successor ch. (order of 2.5 %)**

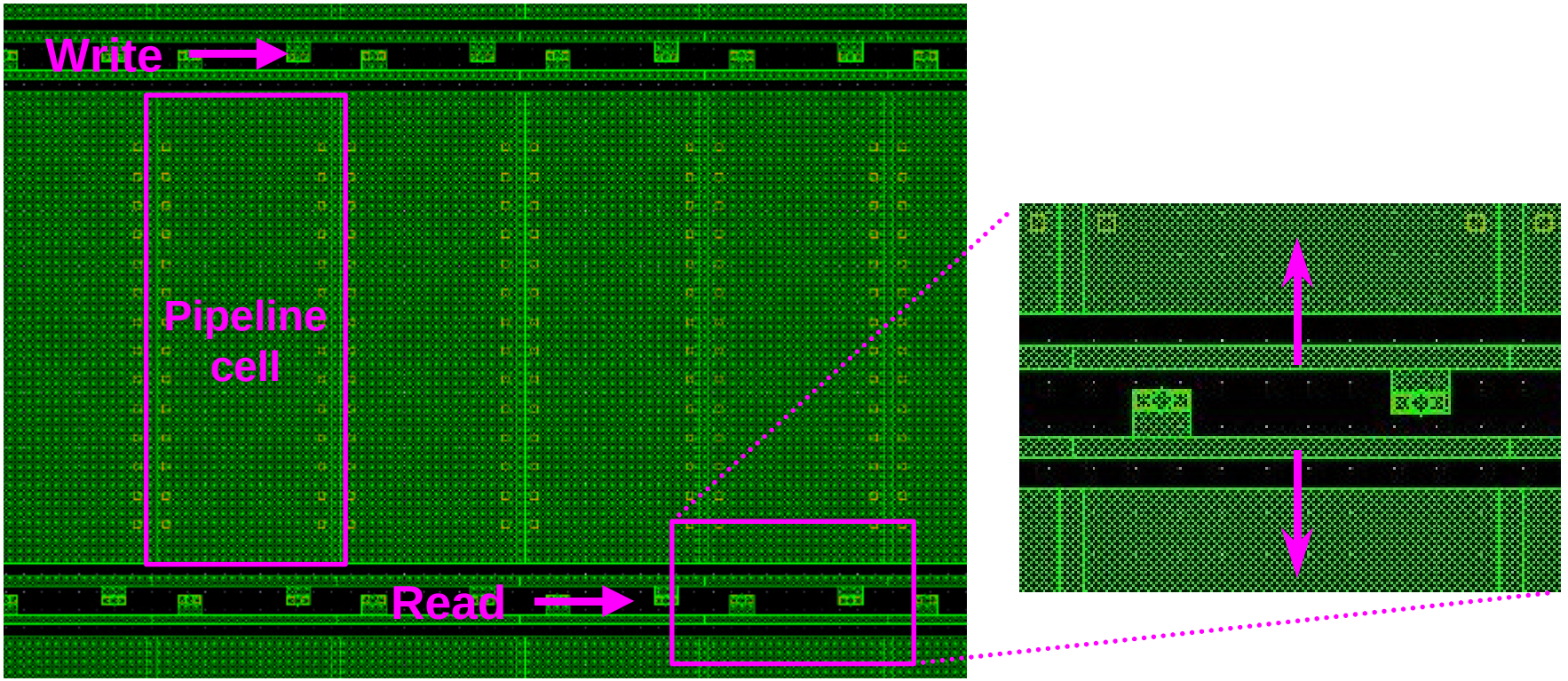
➔ readout line from Pipeline into Pipeamp

➔ capacitance between adjacent lines ~ 60fF

- **verified in simulation**
- **easy to fix**



Channel Crosstalk (3)



Pipeline length: ~ 2 mm

Readout header: parity bit

1 port mode

AO[0]	I0	I1	I2	I3	I4	I5	I6	I7	P7	P6	P5	P4	P3	P2	P1	P0

4 port mode

AO[0]	I0	I4	P1	P0
AO[1]	I1	I5	P3	P2
AO[2]	I2	I6	P5	P4
AO[3]	I3	I7	P7	P6

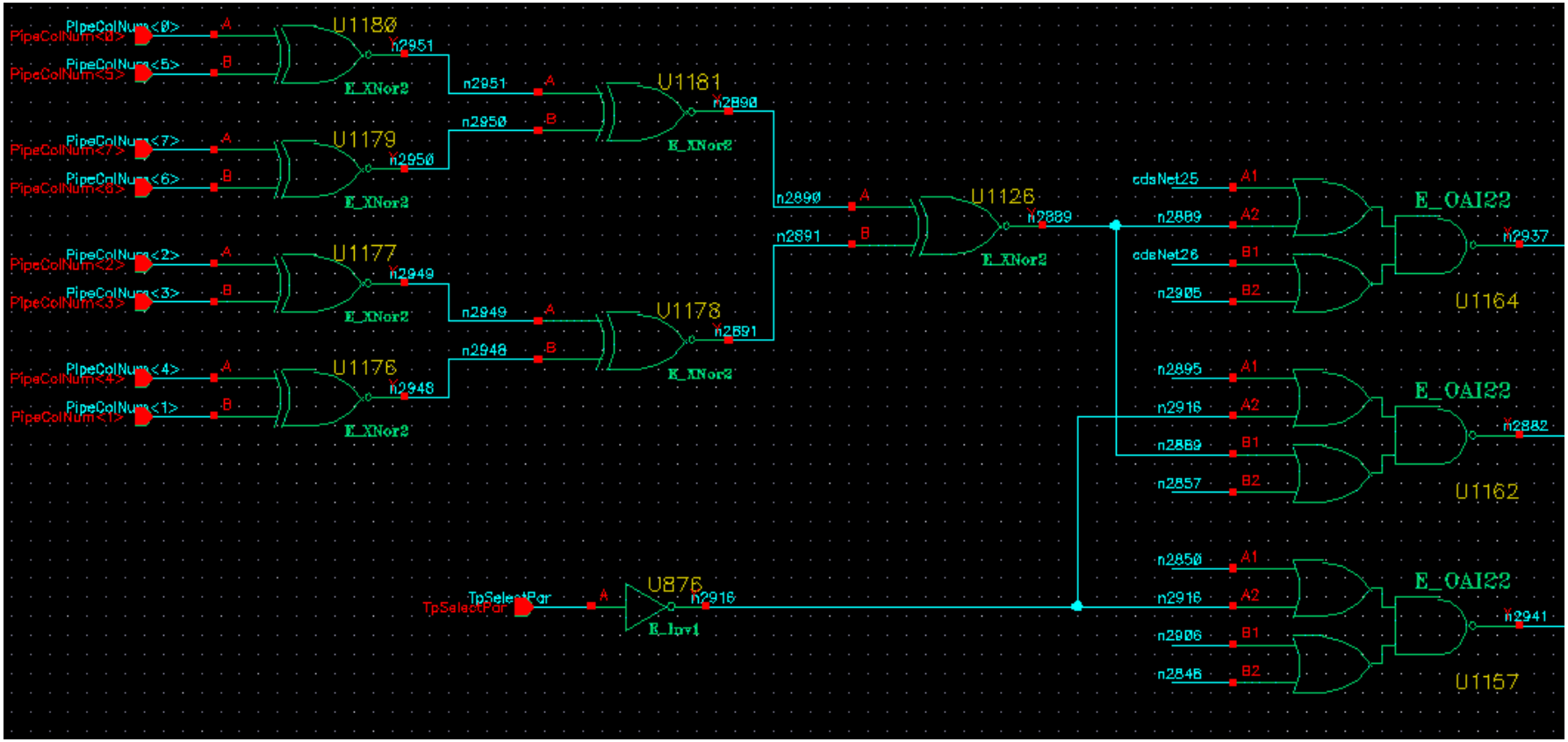
I0	leading bit (always 0)
I1	parity of PCN (even)
I2	Active EDC
I3	parity of reg. CompChTh
I4	parity of reg. CompMask
I5	parity of reg. TpSelect
I6	SEU counter <1>
I7	SEU counter <0>

- **Parity bit (I1) is wrong encoded in 4 port mode and Rclk divider = 0 (LHCb mode)**

  all other modes or Rclk divider settings
  ➔ Parity bit is OK

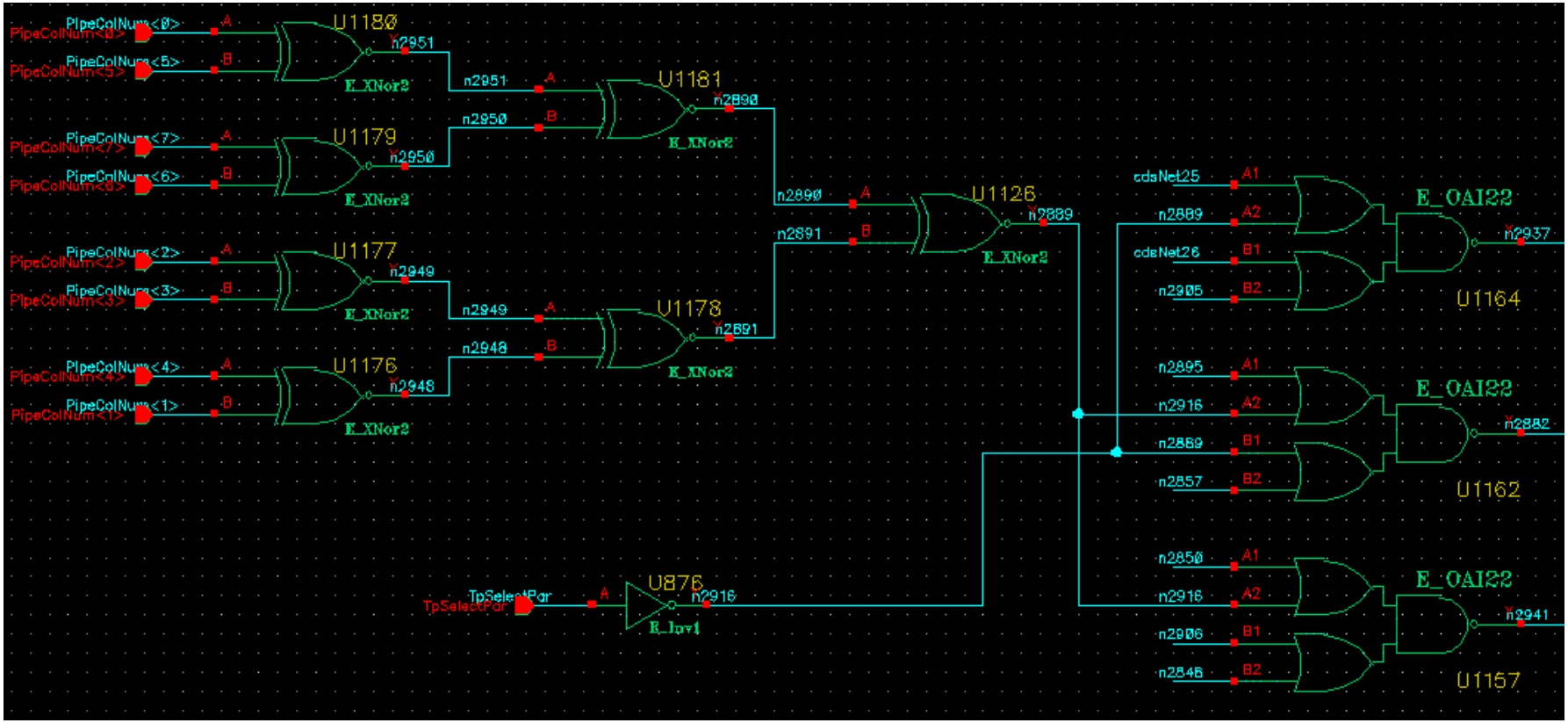
- **problem is understood in verilog**
  - **not so easy to fix**
  - **simple workaround: swap position I1 with I5 could be tested on a 1.3 with a FIB patch**

Parity bit - workaround (1)



schematic of parity-bit generation (part of MuxScheduler)

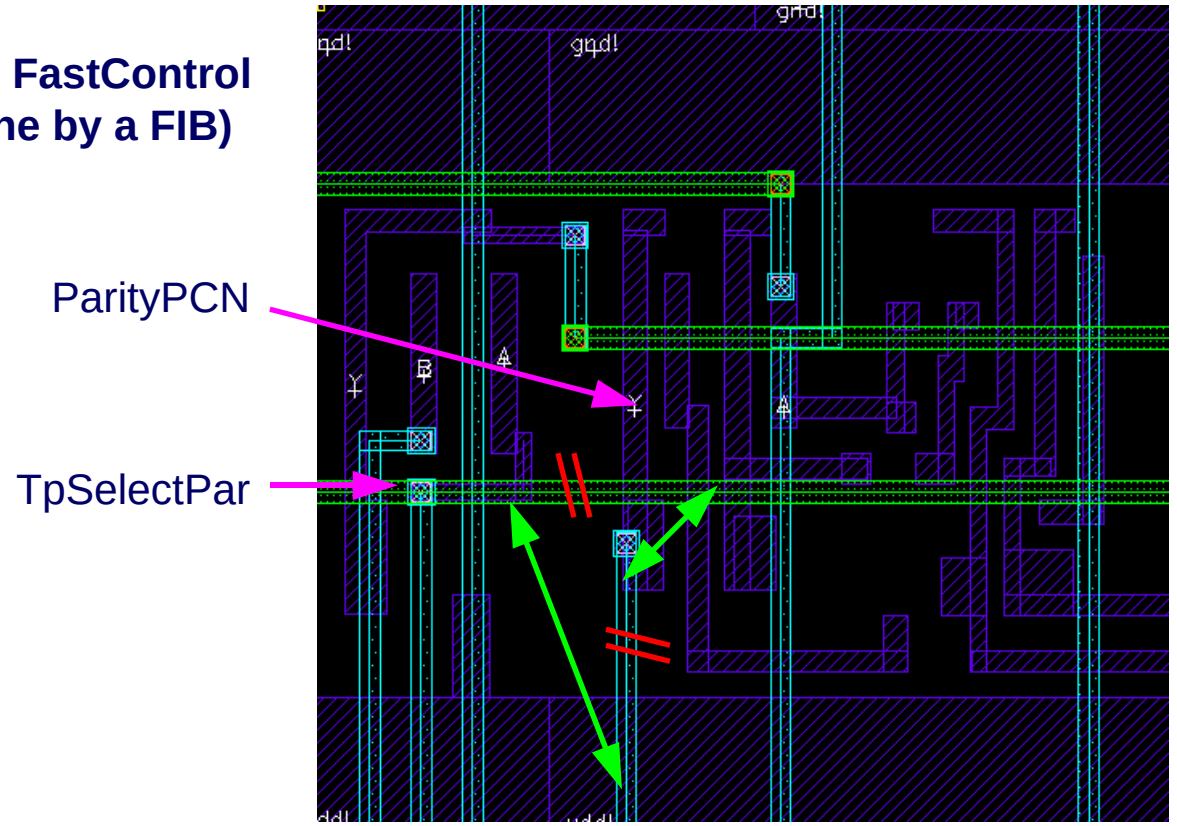
Parity bit - workaround (2)



new schematic of parity-bit patch

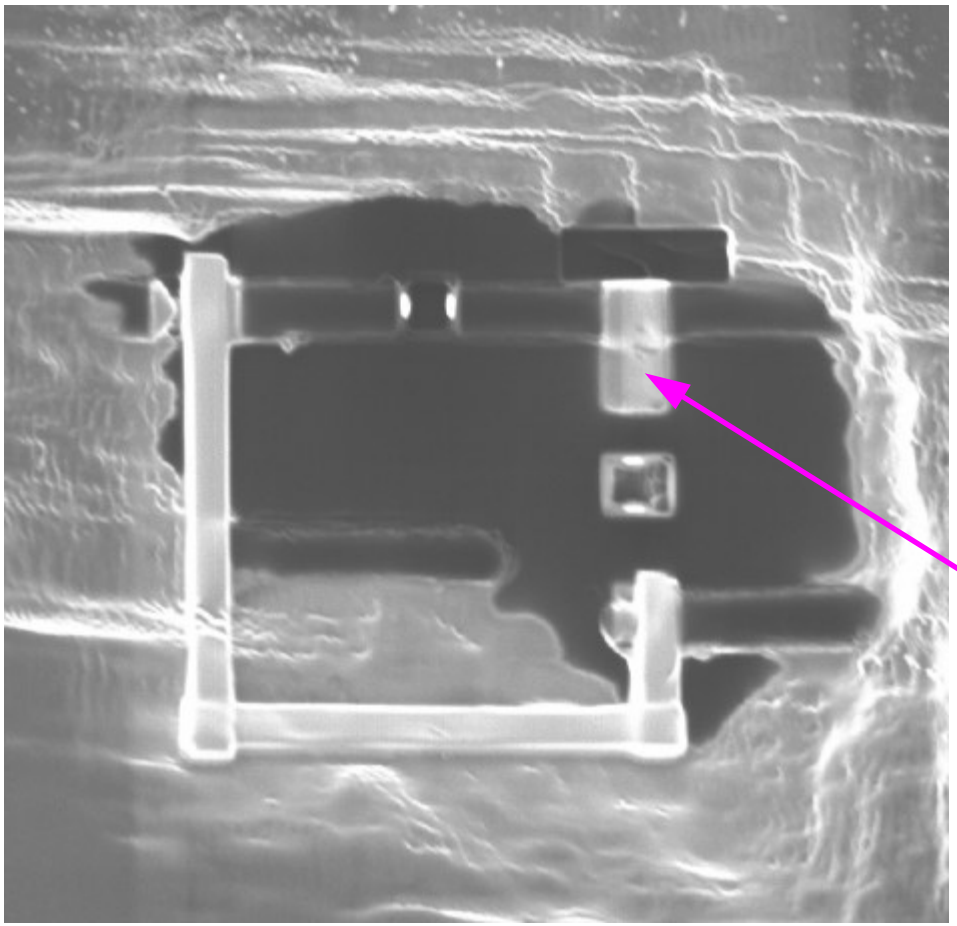
Parity bit - workaround (3)

- **Layout modification in FastControl of Beetle (could be done by a FIB)**
  - **2 cuts**
  - **2 connections**



Output device of ParityPCN generation - E_XNor2 (U1126)

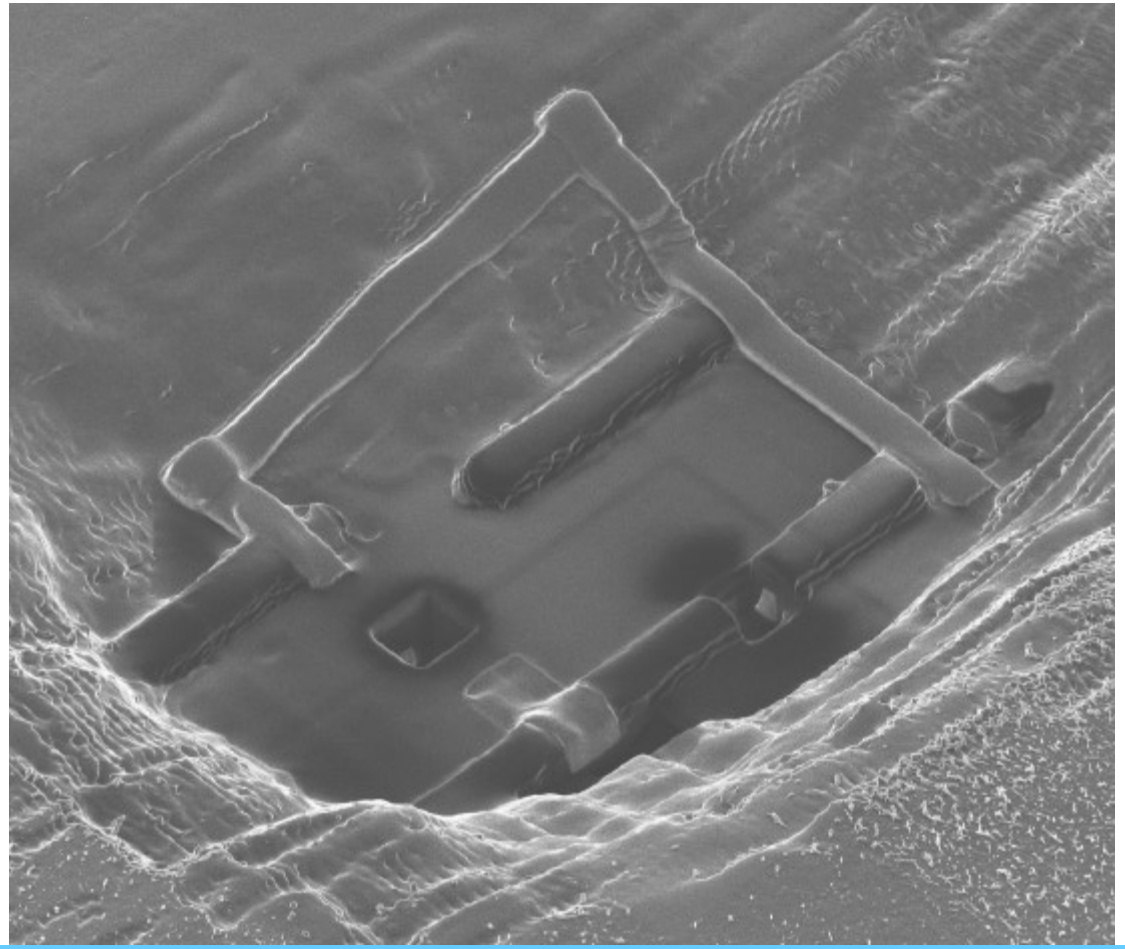
FIB patch (1)



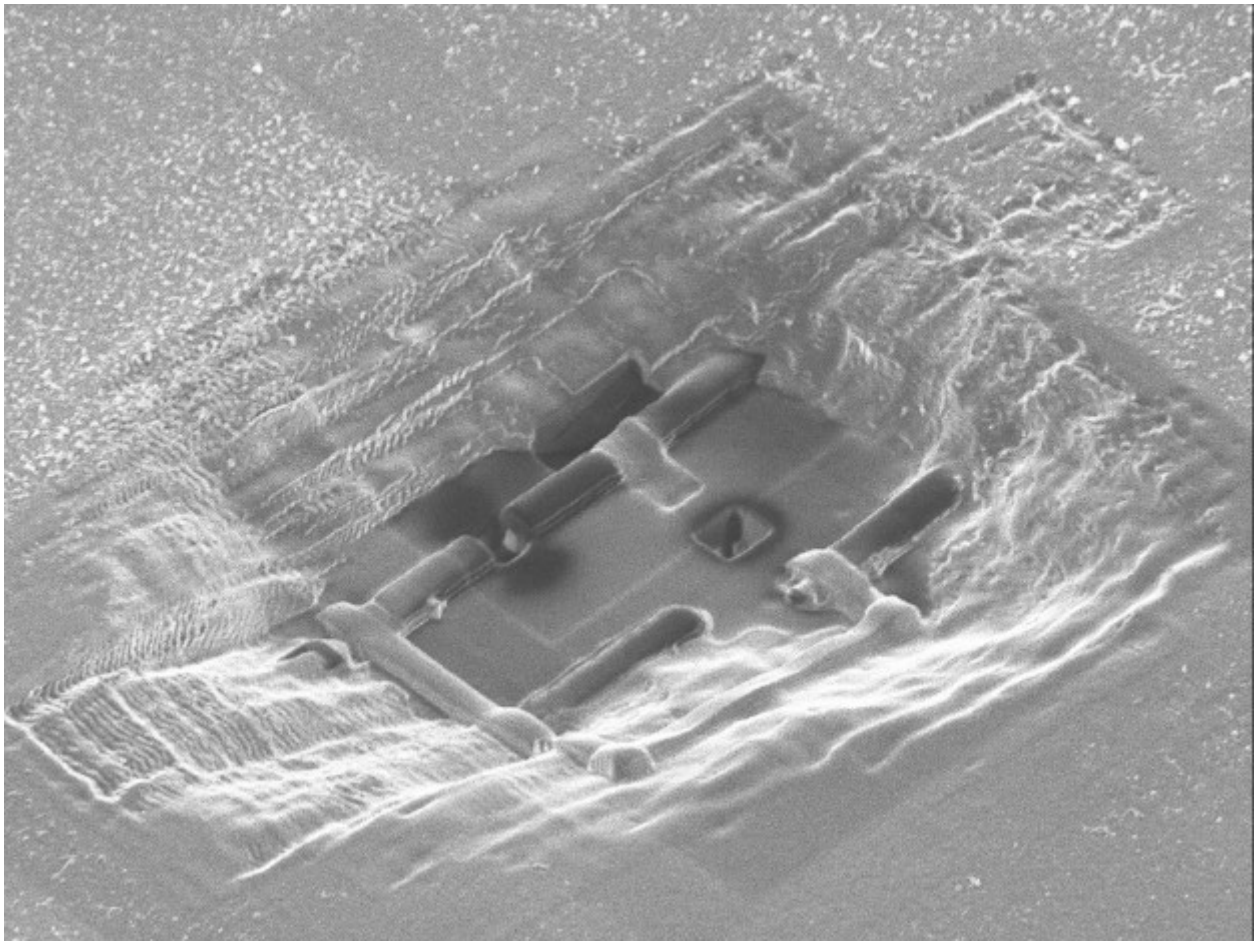
- **Swap header bit I1 with I5**
- **done with a FIB patch (FEICO Munich)**

Output device of ParityPCN generation - E_XNor2 (U1126)

FIB patch (2)



FIB patch (3)



Outlook

- **Beetle 1.3 was tested and characterized substantially in the lab.**
- **Up to now no bugs were found on the chip which would prevent a use of the Beetle in LHCb.**

next steps:

- **Preparation of Engineering run in May 2004**
  - **untouched version of Beetle 1.3**

  and
  - **slightly modified Beetle 1.4 (parity of PCN, cross-talk in pipeline)**