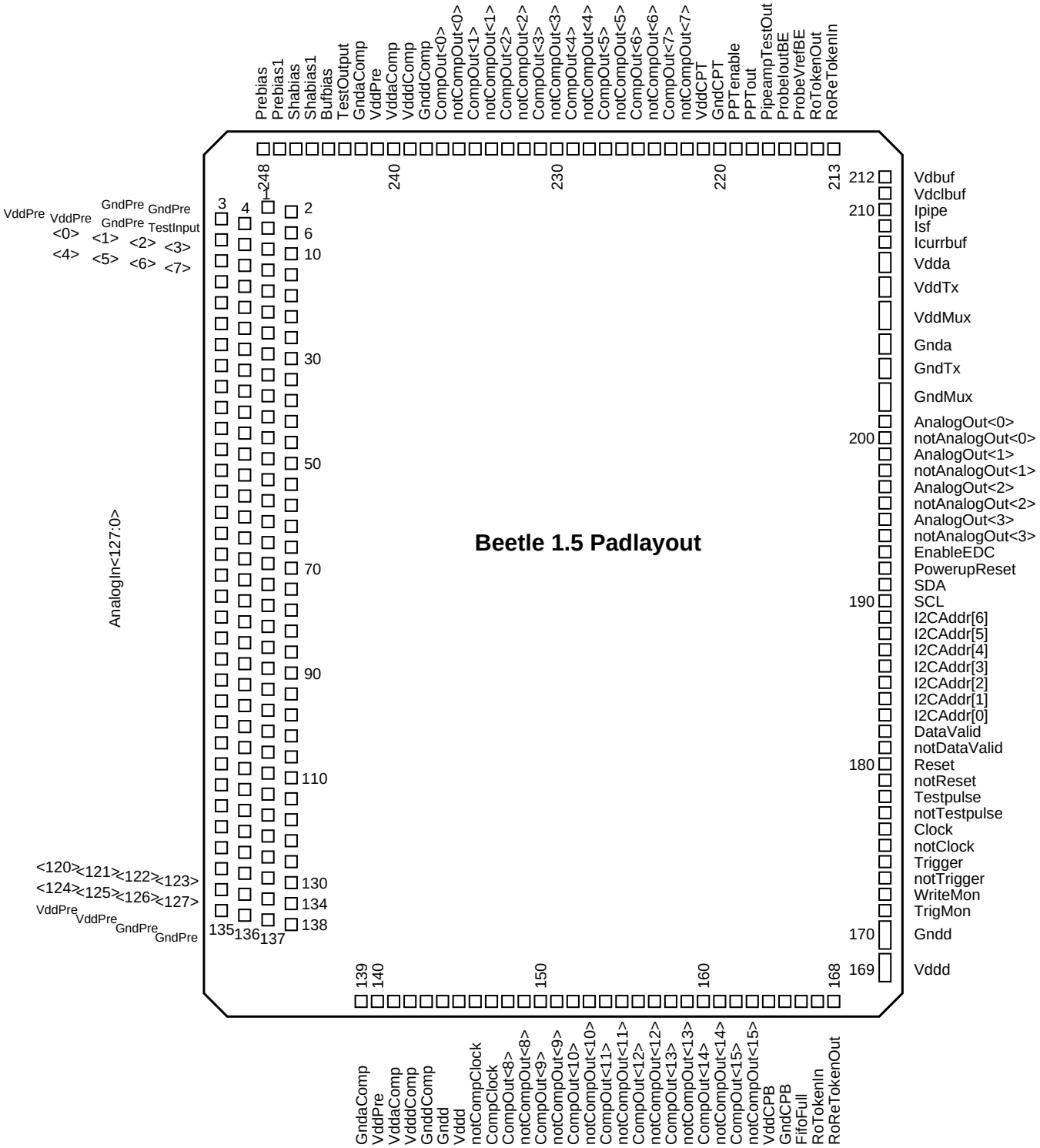
Beetle 1.5 Padlayout
Prebias
Prebias1
Shabias
Shabias1
Bufbias
TestOutput
GndaComp
VddPre
VddaComp
VdddComp
GnddComp
CompOut<0>
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CompOut<1>
notCompOut<1>
CompOut<2>
notCompOut<2>
CompOut<3>
notCompOut<3>
CompOut<4>
notCompOut<4>
CompOut<5>
notCompOut<5>
CompOut<6>
notCompOut<6>
CompOut<7>
notCompOut<7>
VddCPT
GndCPT
PPTenable
PPTout
PipeampTestOut
ProbeloutBE
ProbeVrefBE
RoTokenOut
RoReTokenIn
Vdbuf
Vdclbuf
Ipipe
Isf
Icurrbuf
Vdda
VddTx
VddMux
Gnda
GndTx
GndMux
AnalogOut<0>
notAnalogOut<0>
AnalogOut<1>
notAnalogOut<1>
AnalogOut<2>
notAnalogOut<2>
AnalogOut<3>
notAnalogOut<3>
EnableEDC
PowerupReset
SDA
SCL
I2CAddr[6]
I2CAddr[5]
I2CAddr[4]
I2CAddr[3]
I2CAddr[2]
I2CAddr[1]
I2CAddr[0]
DataValid
notDataValid
Reset
notReset
Testpulse
notTestpulse
Clock
notClock
Trigger
notTrigger
WriteMon
TrigMon
Gndd
Vddd
GndaComp
VddPre
VddaComp
VdddComp
GnddComp
Gndd
Vddd
notCompClock
CompClock
CompOut<8>
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CompOut<9>
notCompOut<9>
CompOut<10>
notCompOut<10>
CompOut<11>
notCompOut<11>
CompOut<12>
notCompOut<12>
CompOut<13>
notCompOut<13>
CompOut<14>
notCompOut<14>
CompOut<15>
notCompOut<15>
VddCPB
GndCPB
FifoFull
RoTokenIn
RoReTokenOut
VddPre
VddPre <0>
GndPre <1>
GndPre <2>
GndPre TestInput <3>
<4>
<5>
<6>
<7>
AnalogIn<127:0>
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<125>
<126>
<127>
VddPre
VddPre
GndPre
GndPre
1
2
3
4
6
10
30
50
70
90
110
130
134
138
135
136
137
139
140
150
160
168
169
170
180
190
200
210
212
213
220
230
240
248