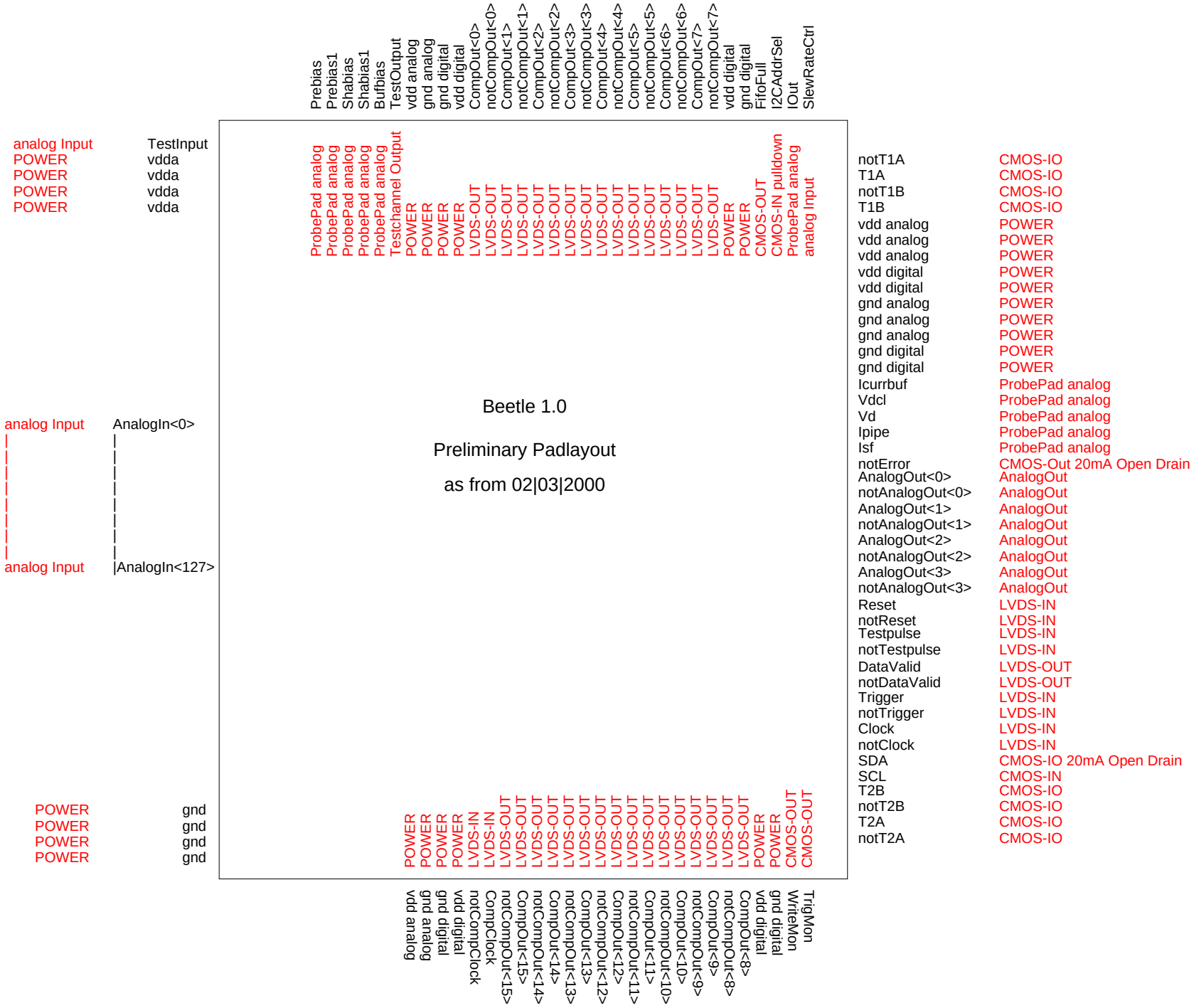
Beetle 1.0
Preliminary Padlayout
as from 02|03|2000
analog Input TestInput
POWER vdda
POWER vdda
POWER vdda
POWER vdda
analog Input AnalogIn<0>
analog Input AnalogIn<127>
POWER gnd
POWER gnd
POWER gnd
POWER gnd
Prebias ProbePad analog
Prebias1 ProbePad analog
Shabias ProbePad analog
Shabias1 ProbePad analog
Bufbias ProbePad analog
TestOutput Testchannel Output
vdd analog POWER
gnd analog POWER
gnd digital POWER
vdd digital POWER
CompOut<0> LVDS-OUT
notCompOut<0> LVDS-OUT
CompOut<1> LVDS-OUT
notCompOut<1> LVDS-OUT
CompOut<2> LVDS-OUT
notCompOut<2> LVDS-OUT
CompOut<3> LVDS-OUT
notCompOut<3> LVDS-OUT
CompOut<4> LVDS-OUT
notCompOut<4> LVDS-OUT
CompOut<5> LVDS-OUT
notCompOut<5> LVDS-OUT
CompOut<6> LVDS-OUT
notCompOut<6> LVDS-OUT
CompOut<7> LVDS-OUT
notCompOut<7> LVDS-OUT
vdd digital POWER
gnd digital POWER
FifoFull CMOS-OUT
I2CAddr-Sel CMOS-IN pulldown
IOut ProbePad analog
SlewRateCtrl analog Input
POWER vdd analog
POWER gnd analog
POWER gnd digital
POWER vdd digital
LVDS-IN notCompClock
LVDS-IN CompClock
LVDS-OUT notCompOut<15>
LVDS-OUT CompOut<15>
LVDS-OUT notCompOut<14>
LVDS-OUT CompOut<14>
LVDS-OUT notCompOut<13>
LVDS-OUT CompOut<13>
LVDS-OUT notCompOut<12>
LVDS-OUT CompOut<12>
LVDS-OUT notCompOut<11>
LVDS-OUT CompOut<11>
LVDS-OUT notCompOut<10>
LVDS-OUT CompOut<10>
LVDS-OUT notCompOut<9>
LVDS-OUT CompOut<9>
LVDS-OUT notCompOut<8>
LVDS-OUT CompOut<8>
POWER vdd digital
POWER gnd digital
CMOS-OUT WriteMon
CMOS-OUT TrigMon
notT1A CMOS-IO
T1A CMOS-IO
notT1B CMOS-IO
T1B CMOS-IO
vdd analog POWER
vdd analog POWER
vdd analog POWER
vdd digital POWER
vdd digital POWER
gnd analog POWER
gnd analog POWER
gnd analog POWER
gnd digital POWER
gnd digital POWER
Icurrbuf ProbePad analog
Vdcl ProbePad analog
Vd ProbePad analog
Ipipe ProbePad analog
Isf ProbePad analog
notError CMOS-Out 20mA Open Drain
AnalogOut<0> AnalogOut
notAnalogOut<0> AnalogOut
AnalogOut<1> AnalogOut
notAnalogOut<1> AnalogOut
AnalogOut<2> AnalogOut
notAnalogOut<2> AnalogOut
AnalogOut<3> AnalogOut
notAnalogOut<3> AnalogOut
Reset LVDS-IN
notReset LVDS-IN
Testpulse LVDS-IN
notTestpulse LVDS-IN
DataValid LVDS-OUT
notDataValid LVDS-OUT
Trigger LVDS-IN
notTrigger LVDS-IN
Clock LVDS-IN
notClock LVDS-IN
SDA CMOS-IO 20mA Open Drain
SCL CMOS-IN
T2B CMOS-IO
notT2B CMOS-IO
T2A CMOS-IO
notT2A CMOS-IO