Lab measurements with the Beetle 1.3

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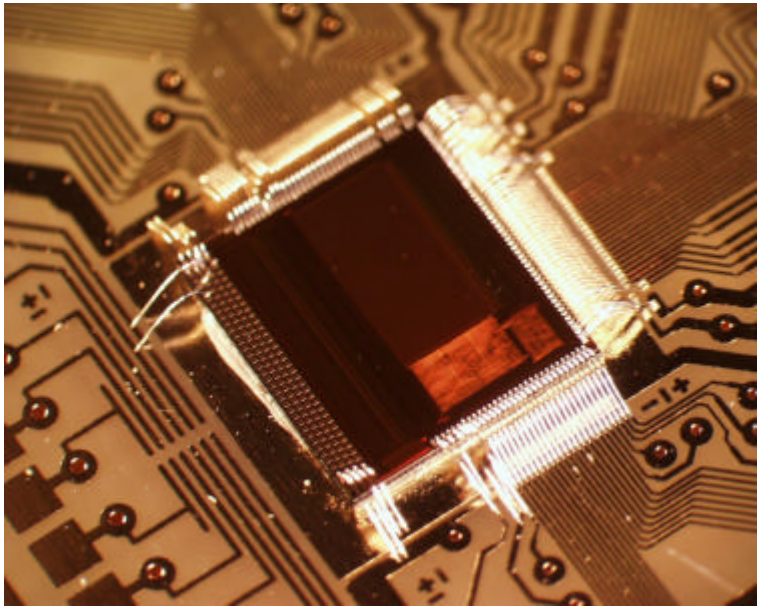

Beetle 1.3 on a test PCB

Motivation for Beetle 1.3

in descending order of priority:

- **Sticky Charge Effect**
- **Comparator Offset Variation**
- **80 MHz Crosstalk**
- **Output Driver Performance**
- **Sagging Readout Baseline**
- **5V tolerant I²C pads**
- **...**

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Modifications in Beetle 1.3

- **Design changes (on schematic level)**
  - **analog delay of MuxTrack signal (sticky charge)**
  - **improved comparator (5 bit threshold / channel)**
  - **Current Output Buffer (inc. gain / diff. output)**
  - **Multiplexer (reduction of switching spikes)**
  - **Control Logic (bug fixes, daisy chain, low-Rclk)**
  - **new I²C-Pads (5V compatible)**
  - **modified Testpulse pattern (“+1/-1” pattern)**
- **Layout and Power Routing**
  - **modified front-end power pads**
  - **improved front-end routing / bias**
  - **separation of comparator core power / LVDS**
  - **improved pipeamp power routing**
  - **on-chip power blocking / additional pads**
- **Crosstalk measures**
  - **reduced no. of FF in MUX**
  - **reduced no. of clock buffers**
  - **on-chip power blocking**

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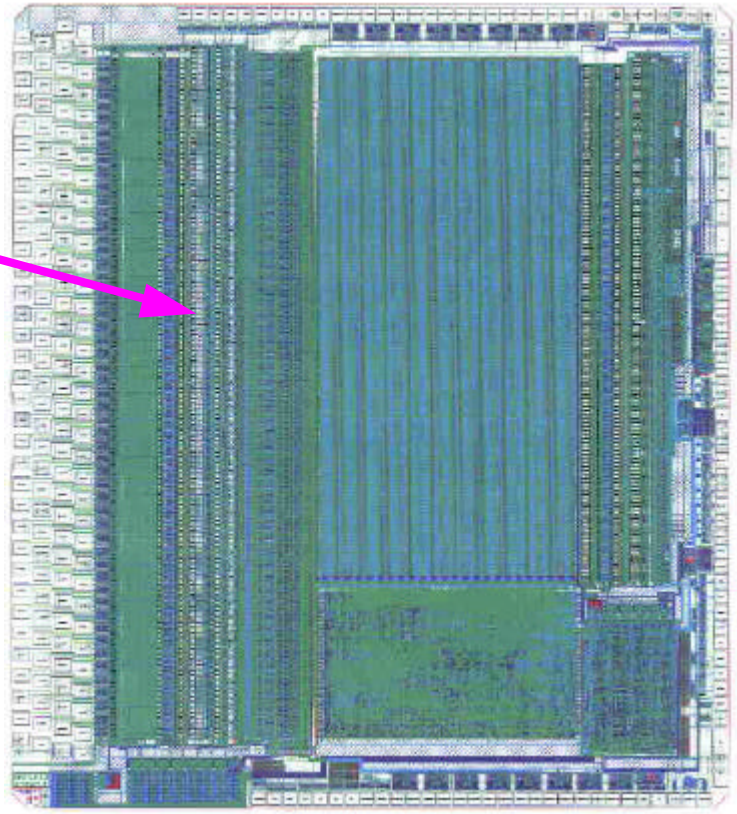
Motivation for Beetle 1.3

Result of hard design work



Beetle 1.3 layout

- **30.06.2003 Submission of Beetle 1.3**
- **22.09.2003 Beetle arrived in Heidelberg**

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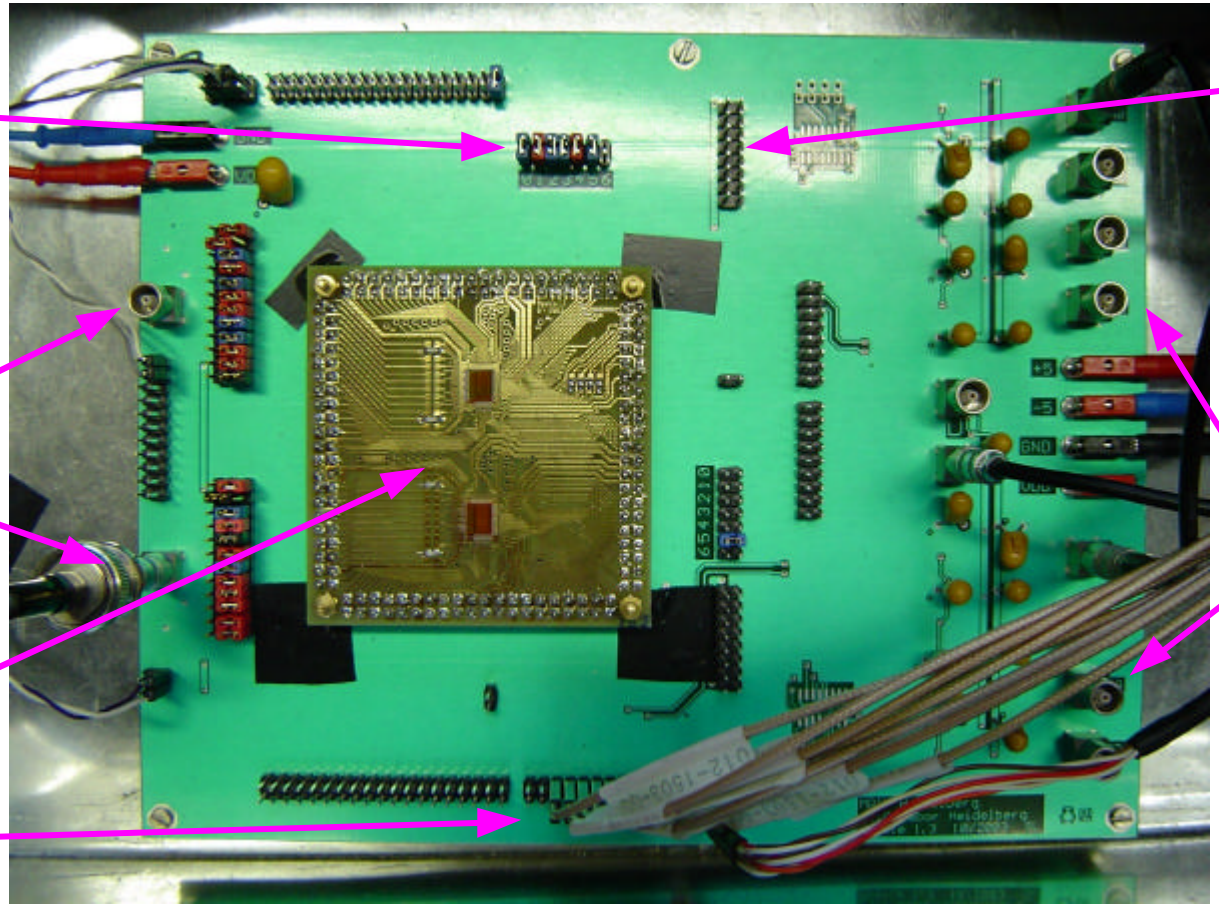
Beetle 1.3 Lab Setup (1)



top view

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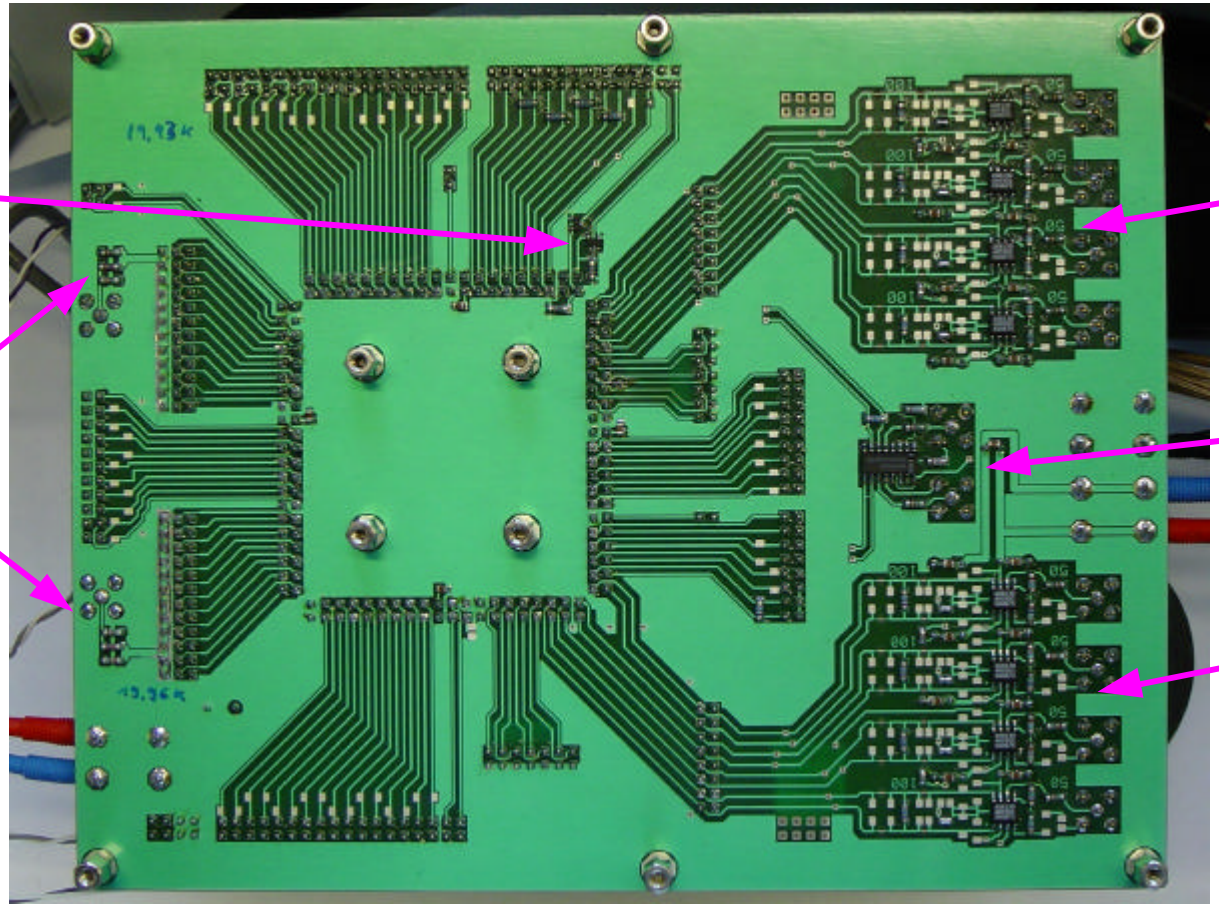
Beetle 1.3 Lab Setup (2)

I²C level shifter
(unnecessary for Beetle 1.3)

Analog In
Voltage divider



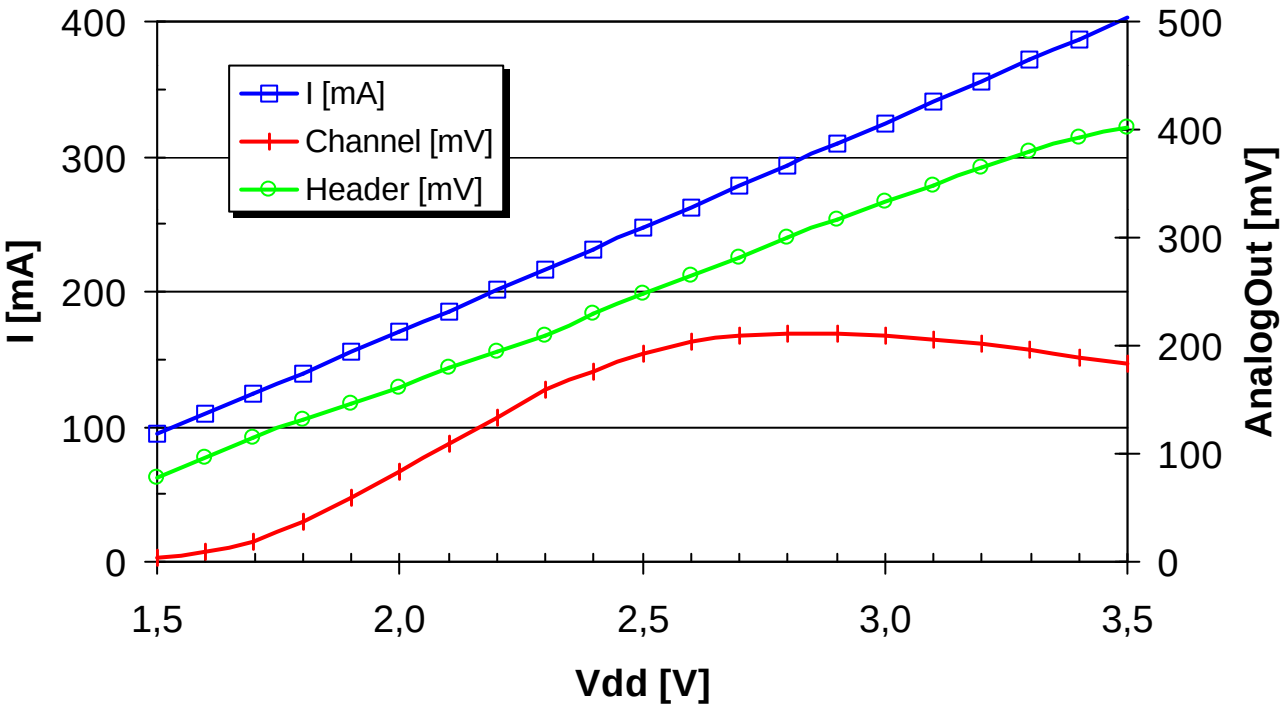
4 Analog Receiver for 2nd Beetle
(AD8130)

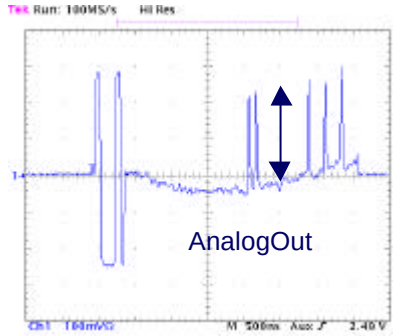
LVDS receiver
(DS90C032)

4 Analog receiver for 1st Beetle
(AD8130)

bottom view

Power Supply Operation





- **Analog / Digital: 1.5V to 3.5V**

Total Power Consumption (1)

Power consumption [mW/ch.]	Minimal	Nominal			Max. operation			Max. DAC
#AO drivers	0	0	1	4	0	1	4	4
without clock	**0,48**	3,49	3,68	**4,25**	4,76	5,02	**5,83**	**14,21**
only 40 MHz clock	**1,26**	4,28	4,46	**5,03**	5,54	5,81	**6,61**	**14,95**
clocked + 1.1 MHz trigger	**1,26**	4,36	4,56	**5,14**	5,62	5,90	**6,70**	**15,12**

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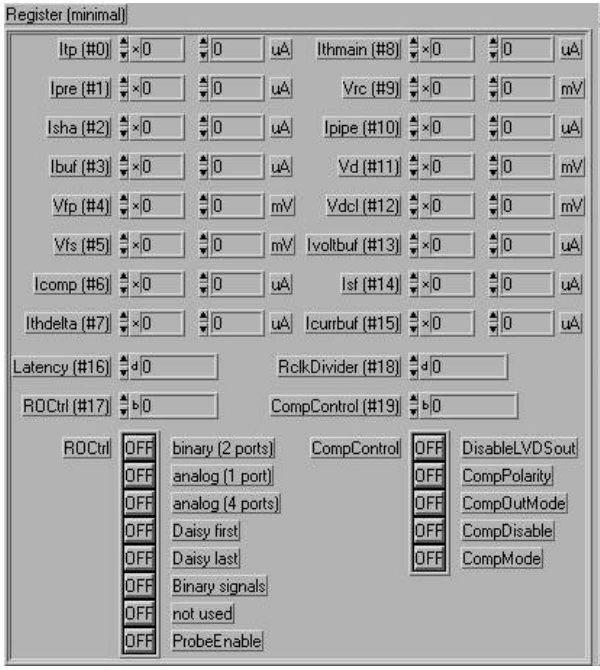
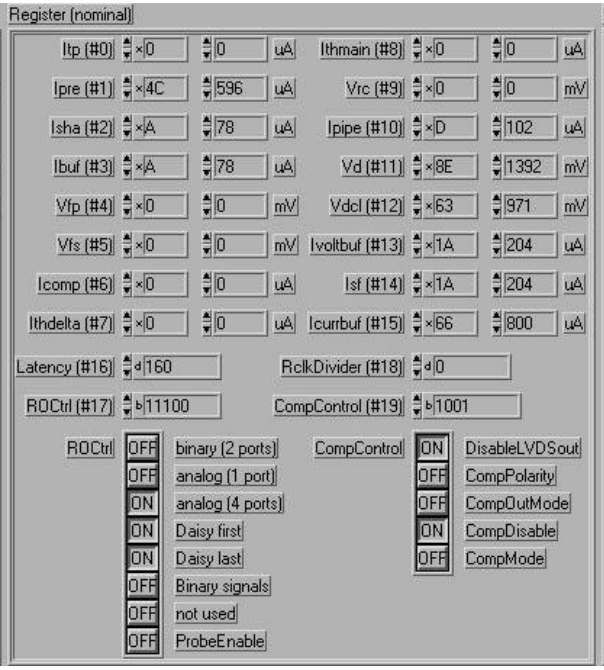
Total Power Consumption (2)

I²C DAC Settings

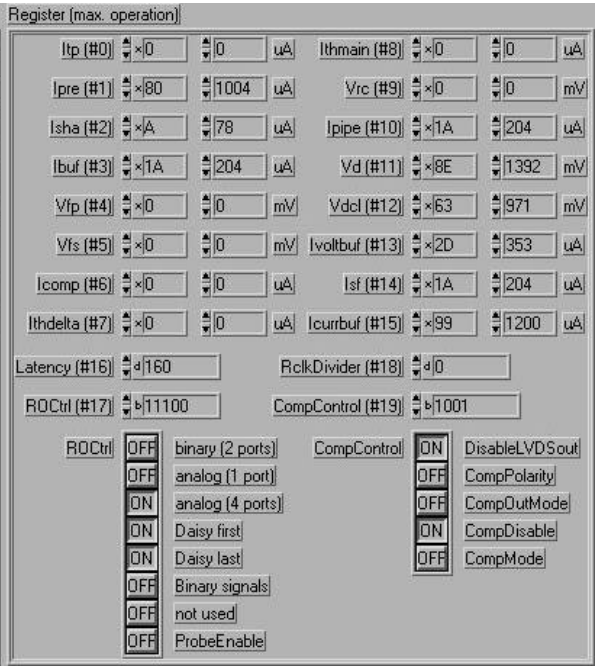
minimal



nominal



max. reasonable values



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Temperature Test

- **Start-up tests (~ 15 times each chip):**
  - **2 Beetle 1.3**
  - **@ T= -44°C, 60°C, 75°C** (facility temperature)
  - **Programming (I^2C)**
  - **1.1 MHz trigger + analog readout**
- **Longtime operating tests (~3 days):**
  - **1 Beetle 1.3**
  - **@ T= -44°C, 60°C, 75°C ($T_{surface}$= -4°C, 94°C, 107°C)**
  - **1.1 MHz + analog readout**
- **Max. stress test:**
  - **1 Beetle 1.3**
  - **max. DAC settings**
  - **@ T= 60°C (Þ $T_{surface}$= 126°C)**
  - **Operating over ~ 12 hour**

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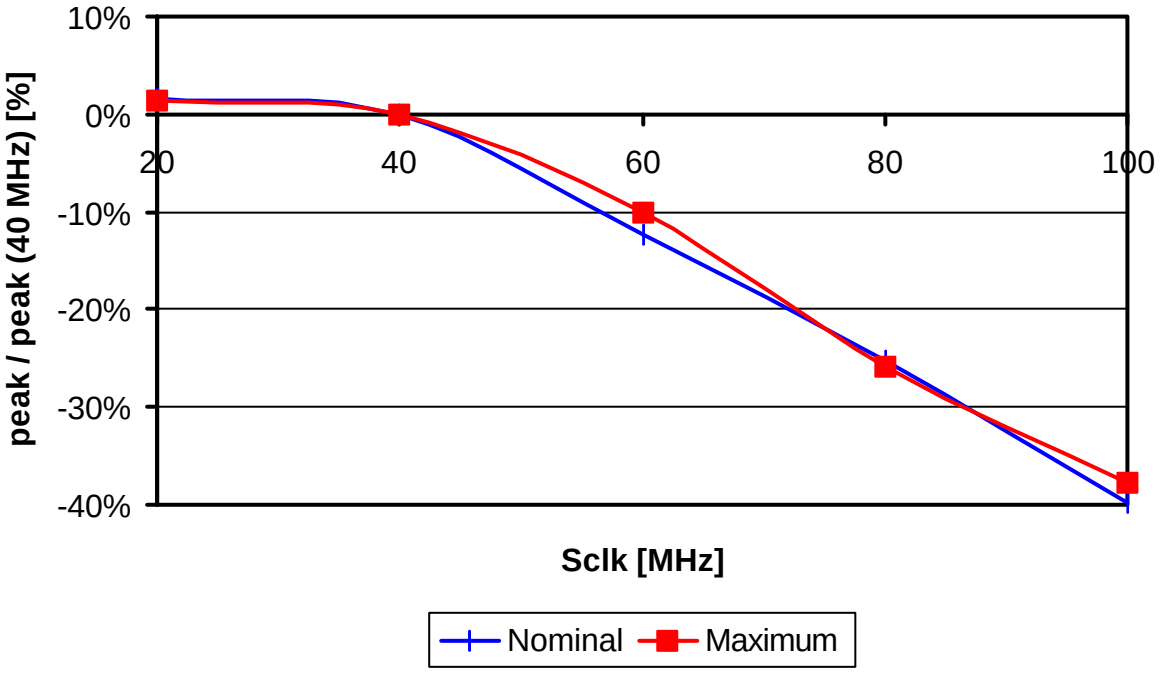
Overclocking Test



frequency test

- **Digital: perfect operation up to 100 MHz**
- **Analog: nearly 40% gain loss @ 100 MHz**

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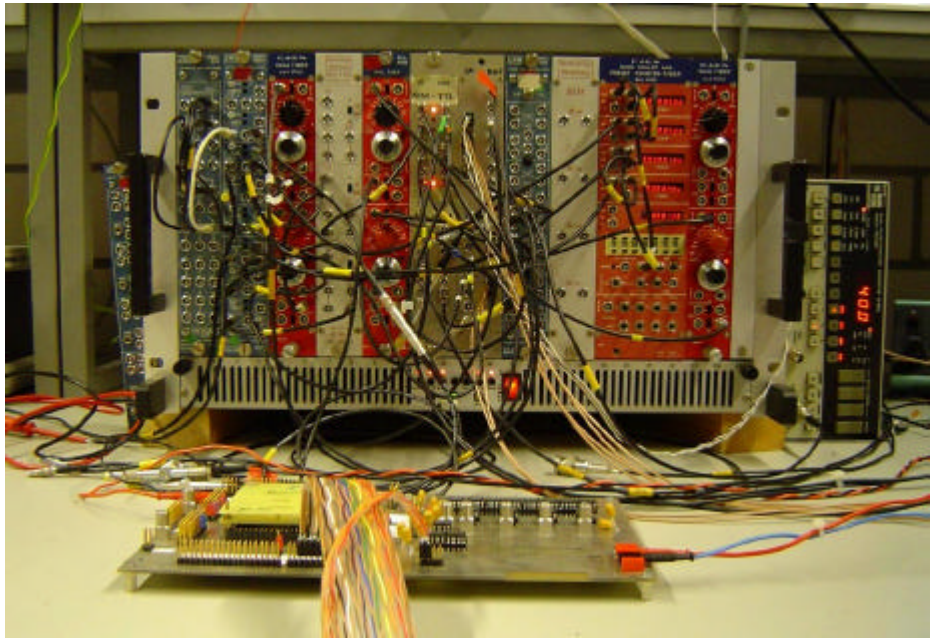
Random Trigger Test

- 2 Beetle 1.3 @ 40 MHz
- 2 x 2.34 · 10^{12} random triggers
  - 172h (1.778 · 10^{12}, Þ 2.87 MHz)
  - 75h (3.039 · 10^{11}, Þ 1.12 MHz)
  - 92h (2.550 · 10^{11}, Þ 0.77 MHz)
- no triggers lost



Beetle 1.3 random trigger test setup

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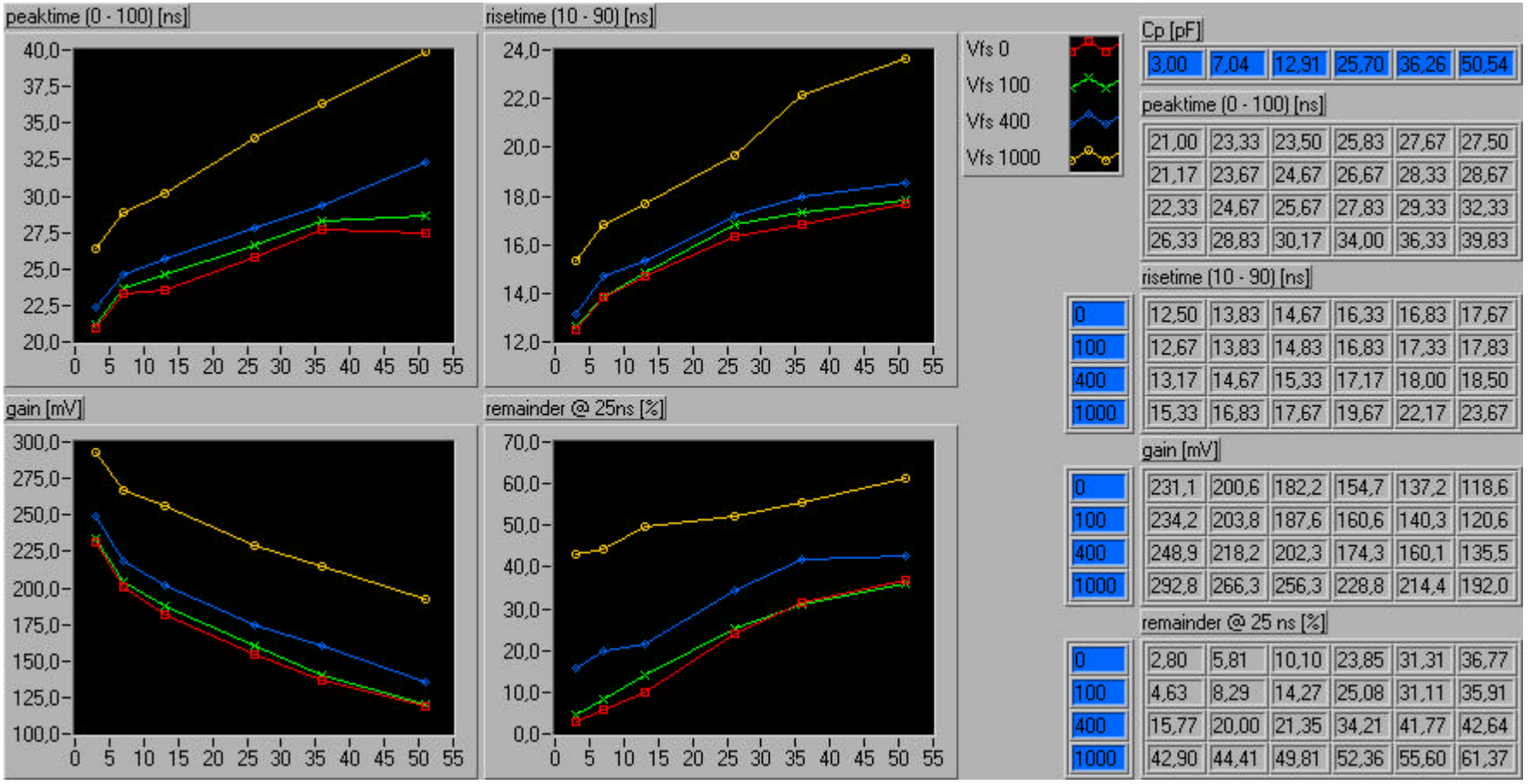
Front end: Pulse-Parameter



Cp [pF]

3,00	7,04	12,91	25,70	36,26	50,54

peaktime (0 - 100) [ns]

21,00	23,33	23,50	25,83	27,67	27,50
21,17	23,67	24,67	26,67	28,33	28,67
22,33	24,67	25,67	27,83	29,33	32,33
26,33	28,83	30,17	34,00	36,33	39,83

risetime (10 - 90) [ns]

0	12,50	13,83	14,67	16,33	16,83	17,67
100	12,67	13,83	14,83	16,83	17,33	17,83
400	13,17	14,67	15,33	17,17	18,00	18,50
1000	15,33	16,83	17,67	19,67	22,17	23,67

gain [mV]

0	231,1	200,6	182,2	154,7	137,2	118,6
100	234,2	203,8	187,6	160,6	140,3	120,6
400	248,9	218,2	202,3	174,3	160,1	135,5
1000	292,8	266,3	256,3	228,8	214,4	192,0

remainder @ 25 ns [%]

0	2,80	5,81	10,10	23,85	31,31	36,77
100	4,63	8,29	14,27	25,08	31,11	35,91
400	15,77	20,00	21,35	34,21	41,77	42,64
1000	42,90	44,41	49,81	52,36	55,60	61,37

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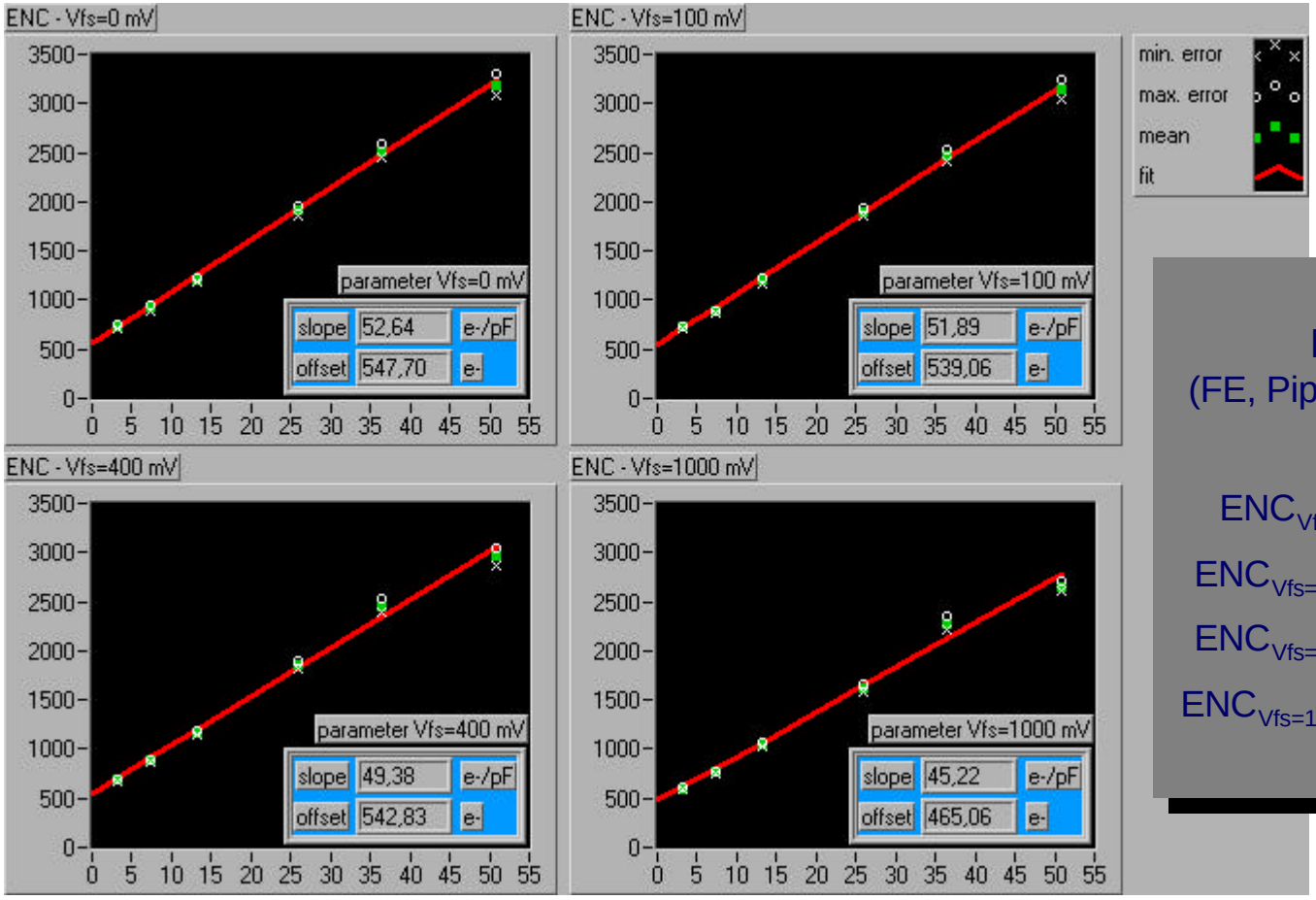
Front end: ENC - Beetle 1.3



Beetle 1.3 ENC
(FE, Pipeline, Pipeamp, Readout)

$ENC_{Vfs=0}$: 547.7 e^- + 52.6 e^-/pF

$ENC_{Vfs=100}$: 539.1 e^- + 51.9 e^-/pF

$ENC_{Vfs=400}$: 542.8 e^- + 49.9 e^-/pF

$ENC_{Vfs=1000}$: 465.1 e^- + 45.2 e^-/pF

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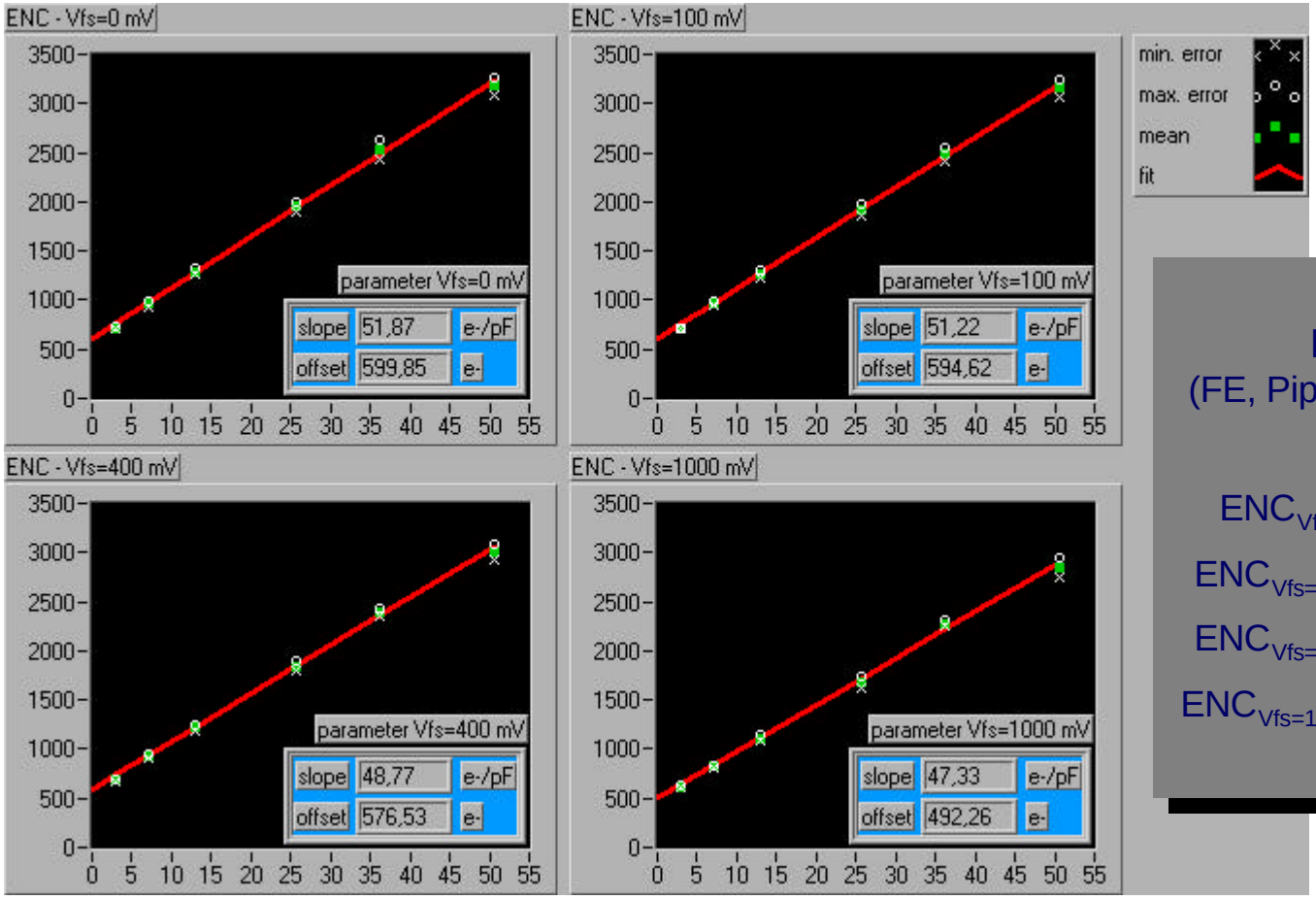
Front end: ENC - Beetle 1.2



Beetle 1.2 ENC
(FE, Pipeline, Pipeamp, Readout)

$ENC_{Vfs=0}$: 599.9 e^- + 51.9 e^-/pF

$ENC_{Vfs=100}$: 594.6 e^- + 51.2 e^-/pF

$ENC_{Vfs=400}$: 576.5 e^- + 48.8 e^-/pF

$ENC_{Vfs=1000}$: 492.3 e^- + 47.3 e^-/pF

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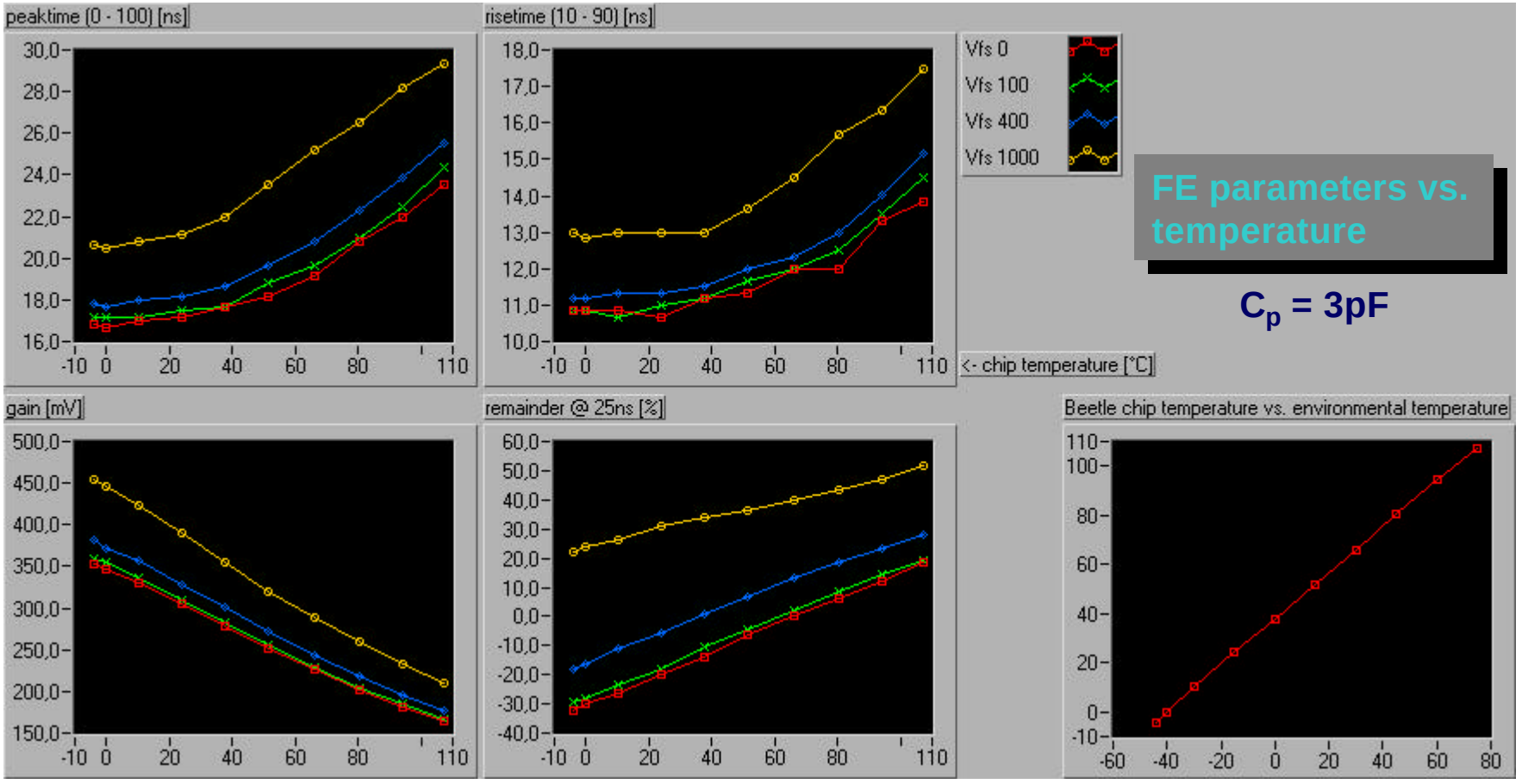
Front end: Temperature (1)



FE parameters vs. temperature

C_p = 3pF

I²C - Input Pads

New 5V tolerant I²C-Pads for Beetle 1.3

- **SCL / SDA input level tested:**
  min. HIGH: 1.5V
  max. HIGH: 7.0V (only tested up to 7.0V)

  min. LOW: -0.7V
  max. LOW: 1.1V @ 2.5V HIGH level
  1.2V @ 3.3V
  1.3V @ 5.0V

- **SDA output delay (ACK): 500ns** (I²C specification: delay > 300ns)

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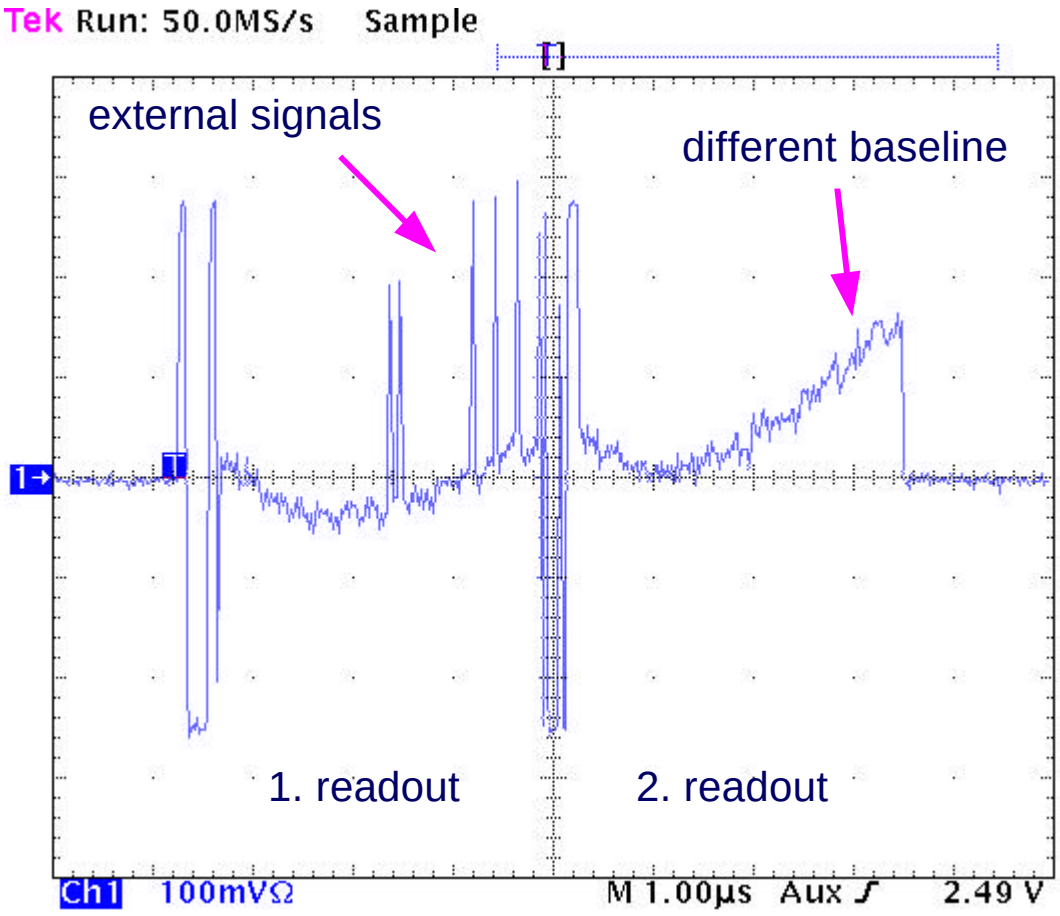
Sticky Charge



Consecutive readout

- **External signals on 5 channel in 1st readout frame**
- **No sticky charge in 2nd readout frame**

  but still a different baseline

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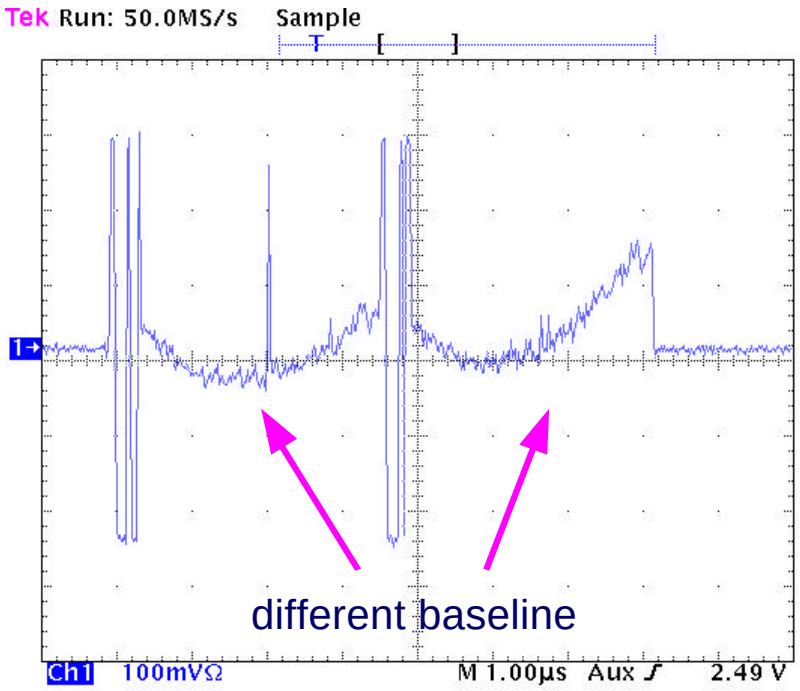
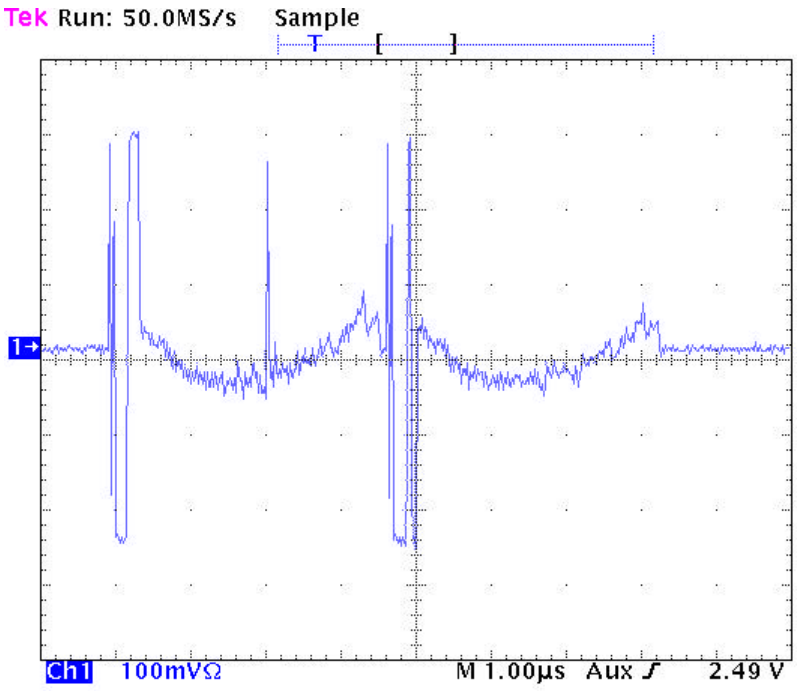
Readout

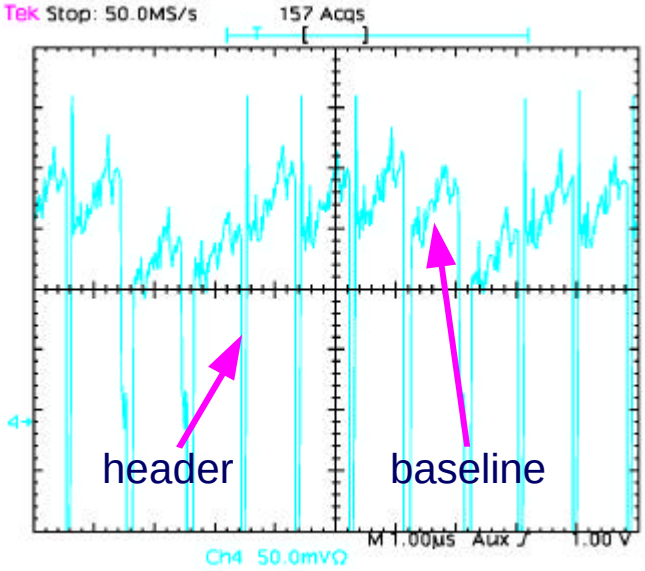


consecutive readout



non-consecutive readout

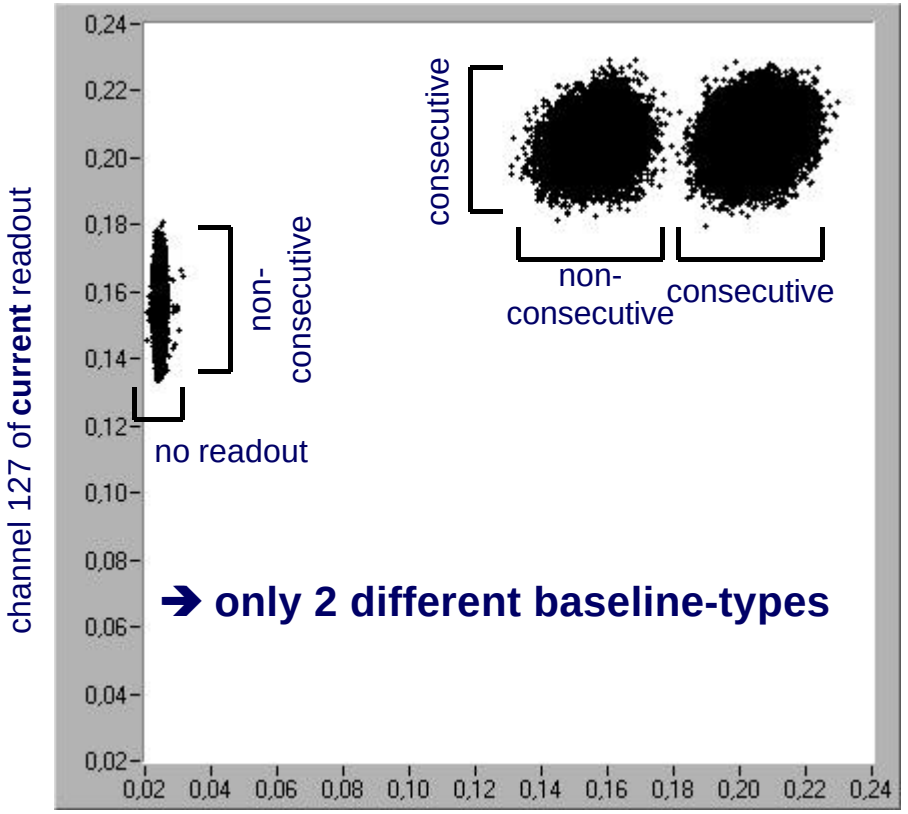
Readout (Baseline)



AnalogOut<3> - channel 96 to 127

- **32 channels on 4 port (LHCb-mode)**
- **non-consecutive & consecutive RO**

previous readout vs. current readout



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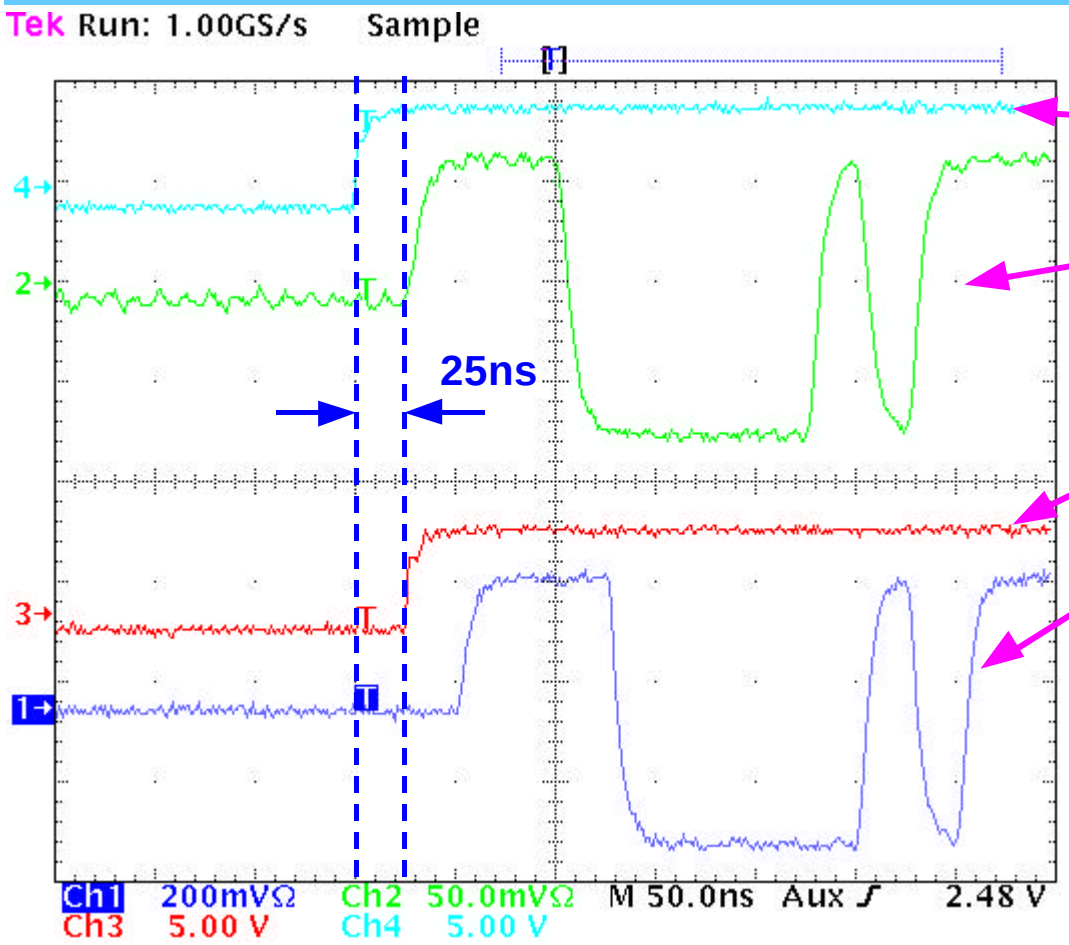
Readout Beetle 1.2 <-> 1.3



DataValid Beetle 1.2

Analog Readout 1.2

DataValid Beetle 1.3

Analog Readout 1.3

Readout of Beetle 1.3 starts 25ns later than in version 1.2

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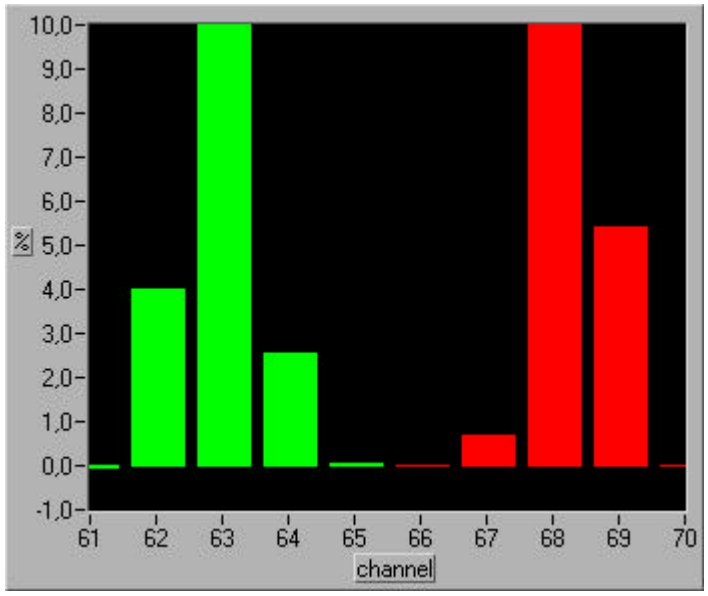
Channel Crosstalk (1)



Testpulse (63. & 68) is standardised to 100%

Channel crosstalk

- **measured a even/odd dependency**
- **this effect is also present in 1.2**

Clarification of crosstalk:

typical Testpulse for a odd channel (e.g. 63):
crosstalk into predecessor channel is larger than into successor channel

typical Testpulse for a even channel (e.g. 68):
crosstalk into successor channel is larger than into predecessor channel

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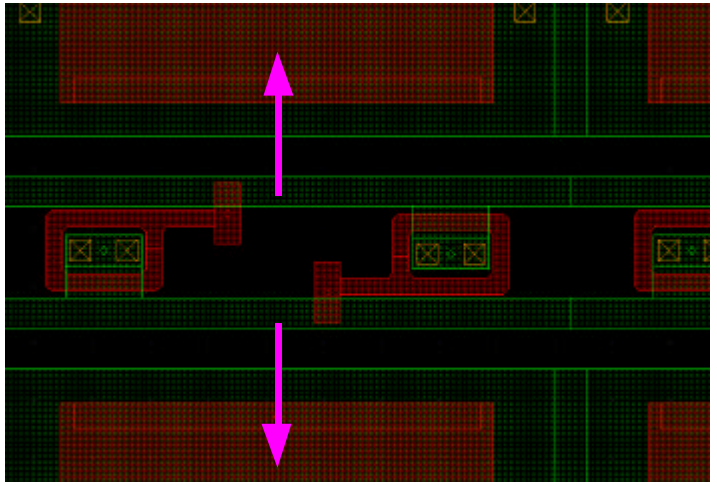
Channel Crosstalk (2)

Channel crosstalk is a superposition of at least two different crosstalks:

- **general “remainder” into next readout channel (order of 2% to 2.5%)**
  - **➔ reason not understood (maybe MUX?)**
- **odd channel: crosstalk into predecessor ch. even channel: crosstalk into successor ch. (order of 2.5 %)**
  - **➔ readout line from Pipeline into Pipeamp capacitance between adjacent lines ~ 60fF**
    - **verified in simulation**
    - **easy to fix (stretch lines)**



Readout header: parity bit

1 port mode

AO[0]	I0	I1	I2	I3	I4	I5	I6	I7	P7	P6	P5	P4	P3	P2	P1	P0

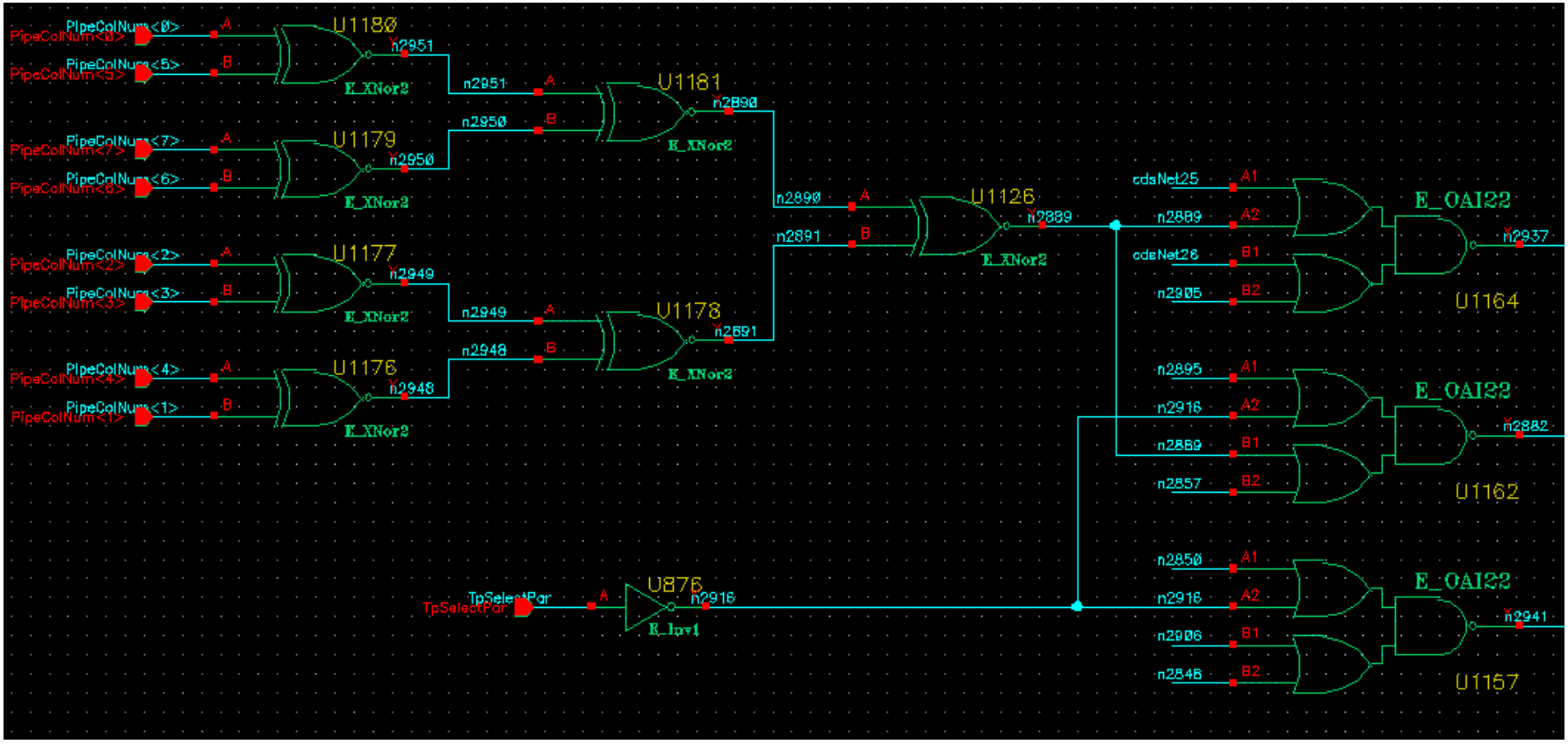
4 port mode

AO[0]	I0	I4	P1	P0
AO[1]	I1	I5	P3	P2
AO[2]	I2	I6	P5	P4
AO[3]	I3	I7	P7	P6

I0	leading bit (always 0)
I1	parity of PCN (even)
I2	Active EDC
I3	parity of reg. CompChTh
I4	parity of reg. CompMask
I5	parity of reg. TpSelect
I6	SEU counter <1>
I7	SEU counter <0>

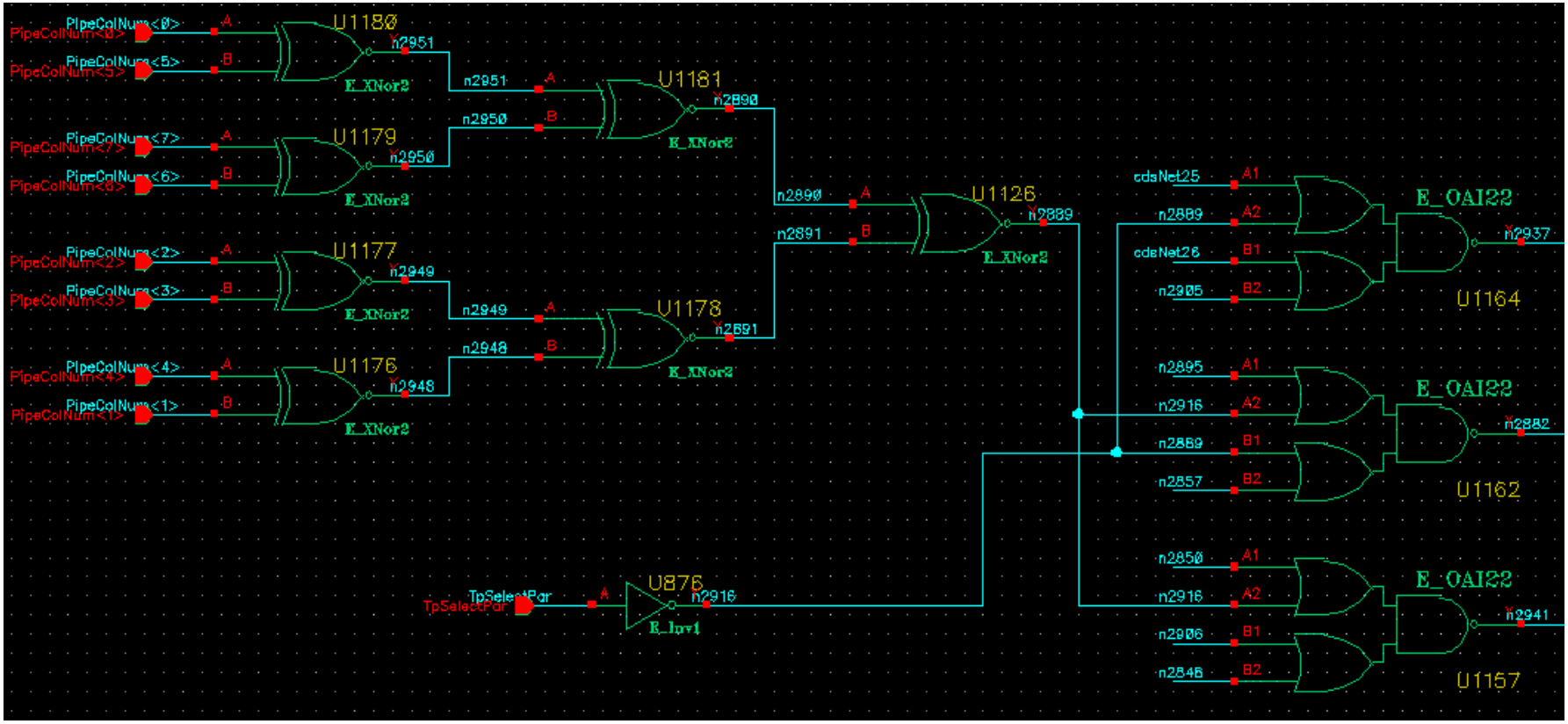
- **Parity bit (I1) is wrong encoded in 4 port mode and Rclk divider = 0 (LHCb mode)**
- **all other modes or Rclk divider settings**
  ➔ Parity bit is OK
- **problem is understood in verilog**
  - **not so easy to fix**
  - **simple workaround: swap position I1 with I5 could be tested on a 1.3 with a FIB patch**

Parity bit - workaround (1)



schematic of parity-bit generation (part of MuxScheduler)

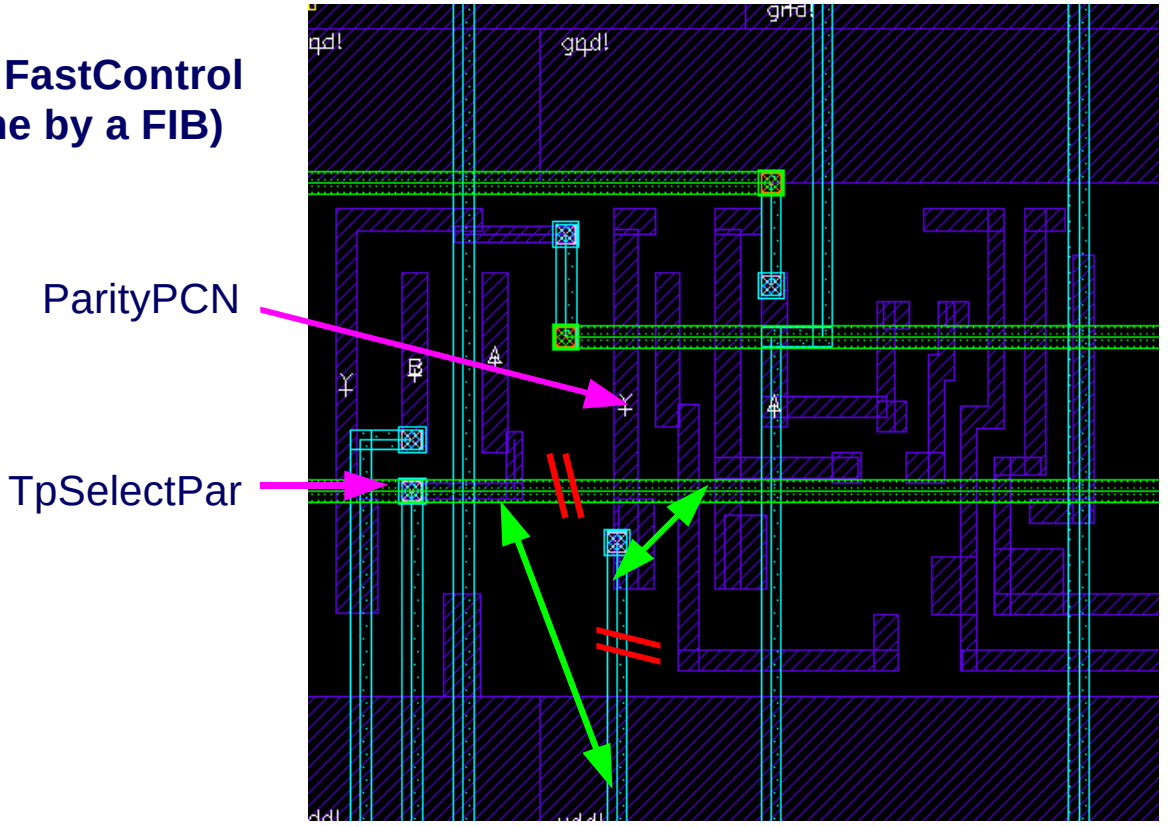
Parity bit - workaround (2)



new schematic of parity-bit patch

Parity bit - workaround (3)

- **Layout modification in FastControl of Beetle (could be done by a FIB)**
  - **2 cuts**
  - **2 connections**



Output device of ParityPCN generation - E_XNor2 (U1126)

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