Design of Beetle1.3

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Motivation for Beetle1.3

in descending order of priority:

- Sticky Charge Effect
- Comparator Offset Variation
- 80 MHz Cross Talk
- Output Driver Performance
- Sagging Readout Baseline

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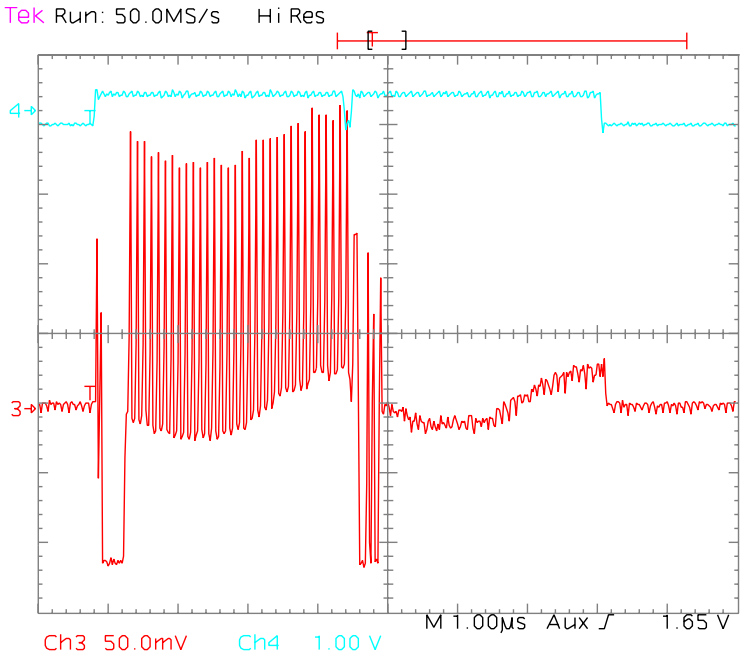
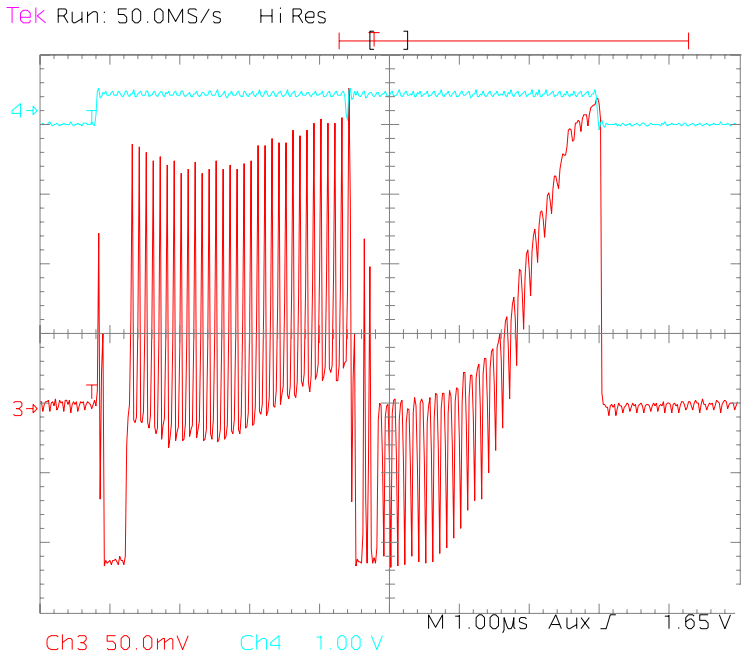
Sticky Charge Effect (1)

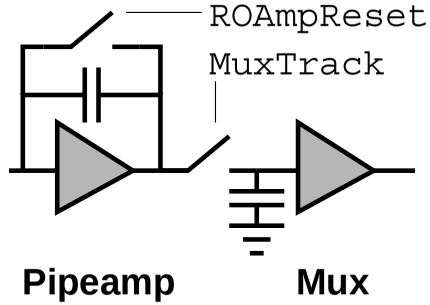
- signal carry–over from previous event into an empty event, strong baseline drift
- only present for consecutive readouts, i.e. during a readout operation a further trigger arives

non–consecutive readout



consecutive readout





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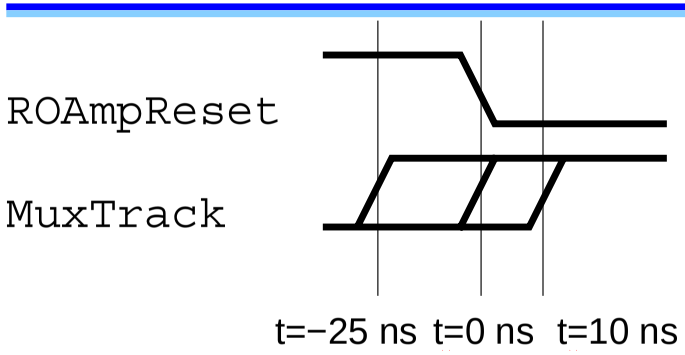
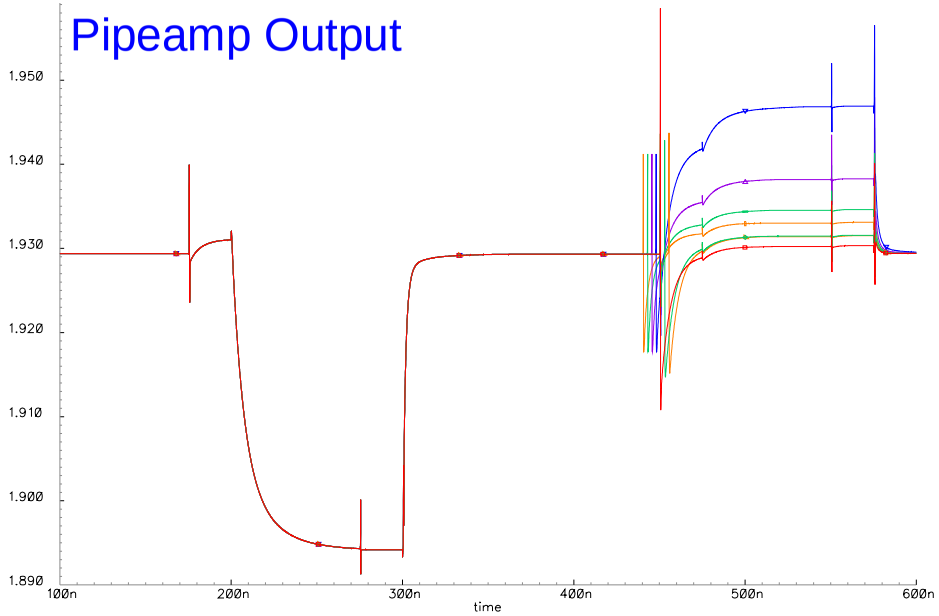
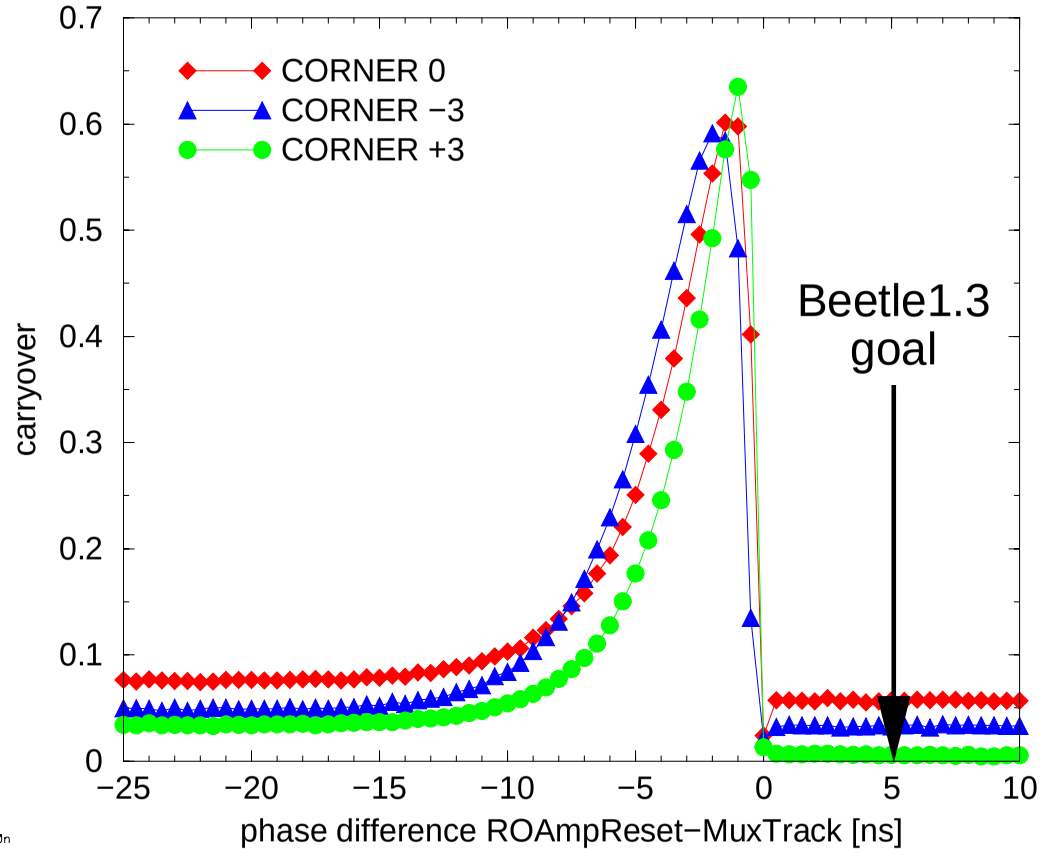
Sticky Charge Effect (3): Simulations







Modification in Beetle1.3: analog delay of MuxTrack by 5 ns

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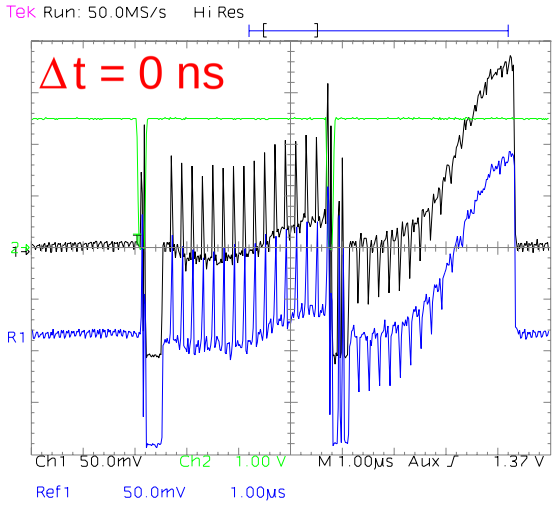
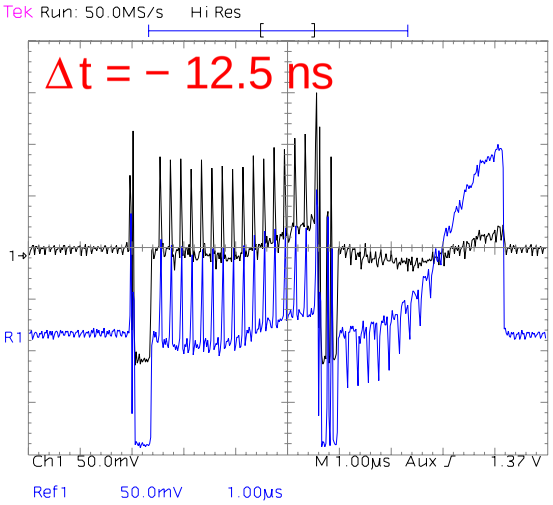
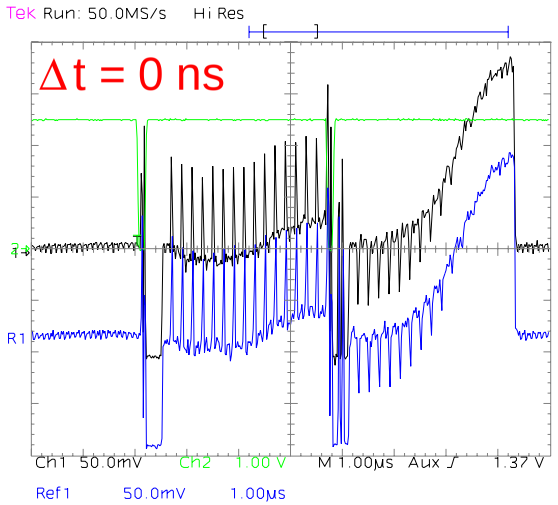
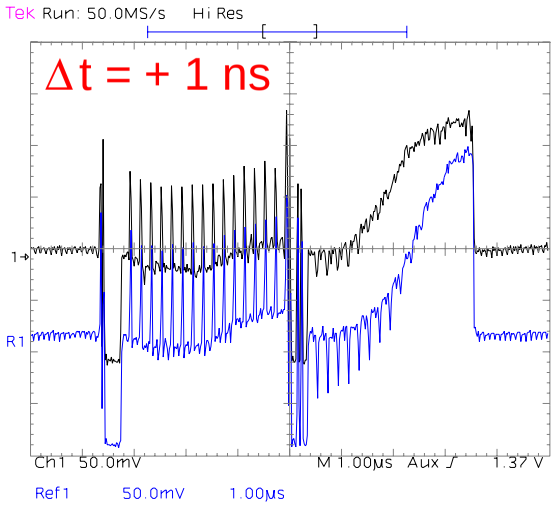
Sticky Charge Effect (4)

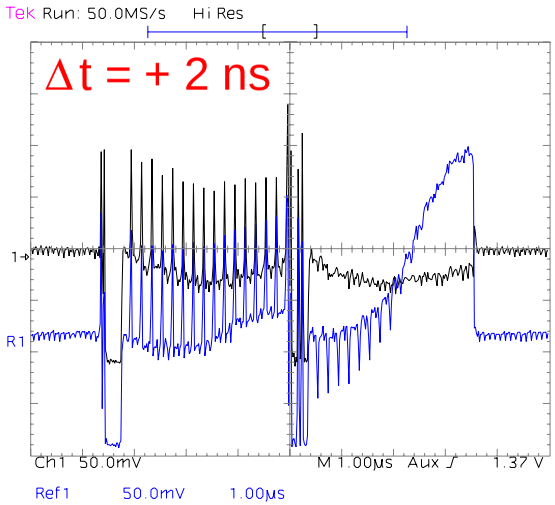
probe needle test with pos. and neg. phase shift











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Comparator Changes

Motivation: offset−spread: σ = 2.4 DAC units = 300 nA = 0.2 MIP

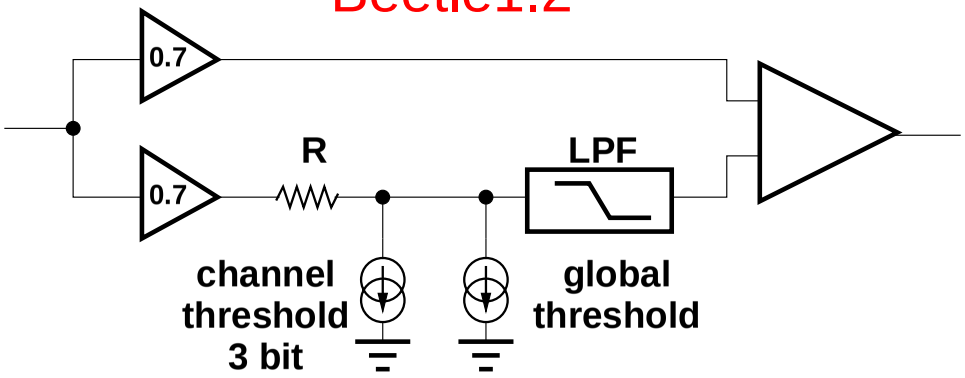
- bipolar
- too large for compensation with present DACs for channel threshold

Measures:

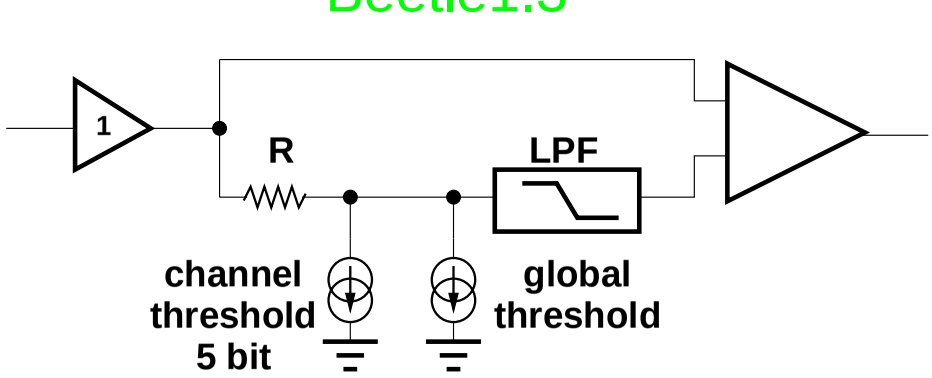
- merging input buffers: reduces additional offset
- gain increase of buffer: reduces influence on offset
- increase resolution of threshold current to 5 bits

  required: ±900 nA = ±0.6 MIP

Beetle1.2



Beetle1.3



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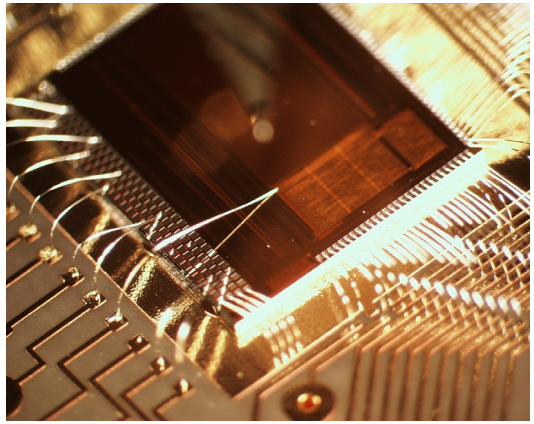
80 MHz X–talk

cross talk with a frequency spectrum of 80 MHz

present on

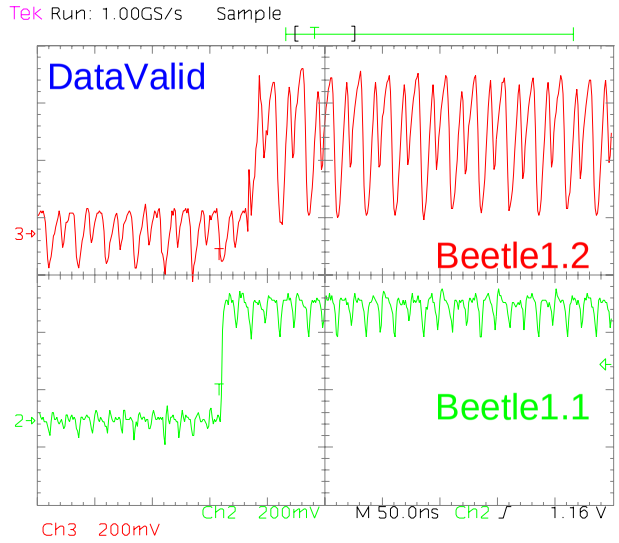
- digital signals, e.g. DataValid
- analogue signals, e.g. AnalogOut
- power supply lines: Vddd, Vdda

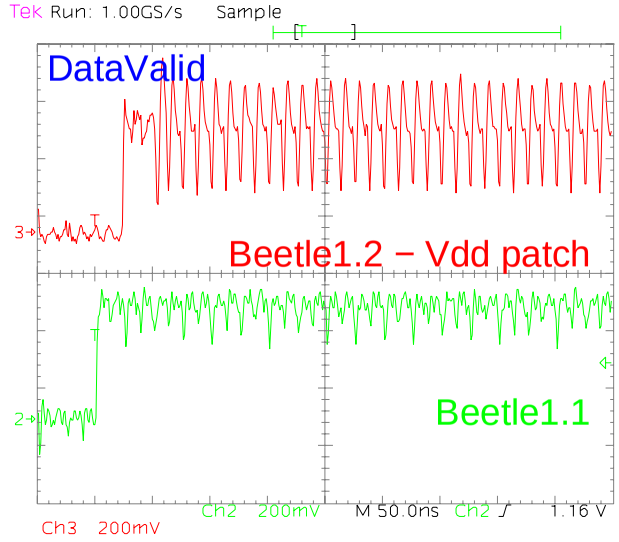
comparison:	Beetle1.1	Beetle1.2
# flip–flops:	1349	3043
# clock buffers:	21	284
guard rings logic core:	analogue	digital



Possible solutions:

- reduced no. of clock buffers
- on–chip power blocking





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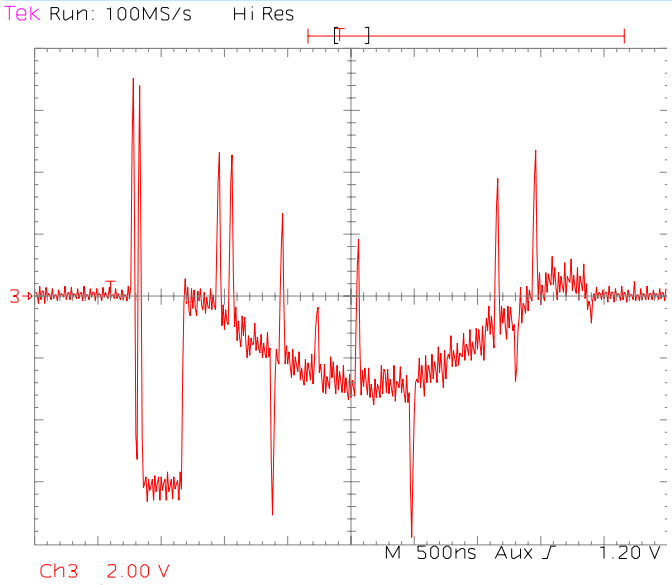
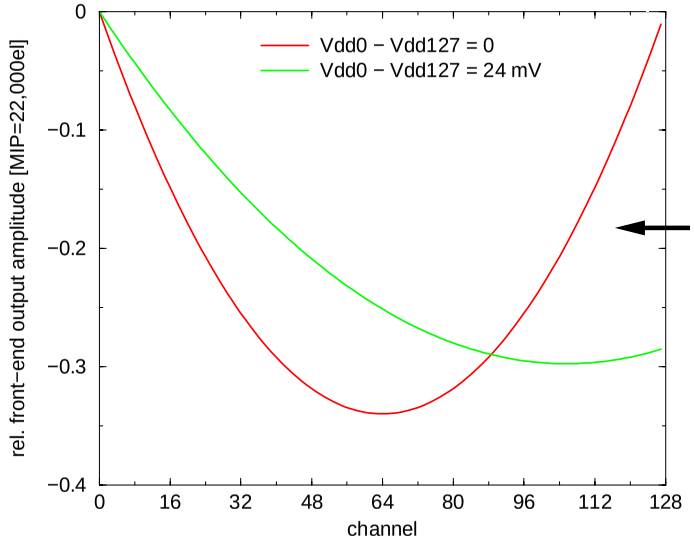
Readout Baseline Variation





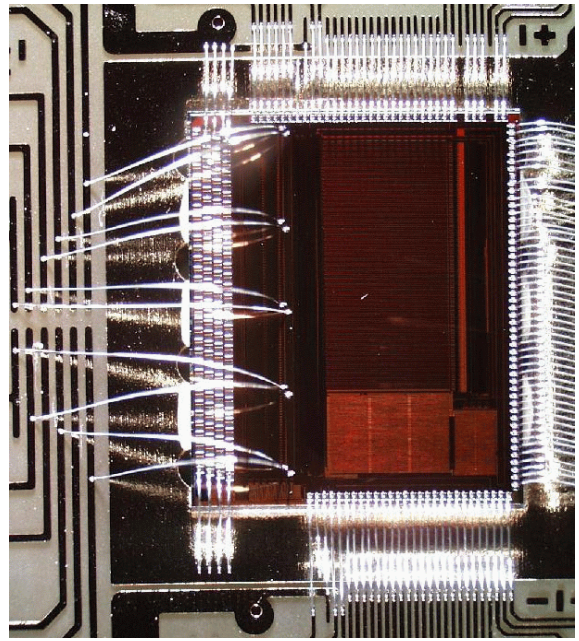
Observation:
shaper bias current affects
amplitude of baseline variation

Laser Patch:
probing shaper power supply
at various channels

difference in VDD between
ch.0 and ch.127: 24 mV

Simulation:
resistive VDD−network in shaper

Beetle Surgery



Modification in Beetle1.3: additional power supply lines in shaper (+ 100 um)

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Modifications in Beetle1.3

Design Changes (on schematic level)

- analogue delay of MuxTrack signal — fix of sticky charge effect
- improved comparator — 5 bit channel threshold resolution
- Current Output Buffer — increased gain, diff. output current
- Mux: Switch Control — reduction of switching spikes
- Control Logic — bug fixes (daisy chain op., low−Rclk op.)
- new I2C−Pads — 5V compatible
- modified test pulse pattern — "+1/−1" pattern

Layout and Power Routing Issues

- modified front−end power pads
  (power and ground at top and bottom of chip)
- improved shaper power routing
- improved front−end biasing scheme
- separation of comparator core and LVDS pad power
- improved pipeamp power routing
- separation of power supply of multiplexer and logic core
- introduction of bias generator probe pad
- implementation of 2 new power pads for logic core
  (located at bottom side)
- merged pad openings of adjacent power pads
- on−chip power blocking — in total 1375 gate caps: ~ 0.9 nF
- improved guard ring structures — n−well and substrate contacts

X−talk Measures

- reduced no. of FF in multiplexer — by factor 3 (414 −> 138)
- reduced no. of clock buffers in logic core — 275 −> 104
- on−chip power blocking

This all together increased chip size by 300 um in x−direction
(now: 5400 x 6100 um2)

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Testpulse / Front−end

Testpulse

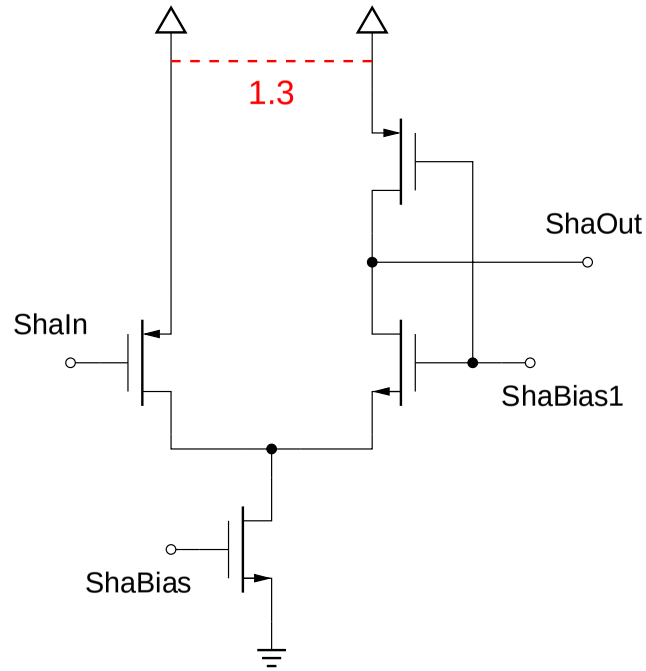
- **reduced testpulse pattern (+1 / −1)**
- **improved guardring structure**

Front−end

- **revised power routing (esp. Shaper)**
- **decoupling capacitors in Buffer (1.3pF/ch)**

	resistances	Beetle 1.2 [mOhm/ch.]	Beetle 1.3 [mOhm/ch.]
power:	Rpreamp	13.83	12.37
	Rshaper1	39.21	11.17
	Rshaper2	70.24	
	Rbuffer	137.70	39.69
bias:	Rprebias	478.64	151.78
	Rprebias1	690.40	278.26
	Rshabias	1569.02	492.94
	Rshabias1	650.30	201.31
	Rbufbias	1569.02	985.88

Front−end Shaper



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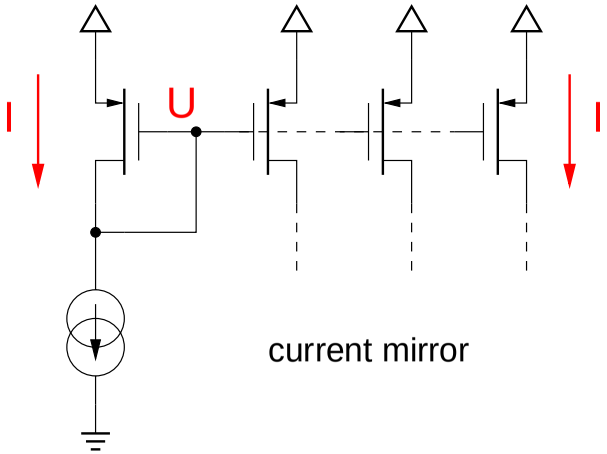
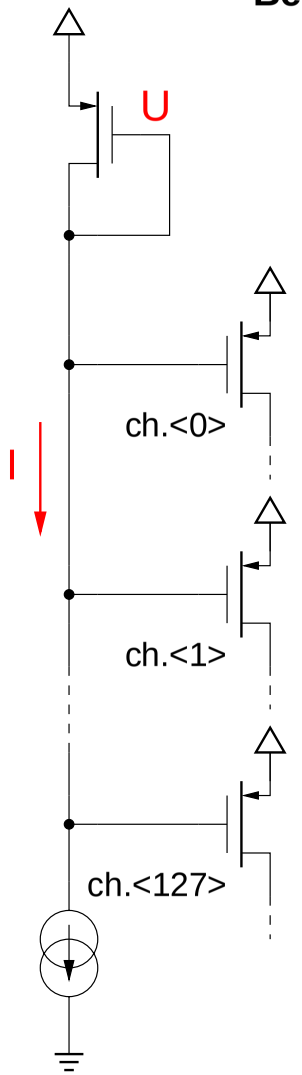
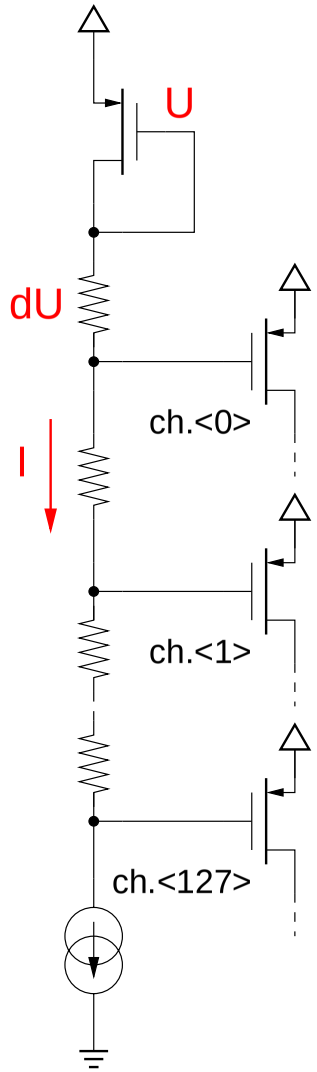
Front−end: biasing

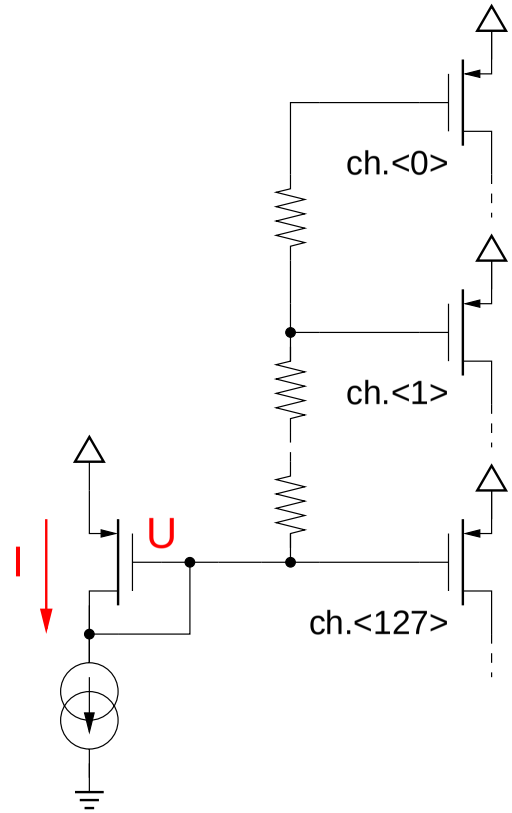


Beetle 1.2





Beetle 1.3



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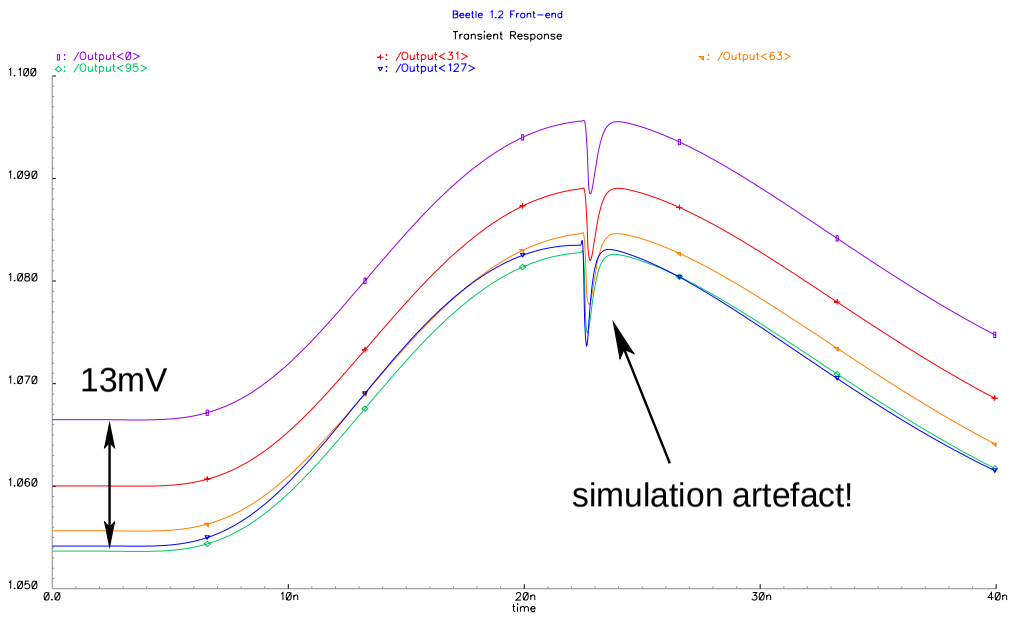
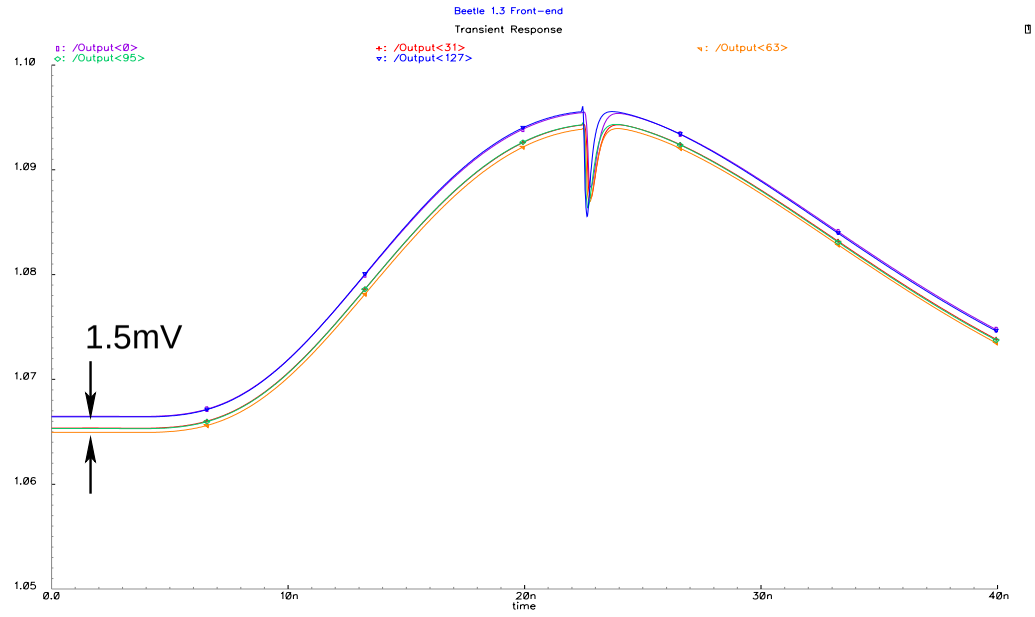
Front−end

Front−end simulation

- **Testpulse, Front−end and Pipeline**
- **128 channels**
- **with channel to channel resitors**



Beetle 1.2



Beetle 1.3

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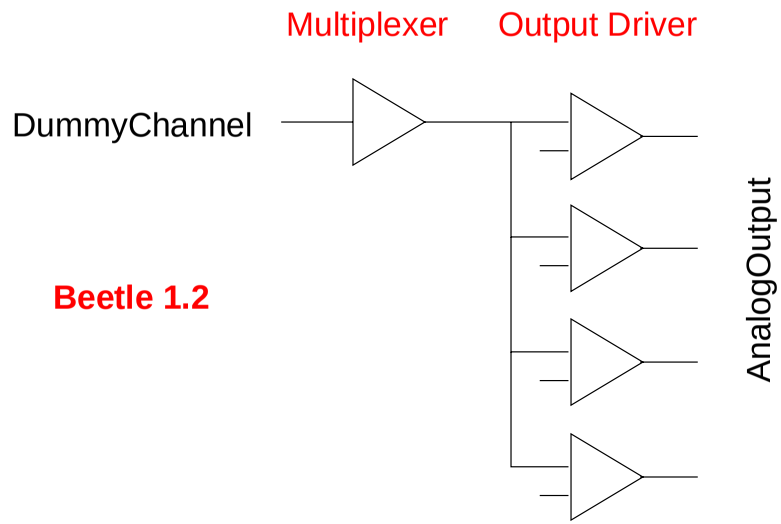
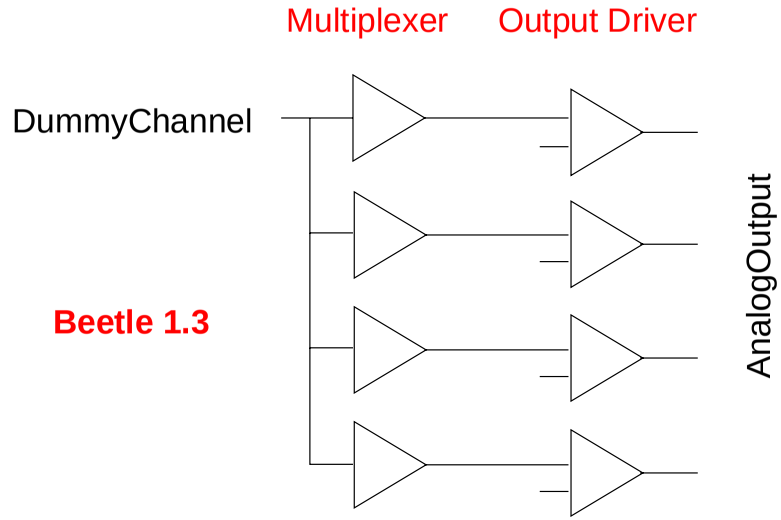
Multiplexer

- reduced number of flip−flops (1/3)
- removed bug during a non−readout in binary mode
- fixed header−crosstalk in 32 on 4 ports mode
- fixed switching spikes in header
- two adjustable header sizes (−2 / +2) and (0 / 5)
- new guardring concept to prevent digital crosstalk
- improved power routing (less ohmic)
- analog power separation MUX / Output driver
- digital power separation MUX / digital core
- decoupling capacitors for digital power net





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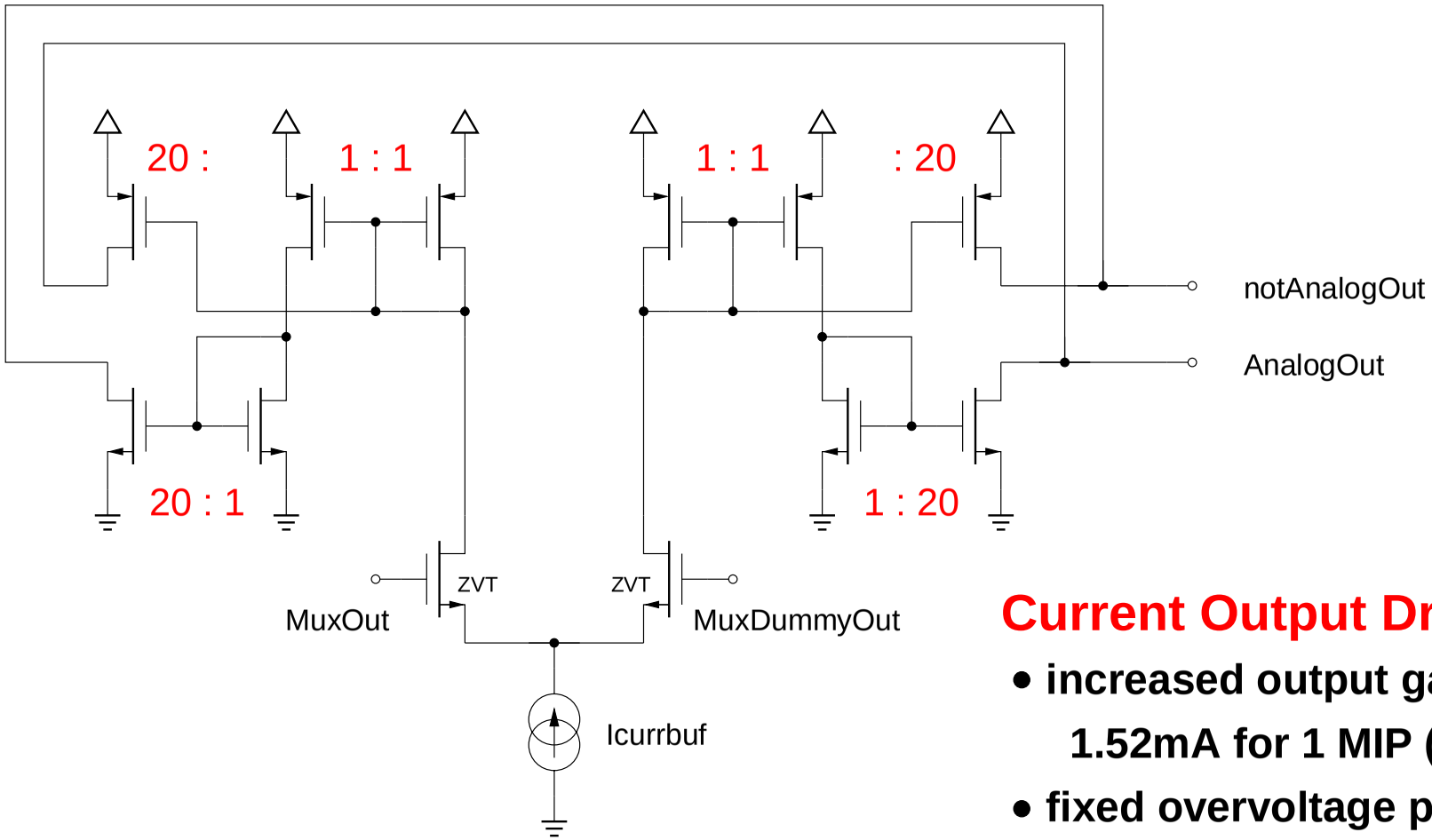
Output Driver



Current Output Driver

- **increased output gain by factor 3.2**
  1.52mA for 1 MIP (22.000e)
- **fixed overvoltage problem**
- **own power supply (pad VddTx)**
- **improved guardrings**

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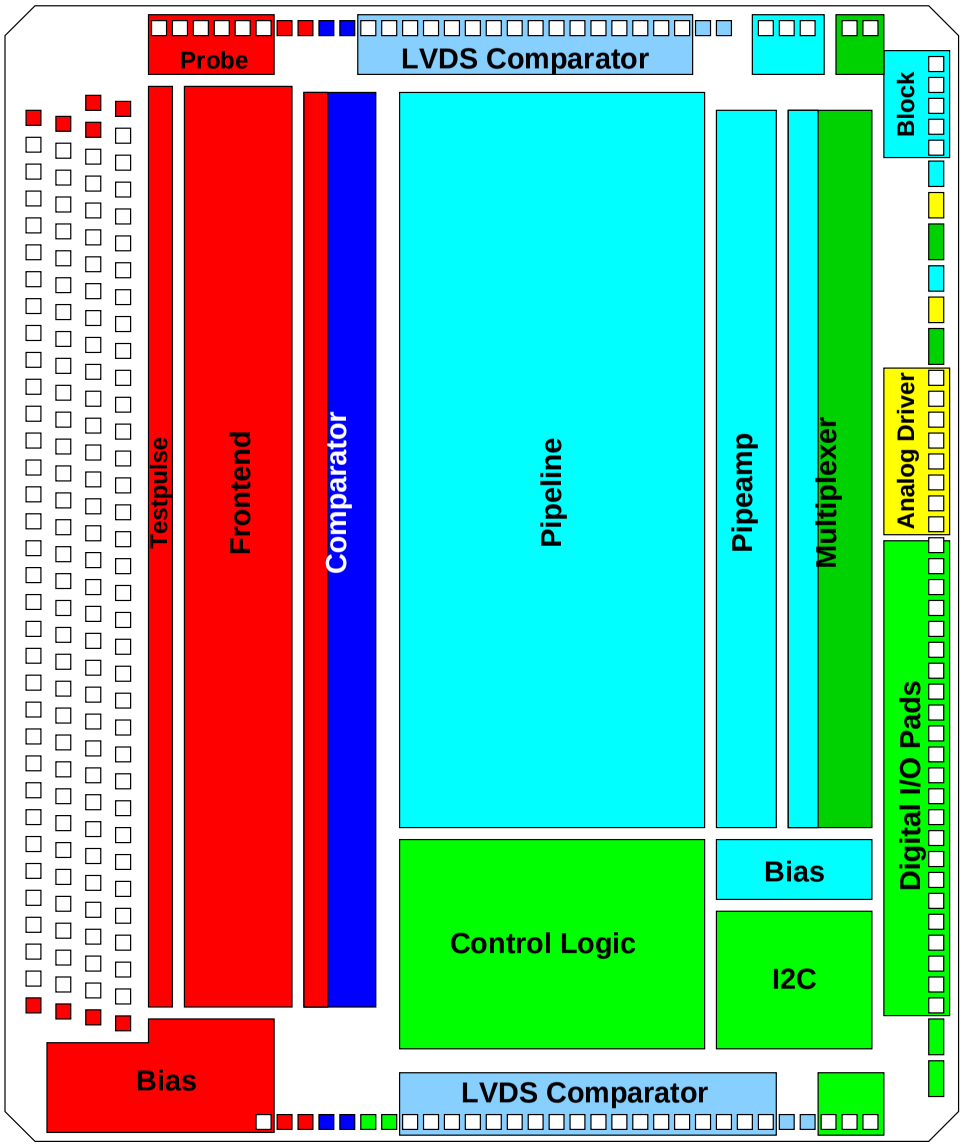
Power Supply / Pads



- chip length increased from 5100µm to 5400µm
- new arrangement of analog power pads
- additional power pads for digital core
- separation of power comparator core / LVDS output driver
- RoTokenIn and RoReTokenIn with int. pulldown
- merged adjacent digital power pads
- I2C pads SCL / SDA now 5V tolerant
- power separation of digital core and multiplexer
- power separation of analog part (MUX/pipeamp) and current output driver
- improved ESD protection
- on chip decoupling capacitors

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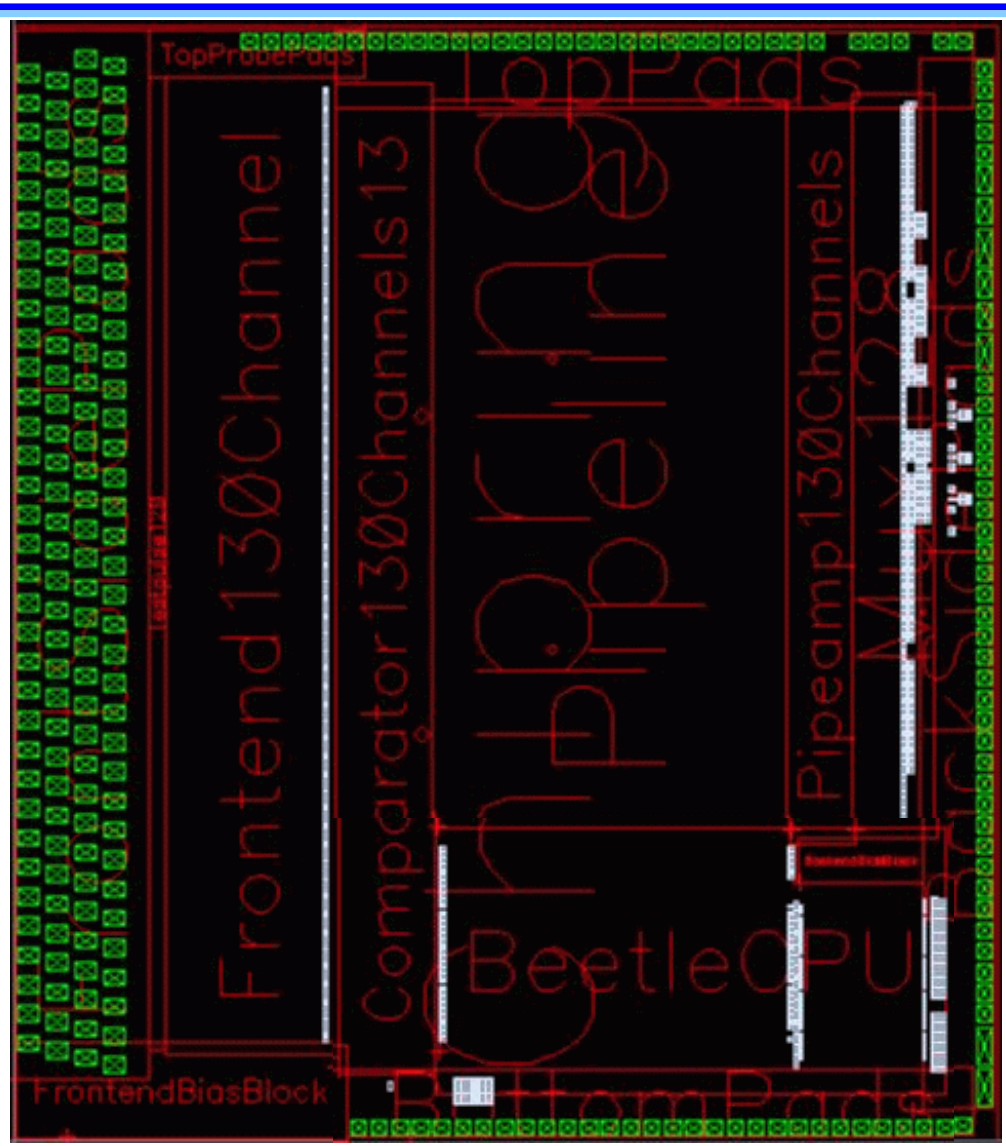
On−Chip Blocking Capacitors



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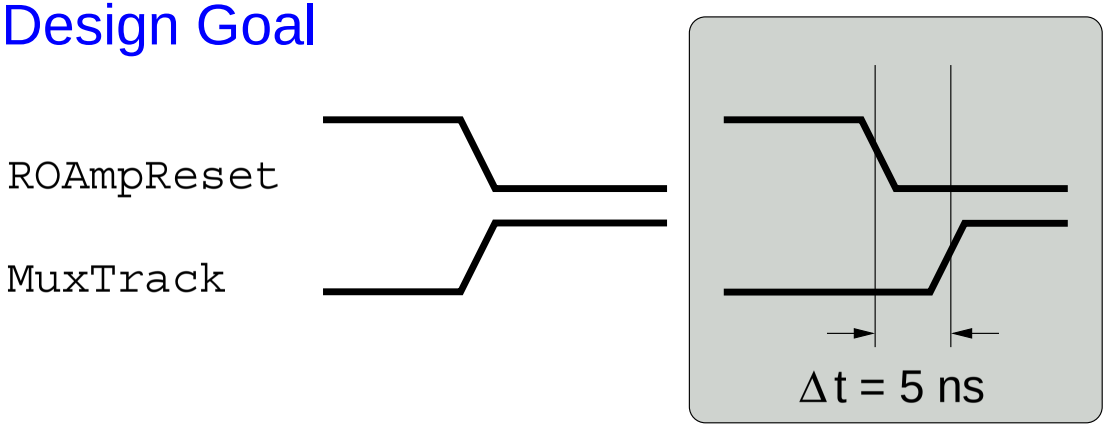
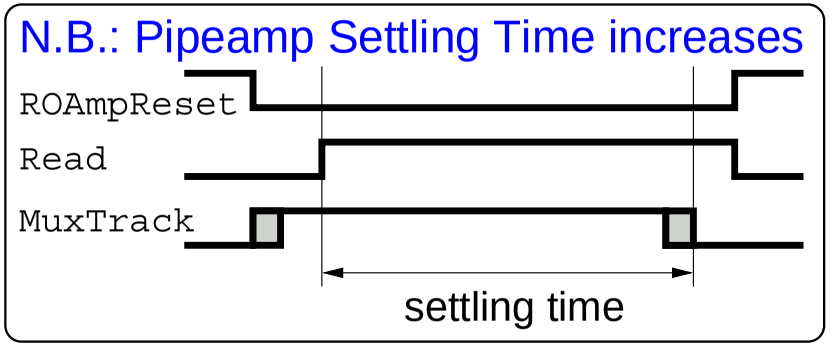
Fix of Sticky Charge Effect

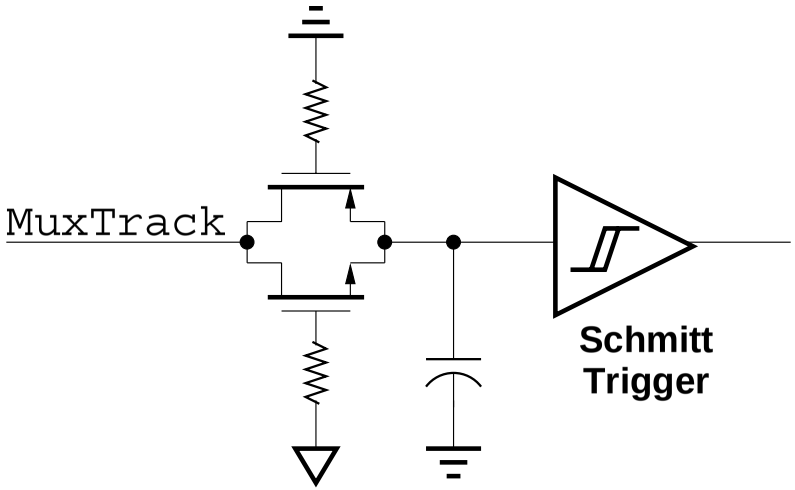
Design Goal



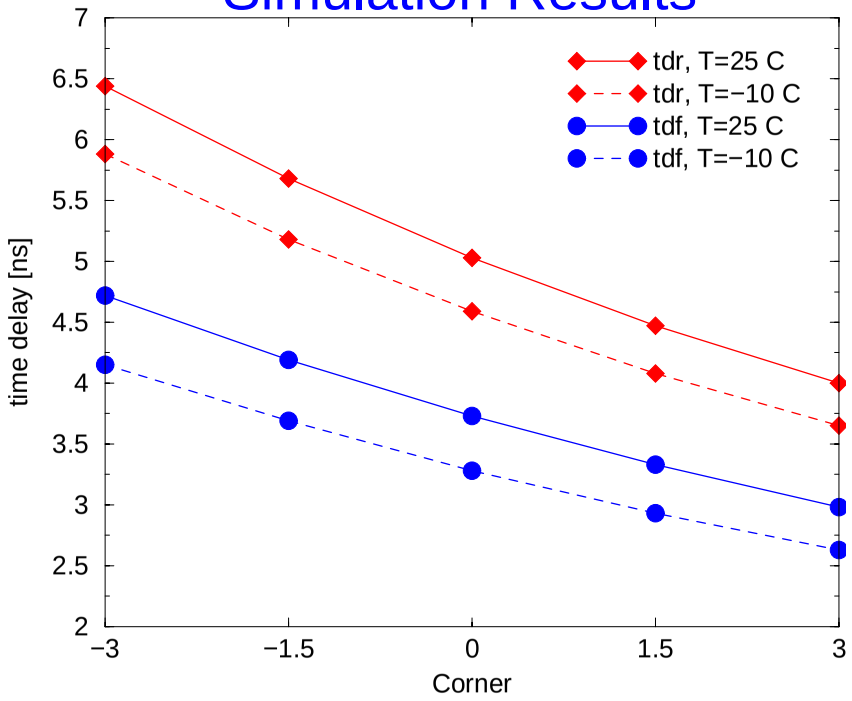
N.B.: Pipeamp Settling Time increases



Analogue Delay



Simulation Results



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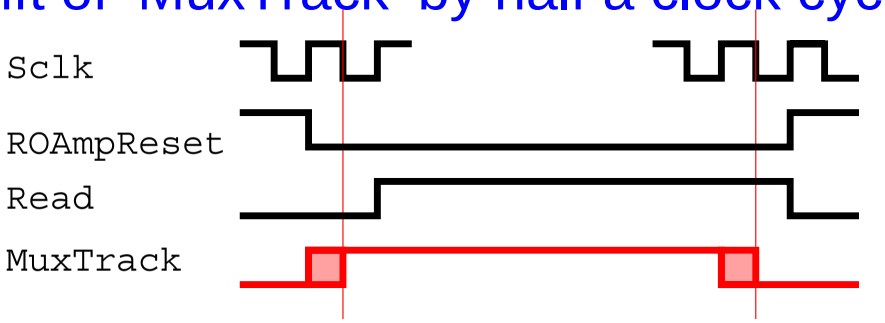
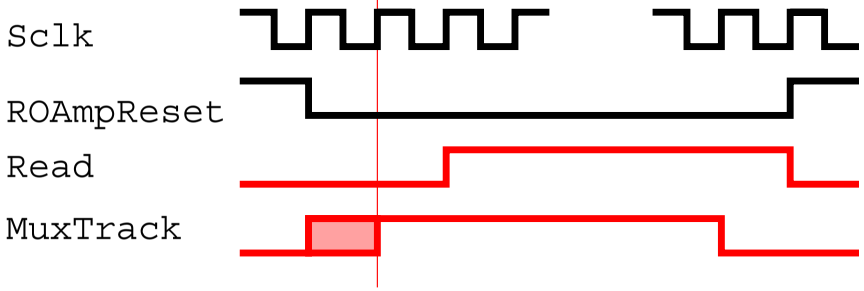
Alternative Fixes

Shift of 'MuxTrack' by half a clock cycle



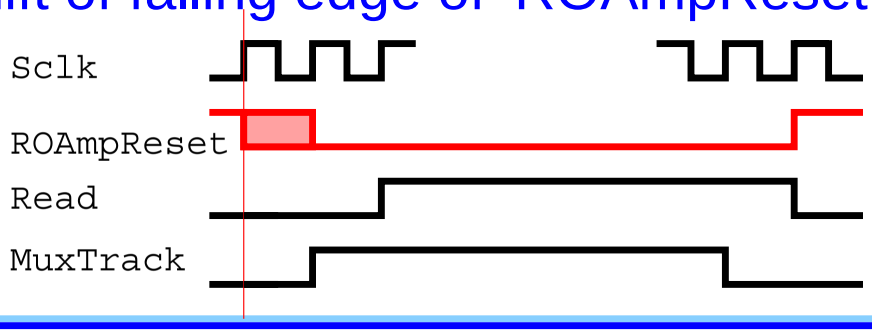
relies on clock duty cycle!

Shift of rising edge of 'MuxTrack' and 'Read' by one clock cycle (+ 25 ns)



reduces pipeamp settling time
from 75 ns to 50 ns

Shift of falling edge of 'ROAmpReset' by one clock cycle (− 25 ns)



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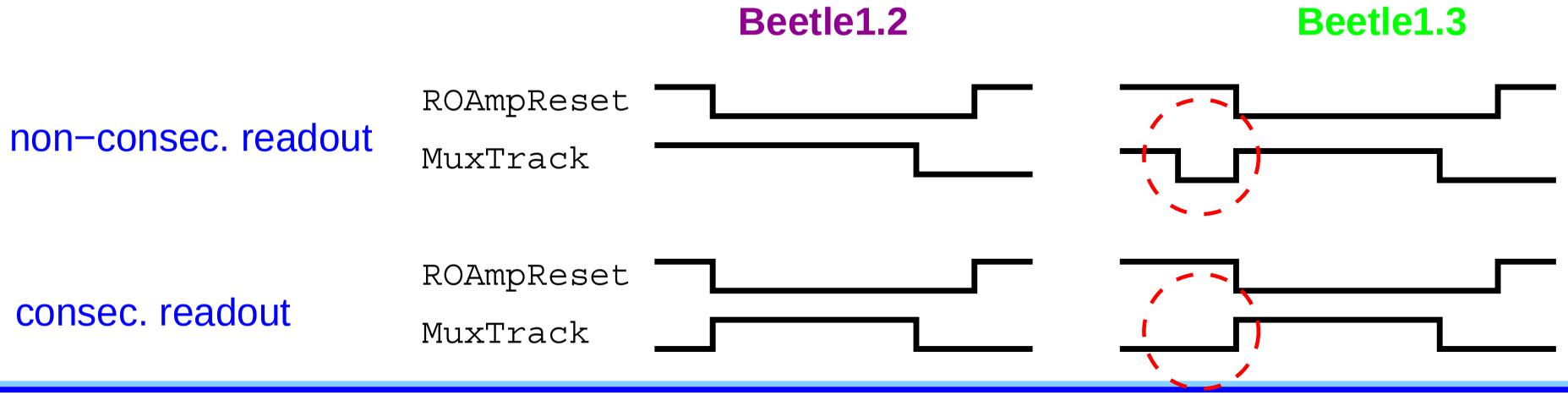
Control Logic: Functional Changes

- bug fix: daisy chain token handling
  last chip in daisy chain (DaisyLast) is no longer sensitive to return token signal (RoReTokenIn)
- bug fix: operation with Rclk < 0.5 Sclk

  Beetle1.2: multiple generation of 'ReleaseColumn' signal (depending on Rclk/Sclk ratio) results in FIFO overflow

  Beetle1.3: generation of 'ReleaseColumn' signal is independent of Rclk frequency
- equalising control sequence cons. / non−consec. readout



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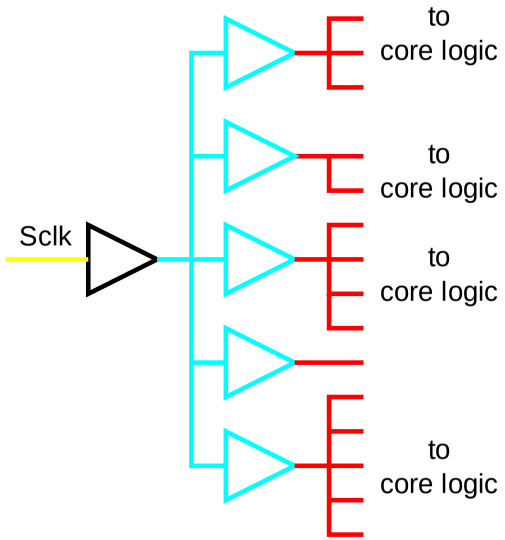
Control Logic: Clock Routing

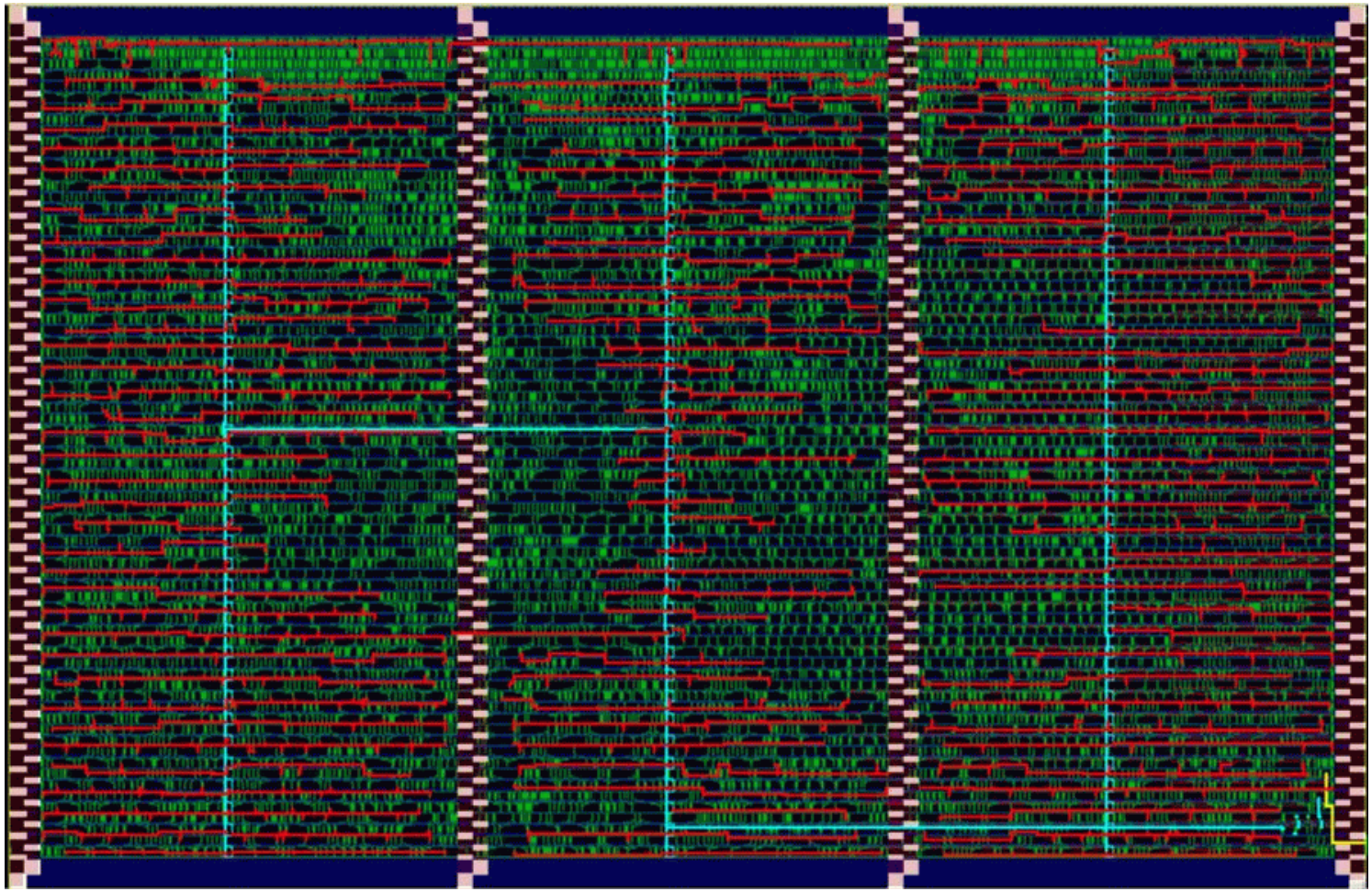
Topology: clock trunk



 # = 104

(on Beetle1.2: # = 275)

layout view of FastControl



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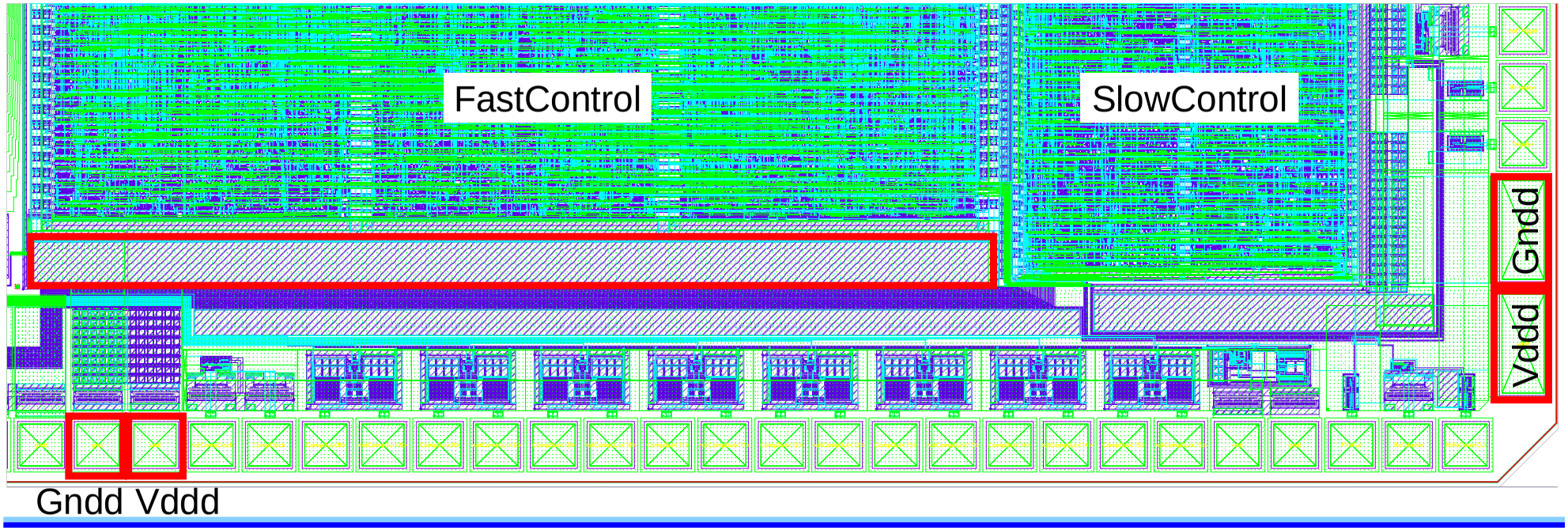
Control Logic: Power Routing

- merged pad openings of existing power pads: enables 1−2 additional bond wires per pad
- additional power pads at bottom side
- blocking capacitors: 414 (core) + 96 (pads): 1/3 nF
- reduced area of FastControl (− 80 um in y−direction): allows improved power routing



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Control Logic: Simulation Performance under Process Variations

- on MPW7 run (Beetle1.2): controlled process variations in stripes across wafer
  variation of transistor length by max. 30 nm: ($\Delta L = 0, -15, -30, +15, +30$ nm)

  experimental observation: Beetle1.2 chips with $\Delta L = -30$ nm (fast chips):
  FIFO overflow after 16 triggers

- Corner Simulations on Beetle1.3: taking into account
  - gate propagation delays (from standard cell library)
  - interconnection delays (extracted from layout)

process corner	functionality
worst case (slow)	OK
typical case	OK
best case (fast)	failed (setup time violations)

↑ reduces yield

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