



- Specifications -

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Beetle Specification: L1 Interface

Rather well defined: (http://lhcb-elec.web.cern.ch/lhcb-elec/html/key_parameters.htm)

- Bunch crossing rate: 40.08 MHz
- Maximum L0 rate: 1.1 MHz.
- L0 latency: 4.0 us = 160 clock periods.
- L0 gap: None
- Consecutive L0 triggers: Max 16
- L0 trigger types: Only one (Normal trigger)
- Samples to extract per L0 accept: One per channel (multiple samples if required)
- L0 derandomizer depth: 16 events
- L0 derandomizer readout time: $(32 + 2 + 2) * 25 \text{ ns} = 900 \text{ ns}$
- L0 restrictions: Emulation of front-end buffers.
 - Predictable release of derandomizer buffers
- Bunch crossing clock and L0 distribution: TTC system
- Synchronization checks: All event data must carry synchronization checking data
 - Pipeline Colum Number (PCN)
- Location and qualification of L0 front-end electronics
 - 0.25µm CMOS & special design rules ensure radiation hardness >10Mrad
- L1 buffer input speed: 900ns minimum spacing between events.
- Reset:
 - Global initialization (i.e. not a reset)
 - L0 front-end reset





Beetle Specification: Detector Interface

	Pile-up Veto	VELO	Inner Tracker	RICH (MAPMTs)
Readout pitch	flexible, 40-60mm	flexible, 40-60 μ m		n/a
Signal polarity	positive and negative	positive and negative		n/a
Pulse height distribution	Landau	Landau	Landau	n/a
Mean signal	11.000 electrons/MiP	11.000 electrons/MiP		n/a
Detector capacitance	10 pF	10 pF	\approx 30pF	n/a
Required S/N (min. comp. threshold)		>14, independent of irradiation		n/a
Coupling to detector	AC	AC		n/a
Single channel leakage current	0 (AC coupling)	0 (AC coupling)		n/a
Radiation dose	> 2MRad/year	> 2MRad/year		n/a
Chip should stand large signals	up to 400Mips	up to 400Mips		n/a
Distance to next DAQ stage	10m	10m	10m	n/a
Required linearity		\leq 5% (\leq 10MIPs)		n/a
signal time jitter		<5ns	<5ns	n/a
Maximum power consumption		<4mW/channel (flexible)		n/a
Signal peaking time	\leq 25nsec	\leq 25nsec	\leq 25nsec	\leq 25nsec
fall time, pulse spill over	\ll 30% after 25ns	\ll 30% after 25ns	\ll 30% after 25ns	n/a
Synchronization & error detection	LHCb 98-052	TRAC - Vertex Detector	Timing & Sync.	n/a
Analog pipeline length	n/a	160 (4 μ s)	160 (4 μ s)	160 (4 μ s)
Readout time	25ns	<900nsec	<900nsec	<900nsec
de-randomizing buffer	n/a	16 triggers	16 triggers	16 triggers
Other issues		not pin compatible, but same control signals as DMILL chip		uses Si-detector front-end w. add. charge divider





Beetle Specs: Other issues

Draft of Beetle Specification available!

Contains all LHCb specs mentioned plus:

- I²C ID programming upon reset
- "Orthogonal" readout modes
- Daisy-chained readout
- Only on type of reset

But:

Spec input needed for

- I²C ID programming
- JTAG boundary scan
- Reset specification
- SEU requirements
- Error encoding in data header
- Error signal definition
- other.....

