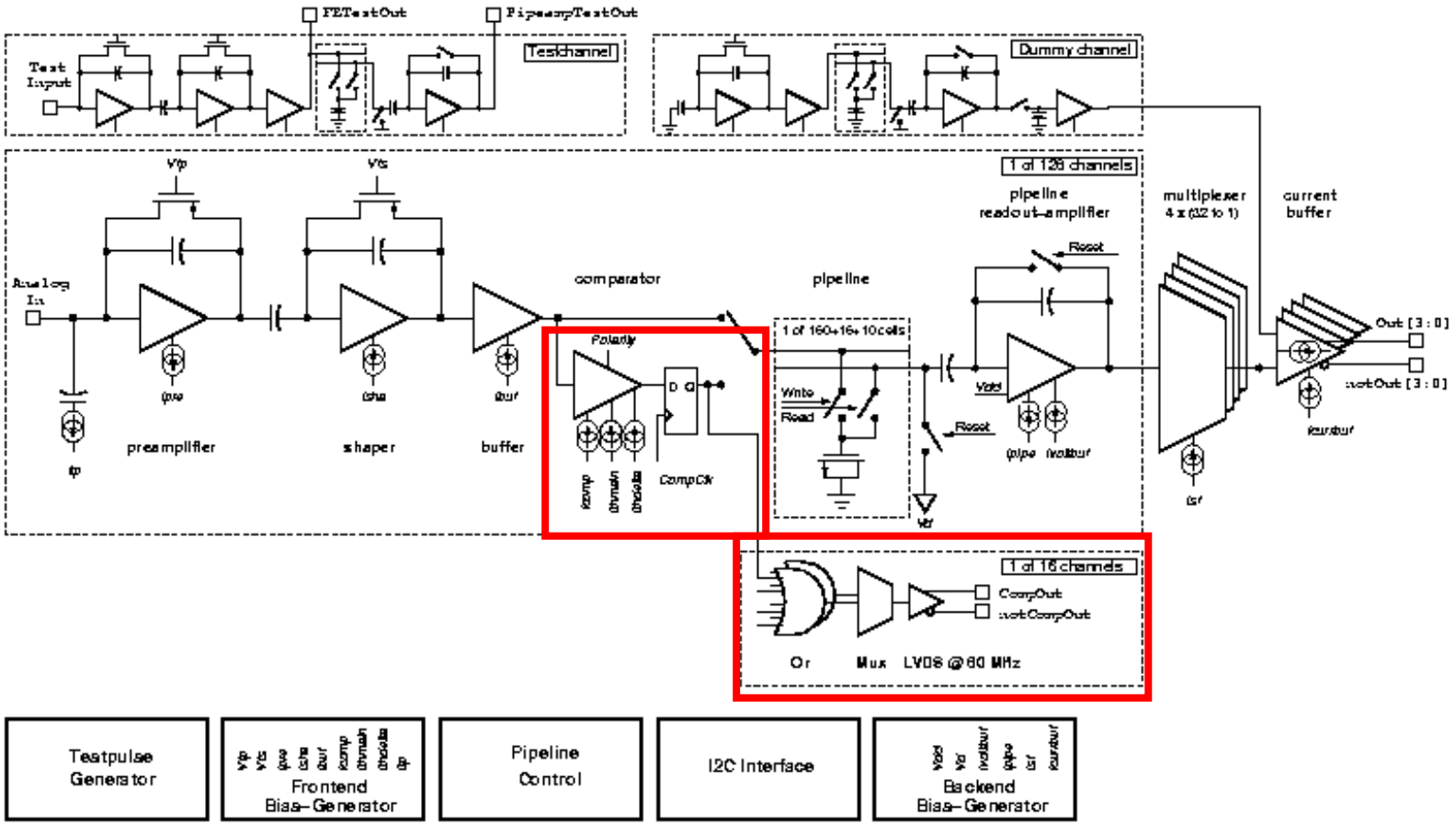
Comparator of Beetle chip 1.1

Outline:

- Introduction
- Comparator details

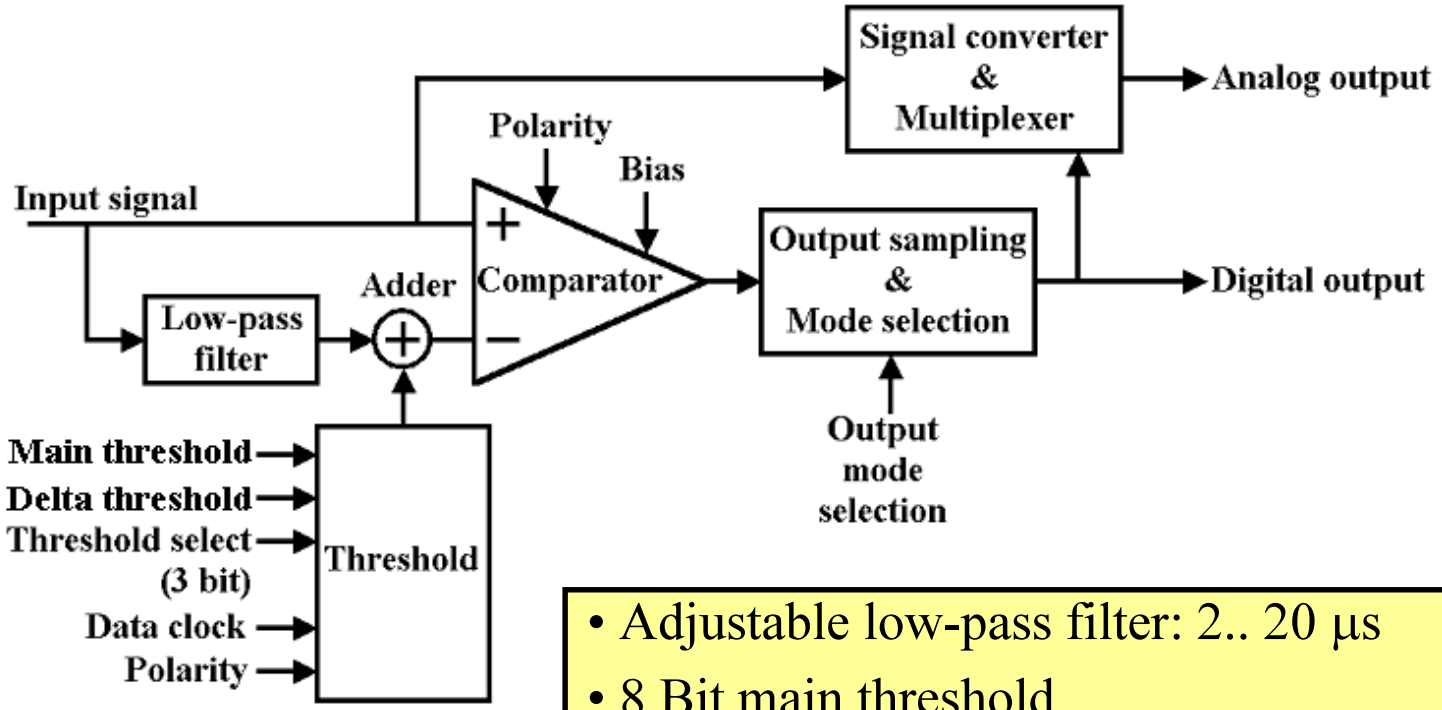
- Offset measurements & simulations
- Proposed modifications
- Conclusions

Beetle block diagram



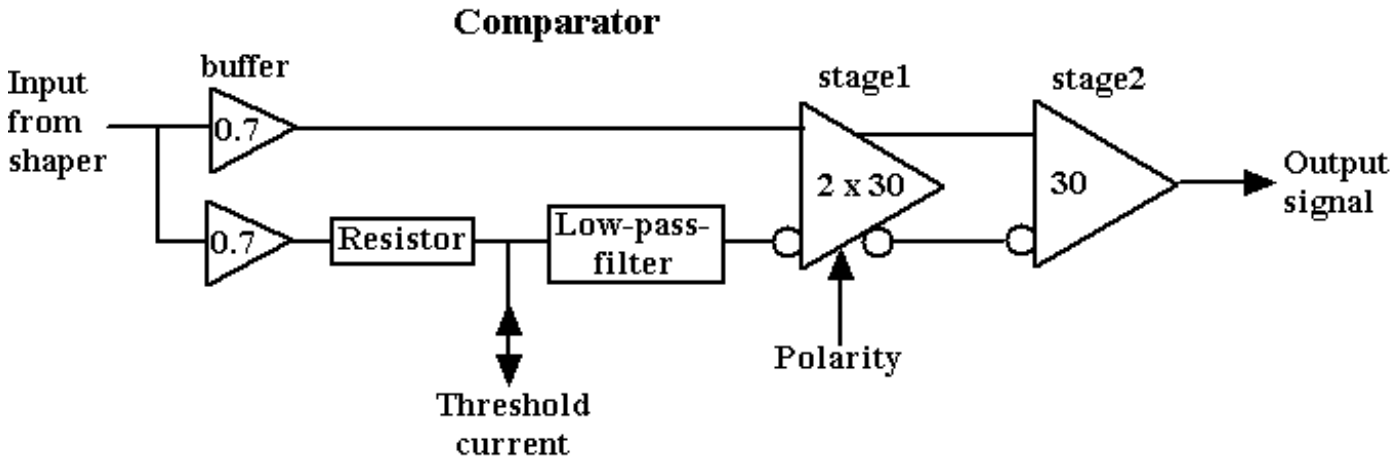
- Logic-or of 4 adjacent channels
- 2 Groups multiplexed on output
- 16 LVDS outputs @ 80 Mbit/s

Comparator block diagram



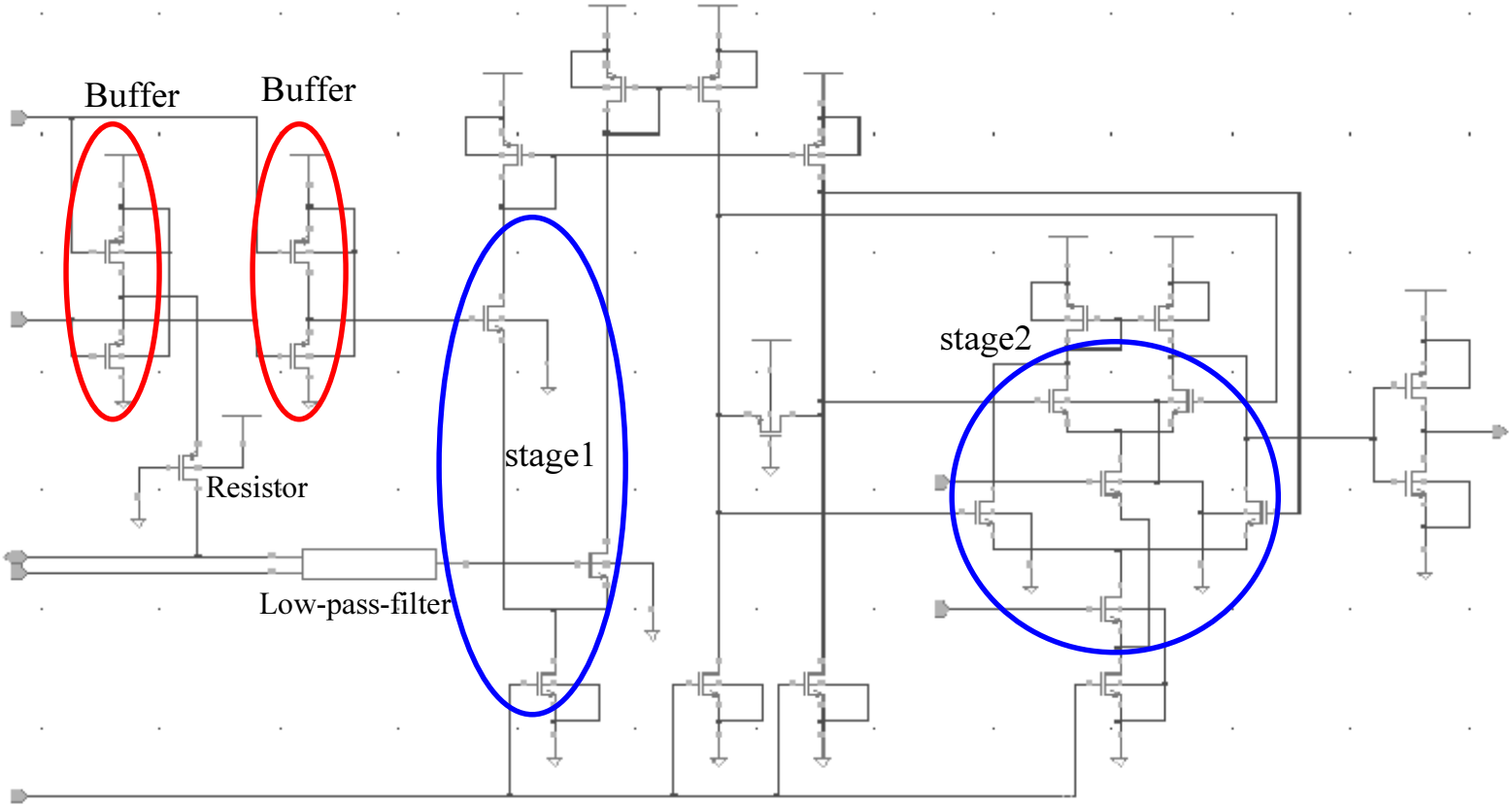
- Adjustable low-pass filter: 2.. 20 µs
- 8 Bit main threshold
- 8 Bit delta threshold
- 3 Bit individual threshold
- Dual polarity
- 2 output modes: tracking or pulse mode
- Adapt digital signal to analogue pipeline level

Comparator circuit

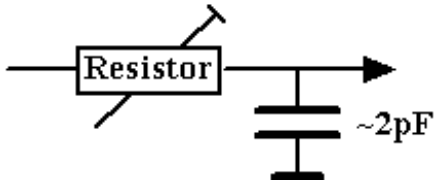


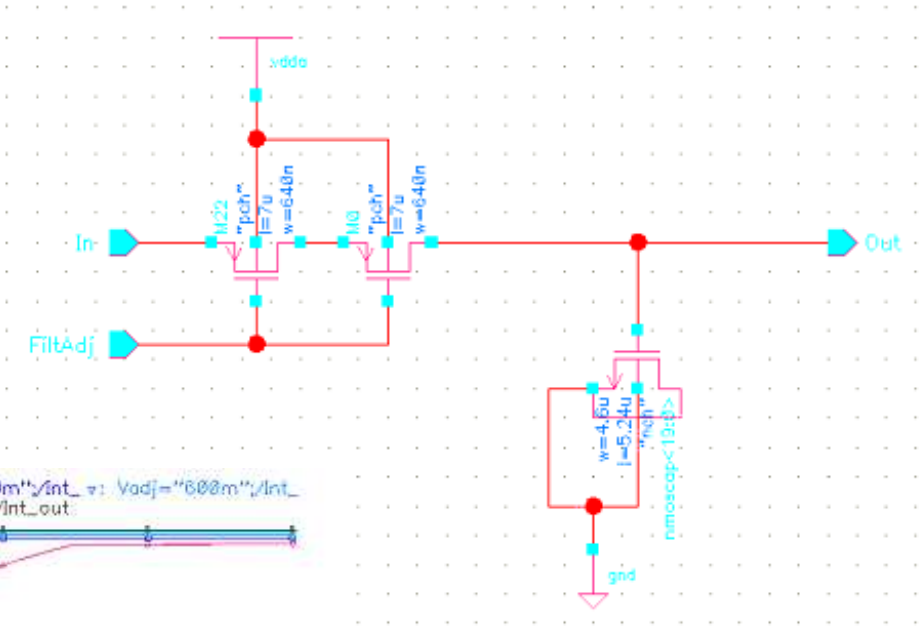
- 2 Buffers followed by 2 gain stages
- Total gain 2160 x
- Output polarity switch

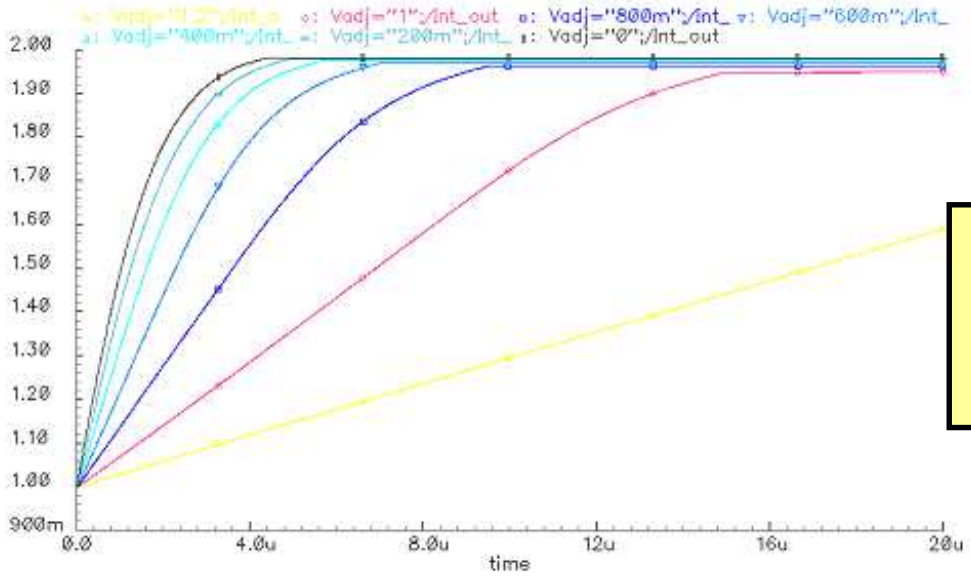
Schematic details



Adjustable Filter

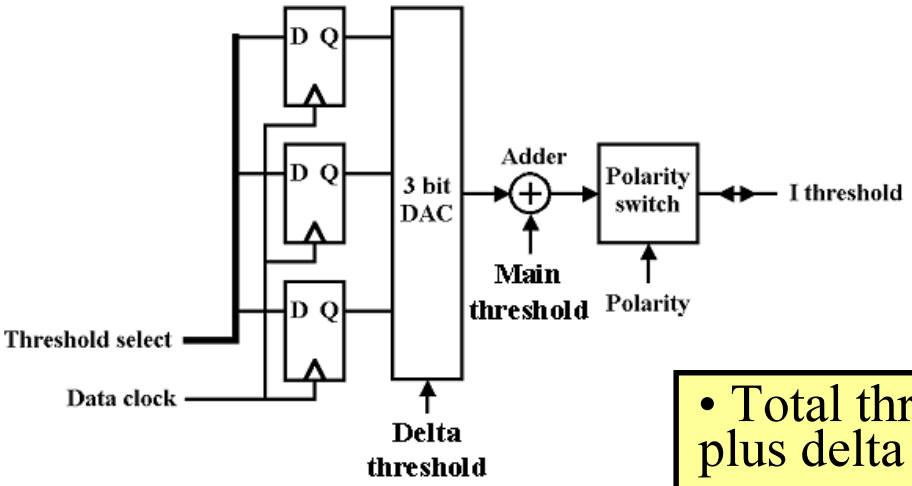




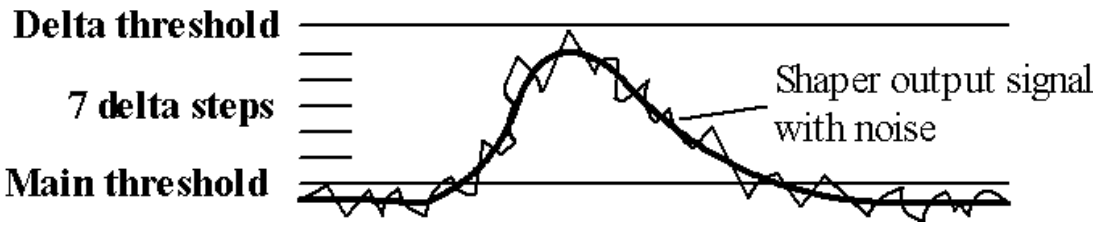


- First order low-pass-filter
- Range 2 µs…20 µs
  8 bit; non-linear

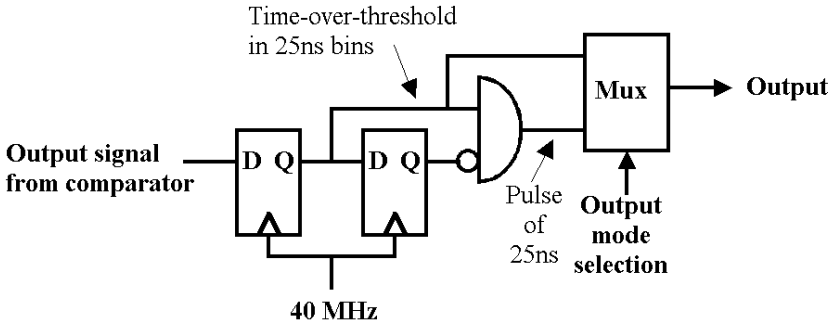
Threshold circuit

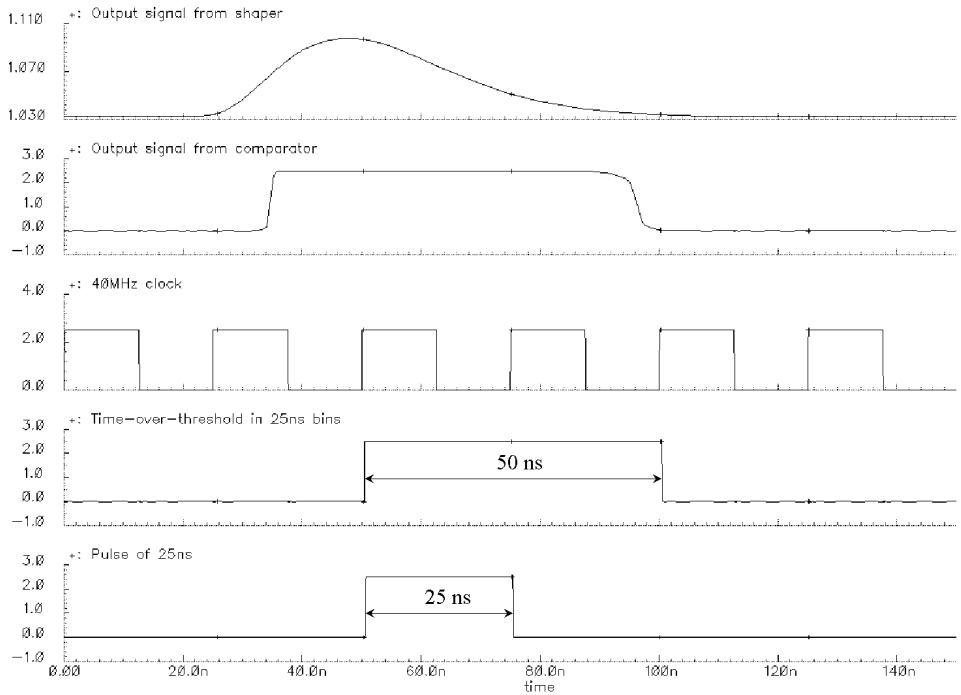


- Total threshold is sum of main threshold plus delta threshold
- 7 Individual threshold steps (3 bit)
- Range of delta threshold and main threshold is common for all channels, 8 bit resolution.
- Polarity of total threshold is selectable



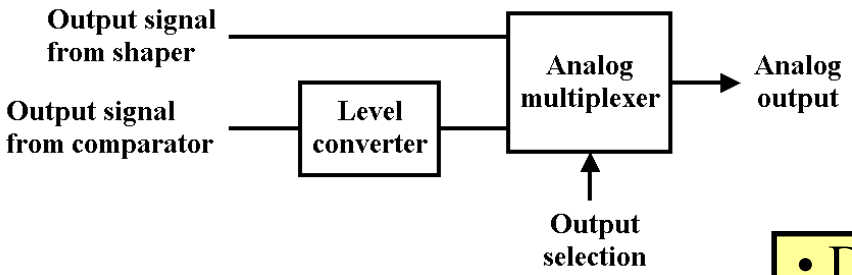
Mode selection circuit





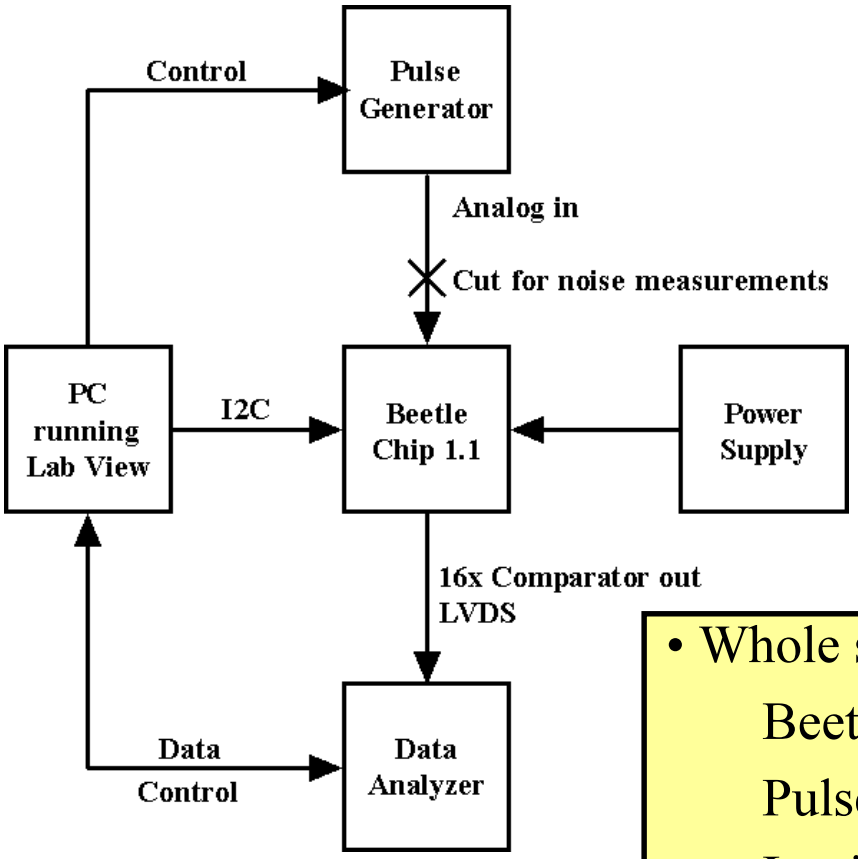
- 2 Output modes
  - Tracking mode (time over threshold)
  - Pulse mode (one clock period)

Level converter circuit



- Digital output (0 to 2.5V) converted to pipeline levels (1 to 1.1V)
- Switch for analogue or binary signal into pipeline

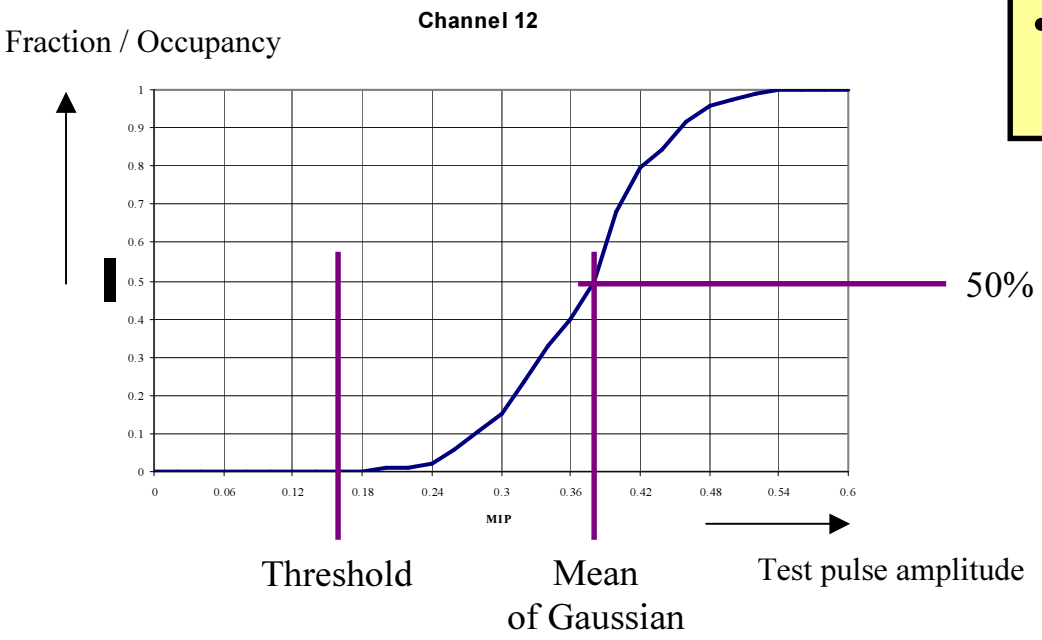
Test setup



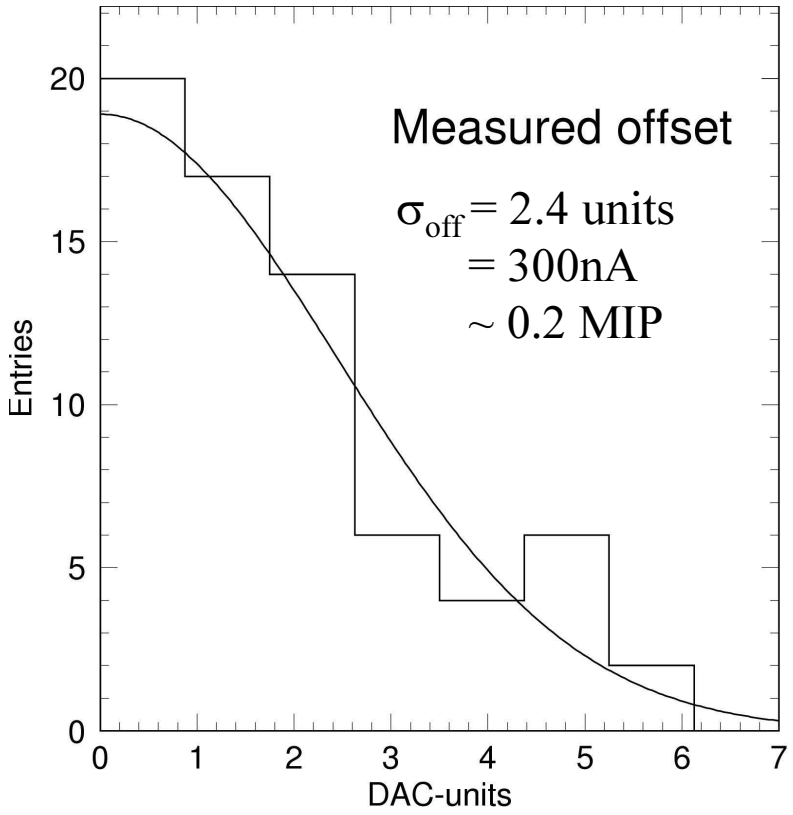
- Whole setup controlled by LabView
  - Beetle settings
  - Pulse generator
  - Logic Analyzer + Oscilloscope
- Test pulse injected via capacitor (3 inputs)
- 16 LVDS output signals plus analogue signal captured simultaneously

Single channel test pulse scan

- Fit with error function
- σ noise (indication)
  channel 12: 0.067 MIP



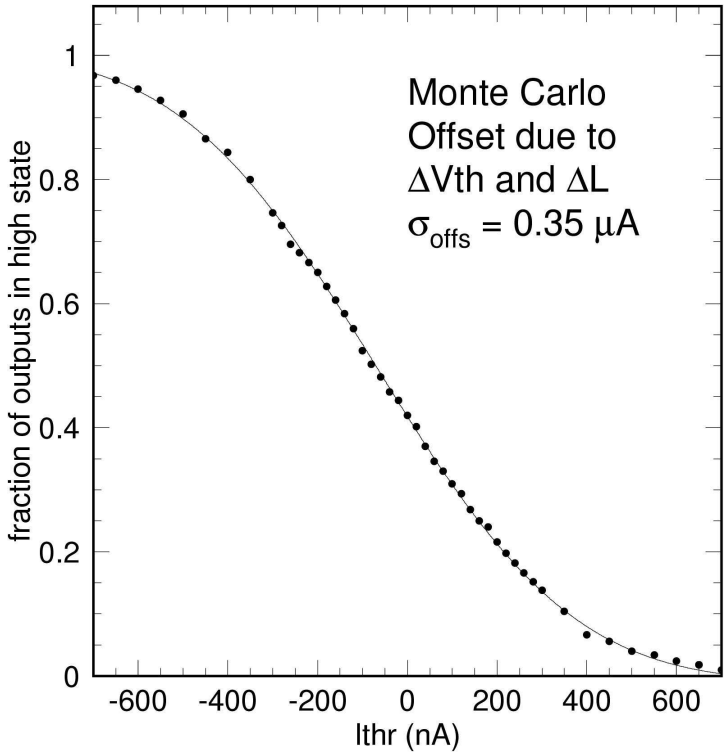
Offset distribution of all channels



- No test pulse
- ~ 50% of channels offset < 0
- Gaussian fit; σ = 2.4 DACsteps
- 1 DACstep corresponds to 125nA
- σ_{off} = 300nA ~ 0.2 MIP

- 2 problems:
- Threshold is unipolar (offset not)
- Large offset spread

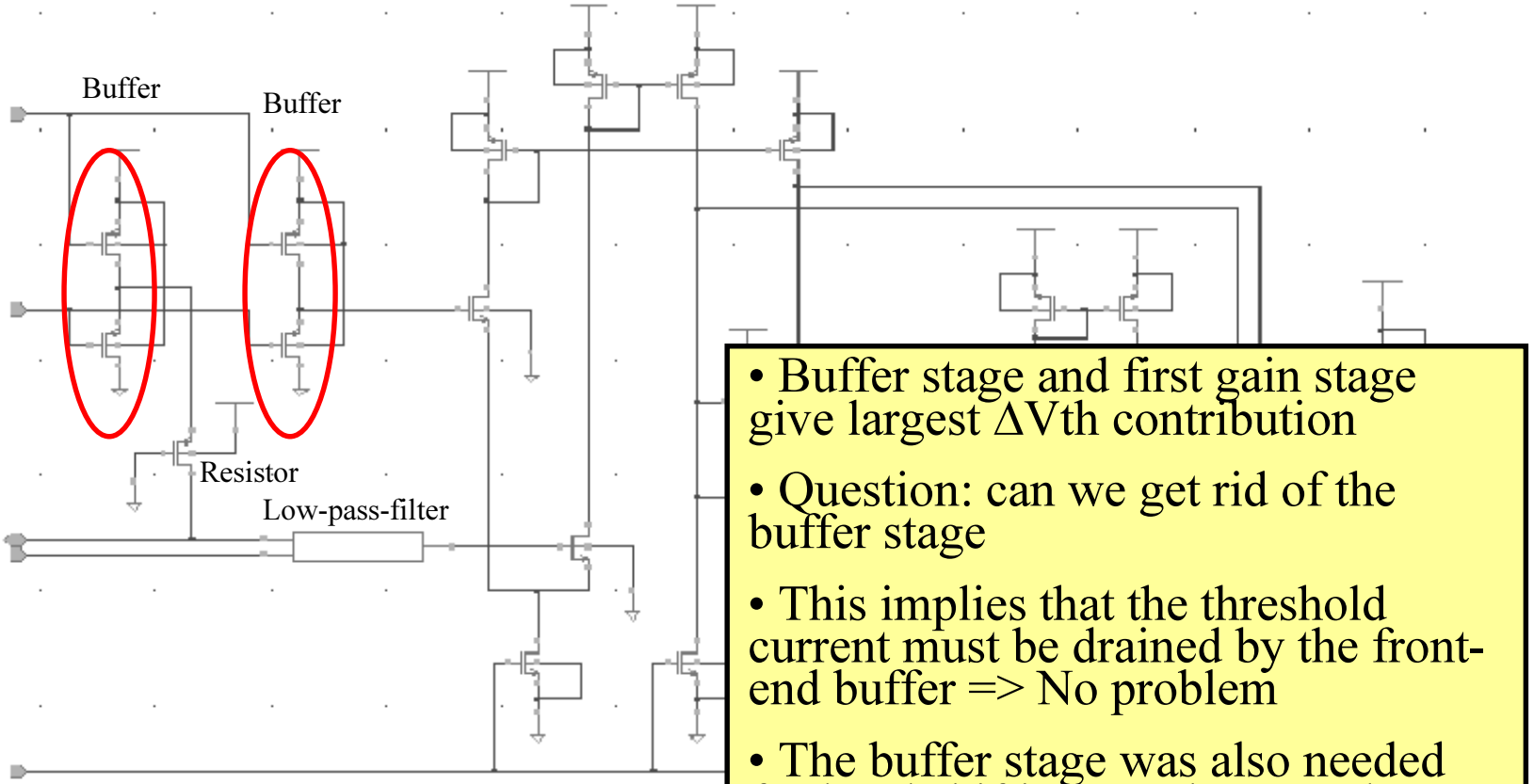
Monte Carlo offset simulation



- 'Error function' due to process parameter variations
- Calculated offset spread σ_{off} = 350nA

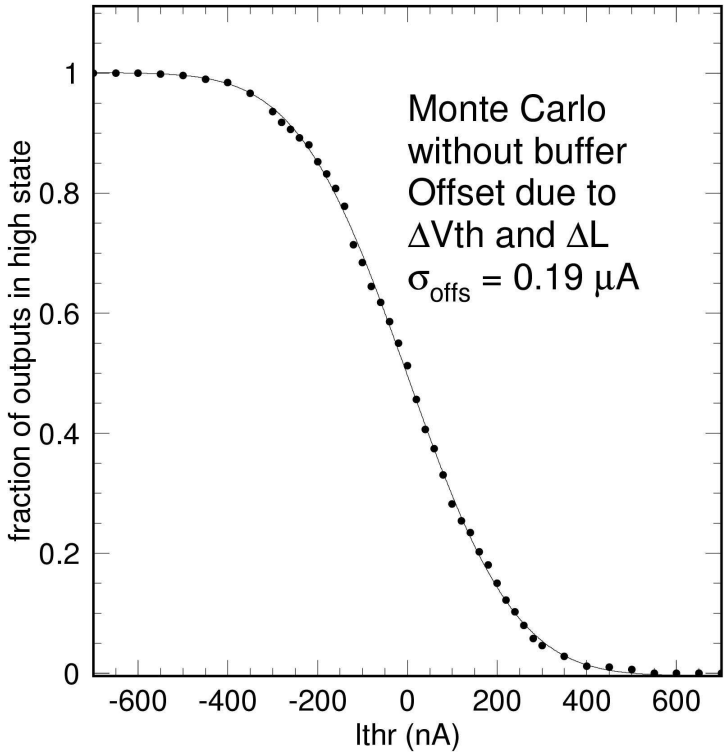
  (measured σ_{off} = 300nA)
- Contribution ΔL: 100nA
- Main contributor ΔVth (inherent to process)

Circuit optimization



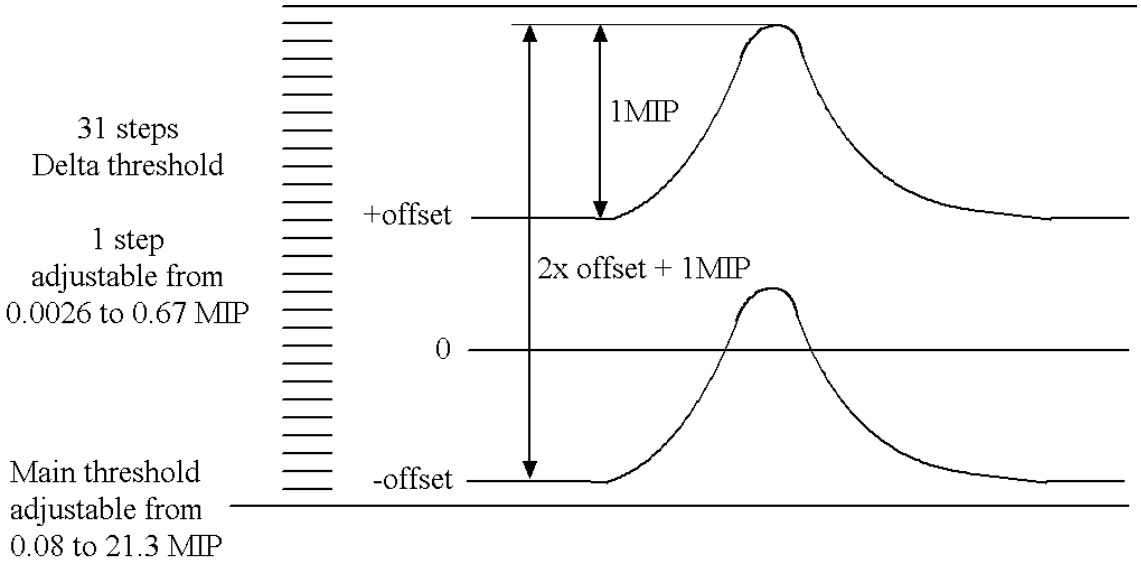
- Buffer stage and first gain stage give largest ΔVth contribution
- Question: can we get rid of the buffer stage
- This implies that the threshold current must be drained by the front-end buffer => No problem
- The buffer stage was also needed for level shifting => change substrate contact of the “resistors”

What do we gain



- σ_{offs} from 0.35 μA to 0.19 μA
- Offset range (-3 σ .. + 3 σ) = 0.76 MIP (calibration depends on front-end settings and C_{load} !)
- 3 bit threshold range too small to correct the offset

New threshold DAC



- Minimal DAC range: 1 + 0.76 MIP
- Required step size < 0.1 MIP
- 5 Bits DAC needed
- Polarity of offset (main threshold) should be opposite to delta threshold
- DAC configuration (1.1/ 1.2): each channel has its own DAC
- This cannot be done for 5 bit DAC (too much area)
- Distribute 5 reference “currents” with local mirror/switches

Conclusions

- Offset spread is too large for 3 bit delta-threshold range
- Solution: remove buffers + extend DAC to 5 bits
- Layout is in progress
- To be implemented for Beetle 1.3