



SEU beam test FIB patch

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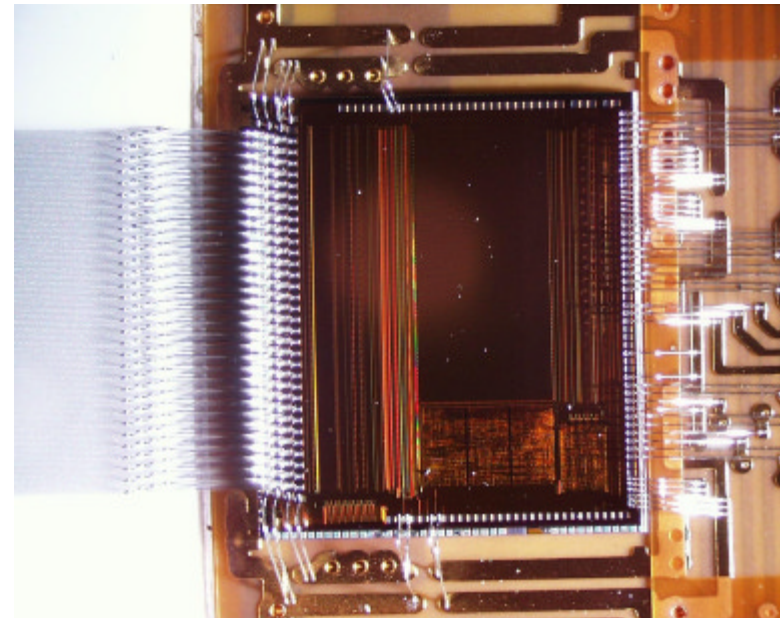
(Max-Planck-Institute for Nuclear Physics, Heidelberg)





Outline

- **SEU beam test**
 - setup
 - results
- **FIB patch**
 - problem
 - patch solution
 - FIB
 - lab-tests



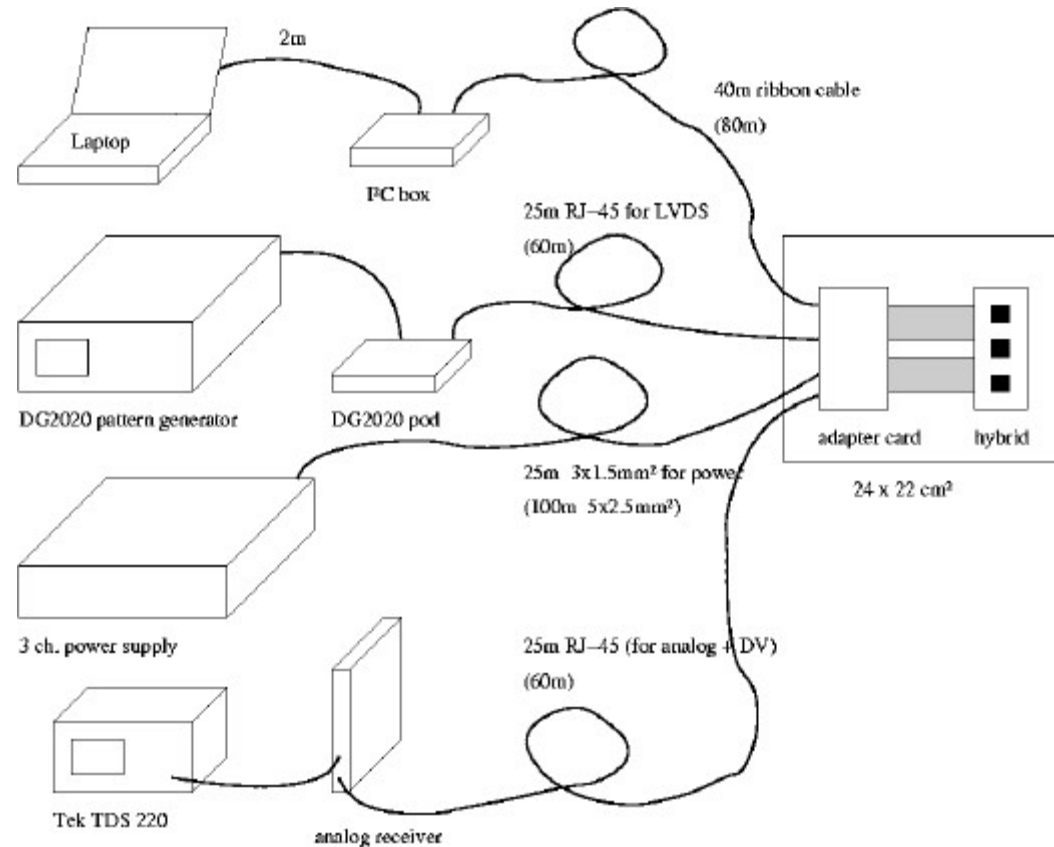
Beetle 1.3 on a IT hybrid





SEU beam test

- SEU beam test at **Proton Irradiation Facility (PIF)** Paul-Scherrer Institute, CH
- Irradiation of 3 Beetle chips:
 - 65 MeV protons
- Check for bit-flips in Beetle registers
 - SEU cross section for a std. flip-flop

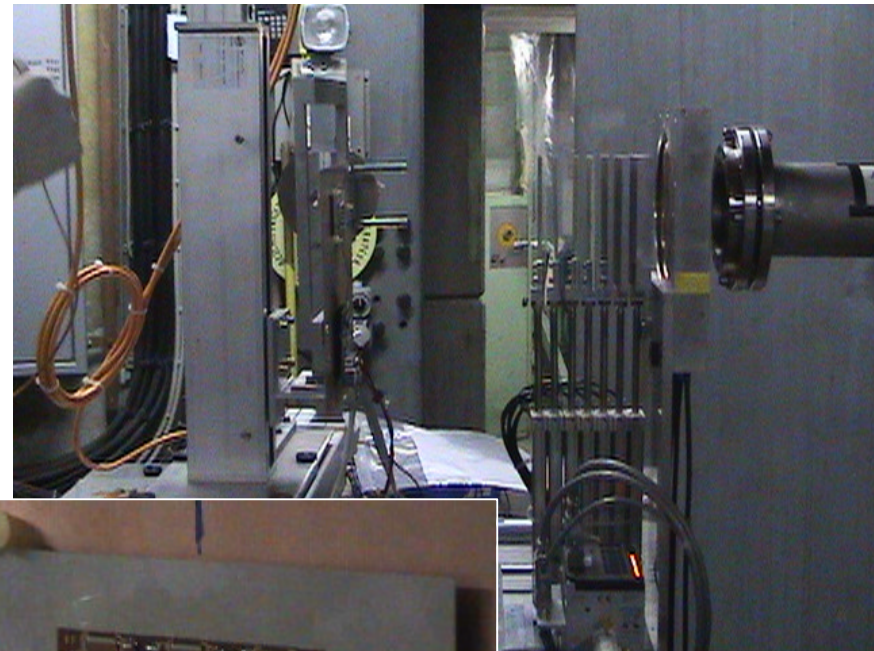




SEU test - setup



setup on top of the irradiation facility



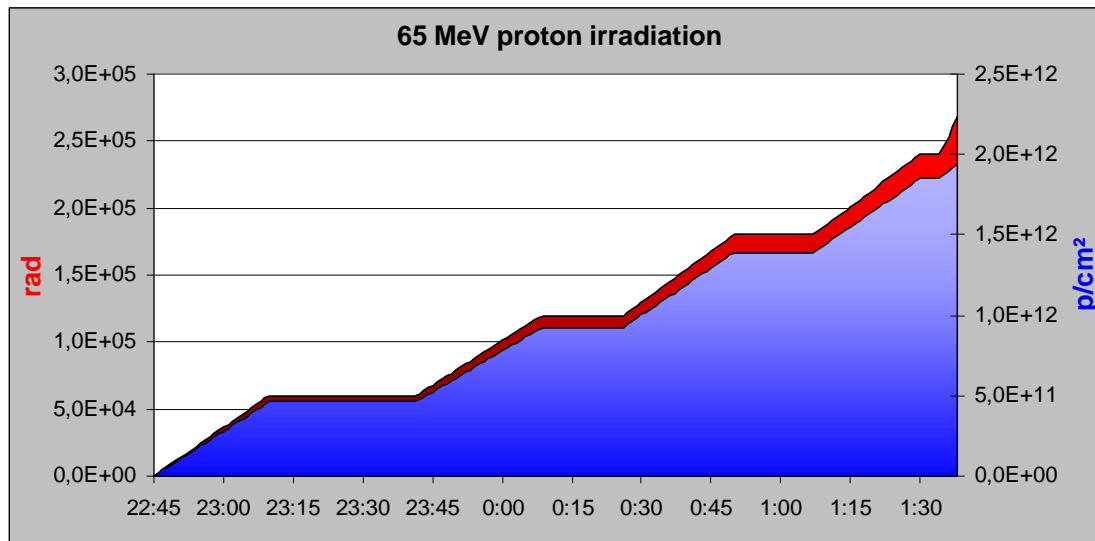


SEU test - irradiation (1)

● Irradiation (Tuesday to Wednesday):

- 65 MeV protons
- mean flux: 3.13×10^8 p/cm²/s
- fluence: 1.95×10^{12} p/cm²
- accumulated dose: 273 krad

- estimated cross section per FF: 10^{-13} to 10^{-15} cm²
 - 1 SEU every 300 s (10^8 p/cm²/s)
 - +/- 1 magnitude



but no SEU bit flips found



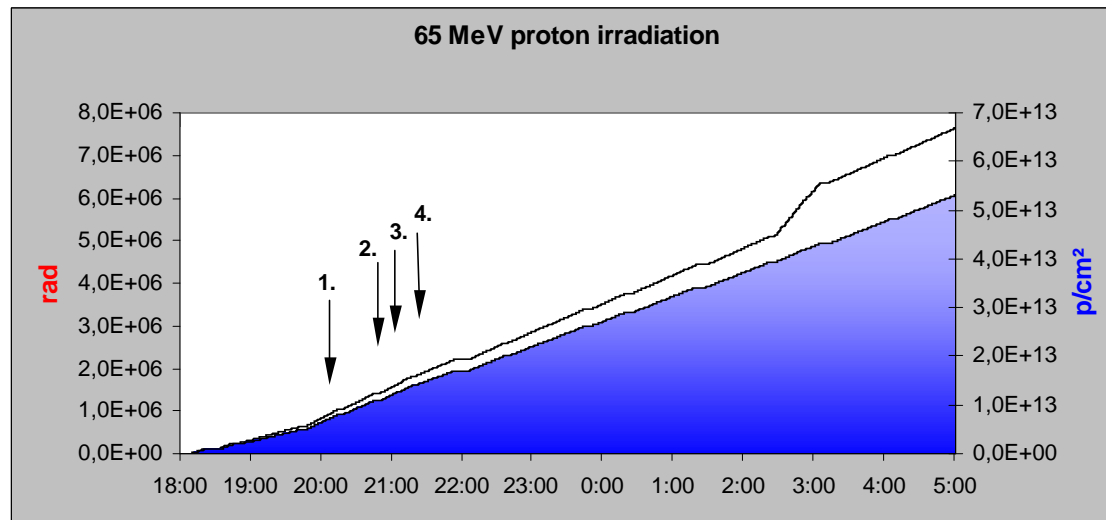


SEU test - irradiation (2)

- **Second irradiation (Thursday to Friday):**

- 65 MeV protons
- mean flux: 1.56×10^9 p/cm²/s
- fluence: 5.31×10^{13} p/cm²
- accumulated dose: 7.66 Mrad

- 4 SEU flips found
- time distribution not yet understood



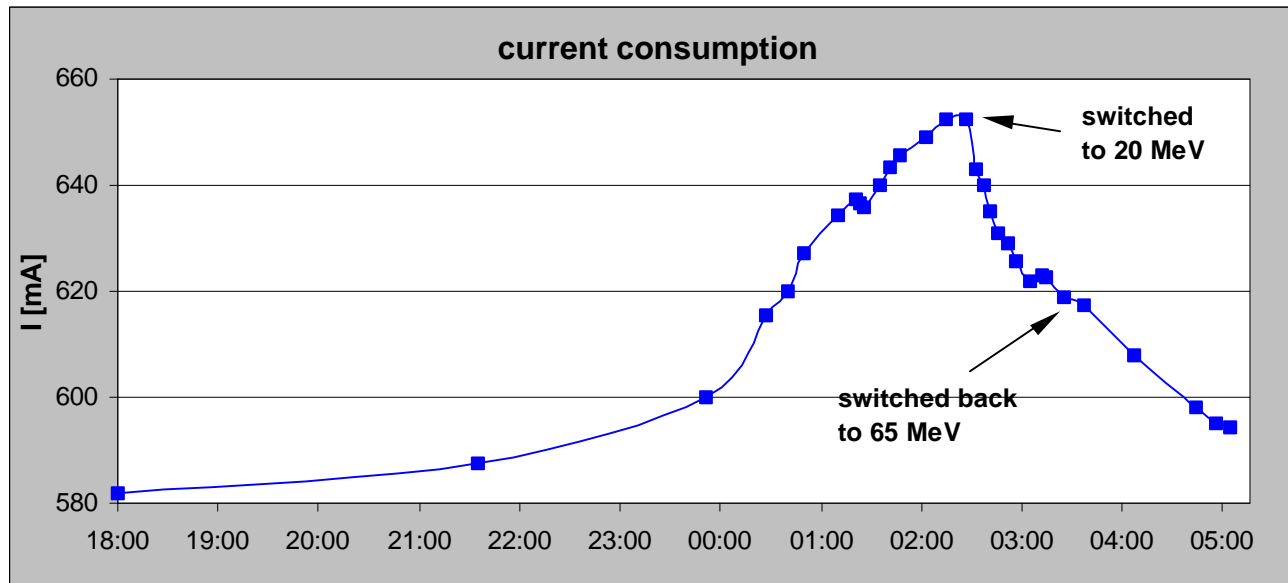
- **Pulse shape scan:**
 - no variation of pulse before / after irradiation





SEU test - power consumption

Current consumption of all 3 Beetle chips



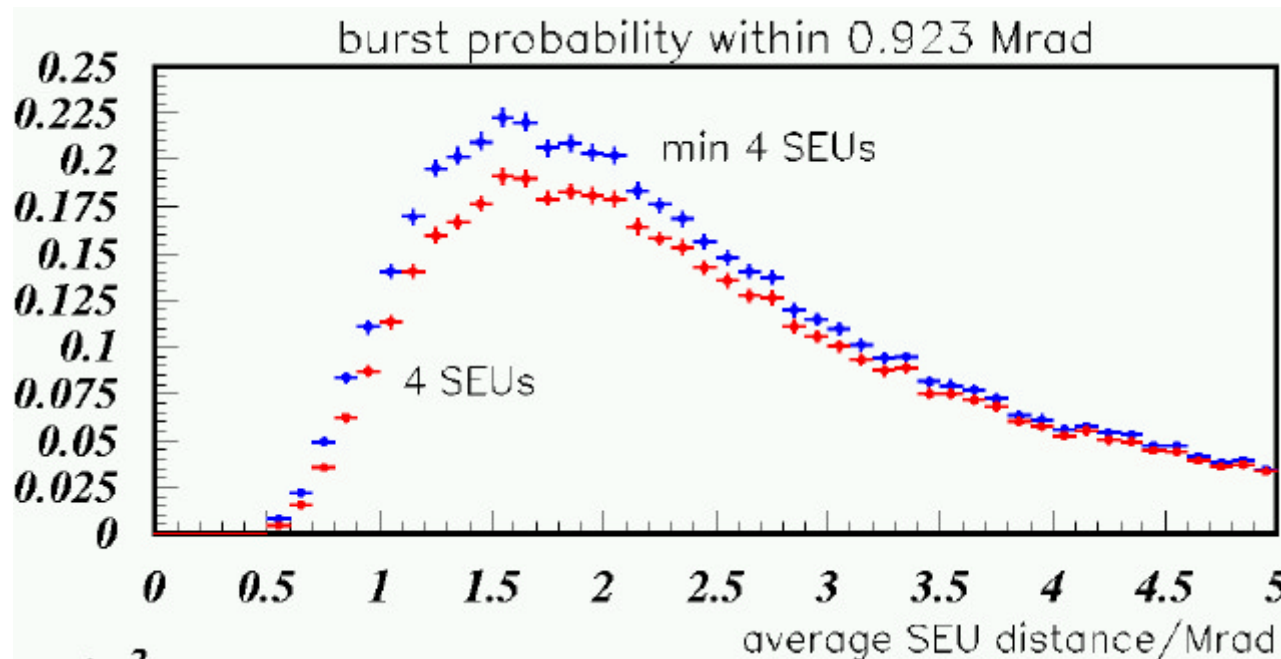
behaviour not yet understood





SEU test - probability

- probability of a burst of 4 SEUs (or more) within a window of 0.923 Mrad (total 6.647 Mrad):
 - 4 SEU: 0,2 % probability... (unlikely...)





SEU test - cross section

- **Analysis is restricted to the 0.923 Mrad window with SEUs under worst condition:**

- 1 monitored SEU per chip per 0.69 Mrad or
- 1 SEU per chip per 0.21 Mrad

- **VELO:**

- 1344 chips (21 stations x 64 chips per station)
- 10 Mrad in 3 years

in total 64230 SEUs or 1 SEU per 25 minutes

- **SEU cross section for a single flip flop for 60 MeV protons:**

$$S = (1.12 \pm 0.56) \cdot 10^{-16} \text{ cm}^2$$

F. Facio: $\sigma = 2 \cdot 10^{-16} \text{ cm}^2$





Readout header: parity bit

1 port mode

AO[0]	I0	I1	I2	I3	I4	I5	I6	I7	P7	P6	P5	P4	P3	P2	P1	P0
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4 port mode

AO[0]	I0	I4	P1	P0
AO[1]	I1	I5	P3	P2
AO[2]	I2	I6	P5	P4
AO[3]	I3	I7	P7	P6

- I0 leading bit (always 0)
- I1 parity of PCN (even)
- I2 Active EDC
- I3 parity of reg. CompChTh
- I4 parity of reg. CompMask
- I5 parity of reg. TpSelect
- I6 SEU counter <1>
- I7 SEU counter <0>

- Parity bit (I1) is wrong encoded in 4 port mode and Rclk divider = 0 (LHCb mode)

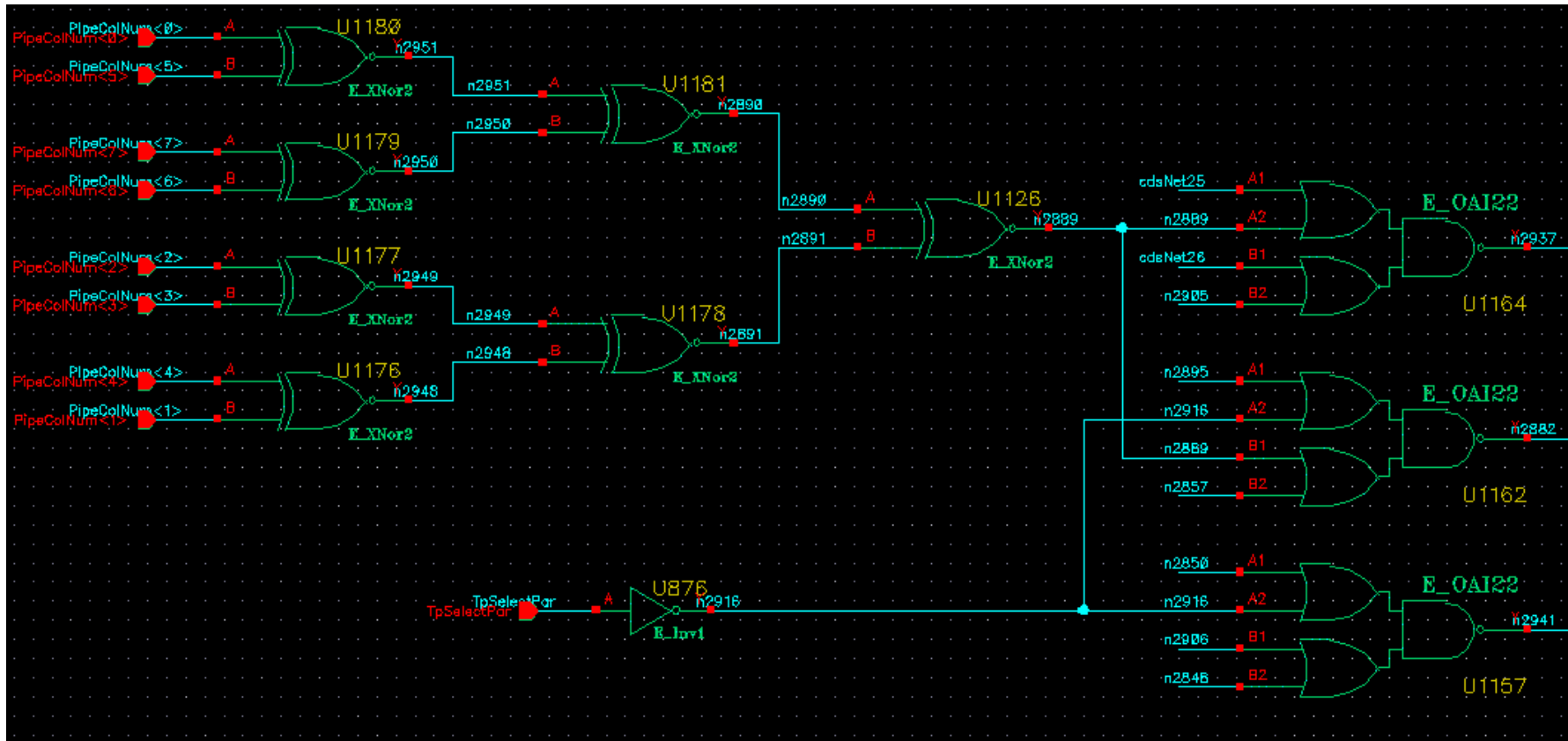
all other modes or Rclk divider settings
→ Parity bit is OK

- problem is understood in verilog
 - not so easy to fix
 - simple workaround: swap position I1 with I5
could be tested on a 1.3 with a FIB patch





Parity bit - workaround (1)

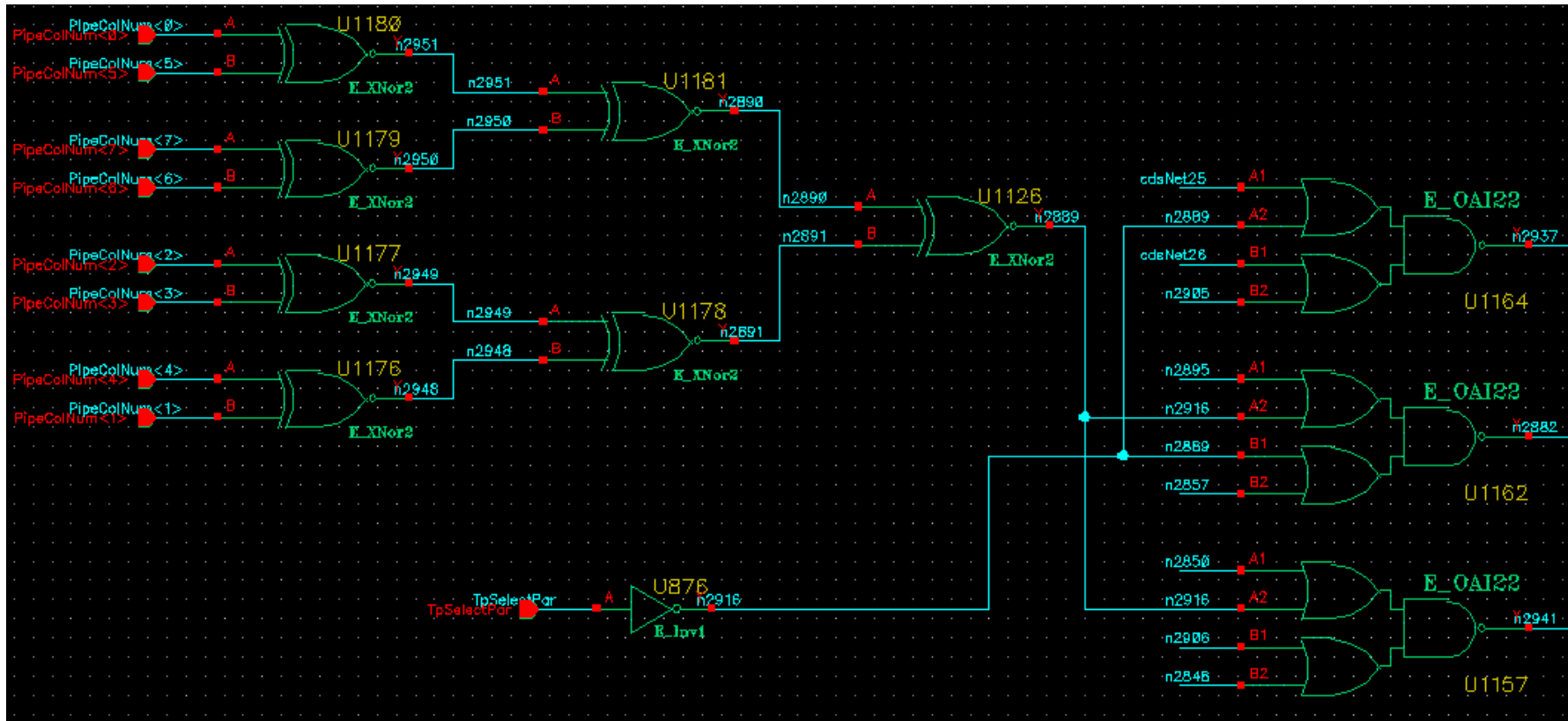


schematic of parity-bit generation (part of MuxScheduler)





Parity bit - workaround (2)



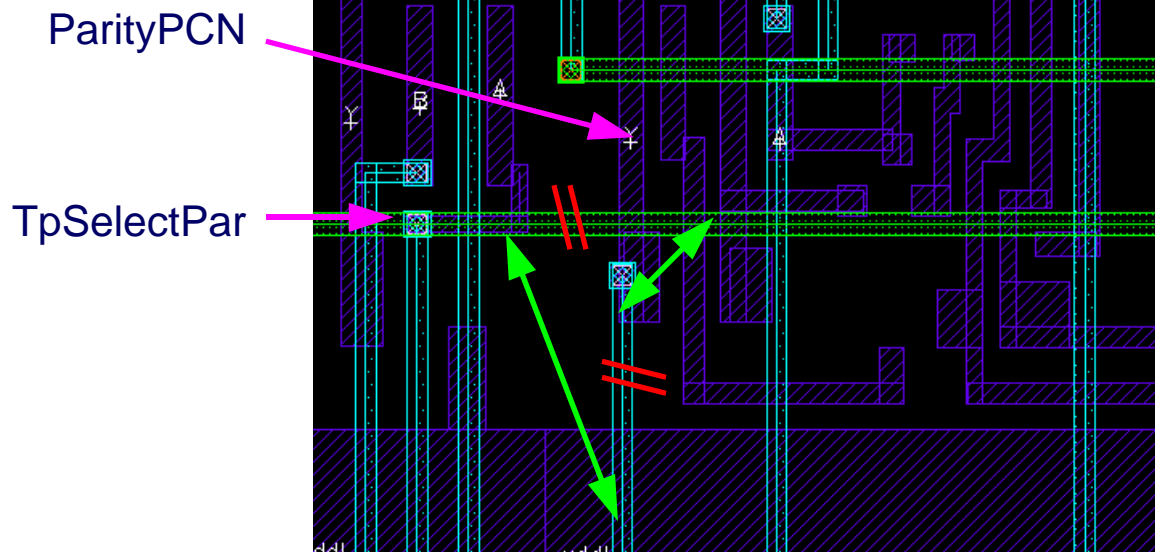
new schematic of parity-bit patch





Parity bit - workaround (3)

- **Layout modification in FastControl of Beetle (could be done by a FIB)**
 - 2 cuts
 - 2 connections

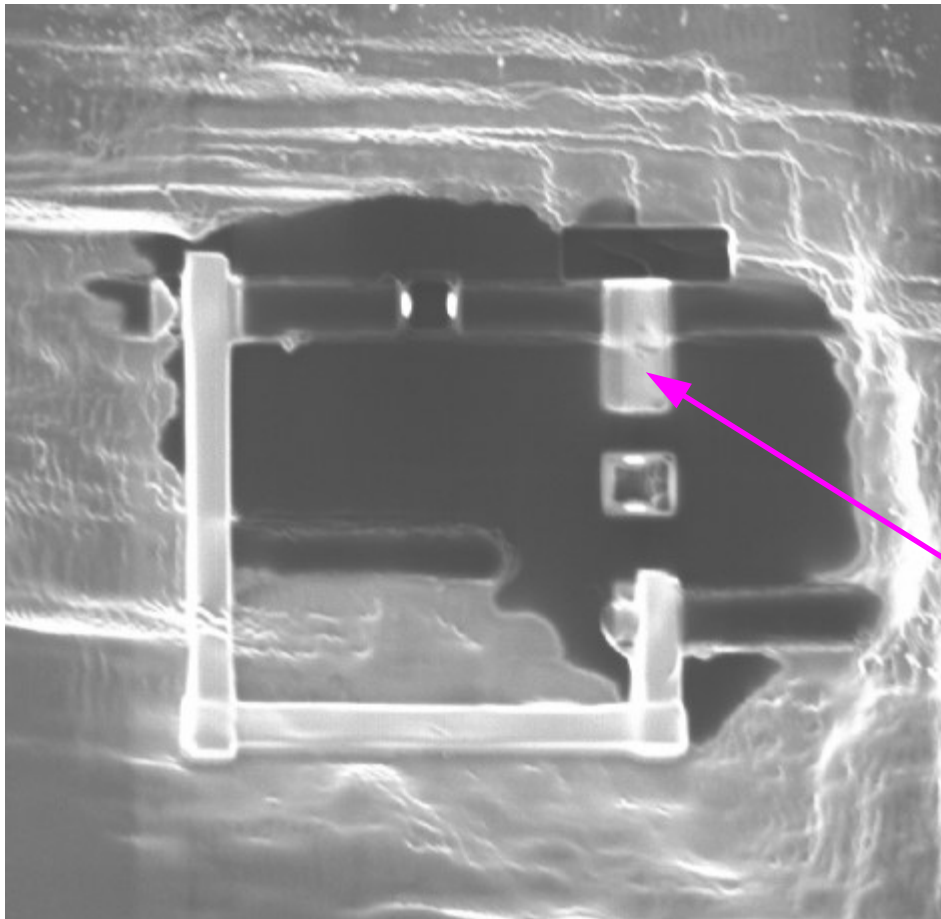


Output device of ParityPCN generation - E_XNor2 (U1126)





FIB patch (1)



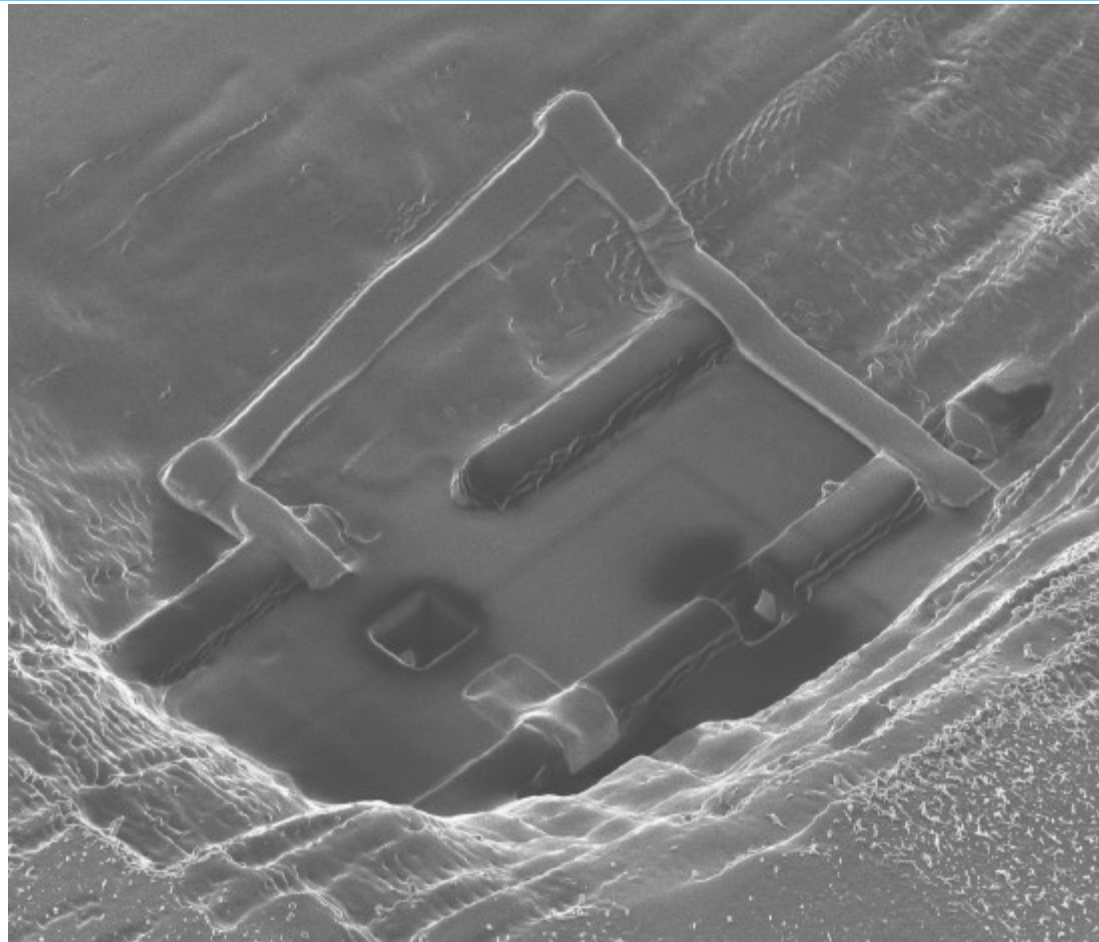
- Swap header bit I1 with I5
- done with a FIB patch (FEICO Munich)

Output device of ParityPCN generation - E_XNor2 (U1126)



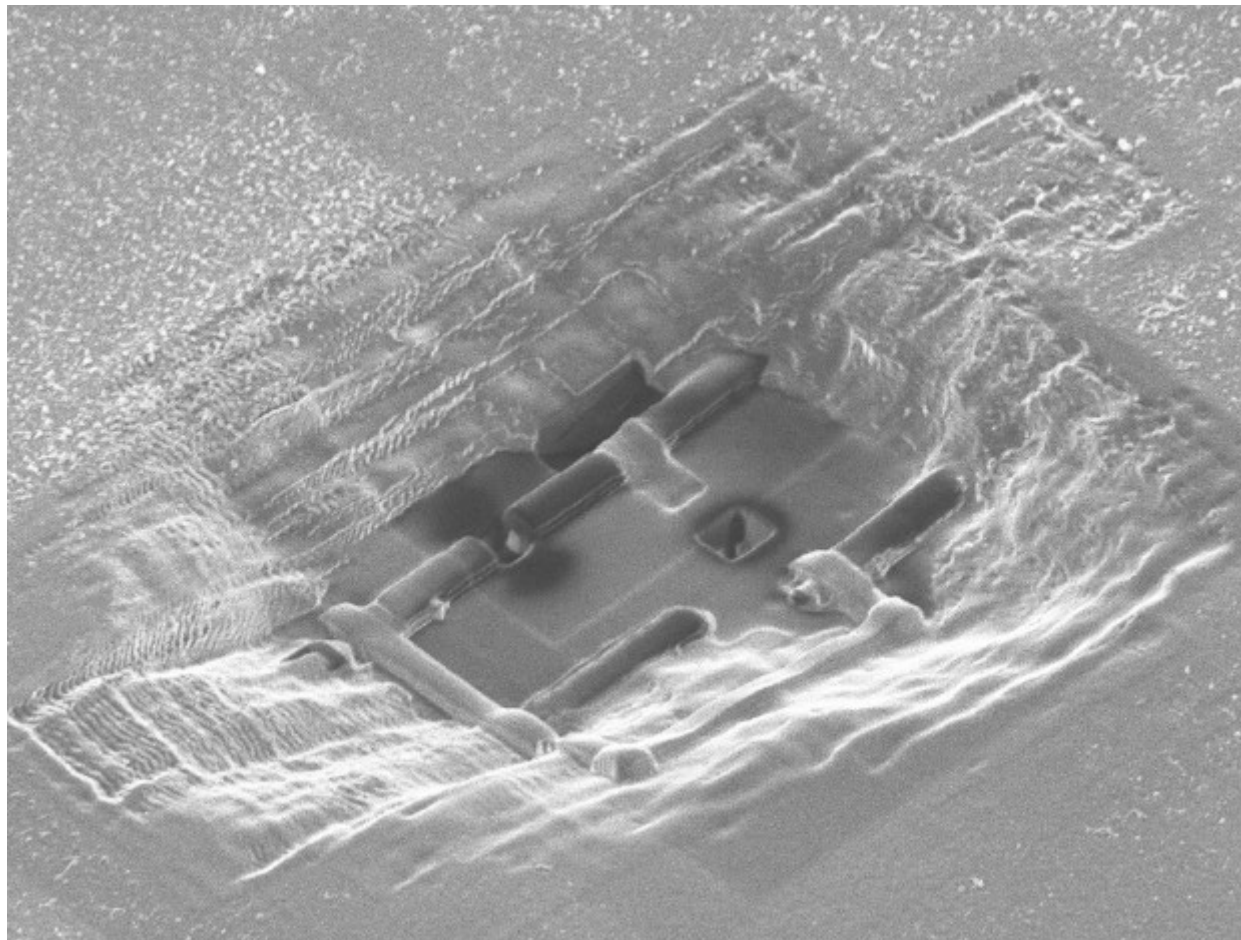


FIB patch (2)





FIB patch (3)





FIB: results:

- **one patched Beetle 1.3 chip tested:**
 - 1 x 10⁶ readouts in 1 port mode (Testmode)
 - 3 x 10⁶ readouts in 1 port mode (LHCb mode)
 - non-consecutive / consecutive readouts
 - different Rclk divider settings
- → Parity bit is now right encoded

- **asynchron trigger:**
 - 3 x 10⁶ readouts
- → no hiccup of FastControl

