Synopsys, Inc. - Synplicity Business Group Presents a Technical Seminar:

Prototyping as a Productive Verification Methodology

Date: Wednesday, September 10, 2008

Location: Ruprecht-Karls-Universitat Heidelberg,
Room 2.404 (2nd Floor)
Im Neuenheimer Feld 227,
69120 Heidelberg, Germany

Time: 1:00 pm - 5:00 pm (Lunch provided)

Register at http://www.synplicity.com/events/protosyncol_2008/register.html

FPGA-based Prototyping has become a mandatory step for successful ASIC/ASSP and SoC design. The use of FPGAs for ASIC or SoC design verification is no longer the "ad-hoc / assembly required" methodology it once was; It has evolved into a truly productive and high-performance ASIC verification solution.

What should you consider when deploying an FPGA-based prototyping system? And, what are the necessary steps involved in getting an ASIC design to work on an FPGA-based prototyping board? You will learn this and more during this FREE technical and educational seminar.

What You Will Get

- A closer look at the HAPS™ architecture and capabilities; System set-up and configuration; Getting the most out of a prototyping system.

- Live demonstrations of the complete flow:
  - Preparing the ASIC design for prototyping
  - Designing partitioning and implementation
  - Prototyping system configuration and bring-up
  - Debugging the design and fixing errors

For more information on FPL, please visit http://www.fpl.org

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