Internship report
Synapse DACs on the HICANN-DLSv2

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1 Introduction

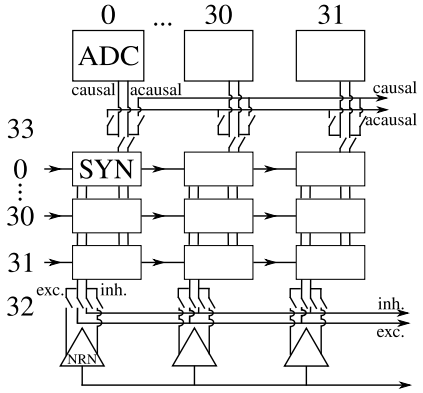

Figure 1: Schematic overview of the HICANN-DLSv2 chip consisting of a two-dimensional array of 32 by 32 synapses with each column of synapses connected to one neuron at the bottom. The current pulse triggered by spike arrival in a synapse can be measured using the output lines.

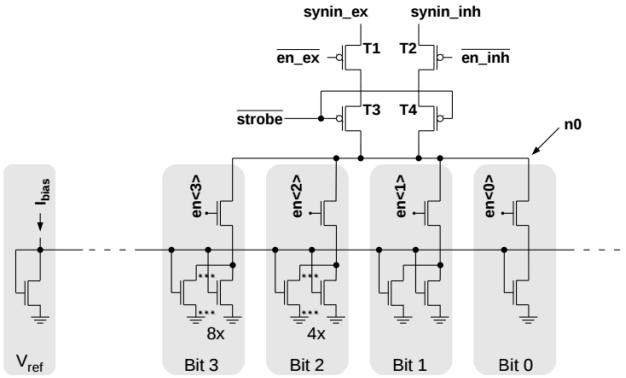

Figure 2: Schematic of synaptic DAC (4-bit version is shown). V_{ref} controls the pulse height. The strobe voltage at T3, T4 is enabled for the duration of the desired pulse length. en_ex and en_inh are used to discern excitatory and inhibitory neuronal input.

The HICANN-DLSv2 is a neuromorphic chip that emulates biologically inspired neural networks in analog circuits. It has been developed as a successor to the HICANN (High Input Count Analog Neural Network) chip to allow for programmable plasticity rules right on the chip as well as a higher integration density (65nm vs. 185nm). The chip's neuron and synapse circuits can be configured to a wide range of model parameters using analog and digital memory. The chip consists of 32 neuronal columns, each with a row of 32 synapses as

shown in Fig. 1. Pre-synaptic spikes are sent to the synapses row-wise from the left as suggested by arrow direction. Each synapse may be assigned a 6-bit address and if a synapse registers a spike addressed to itself, it generates a current pulse with an amplitude proportional to a 6-bit weight that is sent down to the neuron via either the excitatory or inhibitory input (controlled by a static switch). Both weight and address are stored in SRAM local to the synapse.

The height of the generated current pulse is controlled by a 6-bit Digital-to-Analog Converter (DAC) within the synapse that is statically connected to the stored weight. Ideally, the pulse height should be linearly correlated with the stored weight. The slope of this linear correlation, i.e. the maximum current is controlled by the synaptic bias parameter that corresponds to the gate voltage V_{ref} shown in Fig. 2. This parameter is global and applies to all synapses.

The synaptic current output may be directed to the inhibitory and excitatory debug output lines via the switches shown in Fig. 1. The Analog-to-Digital Converters (ADCs) shown at the top are used for reading out spike timing correlation and not relevant in the scope of this report. The main goals of the internship project which are subject to this report are defined as follows

- Verify the linear correlation of synaptic weight and synaptic current for all $32 \cdot 32 = 1024$ synapses and all $2^6 = 64$ possible weights for several reasonable synaptic biases.
- Find the operating range of the synaptic bias parameter, i.e. establish the lower bound where linear correlation breaks down and noise effects start to dominate.

2 Methods

In the following the methods employed to achieve the measurement goals given above are described.

2.1 Linear correlation of synaptic weight and current

The synaptic output current was measured by using a debug pin on the board upon which the HICANN-DLSv2 chip resides. This debug pin is connected to the excitatory output line shown in Fig. 1. This mandates that all synapses are statically switched to the excitatory line. A source meter (Keithley 2635) was used that sources a constant voltage across it's output terminals while measuring the flowing current. The current was averaged over 2 NPLC (Number of Power Line Cycles, corresponding to 0.04s) with an accuracy of $0.15\% + 3$pA.

In order to establish the linearity of the DAC, it would have been ideal to make the DAC output a constant current by constantly providing appropriate gate voltages (strobe $= 1.2$V, en_ex $=$ en_inh $= 1.2$V) on transistors T1, T2, T3 and T4 in Fig. 2. Alas, this was not possible due to chip implementation details. It was therefore decided to subject the synapses

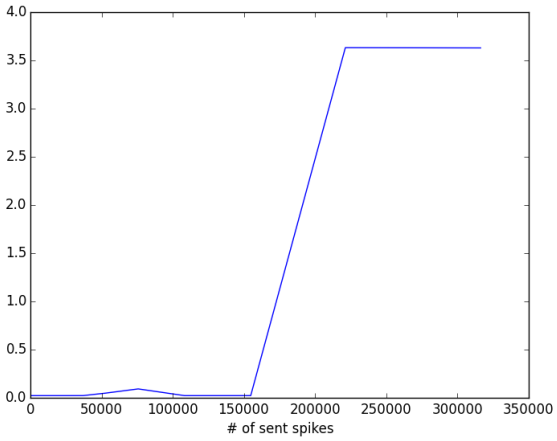

Figure 3: Measured current averaged over 2 NPLC using the source meter in arbitrary units when varying spike number for a fixed individual spike length of 32 clock cycles. As the current reaches a saturation, we choose to send 250000 spikes into a synapse for following measurements.

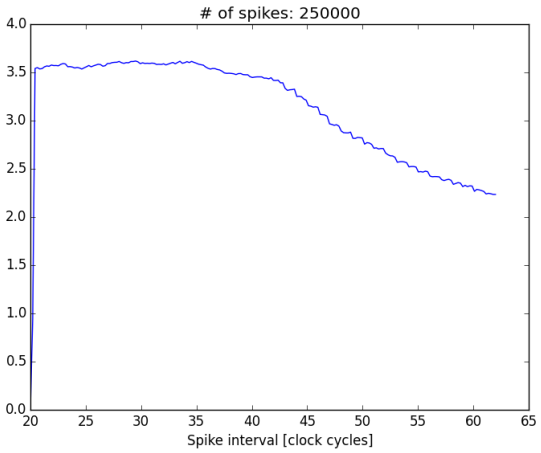

Figure 4: Measured current averaged over 2 NPLC using the source meter in arbitrary units when varying spike interval for a fixed total spike number of 250000. We conclude that if the spike interval is set to 32, the current is in the saturation regime. Later investigation revealed a minimum spike interval of 43 clock cycles, consistent with this graph.

to a train of spikes that resembled this behavior as close as possible. The maximum spike pulse length is 32 clock cycles. The spike interval was set to 32 clock cycles.

The total number of spikes to send into the synapses had to be determined by measuring the current when varying this number. It should be chosen such that the synaptic output current endures over the entire averaging period of 2 NPLC. The expectation was that the current saturate when a certain number of spikes was exceeded. This was confirmed by the measurement presented in Fig. 3 and a total spike number of 250000 was chosen to be appropriate to conduct the weight linearity experiment. Further confirmation of this notion is presented in Fig. 4 where it is shown that a spike interval of 32 clock cycles is well within the saturation regime. Later investigation revealed that the minimum spike interval is in fact 43, explaining why the current only systematically decreases for a spike interval larger than 43.

The actual measurements were conducted using a Python script that built upon existing scripts provided to the author. Because the output line current is the sum of all synaptic column currents, each synapse had to be probed individually. All synapses were assigned the same address and an individual synapse DAC measured by sending the spike train to the corresponding row and setting the proper column switch.

The acquired data was then examined for linearity.

2.2 Operating range of synaptic bias voltage

The usable operating range of the synaptic bias voltage is defined by the lower boundary where noise effects start to dominate the dwindling current and linearity breaks down. This boundary was determined by observing the degree of linear correlation of weight and synaptic current for a range of bias voltages. In any actual use case, the spike pulse length would rarely be set above one single clock cycle and therefore a pulse length of one was used for these measurements.

The synaptic bias voltage corresponds to the gate voltage V_{ref} in Fig. 2 and is given as a fraction of $2^{12} - 1 = 4095$ within the software framework that was used. The maximum operating voltage that is scaled using this fraction is 1.2V.

The script written for the first task was modified to provide the desired functionality.

2.3 Correcting measured currents

All current measurements have to be corrected for the fact that the source meter averages over 2 NPLC and the spike train exhibits a duty cycle specific to the chosen pulse length and pulse interval. As the averaging period of 2 NPLC equivalent to $4 \cdot 10^{-2}\text{s}$ is much larger than the pulse interval in the order of 10^{-8}s, the measured current can be corrected using a factor of L/T where L is the pulse length and T is the pulse period. We therefore measure the actual spike train period for spike intervals set in software in order to find T.

3 Results

3.1 Correcting measured currents

In order to correct the measured currents for the duty cycle of the spike train, the unit clock cycle and minimum spike interval had to be determined. This was done by continually sending a spike train into a row of synapses and observing the post-synaptic voltage at the neuron. A waveform with the period of the spike train was observed using an oscilloscope. This period was measured for a wide range of spike intervals that were set in software. It was observed that the spike interval saturates at a minimum of $(445.38 \pm 0.48)\mathrm{ns}$ (see Fig. 5). The unit period per set clock cycle was obtained from a linear fit in Fig. 6. It is given as $(10.4207 \pm 0.0020)\mathrm{ns}$. This implies that the spike interval saturate at a minimum of $(42.74 \pm 0.05) \approx 43$ clock cycles which is in good agreement with the previous measurement in Fig. 4. The measured current is therefore scaled by a factor of $N/43$, where N is the pulse length in clock cycles.

3.2 Linear correlation of synaptic weight and current

The current from all 1024 synapses for all possible 64 weights was measured once for $V_{\mathrm{ref}} = 0.4102\mathrm{V}$, $V_{\mathrm{ref}} = 0.4400\mathrm{V}$ and $V_{\mathrm{ref}} = 0.4689\mathrm{V}$. The measurement was conducted by sequentially measuring all weights for a single synapse and then proceeding to the next synapse. Exemplary measurements for the highest possible weight are visualized using a heat map in Fig. 7, 8 and 9. From comparing these measurements we can deduce that there is systematic variation between the synapses with respect to the current delivered by their DACs that is not due to statistical fluctuation. Averaging the current across all synapses yields (mean and standard deviation) $(3.52 \pm 0.07)\mu\mathrm{A}$, $(5.94 \pm 0.10)\mu\mathrm{A}$ and $(9.22 \pm 0.13)\mu\mathrm{A}$ respectively.

A two-dimensional histogram of the entire measurement is presented in Fig. 10 for $V_{\mathrm{ref}} = 0.4102\mathrm{V}$. This plot includes all synapses and a substantial degree of linear correlation is evident. This data is averaged over all synapses and plotted with the standard deviation in Fig. 11. A current shift at weight 31 is visible. This is due to a mistake in chip design (well-proximity effects). The degree of linear correlation is quantified as $r > 0.9998$ for all three biases.

3.3 Operating range of synaptic bias voltage

3.3.1 Current offset

The current offset was measured at zero weight and for open switches, i.e. when none of the synapses were connected to the output line.

A measurement was conducted where the synaptic weight was set to zero and a wide range of biases was swept by measuring the synaptic current just as described before. This was

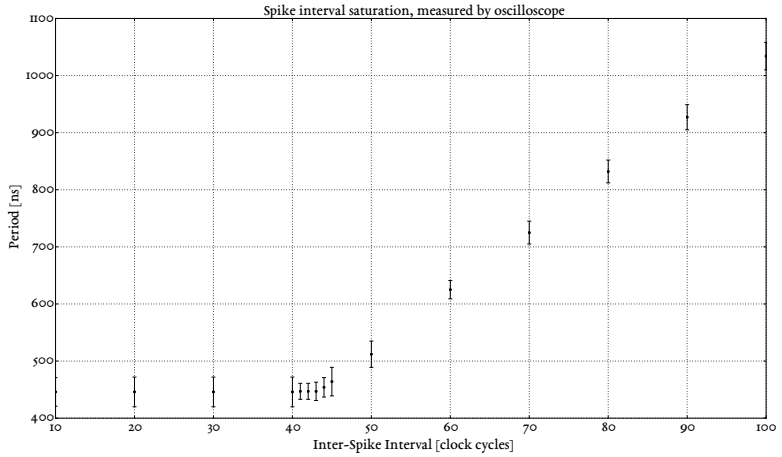

Figure 5: Measured period of spike train for different spike intervals set in software. There is a minimum period for spike intervals less than 43. The period was measured using an oscilloscope and by taking in the order of 10^6 measurements.

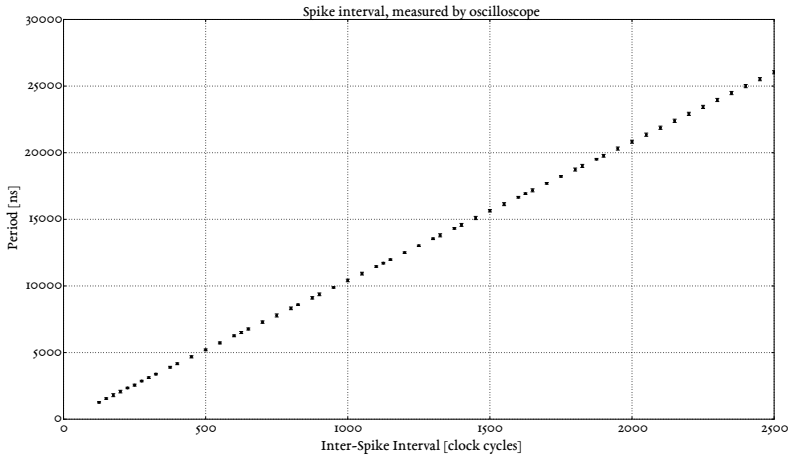

Figure 6: Measured period of spike train for different spike intervals in order to determine the unit clock period. The period was measured using an oscilloscope and by taking in the order of 10^6 measurements. The slope resulting from a linear fit is (10.4207 ± 0.0020)ns per clock cycle.

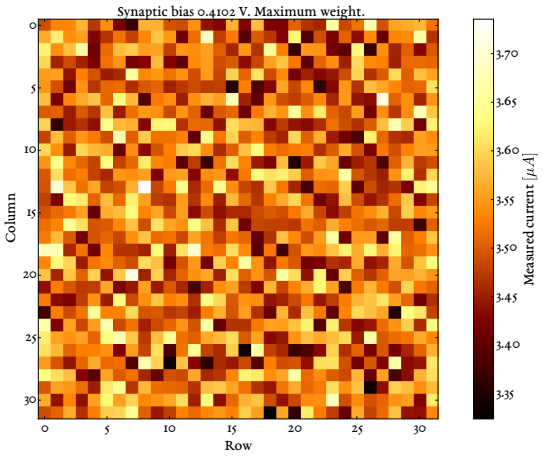

Figure 7: Corrected current for all synapses for $V_{\text{ref}} = 0.4102\text{V}$ and maximum weight when subjecting the synapse with a spike train. The variation is dominated by fixed-pattern noise.

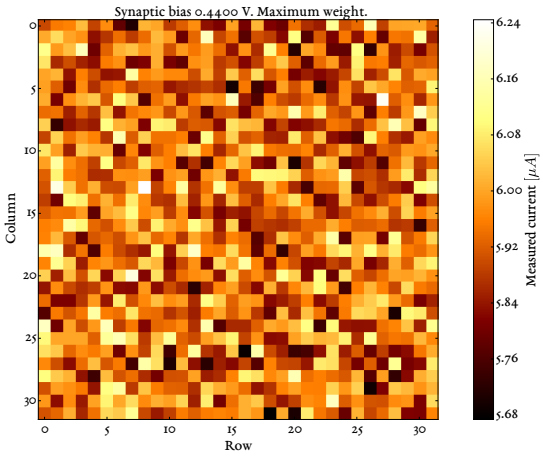

Figure 8: $V_{\text{ref}} = 0.4400\text{V}$

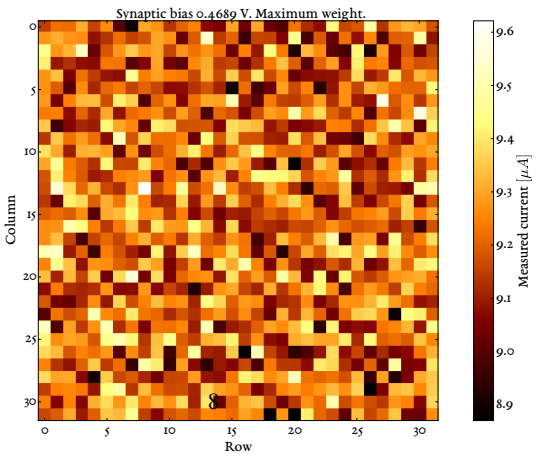

Figure 9: $V_{\text{ref}} = 0.4689\text{V}$

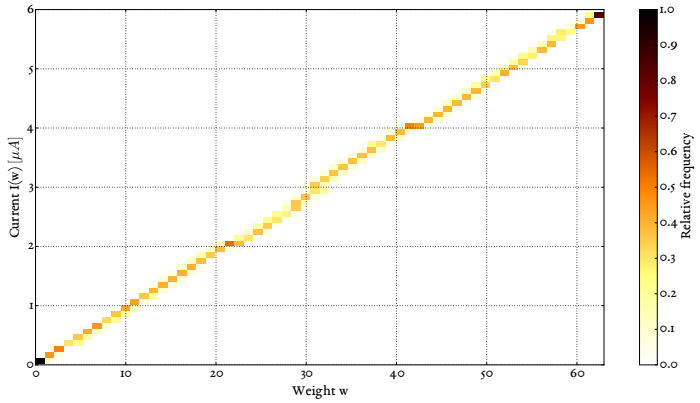

Figure 10: Two-dimensional histogram including measurements of all 1024 synapses for $V_{\text{ref}} = 0.4102\text{V}$.

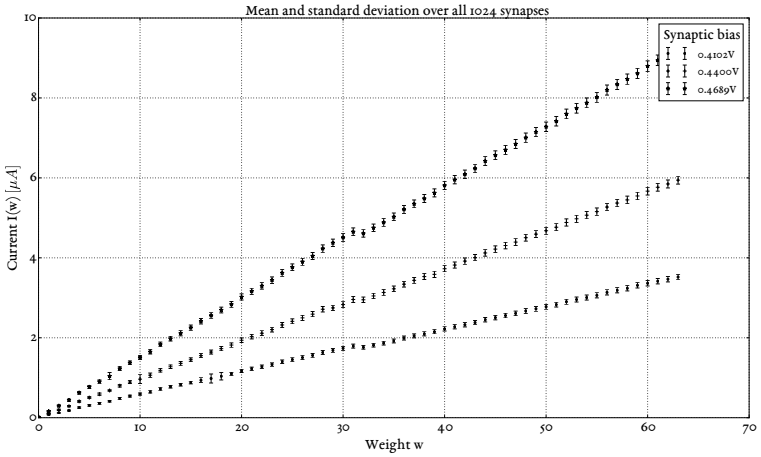

Figure 11: Current over weight for different synaptic biases when averaging over all synapses.

done in order to verify that there is no systematic correlation between the bias and synaptic current at zero weight or when the switches are not closed.

Both measurements were conducted using the three by three synapses in the top left of the chip. The corrected results are given in Fig. 12 and Fig. 13. As the variation of the current is not substantially larger than the precision of 3pA and there is no systematic decrease or increase of the offset for increasing biases in both cases, it is concluded that there is no correlation of synaptic bias and current when the synaptic weight is set to zero or when the switches are open.

3.3.2 Usable range

The relation of weight to synaptic current was examined with respect to linear correlation for different bias voltages and pulse lengths of one, two and three. Because of the large number of synapses, the first measurements were conducted using the top- and leftmost three by three synapses only. The hereby established lower boundary for the usable range was then confirmed using a measurement of all synapses.

Fig. 14 shows the linear correlation (Pearson's r) of the weight-current curve for the mentioned synapses at different bias voltages for a pulse length of one clock cycle. It is evident that for small voltages, the linear correlation breaks down while for larger voltages, it is nearly one (ideal linear correlation) and consistent across the synapses. A preliminary lower boundary was set at $V_{\text{ref}} = 0.20\text{V}$.

Additionally, the same measurement was undertaken for pulse lengths of two and three (Fig. 15 and 16). The same effect of linearity breaking down at small biases is observed.

4 Discussion

4.1 Linear correlation of synaptic weight and current

It was demonstrated that the synaptic current is linearly correlated with synaptic weight. Therefore, it was confirmed that the synaptic DACs work as expected for the used synaptic biases. The systematic shift at weight 31 is explained by a mistake in chip design as mentioned before. It was found that there is some degree of variation with respect to the delivered current between different synapses (Fig. 7, 8 and 9). This is due to fixed-pattern noise and was also expected.

4.2 Operating range of synaptic bias voltage

It was confirmed that the current offset is constant at zero weight as well as for open switches when varying the synaptic bias. When comparing the offset currents in Fig. 12 and 13 with the offset in Fig. 18, we find a remarkable difference of at most 10%. This is presumed to be

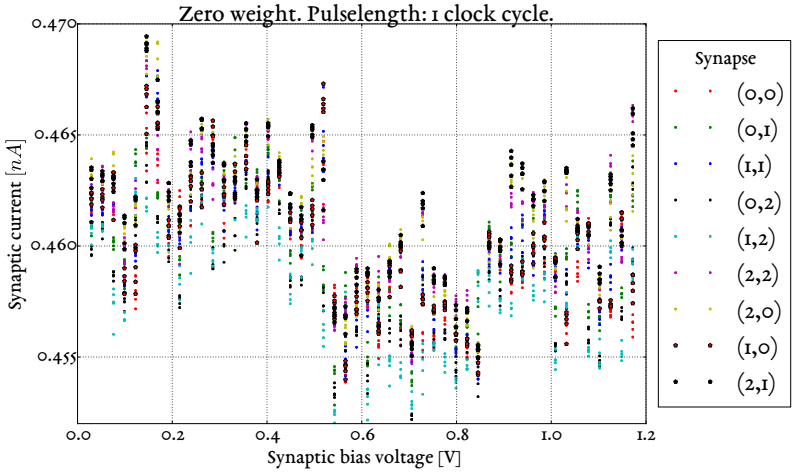

Figure 12: Current offset for zero weight at different synaptic biases. It is concluded that the synaptic bias has no systematic influence on the current offset at zero weight.

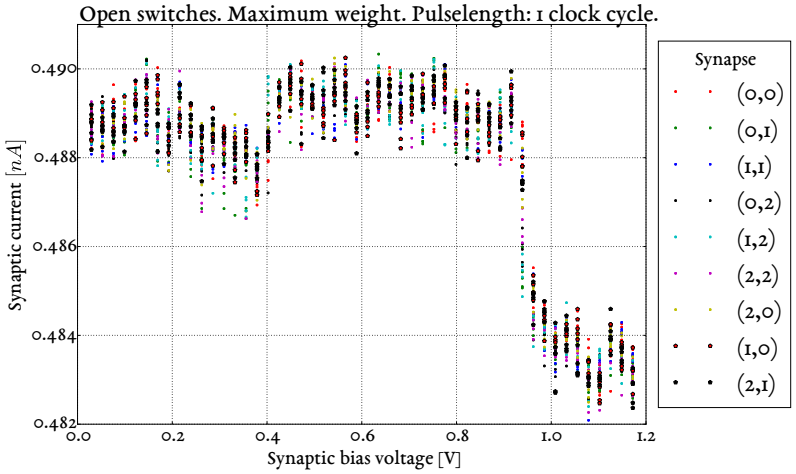

Figure 13: Current offset for open switches at maximum weight for different synaptic biases. It is concluded that the synaptic bias has no systematic influence on the current offset when the switches are open.

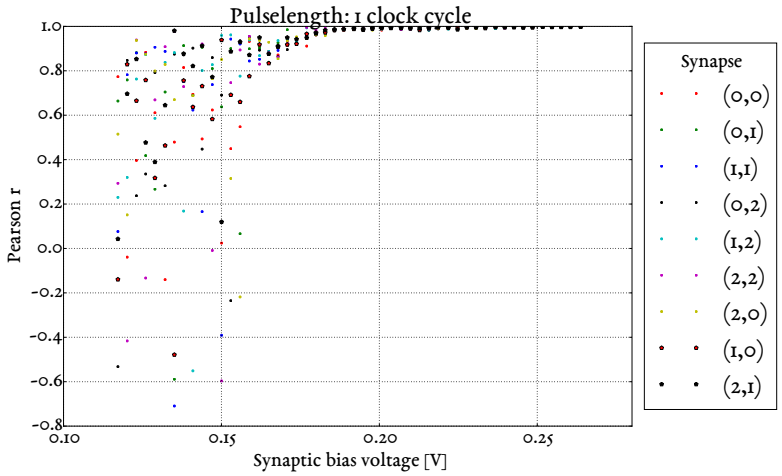

Figure 14: Linear correlation of weight and current for a pulse length of one for a range of bias voltages. The three by three synapses in the top left of the chip were measured. An arbitrary lower boundary may be taken at 0.2V.

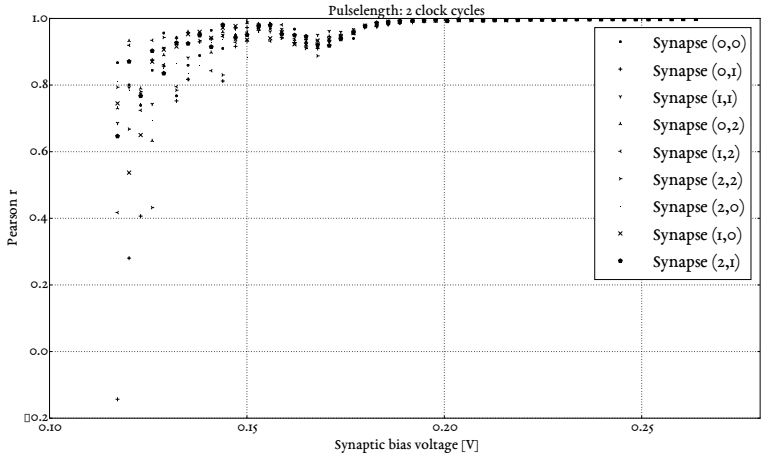

Figure 15: Linear correlation of weight and current for a pulse length of two for a range of bias voltages. The three by three synapses in the top left of the chip were measured.

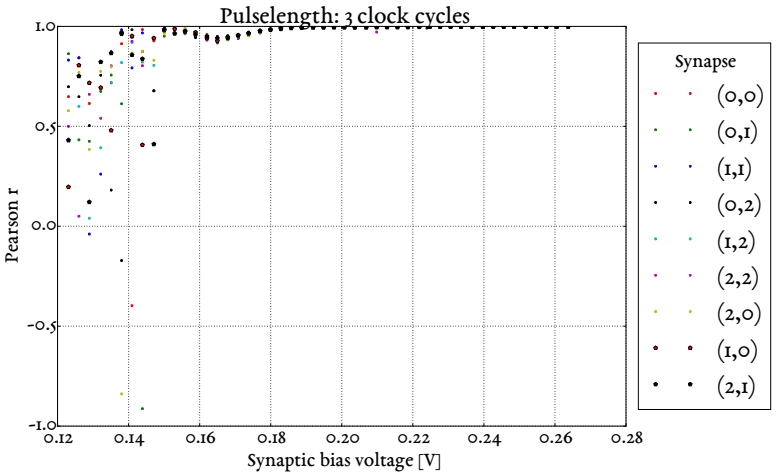

Figure 16: Linear correlation of weight and current for a pulse length of three for a range of bias voltages. The three by three synapses in the top left of the chip were measured.

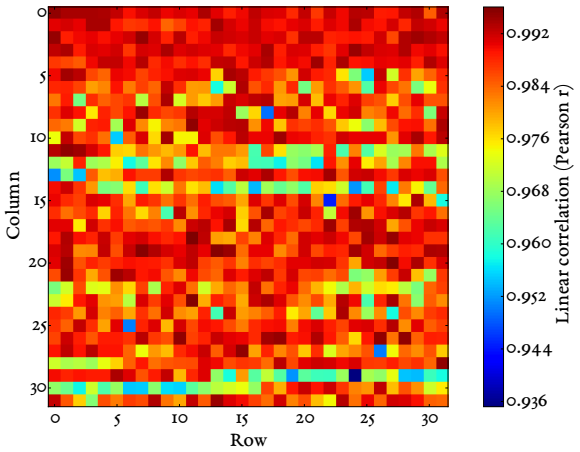

Figure 17: Linear correlation of the current-weight curve for all synapses at the preliminary lower boundary of the bias voltage of 0.20V, visualized using a heat map. This suggests that all synapses provide roughly the same degree of linear correlation.

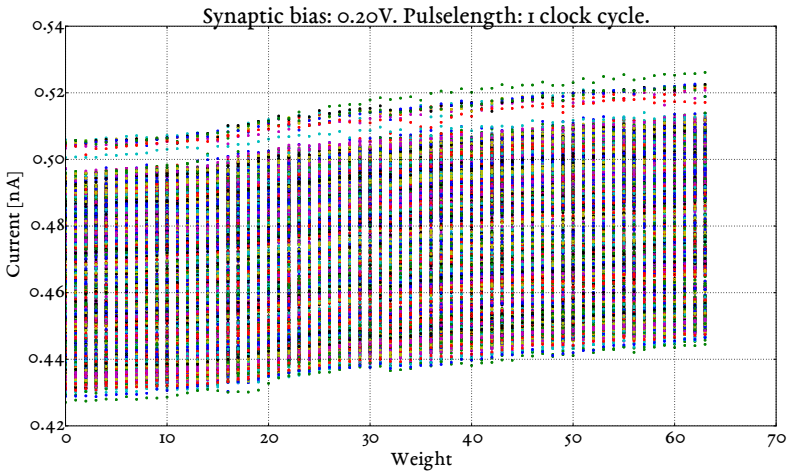

Figure 18: Current-weight curve for all synapses at a bias voltage of $0.20\mathrm{V}$. The offset variation between the synapses is substantially larger than the current variation within their respective curves. All synapses exhibit a monotonous increase in current for larger weights.

because of a temperature dependence of the offset, as measurements during the day yielded offset currents that differed from those taken at night by about the same factor. During the time scale of any individual measurement the room temperature was approximately stable.

The spike interval was shown to be minimal at 43 clock cycles when we would have expected a minimum of around 32 clock cycles that is due to the fact that the serial connection to the chip takes 32 cycles to send one packet. The reason for this discrepancy remains unclear. The clock period is given as $(10.4207 \pm 0.0020)\mathrm{ns}$ which is in good agreement with the set period of $10.42\mathrm{ns}$.

Fig. 14 is provided as a basis for defining the operating range. Choosing the lower boundary is arbitrary, a value of $0.20\mathrm{V}$ was chosen as a preliminary value. Fig. 17 visualizes the linear correlation at this value for all synapses. This heat map together with Fig. 18, where the actual curves for all synapses are plotted, suggests that this indeed a reasonable value for all synapses.

However, it has been pointed out that the small absolute currents at this voltage (around $20\mathrm{pA}$) are too low to be used with the synaptic input amplifier at the neuron. It was also suggested to find an upper boundary for the linear correlation, as it is expected that it also breaks down for large bias voltages. It would have been advisable to measure the offset current before starting the weight-current measurement and after ending it, in order to investigate possible deviations caused by temperature effects. These points will be considered in the Bachelor's thesis subsequent to this work.