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submitted by

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Hardware Design and Reference Current Generation for Neuromorphic Multi-Chip Systems

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Abstract

BrainScaleS-2 Cube systems are neuromorphic development setups with up to two dedicated HICANN chips. This thesis discusses the design of a new hardware platform JABBA, capable of incorporating up to 12 HICANN chips — scaling the BrainScaleS-2 architecture. Shortcomings of the old platform are analyzed and improved upon.

The HICANN chip imposes boundary conditions toward the design of an external reference current source. The current source of the BrainScaleS-2 Cube system is measured toward its compliance. Further, an alternative current source design is evaluated through simulation. Their linear operating ranges as well as sensitivities toward ambient air temperature change are examined.

It was found that both designs meet the given criteria. The selection of a fitting constant current source for JABBA is discussed.

Zusammenfassung

BrainScaleS-2 Cube Systeme sind neuromorphe Entwicklungsplattformen mit bis zu zwei HICANN Chips. Diese Arbeit beschäftigt sich mit dem Design einer neuen Hardwareplattform JABBA, welche bis zu 12 HICANN Chips umfasst und die BrainScaleS-2 Architektur weiter skaliert. Probleme der alten Plattform werden analysiert und behoben.

Der HICANN Chip liefert Randbedingungen bzgl. des Designs einer externen Referenzstromquelle. Die Stromquelle eines BrainScaleS-2 Cube Systems wird durch Messungen auf Kompatibilität geprüft, eine alternative Stromquelle durch Simulation evaluiert. Des Weiteren werden die linearen Parameterbereiche der Stromquellen sowie Abweichungen aufgrund von Variation der Umgebungslufttemperatur charakterisiert.

Als Ergebnis wird festgehalten, dass beide Stromquellen die Anforderungen des HICANN Chips erfüllen. Eine Eignung für JABBA wird diskutiert.

Contents

1 Introduction

As the development of ever-faster conventional computing architectures has slowed in recent years due to the fundamental limitation of downscaling silicon-based transistors beyond a certain size, alternative compute architectures are being developed. One such alternative are capacitor-based hardware neuron systems that are used to explore the governing principles of information processing of biological brains (Monroe 2014).

The spike-based BrainScaleS-2 (BSS-2) neuromorphic architecture, mainly developed at the Kirchhoff Institute for Physics (KIP) in Heidelberg, is based around a neuromorphic application-specific integrated circuit (ASIC) (HICANN) that encompasses 512 mixed-signal neuron circuits along with 512×256 synapses. Neuron and synapse dynamics can be described with the adaptive exponential integrate-and-fire (AdEx) model (Brette et al. 2005) and are accelerated 1000-folds compared to biological time. For internal biasing of the analog circuitry, a constant reference current source is essential. The system setup around the neuromorphic chip consists of a carrier board and field programmable gate array (FPGA) that captures output data and enacts real-time control over the HICANN chip and is thus crucial for its operation (Pehle et al. 2022).

The BSS-2 Cube system is a multichip development platform and includes up to two HICANN chips and four FPGAs. To further increase the neuromorphic chip count, a new hardware platform needs to be developed based on findings from BSS-2 Cube systems.

This thesis deals with the hardware design of an extended and improved system platform JABBA[1], capable of handling up to 12 HICANN chips and 12 FPGAs. Special emphasis is put on the design of the adjustable external constant reference current source. So far, experiments on the BSS-2 platform utilize the internal reference current source of the HICANN chip. Therefore, a need arises to characterize the existing reference current source on BSS-2 Cube systems and validate its performance against boundary conditions imposed by the HICANN chip to design a compliant constant reference current source for JABBA.

[1] Just a Beautiful Bunch of ASICs

2 Theory and Background

2.1 The HICANN Chip

The HICANN ASIC is a neuromorphic chip that is mainly developed at the KIP in Heidelberg as part of the BSS-2 project. Its application is to mimic biological neurons with analog capacitor-based hardware neurons, ultimately allowing the modeling of biological brain function.
A reference input clock signal is needed by the digital I/O of the chip and is redistributed to other digital logic units. For operation, the chip further requires multiple voltage supplies, a voltage reference for its internal analog to digital converter (ADC) and digital processors as well as a reference current source for biasing internal analog processes. Within the HICANN chip, the reference current gets integrated by an internal capacitor that generates a voltage ramp to update analog memory cells in parallel (Hock et al. 2013).

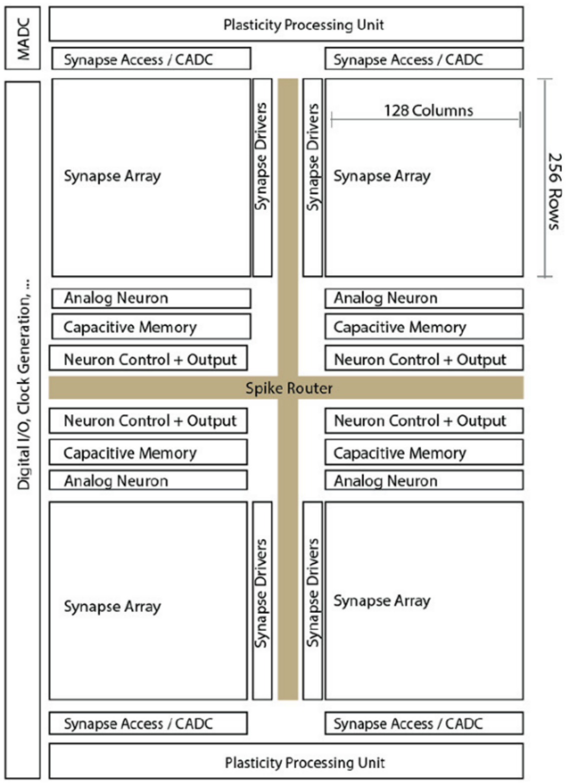

Figure 1: Schematic layout of the HICANN ASIC (Pehle et al. 2022)

FPGAs are used as a low-level interface to configure the chip and build the backbone of every experiment setup.
This thesis puts special emphasis on the design and suitability considerations of constant reference current sources.
An ideal current source has an infinite internal resistance R_i and delivers a constant current,

independent of the connected load.

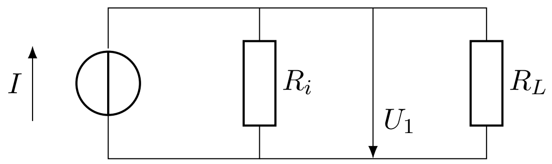

Figure 2: Idealized current source schematic

The voltage across the source is set according to the load resistance in order for the current to remain constant and approaches infinity for open-circuit configuration.

$$U_1 = I \cdot R_L \tag{1}$$

The implementation of a current source in an electric circuit can not deliver arbitrary voltages, as it is limited by its supply voltage. Hence, the current source circuit needs to be designed according to the expected load, in order to operate within a valid range.

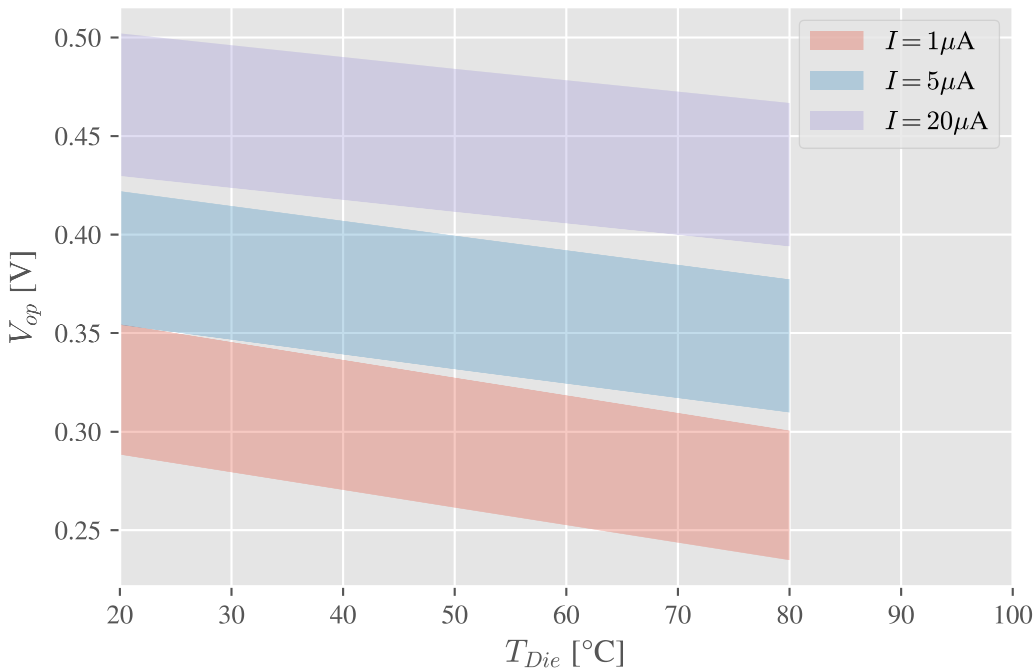

Figure 3: Simulation results of the voltage settling at the external reference input pin of the HICANN chip over all relevant corner variations (Ilmberger 2022)

The HICANN chip shows a decrease in operating voltage (V_{op}) with an increase in die temperature at constant current settings, where the term *operating voltage* refers to the potential of the current source at its output. Over a current range from 1 µA to 20 µA, the minimum and maximum operating voltages are 288 mV and 503 mV respectively over all relevant process corners (see figure 3). These process corners describe the maximum variation that can occur during the fabrication of the ASIC from the wafer substrate and thus cover all operating situations. Under normal operating conditions, the HICANN chip operates at reference currents between 4.1 µA and 9.4 µA. The obtained operating ranges impose boundary conditions that are used to design and validate suitable constant current reference circuits.

2.2 BrainScaleS-2 Cube Systems

BSS-2 Cube systems are highly configurable setups, consisting of up to four FPGAs and two neuromorphic HICANN chips. FPGAs are power-cycled through an UCD9246 (Texas Instruments 2010) power management chip via USB. Due to stability and usability issues of this method, recent efforts shifted toward a network enabled Raspberry Pi based system controller (Stucke 2022b).

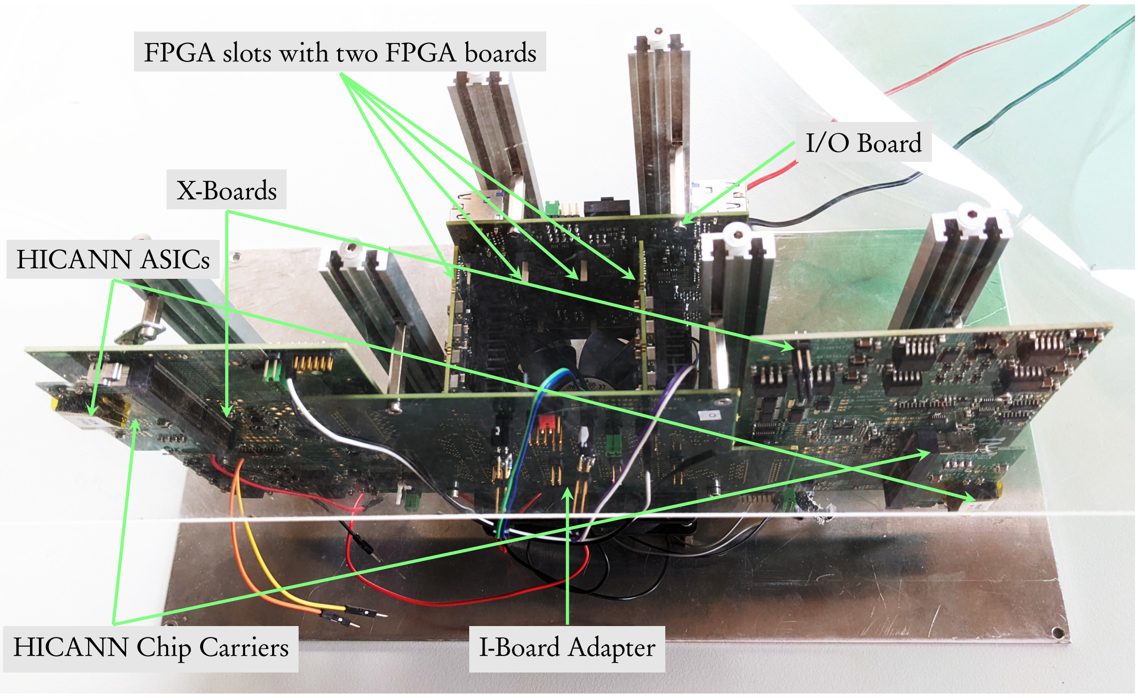

Figure 4: BSS-2 Cube setup with two fitted FPGAs

JABBA aims to replace the X-Boards and I-Board adapter of BSS-2 Cube systems (see figure 4) with a single board, in order to simplify assembly, reduce interconnects between components and ultimately enable scaling.

One issue with the FPGA boards are *stuck bus conditions*, occurring when an I^2C slave continuously pulls the SDA line low - rendering further communication to any I^2C device impossible. Due to the layout of the communication layer, identifying the rogue device or performing a manual reset is not possible. This issue is addressed in the design of JABBA (see section 3.7).

2.3 Printed Circuit Boards

Printed Circuit Boards (PCBs) are arrangements of conductive and non-conductive material layers. They provide a mounting fixture for surface-mounted devices (SMDs) and through-hole technology (THT) devices as well as electric circuitry through dedicated copper structures.

The simplest PCBs consist of a one layer stackup. A single layer is used to provide the required electrical connections between all components. The next evolutionary step is a two layer stackup. The top layer is used to place components and route needed power and signal traces. The bottom layer may consist of a solid copper pour connected to ground (ground plane). Electrical connections between layers are established through copper plated holes (vias), a type of plated through holes (PTHs). The separate ground plane reduces the routing complexity as well as stray capacitance, as ground connections can be established everywhere on the board through vias — avoiding the need of long ground traces. Mechanical connections, such as mounting holes, can be realized by non-plated through holes (NPTHs).

For more complex PCB designs, a higher layer count yields less interference and more routing flexibility through the further abstraction of signal and power planes. Large copper pours on the power planes reduce stray capacitances, increase current carrying capacities and improve thermal performance.

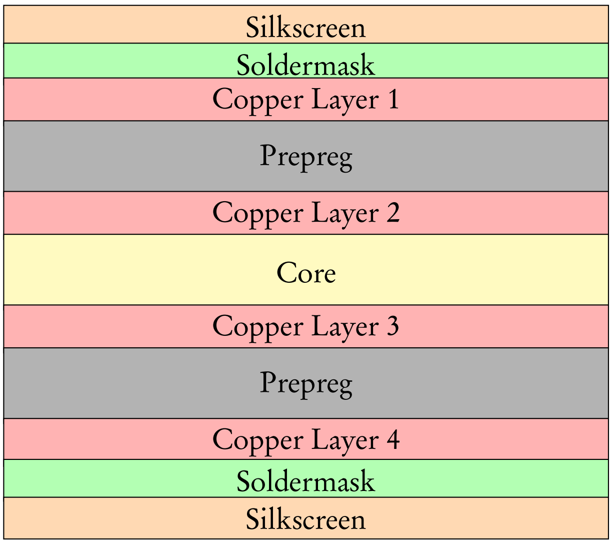

Figure 5: Typical four layer stackup PCB

Non-conductive layers (*prepreg* and *core*) are placed between copper layers for electrical isolation (see figure 5). These isolation layers are usually manufactured from fiber glass materials, adding to the durability of the PCB. A *soldermask* is applied on both sides of the PCB, isolating copper traces but leaving SMD pads and THT holes uncovered. This layer gives the board its usually green color.

The *silkscreen* is used to convey important information, such as component identification and orientation, serial numbers, etc.

3 JABBA Hardware Design

3.1 System Layout

JABBA features 12 HICANN chip carrier and 12 FPGA slots. To reduce noise in the controlled impedance signal (CIS) lines on the top and bottom layers and to provide enough routing flexibility, a six layer PCB design with two inner power/ground plane pairs was chosen and designed with KiCad EDA (KiCad Development Team 2021).

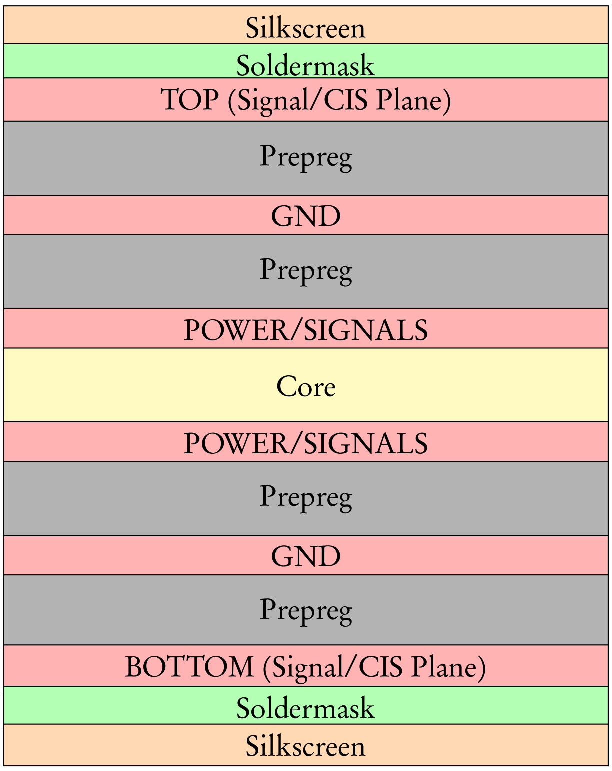

Figure 6: JABBA stackup

The top and bottom layers are used for signal routing and component placement. The inner two layers are dedicated power planes, shielded by adjacent ground planes. This layout ensures that the signal layers are isolated from any electro-magnetic interference (EMI) from the power planes.

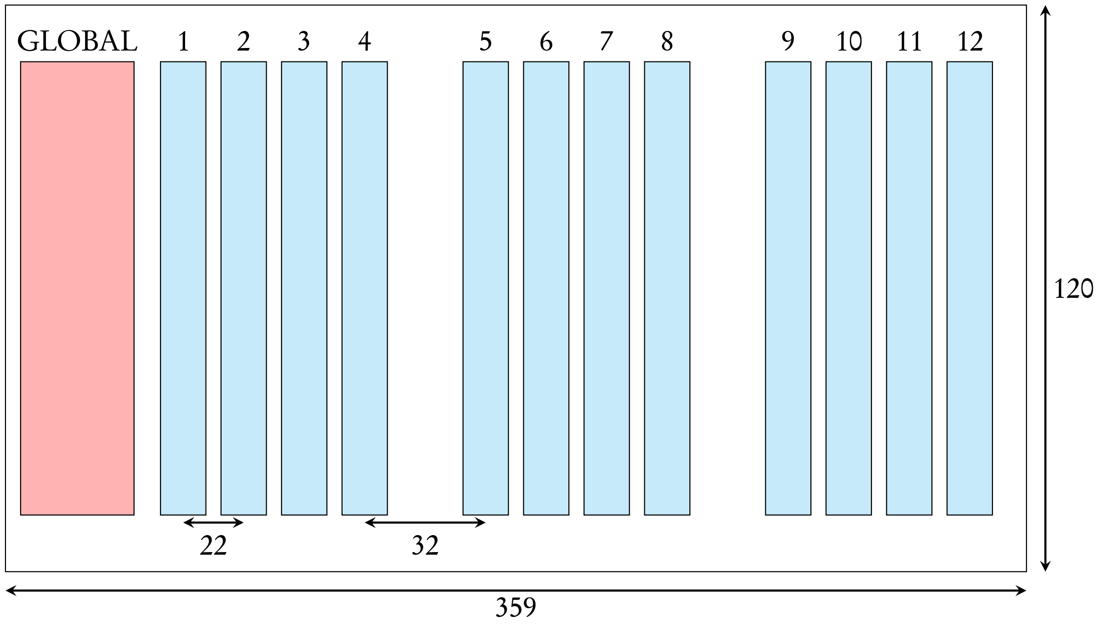

Figure 7: PCB schematic footprint (dimensions in millimeters)
global circuitry (red), HICANN/FPGA slots (blue)

The board outline, mounting points and slot placements are compatible with existing FPGA- and IO-boards. The top layer of the PCB features 12 HICANN chip carrier slots, 12 FPGA slots are present on the bottom layer. Each HICANN/FPGA pair (HFP) forms a local hardware unit with adjacent components, arranged in three clusters consisting of four HFPs each. KiCad schematics were arranged using hierarchical layouts in such a way that the layout of one HFP can be duplicated with *Kicad Action Plugins* (Nemec 2022).

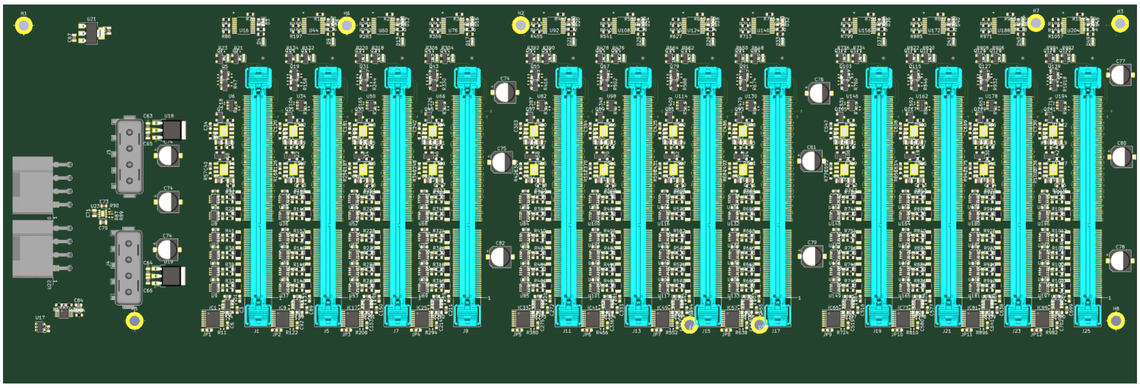

Figure 8: PCB layout topside

3.2 Power Supplies

Two 8-pin peripheral component interconnect express (PCI-E) power connectors provide a 12 V power rail to the FPGAs as well as stepped down analog and digital 3.3 V chip supply rails. The connectors are capable of delivering a total current of up to 54 A (648 W at 12 V).

Two Mate-n-Lok connectors, also known as *Molex connectors*, provide an auxiliary 12 V rail as well as a 5 V rail used to generate the various HICANN supply rails. Each rail can deliver currents of up to 24 A (288 W/120 W at 12 V/5 V).

This connector choice enables standard computer power supplies to be used as a power source.

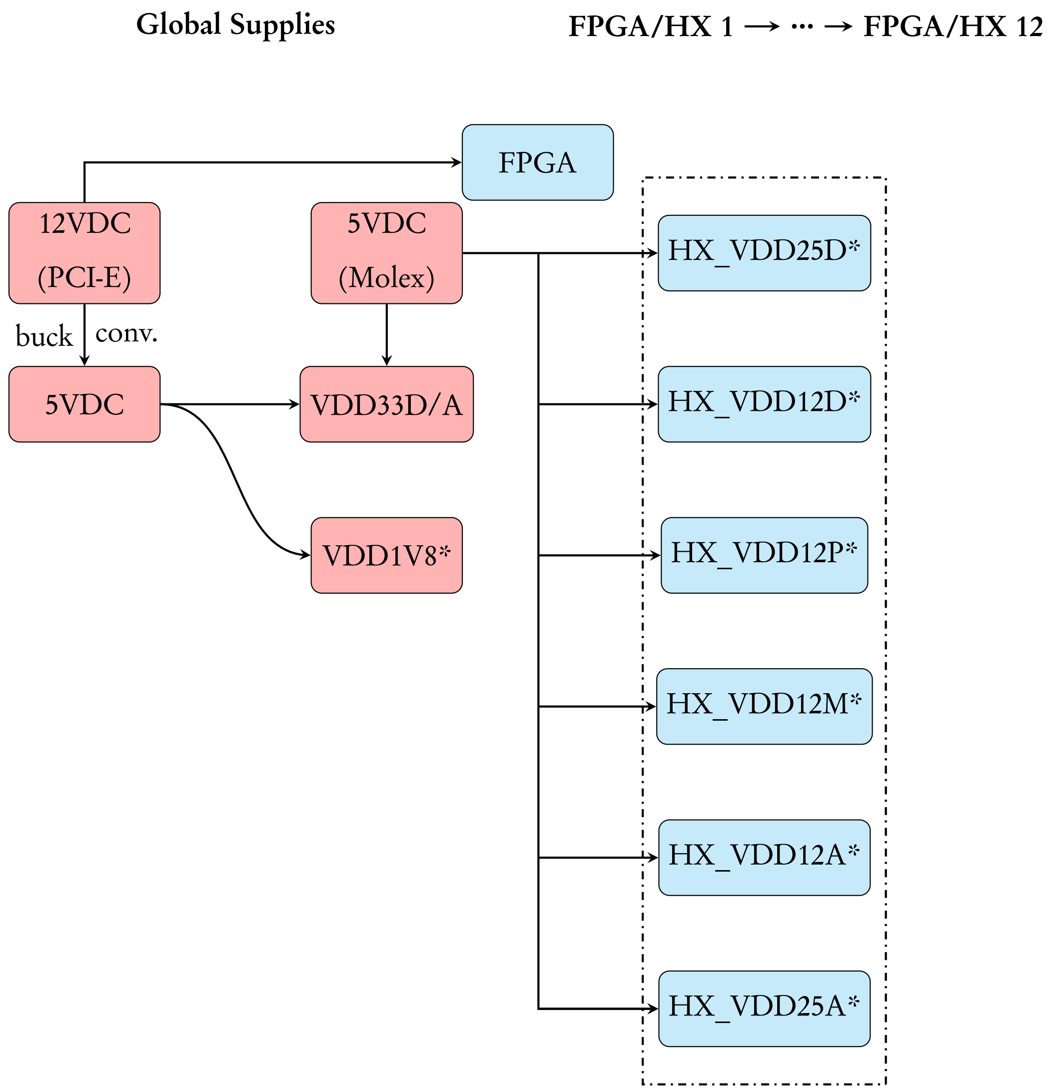

Figure 9: Power supply layout (* current/voltage monitored)

The HICANN chip is supplied with two 2.5 V and four 1.2 V rails (see figure 9). Digital and analog supplies are separated to manage current return paths and to prevent noise from digital signals on analog rails.

Rail	I_{typ} [mA]
HX_VDD12D	190
HX_VDD12A	16
HX_VDD12M	2
HX_VDD12P	8
HX_VDD25D	94
HX_VDD25A	81

Table 1: HICANN supply rails typical currents (Stradmann 2022)

Linear voltage regulators show a very stable line regulation when compared to buck converters, as they do not feature an internal AC switching signal that can propagate to the voltage output and do not need any EMI shielding. With the typical current levels and voltages of the HICANN rails (see table 1), the lower efficiency of linear regulators can be neglected. The rail voltages and currents are individually monitored through a shunt circuit for every HICANN chip (see section 3.3).

3.2.1 HICANN Rails

The HICANN power rails are supplied by a series of linear low-dropout regulators (LDOs) built around the AP7173 (Diodes Inc. 2011) 1.5 A regulator. Its maximum current output of 1.5 A is well above the maximum current expected on any HICANN rail, ensuring good thermal performance (see table 1).

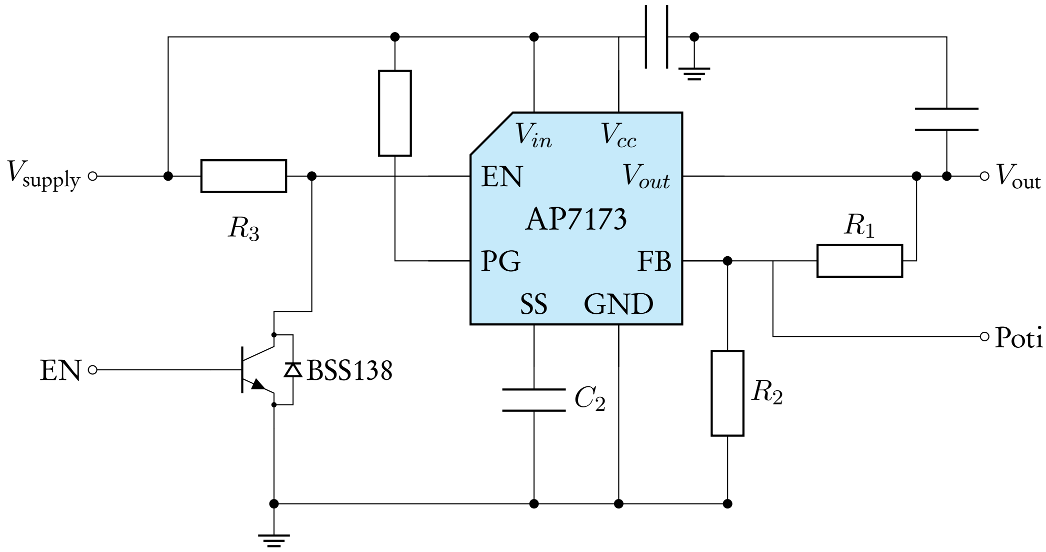

Figure 10: Simplified schematic of a HICANN LDO supply

The output of a power rail is enabled through a BSS138 (Onsemi 2021) n-channel mosfet that is controlled through an I^2C port expander. It pulls the enable pin of the regulator high through the resistor R_3, once its gate is charged.

The allowable output voltage range is set with a voltage divider circuit consisting of R_1 and R_2 with respect to the internal reference voltage $V_{\text{ref}} = 0.8\,\text{V}$ of the regulator. The exact output voltage

$$V_{\text{out}} = V_{\text{ref}} \cdot \left(1 + \frac{R_1}{R_2 + R_{\text{poti}}}\right) \tag{2}$$

is then set through a $10\,\text{k}\Omega$ AD5252 (Analog Devices 2012) digital potentiometer.

A soft start capacitor C_2 limits the initial current surge by slowly ramping up the output voltage to its designated value. With a typical soft start pin current $I_{\text{ss}} = 440\,\text{nA}$ and a capacitor value of $C_2 = 10\,\text{nF}$, the start time computes to

$$t_{\text{ss}} = \frac{V_{\text{ref}} \cdot C_2}{I_{\text{ss}}} = 18.2\,\text{ms}. \tag{3}$$

3.3 Power Monitoring

To monitor the power consumption of every power rail of every HICANN chip in the system, each rail is directly measured by utilizing a shunt resistor and an INA219 Current/Power Monitor (Texas Instruments 2015a). In the following, the measuring setup is characterized for one arbitrary power rail.

The INA chip can be addressed and configured through an I^2C interface. It measures the voltage drop across the shunt resistor R_3 as well as the bus voltage at IN- with respect to ground. With R_3 being a known resistance, the load current as well as the load power can be monitored.

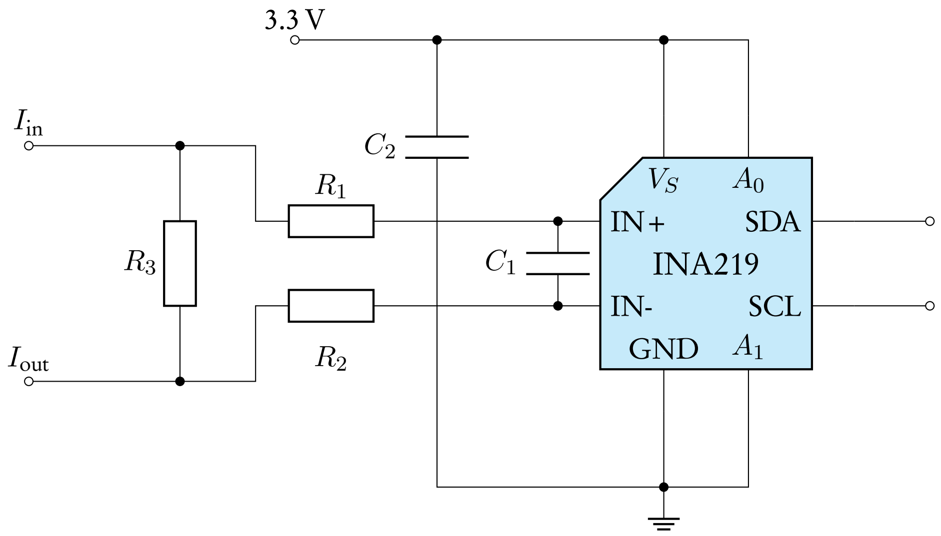

Figure 11: Current Measurement Schematic

3.3.1 Selecting Shunt Resistor

The voltage drop across the shunt resistor R_3 depends directly on the load current as well as the resistance value.

$$V_{R_3} = R_3 \cdot I_{\text{load}} \tag{4}$$

Depending on what resistor value is selected and what shunt voltage range and ADC resolution is programmed, the current measurement resolution can be computed as follows.

$$I_{\text{LSB}} = \frac{V_{\text{range}}^{\text{shunt}}}{\text{Res}_{\text{ADC}}^{\text{INA}} \cdot R_3} \tag{5}$$

Bit 12	Bit 11	Range[mV] (LSB = 10 µV)
0	0	±40
0	1	±80
1	0	±160
1	1	±320

Table 2: Possible shunt voltage range configurations INA219

The configured bus voltage range (either 16 V or 32 V, with LSB = 4 mV) and INA ADC register resolution determine the bus voltage resolution

$$V_{\text{LSB}}^{\text{Bus}} = \frac{V_{\text{range}}^{\text{Bus}}}{\text{Res}_{\text{ADC}}^{\text{INA}}} \tag{6}$$

and the power measurement resolution

$$P_{\mathrm{LSB}} = \mathrm{I}_{\mathrm{LSB}} \cdot \mathrm{V}_{\mathrm{LSB}}^{\mathrm{Bus}}. \tag{7}$$

With a configured ADC resolution of 12 bit, a voltage bus range of 16 V and with regards to the maximum current levels expected on each HICANN rail (see table 1), the following parameters were selected.

Rail	R_3 [Ω]	$V_{\mathrm{range}}^{\mathrm{shunt}}$[mV]	$I_{\max}$ [A]	I_{LSB} [µA]	P_{LSB} [µW]
HX_VDD*D	0.04	±40	1	244.10(6)	1.00(1)
HX_VDD*A/M/P	0.1	±40	0.4	97.70(3)	0.40(1)

Table 3: Power measurement parameters and resolutions

3.4 PLL Input Clock

The FPGA provides a low-voltage differential signal (LVDS) clock signal at 50 MHz that is routed to the single-ended clock input of the HICANN chip through a SN65LVDS2DBV (Texas Instruments 2014) high-speed differential line driver. This clock input is needed for digital processing units within the ASIC. The mentioned integrated circuit (IC) was chosen for its high throughput capabilities (up to 400 Mbit s^{-1} for receivers at 100 Ω loads) and low EMI emissions.

3.5 Reference Current Source Option A

This reference current source circuit design is based on the Texas Instruments Precision Design SLAU507 (Kay 2013) with an OPX333 operational amplifier (Texas Instruments 2015b) and an INA 326 instrumentation amplifier (Texas Instruments 2004) as main components. The circuit delivers a low level reference current I_{ref} to any given load, based on a reference voltage V_{ref} that is supplied by a dedicated digital to analog converter (DAC) (Texas Instruments 2003). In order to ensure a low drift of the DAC output voltages, the voltage reference of the DAC is set at 2.5 V through a low drift voltage reference IC (Linear Technology 2000).

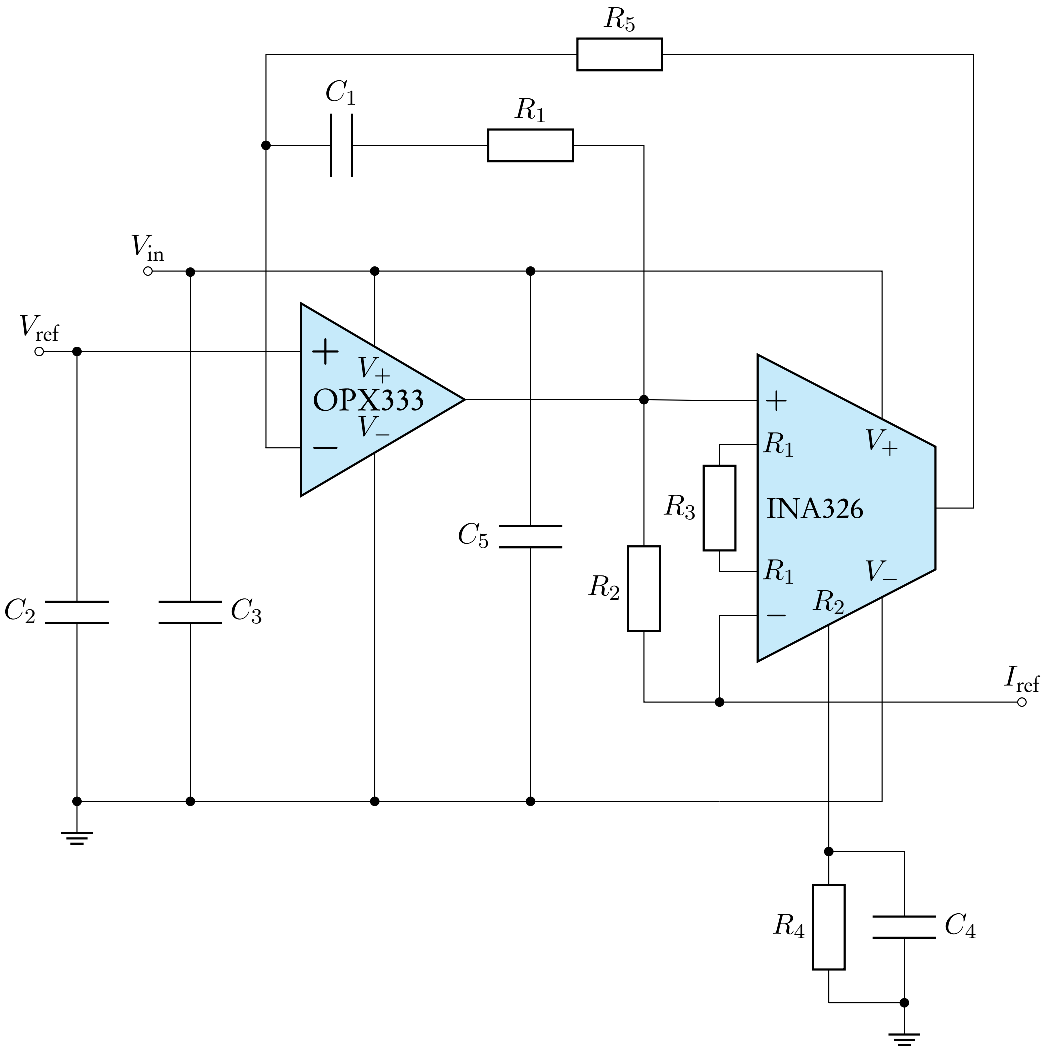

Figure 12: Reference Current Source Option A Schematic

The reference current can be computed by utilizing Ohm's law and the inverse proportionality to the gain G_{INA} of the INA326.

$$I_{\text{ref}} = \frac{V_{\text{ref}}}{G_{\text{INA}} \cdot R_2} \quad \text{with } G_{\text{INA}} = 2 \cdot \frac{R_4}{R_3} \tag{8}$$

3.5.1 Selecting the INA gain

The INA gain directly sets the maximum voltage across R_2. It is beneficial to keep this voltage as low as feasible, as it limits the maximum load voltage. However, a high gain value can be detrimental to the circuit stability.

$$V_{\text{load}}^{\text{max}} = V_{\text{in}} - V_{R_2}^{\text{max}} \text{ with } V_{R_2}^{\text{max}} = V_{\text{ref}}^{\text{max}}/G_{\text{INA}}. \tag{9}$$

To avoid non-linear behaviour with low resistive loads, low output currents and to guarantee stability, a medium gain $G_{\text{INA}} = 2$ with $R_3 = R_4 = 200\,\text{k}\Omega$ is chosen for best performance across the whole output current range. This results in a maximum load voltage of $V_{\text{load}}^{\text{max}} = 2.05\,\text{V}$ with $V_{\text{in}} = 3.3\,\text{V}$ and $V_{\text{ref}}^{\text{max}} = 2.5\,\text{V}$ (see equation 9).

3.5.2 Selecting the reference current range

R_2 is used to set the reference current range (see equation 8). Based on the simulation results of the HICANN chip (see figure 3), a reference current range of 20 µA is chosen. This computes to a value of $R_2 = 62.5\,\text{k}\Omega$ (see equation 8), where 62 kΩ was chosen for R_2 as the closest available E24 resistor value.

It is important to note that a high precision resistor must be used for R_2, as any deviation will impact the reference current range and will require additional calibration. A low thermal coefficient of the resistor ensures high temperature stability of the current source.

3.5.3 Component Selection

Auxiliary components, such as decoupling capacitors and frequency filters, are selected based on the recommendations of the respective data-sheets of the OPX333 and INA326 amplifiers.

Component	Value
OPX333	$V_{-} = 0\,\text{V}$, $V_{+} = V_{in} = 3.3\,\text{V}$
INA326	
R_1,R_5	100 kΩ
R_2	62 kΩ | E24 ± 0.1 %
R_3	200 kΩ
R_4	200 kΩ
C_1	10 nF
C_2	10 µF
C_3,C_5	100 nF
C_4	500 pF

Table 4: Reference Current Source Component Selection

3.6 Reference Current Source Option B

This reference current source is build around the TLV4333 (Texas Instruments 2015c) operational amplifier and PMV65XP (Nexperia 2013) p-channel mosfet and is present on BSS-2 Cube systems. Its voltage reference V_{ref} is supplied by a dedicated 12 bit DAC. To compensate voltage drifts of the current source supply rail, the voltage reference of the DAC is configured to be the input voltage V_{in} of the current source.

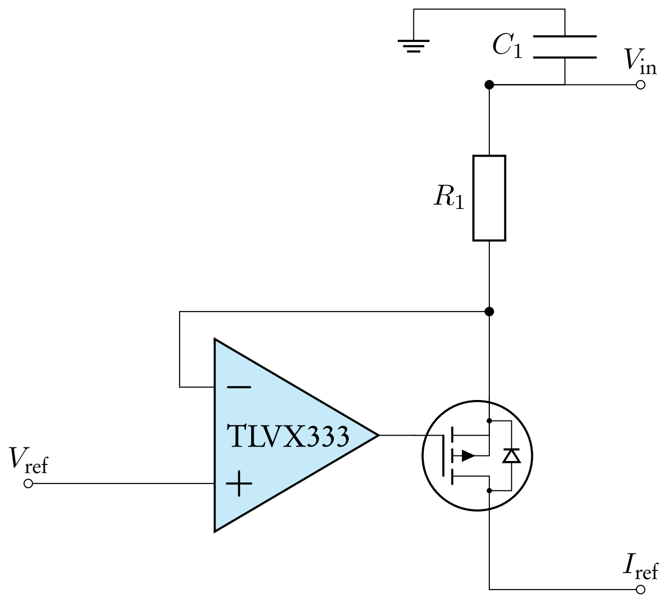

Figure 13: Reference Current Source Option B Schematic

The operational amplifier is configured with a closed feedback loop. The theoretical maximum current is given by the resistor R_1, the input voltage V_{in} and operating voltage V_{op}.

$$I_{\max} = \frac{V_{\text{in}} - V_{\text{op}}}{R_1} \tag{10}$$

The output of the operational amplifier sets the gate potential of the mosfet according to the non-inverting input V_{ref} as well as the voltage drop across the resistor R_1 on the inverting input.

$$V_{\text{out}} = (V_{\text{ref}} - (V_{\text{in}} - I \cdot R_1)) \cdot A_{\text{OL}} \text{ with } I = I\left(U_{\text{gs}}, V_{\text{in}}, R_1\right) \tag{11}$$

The gate-source voltage of the mosfet can then be expressed as follows.

$$U_{\text{gs}} = V_{\text{out}} - (V_{\text{in}} - I \cdot R_1) \tag{12}$$

With $V_{\text{in}} = 2.5\,\text{V}$ and $V_{\text{ref}} = 2.5\,\text{V}$, the gate-source voltage of the mosfet is regulated in such a way that the voltage drop across R_1 equals $V_{\text{in}} - V_{\text{ref}}$. Hence, the source current is zero. The mosfet operates in a weak-inversion mode, thus the conductance characteristics highly depend on the offset of the gate-source voltage to the threshold voltage. If the reference voltage is now decreased, the mosfet starts to conduct a lineraly increasing amount of current until a point is reached, where the amplifier output is limited by its ground rail or the reference voltage falls below the operating point — resulting in a stagnating current output. It has to be noted that the valid voltage reference range is limited by the common-mode voltage range of the amplifier. For values approaching either supply rail, non-linear behaviour is expected.

3.6.1 Selecting the Reference Current Range

Based on the simulation results of the HICANN chip (see figure 3), a reference current range of 20 µA is chosen. The reference current source is configured with an input voltage of $V_{\text{in}} = 2.5\,\text{V}$. This computes to a resistance value of 125 kΩ, where $R_1 = 124\,\text{k}\Omega$ was chosen as the closest resistor value in the E96 series.

The following components were selected for the circuit.

Component	Value
TLV4333	$V_- = 0\,\text{V}$, $V_+ = V_{\text{in}}$
PMV65XP	$-0.9\,\text{V} < U_{\text{gs}} < -0.47\,\text{V}$
R_1	124 kΩ - E96 ± 0.1 %
C_1	100 nF

Table 5: Selected components for reference current source Option B

The performance of the two different current source designs is evaluated in section 5. A selection is discussed in section 6.

3.7 Communication Interface

JABBA is designed to be user friendly and remotely configurable through a network enabled Raspberry Pi (RPi) system controller using TCP. The RPi interfaces the global I^2C level of the system and provides a Joint Test Action Group (JTAG) interface to the FPGAs, enabling their configuration through a dedicated Xilinx Virtual Cable (XVC) network server (Stucke 2022b). A port expander is employed to control n-channel mosfets that are used to toggle each HICANN LDO. Their voltage output can be set through digital potentiometers in a predefined range around their target output (see section 3.2).

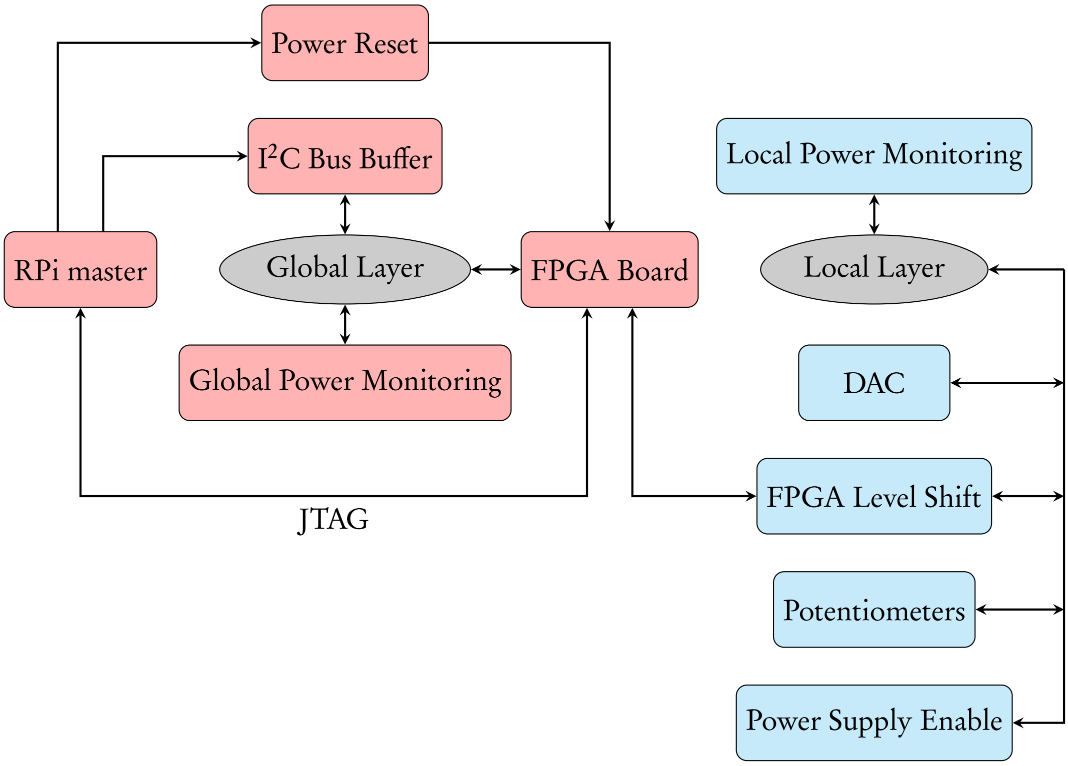

Figure 14: Communications layer JABBA

The FPGA boards occasionally show unexpected behaviour by having a *stuck* I^2C bus. An I^2C bus buffer (Linear Technology 2005) is able to recover such *stuck bus* situations, where an I^2C slave continously pulls the SDA line low, by generating 16 consecutive pulses on the clock line - driving both lines high and freeing the bus. A port expander is used to create a redundant I^2C line to the power resets of each FPGA cluster, enabling a manual power reset of the FPGAs — even when the global I^2C layer is non-functional due to a *stuck bus* condition.

FPGAs receive their unique IPv4 address, used for network access via the I/O board, through four separate bistate identifier pins per slot. Two socket-id pins enumerate the HFP clusters, two edge-id pins the position within the cluster (see also section 3.1).

4 Validation Methods

4.1 Reference Current Source Option A

The reference current source circuit outlined in section 3.5 was not physically tested due to the short time frame of this thesis. Instead, the circuit was simulated using LTspice (Analog Devices 2022) and the respective PSpice models of the employed operational and instrumentation amplifiers (Texas Instruments 2018; Texas Instruments 2017) according to figure 12. The simulation of the DAC was omitted. As a substitute, the reference voltage was provided by an ideal voltage source, in order to study the unskewed performance of the current source design.

Parameter	Range	Increment
T_{amb}	10 °C - 40 °C	5 °C
V_{ref}	0 V - 2.5 V	50 mV
V_{op}	0 V - 3.3 V	100 mV

Table 6: Simulation parameters for Option A validation

To obtain comparable output current levels to the alternative current source that is already present on BSS-2 Cube systems, a current limiting resistor with a value of 150kΩ was chosen for the simulation. To simulate the operation point of the HICANN, the potential of the current output was swept along the V_{op} range. Output current was measured across the current limiting resistor R_2.

4.2 Reference Current Source Option B

The reference current source circuit outlined in section 3.6 is present on BSS-2 Cube systems and is thus measured on this platform. R_1 is configured with a value of 300kΩ $\pm 1\%$.
To characterize the current source and its behaviour under ambient temperature variation, the setup is placed inside a Binder-MK53 (Binder GmbH 2012) climate chamber. Temperature settings are automated using the available RS-485 interface and BinderControl software (Stucke 2022a). A Keithley 2635B (Tektronix 2013a) source measure unit (SMU) was used to set the operating voltage and measure the current at the output.

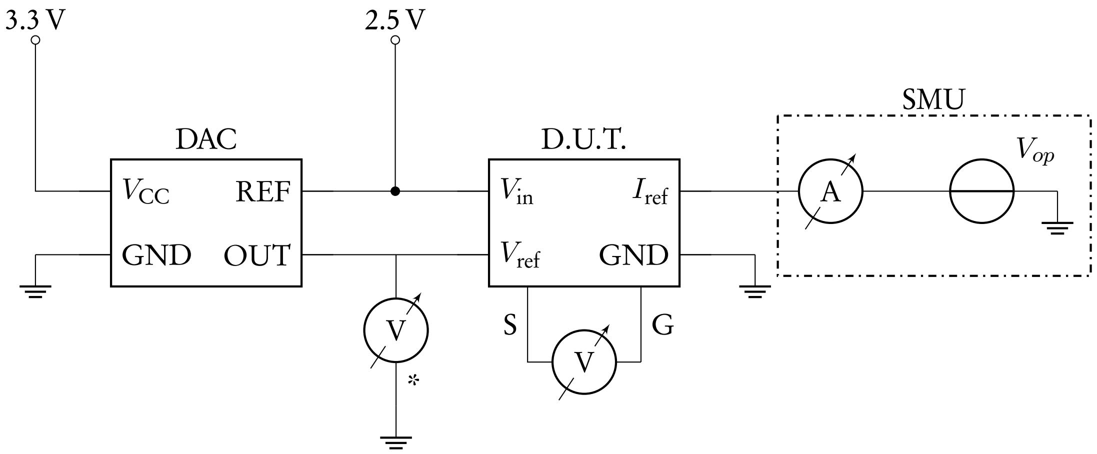

Figure 15: SMU measuring setup with current source as D.U.T.
Mosfet: Gate (G), Source (S)
(* indicates separate measurement run for DAC calibration)

To measure the gate-source voltage of the mosfet and the output voltage of the DAC, a Keithley 2100 (Tektronix 2013b) multimeter was used. Reading out the meters and setting the operation voltage is fully automated with labcontrol (F9 n.d.).

Parameter	Range	Increment
T_{amb}	10 °C - 40 °C	5 °C
V_{ref}	0 V - 2.5 V	125 mV
V_{op}	0 V - 1.9 V	38 mV

Table 7: Measurement parameters for Option B validation - for each measured value, the average of 20 samples is taken.

The operating voltage range is swept for every given voltage reference. This is repeated for all temperature settings.
When the climate chamber reaches the desired target temperature, a 20 minute delay before measurement commencement ensures that a stable equilibrium is reached. It is important to note that given temperature values refer to ambient temperatures, as component junction temperatures will be considerably higher.
Reference voltages were set by adjusting the DAC setting utilizing Coordinate Systems for BrainScaleS architectures (HALCO).

Additionally, the output characteristics for single ($V_{-} = 0\,\mathrm{V}$) and dual supply ($V_{-} = -2.5\,\mathrm{V}$) operation were simulated using LTspice and the respective PSpice models of the amplifier and mosfet (Texas Instruments 2016; Nexperia 2012).

Parameter	Range	Increment
V_{ref}	0 V - 2.5 V	100 mV
$T_{\mathrm{amb}} = 25\,^{\circ}\mathrm{C}$		
$V_{\mathrm{op}} = 0\,\mathrm{V}$		

Table 8: Simulation parameters for single and dual supply configuration of the amplifier

5 Results

In this chapter, the results of the constant current source analyses are presented according to the configurations and validation methods outlined in sections 3.5 through 3.6 as well as sections 4.1 through 4.2.

5.1 Reference Current Source Option A

The used PSpice models, provided by Texas Instruments (TI), showed good convergence behaviour in the configuration outlined in section 3.5 and 4.1.

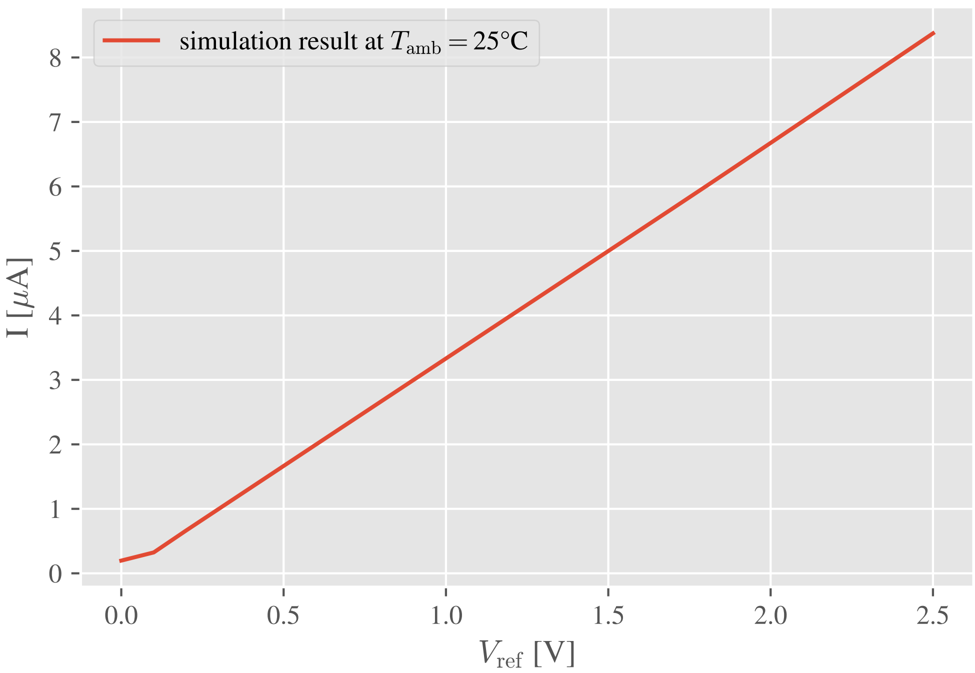

Figure 16: Simulation results for reference voltage sweep with $V_{\mathrm{op}} = 0.53\,\mathrm{V}$ at ambient temperature of 25 °C

A linear output current relation with respect to the voltage reference was observed for reference voltages above the common-voltage input range limit (see figure 16). Due to the 3.3V rail voltage of the amplifiers, a maximum voltage reference value of 2.5V is well within a valid input range.

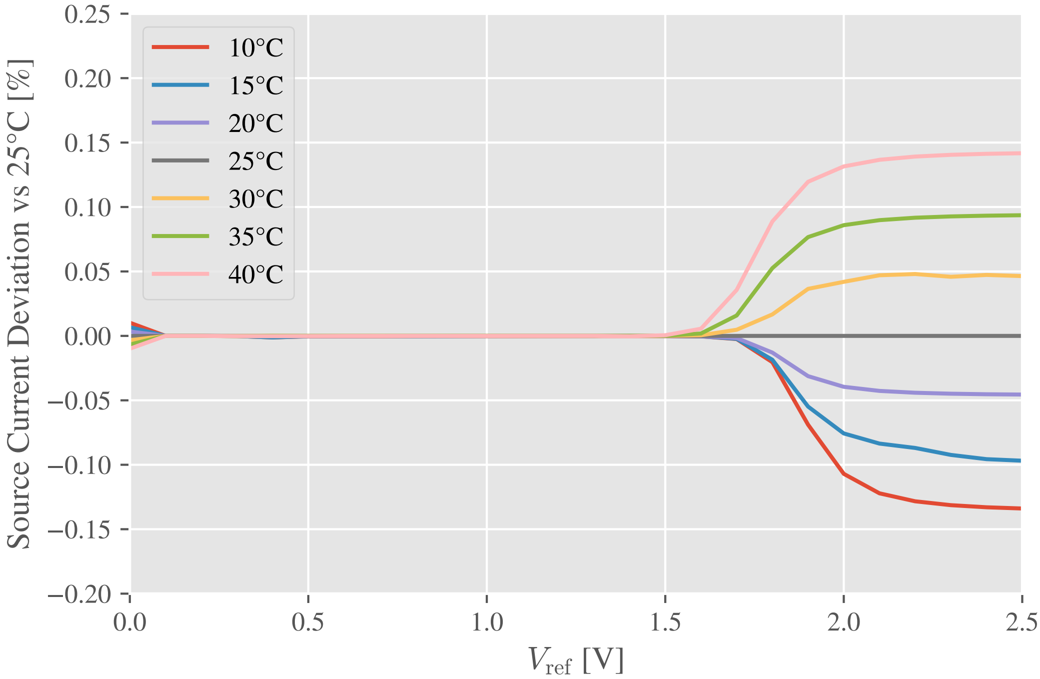

Figure 17: Temperature dependent deviation of source current as a function of V_{ref} at $V_{\mathrm{op}} = 0.5$ V — normalized to 25 °C

Deviations based upon ambient air temperature variation in the range from 10 °C to 40 °C were observed to be below 0.15 % throughout the linear input range compared to a 25 °C reference sweep (see figure 17). This corresponds to a maximum current offset across the selected temperature range of 60 nA with output currents of up to 20 µA. Reference voltages below 1.5 V show a negligible amount of temperature drift.

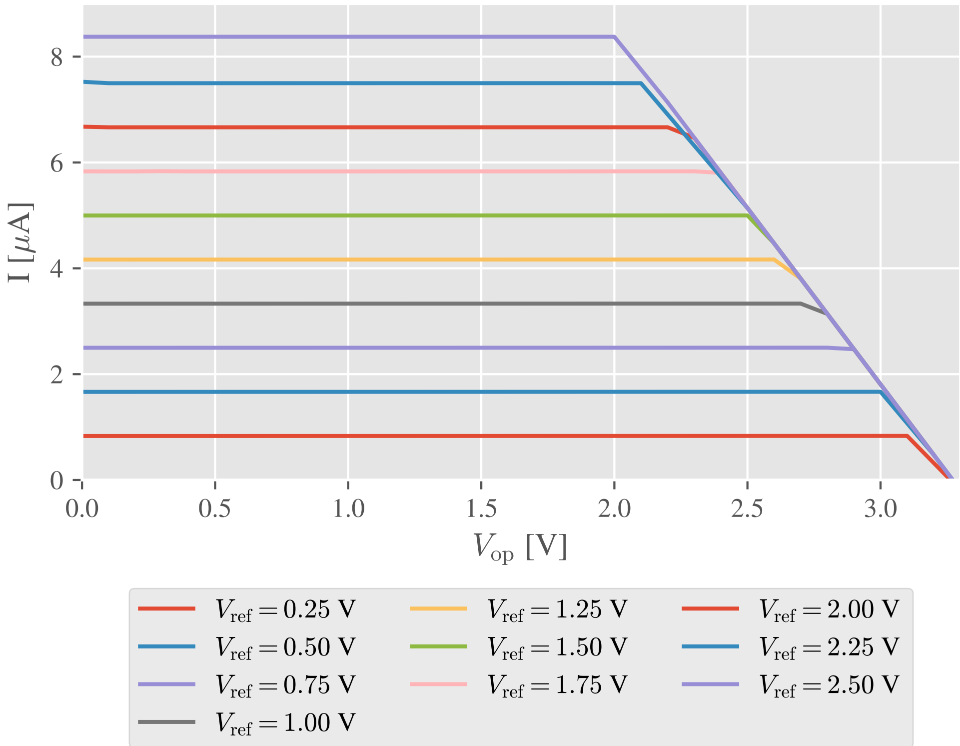

Figure 18: V_{op} sweep at $T_{amb} = 25\,°C$

For operating points of up to 2V, the output current was observed to be constant for voltage reference values up to 2.5V (see figure 18). Based on the 3.3V rail supply of the amplifiers, a constant current output range is expected for operating points up to 2.05V (see equation 9). A shift of the constant operation ranges due to ambient air temperature variation was not observed in the simulation.

It can thus be concluded that the tested constant current source operates as required under the following parameter configuration.

Parameter	Linear Range
V_{ref}	0.1 V - 2.5 V
	0.1 V - 1.5 V (higher temperature stability)
V_{ref}	0.1 V - 1.5 V
V_{op}	0 V - 2 V
T_{amb}	10 °C - 40 °C

Table 9: Stable operating parameter ranges for reference current source Option A

5.2 Reference Current Source Option B

5.2.1 DAC Calibration

The output voltage of the 12 bit DAC supplying V_{ref} to the operational amplifier is set by two 8 bit registers. To establish a relationship between this register value and the actual output voltage, a calibration measurement was conducted.

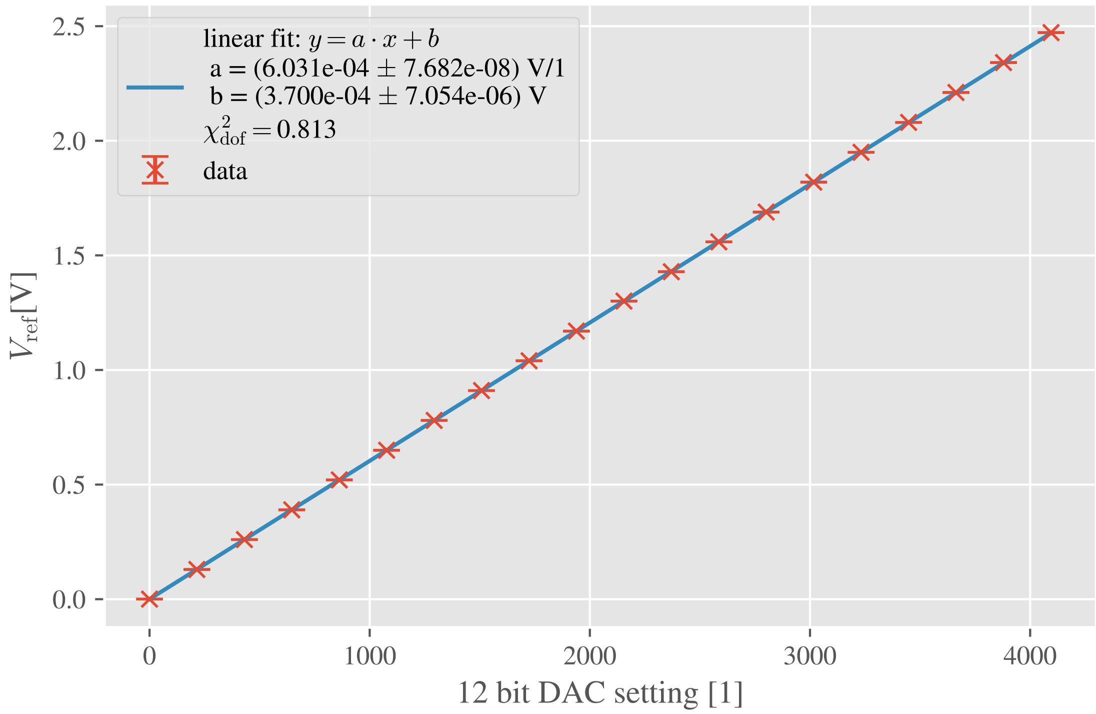

Figure 19: DAC calibration sweep at $T_{amb} = 25\,°C$

As can be seen in figure 19, the output characteristic of the DAC is linear with a negligible offset and gain error. The obtained values allow to convert between register and voltage values.

5.2.2 Performance and Temperature Dependency

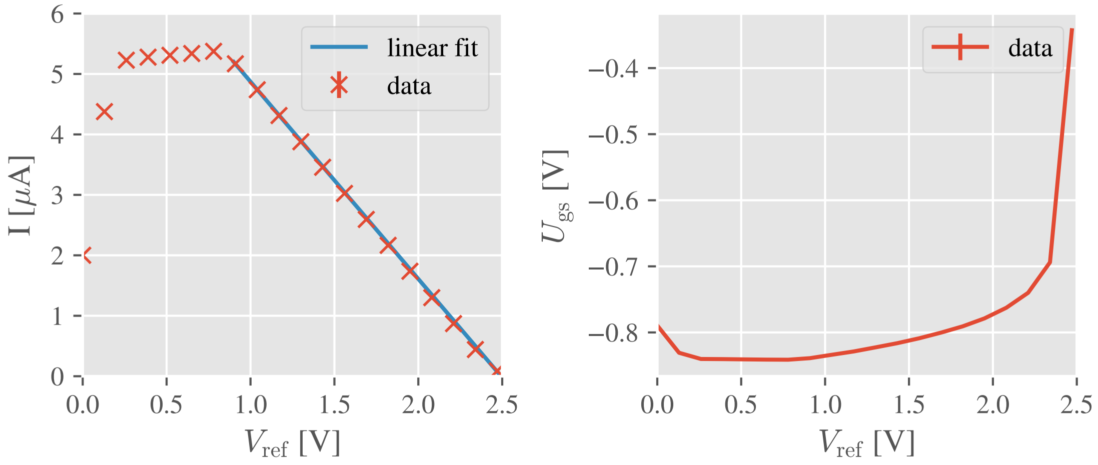

Figure 20: Reference voltage sweep at $V_{\mathrm{op}} = 0.53\,\mathrm{V}$ and $T_{\mathrm{amb}} = 25\,°\mathrm{C}$
Source Current vs V_{ref} (l) U_{gs} vs V_{ref} (r)
The linear fit with the fit function $y = a \cdot x + b$ yielded the parameters
$a = -3.263\,(11)\,\frac{\mu\mathrm{A}}{\mathrm{V}}$, $b = 8.136\,(18)\,\mu\mathrm{A}$ with $\chi^2_{\mathrm{dof}} = 0.45$

As can be seen in figure 20, linear behaviour is only observed for reference voltages above 0.9V. Two phenomena contribute to this behaviour. First, the maximum current is intrinsically limited by V_{op} (see equation 10). This rules out any regulating behaviour for reference voltages with $V_{\mathrm{ref}} < V_{\mathrm{op}}$. Second, the single supply configuration of the amplifier limits the settable gate-source voltage of the mosfet.

With a fitted resistor $R_1 = 300\,\mathrm{k\Omega}$, an operating point of $V_{\mathrm{op}} = 0.53\,\mathrm{V}$ and an input voltage of $V_{\mathrm{in}} = 2.5\,\mathrm{V}$ (see figure 13), one would expect a maximum source current of $\frac{V_{\mathrm{in}} - V_{\mathrm{op}}}{R_1} = 6.6\,\mu\mathrm{A}$. However, figure 20 indicates a maximum current of 5.5 µA. This deviation is due to the inability of the operational amplifier to output voltages below its ground rail and thus limiting the conductance of the mosfet.

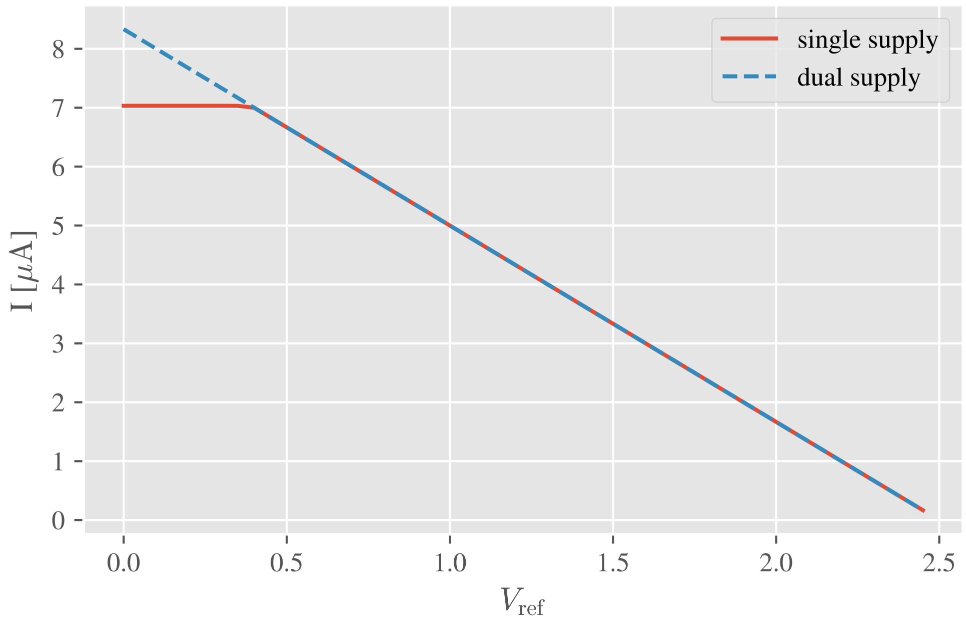

Figure 21: Simulation of single ($V_- = 0\,\text{V}$, $V_+ = 2.5\,\text{V}$) and dual supply ($V_- = -2.5\,\text{V}$, $V_+ = 2.5\,\text{V}$) configuration of the operational amplifier at $V_{\text{op}} = 0\,\text{V}$

As can be seen in figure 21, a single supply configuration of the amplifier limits the maximum output current. This is due to the amplifier being unable to set the required gate-source voltage of the mosfet for maximum current. The simulation result differs from the behaviour seen in figure 20, as not all mosfets are created equal and fabrication variations significantly affect the conductance behaviour — especially in sub-threshold operation.

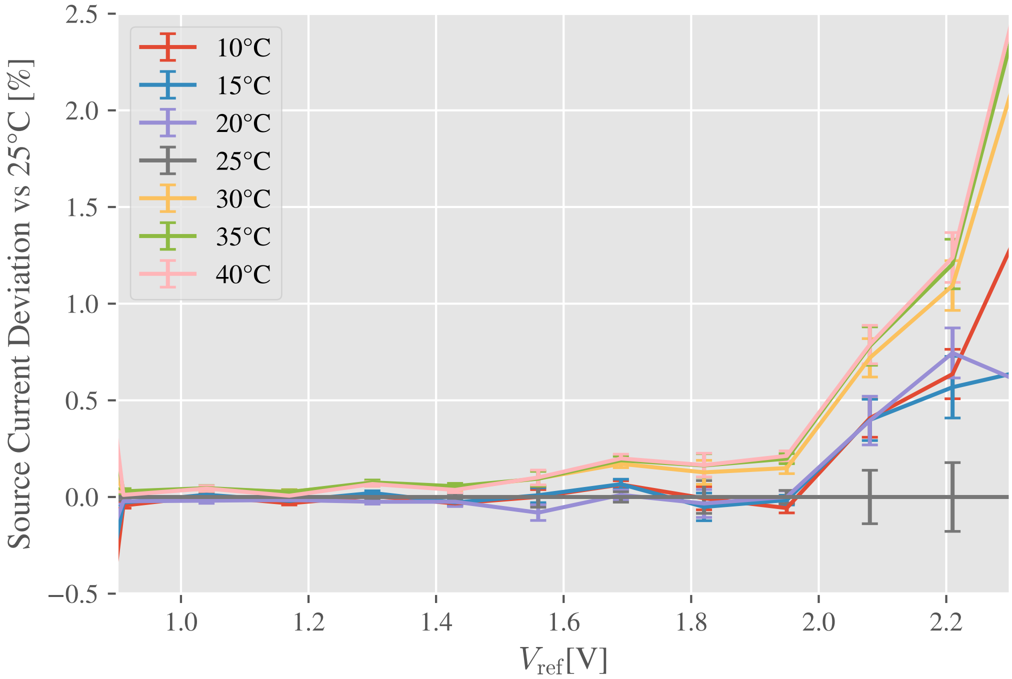

Figure 22: Temperature dependent deviation of source current as a function of V_{ref} at $V_{\text{op}} = 0.53\,\text{V}$, normalized to 25 °C

Reference voltages between 0.9 V and 1.9 V show a current deviation below 0.25 % under ambient air temperature variation from 10 °C to 40 °C. Non-linear behaviour is observed for reference voltages above 2 V with deviations larger than 0.5 %.

Once the reference voltage approaches the common-mode voltage range limit of the operational amplifier ($V_{\text{cm}} = V_{+} - 0.1\,\text{V}$), current deviations increase significantly (see figure 22). This increase is however largely due to the characteristics of the amplifier and is not caused by a change in ambient air temperature alone.

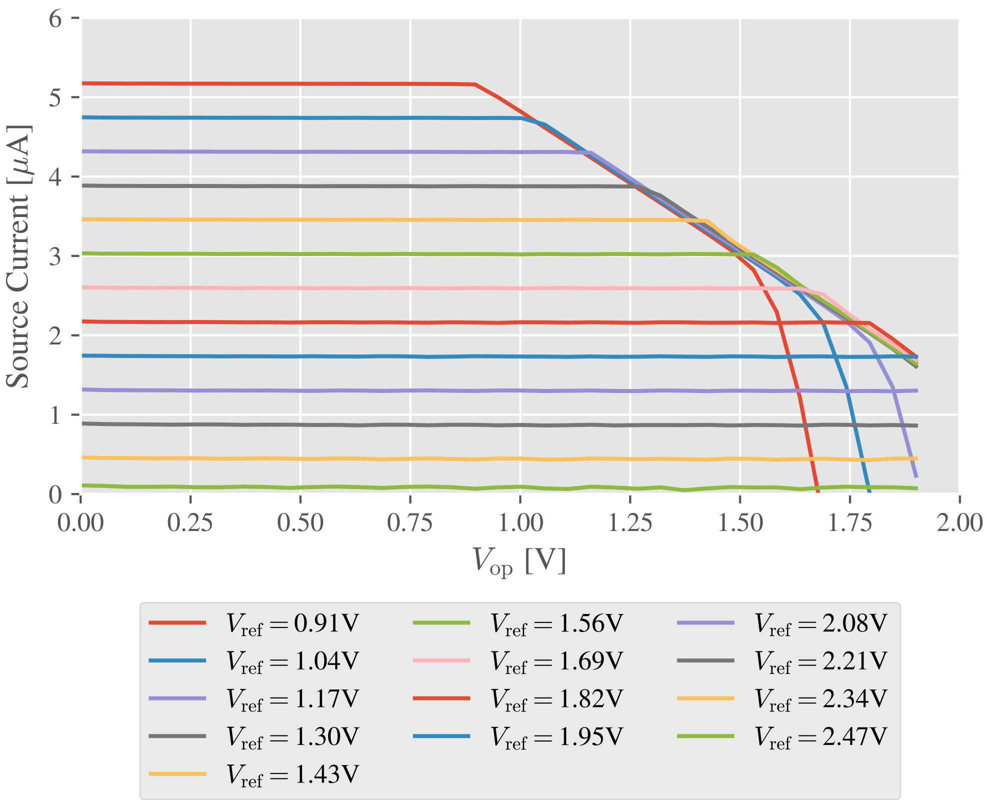

Figure 23: V_{op} sweep at $T_{\mathrm{amb}} = 25\,°\mathrm{C}$

For every voltage reference setting, the operational amplifier sets the gate-source voltage according to the voltage drop across resistor R_1. This ensures a constant current output. Once the operating point V_{op} surpassed the voltage drop across R_1, the polarity of the drain-source voltage switches and the output current collapses (see figure 23). For voltage reference values near the common-mode voltage range limit, the output current shows fluctuating behaviour.
The output current is constant up to an operating point of 0.9 V, satisfying the boundary conditions of the HICANN chip with a maximum operating point voltage of 503 mV (see figure 3).

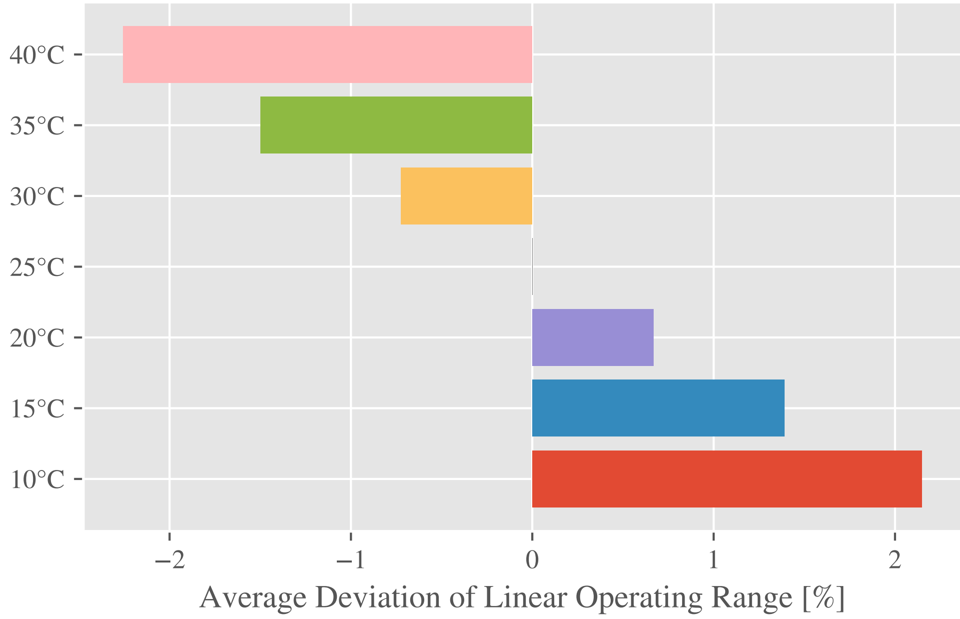

Figure 24: Average deviation of linear operating range due to ambient air temperature variation. Values indicate the change of the operating point where the source current collapses.

The constant current operating range shows deviations below 5 % for ambient air temperature variation from 10 °C to 40 °C. Lower temperatures increase the constant range, higher temperatures have a decreasing effect. Hence, an ambient temperature of 40 °C reduces the maximum valid operating voltage to 0.85 V, compared to 0.9 V at 25 °C. It can thus be concluded that the current source under review operates as required under the following parameter configuration:

Parameter	Linear Range
V_{ref}	0.9 V - 1.9 V
V_{op}	0 V - 0.85 V
T_{amb}	10 °C - 40 °C

Table 10: Linear operating parameter ranges for reference current source Option B

6 Summary and Discussion

This thesis examined the hardware design process of neuromorphic HICANN based multi-chip systems with a focus on adjustable constant reference current sources. Previous issues with BSS-2 Cube setups were taking into consideration and improved upon. Situations where a slave device permanently pulls the I^2C SDA line low, creating a *stuck bus* condition, have been rectified with a dedicated bus buffer, enabling the recovery of such situations. Further, dedicated port expanders provide an additional I^2C line to the power resets of each FPGA cluster. The JABBA PCB can encompass up to 12 FPGAs and HICANN chips with a footprint that is compatible to existing FPGA- and IO-boards. Power is supplied to the board through two PCI-E connectors and two Mate-n-Lok connectors, also known as *Molex connectors*, with a theoretical maximum power input of 1 kW.
Each FPGA can be uniquely addressed through their respective edge- and socket-ID. A network enabled Raspberry Pi system controller is used as an I^2C master, providing a JTAG interface to the FPGAs and enabling their configuration through a dedicated XVC server.

The HICANN chip requires a current source that is able to supply a constant current between 4.1 µA and 9.4 µA at operating voltages of up to 503 mV. This imposes boundary conditions toward the design of suitable external current sources. Consequently, two constant current source designs were tested and evaluated throughout this thesis.

Option A is based on an operational and instrumentation amplifier. Its voltage reference is supplied by a 10 bit DAC that is configured with a dedicated voltage reference IC at 2.5 V. The current source was evaluated through simulation, as a physical testing setup could not be realized within the short time frame of this thesis. The reference voltage on the non-inverting input sets the voltage across the current limiting resistor based on the configured gain value of the instrumentation amplifier. The current output increases linearly with increasing reference voltage for values outside the common-range voltage limit of the amplifier. As the positive rail of the amplifiers is configured with an input voltage of 3.3 V, non-linear behaviour is only observed for reference voltages near the ground rail. Output currents are constant with operating points of up to 2V for a given voltage reference value in the linear range. Deviations of the output current due to ambient air temperature variation between 10 °C and 40 °C are below 0.25 % for reference voltages above 1.5 V and negligible for lower values.

Option B utilizes a p-channel mosfet and an operational amplifier and was measured on a BSS-2 Cube system. The amplifier sets the gate-source voltage of the mosfet in such a way that the potential between the current limiting resistor and the source pin of the mosfet is equal to the reference voltage. The current output is only regulated for reference voltages above 0.9 V due to the single-supply configuration of the amplifier. This needs to be considered when selecting a current limiting resistor, as the maximum settable current value is lowered due to this offset. With the mosfet being operated in a sub-threshold mode at microampere current levels, minor fabrication variations can have a substantial effect on the required gate-source voltage for a given current setting. A dual-supply configuration would alleviate this limitation but would add additional complexity and is thus undesirable. Constant current outputs could be observed for operating voltages of up to 0.9 V at an ambient air temperature of 25 °C. Ambient air temperature variations between 10 °C and 40 °C showed an output current variation below 0.25 % for reference voltages between 0.9 V and 1.9 V. The constant current output range showed a deviation below 5 %, where lower temperatures extended the constant range and higher temperatures had a decreasing effect. At 40 °C, constant current output was observed for operating voltages of up to 0.85 V. It has to be noted that measurements concerning option A have been conducted with the circuit embedded in the BSS-2 Cube system. It can not be ruled out that auxiliary circuitry had an adverse effect on the performance of the current source.

Based on the boundary conditions imposed by the HICANN chip, both current source designs are able to deliver a constant current within the specified operating voltage range with high temperature stability. Although Option A shows a larger constant current output range and linear voltage reference range, Option B can be configured to regulate the required output current range within its linear range at high temperature stability through the selection of a fitting current limiting resistor. Additionally, the input voltage of current source B is also the voltage reference used by the DAC. This configuration is beneficial, as voltage variations on the supply line are compensated. The DAC of Option B is configured with a dedicated voltage reference IC at 2.5 V, as the current source uses a 3.3 V supply. While this enables a more precise control of other DAC output voltages, voltage variations on the input line of the current source are not compensated. As the performance of Option A was only analyzed through the means of simulation, further physical measurements are needed to confirm the obtained results.

Owing to its proven implementation in BSS-2 Cube systems, Option B is preferred due to its simplicity and lower component cost at this point in time.

References

Analog Devices (Aug. 2012). *AD5251/AD5252 Dual 64-/256-Position I2C Nonvolatile Memory Digital Potentiometers*.

– (Aug. 16, 2022). *LTspice*. Version 17.0.35. URL: https://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html.

Binder GmbH (July 2012). *Wechselklimaschraenke*.

Brette et al. (July 2005). "Adaptive exponential integrate-and-fire model as an effective description of neuronal activity". In: *Journal of neurophysiology*. DOI: 10.1152/jn.00686.2005.

Diodes Inc. (Apr. 2011). *1.5A Low Dropout Linear Regulator with Programmable Soft-Start*.

F9 (n.d.). *Labcontrol*. URL: brainscales-r.kip.uni-heidelberg.de:29418/labcontrol.

Hock, Matthias et al. (2013). "An analog dynamic memory array for neuromorphic hardware". In: *2013 European Conference on Circuit Theory and Design (ECCTD)*, pp. 1–4. DOI: 10.1109/ECCTD.2013.6662229.

Ilmberger, Joscha (Aug. 2022). "Personal communication". In.

Kay, Arthur (June 2013). *Low Level (5 uA) V-to-I Converter*.

KiCad Development Team (Dec. 2, 2021). *KiCad EDA*. Version 5.1.10-4. URL: https://archive.archlinux.org/packages/k/kicad/kicad-5.1.10-4-x86_64.pkg.tar.zst.

Linear Technology (July 2000). *LT1790 - Micropower SOT-23 Low Dropout Reference Family*.

– (2005). *LTC4303 Hot Swappable 2-Wire Bus Buffer with Stuck Bus Recovery*.

Monroe, Don (June 2014). "Neuromorphic computing gets ready for the (really) big time". In: *ACM*. DOI: 10.1145/2601069.

Nemec, Mitja (Jan. 15, 2022). *Kicad Action Plugins*. URL: https://github.com/MitjaNemec/Kicad_action_plugins.

Nexperia (Apr. 16, 2012). Version 2. URL: https://www.ti.com/lit/zip/sbom150.

– (Feb. 2013). *20 V, single P-channel Trench MOSFET*.

Onsemi (Nov. 2021). *N-Channel Logic Level Enhancement Mode Field Effect Transistor*.

Pehle et al. (Feb. 2022). "The BrainScaleS-2 Accelerated Neuromorphic System With Hybrid Plasticity". In: *Front. Neurosci.* 16.795876. DOI: 10.3389/fnins.2022.795876.

Stradmann, Yannik (Aug. 2022). "Personal communication". In.

Stucke, Maximilian (Sept. 3, 2022a). Version change-id: 18339.

– (June 2022b). "A network accessible system controller for BrainScaleS-2". In.

Tektronix (May 2013a). *Models 2634B, 2635B and 2636B SourceMeter SMU Instruments*.

– (May 2013b). *Series 2100 6.5-Digit USB Digital Multimeter*.

Texas Instruments (Nov. 2003). *QUAD, 10-Bit, LOW-POWER, VOLTAGE OUTPUT, I2C INTERFACE DIGITAL-TO-ANALOG CONVERTER*.

– (Nov. 2004). *Precision, Rail-to-Rail I/O INSTRUMENTATION AMPLIFIER*.

– (Jan. 2010). *UCD 9246 Digital PWM System Controller*.

– (Dec. 2014). *SN65LVDxx High-Speed Differential Line Drivers and Receivers*.

– (Dec. 2015a). *INA219 Zero-Drift, Bidirectional Current/Power Monitor With I2C Interface*.

– (Dec. 2015b). *OPAx333 1.8-V, microPower, CMOS Operational Amplifiers, Zero-Drift Series*.

– (Dec. 2015c). *TLVx333 2-uV VOS, 0.02-uV/C, 17-uA, CMOS Operational Amplifiers Zero-Drift Series*.

– (Feb. 1, 2016). Version Rev. C. URL: `https://www.ti.com/lit/zip/sbom965`.

– (June 5, 2017). Version Rev. A. URL: `https://www.ti.com/lit/zip/sbom150`.

– (Feb. 22, 2018). Version Rev. G. URL: `https://www.ti.com/lit/zip/sboc084`.

Acronyms

AC alternating current. 10

ADC analog to digital converter. 2, 12, 13

AdEx adaptive exponential integrate-and-fire. 1

ASIC application-specific integrated circuit. 1, 2, 4, 13

BSS-2 BrainScaleS-2. i, 1, 2, 4, 15, 19, 31, 32

CIS controlled impedance signal. 7

DAC digital to analog converter. 13, 16, 19, 20, 25, 31, 32

EMI electro-magnetic interference. 7, 10, 13

FPGA field programmable gate array. 1, 2, 4, 7, 8, 9, 13, 17, 18, 31, 35

HALCO Coordinate Systems for BrainScaleS architectures. 20

HFP HICANN/FPGA pair. 8, 18

I^2C Two-Wire Communication. 4, 11, 17, 18, 31

IC integrated circuit. 13, 31, 32

JABBA Just a Beautiful Bunch of ASICs. i, 1, 4, 5, 7, 17, 18, 31

JTAG Joint Test Action Group. 17, 31

KIP Kirchhoff Institute for Physics. 3, 1, 2

LDO low-dropout regulator. 10, 17

LVDS low-voltage differential signal. 13

NPTH non-plated through hole. 5

PCB Printed Circuit Board. 5, 7, 8, 31

PCI-E peripheral component interconnect express. 9, 31

PTH plated through hole. 5

RPi Raspberry Pi. 17, 18

SMD surface-mounted device. 5, 6

SMU source measure unit. 19, 20

THT through-hole technology. 5, 6

TI Texas Instruments. 13, 22

XVC Xilinx Virtual Cable. 17, 31

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Declaration/Erklärung

I hereby declare that I have written this thesis independently and have not used any materials or aids other than those indicated.

Hiermit versichere ich, dass ich diese Arbeit selbstständig verfasst und keine anderen als die angegebenen Quellen und Hilfsmittel verwendet habe.

Heidelberg, September 4, 2022: ______________________________

Stucke, Maximilian