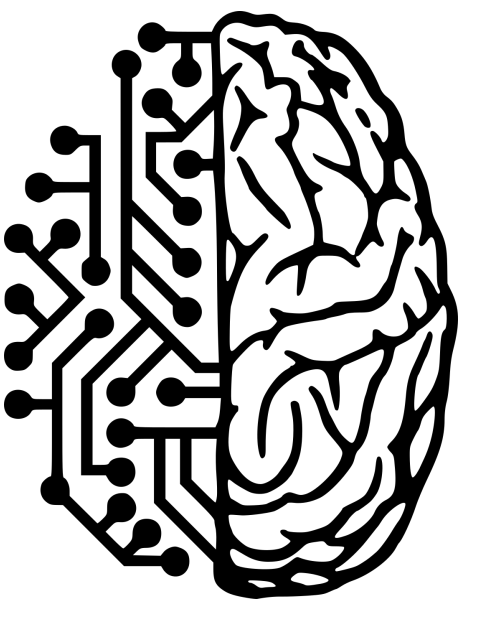


# Gradient Computation With Sparse Observations for Analog Neuromorphic Hardware

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## Introduction

Gradient-based learning has recently been demonstrated to be a suitable learning scheme for analog neuromorphic hardware [1, 2, 3, 7].

While previous approaches either make use of dense observations of neuron dynamics or are limited by assumptions on time constants, spiking behavior, and network topology, here we introduce an approach, based on the EventProp algorithm [8], that does only need spike-time observations from the neuromorphic hardware and is suitable for arbitrary network topologies and loss functions.

- 1. Spike Observations are sufficient for estimating gradients.** By training a feed-forward network of 120 Leaky-Integrate and Fire (LIF) neurons on a low dimensional classification task, we demonstrate for the first time that EventProp can be used as an in-the-loop training algorithm for analog neuromorphic hardware.
- 2. Numerical Gradient Estimates Converge.** We implement a numerical integration scheme for both the forward- and adjoint dynamics of LIF neurons [8] and show that the computed gradient converges to the analytically known solution in cases where an analytical gradient is known.
- 3. Mean Hardware Gradient Estimates agree with Analytical Solution.** We show that the mean gradient estimate obtained using spike time hardware measurements by our algorithm agrees with the analytically known solution in cases where an analytical gradient is known.

## Numerical Gradient Estimate Converges

We use a simple numerical integration scheme (explicit Euler integration) for both the forward and adjoint dynamics of a LIF neuron having exponential-shaped, current-based synapses [8]. To quantify the numerical error, we can compare to the analytical gradient in a special case ( $\tau_{\text{syn}} = \tau_{\text{mem}}$ ,  $\tau_{\text{refrac}} = 0$ ) for which an explicit formula is available, cf. [3]. We consider a situation where a LIF neuron receives a single spike with weight  $w$  (Fig. 1).

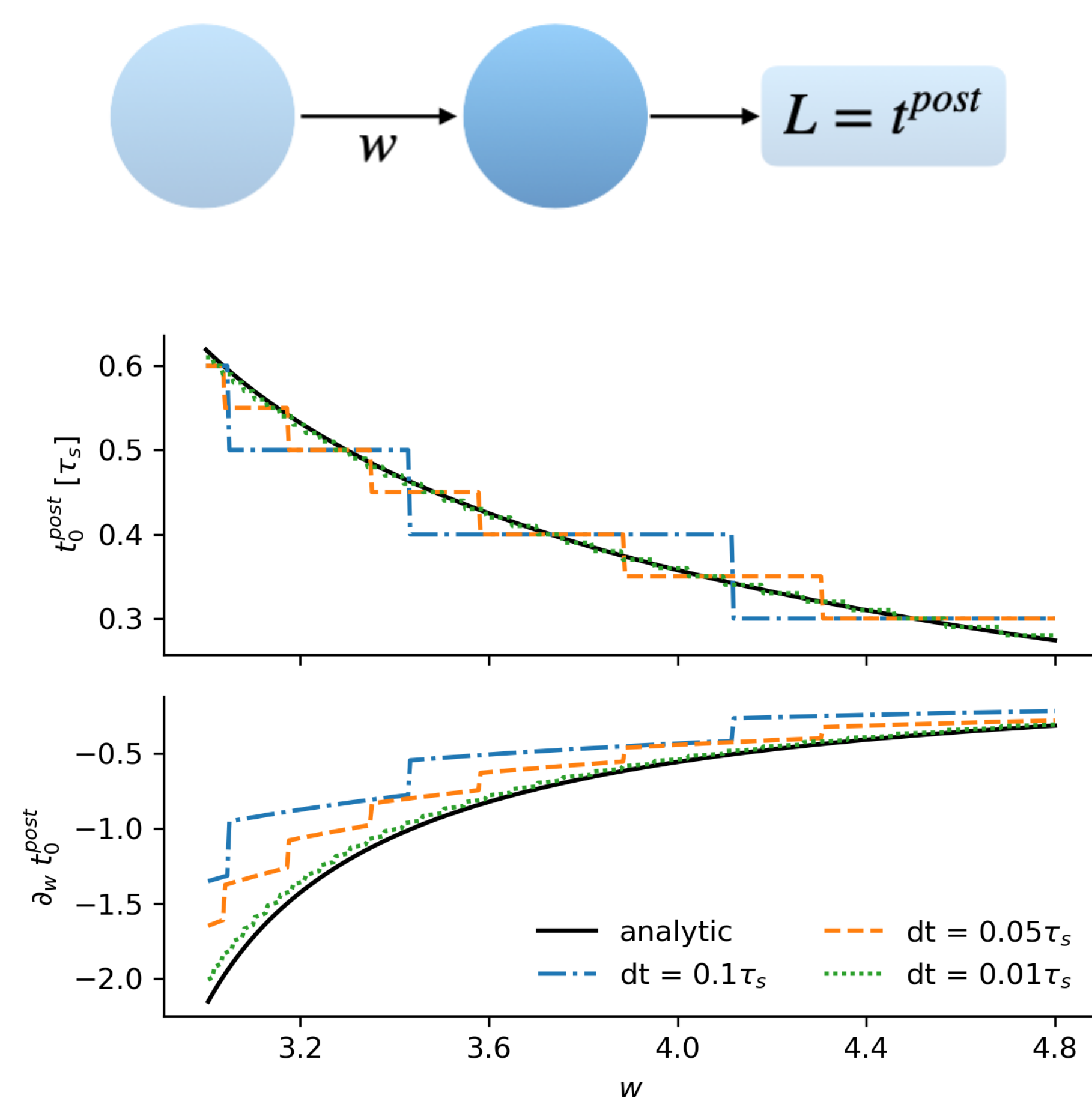


Figure 1. Experiment setup (top), spike time (center) and estimated gradient (bottom) for a loss function  $L = t^{\text{post}}$  as a function of the weight  $w$ . As the numerical integration timestep  $dt$  decreases the numerically estimated gradient (dashed lines) converges to analytically known gradient (solid-black line), cf. Göltz et al. [3].

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## Hardware Training Results on Yin-Yang

We choose the Yin-Yang dataset [4], a simple two-dimensional classification task with three classes, for demonstrating the learning algorithm on BrainScaleS-2, an accelerated analog neuromorphic research platform [6, 5].

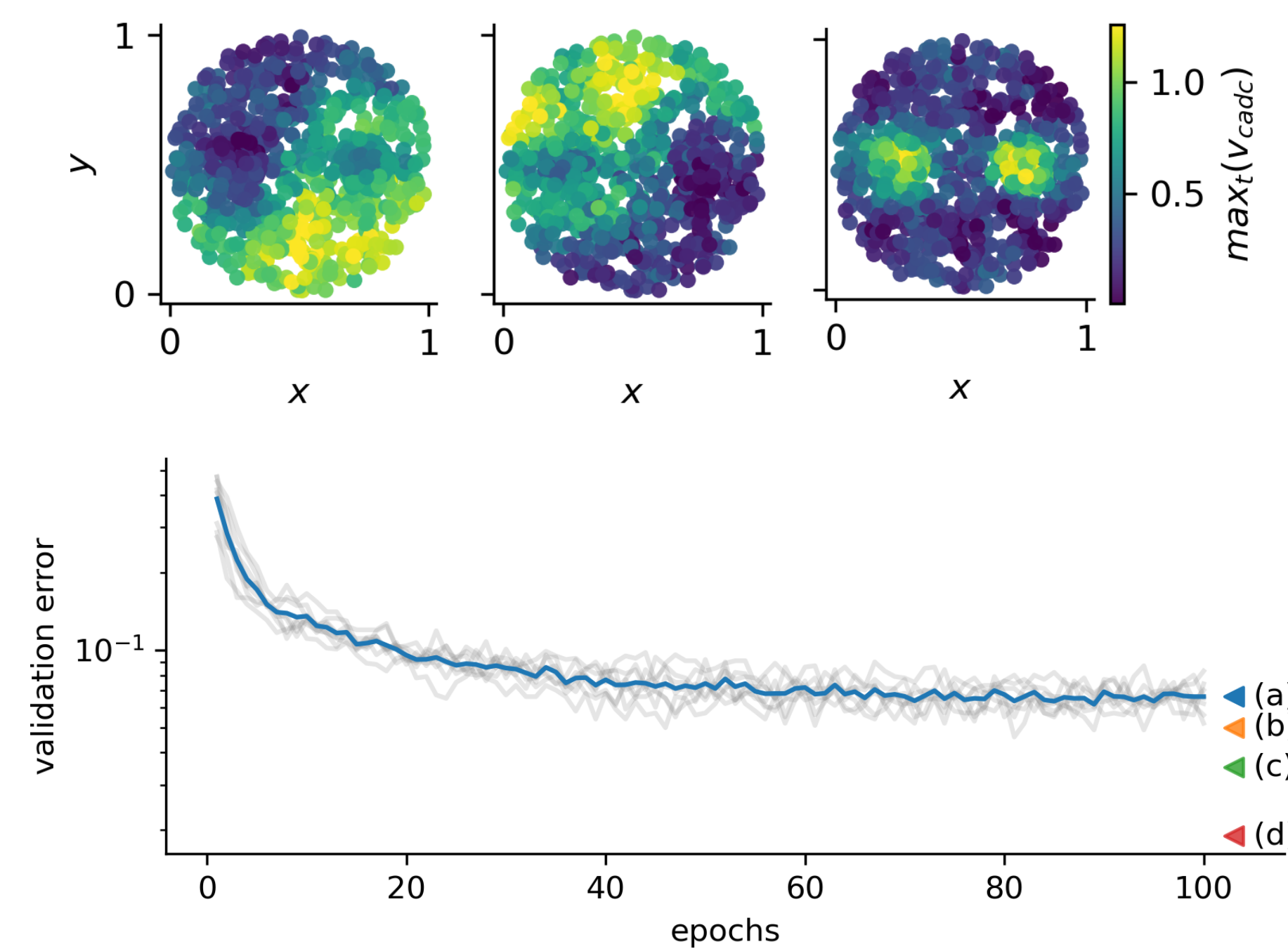


Figure 2. Maximum membrane values over time on validation set after training (top) and validation accuracy (bottom) for hardware-in-the-loop training with EventProp on the Yin-Yang dataset.

Gradient estimator		loss	test acc.
analytical [3]	sim.	TTFS	$95.9 \pm 0.7$
analytical [3]	hw	◀(b)	TTFS $95.0 \pm 0.9$
EventProp [8]	sim.	◀(d)	TTFS $98.1 \pm 0.2$
Surr. Gradient	sim.	Max	$96.0 \pm 0.5$
Surr. Gradient	hw	Max	$93.8 \pm 0.8$
EventProp	sim.	◀(c)	Max $96.5 \pm 0.7$
EventProp	hw	◀(a)	Max $93.4 \pm 0.9$

Table 1. Test accuracy on the Yin-Yang task for three gradient estimators, two loss definitions using numerical integration and hardware emulation. The results marked by 'TTFS' are using a loss based on time-to-first-spike decoding, the 'Max' results are based on 'maximum membrane value over time'.

## Hardware Gradient Estimation

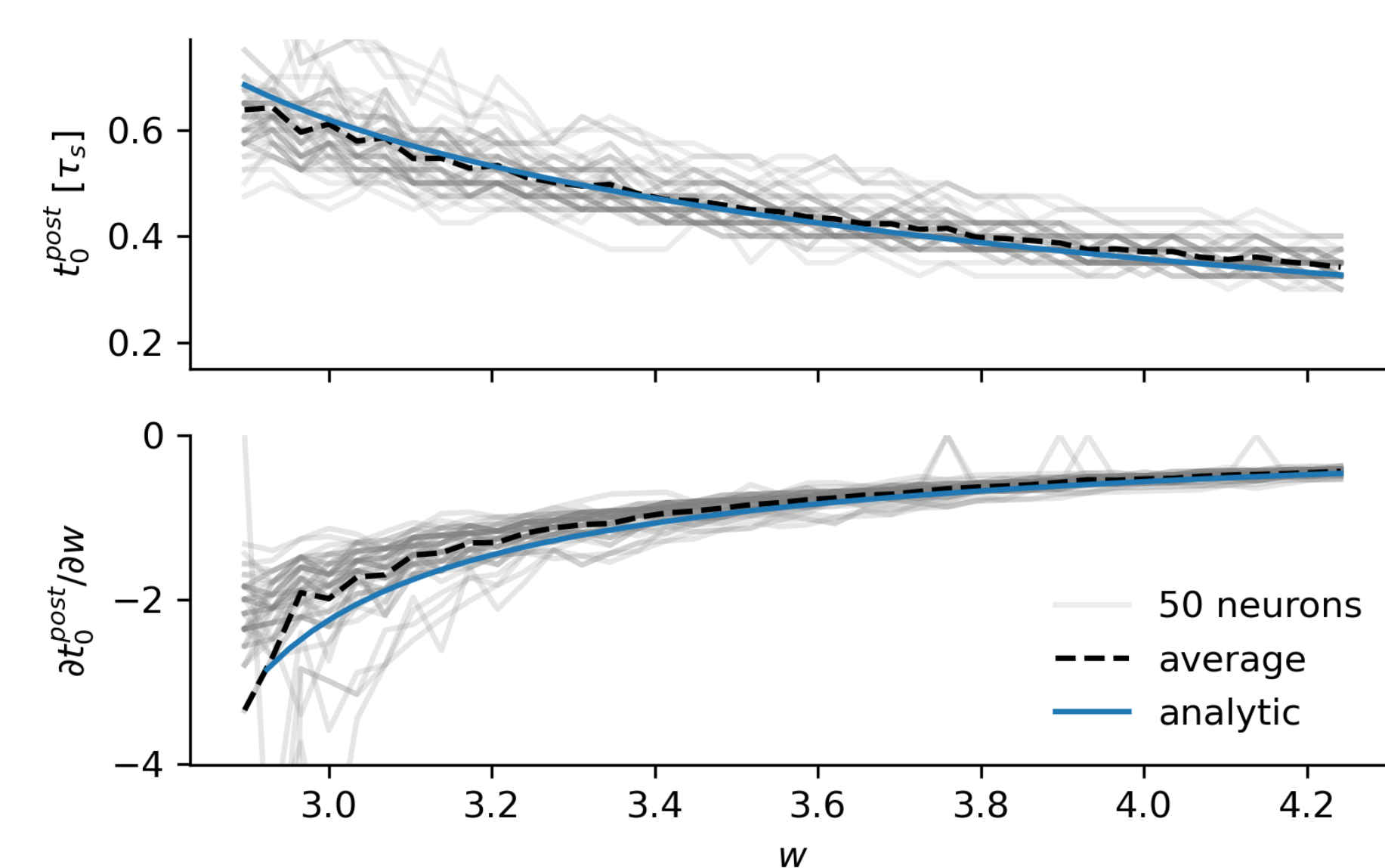


Figure 3. Spike time (top) and estimated gradient (bottom) for a loss function  $L = t^{\text{post}}$  as a function of the weight  $w$ . Results for  $n = 50$  hardware neuron circuits are shown in light grey, the average in dashed black. The analytical result (blue line, see Fig. 1) agrees well with the hardware average.

## Comparison to Surrogate Gradient

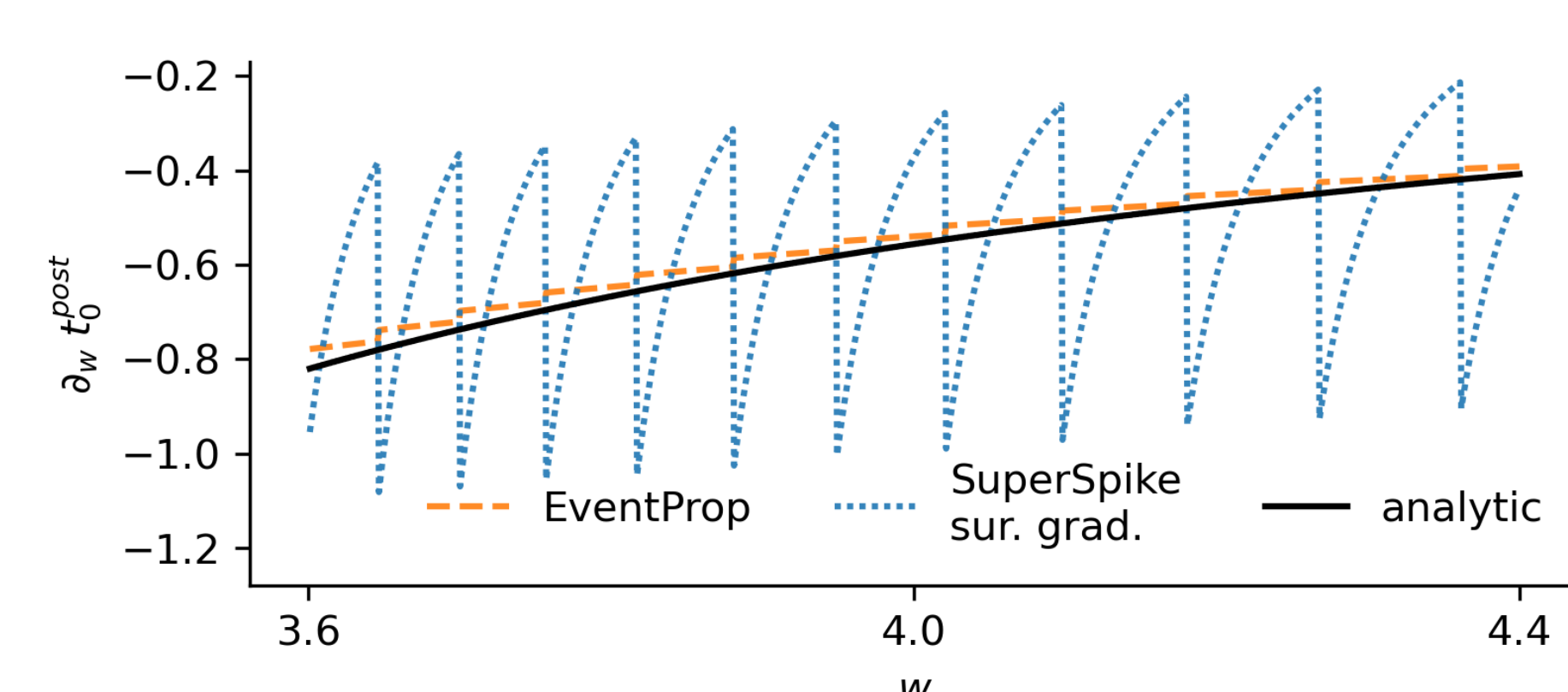


Figure 4. Numerical comparison of surrogate and EventProp gradient estimate evaluated with the same numerical precision to the analytical result. Same experiment as in Fig. 1.

## Hardware-in-the-loop Training

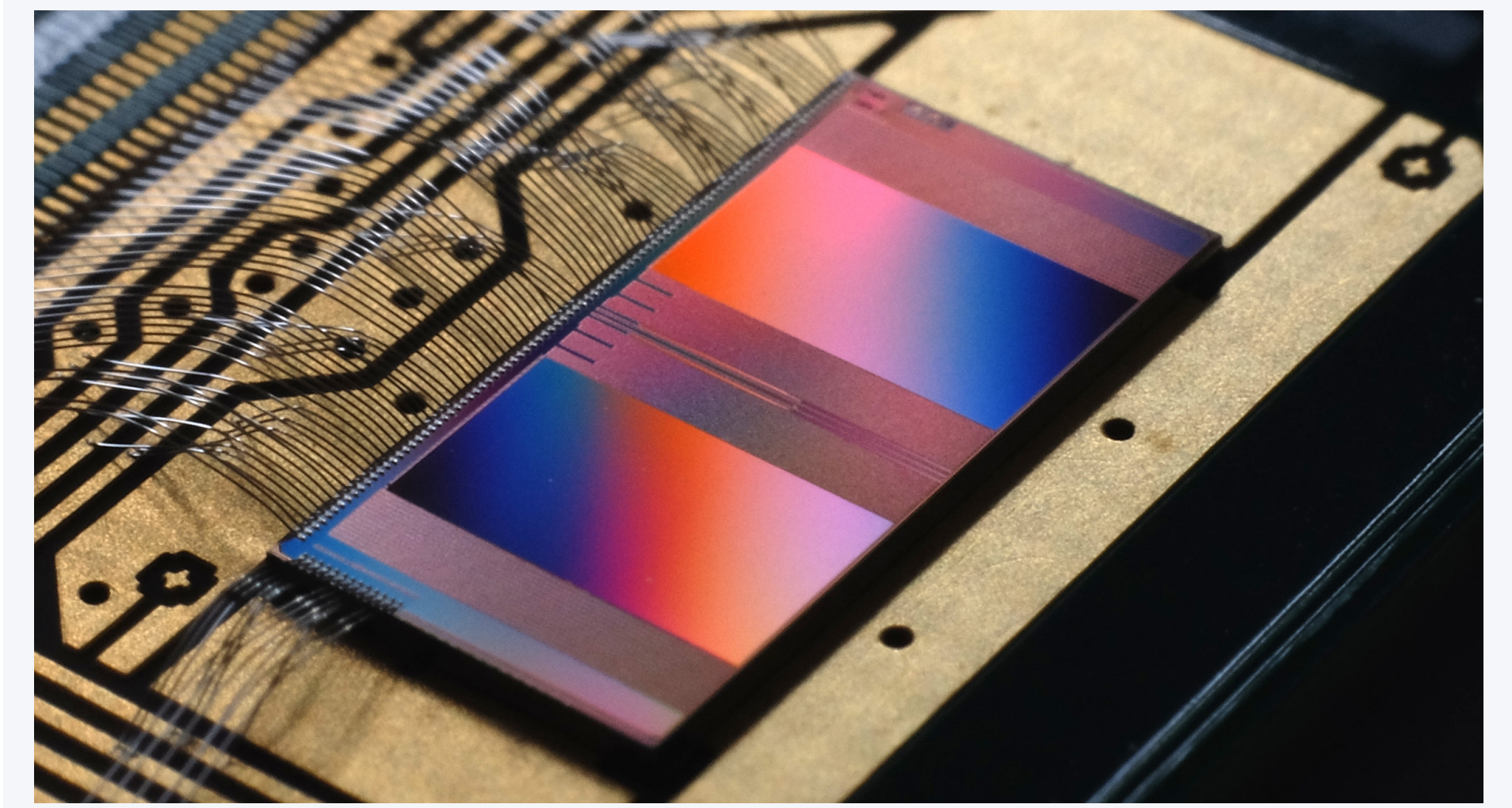


Figure 5. A BrainScaleS-2 neuromorphic chip ( $4 \text{ mm} \times 8 \text{ mm}$ ) bonded to a carrier board, see [6] for detailed information.

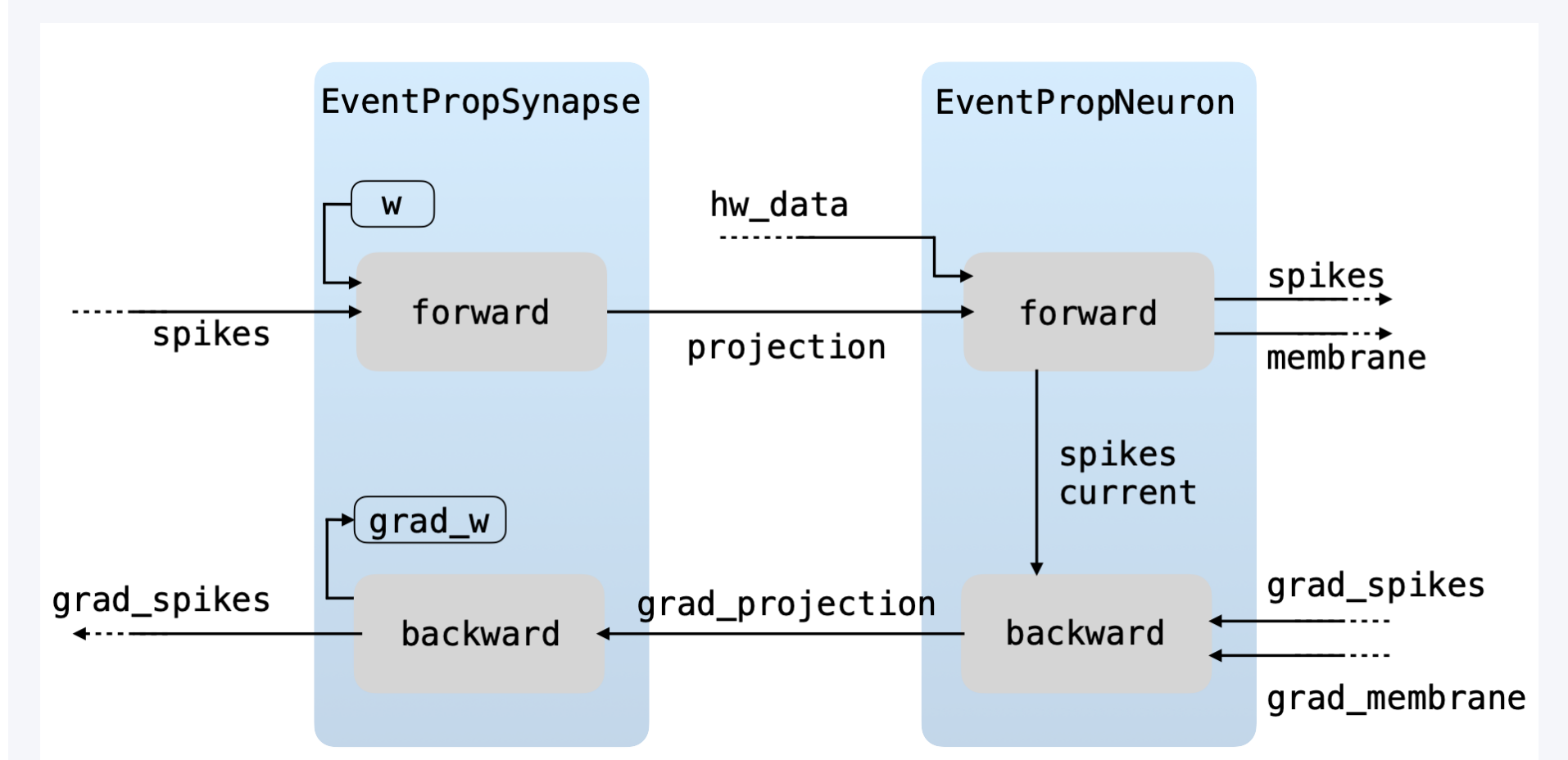


Figure 6. Dataflow occurring during hardware-in-the-loop training.

## Discussion

We have demonstrated a gradient estimation algorithm for analog neuromorphic hardware, which only requires spike observations and makes no assumptions on network topology or loss function. This has the potential to enable scalable gradient estimation in large-scale neuromorphic hardware, as the continuous measurement of observables would be prohibitive in this case. While the results reported here are encouraging further work is needed in several areas:

- We would like to demonstrate the algorithm on further tasks, particularly ones that are not feasible using surrogate-gradient-based in-the-loop training due to hardware trace-memory limitations.
- We would like to use hardware observables to learn the dynamics, instead of assuming a particular model.

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