Department of Physics and Astronomy
University of Heidelberg

Bachelor Thesis in Physics
submitted by

Philipp Dauer

born in Forchheim (Germany)

2020

Characterization of silicon neurons on HICANN-X v2

This Bachelor Thesis has been carried out by Philipp Dauer at the
Kirchhoff Institute for Physics
Heidelberg University
under the supervision of
Dr. Johannes Schemmel and Sebastian Billaudelle

Abstract

HICANN-X is the latest neuromorphic ASIC series, developed by the Heidelberg Electronic Vision(s) group. This thesis presents a fundamental characterization of some of the chip's analog circuits. The implemented analog parameter storage, the circuits describing LIF neuron behavior and the neuron's current based synaptic input were investigated. Of particular interest on the second version of the chip, manufactured in 2020, were the redesigned AdEx neuron extensions, which extended the LIF neuron towards a more biologically inspired behavior. For the fist time, AdEx circuits were measured on *BrainScales-2* and they were shown to be mostly functional. This thesis concludes with the qualitative reproduction of a diverse set of complex biologically inspired firing patterns.

Zusammenfassung

HICANN-X ist die aktuelle neuromorphe ASIC Serie der Heidelberger Electronic Vision(s) Gruppe. Diese Bachelorarbeit stellt eine grundlegende Charakterisierung einiger, sich darauf befindlichen, analogen Schaltungen vor. Dabei wurden unter anderem der kapaziative Speicher der analogen Parameter, Schaltungen des implementierten LIF Neurons und dessen Strom basierter synaptischer Input untersucht. Eine Besonderheit der 2020 gefertigten zweiten Chipversion ist eine neuimplentierung des AdEx Modelles als Erweiterung des LIF Modelles. Zum ersten mal in der Geschichte von *BrainScaleS-2* wurden AdEx Schaltungen vermessen und es konnte gezeigt werden, dass diese fast vollständig funktionieren. Diese Arbeit schließt mit der qualitativen Reproduktion von verschiedenen, komplexen und biologisch inspirierten Spikemustern.

Contents

1 Introduction

When Hodgkin and Huxley (1952) investigated the nerves of european squids *(Loligo vulgaris)*, they developed a model that describes neuron cells as electrical circuits. Their measurements on sodium and potassium channels as well as on cell membrane potentials culminated in four coupled and partly non-linear differential equations. Due to their non-linearity, this equations can be expensive to compute and hard to realize in electrical circuits. To reduce this computational complexity, simplified neuron models such as the decades older leaky integrate-and-fire model (LIF) (Lapicque, 1907) are used. The FitzHugh-Nagumo model (FHN) (FitzHugh, 1961; Nagumo et al., 1962) is an example of a neuron model, which is derived from the Hodgkin-Huxley-model. Of particular interest is the adaptive exponential integrate-and-fire model (AdEx) developed by Brette and Gerstner (2005). In its core, it can be reduced to the simple LIF equation, but its adaptation and exponential extensions allow to reproduce biologically realistic firing patterns.

However supercomputers need a lot of energy to simulate these models, especially in larger networks. Implementing neuron models in silicon hardware can emulate such computations for multiple complex applications as well as for research on the complexity of brains (Meier, 2017).

For nearly two decades, the Electronic Vision(s) group at the Kirchhoff-Institute for Physics Heidelberg researched neuromorphic spiking networks and developed i.a. the *Spikey* platform (Schemmel et al., 2006; Hartel, 2010) and the *BrainScalesS-1* system (Schemmel et al., 2008; Müller et al., 2020b). Their hardware is based on analog circuits for neurons and synapses and digital ones for spike routing and weight calculations. HICANN-X is the latest ASIC generation of such hardware from Heidelberg. 512 neurons with 256 synapses each already allow state-of-the-art experiments and applications (Billaudelle et al., 2019a; Göltz et al., 2019; Cramer et al., 2020; Czischek et al., 2020).

Although the AdEx equations were already implemented in *BrainScalesS-1* and have been present in the first version of HICANN-X, the second version introduces a major rework of the circuits. The new circuit's designs attempt to improve linearity and parameter ranges. This thesis will investigate the behavior of the implemented analog circuits and propose calibration routines for spiking AdEx neurons. Since Stradmann (2016) investigated HICANN-DLS's analog parameter storage and neuron circuit, a comparison of his results with these can illustrate the progress of the last years.

2 Materials and Background

2.1 Biological models

The goal of neuromorphic hardware is to adapt biological neuron models and translates them into electrical circuits. Different models describe different aspects of neuron behavior. Nearly all of them follow the concept that the brain communicates data by short peaks of electrical potentials, called spikes. These action potentials (APs) are transmitted via dendrites of post-synaptic neurons. The soma is then used to perform computations on this incoming spikes. When within the soma a threshold is crossed, a spike is sent via the axon to synapses that connect the neuron to dendrites of other neurons. The following chapter shall give a brief overview of some models describing the soma, which are implemented on the High Input Count Analog Neural Network X (HICANN-X).

Leaky integrate-and-fire model (LIF)

LIF describes the most fundamental aspects of neuron behavior. Mathematically, it is established by a leaky integration of incoming currents on the neuron membrane V_m. A fix threshold potential V_thresh causes the generation of a spike as well as it resets the neuron's membrane potential to a reset potential V_reset. The leaky integration can be realized by a capacity with capacitance C_m and a resistor with conductance g_l in parallel:

$$\begin{aligned} C_\mathrm{m} \cdot \frac{\mathrm{d}V_\mathrm{m}}{\mathrm{d}t} &= g_\mathrm{l} \cdot (V_\mathrm{leak} - V_\mathrm{m}) \\ V_\mathrm{m} &= V_\mathrm{reset}, \text{ if } V_\mathrm{m} > V_\mathrm{thresh} \end{aligned} \tag{2.1}$$

(Gerstner and Kistler, 2002).

Adaptive exponential integrate-and-fire model (AdEx)

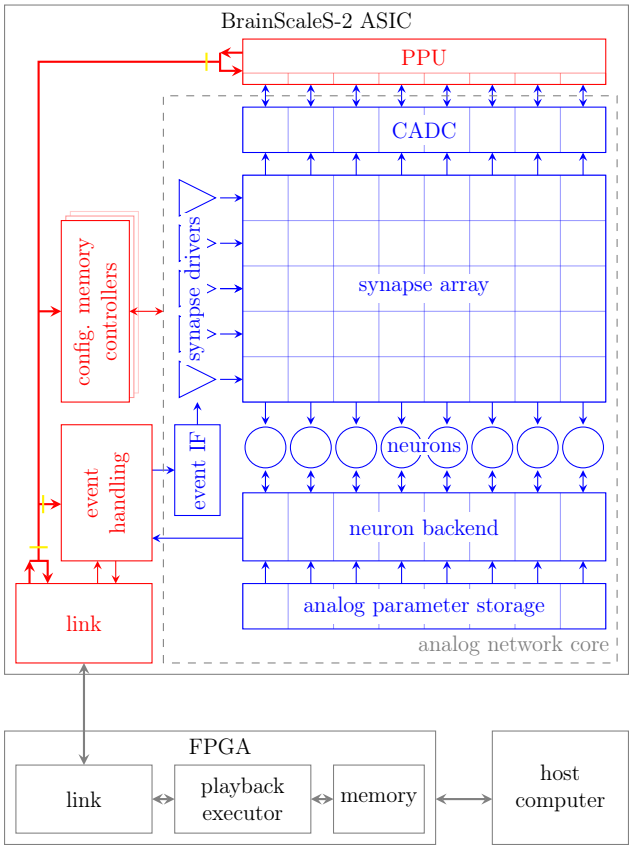
AdEx is an extension to the LIF neuron model. It introduces a smooth threshold, a sub-threshold adaptation and a spike-triggered adaption. Comparing the AdEx equations

$$
\begin{aligned}
C_\mathrm{m} \cdot \frac{\mathrm{d}V_\mathrm{m}}{\mathrm{d}t} &= g_\mathrm{l} \cdot (V_\mathrm{leak} - V_\mathrm{m}) + g_\mathrm{l} \cdot \Delta_\mathrm{T} \cdot \exp\left(\frac{V_\mathrm{m} - V_\mathrm{T}}{\Delta_\mathrm{T}}\right) + I_\mathrm{ext} - w \\
\tau_w \cdot \frac{\mathrm{d}w}{\mathrm{d}t} &= a \cdot (V_\mathrm{m} - V_\mathrm{leak}) - w \\
V_\mathrm{m} &= V_\mathrm{reset} \text{ and } w = w + b, \text{ if } V_\mathrm{m} > V_\mathrm{thresh}
\end{aligned}
\tag{2.2}
$$

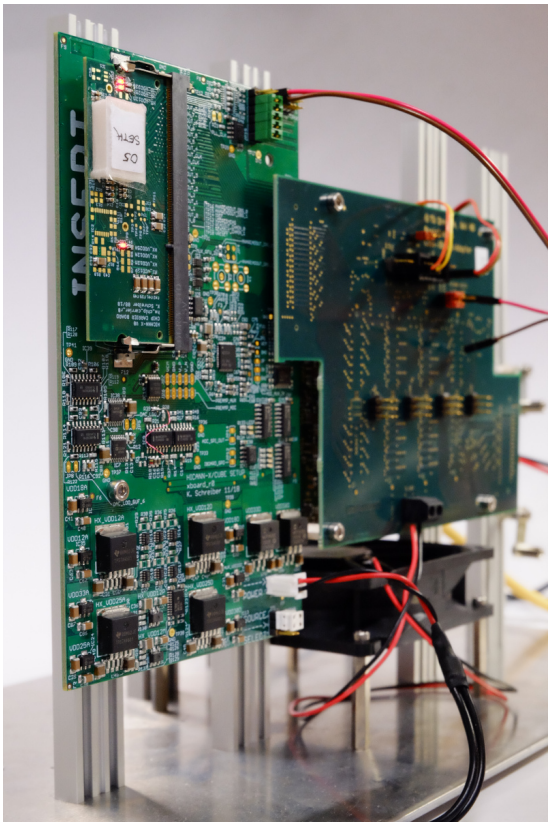
to the LIF equations 2.1, the former equation was extended by a non-linear term and was coupled to another non-linear first-order differential equation. As colored in red, the exponential term consists of a smooth threshold V_T and a slope factor Δ_T. As soon as the membrane passes V_T, a "point-of-no-return" will be reached. The exponential term drives the membrane potential towards the fixed threshold potential V_thresh. Colored in blue, the adaptation term is described as another leaky integrator with time constant τ_w. In the membrane's sub-threshold domain, the adaptation state follows the difference between membrane potential V_m and leak potential V_leak with strength a. When the neuron emits a spike, the adaptation state will be shifted by the current b. AdEx can emulate neuron behavior from the Hodgkin-Huxley model as e.g the firing pattern suggested by Naud et al. (2008).

Current-based model (CUBA) for the synaptic input

Besides the integrating part of the neuron, models of the synaptic input are needed to produce post-synaptic-potentials (PSPs) on the neuron's membrane. Generally speaking, a synaptic input can excite or inhibit the membrane potential. As opposed to the conductance-based model (COBA) for the synaptic input, which modulates time-depended conductances between the membrane and two reversal potentials, the current-based model (CUBA) directly generate a current onto the membrane, shaped by an exponentially decaying kernel. The implemented version of the synaptic input is physically divided into an excitatory and an inhibitory component. Both components are rather similar, as they integrate incoming δ-shaped spikes as decays back to their baseline with time constants τ_syn. Further, an operational trans-conductance amplifier (OTA) is used to generate a current proportional to the state of this integrator, which then affects the membrane.



(a) Block-level diagram of HICANN-X taken from Grübl et al. (2020)



(b) Photo of a cube setup. Under the white cap at the upper left corner, the HICANN-X chip is mounted. Photo: Eric Müller.

Figure 1: Visual introduction of HICANN DLS X.

2.2 Neuromorphic substrate

The HICANN-X chip, based on 65 nm CMOS technology, conjoins nearly two decades of research on neuromorphic hardware in Heidelberg. As part of *BrainScaleS-2*, it clearly steps into the tradition of the High Input Count Analog Neural Network (HICANN) *(BrainScaleS-1)*, which ended up in a wafer-scaled system (Müller et al., 2020b). Afterwards HICANN-DLS was a prototype series of *BrainScaleS-2*, that provided 32 neurons per chip. Since Stradmann (2016) characterized the neurons circuits and the analog parameter storage of HICANN-DLS v2, this thesis will often compare these previous results with results from HICANN-X.

HICANN-X features 512 analog neurons on four blocks, controlled by a memory of 48 bits and 8 voltages as well as 16 currents. Due to limited specific capacitances in CMOS tech-

nologies, the time constants are thousand times smaller compared to biological models, which results in a speed up factor of 1000. For a better dynamic range, biological voltages are scaled and shifted to cover most of the usable supply range with $V_{\text{hw}} = V_{\text{bio}} \cdot 15 + 1.50\,\text{V}$. Like previous chips, HICANN-X is divided into a digital and an analog part. The digital part contains two plasticity processing units (PPUs), data busses and a hand-drawn as well as generated digital logic controlling the neuron. Analog components are the synapse array and the neurons. The neuron backend manages the digital part of the neuron, such as the output spike management. Furthermore analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) were implemented on the application-specific integrated circuit (ASIC)

The synapse array is a matrix of 512 times 256 connections. Each row of the synapse array is connected to a synapse driver, processes input from either a host computer program, a random spike generator or by the spike output of a neuron. At the crossing of a row and a column a 6-bit synapse is placed, which's weight can be updated using learning rules on the host computer or on the PPU. For the neurons' spike input each neuron is connected to one column of this synapse array.

Internally the chip communicates via a bus system. The chip is connected to a field-programmable gate array (FPGA) which is responsible for the host-chip communication. Due to manufacturing uncertainties and the resulting transistor mismatch, all quantities and parameters that corresponds to currents, voltages or biological parameters need to be calibrated.

Mounted in cube setups, each chip is bonded on a chip-carrier-board, that is plugged into an XBoard. This XBord is responsible for power management, passes though data from and to the FPGA and carries DACs (section 3.2). The XBoard is racked into another connection board, which ends in one of four possible FPGA slots. To complete the description of a cube setup, the opposite site of the FPGA is mounted on an I/O-Bord that controls the ethernet ports.

HICANN-X v1

HICANN-X v1 (HXv1), developed in 2018 and produced in 2019, is the first usable version of the HICANN-X chip series. Its analog core differs from the smaller prototyping series mainly in a newly designed leak term and a larger system size.

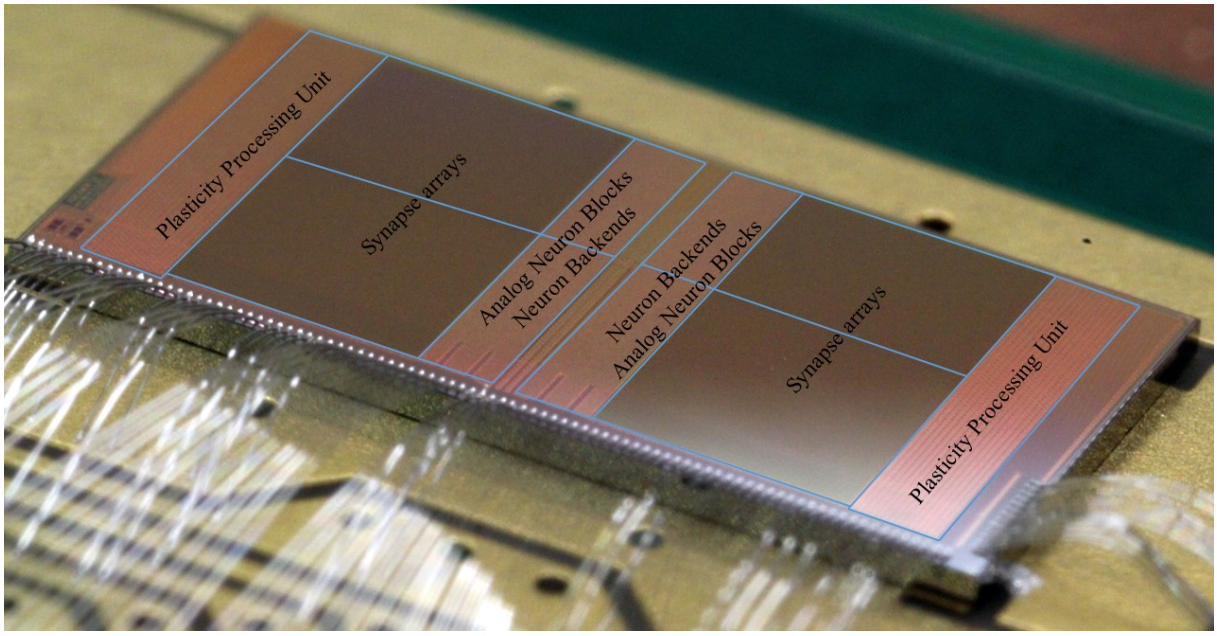


Figure 2: Photo of HICANN DLS X v1 with overlaying schematic. Photo: Eric Müller.

HICANN-X v2

In it's analog neuron, HICANN-X v2 (HXv2) introduces multiple new designed circuits as i.a. new adaptation and exponential terms and a new CUBA synaptic input. Also multiple technical issues of HXv1 were fixed, such as i.a. the reference control of the analog parameter storage is now on a block wise level. Since this chip version will be present in research for the next years, thesis will mainly discuss the behavior of HXv2.

3 Measurement methods

For characterizing the HICANN-X chip, several tools and measurement devices were used and some were developed. They can be split up into software, on-chip-devices and external devices. The former allows to control the chip to execute experiments, the second is used for daily calibration and experiment purposes. Low-level characterization often requires additional, external laboratory equipment for more detailed measurements.

3.1 Software

BrainScaleS-2 software stack

Heidelberg's Electronic Vision(s) group is not only about designing hardware, but also about making this hardware usable (Müller et al., 2020a). For communication between chip and program commands, this includes especially the development of required software. Different layers of hardware-abstraction reduce the complexity of the system to a level of interest. In case of this thesis, mostly individual configuration bits were set. Therefore mostly configuration containers, that concentrate and label multiple configuration bits to a smallest meaningful writable package, were used. Per default, containers are filled with best-guess configurations. The used software includes python-bindings to execute programs via *Python*. A code-snipped of the typical structure that were used to write containers during this thesis is shown below. As usual for software, this software stack is under continuous development and just represent the state of the art during this theses.

```
1 import pyhxcomm_vx as hxcomm
2 import pystadls_vx as stadls
3 import pyhaldls_vx as haldls
4 import pyhalco_hicann_dls_vx as halco
5
6 # Program for chip initialization
7 init = stadls.ExperimentInit()
8 init_builder = init.generate()
9 init_program = init_builder.done()
10
11 # Program for experiments
```

```
experiment_builder = stadls.PlaybackProgramBuilder()

# e.g. write a container responsible for
#      controlling an analog-to-digital converter
config = haldls.MADCConfig()
config.number_of_samples = 1000
experiment_builder.write(
    halco.MADCConfigOnDLS(), config)

experiment_program = experiment_builder.done()

# Start connection and execute program
with hxcomm.ManagedConnection() as connection:
    stadls.run(connection, init_program)
    stadls.run(connection, experiment_program)

# Afterwards the 'experiment program' contains the experiment results
```

Cadence Spectre

The analog components of ASICs in the Electronic Vision(s) group are designed in the *Cadence Virtuoso Analog Design Environment*, and hence a circuit verification with *Cadence Spectre* suggests itself (Grübl et al., 2020). *Cadence Spectre* allows full-custom simulations using Monte Carlo methods as well as corner variations. For setting up a simulation, either the interface of the tool or the arbitrary data interface can be used.

Teststand

Teststand is a *Python* software package between *Cadence Spectre* and the programming language *Python* (Schemmel et al., 2020). It allows to use the full power of *Cadence Spectre* in a programmatic environment including parallelization of circuit simulations. This makes it possible to even calibrate circuits virtually for verification. Furthermore, *teststand* was used to benchmark the analog part of HXv2 with the firing pattern suggested by Naud et al. (2008) (Dauer, 2019). Whenever this thesis references simulation data, these were collected using *teststand* and mostly taken from Dauer (2019).

HICANN-X characterization framework

For this thesis, a new developed framework was based on the framework used for the verification of HXv2. While it separates either hardware or simulation specific backends from measurement methods, it allows a comparison between chips and simulations. The free functions `sweep()` and `search()` apply measurement methods to backends in order to investigate parameters by a parameter sweep or a (binary) search.

3.2 References and analog readout

Keithley 2635B Sourcemeter

For characterizing the chips, elementary measurements were performed with a sourcemeter. Since the on-chip sourcemeter has not yet been put into operation, an external device was used. The *Keithley 2635B Sourcemeter* is a remotely usable programmable high-precision analyzer with a resolution of 0.10 pF.

For remote purpose, an *C++* library which can be called via *Python* is provided (Stradmann, 2016). Before a current measurement can start, a reference voltage needs to be applied by the sourcemeter. Due to leakage offset currents inside circuits, a measured baseline of the background needs to be removed from the acquired data.

Keithley 2635B Sourcemeter does also support to measure voltages.

LeCroy Wavesurfer 44Xs

More for debug purpose than for automated measurements *LeCroy Wavesurfer 44Xs* together with *LeCroy ZS1000* active probes were used to verify settings of the chip manually. The 8-bit scope offers high sampling rates up to 2.50 GS/s and interfaces for *C++* and *Python* libraries.

Analog Devices AD5328 (DAC)

Each XBoard is equipped with a DAC, to provide reference voltages. According to the manual from AnalogDevices (2011), the 12 bit *Analog Devices AD5328* with an output

voltage range between 0 V and 2.50 V has a relative accuracy of typically ±2 LSB and of ±16 LSB at its maximum. This thesis uses the DAC for calibrating the on-chip ADC.

Analog-to-digital converter

HICANN-X is equipped with two different kinds of ADCs: column-parallel ADCs (CADCs) with in total 1024 8 bit channels and a 10 bit ADC with a higher sampling rate. The latter is called MADC and was used frequently in this thesis.

Because of the mismatch within the ADCs, an individual characterization is essential. Therefore the described reference voltage DAC sweeps through a range of voltages, which are measured by the ADC afterwards. As also shown in figure 3, the linear range of the ADC is sufficient from 0.10 V to 1.10 V. Whenever this thesis illustrates voltages in figure, which are measured by the MADC, the regions outside this specification are colored in red.

When neuron potentials such as the membrane, synaptic or adaptation potentials are investigated with the MADC, the neuron readout amplifiers were involved. This buffer was not characterized for this thesis and could distort measured potentials. Experimentally, the MADC can be used to estimate currents. For this purpose the rising voltage on a capacitor of known size, in this case on a neuron membrane, was used. In this thesis, this method was used to calibrate the current's offset in the analog parameter storage as discussed in section 4.

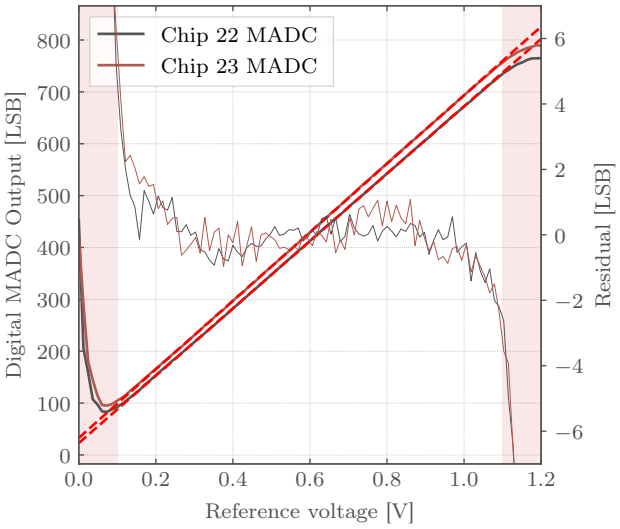


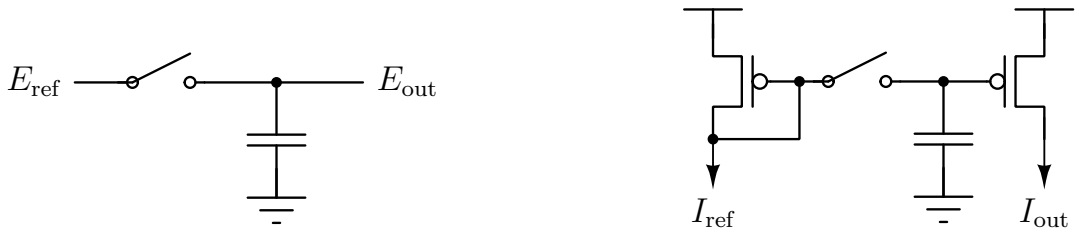
Figure 3: Measurement, fit and residual of the MADC's characteristic curve for chip 22 and chip 23 using the reference DAC on the corresponding XBoard for the input voltages.

4 Characterization of the analog parameter storage

Most analog circuits and especially the neurons of HICANN-X depend on digitally adjustable currents and voltages. The chip's circuits require control voltages between 0.10 V and 1.50 V as well as (bias-)currents between 20 nA and 1 µA with 0 nA output at 0 LSB (Billaudelle, 2019). Furthermore, a linear for all neurons similar translation of digital values into analog quantities is needed for practical usage.

Therefore, four 10 bit capacitive memories, one on each neuron block, are implemented on the ASIC. Each capacitive memory block is divided into current and voltage cells that are mapped in columns and rows. Since HICANN-X has 128 neurons per block, each neuron corresponds to a column with eight voltage and 16 current cells. Two more columns per block are used for block-wide or even global currents or voltages. In total, each HICANN-X provides 4160 voltage and 8320 current cells. An investigation on these analog parameter storages is a solid foundation for further measurements on the chip.

Circuit description



(a) Voltage Cell (b) Current Cell

Figure 4: Simplified drawing of capacitive memory cells taken from Stradmann (2016).

The capacitive memory (Hock, 2015) generates voltages E_{out} as well as currents I_{out} from potentials stored on capacitors. Voltage cells directly expose their stored potentials. Current cells use the latter as gate-source voltages for a transistor biased as a current source, very similar to a split up current mirror. The stored potentials are programmed and periodically refreshed from a global reference voltage ramp E_{ref} or respectively the current I_{ref}, which is derived from E_{ref}. Each cell carries its value in a 10 bit static random-access memory (SRAM) word, which determines the point in time, where its capacitor is attached to the sweeping reference by temporarily closing a switch. It is important to

mention that the local voltage cells are not buffered and therefore can not be loaded.

HXv2 introduced a more fine granulated control over the reference current generator by allowing to control these currents individually per capacitive memory block. The configuration used in this thesis is shown in the appendix table 1.

Due to a oscillation of the reference voltages after closing the switches, corrupted output voltages or currents can be observed when many cells store the same value. This cross talk between cells is known (Hock, 2015) and still unsolved in the current chip version. Nevertheless, setting the bias that stabilized the reference voltage to maximum (`capmem amplifier` = 63 LSB) and a change in the timing of opening and closing the switches to the reference voltage E_{ref} or current I_{ref}, reduces this unwished effect.

For a low-level characterization, the capacitive memory allows to read out the individual cells directly. Local voltage cells are however buffered via a source follower so that the absolute potential of these cells is not available.

Reference slope

The most fundamental observable of this capacitive memory is given by voltage ramp. Demonstrated in figure 5, its slope controls the slope of the output voltages and currents.

Its bias current is adjustable in 6 bits and was calibrated to generate 1.80 V at 1000 LSB in voltage cells. To be scalable in ASICs, an on-chip calibration was preferred. Even if the MADC has an upper limit of 1.10 V, it was the predestined device. Hence the analog parameter storage was calibrated to 0.90 V at 500 LSB. Since the reference voltage slope intrinsically affects the MADC's characteristic by changing its bias currents, for each slope additionally the external DAC at 0.90 V were measured. By sweeping different reference voltage slopes and comparing MADC measurements of the external DAC with the same of multiple global voltage cells, the best reference voltage slope was chosen.

Since - even without calibration - the blocks showed very similar behavior and the slope can only be controlled with a coarse granularity, in the end similar slope settings for all blocks were received.

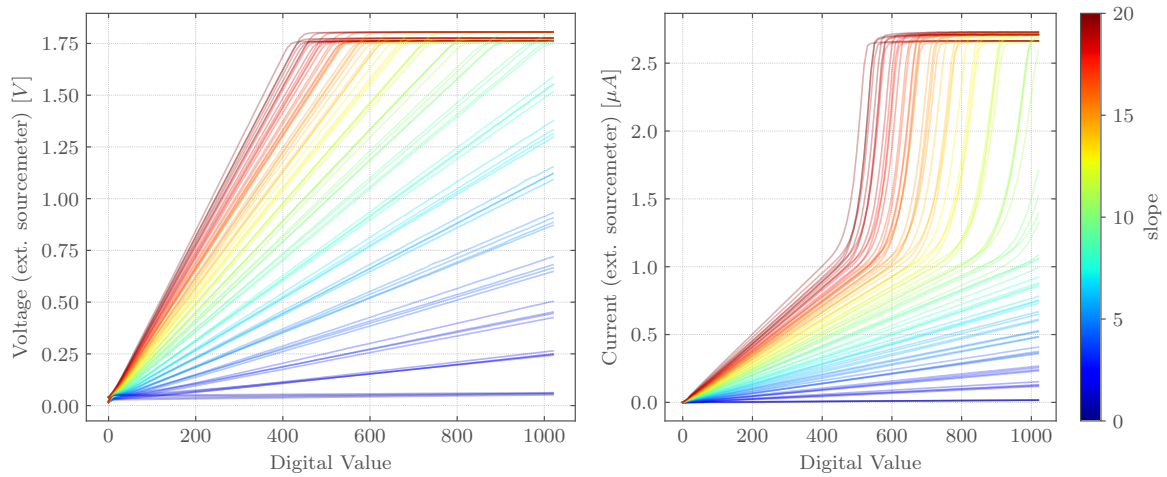


Figure 5: Characteristic curves of row 5 (voltages) and row 8 (currents) on column 128 for all four blocks on chip 22. The capacitive memory slope was arranged for each step from 0 to 20

Current offset

To be able to counteract manufacturing uncertainties, an offset compensation with 64 possible settings is placed in the reference current I_{ref}. Such an offset can beware especially problematic when for a cell programmed to 0 LSB a non-zero current is generated since this would lead to a situation where some circuits cannot be disabled. A further calibration of the offset compensation was required, to harmonize the blocks as well as to ensure about 20 nA at 20 LSB.

Assuming that a maximum compensation finally ensures zero output at 0 LSB, a current estimation as illustrated in section 3.2 was used as baseline. Therefore the offset compensation setting for cells programmed to 0 LSB was increased for each block starting at zero, until the output current crossed the baseline.

It became apparent that this method for calibrating to the former requirement also acceptably caught the latter. Figure 6 illustrates the difference from a uncalibrated to a calibrated offset at an already harmonized slope, measured with an external sourcemeter at chip 22. As noticeable in table 1, the calibrated setting differed a lot between chips and blocks.

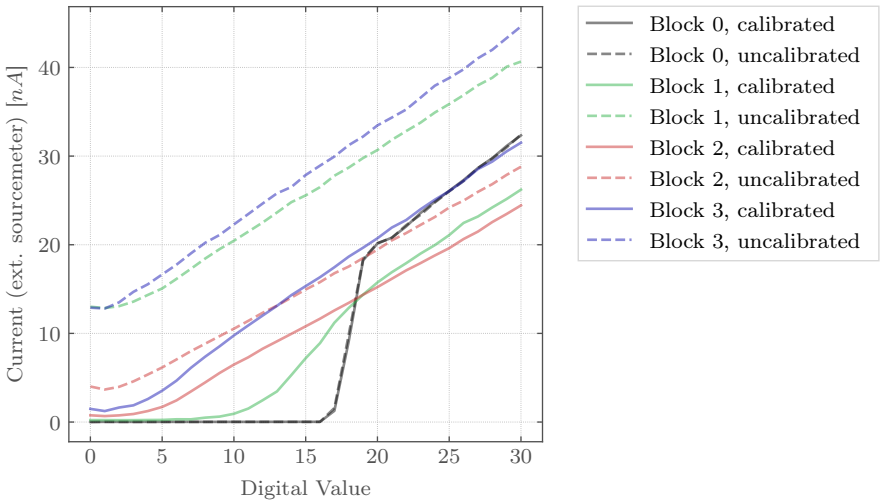


Figure 6: Uncalibrated and calibrated current offset in the capacitive memory blocks of chip 22, measured from the current cells on column 128 and row 8 with an external source meter.

Integrated non-linearity (INL)

Looking on figure 7, where the characteristic curves of voltage and current cells on chip 22 are shown, the saturation of voltage cells attracts attention. In the same time, also the currents diverge at high digital values. Both are correlated as already observable in figure 5. So far it seems to be a problem that could be solved by a less steep slope. Since this would cause a lower maximal output current, it was decided not to do so.

In total, the dynamic range for voltages and currents is reliably given, but not always linear. For the purpose of this thesis, this results in a non-trivial translation between digital value and output current or voltage and prohibits to characterize circuits in absolute units for bias currents and reference voltages.

Differential non-linearity (DNL), integrated non-linearity (INL), gain error and offset error are universal quantities to characterize the performance of an ADC or a DAC. Due to the high resolution of the capacitive memories, the integrated non-linearity (INL) is of more interest than the differential non-linearity (DNL). Since the offset of current cells is already calibrated and voltage cells are designed such that they have a small offset error, in following the INL and the gain error is discussed. The INL describes the difference between a linear fit and the measured outputs for a sweep over all digital settings. The

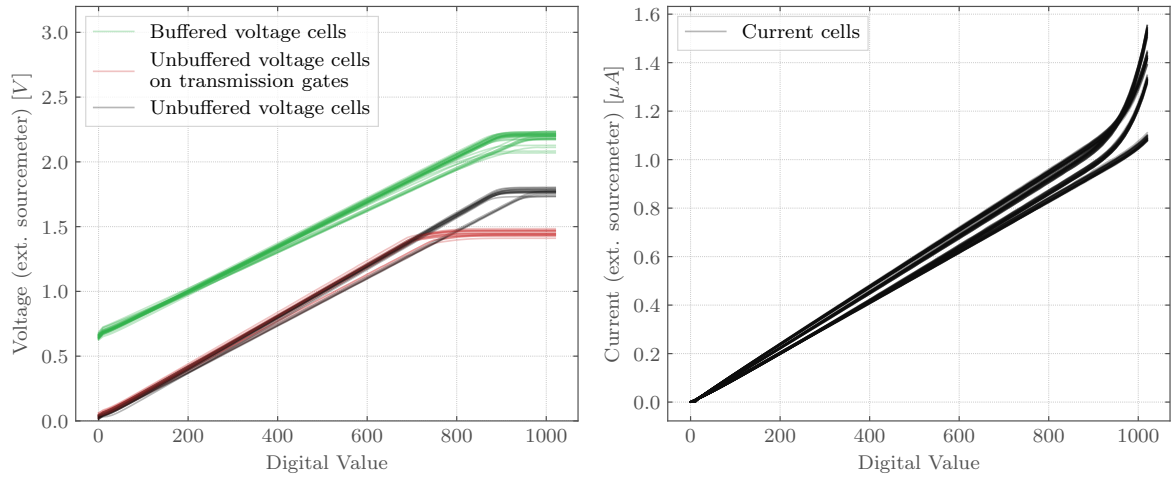


Figure 7: Characteristic curves of column 0 (first neuron on block) and column 128 (global cells) for all four capacitive memories on chip 22 (HXv2) measured with an external sourcemeter in steps of 10 LSB. For each investigated column all 8 voltage rows and all 16 current rows are measured. The `ReferenceGeneratorConfig` is calibrated as given in appendix table 1.

gain error evaluate the difference from the determined slope by the linear fit to the ideal slope.

As observable in voltage cells as well as in current cells, the slope is not precise enough to harmonize the blocks among each other or to a reference voltage. In theory, a linear voltage translation should be given by 1.80 mV/LSB, but the measured values of the calibrated capacitive memory differ significantly from this (figure 9a). Similar, also the current cells overshot their theoretical linear slope given by 1.00 nA/LSB (figure 9c). On the other hand, this figure allows to suspect a similar slope for each neuron of a block.

With respect to the INL, which is drawn in figure 9ab, a linear usable region was found to be between about 0 LSB and 700 LSB for voltages and 20 LSB and 800 LSB for currents. It stands out that for current cells unlike for voltages cells, whose INL for different blocks is quite similar, the INL differed significantly between different blocks.

Conclusion

Overall, there is much more to investigate for a capacitive memory, but for the purpose of this thesis this would be beyond the scope. During this thesis, cross talk was prevented

Characteristic values of an capacitive memory		Ideal	Chip 22 Block 0	Block 1	Block 2	Block 3
Current cells						
Slope (mean)	nA/LSB	1	1.192	1.039	1.070	1.130
Slope (std)	nA/LSB	-	0.008	0.008	0.010	0.010
Lower linear limit	LSB	20	20	20	10	10
Upper linear limit	LSB	1021	800	800	800	800
INL (max, in limits)	nA	-	±5.5	±5.8	±13.5	±7.9
Voltage cells						
Slope (column 128, row 5)	mV/LSB	1.800	1.985	1.839	1.980	2.027
Slope (fit error)	mV/LSB	-	0.003	0.002	0.002	0.003
Lower linear limit	LSB	0	0	0	0	0
Upper linear limit	LSB	1021	700	700	700	700
INL (max, in limits)	mV	-	±41	±20	±25	±49

Figure 8: Table of some characteristic values of the capacitive memories on chip 22. For currents, the cells shown in figure 9 were investigated.

by just setting cells of one investigated neuron unequal to zero at the same time. For calibration purpose, which should be usable for neuronal spiking networks, this needs to be considered. When absolute and precise voltages or currents are required to be known, a block-wise characterization and translation is recommended.

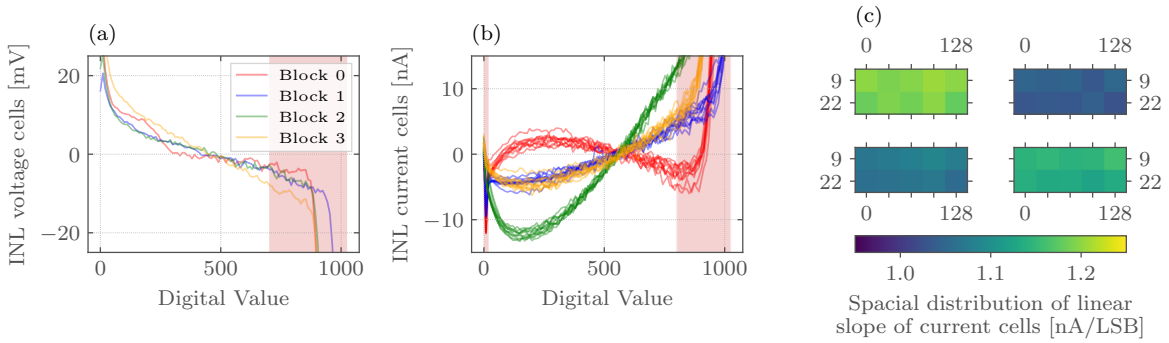


Figure 9: Integrated non-linearity (INL) and slope of the capacitive memories on chip 22.
(a): INL of voltage cells. Column 128; Row 5.
(b): INL of current cells. Columns 0, 4, 64, 124, 127; Rows 5, 9.
(c): Spatial distribution of the linear slope for the current cells investigated in (b).
Blocks are counted from left to right and upper to lower.

5 Neuron characterization

The circuits of the investigated neurons can be considered as an aggregation of components that effect the membrane potential V_m. As illustrated in figure 10, the neuron membrane is realized by a capacitor. Even it's capacitance C_m is tunable in 6 bits, this thesis operates with its maximum value `membrane_capacitor_size` = 63 which was expected to result in about $C_\mathrm{m} = 2.40\,\mathrm{pF}$. A comparator triggers a digital output spike and pulls a reset when the membrane potential V_m crosses the threshold potential V_thresh. Together with the leak term, these three parts provide a LIF neuron without any input. The adaptation and the exponential term instantiate AdEx behavior in the neurons. Symmetrically assembled CUBA synaptic inputs transform input current pulses from synapses into exponentially shaped and amplified currents which then affect the membrane potential. Some experiments, like the firing patterns from Naud et al. (2008), require the membrane to be stimulated by an offset current, which is implemented by the offset current term. In the latest version of HICANN-X, the offset current term can act as excitation or inhibition by switching it's sign. This thesis uses the neuron readout for calibration and characterization of the neuron's circuits, even though it has not been fully characterized itself.

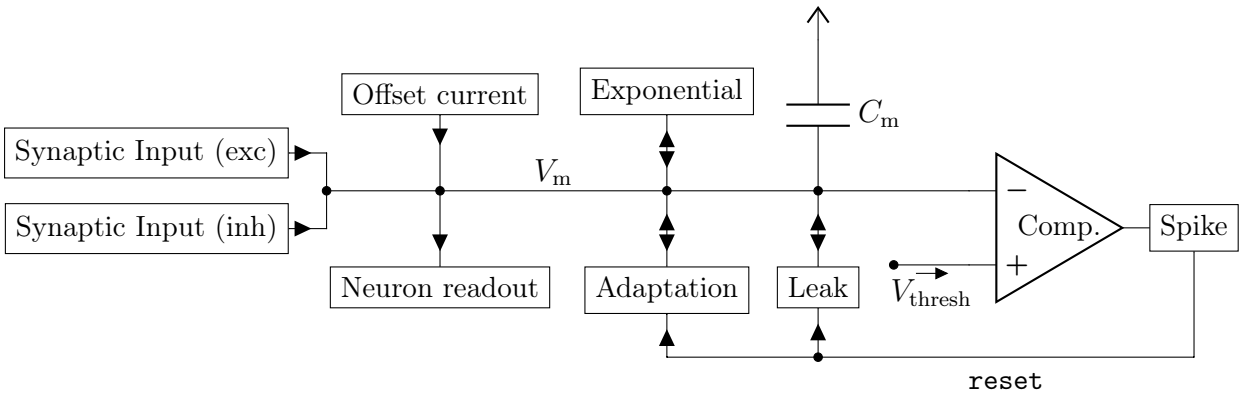


Figure 10: Schematic overview of the neuron terms in HXv2. Arrows marks the direction of information.

5.1 Leak term and threshold comparator

The LIF behavior, as described in equation (2.1), results from the threshold comparator as well as the membrane capacitance C_m and the leak conductance g_l. The latter two

result in the membrane time constant

$$\tau_{\mathrm{m}} = \frac{C_{\mathrm{m}}}{g_{\mathrm{l}}}. \tag{5.1}$$

The following section will discuss these components in detail, which were designed by Sebastian Billaudelle.

Circuit description

While the capacitance C_{m} and threshold comparator are already schematically shown in figure 10, figure 11 presents a simplified circuit diagram of the leak term. In basic terms, the leak term's adjustable resistor is given by an OTA, which connection and resistance can be switched between a leak and a reset mode. Predominately the former is used until the comparator pulls a reset as described in the second line of equation (2.1). In this case the pseudo resistor, which is controlled by the OTA's bias current, switches to a typically higher conductance to nearly instantaneously set the membrane potential V_{m} to the reset voltage. During the time the reset is pulled, the neuron is in a refractory state and not able to emit another spike. In order to realize membrane time constants in the range of sub-micro seconds to, in the best case, hundreds of micro seconds, a conductance multiplication and a division mode is implemented into the OTA and controlled by two digital bits. Each scales the conductance by about one order of magnitude. Iter alia for calibration purposes, on the one hand, the reset of the neuron's membrane can also be forced manually and, on the other hand, the comparator can be disabled to prevent output spikes and resets.

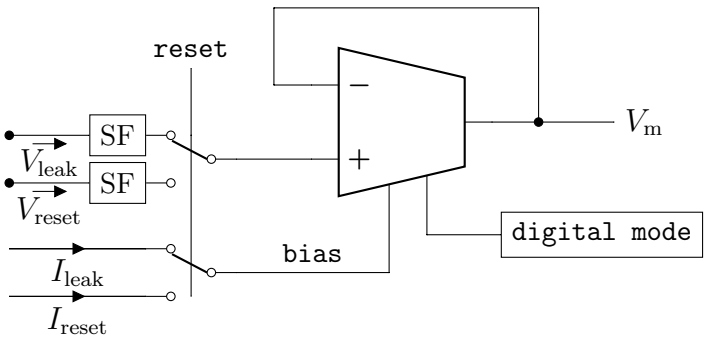


Figure 11: Schematic overview of the leak term circuit. In the centered leak-OTA, digital shift bits enlarges the range of adjustable conductances. For the time, the reset is pulled, the switches on the left hand side change the OTA's input from leak to reset.

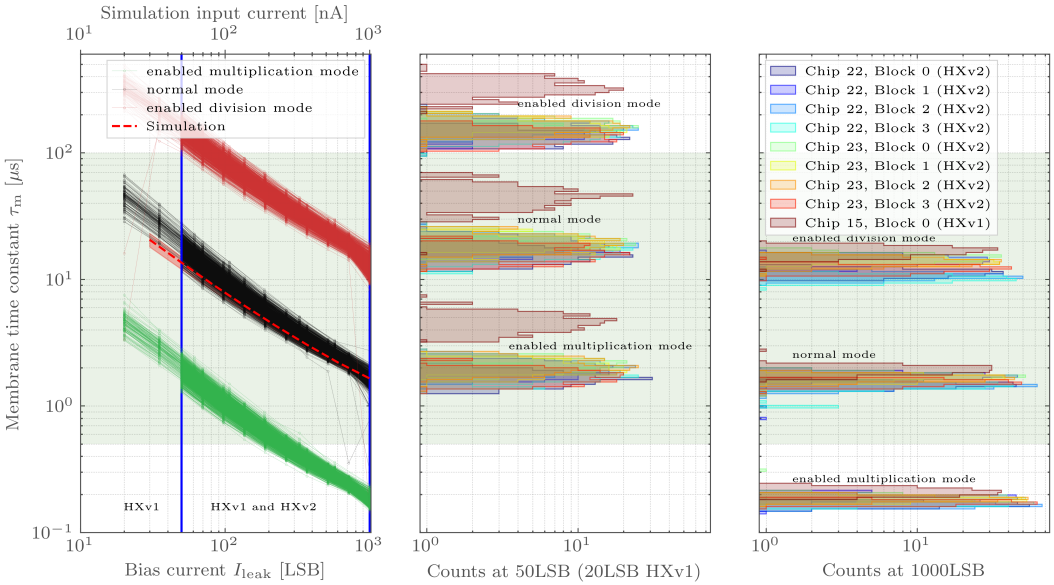


Figure 12: Measured and simulated membrane time constant on HXv2 and HXv1 with respect to the leak bias current I_{leak} and with and without enabled multiplication and division mode for chip 15, chip 22 and chip 23. The distribution of the measurements at 50 LSB and 1000 LSB (marked by blue vertical lines) are shown in the histograms with respect to modes, neurons and blocks.

Membrane time constant

A fundamental quantity of a neuron emulating circuit is given by the membrane time constant τ_{m}. Defined in equation (5.1), it is as a link between the leak conductance with the capacitance. When an external input shifts the membrane potential V_{m} to a voltage unequal to the leak potential, τ_{m} describes the relaxation time. These can then be determined by an exponential fit. Assuming a constant capacitance, it characterizes in particular the leak conductance. In the same way, the reset time constant could also be investigated. However, as far as the reset membrane time constant is typically not calibrated but set to the shortest value possible and both time constants use the same OTA, a second measurement is not of interest for this thesis.

As shown in figure 12 through a green background, a membrane time constant in the range of 0.50 µs and 100 µs is specified. Measured on HXv2 for bias currents I_{leak} between 50 LSB and 1000 LSB, this aim were achieved for almost all neurons. Considering the measurements on HXv1 with bias currents within the range from 20 LSB to 50 LSB, it could be assumed that the leak term in HXv2 is monotonic until the lower border given

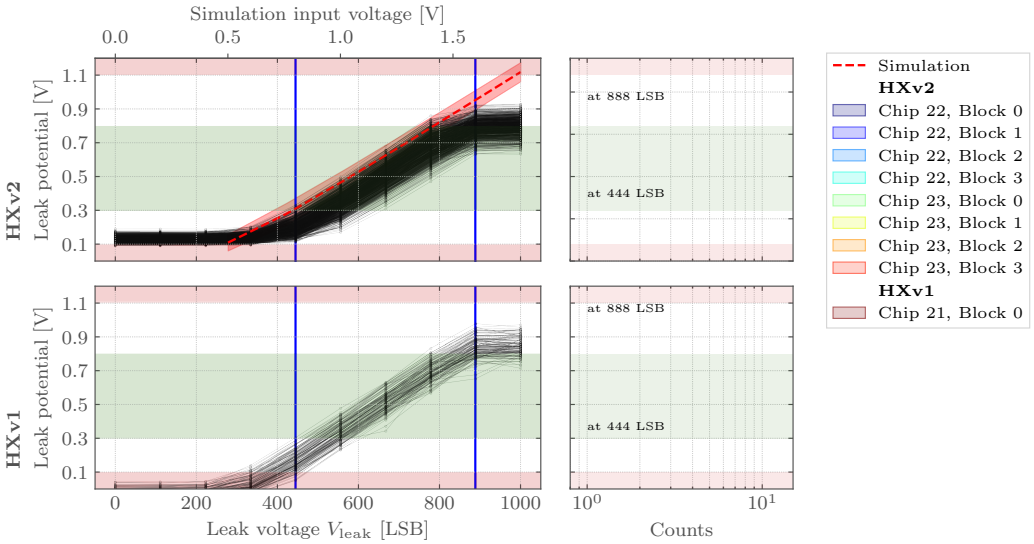


Figure 13: Measured and simulated leak potential on HXv2 (upper) and on HXv1 (lower) with respect to the leak voltage V_{leak} for chip 21, chip 22 and chip 23. The green colored specifications are not satisfied for all neurons. The distribution of the measurements at 444 LSB and 888 LSB (marked by blue vertical lines) are shown in the histograms with respect to neurons and blocks.

by the analog parameter storage. Figure 12 also shows the membrane time τ_{m} constants extracted from a Monte Carlo simulation of the neuron circuit including 20 samples. The mean as well as the standard deviation σ are plotted. Considering the smaller sample size and the fact that the measured data includes a total of 1024 (HXv2) + 128 (HXv1) neurons distributed over three chips from two different manufacturing runs, the measured distribution did not deviate significantly from the simulation. The systematically shorted time constants of the simulation most likely originated from parasitic capacitances not included in the simulation. Throughout all blocks the distribution spreading was in the same order of magnitude and larger than the shift between different blocks. Sporadically an outlier time constant behavior could be observed. This became apparent when it was not possible for the algorithm to find a good fit due to multiple imperfect initial guesses.

Leak voltage

The leak potential was measured by setting the corresponding parameter to a certain value, then waiting for the membrane to settle and finally determining the mean of the membrane potential during an interval of 5 µs by using the neuron readout in combination

with the MADC. So far not discussed, some voltages use a source follower between the analog parameter storage and the consuming circuit, as for instance in the leak and reset voltage. In schematic figure 15, noted by a box with label SF, the output voltage is reduced by approximately 0.70 V. To realize leak potential in biological inspired scaled ranges and utilize a wide dynamic ranges, the circuits were designed for a usable range between 0.30 V and 0.80 V. This upper limit is only achieved by half of the neurons on HXv2 across both chips and all blocks. As a one-block snapshot on HXv1, the lower plot in figure 13 seems to exhibit a slightly better performance. The saturation at large digital values is given by the saturation of the capacitive memory as mentioned in section 4 and can be improved by using a different source follower bias or transistor scaling. Potentially strongly effected by the different setting of the neuron readout and the limitations of the MADC, the first version of HICANN-X allows leak potentials to be set for all neurons less then 0.10 V, but HXv2 does not reach voltages lower then 0.10 V. Simulation data (Dauer, 2019) expect a potentially higher leak potential because of a different source follower bias, deviations in the manufacturing process, as well as an imperfect capacitive memory translation, were used. Since the simulation did not simulate the analog parameter storage, the leak saturation does not appear for this data. The simulation already forecasts input offsets of the source follower and the OTA, but in measurements this distribution expands significantly. The predestinated methodology is already in use for PPU-based calibration. Within the dynamic range of the leak voltage for calibration a linear relation between hardware parameter and observable seems to be a good assumption.

Reset voltage

The reset potential can be determined by forcing a reset and measuring the membrane potential during the refractory time. In terms of the claimed dynamic range, which is similar to the range of the leak potential and also noted in the green background of figure 14, the upper target was not hit by the majority of neurons. Due to the fact that leak potential and reset potential are designed symmetrically, the result of the reset potential measurement in figure 14 did not differ from the leak potential results. For this reason, figure 14 does not show results from HXv1. Unlike for the leak potential, deviations between measurement and simulation results became significant. Saturation and offset at the top and bottom areas of the measurement data were caused by the reasons previously described for the leak potential. As already discussed for leak potential, inside the dynamic range of each neuron a linear relation between hardware parameter and

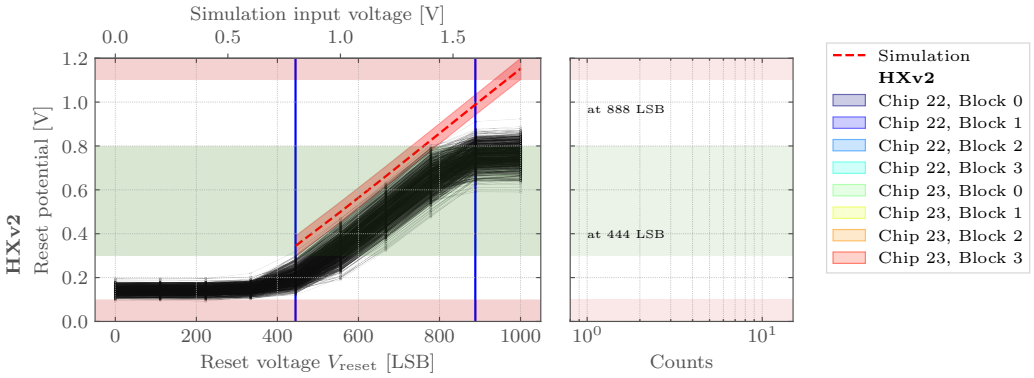


Figure 14: Measured and simulated reset potential on HXv2 with respect to the corresponding hardware parameter for chip 22 and chip 23. The green colored specifications are not satisfied for all neurons. The distribution of the measurements at 444 LSB and 888 LSB (marked by blue vertical lines) are shown in the histograms with respect to neurons and blocks.

observable is a good assumption for calibration.

Leak conductance

One fundamental measurement in this thesis was the measurement of the leak OTA's output current. An idealized OTA is given by

$$I_{\text{out}} = g(I_{\text{bias}}) \cdot (V_{+,\,\text{in}} - V_{-,\,\text{in}})\,, \tag{5.2}$$

with the transconductance $g(I_{\text{bias}})$. Since the input voltage $V_{-,\,\text{in}}$ figure 24 is connected to the OTA's output, a pseudo resistor is created.

Using the external sourcemeter, V_{m}, V_{leak} and I_{leak} were investigated. To reduce the measurement time to an acceptable level, only neurons 0, 4, 64, 124 and 127 on each block were analyzed. Unfortunately, due to technical issues, the responses for two neurons were lost.

Setting the leak potential per calibration on a certain voltage and clamping the membrane potential using the sourcemeter to another voltage, the sourcemeter measured the OTA's output current as illustrated in figure 15. For each leak potential and bias current, the

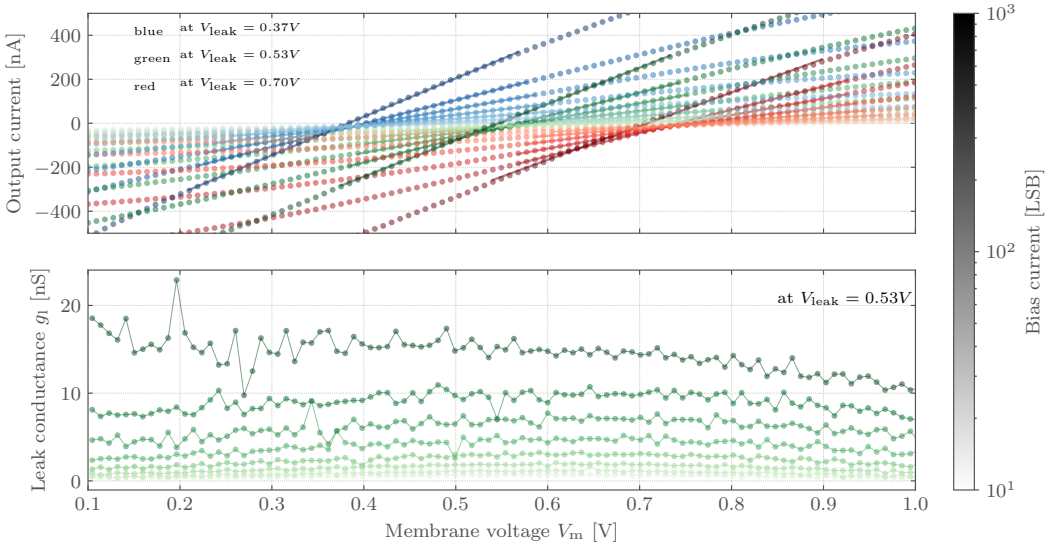


Figure 15: Characteristic curve of leak OTA's output with respect to the membrane potential V_m on chip 22, block 0 and neuron 0. The output current was measured for multiple leak bias currents I_{leak} (shown by brightness) and calibrated leak voltage potentials (shown by color). For the green leak voltage, its current's derivative with respect to the membrane potential V_m is shown in the lower plot.

trans-conductance g_l was given by the derivative of the output current with respect to the membrane potential (c.f. figure 15 lower plot).

Looking on an ideal OTA, the current crosses the x-axis where the membrane potential equals the leak potential and the output current slope is linear for all input voltages. The former can be described as an offset and is illustrated in figure 16b with respect to the leak bias current I_{leak}. Figure 16a shows the determined trans-conductance g_l. Due to offset currents, the uncertainty in measurement increased with decreasing bias current and the spread of the conductance band expands. The expanding on the upper end was probably caused by the diverging currents from the capacitive memory.

Even though biological models often describes the quantity of conductance, the membrane time constant is usually calibrated instead. This is justifiable by the complexity of the measurement method. A reverse calculation, when the capacitance is known, is given by equation (5.1).

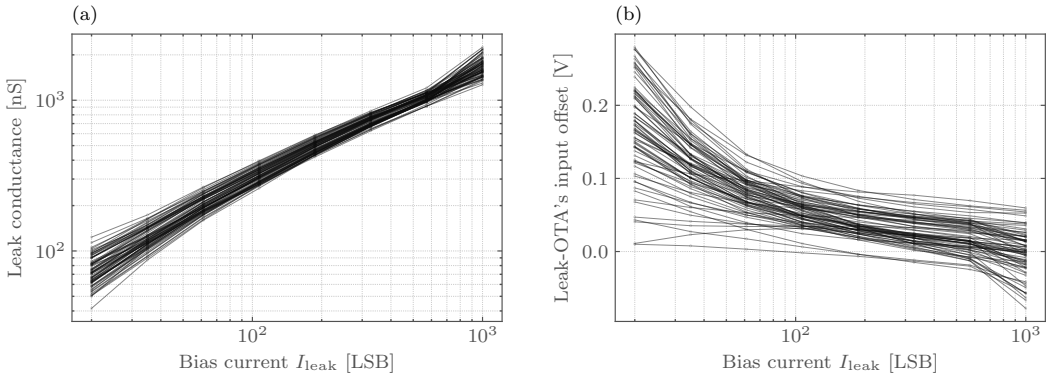


Figure 16: Leak OTAs. (Chip 22, Block 0-3, Neurons 0, 4, 64, 124, 127).
(a) Leak OTA's conductance with respect to the leak bias current.
(b) Lak OTA's offset with respect to the leak bias current.
For each neuron, all three measured leak voltages are drawn.

Membrane capacitance

When time constant and conductance of a leaky integrator are known, equation (5.1) gives the size of the corresponding capacitor. Designed for 2.40 pF, the manufacturing process related deviations and potential parasitic effects need to be estimated. Since for small bias currents leakage currents lead to high measurement uncertainties, g_l and C_m were investigated for a leak bias current of 1000 LSB. Averaging over three curves measured for different leak potentials (figure 15) the conductance was estimated. The determined values for chip 22 are illustrated spatially in figure 17. Two neurons are white due to missing data. Finally the averaged capacitance could be established to

$$\overline{C_\text{m}} = 2.39 \pm 0.16\,\text{pF},$$

with the uncertainty calculated for 18 neurons. A minimum of 2.08 pF and a maximum of 2.80 pF was measured. At some point, a further investigation of the capacitance's 6 bit adjustability could enable them to be calibrated.

Threshold voltage

The last component investigated in this section is the threshold comparator. The comparator gives an output signal when the membrane potential crosses the threshold potential. A reset signal is generated from this output. Unlike leak and reset potential the threshold

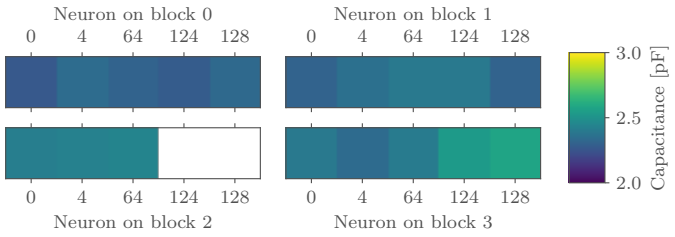


Figure 17: Spatial distribution of the neurons' capacitances on chip 22.

potential is not buffered by a source-follower.

In order to measure the threshold potential, multiple spikes were triggered and the maximum of the trace was extracted. Therefore strong excitatory synaptic input was enabled to push the membrane potential towards the threshold. For accelerating this process, a small leak conductance was adjusted. Assuming the leak term reliably and quickly pulls the membrane back to the reset potential when a spike or rather a reset is emitted by the comparator, this peak potential is a good estimate for the threshold. This method is limited by the lower limit of the reset potential because the reset needs to be under the threshold potential. Typically threshold potentials between 0.90 V and 1.10 V are used to maximize the dynamic range of the membrane potential.

Figure 18 shows the characteristic curve of the threshold potential. With the comparator implemented using thin oxide transistors, its range is limited to 1.2 V. Unfortunately, voltages above 1.1 V are not reliable resolved by the readout chain and MADC. At its lower end, the curves spread due to the limitations of the reset potential. For calibration purposes the used method is recommended. Inside the dynamic range of the threshold potential, a linear relation between hardware parameter and threshold potential seems to be a good calibration sufficient description.

Conclusion

Overall, nearly all specifications seems to be reached for a vast majority of neurons across blocks and chips. Nevertheless, the leak and reset potentials do not reach the upper specified limit. With the source follower in mind, a further investigation could reduce this issue. If not, changes to the design should be made for the next chip version.

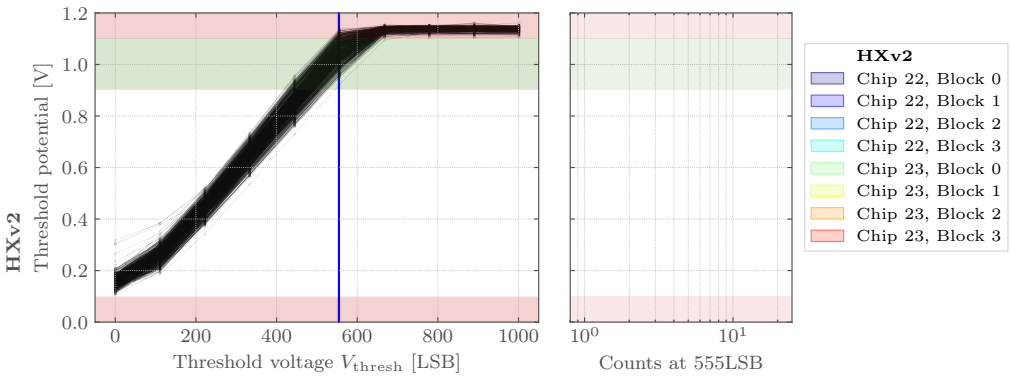


Figure 18: Measured threshold potential on HXv2 with respect to the corresponding hardware parameter for Chip 22 and Chip 23. The distribution of the measurements at 555 LSB (marked by blue vertical lines) are shown in the histograms with respect to neurons and blocks.

5.2 Synaptic Input

In HXv2 new circuits for a current-based synaptic input synaptic input was introduced by Sebastian Billaudelle. As illustrated in figure 10, inhibiting and exciting spikes have separated synaptic inputs. For further chip versions, it has been planned to also implement a conductance-based synaptic input.

Circuit description

Figure 19 shows an excitatory synaptic input because inhibitory and excitatory synaptic inputs are mostly symmetric. However, the OTA's inputs are inverted for an inhibitory synaptic input. The synaptic line I_{syn}, which connects all excitatory synapses of a column in the synapse array with the excitatory synaptic input of a corresponding neuron, drives an RC-circuit with resting potential V_{DD}. Each spike is a δ-shaped current pulse with a height proportional to the synaptic weight, that pulls the synaptic potential to a lower voltage. Considering the adjustability of the synaptic time constant, the resistor is realized as a pseudo resistor, whose bias current controls its conductance. To reliably reach time constants between 0.50 µs and 100 µs, this circuit has, similar to the OTA in the leak term, a digital switch to extend the conductance range by an additional high-resistance mode. Furthermore, another switch is implemented to further reduce the synaptic time constant τ_w, since the synaptic line itself represents a capacitor of reasonable size. This is not investigated in this thesis. An OTA is used to generate a current from the synaptic integrator's voltage. For an offset calibration this OTA, both OTA-inputs are buffered by tunable source followers. A digital switch between the OTA's output and the neuron's membrane allows to disable the synaptic input.

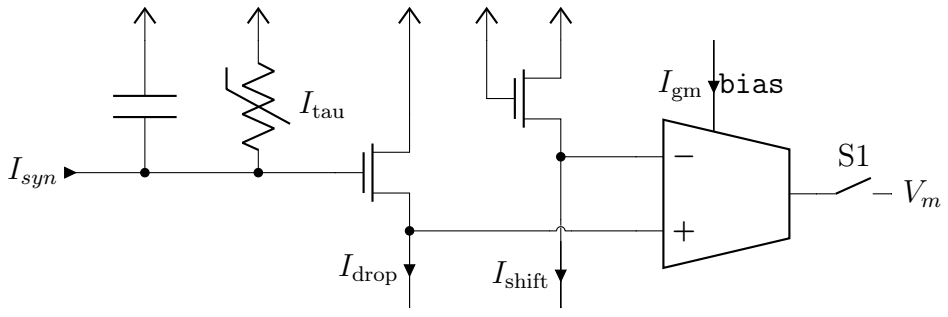


Figure 19: Schematic overview of excitatory synaptic input circuit. In the inhibitory synaptic input the OTA's inputs are inverted.

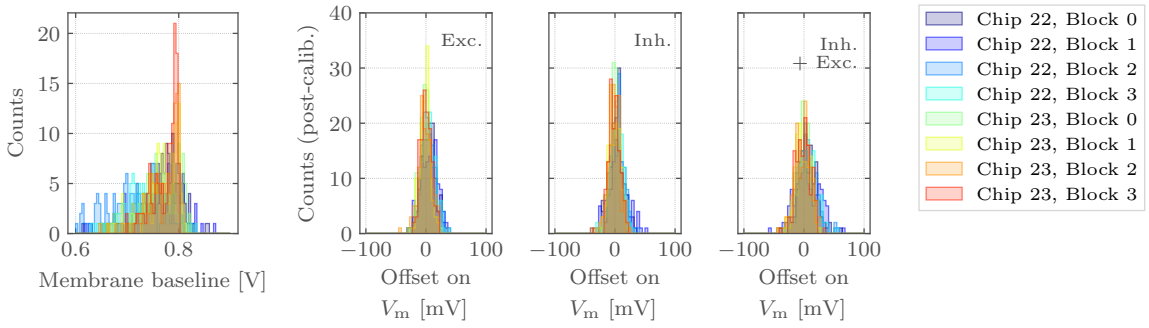


Figure 20: Post-calibrated membrane offset caused by the synaptic input. $I_{\text{gm}} = 700\,\text{LSB}$, $\tau_{\text{m}} = 10\,\mu\text{s}$

Offset compensation

To not affect the membrane with an offset current, the OTA's offset has to be calibrated for the inhibitory as well as the excitatory synaptic input. This service as a foundation for further measurements. Therefore the source follower bias currents I_{drop} and I_{shift} are introduced. I_{shift} was designed to set one of the OTA's inputs to a certain potential. For calibration I_{shift} needs be varied until the OTA's output is zero. The OTA's output current can be measured by disabling the spike comparator, setting the membrane time constant to a maximum and observing the membrane potential with reference to a baseline with disabled synaptic input. As for many neurons the dynamic ranges of I_{drop} did not satisfy for offset compensation, I_{shift} was additionally calibrated to extend the offset compensation range. In figure 20 the post-calibrated offsets are illustrated for enabling both inputs individually and simultaneously. For calibration purposes the used nested binary-search method on I_{drop} and I_{shift} is recommended.

Noise estimation

In HXv1, high levels of noise originating from the synaptic inputs were measured on the membrane. To quantify these perturbations on HXv2, the leak was configured for extremely long time constants by setting the bias current I_{leak} to 10 LSB and enabling the leak OTA's division mode. Due to the nearly disabled leak term it is expected to see Braunian-noise. This expectation can be deduced from the fact that random currents from the synaptic input cause a random walk on the membrane potential. The membrane potential was then digitized for durations of 100 ms and the standard deviation of these

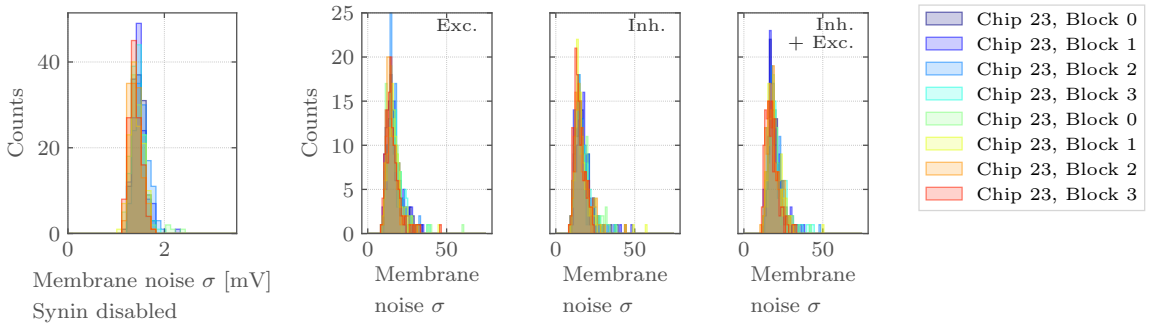


Figure 21: Membrane noise caused by the synaptic input. $I_{\mathrm{gm}} = 700\,\mathrm{LSB}$, $I_{\mathrm{leak}} = 10\,\mathrm{LSB}$, τ_{m} division mode enabled.

traces were extracted (figure 21). This was repeated for disabled and individually enabled synaptic inputs as well as for the case of both input circuits being enabled.

Synaptic time constant

The synaptic time constant is given by the digital mode and the bias current of the pseudo resistor. Generally the synaptic time constant can be determined either by looking on the exponential decay of an input spike on the synaptic integrator potential or by fitting the resulting PSP on the neuron's membrane. Since the latter is based on unstable fits, the former was used for measuring the synaptic time constant. In further investigations it would also be interesting to measure the membrane as well as the synaptic time constant by fixating the fit parameters for the PSP as far as possible.

Figure 22 illustrates the results measured on the synaptic line for the inhibitory and excitatory synaptic input with and without the high-resistance mode enabled and with respect to the bias current. At the upper end of the bias currents, the time constant bands spread due to the diverging currents of the capacitive memory. Furthermore the diverging on the lower end of the bias currents is caused by unstable fits for long time constants and, more importantly, by the diverging currents of the analog parameter storage as investigated in section 4. For all neurons the specification to reach inhibitory and excitatory time constants between 0.50 µs and 100 µs was achieved.

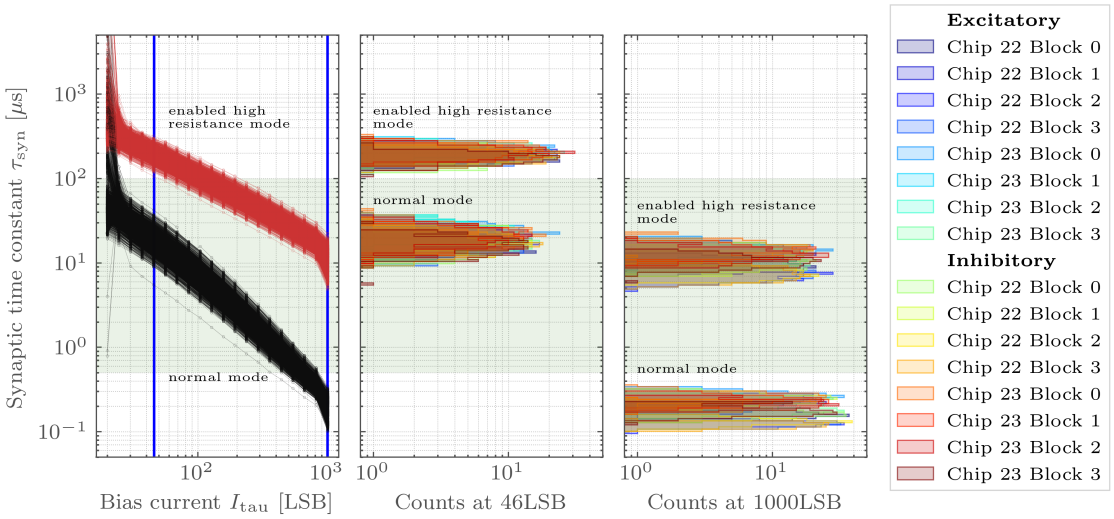


Figure 22: Measured inhibitory and excitatory synaptic time constants on HXv2 for the normal and high-resistance mode on chip 22 and chip 23. This corresponds to 2048 lines per mode. The distribution of the measurements at 48 LSB and 1000 LSB (marked by blue vertical lines) are shown in the histograms with respect to modes and neuron blocks.

Synaptic linearity

The OTA biased by I_{gm} needs to be tested for its linearity. PSP amplitudes corresponding to different weights of incoming spikes were determined for the synaptic line as well as for the membrane. Therefore the synapses of 64 synapse array rows are configured to enumerate the 64 possible synapse weights. To realize weights greater than 63, multiple synapse drivers are used simultaneously, e.g. for weight 70 the synapse driver for the synapse row configured to a weight of 63 fire together with the one configured to a weight of 7. This method is similar to the super-synapses algorithm used for the insect navigation experiment by Korbinian Schreiber (Billaudelle et al., 2019b).

In this analysis, the PSPs were characterized by their absolute amplitude and not by the fit of the analytical solution of the differential equations to the membrane and synaptic line traces. This was found to be a much more stable method, even if it does not investigate the time constants of the synaptic input and of the membrane. Figure 23 illustrates the amplification for a single neuron in the center of the first block on chip 22.

The synaptic line is specified until a maximum voltage drop of 0.20 V. Here a linear increase with respect to the weight of the input is expected.

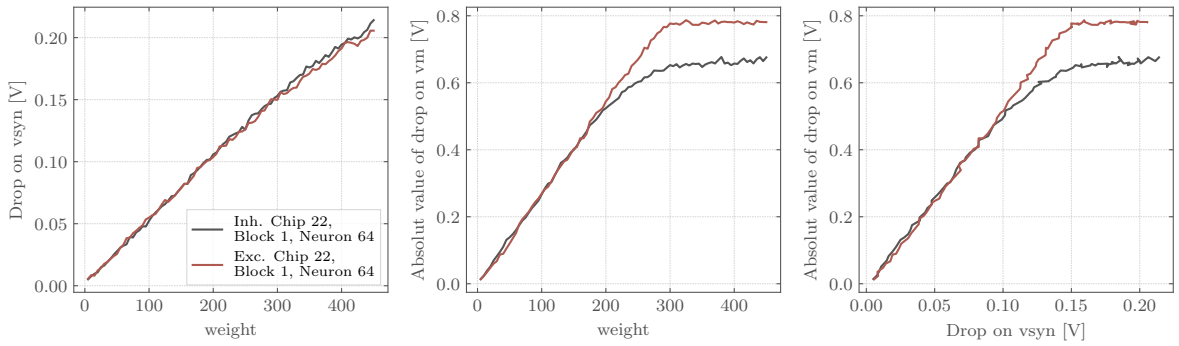


Figure 23: Measured voltage drops caused by spikes on the synaptic line and on the membrane for a single single neuron. The right plot represents the amplification factor of the OTA with respect to its input voltage.

However, this measurement was highly influenced by the differences in the synapse drivers, synapses and timing of the spikes. Due to this reason, a quantitative investigation of the linearity was not constructive. Beside the named issues, the synaptic line seems to be linear in terms of a qualitative observation.

All amplitudes of PSPs on the neuron membrane are limited by the dynamic range of the membrane. To maximize this usable dynamic range, for the inhibitory input the leak potentials were set to approximately 0.80 V, while for the excitatory input they were fixed to circa 0.30 V. The saturation in the absolute values of the amplitudes fits well to the expected dynamic range of the membrane.

A membrane time constant of to approximately 15 µs and a synaptic time constant of approximately 5 µs was configured. Qualitatively, the absolute amplitude of the PSPs on the membrane increases linearly with the synaptic weight (c.f. middle plot in figure 23), and even more with respect to the amplitude on the synaptic line (c.f. right plot in figure 23) demonstrating the linearity of the OTA. An overview on all synaptic inputs is given in appendix figure 35.

Some neurons or even complete neuron blocks showed a non-linear behavior on the synaptic line. Probably, this was related to a different timing of input spikes, when multiple synapses were used. Furthermore, in some neuron blocks neurons the membrane potential did not response to PSPs as expected. Due to time constrains, this issues were not investigated further.

Conclusion

Overall the synaptic input benefits from the redesigned circuits. Especially the offset compensation exhibits reasonable results. Also the noise on the membrane caused by the synaptic input is reduced in HXv2 compared to HXv1, where previously random jumps in the membrane potential occurred. The time constants reaches their specification for all tested 1024, neurons inhibitory as well as excitatory. A further investigation on the synapse arrays and PSPs is needed as described.

5.3 Adaptation term

One of the most significant changes between HXv1 and HXv2 are the new designed adaptation and exponential circuits. Developed by Sebastian Billaudelle, linearity and ranges of the circuits are improved. A main benchmark was given by the reproduction of firing pattern suggested by Naud et al. (2008) and simulation showed, that this benchmark is hard but achievable (Dauer, 2019). However, the specification ranges in this section were inspired by this pattern. The following section will investigated the parameters of this new adaptation circuits.

Circuit description

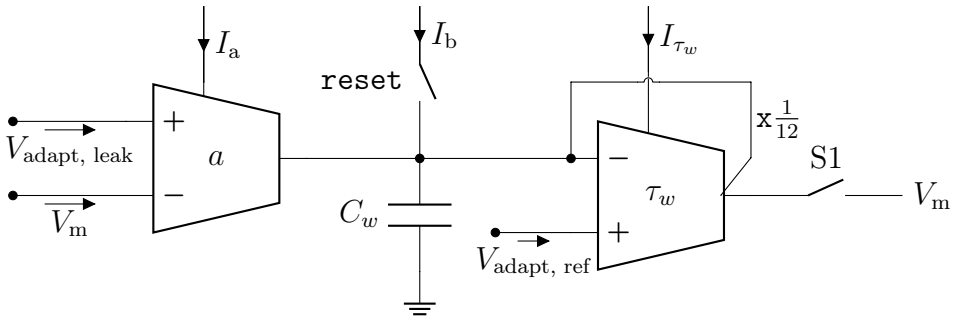


Figure 24: Schematic overview of the adaptation circuit. For realizing negative values for the parameter a and b in equation (2.2), the a-OTA's inputs as well as the current I_b the can be inverted. The voltages $V_{\mathrm{adapt,\ leak}}$ and $V_{\mathrm{adapt,\ ref}}$ are buffered by source followers dropping these voltages around about 0.70 V.

As given in equation (2.2), the adaptation term is based on an additional state variable w, which in the circuit is stored as a voltage on a leaky integrator. Like the leak term, this leaky integrator is represented by a RC-circuit realized by an OTA with negative feedback and a capacitance C_w. In figure 24 this OTA is named τ_w and provides two different output stages, one stimulating the neuron's membrane V_m and another for the feedback loop. This feedback loop is designed to be 12 times weaker then the V_m-output, which allows long time constants τ_w. The resting potential $V_{\mathrm{adapt,\ ref}}$ of the adaptation state w can be controlled independently from the membrane's leak potential to maximize the dynamic range available for the adaptation state w. The leaky integrator's input in sub-threshold regime is given by the difference of leak potential and the membrane potential scaled by a factor a. This is implemented by the a-OTA, biased with I_a. Since the OTA's behavior can not inverted by e.g. simply inverting the bias current, a not drawn

switch can invert the a-OTA's inputs. Finally, an also invertible current I_b together with an adaptation-pulse-switch realize the spike-triggered adaptation. The height and the length of this pulse controls the charge that is added to the adaptation state. Since the adaptation state variable w is not implemented as current but as voltage, the charge manifests itself as an increment of Δv_b on w. All circuits can be disabled by a switch disconnecting the adaptation term from the neuron's membrane.

Input offset compensation

As described, the a-OTA compares the membrane potential to the leak potential. Since OTAs always have an input offset, the adaption leak potential $V_{\mathrm{adapt,\,leak}}$ is not equal to the membrane leak potential V_leak, but allows to counteract that OTA-specific offset. The adaptation state's baseline is determined by the τ_w-OTA and can be controlled by $V_{\mathrm{adapt,\,ref}}$. Without calibration, the input offset of the τ_w-OTA leads to a spread of the baseline potential by $\pm 135\,\mathrm{mV}$ at $V_\mathrm{leak} = 500\,\mathrm{LSB}$. Nevertheless, it needs to be mentioned, that this target spreads between approximately $0.30\,\mathrm{V}$ and $0.80\,\mathrm{V}$ and causes very different dynamic ranges for adaptation states.

The input offset of the a-OTA was calibrated by using a binary search algorithm for four different leak voltages V_leak. Figure 25 shows the post-calibrated offset of the adaptation state caused by the a-OTA. The histograms show a clear clustering of values around the target value. However, a small number of neurons ($5.86 \pm 0.02\,\%$) could not be successfully calibrated for all four investigated V_leak values. This was probably caused by the fact that the membrane leak potential V_leak was not calibrated before optimizing the a-offset, which then had to account for both, the leak term's as well as the a-OTA's input offset. As the leak voltage is usually calibrated, this measured offset show a worse-case scenario which is expected not to occur for a fully calibrated system.

Further, it is interesting, whether the offset changes with respect to the membrane potential or, in the investigated case, with respect to the membrane leak voltage. In principle, it would be necessary to calibrate the offset by a binary search for every single leak voltage setting. Nevertheless, to speed up calibration, the offset compensation was linear extrapolated for arbitrary leak potentials. Taking into account that the outliers were not removed before fitting and that only four data points were recorded in the first place, this method yielded sufficient results for all further investigations of the adaptation term.

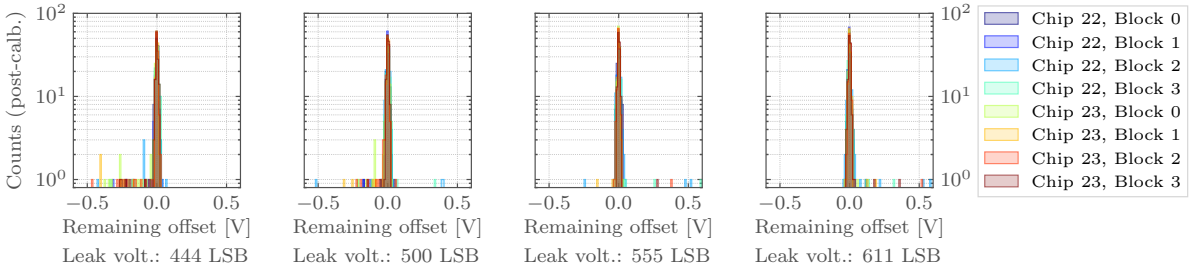


Figure 25: Adaptation-a offset calibration and corresponding adaptation state potential w with respect to four different leak potentials for chip 22 and chip 23. The leak potential is limited by the ranges needed for offset compensation of the a-OTA. Due to the uncalibrated adaptation reference voltage, the adaptation state potential is widely spreaded.

However, for future use, it is recommended to improve the extrapolation or to determine the corresponding.

When the a-OTA's inputs are inverted to realize negative sub-threshold adaptation strength, the offset compensation is invalid and needs to be done again. Even this state is used for some firing pattern (Naud et al., 2008), it is not further investigated in this thesis since its method an results are similar to the non-inverted calibration.

Adaptation time constant

The adaptation time constant τ_w is the third and last time constant, which is investigated in this thesis. Like for the time constants of the other leaky integrators, an input stimulus shifts the integrator's state variable. Fitting the state variable exponentially, when it relaxes back to the integrator's baseline potential determine the time constant. For the adaptation time constant τ_w this shifting is realized by using spike-triggered or more precisely reset-triggered adaptation pulses. Therefore, the spike-triggered adaptation current is set to its maximum. Unlike the other leaky integrators, the OTA representing the conductance of this RC-circuit has no switches to enlarge the time constant's range. The adaptation time constant τ_w is typically larger as the membrane time constant τ_m to introduce a different time scale for sub-threshold adaptation. Hence it was designed to cover at least the range of 50 µs to 300 µs used to reproduce AdEx firing pattern (Naud et al., 2008).

In figure 26 the measured an simulated time constants are illustrated. Due to the use

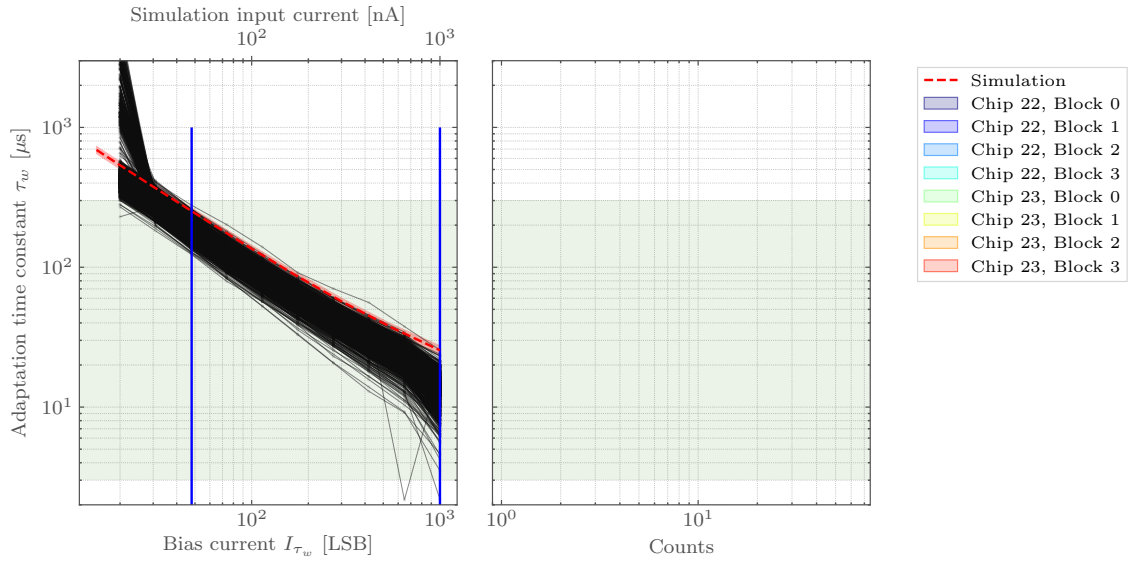


Figure 26: Measured adaptation time constant τ_w with respect to the bias current I_b on HXv2 on chip 22 and chip 23. The distribution of the measurements at 48 LSB and 1000 LSB (marked by blue vertical lines) are shown in the histograms with respect to different neuron blocks.

of the spike-triggered adaptation, which, as discussed later, had shown unreliability, this measurement was afflicted with uncertainties. The spread at small bias current is caused by almost one block on chip 23, which analog parameter storage's offset was overcompensated even for a minimum value of the corresponding offset bias current. Hence this block provides a nearly zero output at 20 LSB. For large bias currents, the measurements spread as well, due to the mentioned diverging currents of the analog parameter storage for digital values greater 800 LSB (c.f. section 4). However, the measured and simulated values differ significantly and the simulation is always slower then the measured time constants. This can be due to many reasons, e.g. a slightly different doping of the silicon or a systematic mismatch of the capacitor models. Nevertheless, nearly all neurons reach the specifications.

For automated calibration purpose, again a power function of the minus fourth degree seems to be a good prediction. How to calibrate the adaptation time constant on the PPU needs to be further investigated.

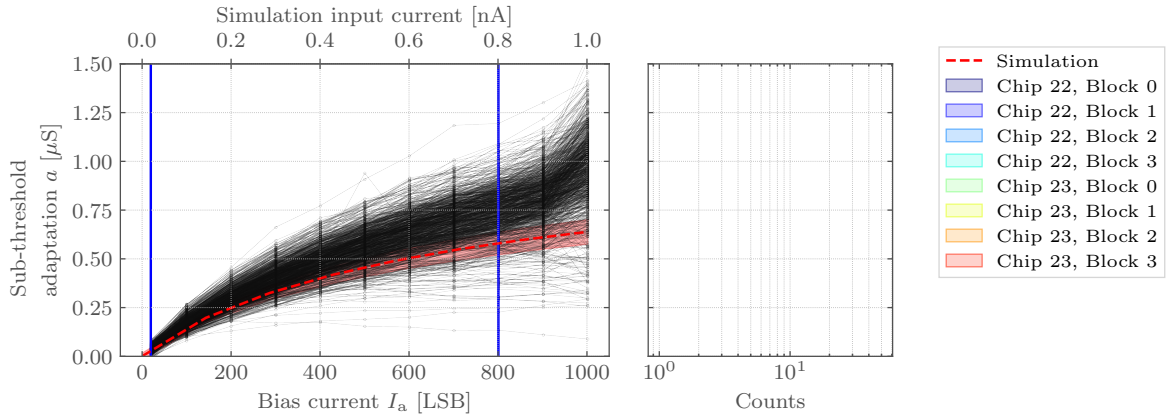


Figure 27: Measured sub-threshold adaptation a with respect to the bias current I_a on HXv2 on chip 22 and chip 23. The distribution of the measurements at 20 LSB and 1000 LSB (marked by blue vertical lines) are shown in the histograms with respect to different neuron blocks.

Sub-threshold adaptation

Next, the non-inverted sub-threshold adaptation is measured. Measuring the voltage shift on the membrane potential caused by a current-step-stimulus with (Δ_a) and without (Δ) sub-threshold adaptation enabled, the non-inverted sub-threshold adaptation $a \geq 0$ is given by

$$a = g_\mathrm{l} \cdot \left(\frac{\Delta}{\Delta_a} - 1 \right) \tag{5.3}$$

(Kriener, 2017). On HXv2, the offset currend generator was used to produce the required current step function. It became apparent, that the choosing the time constants and leak potentials has a huge impact on the measurement's quality. The latter is probably caused by a saturation of the adaptation state variable. As a good estimate, the membrane time constant was calibrated to 5 µs, the leak potential to 0.50 V and I_{τ_w} was set to 200 LSB which corresponds to an adaptation time constant τ_w of approximately 5 µs.

Figure 27 shows the measurement and simulation results with respect to the a-OTA's bias current. Neurons, that does not reach strong sub-threshold adaptation probably saturated in their adaptation state variable w. Even it concerns only a few neurons, their sub-threshold adaptation are widely spread. A divergence of the sub-threshold strength

at 1000 LSB is caused by the divergence of the capacitive memories output currents. Nevertheless, the measurements of the sub-threshold adaptation show a significant stronger sub-threshold adaptation for bias greater than 500 LSB as simulated by Dauer (2019). Since they meet at zero bias, this does not reduce the performance of the circuits, it even increases the usable range. This systematic effect – as well as the large spread – could be caused by the propagation of errors for quantities from equation (5.3), e.g. the leak conductance g_l, which is inferred from the time constant τ_m and hence influenced by deviations of the membrane capacitance C_m.

As illustrated, the measurement method does not necessarily produce smooth lines, not even monotonic ones. Since there is no reason for this, it can be assumed that the used method is not optimal. For non-monotonic functions, it is not possible to use a binary search for calibration. Due to this, the used routine needs to be improved.

As tested for simulation data, a fourth order polynomial seems to be a good representation of the data.

Spike-triggered adaptation

A spike-triggered adaptation mechanism is implemented by a short reset-triggered current pulse on the adaptation state variable w. This pulse charges the adaptation capacitance C_w, which results in a voltage jump Δv_b. Further, the sub-threshold adaptation strength is given by

$$b = g_\mathrm{adapt} \cdot \Delta v_\mathrm{b}. \tag{5.4}$$

The adaptation conductance g_adapt is given by the adaptation time constant and the assumed adaptation capacitance C_w of approximately 2 pF. For negative spike-triggered adaptation $b < 0$, a switch allows to invert its input current I_b. Since inverted and not inverted spike triggered adaptation is rather similar, the inverted spike-triggered adaptation was not investigated in this thesis.

Since the absolute value of b was not of special interest, because it can be directly inferred from the former, only Δv_b was measured. First, a reset was programmed to activate the spike-triggered adaptation. Then, the rising edge of the was measured by the MADC to extract the voltage w before and after the pulse appears. Unfortunately, it was observed that the pulse length is not stable through different experiments and not even for multiple resets in the same experiment (c.f. appendix figure 36). The measured pulse length was significantly lower in 50 % of the spikes.

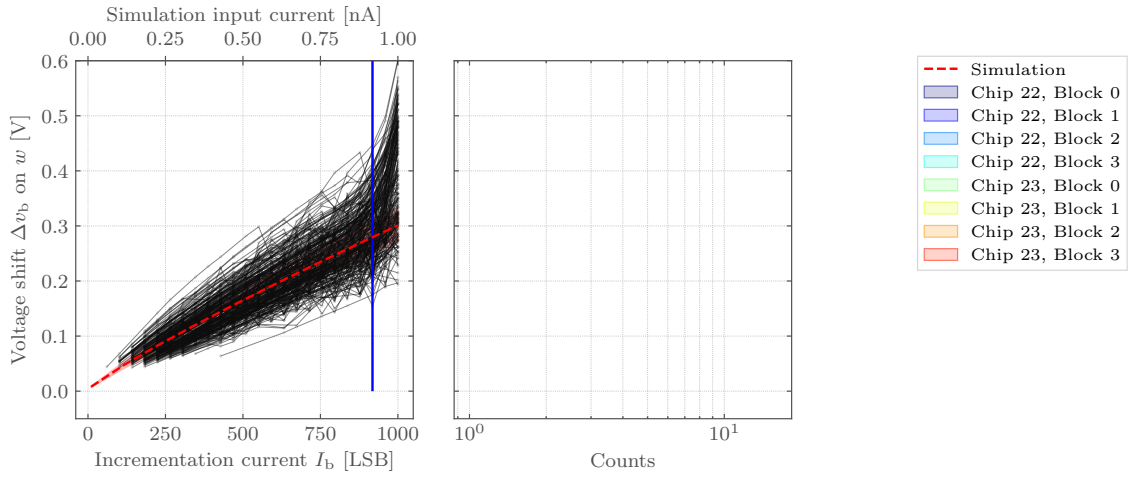


Figure 28: Measured spike-triggered adaptation b with respect to the input current I_b on HXv2 on chip 22 and chip 23. The distribution of the measurements at 918 LSB (marked by blue vertical lines) are shown in the histograms with respect to different neuron blocks.

A certain timing uncertainty is expected, since here analog time-continues circuits are driven by digital clock-driven digital logic. However, a short adaptation pulse results in a smaller charge on the capacitance and a smaller related voltage drop. So far this problem is not understood, but assumed to be localized within the neuron backend.

Further, to investigate the neuron's analog circuits, not only Δv_b but also the pulse length was measured. The latter was defined by the duration between the first and last ADC sample, which an derivative greater than 0.05 V/µs.

Figure 28 still tries to visualize the dependency of Δv_b on the configured current. For this purpose, outliers, defined as pulses with a width smaller then 0.50 µs were removed. In the course of this method, unfortunately also small Δv_b-values corresponding to small input currents were removed. Even this removing of invalid values did not catch all adaptation pulses with a incorrect length, its result allowed to estimate the characteristic curves of the spike triggered adaptation.

Ignoring the neuron backend related timing issue, the measured voltage jumps fit nicely the simulation. Just the spread was much wider and, again the divergence at high input currents was caused by the analog parameter storage.

For calibration purposes, a b_{target}-corresponded target $\Delta v_{\text{b, target}}$ can be calculated by

$$\Delta vb_{\text{target}} = \frac{b_{\text{target}}}{g_{\text{adapt}}} = \frac{b_{\text{target}}}{12 \cdot g_{\tau_w}} = \frac{b_{\text{target}} \cdot \tau_w}{12 \cdot C_w}, \tag{5.5}$$

where the g_{adapt} and g_{τ_w} describe the two coupled outputs of the τ_w-OTA (Dauer, 2019). Since the removing of invalid values, on the one hand, bases on a calculated derivative and, on the other hand, is partly non-monotonic due its imperfection, it can not be used on the PPU and even not combined with a binary search. However this method running on a host computer could be a workaround for calibrating the spike triggered adaptation. Furthermore, simulations had shown, that a polynomial of second order seems a good representation of the data.

Conclusion

In terms of the adaptation term, the a-OTA's input offset, the adaptation time constant, the sub-threshold and spike-triggered adaptation were investigated. The analog part of each parameter was tested to majorly reach the given specifications. Nevertheless, the inverted parameters were not characterized, since they are almost symmetrical. It needs to be mentioned, that the spike-triggered adaptation shows the expected behavior in 50 % of the cases and therefore needs to be marked as highly unstable. At this point it a configuration error can not be ruled out. Further investigations are required to pinpoint the issues origin.

5.4 Exponential term

The exponential term integrates a smooth threshold into the AdEx neuron. Unfortunately, the former circuit design did not satisfy the parameter ranges required for AdEx firing pattern, even in simulation (Kriener, 2017). Also the two parameters of the model, the slope factor Δ_T and the threshold V_T, could not be controlled individually. For HXv2, Sebastian Billaudelle developed a new exponential term circuit, that shall remove this issues. The following section will investigate their behavior.

Circuit description

Figure 29 illustrates the exponential term circuit. Using a bulk-driven OTA combined with an active load M2 as input stage of the NMOS-transistor M1, biased in it's sub-threshold regime, this transistor's drain-source-current is proportional to the exponential of the difference between the OTA's inputs.

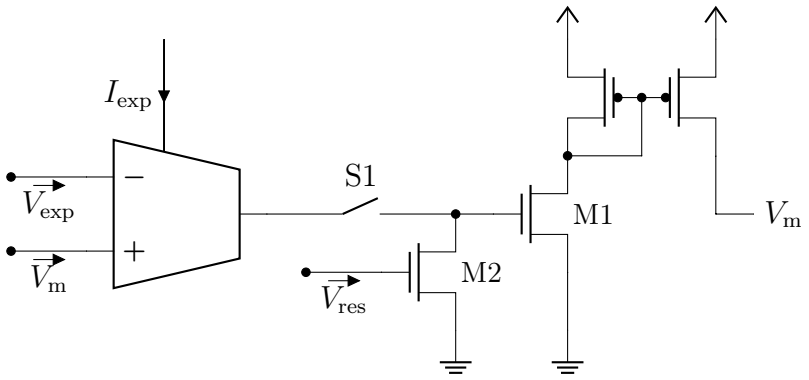


Figure 29: Schematic overview of the exponential term circuit.

Transistor M2, controlled by V_{res}, is biased in its linear regime and further – as a pseudo-resistor – transforms the OTA's output current into a linear voltage, which is then is applied to the gate of M1. In limits, it's mismatch only affects the output current as an additional factor in the output current's exponent. For disabling the exponential term's circuit, the switch S1 allows to disable the output stage of the circuit.

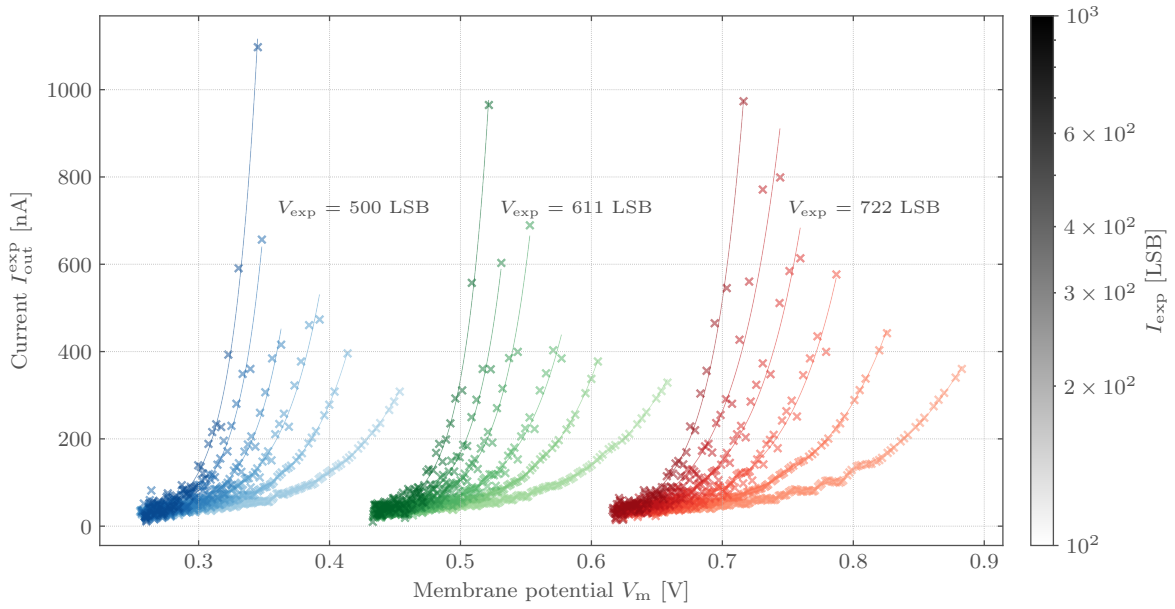


Figure 30: Extracted exponential term's output current $I_{\text{out}}^{\text{exp}}$ with respect to the reference voltage V_{exp} (color) and the bias current I_{exp} (brightness) for neuron 4 on block 0 on chip 22. The continuous lines are calculated from a fit (equation (5.7)).

Measurement protocol

Since the exponential term's output is given by the current $I_{\text{out}}^{\text{exp}}$, it's direct measurement would require a sourcemeter. Due to the fact that during the thesis the on-chip sourcemeter was not usable and the used measurement routine was preferred to operate without external devices, a transient measurement of $I_{\text{out}}^{\text{exp}}$ was chosen. Hence this current was provoked by a constant current stimulus. Therefore the membrane potential increased nearly linearly until the exponential term took effect and dominated the further increase up to the threshold potential. To extract the exponential term's output current $I_{\text{out}}^{\text{exp}}$ from membrane trace V_{m}, the capacitor equation

$$I = C_{\text{m}} \cdot \frac{\mathrm{d}V_{\text{m}}}{\mathrm{d}t} \tag{5.6}$$

with an assumed and constant capacitance $C_{\text{m}} = 2.40\,\text{pF}$, was used. This measurement was repeated for different configurations of the bias current I_{exp} and the reference voltage V_{exp}.

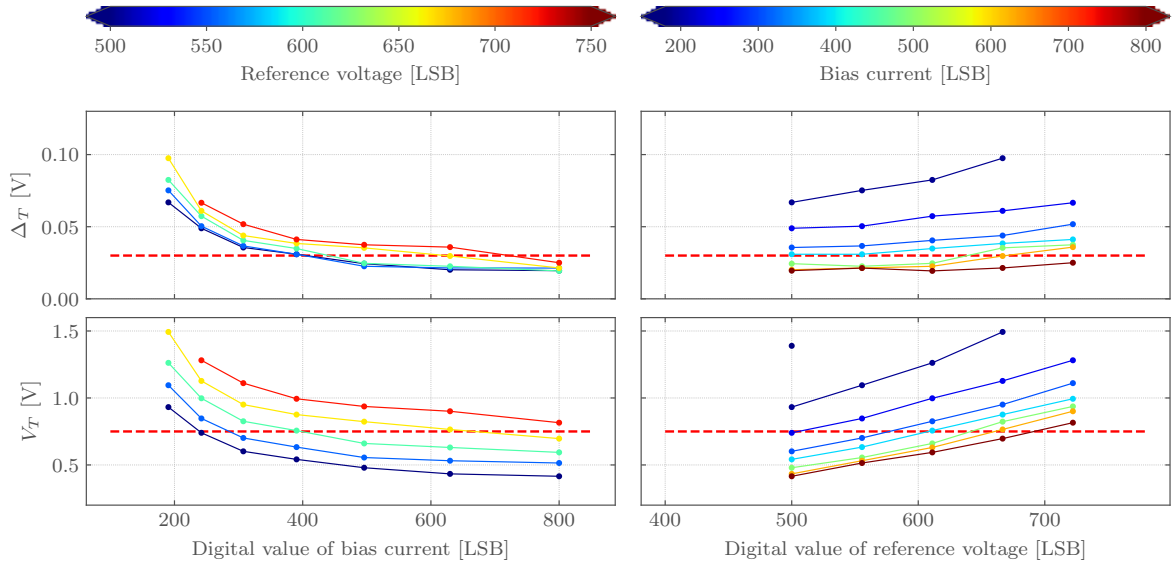


Figure 31: An exemplified exponential term measurement on HXv2, chip 22, block 0, neuron 4. Illustrating the parameters Δ_T and V_T for the biological model with respect to the OTA's reference voltage and bias current.

The crosses in Figure 30 illustrates these extracted current that contains the exponential currents but might also include leakage currents, which would have to be absorbed in a suitable fitting function. Here, it was assumed that all other neuron's components affecting the membrane were fully disabled and hence the extracted currents were fitted by the AdEx equation's exponential term

$$I_\mathrm{out}^{exp} = g_\mathrm{l} \cdot \Delta_\mathrm{T} \cdot \exp\left(\frac{V_\mathrm{m} - V_\mathrm{T}}{\Delta_\mathrm{T}}\right) = \exp\left(\frac{V_\mathrm{m} - \tilde{a}(\Delta_\mathrm{T}, V_\mathrm{T}, g_\mathrm{l})}{\tilde{b}(\Delta_\mathrm{T})}\right) \tag{5.7}$$

which is also shown by continuous lines in figure 30. The parameters $\tilde{a}$ and $\tilde{b}$ correspond to a more direct but equivalent description of the circuit and are linked individually to the bias current I_exp or the reference voltage V_exp (Dauer, 2019). Even the latter description is useful for calibration purpose, the former was used during this thesis to illustrate configurable parameter ranges in the model's quantities.

For the same neuron, investigated in figure 30, all measured dependencies are shown in figure 31 including more data points. The dotted red lines represent a calibration target equivalent to a biological settings of $V_\mathrm{T} = -50\,\mathrm{mV}$ (bio) and $\Delta_\mathrm{T} = 2\,\mathrm{mV}$ (bio) required to reproduce AdEx firing patterns (Naud et al., 2008).

With $\Delta_T \sim \tilde{b}$ in mind, Δ_T with respect to the bias current I_{exp} behaved as expected. It's remaining dependency on the the reference voltage V_{exp} are illustrated upper right plot. It is expected to see constant, horizontal lines with distances that are scaled logarithmically.Especially for an increasing reference voltage I_{exp} or a decreasing bias current I_{exp}, the measurements differed from this expectation. This could be caused by a cross-dependency of the OTA's transconductance on the input common-mode, or more precisely by the reference potential. However, since such a behavior was not observable in simulation and the used routines so far assumed the absence of leakage currents, a more thorough analysis is expected to yield better results.

Since V_T is composed of I_{exp}, V_{exp} and g_l, it is hard to extract evaluations from this parameter using the naked eye. Further, V_T with respect to the bias current I_{exp} is shaped exponentially and with respect to the reference voltages V_{exp} almost linearly. This linearity of V_T with respect to V_{exp} is also shown in the lower right plot.

Exponential term slope factor Δ_T

As mentioned in the circuit discussion, a transistor M1, biased in it's sub-threshold regime, is used to generate an exponential dependency. In this biasing regime, transistors are especially prone to variations in the manufacturing process which manifest themselves as fixed-pattern noise. To quantify such deviations between neurons the exponential measurement's routine were applied to all 1024 neurons on chip 22 and chip 23. On the one hand, due to technical issues and time constraints and, on the other hand, due to unstable initial guesses for the fit algorithm, only a subset of neurons are shown in figure 32. For a clear arrangement, this ended up in two slices of data, such that the left plot respects only a single reference voltage configuration and the right plot only a single bias current configuration. Both slices were chosen by taking the red dotted target into account.

As already mentioned in figure 31 with respect to a single neuron and multiple reference voltage values, also in figure 32 but with respect to different neurons and only a single reference voltage significant variations from the expectations were observed. All shown neurons crosses the target and hence the exponential terms of all this neurons seems to allow to configure their slope factor towards this supposed target.

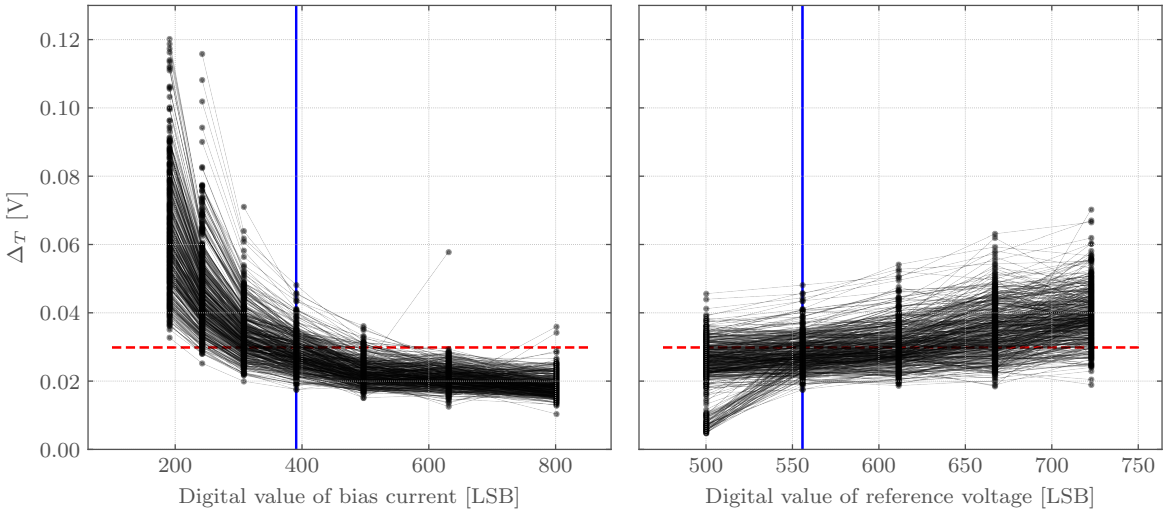


Figure 32: Exponential term's slope factor Δ_T for 455 neurons on chip 22 (block 0 almost completely) and chip 23 (block 2 and 3; block 1 almost completely) with respect to the bias current and the reference voltage.
(left): Reference voltage: 556 LSB.
(right): Bias current: 390 LSB.

Exponential term threshold V_T

For the same reasons discussed for Δ_T and furthermore because the exponential term threshold V_T depends on multiple hardware parameters, the fixed-pattern noise on V_T needed to be investigated. Figure 33 shows, very similar to figure 32, a subset of the acquired data. As previously discussed, in both cases the not swept parameter was chosen, by taking the target given by Naud et al. (2008) into account.

The linearity of V_exp with respect to the reference voltage V_exp is clearly visible. Nevertheless, the wide distribution of the curves offsets' is expected due to the discussed fixed-pattern noise. Also for V_T almost all shown neurons cross the red dotted target value. Further, the very few outliers seems to hit the target by a small extrapolation of reference voltages.

Conclusion

These measurements primarily have shown that it is possible to extract the exponential term's model parameter Δ_T and V_T from membrane traces using the MADC. Further, the

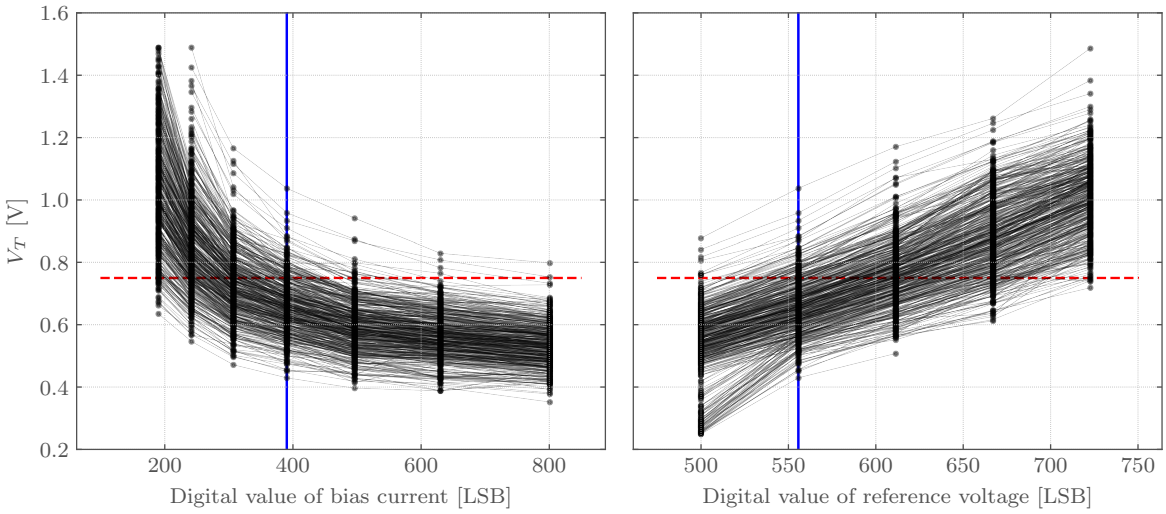


Figure 33: Exponential reference voltage V_{T} for 455 neurons on chip 22 (block 0 almost completely) and chip 23 (block 2 and 3; block 1 almost completely) with respect to the bias current and the reference voltage.
(left): Reference voltage: 556 LSB.
(right): Bias current: 390 LSB.

measured results led to the assumption, that the exponential term can be configured to the target values required to reproduce various AdEx firing patterns. Nevertheless, the fit routines and initial guesses can be improved to yield more reliable results.

6 AdEx firing pattern

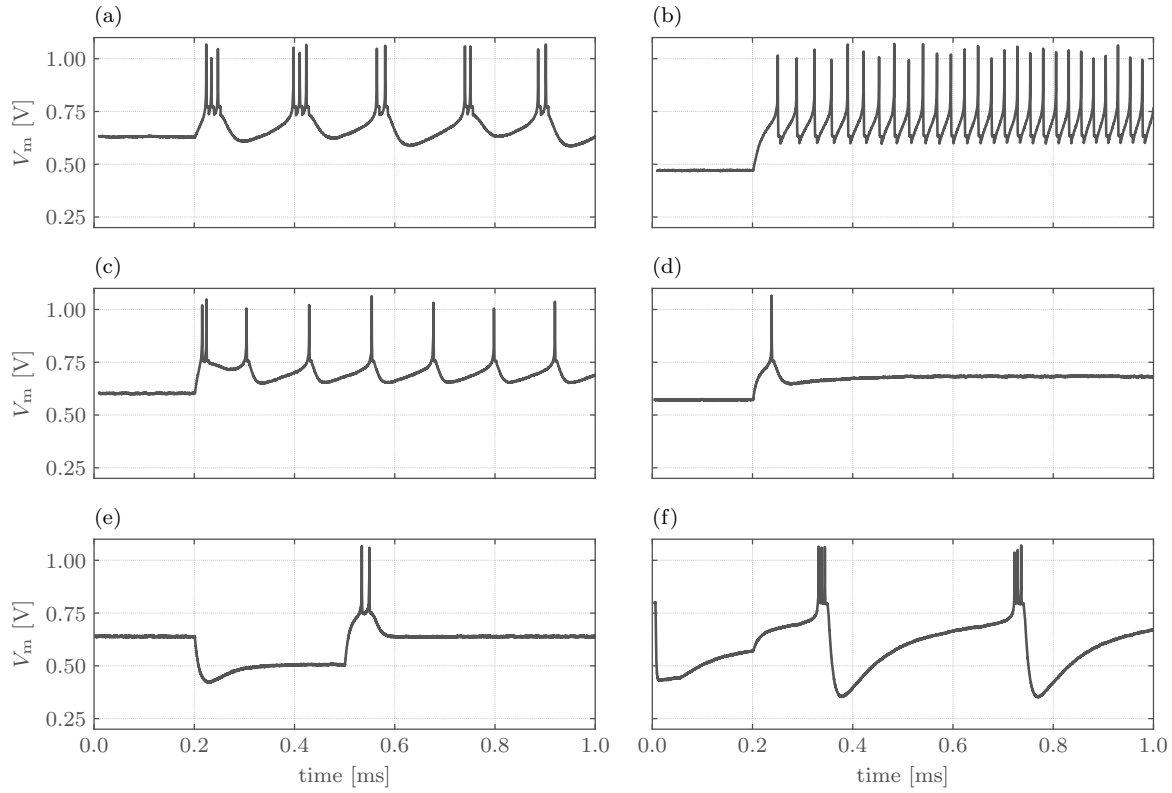


Figure 34: Neuron membrane traces for AdEx firing pattern on chip 22, block 0, neuron 4 inspired by the firing pattern suggested by Naud et al. (2008).
(a) regular bursting, (b) delayed spiking and acceleration, (c) initial bursting, (d) transient spiking, (e) inhibitory rebound, (f) delayed regular bursting.
Parameters given in appendix table 5.

The AdEx model allows to emulate biologically inspired firing patterns. Since they cover a wide area of the model's phase plane, the firing pattern suggested by Naud et al. (2008) were chosen to benchmark the ASIC. Figure 34 shows exemplary membrane traces for measurements on HXv2. Due to time constraints, the shown collection of firing patterns only demonstrates measurements on a single neuron. A basic routine was used to calibrate the leak term and $V_{\text{adapt, leak}}$ automatically, but all other parameters were configured by hand. Due to leakage currents from the adaptation term, a post-calibration of the leak voltage was required.

For almost all tested pattern, a rather stable hardware parameter set was found. These parameters showed a reasonable invariability regarding small changes and yielded a re-

produce behavior. However, the discussed adaptation-pulse-length related bug can be observed, when spike-triggered adaptation is enabled. When the adaptation pulse did not reached its full length, the adaptation state was not fully incremented and probably sometimes causing unexpected spike bursts. With inverted sub-threshold adaptation enabled, a positive feedback loop was established, which can already become an issue in numerical simulations. Within this highly unstable situation, as e.g. given in the pattern *delayed regular bursting*, often a continuous high frequently spiking neuron was observed. To prevent this unwished continuous spiking behavior, a forced reset in combination with an enabled leak multiplication at the beginning of each experiment was implemented to inhibit the membrane potential V_{m} as well as the adaptation state w. With this forced initialization, even such unstable firing pattern was reproduced

Overall, all tested firing pattern were reproducible with the HXv2 hardware.

7 Discussion and Outlook

Within this thesis, the analog parameter storage and the analog neuron circuits of HICANN-X v2 were investigated. For this purpose, new measurement protocols and calibration routines were developed and resulted in contributions to an existing calibration framework as well as the prototype of a neuron characterization tool. Furthermore, it could be shown that a rich set of AdEx firing patterns can be reproduced by the new neuron circuits. During this thesis, the author has contributed to putting HXv2 into operation including the commissioning of multiple *BrainScaleS-2* setups.

First, the analog parameter storage was calibrated to sufficiently provide currents and voltages. It was found that, for the utilized parameterization, the capacitive memory's cells saturated for large currents and voltages, such that its linear range shrank to the range between 0 LSB and 700 LSB for voltages as well as 20 LSB and 800 LSB for currents. A further investigation of the respective configuration as well as possible cross-talk between cells is recommended.

The investigation of the analog neuron circuits included measurements of the leak and threshold circuits, the synaptic input, the adaptation term and the exponential term. To characterize basic LIF behavior, the membrane time constant τ_m, the leak voltage V_{leak}, the reset voltage V_{reset} and the threshold voltage V_{thresh} were investigated systematically for 1024 neurons on two chips. Using external laboratory equipment, the leak conductance g_{l} were measured for multiple neurons and hence it was possible to estimate the membranes capacitance C_{m}. Looking on the newly designed synaptic input, the g_{m}-OTA's input offset was calibrated and the noise on the membrane, caused by the synaptic input, was estimated systematically. Further the synaptic time constant τ_{syn} was measured for all available neurons. A fist look on the synaptic input's linearity was enabled by measurements of an exemplary neuron. Within the adaptation term, first, the a-OTA's offset was calibrated. Then the adaptation time constant τ_w, the sub-threshold adaptation parameter a and the spike-triggered adaptation parameter b were investigated systematically. Furthermore the exponential term parameters Δ_{T} and V_{T} were measured for multiple neurons and discussed.

Hence all analog circuits in the neuron of HXv2 were investigated.

In the analog neuron circuits, only three reasonably deviations from the ASIC's specification were found: On the on hand, the limitation of the leak voltage (and therefore also

reset voltage) dynamic range. On the other hand, a timing issue in the adaptation-pulse used for the spike-triggered adaptation. Last minute simulations by Sebastian Billaudelle have shown, that this issue is caused by parasitic capacities, which were not taken into account for the design. Finally, a suspected issue in the measurement protocol yielded distorted results for the investigation of the synaptic input's linearity. All other components showed behavior as expected. Furthermore, after calibrating the analog parameter storage, all the further measurement quantities deviated more within blocks as between blocks or chips.

For larger neural network experiments, automated calibration are required. Leibfried (2018) has shown, that the PPU is suitable for this on-chip calibration. Here, results and methods presented in this thesis could be adopted for automated calibrations of the adaptation term and the exponential term.

Such a calibration framework can then be used to more faithfully reproduce the AdEx firing patterns. While this thesis has shown that the neuron circuit can be tuned to exhibit the desired behavior, an automated parameter lookup will facilitate a large scale invetigation of these patterns in the near future.

Appendix

Configuration of the analog parameter storage	HXv2		HXv1
Parameter	Chip 22	Chip 23	default
ReferenceGeneratorConfig			
Enable internal reference current	True	True	True
Enable reference current output	False	False	False
Enable reference current input	False	False	False
Reference control DAC value	2	2	10
Resistor control DAC value	60	60	40
Reset signal in current generator	0	0	0
CapMem block 0/1/2/3 amp. bias current	63/63/63/63	63/63/63/63	60
CapMem block 0/1/2/3 offset bias current	0/13/ 4/18	6/ 1/63/ 0	0
CapMem block 0/1/2/3 slope bias current	9/ 8/ 9/ 9	8/ 9/ 8/ 9	5
CapMemBlockConfig			
Pulse a	110		11
Pulse b	120		15
Sub counter	128		16
Pause counter	20000		8096
Enable capmem	True		True
Boost a	0		0
Boost b	0		0
Boost factor	0		0
Current cell resistor	8		8
Enable autoboost	False		False
Enable boost	False		False
Prescale pause	3		3
Prescale ramp	3		3
V global bias	7		7

Table 1: Default configuration of the analog parameter storage as used in this thesis.

Default configuration of the neuron backends Parameter	HXv2 default	HXv1 default
CommonNeuronBackendConfig		
Enable event register	`True`	`True`
Force reset	`False`	`False`
Enable clocks	`True`	`True`
Clock scale slow	`4`	`4`
Clock scale fast	`4`	`4`
Set sample positive edge 0/1/2/3	`True/True/` `True/True`	`True/True/` `True/True`
Clock scale adaptation pulse	`7`	`0`
Clock scale post pulse	`0`	`0`
Wait global post pulse	`128`	`128`
Wait spike counter reset	`4`	`4`
Wait spike counter read	`112`	`112`
Wait fire neuron	`4`	`4`
NeuronBackendConfig		
Address out	*neuron specific*	*neuron specific*
Reset hold off config	`15`	`15`
Refractory time	`40`	`80`
Post overwrite	`False`	`False`
Select input clock	`0`	`0`
Enable adaptation pulse	`True`	`False`
Enable bayesian extension	`False`	`False`
Enable neuron slave	`False`	`False`
Connect fire bottom	`False`	`False`
Connect fire from right	`False`	`False`
Connect fire to right	`False`	`False`
Enable spike out	`True`	`True`
Enable neuron master	`True`	`True`
Enable 0 bayesian	`False`	`False`
Enable 1 bayesian	`False`	`False`

Table 2: Default configuration of the (common) neuron backend as used in this thesis.

Default values of analog parameters Parameter		HXv2 default	HXv1 default
Local analog parameters			
Leak voltage V_{leak}	LSB	667	667
Adaptation leak voltage $V_{\text{adapt, leak}}$	LSB	667	-
Reset voltage V_{reset}	LSB	667	556
Threshold voltage V_{thresh}	LSB	556	556
Adaptation reference voltage $V_{\text{adapt, ref}}$	LSB	667	0
Exponential reference voltage V_{exp}	LSB	556	-
Offset current bias I_{ext}	LSB	0	0
Synin exc tau bias $I_{\text{exc, }\tau_{\text{syn}}}$	LSB	500	400
Synin exc drop bias $I_{\text{exc, drop}}$	LSB	500	-
Synin exc shift bias $I_{\text{exc, shift}}$	LSB	500	-
Synin exc gm bias $I_{\text{exc, gm}}$	LSB	1000	1000
Synin inh tau bias $I_{\text{inh, }\tau_{\text{syn}}}$	LSB	500	400
Synin inh drop bias $I_{\text{inh, drop}}$	LSB	500	-
Synin inh shift bias $I_{\text{inh, shift}}$	LSB	500	-
Synin inh gm bias $I_{\text{inh, gm}}$	LSB	1000	100
Leak bias I_{leak}	LSB	50	20
Reset bias I_{reset}	LSB	1000	1000
Adaptation tau bias I_{τ_w}	LSB	6	0
Adaptation a bias I_{a}	LSB	10	-
Adaptation b bias I_{b}	LSB	300	-
Exponential bias $I_{\text{inh, gm}}$	LSB	500	-
Multicompartment bias	LSB	0	0
Global analog parameters			
Neuron v-cascade bias	LSB	333	-
Neuron source follower bias	LSB	100	500
Neuron readout amplifier bias	LSB	100	150
Neuron spike comparator bias	LSB	200	1001
Readout out amplifier bias 0	LSB	1000	1000
Readout out amplifier bias 1	LSB	1000	1000
Readout pseudo diff. buffer bias	LSB	1000	1000
Readout AC mux bias	LSB	500	500
Readout MADC input 500 nA	LSB	500	500
Readout SC amplifier bias	LSB	500	500
Readout SC amplifier reference voltage	LSB	400	400
Readout pseudo diff. reference voltage	LSB	400	400
Readout iconv test voltage	LSB	400	400
Readout iconv SC amplifier reference voltage	LSB	400	400

Table 3: Default analog parameters as used in this thesis. CADC related values not listed, since the CADC was not used. For HXv1, only parameter also available in HXv2 are listed.

Default configuration of the neurons Parameter	HXv2 default	HXv1 default
Connect bottom	False	False
Connect membrane right	False	False
Connect soma	False	False
Connect soma right	False	False
Enable adaptation	False	False
Enable read vw	False	False
Enable bypass exc	False	False
Enable bypass inh	False	False
Enable capacitor merge	False	False
Enable div. multicomp. cond. bias	False	False
Enable exponential	False	False
Enable fire	False	False
Enable leak degeneration	False	False
Enable leak division	False	False
Enable leak multiplication	False	False
Enable membrane offset	False	False
Enable mul. multicomp. cond. bias	False	False
Enable pause	True	-
Enable readout	False	False
Enable readout amplifier	True	True
Enable reset degeneration	False	False
Enable reset multiplication	True	True
Enable strong fire	False	False
Enable synin exc	False	False
Enable synin exc high resistance	False	False
Enable synin exc small capacitance	False	False
Enable synin inh	False	False
Enable synin inh high resistance	False	False
Enable synin inh small capacitance	False	False
Enable comparator	True	True
Enable unbuffered access	False	False
Invert a	False	False
Invert b	False	False
Invert current	False	False
Membrane capacitance select	63	63
Readout select	vm	vm

Table 4: Default neuron configuration as used in this thesis. For HXv1, only parameter also available in HXv2 are listed.

AdEx firing pattern		Regular bursting	Delayed accelerating	Initial bursting	Transient spiking	Inhibitory rebound	Delayed regular bursting
Biological parameters							
C	pF	200	200	130	100	-	100
g_{L}	nS	10	12	18	20	-	10
E_{L}	mV	-58	-70	-58	-65	-	-65
V_{T}	mV	-50	-50	-50	-50	-	-50
Δ_{T}	mV	2	2	2	2	-	2
a	mS	2	-10	4	15	-	-8
τ_w	ms	120	300	150	90	-	90
b	pA	120	0	120	300	-	50
V_{r}	mV	-46	-58	-50	-47	-	-47
I_{ext}	pA	210	300	400	350	-	110
Hardware parameters							
Chip 22, Block 0, Neuron 4							
τ_{m} bias current	LSB	491	DIV 644	108	108	108	70
Leak voltage	LSB	602	598	677	677	798	599
Reset voltage	LSB	804	711	793	793	792	824
Threshold voltage	LSB	556	556	556	556	556	556
a bias current	LSB	5	INV 35	30	70	400	INV 15
b bias current	LSB	300	0	700	500	100	900
τ_w bias current	LSB	110	25	100	100	80	170
Adapt. leak voltage	LSB	524	690	524	524	524	711
Exp. bias current	LSB	400	400	400	400	400	400
Exp. ref. voltage	LSB	762	762	762	762	762	762
Offset current	LSB	220	150	350	300	INV 400	120

Table 5: Parameters for AdEx firing pattern suggested by Naud et al. (2008). Biological parameters for delayed regular bursting and transient spiking are modified such such they match with the figures in Naud et al. (2008) (Dauer, 2019). Hardware parameters are inspired by there biologic example and calibrated using an educated guess.

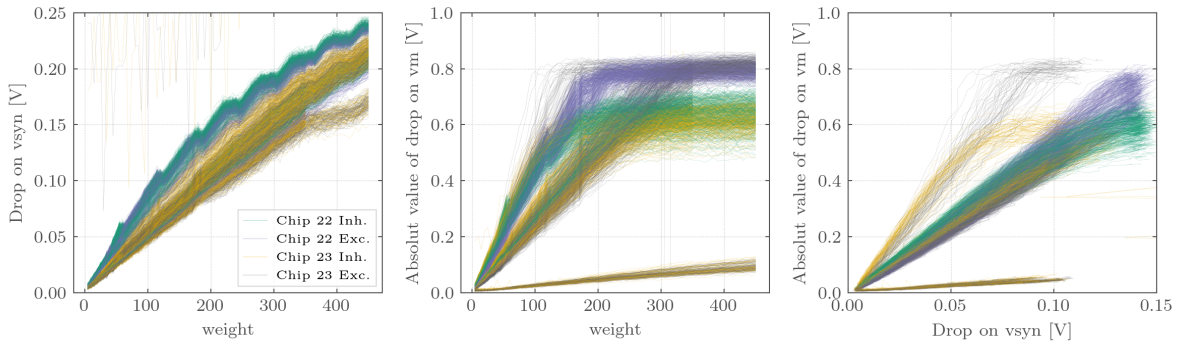


Figure 35: Measured voltage drops caused by spikes on the synaptic line and on the membrane for all investigated neurons. The right plot represents the amplification factor of the OTA with respect to its input voltage.

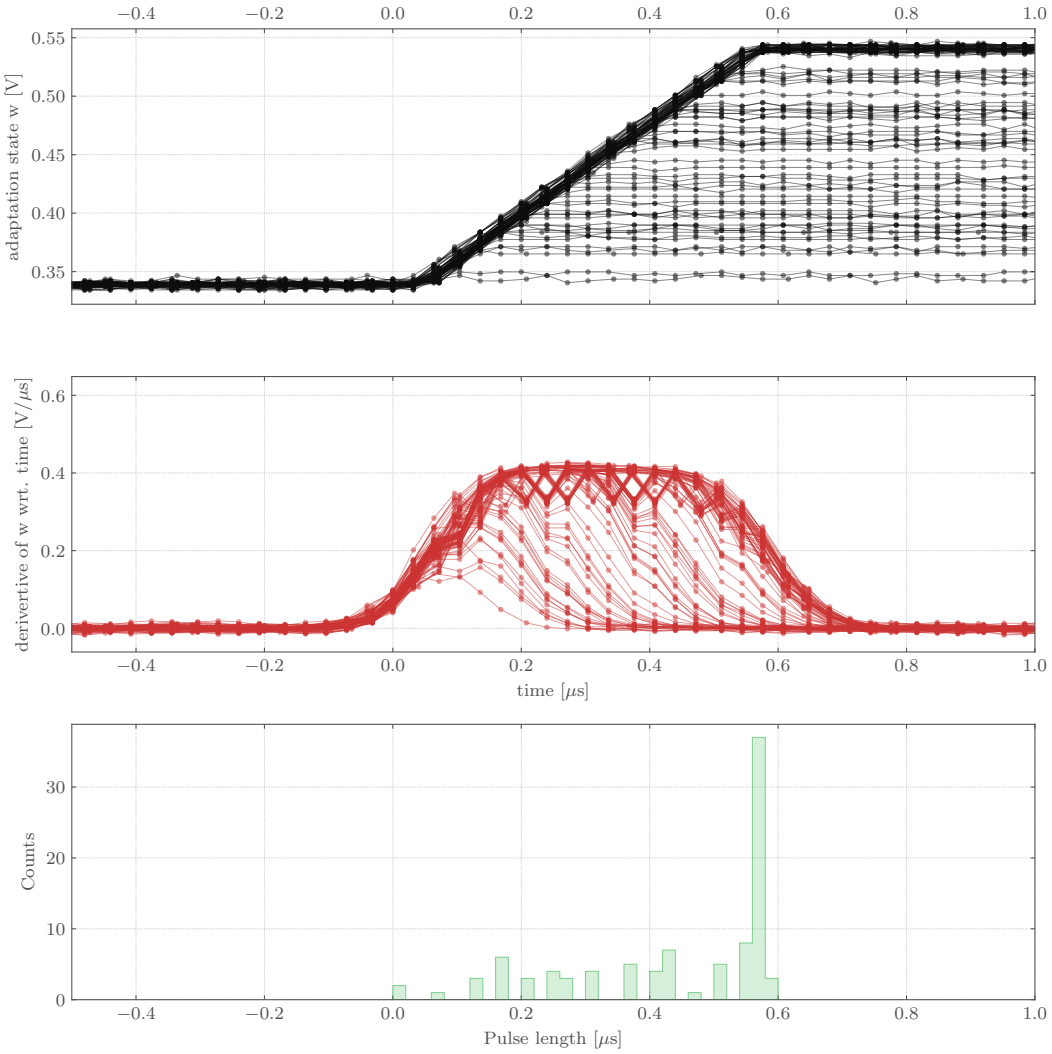


Figure 36: Illustration of the adaptation-pulse-related bug in the neuron backend. It shows 100 times the exact similar experiment, that provoked an adaptation-pulse by forcing a reset and recorded the adaptation state for $I_b = 500\,\mathrm{LSB}$ on chip 22, block 0, neuron 0. The starting point of the current ramp has been standardized for better clarity.

References

AnalogDevices: 2.5 V to 5.5 V Octal Voltage Output 8-/10-/12-Bit DACs in 16-Lead TSSOP, Analog Devices, One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A., rev.F, 2011.

Billaudelle, S.: Personal communication, 2019.

Billaudelle, S., Cramer, B., Petrovici, M. A., Schreiber, K., Kappel, D., Schemmel, J., and Meier, K.: Structural plasticity on an accelerated analog neuromorphic hardware system, arXiv preprint arXiv:1912.12047, 2019a.

Billaudelle, S., Stradmann, Y., Schreiber, K., Cramer, B., Baumbach, A., Dold, D., Göltz, J., Kungl, A. F., Wunderlich, T. C., Hartel, A., et al.: Versatile emulation of spiking neural networks on an accelerated neuromorphic substrate, arXiv preprint arXiv:1912.12980, 2019b.

Brette, R. and Gerstner, W.: Adaptive exponential integrate-and-fire model as an effective description of neuronal activity, Journal of neurophysiology, 94, 3637–3642, 2005.

Cramer, B., Stöckel, D., Kreft, M., Wibral, M., Schemmel, J., Meier, K., and Priesemann, V.: Control of criticality and computation in spiking neuromorphic networks with plasticity, Nature Communications, 11, 1–11, 2020.

Czischek, S., Baumbach, A., Billaudelle, S., Cramer, B., Kades, L., Pawlowski, J. M., Oberthaler, M. K., Schemmel, J., Petrovici, M. A., Gasenzer, T., et al.: Spiking neuromophic chip learns entangled quantum states, arXiv preprint arXiv:2008.01039, 2020.

Dauer, P.: Pre-tapeout calibration and benchmarking of simulated neuron circuits, Internship report, Universität Heidelberg, 2019.

FitzHugh, R.: Impulses and physiological states in theoretical models of nerve membrane, Biophysical journal, 1, 445, 1961.

Gerstner, W. and Kistler, W. M.: Spiking neuron models: Single neurons, populations, plasticity, Cambridge university press, 2002.

Göltz, J., Baumbach, A., Billaudelle, S., Breitwieser, O., Dold, D., Kriener, L., Kungl, A. F., Senn, W., Schemmel, J., Meier, K., et al.: Fast and deep neuromorphic learning with time-to-first-spike coding, arXiv preprint arXiv:1912.11443, 2019.

Grübl, A., Billaudelle, S., Cramer, B., Karasenko, V., and Schemmel, J.: Verification and Design Methods for the BrainScaleS Neuromorphic Hardware System, Journal of Signal Processing Systems, doi:10.1007/s11265-020-01558-7, URL https://doi.org/10.1007/s11265-020-01558-7, 2020.

Hartel, A.: Improving and Testing a Mixed-Signal VLSI Neural Network Chip, Diplomarbeit, Universität Heidelberg, 2010.

Hock, M.: Capacitive Memory Specication, URL https://brainscales-r.kip.uni-heidelberg.de/projects/cm-spec, 2015.

Hodgkin, A. L. and Huxley, A. F.: A quantitative description of membrane current and its application to conduction and excitation in nerve, The Journal of physiology, 117, 500, 1952.

Kriener, L.: Characterization of Single-Neuron Dynamics in the Development of Neuromorphic Hardware, Master's thesis, Heidelberg University, 2017.

Lapicque, L.: Recherches quantitatives sur l'excitation électrique des nerfs traitée commeune polarisation, J. Physiol. Pathol. Gen, 9, 620–635, 1907.

Leibfried, A.: On-chip calibration of analog neuromorphic circuits, Bachelorarbeit, Universität Heidelberg, 2018.

Meier, K.: Special report: Can we copy the brain?-The brain as computer, IEEE Spectrum, 54, 28–33, 2017.

Müller, E., Mauch, C., Spilger, P., Breitwieser, O. J., Klähn, J., Stöckel, D., Wunderlich, T., and Schemmel, J.: Extending BrainScaleS OS for BrainScaleS-2, arXiv preprint arXiv:2003.13750, 2020a.

Müller, E., Schmitt, S., Mauch, C., Billaudelle, S., Grübl, A., Güttler, M., Husmann, D., Ilmberger, J., Jeltsch, S., Kaiser, J., et al.: The Operating System of the Neuromorphic BrainScaleS-1 System, arXiv preprint arXiv:2003.13749, 2020b.

Nagumo, J., Arimoto, S., and Yoshizawa, S.: An active pulse transmission line simulating nerve axon, Proceedings of the IRE, 50, 2061–2070, 1962.

Naud, R., Marcille, N., Clopath, C., and Gerstner, W.: Firing patterns in the adaptive exponential integrate-and-fire model, Biological cybernetics, 99, 335, 2008.

Schemmel, J., Grubl, A., Meier, K., and Mueller, E.: Implementing synaptic plasticity in a VLSI spiking neural network model, in: The 2006 IEEE International Joint Conference on Neural Network Proceedings, pp. 1–6, IEEE, 2006.

Schemmel, J., Fieres, J., and Meier, K.: Wafer-scale integration of analog neural networks, in: 2008 IEEE International Joint Conference on Neural Networks (IEEE World Congress on Computational Intelligence), pp. 431–438, IEEE, 2008.

Schemmel, J., Billaudelle, S., Dauer, P., and Weis, J.: Accelerated Analog Neuromorphic Computing, arXiv preprint arXiv:2003.11996, 2020.

Stradmann, Y.: Characterization and Calibration of a Mixed-Signal Leaky Integrate and Fire Neuron on HICANN-DLS, Bachelorarbeit, Universität Heidelberg, 2016.

Acronyms

ADC analog-to-digital converter ..... XII, 5, 10, 15, 41

AdEx adaptive exponential integrate-and-fire model VI, 1–4, 19, 37, 43, 45, 48, 49, 51, 52

AP action potential 2

ASIC application-specific integrated circuit 1, 3–5, 8, 12, 13, 49, 51

CADC column-parallel ADC ..... IV, 10

COBA conductance-based model 3, 29

CUBA current-based model 3, 4, 6, 19, 29

DAC digital-to-analog converter 5, 9–11, 13, 15

DLS Digital Lerning System XII

DNL differential non-linearity 15

FHN FitzHugh-Nagumo model 1

FPGA field-programmable gate array 5

HICANN High Input Count Analog Neural Network ..... XII, 2, 4

HICANN-DLS High Input Count Analog Neural Network DLS 4

HICANN-X High Input Count Analog Neural Network X . XII, 1–7, 9, 10, 12, 19, 23, 51

HXv1 HICANN-X v1 ..... IV, V, 5, 6, 21–23, 30, 34, 35

HXv2 HICANN-X v2 . IV, V, 2, 6, 8, 9, 13, 19, 21–24, 28–30, 32, 34, 35, 38, 39, 41, 43, 45, 49–51

INL integrated non-linearity 15, 16, 18

LIF leaky integrate-and-fire model 1–4, 19, 51

OTA operational trans-conductance amplifier ..... VII, 3, 20, 21, 23–26, 29, 30, 32, 33, 35–37, 39, 42, 43, 45, 46, 51

PPU plasticity processing unit 5, 23, 38, 42, 52

PSP post-synaptic-potential 3, 31–34

SRAM static random-access memory 12

Statement of Originality (Erklärung)

I certify that this thesis, and the research to which it refers, are the product of my own work. Any ideas or quotations from the work of other people, published or otherwise, are fully acknowledged in accordance with the standard referencing practices of the discipline.

Ich versichere, dass ich diese Arbeit selbstständig verfasst und keine anderen als die angegebenen Quellen und Hilfsmittel benutzt habe.

Heidelberg, August 28, 2020