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Calibration of the Analog HICANN Readout Process

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Kalibration der Analogen HICANN Auslese

Das neuromorphe Hardware System *BrainScaleS* ermöglicht das Emulieren von großskaligen neuronalen Netzwerken auf analogen Schaltungen. Der *High Input Count Analog Neural Network chip* (HICANN) trägt als Grundbaustein des Systems die analogen Neuron- und Synapsenschaltkreise. Da diese in vollautomatischen Prozessen kalibriert werden müssen, sind präzise Messungen des analogen Membranpotentials unerlässlich um eine stabile Kalibration gewährleisten zu können. Im Rahmen der vorliegenden Arbeit wurde die zukünftig über die *ANAlog Network Attached Sampling units* (ANANAS) ablaufende analoge HICANN Auslese analytisch untersucht und darauf aufbauend das Konzept einer Kalibration der Digitalumsetzer entwickelt. Diese wurde experimentell auf dem Wafer und unter der Verwendung eines Source Meters, eines Funktionsgenerators und eines Oszilloskops im Hinblick auf die benötigte Präzision und Langzeitstabilität untersucht. Besonderes Augenmerk wurde auf die Korrektur von Übersprecheffekten in den Digitalisierungsbauteilen gelegt. Diese erschweren parallele Messungen mit mehr als drei Kanälen des ANANAS Boards. Eine in dieser Arbeit vorgestellte Lösung des Problems ermöglicht die parallele Verwendung von bis zu 42 aus 48 Kanälen, was zu einer merklichen Beschleunigung in der Beschaffung experimenteller Daten führt. Weiterhin wird dadurch die Robustheit automatisierter Kalibrationen von Neuronen und Synapsen erhöht. Aufgrund der großen Unsicherheit, die sie in der Messung analoger Membranspannungen hervorrufen, wurden die Ausgangsimpedanzen der HICANNs einer Hälfte eines Wafermoduls untersucht.

Calibration of the Analog HICANN Readout Process

The *BrainScaleS* neuromorphic system enables the emulation of large-scale neural networks on analog circuits. Being the principal building block of this system, the *High Input Count Analog Neural Network chip* (HICANN) consists of neuronal and synaptic analog circuits. These need to be calibrated by fully automated calibration routines. Therefore, a precise measurement of the analog membrane trace is crucial for the robustness of these processes. In the framework of this thesis, the HICANN analog readout chain, which will involve the *ANAlog Network Attached Sampling unit* (ANANAS) in the future, has been analysed and a calibration routine has been developed for the digitizing components. Afterwards, it has been tested experimentally with regard to the required precision and long-term stability of calibration data. Tests have been performed on-wafer as well as using a source meter, a function generator and an oscilloscope. Emphasis has been put on the correction of internal crosstalk of the digitizing components, hindering parallel measurements with more than three channels of the ANANAS. The solution introduced in this thesis enables an utilization of 42 out of 48 channels to be used in parallel. This leads to a significant speed-up in the acquisition of experimental data. Meanwhile, the robustness of automated neuron and synapse calibration routines is increased additionally. Representing an important source of error, the HICANN source impedances of half a wafer have been determined in order to reduce the uncertainty of the readout of analog membrane traces.

Contents

1 Introduction

In the field of computational neuroscience emulation of biologically inspired neural network models can be carried out with neuromorphic hardware. Offering a physical representation of the constituents which follow the differential equations of a biological neural system, it is a significantly different approach than numerical simulations on traditional von Neumann devices. In contrast to synchronous digital simulations the analog topology allows to execute experiments in biological time accelerated by a factor of 10^4 This is due to the network model evolving on time scales which follow the intrinsic time constants of the constituents. The neuromorphic approach is also considerably more energy-efficient since it uses wafer-scale integration modules [Sch+10].

The *BrainScaleS* neuromorphic hardware system is depicted in Figure 1.1. It consists of multiple racks, five of them containing four wafer modules structured according to Figure 1.2, respectively. Each module can be roughly subdivided into two parts: firstly, a 20 cm diameter silicon wafer containing the neuron and synapse circuits, and secondly a set of *printed circuit boards* (PCB) providing power and analog connections as well as digital communication modules connecting the wafer to a host PC or other modules.

Figure 1.1: BrainScaleS neuromorphic compute system for 20 wafer modules. Each module has 384 HICANN chips with up to 512 neurons and 114 688 synapses each. This corresponds to 0.2×10^6 neurons and 44×10^6 synapses. For the complete system including 20 wafer modules in total this scales to roughly 3.9×10^6 neurons and 880×10^6 synapses.

The principal building block of the wafer is the *High Input Count Analog Neural Network chip* (HICANN) [SFM08]. It contains the mixed-signal neuron and synapse circuits as well as the necessary support circuits and the digital communication interface. Eight HICANNs are integrated in a single reticle. Each reticle is provided

with switchable power supply and two analog readout connections for measurements of the membrane potential.

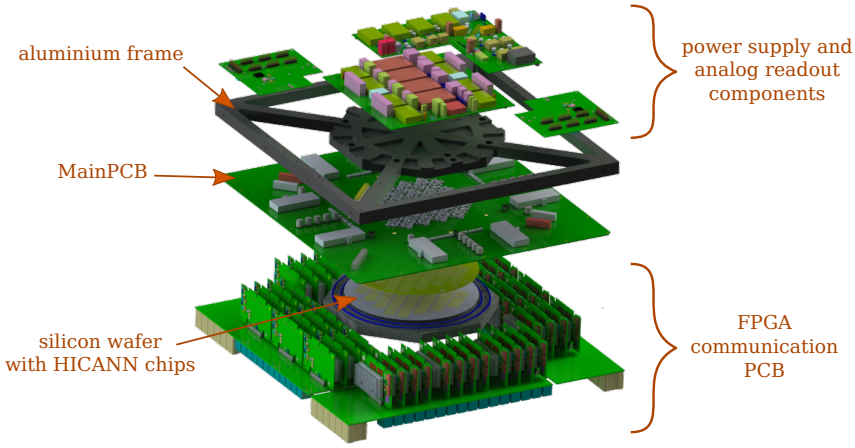

Figure 1.2: Exploded view of a complete BrainScaleS wafer module [Güt17]. The silicon wafer containing the HICANN chips is connected to the MainPCB via elastomeric strip connectors. HICANN configuration, recording of spike data and inter-wafer communication is controlled by the FPGA communication PCB.

Due to variations in the manufacturing process, neuron and synapse parameters need to be calibrated. This is usually done by recording the analog membrane potential with external analog-to-digital converters. Thus prerequisite for the calibration of neuron and synapse parameters is the calibration of the analog-to-digital converters and the determination of the HICANN source impedance. The analog signals coming from the HICANN are single ended with an approximate source impedance of 50 Ω. Hence 50 Ω terminated DC measurements of the membrane potential are prone to large uncertainties. An accurate measurement is only possible with this calibration.

In the framework of this thesis a concept for a calibration routine of the analog HICANN readout process has been developed and tested. Important aspects were:

- *Analog accuracy.* The calibration routine aims to approximate the characteristics of analog-to-digital converters as accurately as possible without being too flexible. The required precision had to be evaluated in contrast to

- *Long-term stability.* The most accurate modelling of the input-output translation of the analog-to-digital converters can be worthless if the system changes over a large period of time. Temperature variations could also have an impact on the robustness of the calibration. Thus, the variations of calibration data have been investigated over the course of several weeks.

- *Source impedance measurement.* The uncertainty in membrane voltage measurements arising from the variations of the HICANN source impedance is assumed to be the most important systematic error in the analog readout process[1]. Hence a procedure to precisely determine these impedances has been developed.

- *User-friendliness.* The hardware setup and required software stack have been chosen to enable an uncomplicated application of the calibration routine. Additionally the runtime of the calibration has been tried to be kept as low as possible.

[1] Personal communication with Joscha Ilmberger and Maurice Güttler

1.1 Terms and Definitions

The main focus of this thesis is the characterization and calibration of electronic components on the *ANAlog Network Attached Sampling unit* which will be used for the analog readout of the HICANNs in the future. This regards especially the conversion of analog to digital signals. Furthermore, established source meter units are used for the calibration routine. The next sections introduce the important electronic components and provide a basic understanding of the most important technical terms and definitions used throughout this document.

1.1.1 Analog-to-Digital Converter

As suggested by its name, an *analog-to-digital converter* (ADC) is an *integrated circuit* (IC) used to translate analog signals into digital ones. An ADC receives a signal *continuously* in time and amplitude, e.g. a voltage signal, and converts it into a *discrete* representation of the original. Accordingly a quantization of the primary signal is introduced in two dimensions: Input values are sampled periodically at discrete steps in time and represented by quantized digital values which depend on the maximum input range and the precision of the ADC [Fra10].

Limiting factors to the quality of the digital representation of the analog input have to be discussed. One of the most important constraints to be considered is the *resolution* of an ADC. Since the output data is usually stored in a binary format, the total number of possible discretized values corresponds to a power of two. In general the resolution is specified by a certain number of bits. This means that the number of representable values N for an ADC with a resolution of x bit is given by:

$$N = 2^x. \tag{1.1}$$

There are a variety of different ADC types available on the market. However all models share the common approach of comparing the measured input with a reference value. In this thesis two different models have been considered that are characterized as follows [HBG17]:

- Integrating ADC: The input current is integrated over a fixed period of time. Subsequently, the voltage on the integrator is compared to a reference voltage. This is done by applying the reference voltage to the integrator and measuring the time until the output voltage of the integrator is zero. This topology can be used for measurements that require a high precision.

- Differential Flash ADC: The input voltage is measured differentially against a, often user-definable, *common mode* (CM) voltage. Several comparators are used to digitize the signal with reference to the common mode voltage which allows for higher sampling speeds in most cases.

1.1.2 Least Significant Bit

The *least significant bit* (LSB) is an important quantity for discussing the available accuracy of an ADC when investigating the deviations of digital output values from known input values. It is defined as the smallest possible value that an ADC is able to distinguish between two analog values. Hence, it further defines the resolution of an ADC. The *full scale range* (FSR) voltage V_{FSR} of an ADC is determined by the lower and upper limits V_{lo} and V_{up} of the measurement range via

$$V_{\mathrm{FSR}} = V_{\mathrm{up}} - V_{\mathrm{lo}}. \tag{1.2}$$

Under the application of equation (1.1) the LSB is:

$$1\,\mathrm{LSB} = \frac{V_{\mathrm{FSR}}}{N-1} = \frac{V_{\mathrm{FSR}}}{2^x - 1}. \tag{1.3}$$

1.1.3 Gain and Offset

The characteristic curve describing the output value f as a function of the input value x of an ideal ADC is a linear function:

$$f(x) = G \cdot x + V_0. \tag{1.4}$$

In this relationship two new parameters are introduced. The gain G is a proportionality factor containing the information how the ADC transfers a change in the input value to the output. Therefore, it is directly linked to the previously defined LSB:

$$G = \frac{1}{1\,\mathrm{LSB}}. \tag{1.5}$$

The second parameter, the offset V_0, corresponds to the output value in an idle state of the ADC with $x = 0$, thus no input applied. For a differential ADC, this corresponds to an input equal to the reference voltage, and for the integrating topology to an input current of $I = 0\,\mathrm{A}$.

Both quantities G and V_0 underlie uncertainties that can for example be temperature dependent or conditioned by the production process. In general these errors are reported by the manufacturer in the respective data sheets accompanying the device. Precisely also ADC internal non-linear effects are reported. They are in general referenced to as *integral non-linearity* (INL) and *differential non-linearity* (DNL), characterizing the deviations from an ideal linear characteristic curve[2]. In this thesis, these deviations are quantified in a simplified manner by investigating the residuals of measured values from a linear best-fit obtained by least squares methods.

Considering an current input integrator ADC the ideal offset might be an artificial output value larger than zero at an assumed input current of 0 A. This offset might be introduced to allow slightly negative currents to be measured. The offset error would be characterized by the difference between the actually measured output and the theoretical ideal value. In this case temperature dependent dark current effects could be one reason for the appearance of an offset error. One needs to study these errors when investigating the stability of a calibration over a large period of time.

[2] cf. equation (1.4)

1.1.4 Source Meter

A *Source Meter*[3] (SM) is capable of sourcing a voltage or a current with a very high precision and carrying out voltage and/or current measurements at the same time. It consists of two parts: A power supply with electronically controlled outputs for voltage and current and a multimeter. High-quality models can source and measure at ranges from mV to 10^2 V and nA to A. Serviced on a regular basis this makes it a suitable device for automated calibration routines. Here it is mainly used as a high-precision remote-controlled voltage source that automatically tracks the reference voltages the output of the ADCs is compared with.

1.2 The Analog Network Attached Sampling unit

The *ANAlog Network Attached Sampling unit* (ANANAS) [Ilm17] has been developed to offer a faster and more robust calibration of the HICANNs and usage of the BrainScaleS hardware in general compared to the current digitizer system. An overview of the PCB is shown in Figure 1.3.

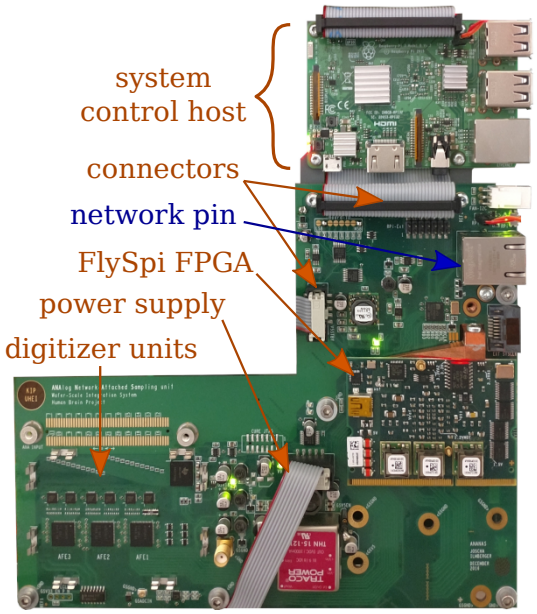

Figure 1.3: Fully equipped PCB of the ANANAS. The lower left side contains the digitizer units and the power supply. Slow-control of the units is provided by the *FlySpi FPGA* board attached to the PCB on the lower right side. Connectors to power and the system control host, a *RaspberryPi 3*, as well as an Ethernet network pin are located above the FPGA. Copyright: Joscha Ilmberger

The system aims to enable full parallel readout of up to 48 membrane traces with 50 Ω termination at a resolution of 12 bit. It is also capable of precise DC measurements with high input impedance at a resolution of 20 bit. For this purpose two different types of ADCs have been included in the circuitry:

1. Three 16-channel *AFE5851* [Ins10] (hsADC[4]) with 31.25 MHz sampling rate at 12 bit resolution. The model is based on differential signaling topology, measuring the input symmetrically around a common mode voltage V_{CM}. The internal $V_{\mathrm{CM}} = 1.6\,\mathrm{V}$ is referenced to ground. With a membrane voltage range

[3] Another common term is *Source Measure Unit*.
[4] high speed analog-to-digital converter

of $V_M = 0\,\text{mV}$ to $900\,\text{mV}$, which follows from the $50\,\Omega$ terminated power supply of the HICANNs, the predefined V_{CM} is not suitable for all input values. Thus the hsADC is operated on a shifted ground supply voltage $V_{GS} = -1.15\,\text{V}$. This shifts the $V_{range} = 1\,\text{V}$ input range[5] of the hsADC symmetrically around the V_M range:

$$V_{\text{hsADC,in}} = V_{GS} + V_{CM} \pm \frac{V_{range}}{2} = (450 \pm 500)\,\text{mV}. \tag{1.6}$$

The shifted ground approach demands a coordinate transformation from the hsADC-internal coordinate system to the one referenced to the ground of the ANANAS board.

2. One *DDC264* [Ins16] (lsADC[6]) with 64 internal 20 bit ADCs allowing for parallel measurements of all 48 inputs coming from the wafer at a sampling rate of 3 ksps. The model is an integrating ADC intended to be used in precise DC calibration routines.

A schematic overview of the analog frontend implementation is shown in Figure 1.4. Errors arise from the external input impedances and terminating resistors as well as the internal biasing resistors. Combined with the ADC specific gain and offset errors as well as non-linearities this demands a calibration of the analog frontend. Ideally this calibration has to be executed only one time for the life span of the board.

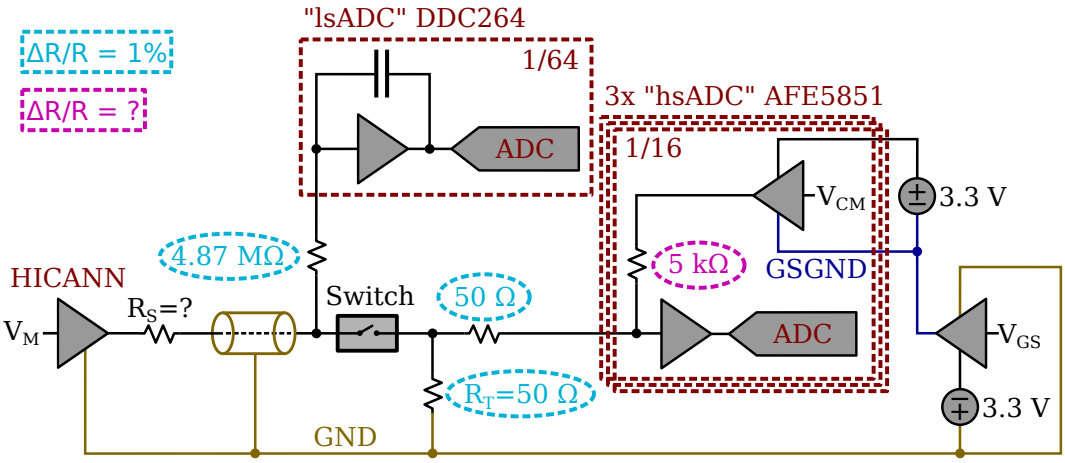

Figure 1.4: Schematic of the analog frontend, adapted from: Joscha Ilmberger [Ilm17]. The input membrane voltage V_M coming from the HICANN is fed to the analog readout devices ground referenced single ended. The unknown source impedance R_S is approximately $50\,\Omega$. The lsADC is used with a high input impedance of $4.87\,\text{M}\Omega$ to convert the voltage into a current suitable for the internal integrators. An analog switch *MAX14662* [Int14] can be set to enable $50\,\Omega$ terminated measurements with the hsADC which is supplied with a shifted ground voltage V_{GS}. Resistor values are color-coded in order to give an estimate for the relative error they induce on the voltage measured by the ADCs. The error of the internal $5\,\text{k}\Omega$ resistor is not specified by the manufacturer [Ins10].

Further unterminated measurements with the lsADC could potentially be disturbed by small leakage currents through the analog switch. The manual [Int14] reports

[5] Referenced to global ANANAS ground
[6] low speed analog-to-digital converter

a maximum leakage current at 11 V potential difference between the open pins of $I_{\text{leak}} = 50\,\text{nA}$. Compared to the maximum current I_{max} entering the lsADC in an unterminated configuration this would result in a relative error of

$$\frac{I_{\text{leak}}}{I_{\text{max}}} = \frac{50\,\text{nA}}{1.8\,\text{V} \cdot 4.87\,\text{M}\Omega} \approx 13.5\,\%. \tag{1.7}$$

This calculation can be seen as an absolute worst-case approximation. This is because the maximum potential difference across the switch is much smaller in an actual experiment compared to the configuration specified in the data sheet. Another difference between the reported testing conditions and the actual application on the ANANAS board is the parallel connection of the high input impedance of 4.87 MΩ which could reduce the maximum leakage current additionally.

Lastly a hsADC-internal crosstalk has been observed in previous experiments while applying a 10 kHz stimulus to a specific channel and recording its output parallel to the output of a neighbouring channel of the same hsADC [Ilm17]. This crosstalk is assumed to couple in on the common mode via the 5 kΩ internal biasing resistor. It leads to an error of minimum 1 % in the output value. This would hinder parallel measurements and automated calibration routines of the HICANNs and needs to be taken into account when considering the calibration of the hsADC.

2 Theoretical Considerations

In this chapter the theoretical concepts for the calibration of the different components relevant for a reliable measurement of the membrane traces coming from the HICANN will be worked out. A coarse subdivision of the routine is the differentiation between

1. the calibration of the ANANAS and its individual digitizing components and

2. the calibration of the analog drivers inside the HICANN chips on the wafer themselves. This is based on the determination of their individual source impedances.

An outline of the characteristics to be considered when calibrating the individual ADCs of the ANANAS and the HICANN will be given in the following.

2.1 Low Speed ADC

The lsADC can be used both unterminated and terminated. An overview of the two different arrangements possible for a measurement and the internal configuration of the lsADC input structure is shown in Figure 2.1. Because the terminating resistor R_T operates like a voltage divider to global ground combined with the approximate $50\,\Omega$ source impedance, both terminated and unterminated configurations have to be treated separately.

Unterminated Measurements

The sourced voltage V_IN is directly applied to the input stage of the lsADC. This is with the exception of small leakage currents over the open analog switch. The lsADC is an input current integrating type, thus the measured voltage V_lsADC is proportional to the current I through the series connected resistors R_IN and $R_\mathrm{Meg} = 4.87\,\mathrm{M}\Omega$ over the integration time t_int in first approximation:

$$V_\mathrm{lsADC} \propto \int_{t_\mathrm{int}} I \,\mathrm{d}t = \int_{t_\mathrm{int}} \frac{V_\mathrm{IN}}{R_\mathrm{IN} + R_\mathrm{Meg}} \,\mathrm{d}t. \tag{2.1}$$

For the calibration an ideal source impedance $R_\mathrm{IN} = 50\,\Omega$ is assumed. Even with an approximate uncertainty of $\Delta R_\mathrm{IN} \approx 0.01 \cdot R_\mathrm{IN}$, the dominating source of error is the

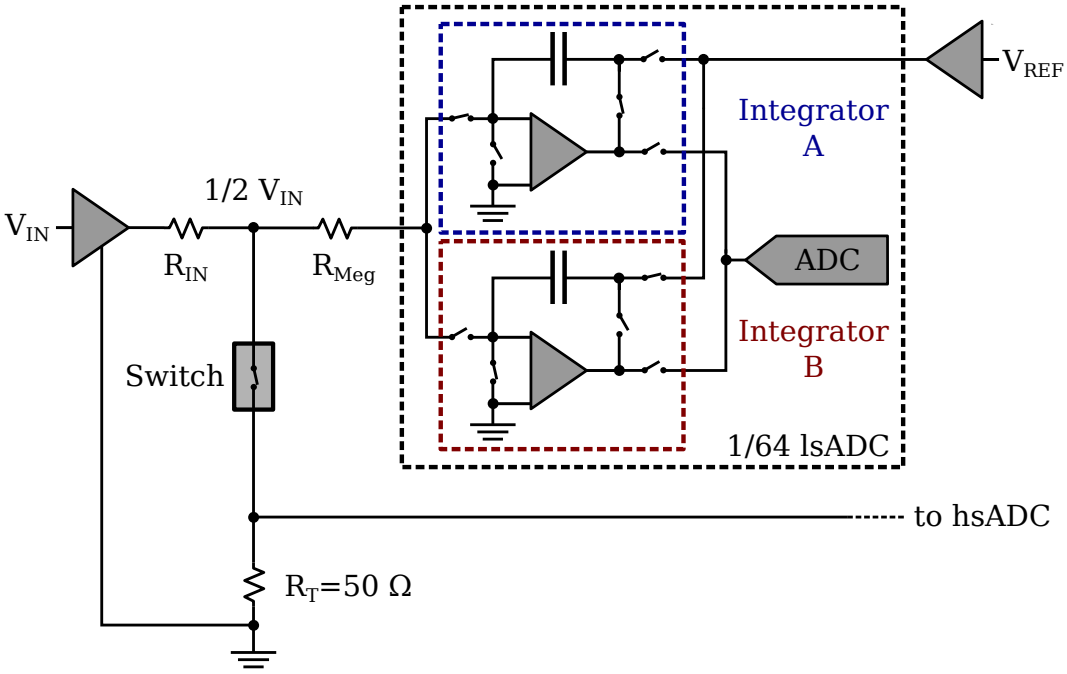

Figure 2.1: Schematic overview of the lsADC input configuration, adapted from: Joscha Ilmberger [Ilm17] and [Ins16]. In general two different measurement configurations are possible, depending on the state of the analog switch connecting to the terminating resistor R_T. In the displayed configuration, terminated measurement would be enabled, leading to an effective input voltage of $\frac{V_\mathrm{IN}}{2}$ under the assumption that $R_\mathrm{IN} = 50\,\Omega$. Each lsADC input consists of two integrators, alternately sampling the input voltage in order to guarantee continuous integration.

high input impedance $R_\mathrm{Meg} = (4.87 \pm 0.05)\,\mathrm{M}\Omega$[1]:

$$\frac{\Delta I}{I} = \sqrt{\left(\frac{\Delta R_\mathrm{IN}}{R_\mathrm{IN}+R_\mathrm{Meg}}\right)^2 + \left(\frac{\Delta R_\mathrm{Meg}}{R_\mathrm{IN}+R_\mathrm{Meg}}\right)^2} \overset{\Delta R_\mathrm{Meg} \gg \Delta R_\mathrm{IN}}{\approx} \frac{\Delta R_\mathrm{Meg}}{R_\mathrm{IN}+R_\mathrm{Meg}}. \tag{2.2}$$

Therefore all deviations from an ideal linear characteristic curve can be referred to the lsADC input stages themselves and the impact of leakage currents over the analog switch for unterminated measurements. It is sufficient to apply a sweep with the source meter over the expected range of the input voltage $V_\mathrm{IN} = 0\,\mathrm{V}$ to $1.8\,\mathrm{V}$, where the maximum corresponds to the HICANN power supply voltage. Then one can measure the sourced voltage as a reference value, which can be done with the multimeter integrated in the source meter, as well as the output of the lsADC. Subsequently a linear least squares fit can be performed to the output data against the sourced reference values with a polynomial P of first order:

$$P(x) = a \cdot x + b. \tag{2.3}$$

By comparing this equation with (1.4) one notices that the gain G corresponds to the slope a and the offset V_0 to parameter b. Note that this equation models the ideal case of the input-output conversion of an ADC. A polynomial of higher order might be necessary in case the non-linearities in the characteristic curve lead to a significant loss of precision.

[1] Resistor value with 1 % uncertainty.

This would result in a set of 48 pairs of calibration values. The two different integrators A and B of each lsADC input have to be considered separately as the internal capacitors and operating amplifiers can also vary. The data sheet [Ins16] reports an offset error match of $\pm 150\,\mathrm{ppm}$[2] of the FSR, a range error match of 0.1 % of the FSR and a range drift match of $\pm 5\,\mathrm{ppm/°C}$ between two integrators of the same channel. Stronger deviations have been observed in section 3.2.2. Ultimately this leads to $2 \cdot 96 = 192$ different values for a full calibration of all 48 channels. This does only relate to the inputs reserved for the HICANNs, the remaining 16 channels cannot be calibrated as an external header for these inputs does not exist.

Terminated Measurements

With the termination set for a single channel, its effective gain and offset values change. The lsADC measures the voltage V_{lsADC} at the node between the source impedance R_{IN} and the series resistor R_{Meg}. Closing the analog switch leads to

$$I = \frac{V_{\mathrm{IN}}}{R_{\mathrm{IN}} + R_{\mathrm{T}} \parallel R_{\mathrm{Meg}}} \overset{R_{\mathrm{T}} \ll R_{\mathrm{Meg}}}{\approx} \frac{V_{\mathrm{IN}}}{R_{\mathrm{IN}} + R_{\mathrm{T}}} \tag{2.4}$$

and under the approximation

$$R_{\mathrm{T}} \approx R_{\mathrm{IN}} \tag{2.5}$$

the measured voltage V_{lsADC} can be calculated with:

$$V_{\mathrm{lsADC}} = V_{\mathrm{IN}} - I \cdot R_{\mathrm{IN}} \approx \frac{1}{2} \cdot V_{\mathrm{IN}}. \tag{2.6}$$

In a first approximation all constituents of the circuitry are linear components. Let G_{off} and $V_{0,\mathrm{off}}$ be the gain and offset values that have been found in the unterminated measurement. Under the assumption that they are characteristics of the lsADC and the resistor R_{Meg} alone, the termination linearly affects the measured voltage with gain factor G_{on} and offset $V_{0,\mathrm{on}}$:

$$V_{\mathrm{lsADC}} = G_{\mathrm{off}} \cdot (G_{\mathrm{on}} \cdot V_{\mathrm{IN}} + V_{0,\mathrm{on}}) + V_{0,\mathrm{off}}, \tag{2.7}$$

which is a linear equation of V_{IN} again. Thus one can proceed with the voltage sweep outlined above. Then a linear fit according to equation (2.3) suffices. This is unless the residuals of the best fit do not demand otherwise.

It is a reasonable approach to correct the values received from a terminated calibration with the parameters of the unterminated voltage sweeps. This implies a subtraction of $V_{0,\mathrm{off}}$ and a division by G_{off} of the measured values:

$$V'_{\mathrm{lsADC}} = \frac{V_{\mathrm{lsADC}} - V_{0,\mathrm{off}}}{G_{\mathrm{off}}}. \tag{2.8}$$

This means that effectively

$$V'_{\mathrm{lsADC}} = G_{\mathrm{on}} \cdot V_{\mathrm{IN}} + V_{0,\mathrm{on}} \tag{2.9}$$

is modelled by the linear fit defined in equation (2.3). This allows to deduce the value of the terminating resistor R_{T} from the gain G_{on}. R_{T} is needed for the reconstruction of the HICANN source impedance. A detailed description of this task is outlined in section 2.3.

[2] Due to the high resolution of the lsADC most values in the data sheet are referenced to LSB.

2.2 High Speed ADC

The fundamental approach to characterize the hsADC is the same as for the lsADC. By applying a known input voltage to the individual channels of the hsADC and recording its output, one can perform a linear least squares fit of a polynomial of certain order and extract the best-fit parameters representing the calibration values. There is an additional effect to consider which is the preliminary described hsADC-internal crosstalk. A narrowed display of the hsADC input configuration for a measurement of a single channel is shown in Figure 2.2.

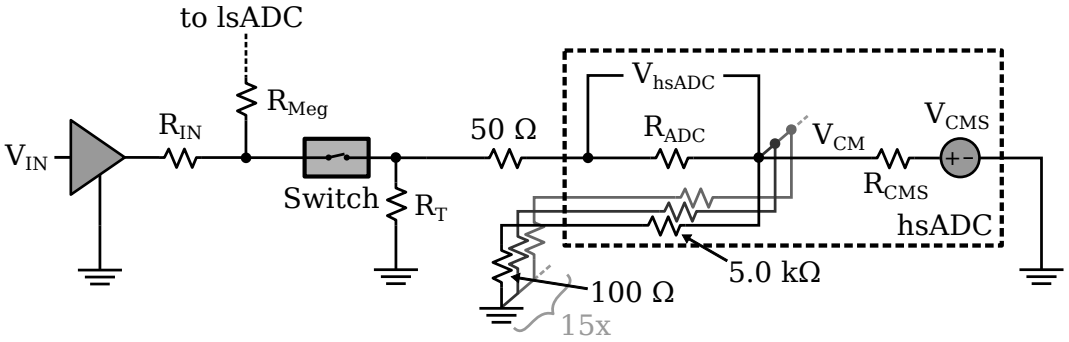

Figure 2.2: Input configuration of the hsADC for a single channel, adapted from [Ins10]. The input voltage V_{hsADC} is measured across the internal biasing resistor $R_{\mathrm{ADC}} = 5\,\mathrm{k\Omega}$. The hsADC measures differentially against the CM reference voltage. In this representation of the circuitry the CM source has been modelled with an equivalent voltage source $V_{\mathrm{CMS}} = 450\,\mathrm{mV}$ and source impedance R_{CMS} that is unknown. Further V_{CMS} is applied to all 16 channels in parallel. Because the analog switches of the remaining 15 channels are left open, their inputs are pulled to ground with $R_{\mathrm{ADC}} + 50\,\Omega + R_{\mathrm{T}} \approx 5\,\mathrm{k\Omega} + 100\,\Omega = 5.1\,\mathrm{k\Omega}$ with the $100\,\Omega$ series resistor of termination and hsADC input impedance. Therefore the CM voltage V_{CMS} is terminated an additional 15 times with $5.1\,\mathrm{k\Omega}$ each.

In this setup an arbitrary input voltage V_{IN} influences the effective common mode voltage V_{CM} by coupling in on the respective node over the internal $5\,\mathrm{k\Omega}$ biasing resistor. As a result the common mode voltage is not constant but rather a function of the input: $V_{\mathrm{CM}}(V_{\mathrm{IN}})$. Because the hsADC measures differentially against V_{CM}, a change in V_{CM} is transferred directly on the measured voltage V_{hsADC}. This means that the channel inflicts its own measurement with an uncertainty equal to the total change of V_{CM}.

The variations of the common mode voltage do not only falsify the measurement of a single channel. Measurements carried out on neighbouring channels are also affected as they are referenced to the same common mode voltage V_{CM}. The effect should be stronger the further away V_{IN} is from $2 \cdot V_{\mathrm{CM}}$ as the current through the biasing resistor $R_{\mathrm{ADC}} = 5\,\mathrm{k\Omega}$ is smallest for equal strength of the drivers. This means that in an actual experiment only one channel per hsADC could be used while leaving the remaining inputs undriven to avoid crosstalk. The influence of a channel on its own measurement could be cancelled out by applying channel specific fits. This is however not desired as it would lead to a maximum of three channels out of the total 48 that could be used in parallel.

In order to eliminate the effect of the common mode shifting the additionally reduced

schematic for a driven and an undriven channel in Figure 2.3 will be considered. Note that for the following considerations the shifted ground GSGND in Figure 1.4, on which the common mode reference voltage is operated, will not be involved as it is of no relevance for the correction. All voltages reference to the global ground GND.

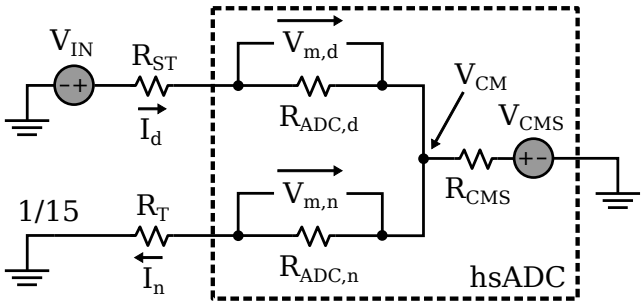

Figure 2.3: Layout for a parallel measurement of two neighboring hsADC channels. One channel is driven with an input V_{IN}, the neighboring channel is left open terminated with $R_{\mathrm{T}} = 100\,\Omega$. R_{ADC} denotes the $5\,\mathrm{k}\Omega$ internal biasing resistors over which the voltage V_{m} is measured. $R_{\mathrm{ST}} = 75\,\Omega$ is the Thévenin equivalent resistor of source impedance, termination and the $50\,\Omega$ series resistor.

The first issue to be considered is to keep track of the varying V_{CM}. A channel that is not in use is not provided with an individual input voltage V_{IN} over the closed analog switch. Hence it can measure V_{CM} against global ground. This is the hsADC output $V_{\mathrm{m,n}}$[3] in Figure 2.3. Under the assumption that $V_{\mathrm{CM}} > 0\,\mathrm{V} = V_{\mathrm{GND}}$, $R_{\mathrm{ADC,n}} = 5\,\mathrm{k}\Omega$ and the total terminating $R_{\mathrm{T}} = 100\,\Omega$ equivalent series resistor of $50\,\Omega$ termination and hsADC input impedance the following relation holds true:

$$I_{\mathrm{n}} = \frac{V_{\mathrm{CM}}}{R_{\mathrm{ADC,n}} + R_{\mathrm{T}}}. \tag{2.10}$$

I_{n} is the current from the virtual V_{CM} to global ground that flows in the neighboring channel. Hence:

$$V_{\mathrm{m,n}} = R_{\mathrm{ADC,n}} \cdot I_{\mathrm{n}} = -\frac{5000}{5100} \cdot V_{\mathrm{CM}}. \tag{2.11}$$

The resistors have been assumed to be ideal. Then the common mode voltage can be expressed by the measured voltage:

$$V_{\mathrm{CM}} = -\frac{5100}{5000} \cdot V_{\mathrm{m,n}}. \tag{2.12}$$

In the following it will be assumed that $V_{\mathrm{IN}} > V_{\mathrm{CM}}$. For $V_{\mathrm{IN}} < V_{\mathrm{CM}}$ only the sign of the measured voltage is flipped, the remaining calculations stay the same. The measured voltage on the driven channel $V_{\mathrm{m,d}}$ can be expressed as a function of V_{CM}. With the current through the driven channel

$$I_{\mathrm{d}} = \frac{V_{\mathrm{IN}} - V_{\mathrm{CM}}}{R_{\mathrm{ST}} + R_{\mathrm{ADC,d}}} \tag{2.13}$$

one receives:

$$V_{\mathrm{m,d}} = R_{\mathrm{ADC,d}} \cdot I_{\mathrm{d}} = (V_{\mathrm{IN}} - V_{\mathrm{CM}}) \cdot \frac{R_{\mathrm{ADC,d}}}{R_{\mathrm{ST}} + R_{\mathrm{ADC,d}}}. \tag{2.14}$$

Using equation (2.12) it follows that

$$V_{\mathrm{m,d}} = \left(V_{\mathrm{IN}} + \frac{5100}{5000} \cdot V_{\mathrm{m,n}}\right) \cdot \frac{R_{\mathrm{ADC,d}}}{R_{\mathrm{ST}} + R_{\mathrm{ADC,d}}}. \tag{2.15}$$

[3] The "n" stands for "neighboring".

The input voltage V_{IN} can finally be obtained from the two measurements $V_{\mathrm{m,d}}$ and $V_{\mathrm{m,n}}$ via

$$V_{\mathrm{IN}} = \frac{R_{\mathrm{ST}} + R_{\mathrm{ADC,d}}}{R_{\mathrm{ADC,d}}} \cdot V_{\mathrm{m,d}} - \frac{5100}{5000} \cdot V_{\mathrm{m,n}}. \tag{2.16}$$

This is the result for correcting the common mode influence. It is necessary to track V_{CM} with a dedicated channel and subtract it from the measured values of the driven channel with a factor of $\frac{5100}{5000}$. The factor $\frac{R_{\mathrm{ST}}+R_{\mathrm{ADC,d}}}{R_{\mathrm{ADC,d}}} = \frac{5075}{5000}$ of the first term can be left to be corrected by the calibration data obtained from a linear fit according to equation (2.3). This is due to the fact that it consists only of quantities inherent to a specific channel. The considerations above are also extensible to the influence of multiple channels disturbing the common mode in parallel as the neighboring channel records every source of error in V_{CM}. In total six channels out of the 48 inputs from the three different hsADCs need to be reserved for the tracking of the common mode. The double number of channels compared to the number of chips is due to the fact that the hsADC samples eight of its input channels at alternating clock cycles [Ins10]. Therefore six groups of eight input channels can be sampled in parallel, each demanding one reserved CM-tracking channel. These groups are called *Trigger Groups* (TG).

A Fourier transformation has been taken into consideration as an alternative approach to eliminate the common mode influence[4]. This would involve the measurement of a transfer function yielding frequency-specific weights. In a Fourier transformation of the recorded voltage trace it would then be possible to correct the different frequency components with the information from the transfer function. This does however only work under the assumption that the common mode voltage is known. Since this would involve a separate measurement of the common mode, which yields no improvement over the approach outlined before, the correction with the trace from a neighboring channel has been chosen.

Attention should be paid to the negligence of the influence of the common mode back onto the input voltage of the hsADC inputs. Let $V_{\mathrm{IN,eff}}$ be the effectively measured input voltage against the common mode voltage as shown in Figure 2.4.

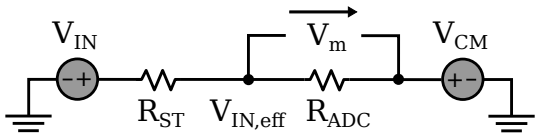

Figure 2.4: Strongly simplified sketch of the CM voltage V_{cm} coupling back in on the effective hsADC input voltage $V_{\mathrm{IN,eff}}$.

Then $V_{\mathrm{IN,eff}}$ depends on V_{CM}:

$$V_{\mathrm{IN,eff}} = V_{\mathrm{IN}} - (V_{\mathrm{IN}} - V_{\mathrm{CM}}) \cdot \frac{R_{\mathrm{ST}}}{R_{\mathrm{ST}} + R_{\mathrm{ADC}}}. \tag{2.17}$$

The change in $V_{\mathrm{IN,eff}}$ with V_{CM} is

$$\frac{\partial V_{\mathrm{IN,eff}}}{\partial V_{\mathrm{CM}}} = \frac{R_{\mathrm{ST}}}{R_{\mathrm{ST}} + R_{\mathrm{ADC}}} \approx 1.5\,\% \tag{2.18}$$

under the assumption that $R_{\mathrm{ST}} = 75\,\Omega$ using the Thévenin equivalent $25\,\Omega$ series resistor of source impedance and termination in series with the $50\,\Omega$ resistor. Compared to the error equal to the total variation of the common mode itself this is negligible.

[4]Personal communication with Joscha Ilmberger

It is also to be considered that the common mode voltage on the ANANAS is decoupled from the shifted ground with a set of different capacitors in order to prevent high frequency components from coupling in. These capacitors form an RC lowpass-filter with the hsADC-internal 5 kΩ biasing resistor. This circumstance could possibly lead to a phase shift between the trace of the actively driven and a neighboring channel tracking the common mode. However, for low frequencies, which are close to DC, this is negligible as the phase response of a low-pass filter exhibits a phase of 0 for frequencies $\nu \to 0\,\mathrm{Hz}$ [HBG17]. At high frequencies, the damping of the low-pass filter suffices to suppress these components completely. Hence, this fact has been accepted for the procedure as one is only interested in DC measurements.

There are however numerous advantages involved by this procedure:

1. The approach is more accessible than e.g. a correction via a Fourier transformation. All frequency components contributing to the disturbance of the common mode are treated equally as the circuitry consists of linear components in first approximation.

2. With the subtraction of the neighbouring channel data which measures the common mode against global ground due to the respective analog switch left open, an immediate coordinate transformation from the hsADC system to the one referenced to global ground is performed. No further calculations are necessary to perform this transformation.

3. Automated calibration routines for neuron and synapse parameters could perform much more reliable. Random steps in the membrane traces due to crosstalk from experiments over a neighbouring channel could be eliminated completely.

4. Every additional noise coupling in on the experiment from the hsADC power supply or the hsADC-internal reference voltage can also be corrected due to the channels being read out in parallel.

5. Up to 42 channels of the total 48 inputs coming from the HICANNs can be used in parallel. This is a significant improvement compared to a maximum utilization of 3 channels out of 48 without the correction.

2.3 HICANN

The last step for a full calibrated analog readout chain is the calibration of the HICANN source impedances. In general they possess a significantly larger error than the various resistors on the ANANAS board due to the more complex manufacturing process[5]. Thus they are the most important source of uncertainty and need to be known precisely.

[5] Personal communication with Joscha Ilmberger and Maurice Güttler

Usage of the lsADC is suited for the determination of the source impedances. Consider the excerpt of the ANANAS analog input configuration shown in Figure 2.5.

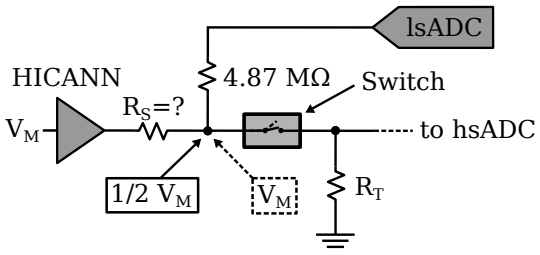

Figure 2.5: Schematic of a HICANN-attached ANANAS input configuration. Depending on the state of the analog switch either V_M or approximately $\frac{1}{2} \cdot V_\mathrm{M}$ are measured by the lsADC. R_S denotes the source impedance of the HICANN.

A two-step procedure is required to deduce the value of R_S:

1. Accurate measurement of the membrane input voltage V_M. By leaving the analog switch to the terminating resistor R_T open, the lsADC approximately measures the true source voltage as the voltage drop over R_S is negligible:

$$I = \frac{V_\mathrm{M}}{R_\mathrm{S} + 4.87\,\mathrm{M\Omega}}, \tag{2.19}$$

   hence

$$V_\mathrm{lsADC,off} = V_\mathrm{M} - R_\mathrm{S} \cdot I = V_\mathrm{M} \cdot \left(1 - \frac{1}{1 + \frac{4.87\,\mathrm{M\Omega}}{R_\mathrm{S}}}\right) \overset{R_\mathrm{S} \ll 4.87\,\mathrm{M\Omega}}{\approx} V_\mathrm{M}. \tag{2.20}$$

2. Measurement of the effective membrane input voltage while loading the source with the terminating resistor over the closed analog switch. In an ideal case of $R_\mathrm{S} = R_\mathrm{T}$ the measured voltage of the lsADC should be half of the input. By replacing the current I in equation (2.20) with

$$I = \frac{V_\mathrm{M}}{R_\mathrm{S} + 1/\left(\frac{1}{R_\mathrm{T}} + \frac{1}{4.87\,\mathrm{M\Omega}}\right)}, \tag{2.21}$$

   the equation for V_lsADC changes to:

$$V_\mathrm{lsADC,on} = V_\mathrm{M} \cdot \left(\frac{R_\mathrm{S}}{R_\mathrm{S} + 1/\left(\frac{1}{R_\mathrm{T}} + \frac{1}{4.87\,\mathrm{M\Omega}}\right)}\right) \overset{R_\mathrm{T} \ll 4.87\,\mathrm{M\Omega}}{\approx} V_\mathrm{M} \cdot \frac{R_\mathrm{T}}{R_\mathrm{S} + R_\mathrm{T}}. \tag{2.22}$$

The value of R_T is gathered in the calibration of the lsADC for each channel individually. With the known terminating resistor R_T it is possible to deduce R_S via

$$R_\mathrm{S} = R_\mathrm{T} \cdot \left(\frac{V_\mathrm{lsADC,off}}{V_\mathrm{lsADC,on}} - 1\right). \tag{2.23}$$

The input membrane voltage should be adjusted to be constant in order to properly measure the sourced voltage V_M. This can be controlled with the neuron parameters of the HICANN, particularly ensuring that the leak potential is much smaller compared to the threshold potential.

3 Calibration Routine and Evaluation

A setup for the calibration of the two ADCs on the ANANAS board will be introduced in the following. The used hardware as well as the required software stack will be described shortly. Further the evaluation of data gathered throughout multiple tests of the calibration routines, which were outlined in chapter 2, will be presented. On the foundation of the investigated long-term stability of calibration data, the necessary order of the fit describing the characteristic curves of the ADCs can be estimated. This means that if the errors evoked by gain and offset drifts over a long period of time dominate the systematic error due to a linear approximation of the characteristic curve of the ADCs, it is not necessary to increase the order of the fit. Finally the setup for the determination of the HICANN source impedances will be outlined, accompanied by an exemplary readout of a spiking membrane trace.

3.1 ANANAS Calibration Setup

The calibration of the ANANAS can in general be considered completely detached from the HICANN-related measurements. One objective is to attach the ANANAS boards permanently to the wafer modules in the BrainScaleS system. Thus, the calibration setup should be adaptable to future constraints given by the layout of the experiment. An introduction to the design choices made for a proper calibration routine will be given in this section.

3.1.1 Hardware Overview

For the calibration of both the lsADC and the hsADC the setup depicted in figure 3.1 has been used.

The general approach for any calibration of a system is the comparison of the system's output with the expected value. For the ANANAS this means a sweep of precisely known voltages is applied to the analog inputs with the use of a *Keithley 2635B System SourceMeter Instrument* [Kei12]. The source meter output is measured in parallel for each step within the voltage sweep with the integrated multimeter. In order to avoid re-routing of the coaxial cable output for every analog input channel the inputs are shorted on the ANANAS board. Hence, every channel receives the identical input voltage. A picture of the adapter can be seen in figure 3.2.

Due to the shortening of the analog inputs a single channel of the lsADC experiences a slightly different termination. This arises from the 47 additional 4.87 MΩ impedances

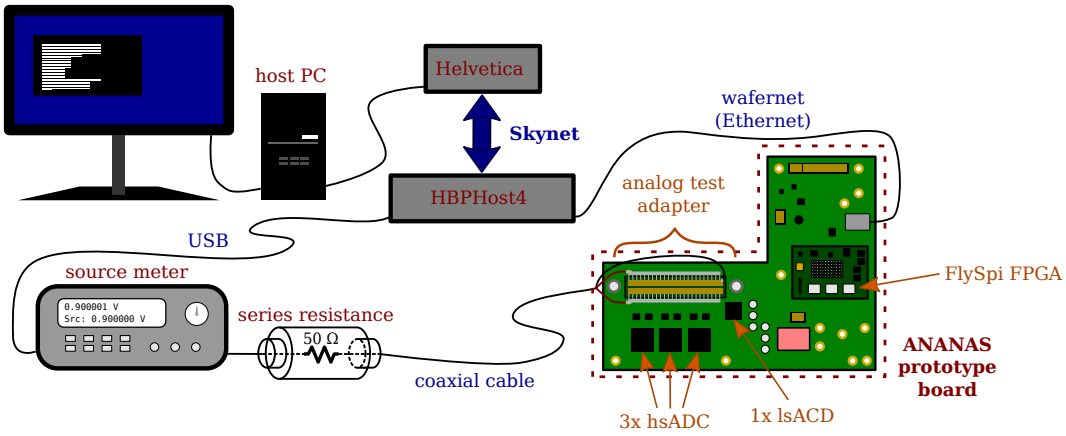

Figure 3.1: Sketch of the setup used for the calibration of the ANANAS. The calibration script is send from a host PC to the cluster via the frontend `Helvetica`. The actual script is run on the dedicated cluster node `HBPHost4`. An USB connection transmits control commands to the source meter. The sourced voltage is applied to the analog input header of the ANANAS with 50 Ω source impedance through a coaxial cable. Shortened inputs on an analog test adapter distribute the sourced voltage equally to all inputs of the lsADC. By closing the analog switches via slow-control using the FPGA, the hsADC can also be accessed. The ADC data can either be written to the FPGA-internal RAM and then read out afterwards or live streamed directly back to the host via an Ethernet connection. The cluster nodes are located in the racks of the BrainScaleS system. Thus, the source meter can without further ado be placed next to the setup and routed to the cluster and the wafer-attached ANANAS board.

leading to the remaining channels. This configuration differs from an actual experiment as only one 4.87 MΩ resistor is parallel connected to the 50 Ω termination. The influence of the additional high impedances can, however, be neglected. This can be shown by the calculation of the total resistance R_{tot}:

$$R_{\text{tot}} = \frac{1}{\frac{48}{4.87\,\text{M}\Omega} + \frac{1}{50\,\Omega}} \approx 49.975\,\Omega \approx 50\,\Omega. \tag{3.1}$$

Operating the source meter as a voltage source enables a low output impedance of the device [Kei12]. Hence, the source impedance has to be adjusted manually in order to provide test conditions comparable to a real experiment on the wafer. An adapter providing an additional 50 Ω series resistor that can be attached to the source meter output has been made. The component can be seen in figure 3.3. The framework has been chosen such that it provides male and female connectors allowing for seamless integration in the connection scheme of the setup in figure 3.1. Four 200 Ω wire-wound resistors have been soldered in parallel between the pins of the inner conductor. This leads to a total output resistance of $R_{\text{S,ad}} = \frac{200\,\Omega}{4} = 50\,\Omega$. With an assumed tolerance of $\frac{\Delta R}{R} \approx 1\,\%$ for the individual resistances R the error of the source impedance[1] is then:

$$\Delta R_{\text{S,ad}} = \frac{\Delta R}{4} = 0.5\,\Omega. \tag{3.2}$$

The resistance $R_{\text{S,ad}}$ of the source impedance adapter has been measured with a *Keithley 2100 Digital Multimeter* [Kei07] using a four-wire[2] resistance measurement:

[1] Under the assumption that the commercial resistors are Gaussian distributed.

[2] Two-wire methods are not recommended for low impedance measurements $R < 1\,\text{k}\Omega$ due to the strong influence of possible voltage drops over the lead resistances of the measuring device [Kei07].

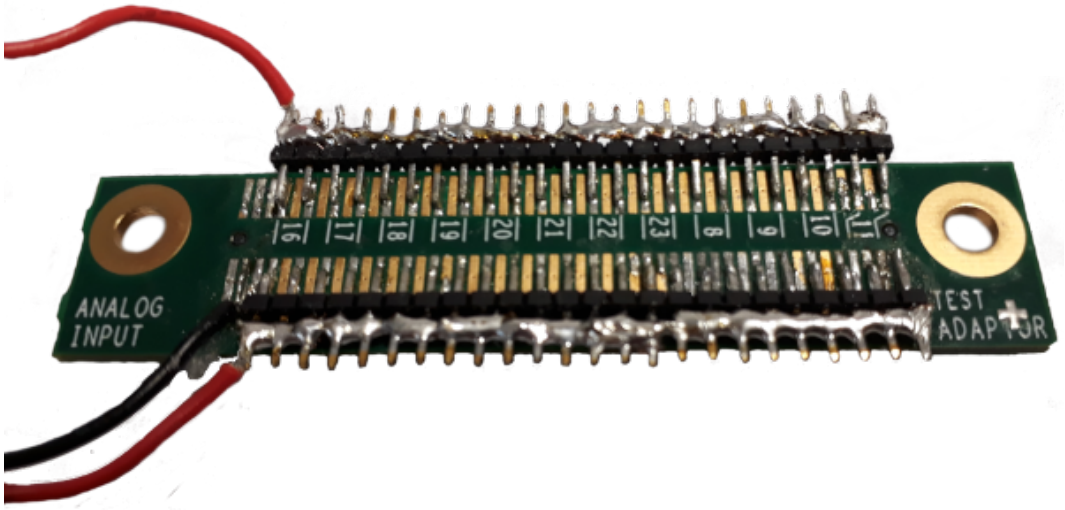

Figure 3.2: Analog input test adapter. The 48 input channels are shorted by bridging every second pin with 2 mm multi-pin connectors and soldered copper wire. Pins left open are connected to global ground. The SM output is distributed to both sides of the adapter with separate wires branched off from the inner conductor of the coaxial cable (Red) while the shielding is connected to ground (Black).

$$R_{\mathrm{S,ad}} = (49.85 \pm 0.05)\,\Omega. \tag{3.3}$$

Here, the uncertainty has been estimated from the variation of the measured value over the time of the measurement procedure. The obtained value lies well within the estimated error range from equation (3.2). This value can explicitly be used to determine the value of the terminating resistors R_{T} on the ANANAS. Hence, the precision of the measurement of R_{T} is limited by the total error of $R_{\mathrm{S,ad}}$ next to the precision of the lsADC, which has been evaluated in section 3.2.2. This is also a limiting factor for the precision of the source impedance of the HICANNs. Yet, an error of magnitude 10^{-2} should be acceptable.

Figure 3.3: Series resistor adapter for buffering the SM output with 50 Ω source impedance. Four 200 Ω resistors have been soldered in between the inner conductor pins of the adapter. Heat-conductive paste has been used to offer heat exchange with the environment over the metal frame.

3.1.2 Software Requirements

If not referenced otherwise, all software mentioned in the following has been developed group-internally. The calibration routine is building up on the Python-based, `Labcontrol` measurement device control software. To enable usage of the source meter the library `lib-keithleysourcemeter` has to be included in the project which provides the necessary Python-wrapping features. Also the slow-control access via `sctrltp` falls back on a Python-wrapped library that is `pysctrltp`. This allows to describe the whole communication with the source meter and the FPGA over a single Python script. The script includes setting and reading back the input voltages to the ANANAS frontend, the request and receive data commands to the ADCs as well as the control of the analog switches and status readouts of the FPGA. The software has been built with the build automation tool `Waf` [Nag18] and run using `singularity` [Inc18] containers. The calibration scripts, which have been developed in the framework of this thesis, are available on the group-internal *git* server as part of the `ananas-calibration` repository[3].

3.2 lsADC Calibration

This section will discuss the application of the previously in section 2.1 outlined steps for a full calibration of the lsADC. After a clarification of the important characteristics of the lsADC the calibration routine will be explained on the basis of data from a single channel. The calibration is split up into the analysis of terminated and unterminated data. By measuring the value of the 48 terminating resistors of each channel, the basis for the determination of the HICANN source impedances will be provided. Subsequently, the quality of the calibration will be broke down with regard to the order of the performed polynomial fit, the long-term stability of the calibration values and by comparing measurements with the output of an oscilloscope.

3.2.1 lsADC Characteristics

It is important to settle two characteristic quantities of the lsADC, the first one being the LSB. For the *DDC264CK* [Ins16] which is assembled on the ANANAS prototype board, a maximum input charge range of $Q_{\text{range,max}} = 150\,\text{pC}$ and a minimum settable integration time of $t_{\text{int,min}} = 160\,\mu\text{s}$ can be found. Together with the high input impedance $R_{\text{meg}} = 4.87\,\text{M}\Omega$ this yields a full scale range voltage V_{FSR} of:

$$V_{\text{FSR}} = R_{\text{meg}} \cdot \frac{Q_{\text{range,max}}}{t_{\text{int,min}}} \approx 4.56\,\text{V}. \tag{3.4}$$

The lsADC has a resolution of 20 bit thus the LSB is

$$1\,\text{LSB} = \frac{V_{\text{FSR}}}{2^{20} - 1} \approx 4.35\,\mu\text{V}. \tag{3.5}$$

[3] status at handing in thesis: git commit 19 900 755

The *DDC264C* chips of the lsADC used on the revised versions of the ANANAS are twice as slow as the *DDC264CK*, resulting in a maximum FSR of approximately 2.28 V. This has to be kept in mind when comparing the calibration parameters presented in this thesis with future calibration values of other ANANAS boards. In general the gain values of future calibrations with the correct lsADC version should be greater by a factor of 2. Yet, for all upcoming calculations the settings outlined above have been used.

The second characteristic is an artificial offset of the lsADC which allows to measure small negative currents through the analog inputs. The data sheet reports this negative FSR to be approximately −0.4 % of the positive FSR [Ins16]. For a 20 bit ADC this corresponds to a bias of $V_{0,\mathrm{art}} = 4096\,\mathrm{LSB}$ for an input current $I = 0\,\mathrm{A}$. In this thesis this value has been used for the theoretical conversion of lsADC output to ideal values together with the LSB calculated above. These values have been used as a reference to the calibrated output values.

Since the lsADC offers such a high precision compared to other ADCs, it is important to know the impact of noise within the setup that the device is used in. Erroneous readouts of the actual input voltage could for example be evoked by thermal noise or noise produced by the power supply. The lsADC itself does also contribute to a limited precision via noise inherent from the integrators and the on-chip ADCs. An analysis of the various possible sources of noise and the total measurement noise for the prototype has been given in [Ilm17].

The measurement of the total noise presented in [Ilm17] has been reproduced for comparison using the setup presented in section 3.1.1. Here, all on-board analog switches have been opened to avoid influence of the common mode voltage supply on the measured node. Additionally, all inputs have been shorted with global ground in order to provide an ideal input voltage. Then the output of a single lsADC channel has been read out 100 000 times, resulting in a total number of 50 000 samples for each integration side. The distribution of the output values from a single integrator for the *DDC264CK* with the *ADR3440* used as voltage reference is shown in Figure 3.4. The distribution shows a standard deviation of approximately 24 LSB which is

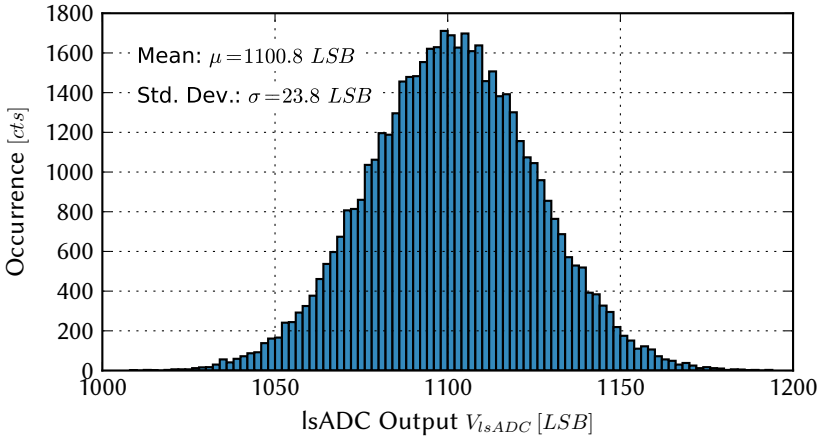

Figure 3.4: The output distribution of lsADC channel 63 at ideal grounded input on the *DDC264CK* [Ins16] with *ADR3440* [Dev18] voltage reference.

slightly larger but consistent in magnitude with the grounded input measurement in [Ilm17]. Here, a standard deviation of 22 LSB has been measured.

In order to improve the single sample noise a reduction of the reference voltage noise has been taken into account [Ilm17]. The *LT6654AHS6* [Dev17] reference voltage IC has been assembled on a different ANANAS board because it promises an improved output voltage noise by a factor of 10^{-34} compared to the *ADR3440*[5]. Another measurement of the total grounded input noise has been executed with this board. The distribution of lsADC output values for the updated lsADC voltage reference can be seen in Figure 3.5. The distribution exhibits a shifted mean compared to

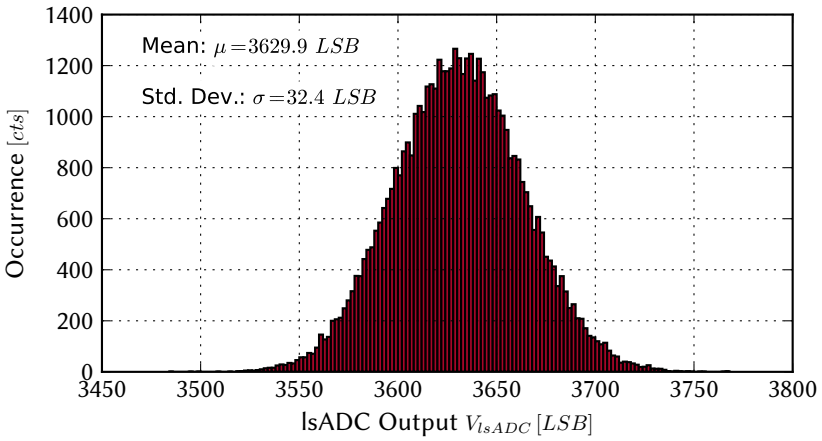

Figure 3.5: lsADC channel 63 ideal ground output distribution on the *DDC264CK* [Ins16] with *LT6654AHS6* [Dev17] voltage reference on the revised ANANAS board. The standard deviation is significantly larger than for the prototype board with the *ADR3440* reference voltage.

the one displayed in Figure 3.4. This might have been due to the examination of a channel on a different ANANAS board. The standard deviation of approximately 32 LSB is considerably larger than for the prototype board with the other voltage reference. The reasons for this fact have not been investigated further but it has to be kept in mind when considering the reduction of statistical errors in measurements with boards different from the prototype examined in the framework of this thesis.

3.2.2 Calibration Routine

The calibration of the lsADC is divided into two parts. Measurements without termination yield the characteristic behaviour of the lsADC itself whereat those with termination allow a deduction of the value of the terminating resistors. Since the calibration data of an unterminated sweep is required for this step, the calibration routine for a configuration without terminating resistor will be considered firstly.

Unterminated Calibration

As explained in section 2.1 a voltage sweep from $V_{\mathrm{SM}} = 0\,\mathrm{V}$ to $1.8\,\mathrm{V}$ with the source meter while recording the lsADC output and the sourced voltage as a reference is applicable for the acquisition of calibration data for the different channels. It is necessary to separate the data of different integrators from the same lsADC channel. This can be seen in the enhanced excerpt of the output values V_{lsADC} in voltage sweep displayed in Figure 3.6. The output values received from the lsADC have

[4] $1.6\,\mathrm{ppm_{PP}}$ [Dev17]
[5] $10\,\mu\mathrm{V_{PP}}$ [Dev18]

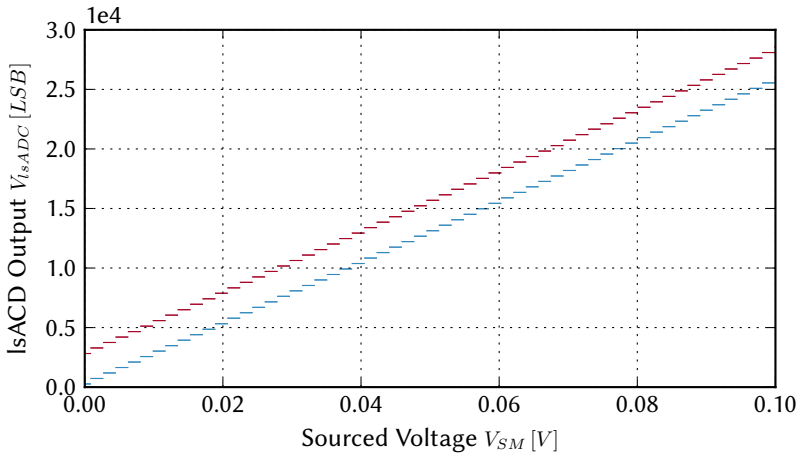

Figure 3.6: Comparison of the lsADC output from two different integrators of the same channel. Blue: Integrator A. Red: Integrator B. The offset of approximately 3000 LSB could be due to variations of the operating amplifiers or a mismatch in the integration time.

been separated between different integration sides with a specific bit in the raw data coming from the FPGA. This bit is set or unset with respect to the integrator that has been used. An offset of approximately 3000 LSB can be observed. The gain factor could also vary between different integrators, resulting in additional deviations at higher input voltages. In the data sheet [Ins16] an offset error match between both integration sides of the same input of approximately 150 LSB is reported. This could for example be due to variations of the operating amplifiers. This is not enough to explain the observed difference. A mismatch in the integration time could also be taken into account whereat the data sheet does not report an error for this quantity. The high impedance input resistor of 4.87 MΩ can, however, be excluded as it is shared by both integration paths. The explicit cause of the offset does, however, not have to be known for a correct calibration of the lsADC because of the separation of calibration data between the integration side.

Now considering the complete range of input values, Figure 3.7 shows the resulting voltage trace from channel 46 of the chip for a precise sweep with 1000 voltage steps. The step size is approximately 2 mV, which has been arbitrarily chosen to sample the characteristic curve appropriately. 100 samples $V_{\mathrm{lsADC,i}}$ have been recorded for each of the total 48 input channels, at every voltage step respectively. Due to the alternating sampling of the input over two different integrators the total number of samples per integrator is divided by two. Thus, approximately $N = 50$ remaining samples[6] are used to receive an average output V_{lsADC} per step:

$$V_{\mathrm{lsADC}} = \frac{1}{N} \sum_{i=0}^{N} V_{\mathrm{lsADC,i}}. \tag{3.6}$$

The error of the mean $\Delta V_{\mathrm{lsADC}}$ is obtained by scaling down the standard deviation $\sigma_{V_{\mathrm{lsADC}}}$ from the set of measured values per step by the square root of the total number of samples N:

$$\Delta V_{\mathrm{lsADC}} = \frac{\sigma_{V_{\mathrm{lsADC}}}}{\sqrt{N}}. \tag{3.7}$$

This error is then considered in the fit routine. The lsADC output V_{lsADC} is plotted as a function of the sourced voltage V_{SM} in Figure 3.7. The best-fit gain G and offset V_0 from a linear least squares fit to the data according to equation (2.3) are also

[6] Depending on possible loss of packages via slow-control communication.

displayed. Further, the residuals of the measured values from the linear best-fit are shown in the plot below. They are displayed in units of the error $\Delta V_{\mathrm{lsADC}}$ for every voltage step.

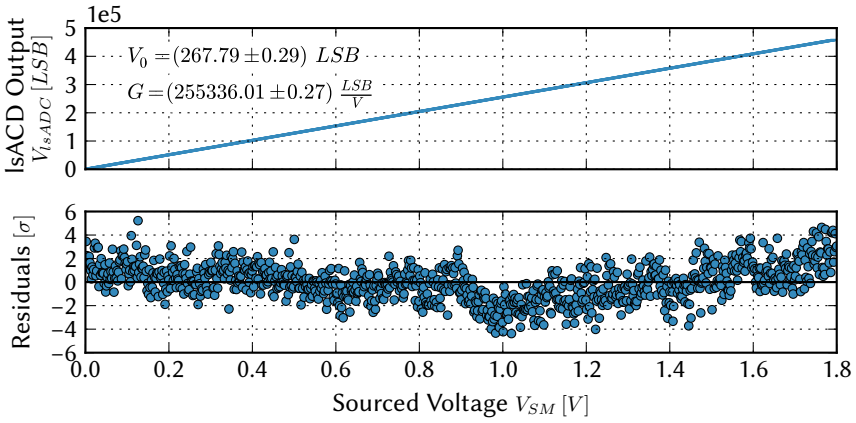

Figure 3.7: Single lsADC channel 46 voltage sweep. Top: Recorded lsADC output as a function of the sourced input voltage from the SM. Each displayed point corresponds to the mean of approximately $N = 50$ samples taken per voltage step. Bottom: Linear best-fit residuals normalized by the error of the mean output $\frac{\sigma_{V_{\mathrm{lsADC}}}}{\sqrt{N}}$ per voltage step.

One can notice that the residuals of the characteristic curve exhibit systematic deviations larger than $3\,\sigma$ from the linear best-fit in the boundary areas at $V_{\mathrm{SM}} \approx 0\,\mathrm{V}$ and $V_{\mathrm{SM}} \approx 1.8\,\mathrm{V}$ as well as the center of the swept voltages at $V_{\mathrm{SM}} \approx 1.0\,\mathrm{V}$. The trend of the residuals is the same for different channels of the lsADC. This can be seen by comparing the observed deviations with another channel. The recorded trace and the residuals from a linear best-fit for channel 63 on the same chip are depicted in Figure 3.8.

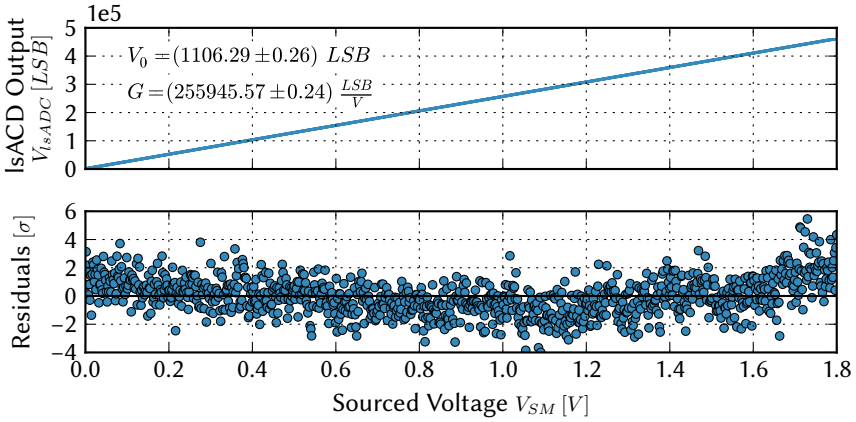

Figure 3.8: Single lsADC channel 63 voltage sweep for comparison of the residuals obtained from a linear fit. The coarse shape of the trend of the residuals is consistent with the one observed in Figure 3.7. This means that, with high probability, the same fit function should be applicable to all channels of the lsADC.

For further investigation of the quality of the linear fit the histogram of all residuals for the specific sweep of channel 46 are shown in Figure 3.9.

The distribution is not perfectly symmetrical. In order to quantify the systematic error arising from the fit one could use the width of the distribution of residuals which has been calculated to 4.4 LSB. However as one is interested in the error corresponding to specific input voltages it might be more reasonable to check the influence of a higher order polynomial function. In order to do this, an additional fit with a polynomial of second order has been performed to the data:

$$P(x) = a \cdot x^2 + b \cdot x + c. \tag{3.8}$$

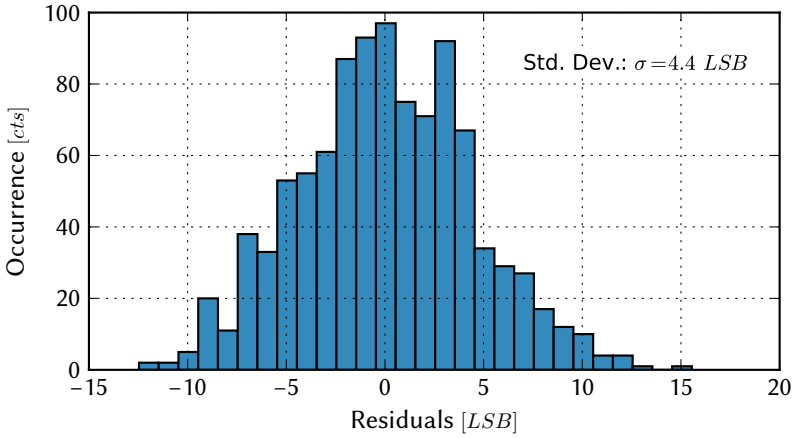

Figure 3.9: Histogram of residuals from a linear least squares fit with polynomial of first order for lsADC channel 46 voltage sweep. The distribution possesses a slight displacement to smaller negative deviations but spreads wider in the positive range.

The resulting residuals of the data from a quadratic linear least squares fit can be seen in Figure 3.10.

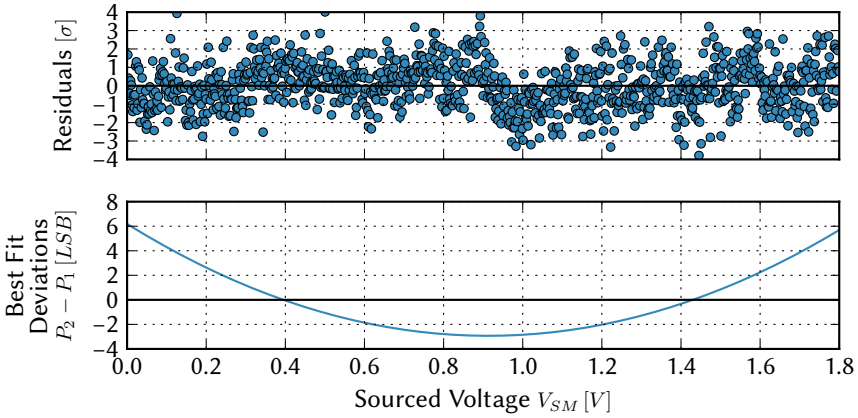

Figure 3.10: Comparison of linear fit function with polynomial fit of second order, assumed as a better characteristic of the lsADC. Top: Residuals from linear least squares fit with polynomial of second order. Bottom: Difference between quadratic and linear best fit as a function of sourced voltage.

The residuals in the upper plot still do not lie completely uniformly around zero, but most of the deviations are within the $3\,\sigma$ range. Therefore, the quadratic fit has been assumed as the better characteristic curve for the following considerations. Let P_1 denote the linear best-fit corresponding to equation (2.3) with the respective best-fit parameters shown in Figure 3.7 and P_2 the best-fit of second order. In the lower plot of Figure 3.10 the difference

$$D = P_2 - P_1 \tag{3.9}$$

of the two fits is displayed as a function of the sourced voltage V_{SM}. One can observe that the largest deviations occur at the boundary areas of the sweep. There, a maximum error of approximately 6 LSB arises compared to the characteristic curve from the quadratic fit used as reference.

A single measurement with the lsADC in an experiment is afflicted with both a systematic and a statistical error. The systematic error of 6 LSB can now be compared to the total statistical error due to noise. It is then possible to estimate the minimum number of samples N to be taken per voltage step in order to let the statistical error $\sigma_{V_{\mathrm{lsADC}}}$ become insignificant in comparison to the systematic error. By converting equation (3.7) and interpreting the error of the mean $\Delta V_{\mathrm{lsADC}}$ as the maximum

deviation from the true characteristic curve of 6 LSB one can find:

$$N = \left(\frac{\sigma_{V_{\mathrm{lsADC}}}}{\Delta V_{\mathrm{lsADC}}}\right)^2 \approx \left(\frac{24\,\mathrm{LSB}}{6\,\mathrm{LSB}}\right)^2 = 16. \tag{3.10}$$

This means that a minimum of 16 samples per voltage step taken from the lsADC channels per integrator should not be undercut in a calibration sweep in order to sufficiently sample the characteristic curve of the lsADC channels.

The required order of polynomial fit is, however, not solely dependent on the maximum deviation from the true characteristic curve. Long-term effects such as for example drifts due to temperature variations also have to be taken into account when discussing the necessary precision. If a calibration of high order shows a poor robustness in the context of its stability over a long period of time, it is not necessary to perform a fit of such high precision. This issue will be investigated further in section 3.2.3

Terminated Calibration

After the unterminated calibration has been carried out, the lsADC specific calibration data can be used to extract the impact of the terminating resistor on a measurement with closed analog switches. In large part, the routine is the same as for the unterminated calibration. The most important factor to keep in mind is to close only one specific analog switch and leave the remaining ones open. Due to the shorted inputs on the analog test adapter a falsification of the measurements through additional terminating resistors coupling in on the measured node should be avoided.

The connected inputs on the adapter allow for a calibration of all terminations with a single lsADC channel. Every individual terminating resistor on the board can be seen by every input channel. This reduces the number of channels to be calibrated in an unterminated configuration to 1 for a complete determination of all resistor values. Then, a voltage sweep corresponding to the measurements without termination can be applied for the 48 possible configurations with every individual terminating resistor. After subtracting the channel- and integrator-specific offset calibration value $V_{0,\mathrm{off}}$ from the lsADC output values and dividing them by the acquired gain factor G_{off}, the resulting voltage trace has been converted to V. It does also only exhibit offset and gain variations due to the termination and the impact of the common mode voltage V_{CM} on the measured node.

Note that for the execution of a linear least squares fit on the calibrated data also the errors of each data point have been modified. This has been done according to Gaussian error propagation for correlated measurements. Gain G and offset V_0 are assumed to be correlated for the unterminated sweep, which has been confirmed by investigating the covariance matrix originating from the chosen fit routine. Let $V_{\mathrm{lsADC,on}}$ denote the measured lsADC output values with calibration applied, G_{off} and $V_{0,\mathrm{off}}$ the calibration values obtained from an unterminated sweep with errors ΔG_{off}, $\Delta V_{0,\mathrm{off}}$ and covariance $Cov\,(G_{\mathrm{off}}, V_{0,\mathrm{off}})$. V_{lsADC} is the measured output averaged over N samples with statistical error $\sigma_{V_{\mathrm{lsADC}}}$. Then, the following equations hold:

$$V_{0,\mathrm{on}} = \frac{V_{\mathrm{lsADC}} - V_{0,\mathrm{off}}}{G_{\mathrm{off}}} \tag{3.11}$$

and therefore

$$\begin{aligned}\Delta V_{0,\mathrm{on}} &= \left[\left(\frac{\partial V_{0,\mathrm{on}}}{\partial V_{0,\mathrm{off}}}\cdot\Delta V_{0,\mathrm{off}}\right)^2+\left(\frac{\partial V_{0,\mathrm{on}}}{\partial G_{\mathrm{off}}}\cdot\Delta G_{\mathrm{off}}\right)^2+2\cdot Cov\cdot\frac{\partial V_{0,\mathrm{on}}}{\partial V_{0,\mathrm{off}}}\cdot\frac{\partial V_{0,\mathrm{on}}}{\partial G_{\mathrm{off}}}\right]^{1/2}\\ &= \left[\left(-\frac{\Delta V_{0,\mathrm{off}}}{G_{\mathrm{off}}}\right)^2+\left(\frac{V_{\mathrm{lsADC}}-V_{0,\mathrm{off}}}{G_{\mathrm{off}}^2}\cdot\Delta G_{\mathrm{off}}\right)^2\right.\\ &\qquad\left.+2\cdot Cov\left(G_{\mathrm{off}},V_{0,\mathrm{off}}\right)\cdot\frac{V_{\mathrm{lsADC}}-V_{0,\mathrm{off}}}{G_{\mathrm{off}}^3}+\left(\frac{\sigma_{V_{\mathrm{lsADC}}}}{G_{\mathrm{off}}}\right)^2\right]^{1/2}.\end{aligned} \tag{3.12}$$

Figure 3.11 depicts the calibrated trace for a sweep with channel 46 and analog switch 42 set. The slope of the resulting trace for V_{lsADC} as a function of the sourced

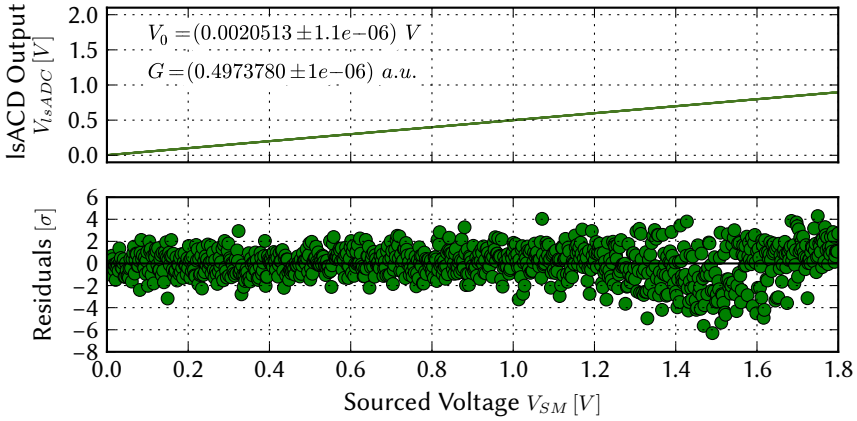

Figure 3.11: Terminated single lsADC channel 46 voltage sweep with analog switch 42 activated. Due to the application of unterminated calibration data, the lsADC output is already converted to V. The trace possesses a slope of approximately 0.5 due to the voltage divider originating from the source impedance and the termination.

voltage V_{SM} is approximately 0.5 which corresponds to the expectations described in section 2.1. Again, a linear least squares fit of first order according to equation (2.3) has been chosen to model the trend of the recorded lsADC output trace. Regarding the quality of the chosen fit function, the residuals of the best-fit are displayed in the plot on the bottom of Figure 3.11. They do not show a significant excess from zero in the range of 0 V to 1.0 V. Furthermore, they seem to be uniformly distributed in this area, which confirms the selection of a linear fit function. However, slightly significant deviations from the true measured output values become visible in the range from 1.2 V to 1.8 V. Here, they dip towards smaller voltages.

The source of these deviations is not known precisely yet. A possible explanation could be an interference of the 1.8 V analog supply voltage of the on-chip ADC from the hsADC [Ins10]. Since the hsADC is operated on a shifted ground voltage of −1.15 V, the analog supply voltage is 650 mV referenced to global ground. One could argue that the deviations in Figure 3.11 start to become significant at a sourced voltage of approximately 1.3 V. Due to the voltage divider this would result in an effective voltage of 650 mV at the common node of lsADC and hsADC input yielding the same range as the analog supply voltage. However, due to the high precision of the the sweep with 50 samples per voltage step and integrator, the deviations are only a few LSB and have been accepted for the moment. It will be proved that this assumption is correct in the context of long-term stability of the calibration.

Since the calibration of the lsADC characteristics have already gone into the acquisition of terminated calibration data, a major source of error has been eliminated at this point. Hence, it is possible that a smaller number of samples and voltage steps would suffice for a good calibration result. This would be desirable in the context of the total runtime for a full calibration of the ANANAS board. Six unterminated calibration sweeps have to be carried out with high precision due to the parallel recording of eight channels per trigger group. This corresponds to a runtime of approximately 25.6 min. For the terminated calibration though all 48 terminations have to be swept separately, increasing the runtime of the calibration at the same precision by a factor of 8.

A considerably degraded sweep with 10 voltage steps and the minimal required number of 16 samples per step has been carried out shortly after the sweep presented in Figure 3.11. This was done to minimize the impact of temperature variations in order to compare the fit results obtained from both measurements. For the complete sweep of all 48 channels, the runtime was approximately 1.8 min. In contrast to an expected runtime of approximately 200 min for a sweep with 1000 samples per step, this is a significant improvement. The resulting trace and linear best-fit residuals can be seen in Figure 3.12. The obtained gain factor G differs from the factor received in

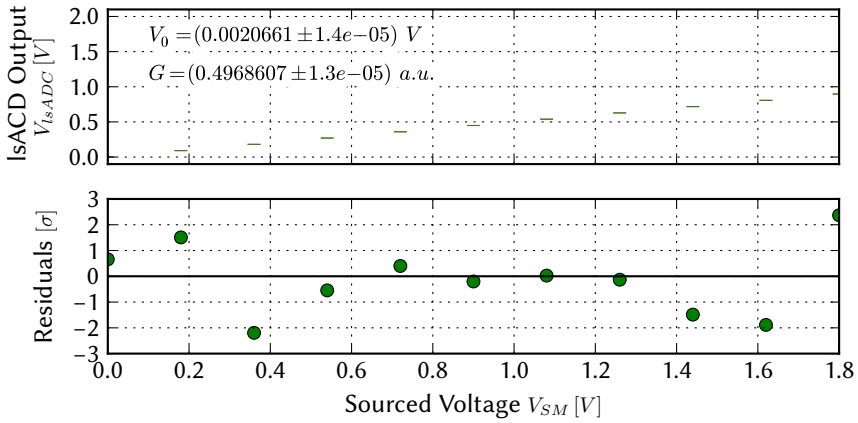

Figure 3.12: Terminated output trace and linear best-fit residuals for single lsADC channel 46 voltage sweep with activated analog switch 42 at reduced number of samples and voltage steps.

the high precision sweep on an order of 5×10^{-4}. This error is smaller than the error of the $R_{\mathrm{S,ad}} = (49.85 \pm 0.05)\,\Omega$ source impedance adapter[7] by an order of 10^{-2}. Thus, it is negligible as the main source of error is the external source impedance of the source meter.

Accordingly, the terminating resistor values R_{T} have been determined by using sweeps with a reduced number of samples and voltage steps only. Consider the simplified circuit including a voltage source V_{S} with source impedance R_{S} and the terminating resistor R_{T} displayed in Figure 3.13. The voltage dropping off at the terminating resistor is denoted with V_{T} and the current I is assumed to flow through the two resistors R_{S} and R_{T} only. For the following calculations the influence of the common mode voltage on the node seen by R_{T} has been neglected as the evoked error should be on the order of 1 %. In order to see this, compare Figure 1.4. The ratio of hsADC-internal biasing resistor and the 50 Ω input impedance is $\frac{50}{5000} \approx 0.01$.

[7] Compare section 3.1.1.

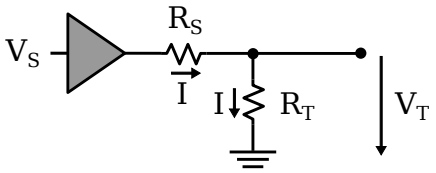

Figure 3.13: Schematic for the determination of the terminating resistor values R_T.

Without offset errors to be considered the gain G_on received from the terminated sweep describes the relative amplifying of the voltage over the termination V_T compared to the input voltage V_S:

$$G_\mathrm{on} = \frac{V_\mathrm{T}}{V_\mathrm{S}}. \tag{3.13}$$

The ratio $\frac{V_\mathrm{T}}{V_\mathrm{S}}$ can also be deduced over the current I flowing through the circuit:

$$I = I_\mathrm{S} = I_\mathrm{T} = \frac{V_\mathrm{S}}{R_\mathrm{S} + R_\mathrm{T}}. \tag{3.14}$$

This yields

$$\frac{V_\mathrm{T}}{V_\mathrm{S}} = \frac{I \cdot R_\mathrm{T}}{I \cdot (R_\mathrm{S} + R_\mathrm{T})} = \frac{R_\mathrm{T}}{R_\mathrm{S} + R_\mathrm{T}} \tag{3.15}$$

and, therefore, by using equation (3.13)

$$R_\mathrm{T} = \frac{G_\mathrm{on}}{1 - G_\mathrm{on}} \cdot R_\mathrm{S}. \tag{3.16}$$

Under negligence of the gain error ΔG compared to the uncertainty of the source impedance the error of the termination is

$$\Delta R_\mathrm{T} = \frac{G_\mathrm{on}}{1 - G_\mathrm{on}} \cdot \Delta R_\mathrm{S}. \tag{3.17}$$

The 48 terminations R_T have been determined for the ANANAS prototype board with this procedure. The resulting histogram of the termination values is displayed in Figure 3.14.

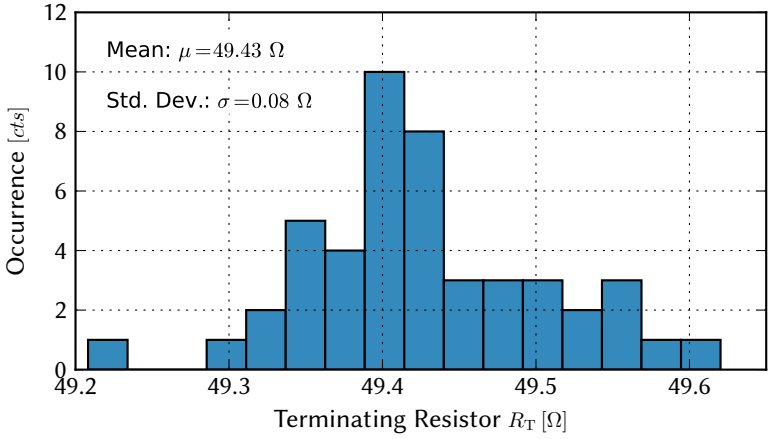

Figure 3.14: Distribution of terminating resistor values R_T for the ANANAS prototype board. The standard deviation of 0.08 Ω is slightly better than the expected 1 % error for the resistors assembled on the board.

The distribution exhibits a standard deviation of approximately 0.08 Ω, slightly exceeding the expected precision of 1 % for the resistors on the board. The E series

value of the used resistors is 49.9 Ω, which is approximately 1 % larger than the calculated values from above. A possible reason for this could be the negligence of the common mode voltage impact of 1 % on the node where V_T drops off in Figure 3.13. Since the spread of the HICANN source impedances is assumed to be much larger than the 1 % uncertainty inherent to the terminations R_T, this circumstance has been accepted.

3.2.3 Calibration Quality and Long-Term Stability

After the calibration routine of the lsADC has been introduced theoretically and explained on the basis of the data from a single channel, the quality of calibration data is examined in the following section. The spread of uncalibrated data and such that has undergone a correction with the acquired calibration data will be investigated. Additionally, a comparison of a signal provided by a function generator recorded with the lsADC and an oscilloscope will test the correct range of output values received by the calibration. Finally, the routine will be judged with regard to its stability over a long period of time and its robustness against external temperature variations.

Comparison of Pre- and Post-Calibration Data

To receive a first impression on how the calibration of the lsADC improves precision and accuracy of the output values across all 48 input channels, the data used for the acquisition of the calibration parameters G_{off} and $V_{0,off}$ in the unterminated sweep can be used a second time. Since approximately 50 samples per integrator and 100 per channel received at each voltage step exceed the minimal required number of 16 samples needed to suppress the statistical error in comparison to the systematic one, the lsADC output is well-known. The output received in [LSB] can now be converted to a voltage in two ways:

1. Ideal conversion via subtraction of the artificial biasing offset $V_{0,art}$ and multiplication with the previously calculated $1\,\text{LSB} \approx 4.35\,\mu\text{V}$.

2. Conversion by subtracting the received offset value $V_{0,off}$ and division of the remaining value by the gain factor G_{off}.

The histograms presented in Figure 3.15 and 3.16 represent the distributions of lsADC output values in volt across all 48 input channels obtained with a theoretical conversion and an application of calibration data, respectively.

A reference sourced input voltage of $V_{SM} = 102.59\,\text{mV}$ has been recorded with the measuring function of the source meter. This value is displayed in Figure 3.15. It can be seen that both distributions of the 48 different output values spread to lower and higher values around the reference voltage. The single values obtained by ideal conversion, however, exhibit a wider displacement with respect to the reference value, which is on an order of $10^{-3}\,\text{V}$. The calibrated values show maximum deviations on

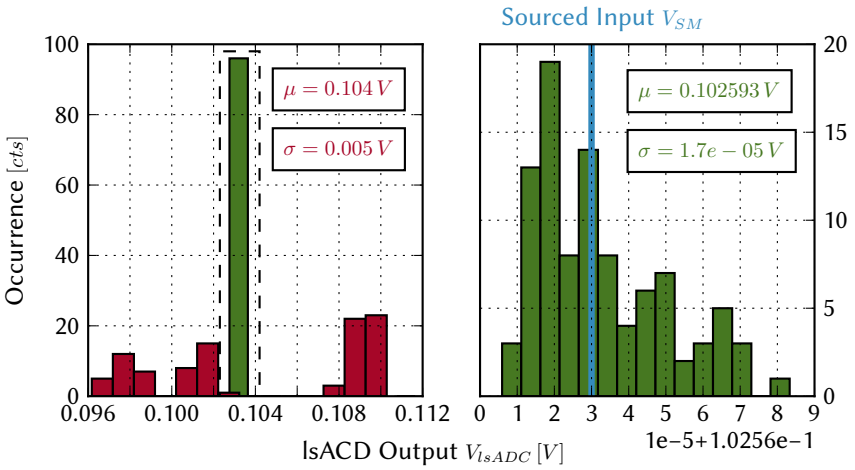

Figure 3.15: Distributions of converted lsADC output voltages at sourced input of $V_{\mathrm{SM}} = 102.59\,\mathrm{mV}$. Red: Ideally translated data with offset $V_{0,\mathrm{art}}$ and LSB extracted from the data sheet [Ins16]. Green: Data corrected with calibration offset $V_{0,\mathrm{off}}$ and gain G_{off}. Blue: True input voltage.

an order of $10^{-5}\,\mathrm{V}$. The difference in the spread can also be seen by comparing the standard deviations of both distributions.

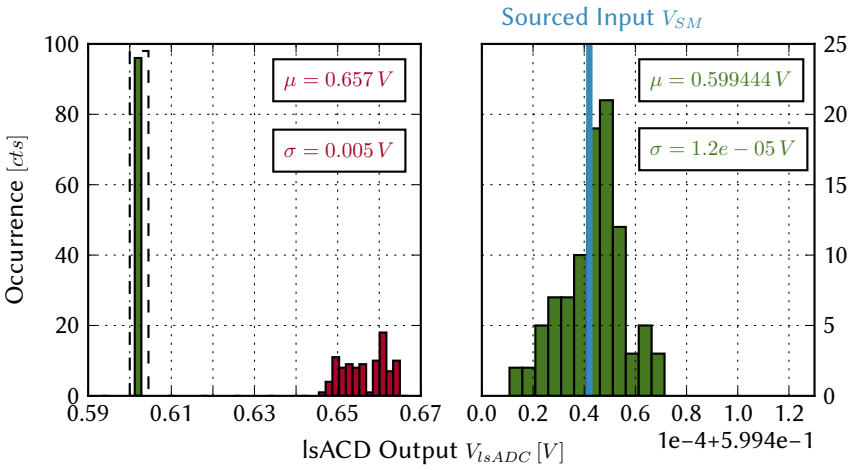

Figure 3.16: Distributions of converted lsADC output voltages at sourced input of $V_{\mathrm{SM}} = 599.44\,\mathrm{mV}$. The shifting of the center of mass of the uncalibrated distribution with respect to the true sourced voltage is clearly noticeable. The calibrated data on the other hand exhibits a considerably higher accuracy.

The calibration does not only improve the consistency of different channels at a given input voltage though. At higher voltages the error resulting from a deviation between the ideal LSB and the inverse of the gain $\frac{1}{G_{\mathrm{off}}}$ becomes noticeable. The correspondingly generated distributions at an input voltage of $V_{\mathrm{SM}} = 599.44\,\mathrm{mV}$ are depicted in Figure 3.16. While the drift of the uncalibrated lsADC output values with respect to the reference voltage V_{SM} is on an order of $10^{-2}\,\mathrm{V}$, the calibrated data maintains its accuracy and scatters almost symmetrically around V_{SM}. The remaining spread and asymmetries in the calibrated data can be referred to the deviations of the linear fit from the true characteristic curve.

As a final test of the quality of the calibration routine, a sawtooth-shaped pulse with the following properties has been generated with a function generator [8]:

1. Frequency: $\nu = 1\,\mathrm{Hz}$

2. Offset: $V_{0,\mathrm{saw}} = 450\,\mathrm{mV}$

[8] *Hewlett Packard 8116A* [Pac93]

3. Peak-to-peak amplitude: $V_{\mathrm{PP,saw}} = 520\,\mathrm{mV}$

4. Duty cycle: 80 %

The low frequency of the input signal is required by the sampling rate of 6 ksps of the lsADC. Next to the lsADC, an oscilloscope[9] has been used to record the signal as a reference measurement. Note that offset and amplitude of the generated signal are already referenced to a termination of 50 Ω and effectively have to be doubled to deduce the actually sourced voltages. The resulting traces can be seen in Figure 3.17.

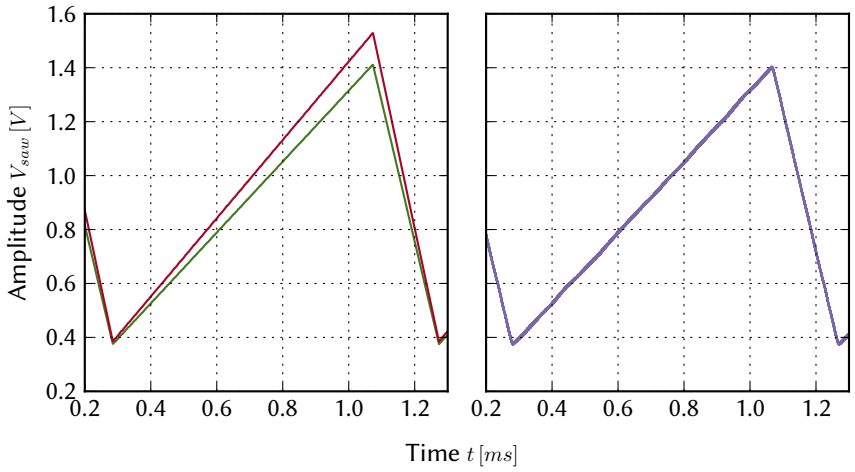

Figure 3.17: lsADC output voltage and trace measured with an oscilloscope for a sawtooth-shaped input signal at 50 Ω termination. Left: Ideally converted lsADC trace (Red) and data corrected with calibration values from unterminated and terminated sweep (Green). Right: Oscilloscope output with DC 50 Ω coupling.

A terminated configuration has been chosen for the measurements with the lsADC. The traces on the left side correspond to the same data measured with the lsADC. As before, the data indicated in red has been translated from LSB to V using the theoretical values $V_{0,\mathrm{art}} = 4096\,\mathrm{LSB}$ and $1\,\mathrm{LSB} \approx 4.35\,\mu\mathrm{V}$. Due to the termination an additional factor of 2 has been used for scaling under the assumption of $R_\mathrm{S} = R_\mathrm{T}$. The green trace on the other hand has been corrected with both sets of calibration values from an unterminated and a terminated sweep of the channel. On the right side, the output of the oscilloscope is displayed. Multiple samples have been used for the displayed oscilloscope trace to receive an average of the signal. This has been done using the trigger functions of the device. It can be observed that the calibration results in a considerable improvement over the ideally converted raw data. Gain errors at high input voltages are eliminated and the offset is also matched correctly. In comparison to the oscilloscope, the lsADC certainly offers a higher precision due to its 20 bit resolution[10] but both traces match well by visual judgement.

Long-Term Stability Investigation

As a final quantification of the performance of the lsADC calibration, long-term measurements have been performed by carrying out daily voltage sweeps for the acquisition of calibration data in an unterminated configuration. This has been done for a period of one month. For lsADC channel 63, the evolution of the

[9] *LeCroy WaveRunner 44Xi* [LeC08]
[10] The oscilloscope offers a vertical resolution of 8 bit [LeC08].

calibration parameters $V_{0,\text{off}}$ and G_{off} has been tracked. The best-fit parameters of each calibration sweep have been converted from $\frac{\text{LSB}}{\text{V}}$ for the gain factor and LSB for the offset to arbitrary units and V, respectively.

The drift of the offset calibration value $V_{0,\text{off}}$ over a period of 37 days is shown in Figure 3.18. The errors of each measured point correspond to the errors obtained from the diagonal elements of the covariance matrix provided by the least squares fit routine.

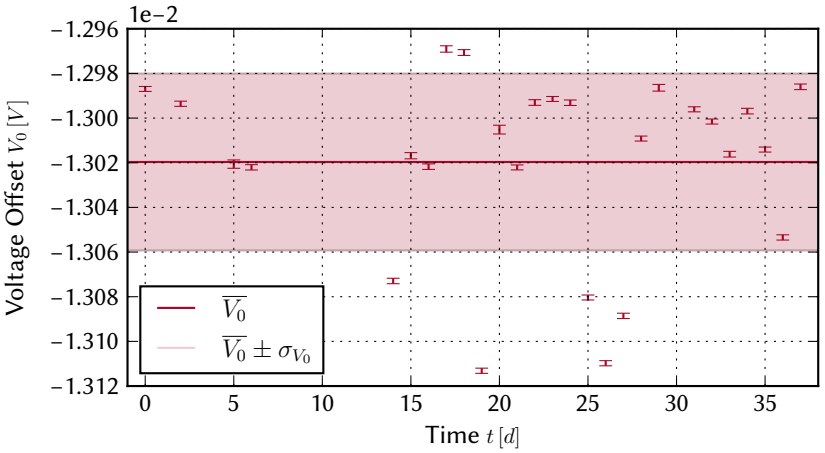

Figure 3.18: Best-fit offset $V_{0,\text{off}}$ of an unterminated lsADC calibration as a function of time. The mean offset $\overline{V_0}$ has been deduced from all displayed values and is framed by the $1\,\sigma$ limits corresponding to the standard deviation of all values.

The mean as well as the limits received by variation according to the standard deviation of all values have been included in order to quantify the spread of the offset values. It can be seen that the error of an individual measured point is considerably smaller than the overall spread. The scattering of the fit values around the mean does not seem to exhibit a correlation with the time t. In this context, one can say that the values are randomly distributed.

The same approach has been applied to the gain parameters G_{off} with the resulting best-fit values shown in Figure 3.19. As for the offset, the gain values scatter in

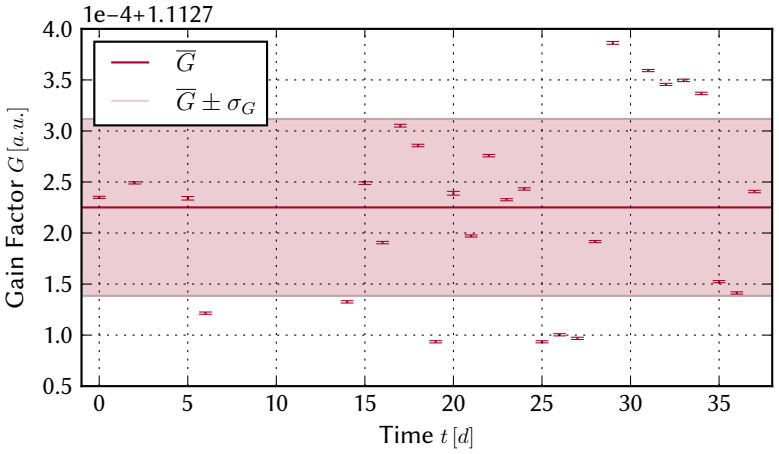

Figure 3.19: Best-fit gain G_{off} of an unterminated lsADC calibration as a function of time. The mean gain $\overline{G}$ has been deduced from all displayed values and is framed by the $1\,\sigma$ limits corresponding to the standard deviation of all values.

a considerably larger range than the individual errors inherent to each data point. With the exception of a set of five outliers in the upper right corner and a set of three consecutively low gain values at $t = 25\,\text{d}$ no systematic trend can be recognized

in the scattering.

The order of the polynomial fit used to model the characteristic curves of the channels does not need to be increased. This can be concluded from the large spread of the offset and gain values over time compared to the errors of the individual fit values. In fact, long-term drifts of gain and offset are the main source of error that leads to a loss of accuracy. Temperature variations might be a reason for the observed scattering. The ANANAS prototype board is operated in a testing room adjacent to the climate controlled room containing the wafer modules. Due to the necessary cooling of the system the door between both rooms is in general left open, leading to a relatively stable temperature of approximately 19 °C at the prototype board. On hot days, however, the cooling system cannot completely compensate for the high temperatures outside the wafer room, leading to temperature variations. These can be enhanced by obstacles hindering the air flow between the wafer room and the testing room containing the ANANAS prototype, such as a half opened door for example.

The temperature dependency of the calibration results has been investigated by tracking the temperature in the testing room with wafer module 17. Each wafer module measures the temperature of the intake air. The web-based visualization tool *Grafana* [Lab18] has been used to extract the testing room temperature over time. An error of approximately 1 °C is estimated for the room temperature.

The distribution of gain and offset best-fit values has been examined again with the room temperature as an additional parameter. In Figure 3.20, the correlation between $V_{0,\text{off}}$ and G_{off} is displayed with the room temperature T as a third dimension in parameter space. One can recognize a trend of larger results for the fit parameters

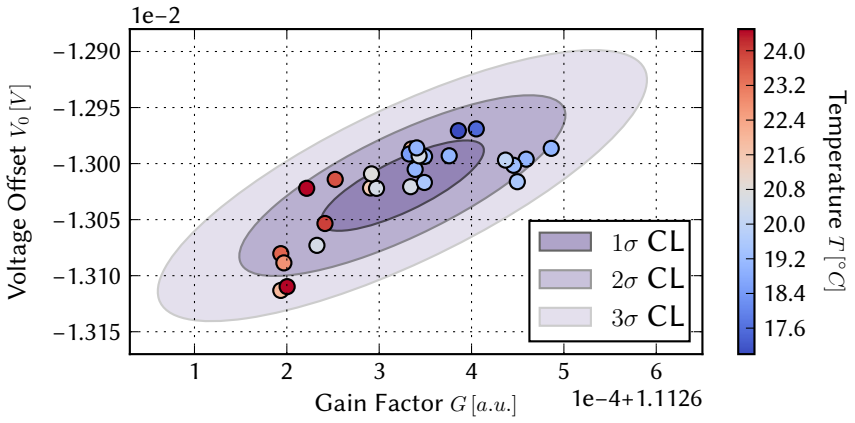

Figure 3.20: Scatter plot of best-fit voltage $V_{0,\text{off}}$ and gain factor G_{off}. The temperature during the corresponding sweep has been color-coded. $V_{0,\text{off}}$ and G_{off} exhibit a strong correlation which seems to be related to temperature variations. 1, 2 and 3 σ confidence limits have been drawn to estimate the set of calibration values to be expected over a long period of time.

occurring at lower temperatures, though this relation does not seem to be perfectly linear. The temperature gradient roughly points from the lower left to the upper right of the plot. Since the temperature dependency of electronic units is in general not linear[11] it is not possible to make quantitative statements on the relationship between gain and offset drifts and the temperature from Figure 3.20 alone. Qualitatively however, it can be stated that the temperature might influence the measurements and evoke the observed correlation between offset and gain.

[11] For example the conductivity is in an exponential relationship with the temperature.

In order to quantify the impact of long-term drifts on a single measurement carried out with the lsADC, the worst-case deviation of an erroneous readout from an ideal characteristic curve due to gain and offset variations has been estimated. Let V_{lsADC} be the measured lsADC output value at a specific gain value G and offset V_0 as a function of the input voltage V_{SM}:

$$V_{\mathrm{lsADC}} = G \cdot V_{\mathrm{SM}} + V_0. \tag{3.18}$$

Another measurement V'_{lsADC} that is carried out under different conditions, for example after a few weeks or at several °C temperature difference, now varies by one standard deviation of the spread in gain and offset depicted in Figure 3.19 and 3.18:

$$V'_{\mathrm{lsADC}} = (G + \sigma_G) \cdot V_{\mathrm{SM}} + (V_0 + \sigma_{V_0})\,. \tag{3.19}$$

The difference $D = V'_{\mathrm{lsADC}} - V_{\mathrm{lsADC}}$ can then be interpreted as the maximum error to be expected when using the same calibration values that have been used in a measurement carried out one month ago. Under application of equations (3.18) and (3.19) one can find:

$$D = V'_{\mathrm{lsADC}} - V_{\mathrm{lsADC}} = \sigma_G \cdot V_{\mathrm{SM}} + \sigma_{V_0}. \tag{3.20}$$

A visual representation of the considerations that have gone into the deduction of equation (3.20) is displayed in Figure 3.21. Here, a hypothetical ideal characteristic

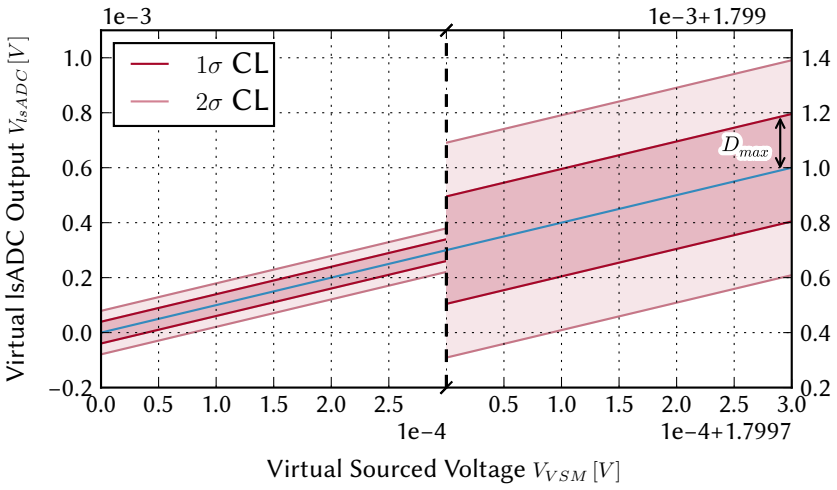

Figure 3.21: Comparison of a characteristic curve with maximum deviation in gain and offset (Red) with an ideal curve with slope 1 and offset 0 V (Blue) estimated over the course of one month. Left: Minimum input voltage. Right: Maximum input voltage. For clarity, the range of input and output voltages on the left and the right side of the plot have been cut as the errors are not visible when displaying the whole trace.

curve of an ADC translating a virtual sourced voltage V_{VSM} to a virtual output value V_{lsADC} has been considered. The theoretical curve has zero offset and a gain factor of one. Its output is compared to a curve that differs from it by one standard deviation in the gain and offset values. One can see that for the observed errors the largest deviations clearly occur at the maximum input voltage of 1.8 V. Equivalent ranges have been chosen for x- and y-coordinates on the left and the right side of the plot. This leads to the conclusion that the impact of the gain error dominates the measurement since the deviations due to the offset error at small sourced values are comparably small. By reading off the maximum difference D_{max} between the dark red curve and the blue ideal one at $V_{\mathrm{SM}} = 1.8\,\mathrm{V}$ one finds:

$$D_{\mathrm{max}} \approx 0.2\,\mathrm{mV}. \tag{3.21}$$

This corresponds to a worst-case deviation of

$$\frac{0.2\,\mathrm{mV}}{1.8\,\mathrm{V}} \approx 0.011\,\%. \tag{3.22}$$

The difference $D_{\max} \approx 0.2\,\mathrm{mV}$ can be converted into a loss of precision in LSB with the lsADC $1\,\mathrm{LSB} \approx 4.35\,\mu\mathrm{V}$:

$$D_{\max,\mathrm{LSB}} = \frac{D_{\max}}{1\,\mathrm{LSB}} \approx 45\,\mathrm{LSB}. \tag{3.23}$$

The combined error σ_{tot} from systematic deviation $D_{\max,\mathrm{LSB}}$ and the statistical uncertainty of $\sigma_{\mathrm{stat}} \approx 24\,\mathrm{LSB}$ for a single measurement with the lsADC is then:

$$\sigma_{\mathrm{tot}} = \sqrt{D^2_{\max,\mathrm{LSB}} + \sigma^2_{\mathrm{stat}}} = 51\,\mathrm{LSB}. \tag{3.24}$$

Finally, the number X of bits lost in resolution can be obtained via:

$$X = \log_2\left(\sigma_{\mathrm{tot}}\right) \approx 5.7\,\mathrm{bit}. \tag{3.25}$$

This seems to be a lot in comparison to the total resolution of 20 bit the lsADC offers. However these deviations occur only at very large input voltages and should be considerably smaller in an actual experiment since the membrane voltages of the analog neurons usually do not reach such large input values. Keep in mind that in addition the statistical error can be scaled down significantly by averaging over multiple measurements. Even though the systematic error seems to dominate the error.

3.3 hsADC Calibration

In this section, the hsADC calibration routine will be explained. As before, the hsADC will first be characterized followed up by a step-by-step description of the procedure to acquire calibration data. Emphasis will be placed on the correction of the common mode influence. Further, the transformation from the hsADC-internal coordinate system, referenced to the shifted ground voltage, back into the global coordinate system of the ANANAS board, relating to its and HICANN ground, will be addressed. The quality of the calibration will be judged in the background of comparable measurements with an oscilloscope and long-term stability.

3.3.1 hsADC Characteristics

Each of the 16 input channels of one of the three *AFE5851* assembled on the ANANAS board consists of a *Variable Gain Amplifier* (VGA) followed by an ADC that is shared between two channels respectively [Ins10]. Due to the VGA the LSB of the hsADC depends not only on the input range and bit size of the ADC, but also on the gain factor being applied in the amplifier stage as well as the input range of the VGA. The data sheet reports the VGA input range to $V_{\mathrm{VGA,in}} = V_{\mathrm{CM}} \pm 500\,\mathrm{mV}$ around the common

mode reference voltage V_{CM}. Its output range swing is $V_{\mathrm{VGA,out}} = 2\,\mathrm{V_{PP}}$, driving the 12 bit internal ADC. Throughout this thesis, an implicit amplification factor of 2 from the VGA will be assumed, leading to an effective FSR of $V_{\mathrm{ADC,FSR}} = 2\,\mathrm{V_{PP}}$. One has to keep in mind that every calibration routine carried out with a specific configuration of the VGA does only apply to these settings. Every change of the hsADC-internal amplification requires a new calibration of the board or the use of calibration data gathered with these specific settings.

Under these preconditions, the LSB of the hsADC is:

$$1\,\mathrm{LSB} = \frac{V_{\mathrm{ADC,FSR}}}{2^{12} - 1} \approx 488\,\mu\mathrm{V}. \tag{3.26}$$

Additionally, the user has the option to choose between an AC- or DC-coupled input. DC-coupling has been chosen for the calibration routine.

Due to the differential measuring topology, the output data from the hsADC is returned in a signed format. Hence, an output of 0 LSB corresponds to an input voltage equal to the common mode voltage. Throughout this thesis the raw data has been inverted such that an increasing input voltage also results in an increasing output value. Thus, a comparison of future calibration sweeps with those executed in the framework of this thesis is possible when ensuring that the gain factor has been adjusted correctly and the sign of the output values matches.

The statistical error of a single measurement with the hsADC has been estimated with a 50 Ω terminated grounded-input measurement. The analog switches have been closed while shorting the pin and shielding of the coaxial cable of the analog test adapter driving the input voltage. $N = 2^{19} \approx 524\,000$ samples have been recorded for a densely sampled distribution. The hsADC allows such a large number due to its enhanced sampling rate of approximately 10^4 compared to the lsADC. An excerpt of the resulting output trace of channel 3 of TG0 is shown in Figure 3.22.

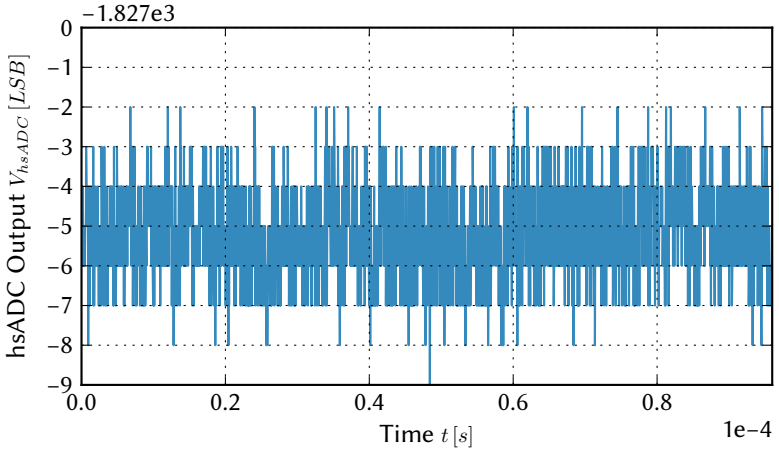

Figure 3.22: hsADC output trace of channel 3 of TG0 at an ideally grounded 50 Ω terminated input as a function of time. The jitter of the trace is limited to a range of 8 LSB for this small excerpt of data. With the exception of possible power noise the spread seems to be uniformly distributed around a mean value of approximately −1832 LSB.

For the complete set of measured points this results in the distribution displayed in Figure 3.23.

The intrinsic noise of the hsADC is acceptable with a standard deviation of 1.1 LSB. This means that measurements are afflicted with a statistical error that is of the

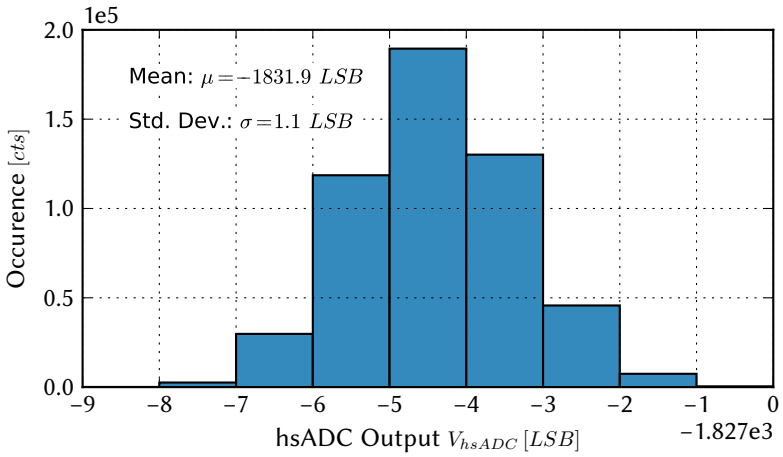

Figure 3.23: Distribution of TG0 channel 3 output at ideal ground. The statistical error corresponds to approximately 1.1 LSB.

order of the total resolution of the device.

Additional noise has, however, been observed when applying a constant input voltage to the hsADC inputs with the source meter. For the identical chip and channel, an input of 0 V has been applied with the source meter and recorded with the same number of samples. The analog switches have been closed again. The resulting trace can be seen in Figure 3.24.

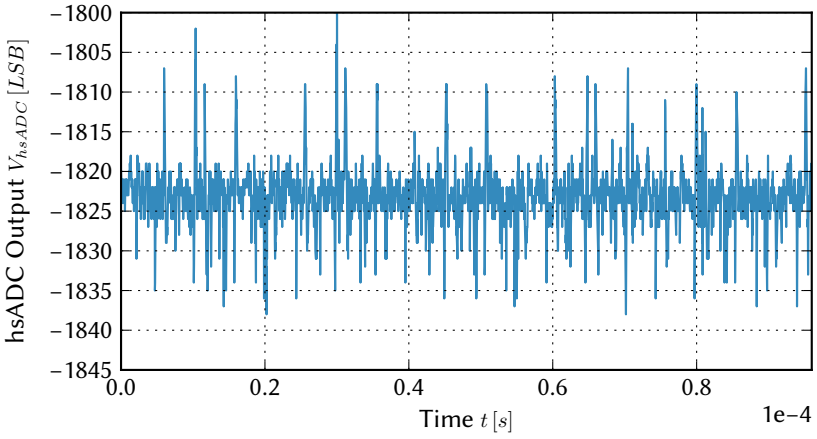

Figure 3.24: hsADC output trace of channel 3 of TG0 at a constant SM input voltage of 0 V as a function of time. The spread of the output values has increased considerably in comparison to Figure 3.22. Periodic spikes in the trace suggest a coupling of additional frequency components in on the measured node.

This additional noise can be referred to the source meter as there has not been a different actively driving input on one of the remaining other channels. The corresponding distribution of all 2^{19} measured points can be seen in Figure 3.25.

With a standard deviation of 3.8 LSB the spread statistical error is approximately four times as large as for an ideal voltage source. Due to the nearly symmetric shape and the distinct peak of the distribution in Figure 3.25, however, it should be possible to compensate for this error by averaging over a larger number of samples. In order to reduce the statistical error in a measurement with the source meter one would require to average over

$$N = \left(\frac{3.8\,\mathrm{LSB}}{1.1\,\mathrm{LSB}}\right)^2 \approx 12 \tag{3.27}$$

samples. Averaging over 100 samples per voltage step is manageable with the high hsADC sampling rate of 31.25 MHz, certainly cancelling out the source meter noise.

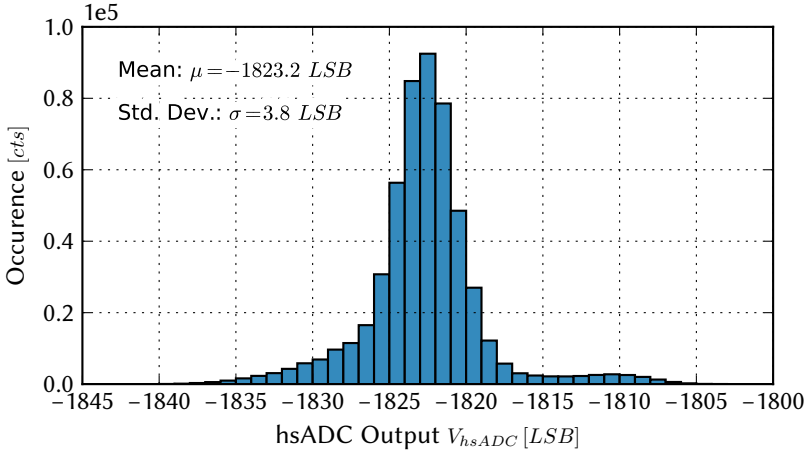

Figure 3.25: Distribution of TG0 channel 3 output at a constant SM input voltage of 0 V. The statistical error corresponds to approximately 3.8 LSB. The distribution exhibits a slight asymmetry with additional weight towards larger output values.

The slight displacement of the mean compared to the ideally grounded measurement might have arisen from a coupling of the sourced voltage on the common mode or an offset from the source meter. However, this issue has not been investigated further.

3.3.2 Calibration Routine

The hsADC can only be used terminated thus there is only one possible configuration to be considered when aiming for a full calibration of all 48 channels. Operating the hsADCs on a shifted ground eliminates the generality of calibration data which would be acquired by the same procedure as for the lsADC. The reason for this is that other than the global ground of the ANANAS, the shifted ground is created by a DAC[12] [Inc15] and therefore variable. This means that offset values obtained in a linear fit to the hsADC output data given a range of input voltages of the source meter are only applicable if the shifted ground voltage is still the same. Thus, it is desirable to find calibration values which are independent of input voltages referenced to global ANANAS ground. They should only apply to the hsADC-internal translation of input to output values referenced to the common mode voltage. In a rough distinction, the routine for the acquisition of calibration data for a single channel can be divided into five steps, which will be explained in the following.

Step 1: Baseline Recording

The first step is to determine the idle state of each channel for a given common mode setup. Since the shifted ground supply voltage is generated with a DAC with user-definable output value [Ilm17], the common mode voltage V_{CM} is also only fixed for a specific setup of the DAC. This is valid with the exception of temperature or time dependent drifts. The baseline denotes the output of a specific channel with open analog switches, which is effectively the idle state of the common mode for an input terminated to global ground with 50 Ω. A measurement of all 48 baselines with 112 samples per channel can be seen in Figure 3.26.

[12] digital-to-analog converter

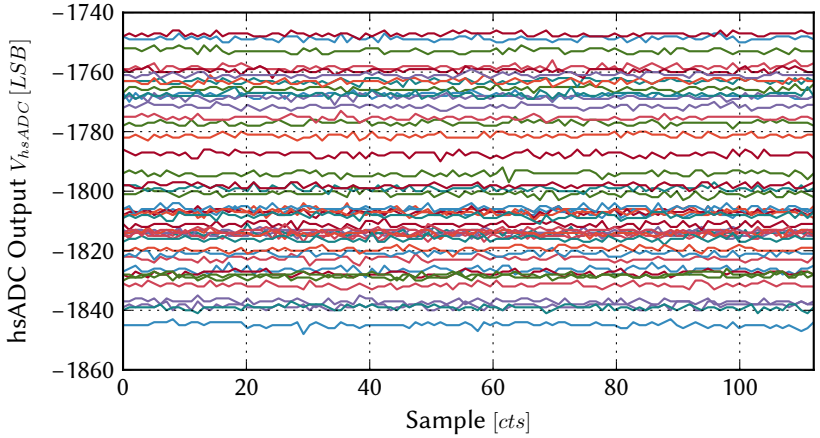

Figure 3.26: Baseline measurement for the determination of the terminated CM of each of the 48 hsADC channels. The discrepancy between the channels can already be seen as all channels are supplied with the same CM reference voltage and are all tied to ground due to the open analog switches.

With a difference of approximately 100 LSB between the maximum and the minimum average baseline value, the variation between the different channels becomes clear. The deviations most likely arise from the variations of the internal 5 kΩ biasing resistor. They, however, can also imply gain as well as offset errors from the VGAs and ADCs inside the hsADC. This is because the measurement has been performed at the lower end of the input range of the VGA.

Effectively, one does only need the average baseline of the six channels that are going to be used for tracking the common mode. This is due to the fact that the measurement will be used as a reference on how V_{CM} changes over the course of the calibration voltage sweep due to the influence of the input voltage[13].

Step 2: Voltage Sweep

The second task is the application of a voltage sweep with the source meter which is nearly the same as for the lsADC. Because of the slight shifting of the input range $V_{\mathrm{hsADC,in}}$ to negative voltages[14] it is necessary to modify the range of the voltage source. The complete characteristic curve of the hsADC channels could be sampled with the shifted ground voltage calculated in equation (1.6) and the VGA gain of 2 using a range of $V_{\mathrm{SM}} = -0.2\,\mathrm{V}$ to 1.8 V. In general, it is to keep in mind which gain and shifted ground settings have been used in order to receive an estimate for the sweeping range that has to be applied. If the range is chosen appropriately, the output should go in saturation for a small part of the upper and the lower limits of the sourced range. In this case, a large part of the measured data points can be used for the fit routine yielding a lower error of the fit parameters. For the sweeps presented in the following, a step size of 2 mV has been chosen, leading to a total of 1000 voltage steps for each channel. At each step, 112 samples per channel have been read back.

Regarding the execution of the voltage sweep, parallel readout of the 48 channels at each voltage step is not possible. The reason for this is that only one analog switch can be activated at a time in order to prevent the measurement from being falsified by the

[13] cf. section 2.2
[14] cf. equation (1.6)

shorted inputs on the analog test header. Otherwise, the sourced voltage is terminated with additional parallel connected 50 Ω resistors from neighboring channels. In the calibration routine, this issue is addressed by first sourcing an input voltage with the source meter and then closing the switch and reading out data belonging to a single channel of the hsADCs. Compared to the terminated measurement with the lsADC, this approach leads to an increased runtime of approximately 17 min since the voltage step resolution is greater by a factor of 10^2.

While the voltage sweep is applied, three dedicated channels keep track of the common mode variations. One channel per hsADC is chosen because the phase shift between two channels of the same chip but different trigger groups can be neglected. This is due to the large number of samples used for averaging. The CM-tracking with a specific channel is done by leaving the corresponding analog switches open and requesting data from it while the sourced voltage is applied to a different channel of the same chip. The result is a measurement of the indirect effect of the voltage sweep on the idle state of the common mode. An example on how the traces for an actively driven and a neighboring CM-tracking channel look like is given in Figure 3.27.

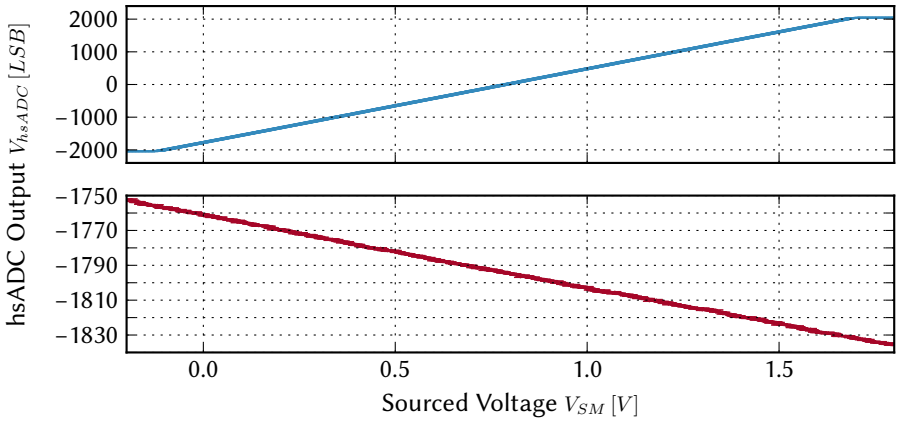

Figure 3.27: hsADC output of two channels of TG3 Top: Actively driven channel 2. Bottom: Neighboring channel 7, tracking the CM change over the course of the sweep. While the sweep is performed, the decreasing output of the neighboring channel corresponds to an increase of the CM.

On the neighboring channel trace, a maximum variation of approximately 80 LSB can be observed. The decrease of the output is evoked solely by a change of the common mode reference voltage. The output is obtained by a differential measurement of a grounded input against the common mode. Thus, one can conclude that the common mode increases over the course of the calibration sweep. It is clear that this also falsifies the measurement of the actively driven input as every channel of the same hsADC is measuring its input differentially against the same reference node. For the acquisition of calibration data, this circumstance has to be taken into account.

Step 3: common mode Correction

The tracked common mode trace of the neighboring channel is referenced to global ground thus carries an unwanted offset. It is favorable to investigate the output values of the hsADC in its own coordinate system, meaning that the values are referenced to the common mode voltage V_{CM}. In order to extract only the deviations of the common mode in the coordinate system of the hsADC with respect to its idle state, the mean value of the channel baseline recorded in the beginning has to be subtracted from the trace. The resulting output is displayed in Figure 3.28.

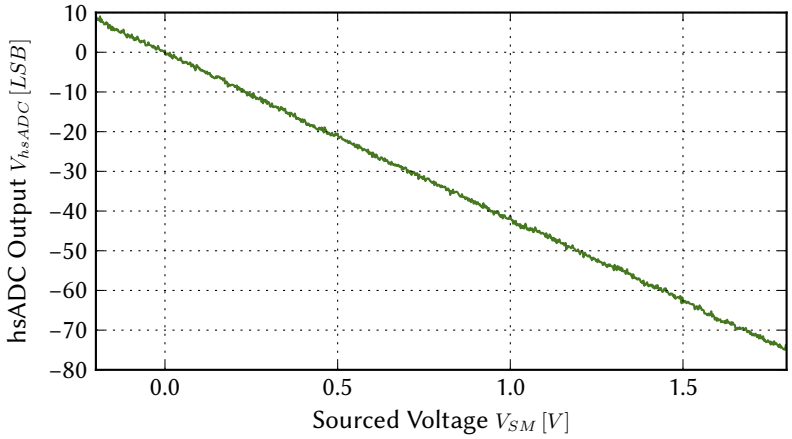

Figure 3.28: CM variation relative to an idle state at ideal ground recorded with channel 7 of TG3. The deviations occur over the course of a voltage sweep of adjacent channel 2 on the same chip.

The relative error between different channels seen in the baseline measurement in Figure 3.26 has also been prevented from falsifying the upcoming correction with this approach. According to equation (2.16), a factor of $\frac{5100}{5000}$ has to be considered when subtracting the common mode shift recorded on a neighboring channel from the trace of the driven channel. For the acquisition of calibration data, the common mode trace displayed in Figure 3.28 is fitted with a linear function according to equation (2.3) in order to eliminate the noise on the trace. Then, by multiplication of the fit result with $\frac{5100}{5000}$ and subtraction of the result from the upper trace in Figure 3.27 one receives the common mode corrected trace in Figure 3.29.

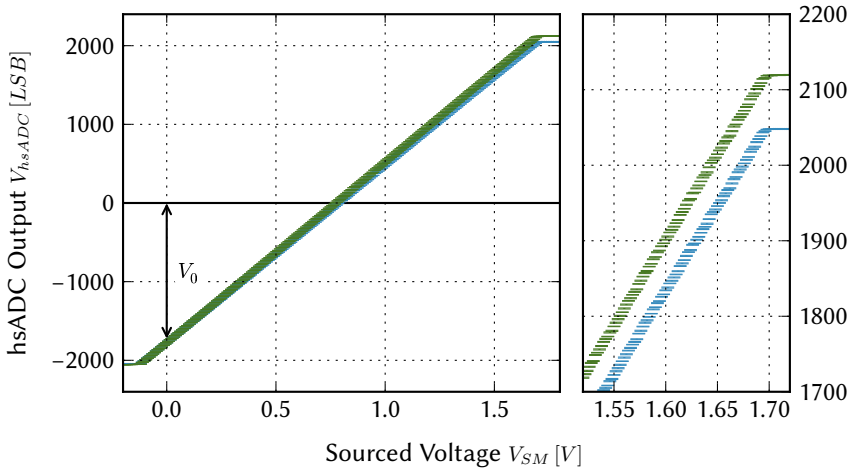

Figure 3.29: CM correction, comparison of pre- and post-corrected data of TG3 channel 2 with full voltage sweeping range displayed on the left side and small excerpt close to the upper limit shown on the right. Blue: Trace without correction. Green: Same trace with CM influence eliminated. V_0 denotes the offset observed at a sourced voltage of 0 V obtained in a linear fit.

Over the expanded excerpt of the traces at the upper end of the sourced voltage range V_{SM} one can see that the corrected trace exhibits larger output values compared to the uncorrected one. This is understandable since an increase of the common mode reference voltage has been observed in Figure 3.27, ultimately leading to a constant underestimation of the actually sourced voltage. At the lower end the effect is not equally strong since the sourced voltage has only covered a small range of negative voltages. The nonconsideration of the common mode would ultimately have lead to an underestimation of the gain factor of the hsADC with regard to the trace in Figure 3.28.

It should be made clear that an additional error has been neglected in the correction

introduced above. In the first acquisition of calibration data, the assumption is made that the error arising from the subtraction of an uncalibrated voltage trace from a neighboring channel is small compared to the absolute error introduced by the hsADC crosstalk. It becomes clear that the maximum difference $D_{\max} = 80\,\mathrm{LSB}$ of the common mode correction corresponds to $\frac{80\,\mathrm{LSB}}{4096\,\mathrm{LSB}} \approx 2.0\,\%$ of the FSR with the traces observed in Figure 3.28 and 3.29.

The data sheet [Ins10] reports a gain matching across channels of $\pm 0.1\,\mathrm{dB}$. For the ratio of two outputs V_1 and V_2 of two arbitrary channels 1 and 2 this leads to

$$\frac{V_1}{V_2} = 10^{0.01/20} \approx 1.012. \tag{3.28}$$

which corresponds to an error of $\frac{V_1}{V_2} - 1 = 0.012 \mathrel{\widehat{=}} 1.2\,\%$. Thus, for an approximate gain of $G = 2300\,\frac{\mathrm{LSB}}{\mathrm{V}}$, which corresponds to the average values obtained in the calibration, the error is

$$\Delta G = \left(\frac{V_1}{V_2} - 1\right) \cdot G \approx 28\,\frac{\mathrm{LSB}}{\mathrm{V}}. \tag{3.29}$$

Together with the calculated value of $1\,\mathrm{LSB} \approx 488\,\mu\mathrm{V}$ in equation (3.26) the introduced error can be estimated:

$$\frac{1\mathrm{LSB} \cdot D_{\max} \cdot \Delta G}{N} \approx 0.02\,\%, \tag{3.30}$$

where $N = 2^{12}$.

Thus, the error due to the negligence of gain variations between the two channels should be small compared to the total error arising from the variation of the common mode. However, for a full calibration of the hsADC, the CM-tracking channel still has to be calibrated. This is done following the same approach from above after the channel has been used to obtain calibration data for the other 15 channels of the same hsADC. For this additional calibration, the common mode shifts can be recorded with one of the already calibrated channels.

Note, that an additional correction has to be performed in order to receive an output which is characterized by the hsADC alone. This correction applies to the imperfect voltage divider of the source meter source impedance adapter $R_{\mathrm{S,ad}} = (49.85 \pm 0.05)\,\Omega$ and the individual terminating resistor value R_{T}, which has been determined in the terminated measurements with the lsADC in section 3.2.2. The small deviations of the resistors from an ideal value of $50\,\Omega$ falsify the actual input voltage that is applied to the inputs of the hsADC. Thus, the input voltage $V_{\mathrm{hsADC,IN}}$ is not exactly half of the sourced value reported by the source meter V_{SM} but rather

$$V_{\mathrm{hsADC,IN}} = \frac{R_{\mathrm{T}}}{R_{\mathrm{S,ad}} + R_{\mathrm{T}}} \cdot V_{\mathrm{SM}}. \tag{3.31}$$

An example of the impact of this effect can be estimated by using the mean value $R_{\mathrm{T}} = (49.43 \pm 0.08)\,\Omega$ from Figure 3.13 as the terminating resistor. Then, the following equation holds true:

$$V_{\mathrm{hsADC,IN}} = \frac{49.43\,\Omega}{49.85\,\Omega + 49.43\,\Omega} \cdot V_{\mathrm{SM}} \approx 0.4979 \cdot V_{\mathrm{SM}}. \tag{3.32}$$

The set of measured input voltages V_{SM} should now be corrected with the factor 0.4979 to obtain the actual sourced voltage. Since the hsADC can only be used terminated, however, it is also applicable to introduce an additional factor of two to the shifted input values. This maintains the information of the terminated measurement topology such that a future application of the calibration data immediately corrects for it. The input voltages from the source meter V_{SM} then have to be scaled with the correction factor $Corr = 2 \cdot 0.4979$ to receive the set of input values V'_{SM} which are corrected for the errors in R_{T} and $R_{\mathrm{S,ad}}$:

$$V'_{\mathrm{SM}} = Corr \cdot V_{\mathrm{SM}} \approx 0.9958 \cdot V_{\mathrm{SM}}. \tag{3.33}$$

This corresponds to a correction of

$$1 - 0.9958 = 0.0042 \mathrel{\widehat{=}} 0.42\,\%. \tag{3.34}$$

The error of the correction factor is

$$\begin{aligned} \Delta Corr &= 2 \cdot \sqrt{\left(\frac{\partial Corr}{\partial R_{\mathrm{T}}}\right)^2 + \left(\frac{\partial Corr}{\partial R_{\mathrm{S,ad}}}\right)^2} \\ &= \frac{2}{\left(R_{\mathrm{S,ad}} + R_{\mathrm{T}}\right)^2} \cdot \sqrt{\left(R_{\mathrm{S,ad}} \cdot \Delta R_{\mathrm{T}}\right)^2 + \left(R_{\mathrm{T}} \cdot \Delta R_{\mathrm{S,ad}}\right)^2} \\ &\approx 0.0010 \end{aligned} \tag{3.35}$$

This corresponds to a relative error of:

$$\frac{\Delta Corr}{Corr} = \frac{0.0010}{0.0042} \approx 0.238 \mathrel{\widehat{=}} 23.8\,\%. \tag{3.36}$$

Thus, the error is not negligible. Since the error of the termination dominates the uncertainty, the individual terminating resistors of each channel should be considered for the input voltage correction. After this correction it is possible to model the characteristic curve of the hsADC inputs with the actually sourced reference values.

Step 4: Fitting

It is then again possible to perform a linear fit on the corrected data according to equation (2.3) to obtain offset and gain values V_0 and G. Note, however, that the offset value V_0 does *not* allow for any statements on the *hsADC-internal* offset because it has been obtained with reference to the global ground of the ANANAS. Hence, the acquisition of valid offset calibration data will be addressed in the upcoming step. Yet, the gain value G is independent of the coordinate system on which the data is referenced on, thus can be directly taken from the linear fit. The trace displayed in Figure 3.30 has been shifted into the coordinate system of the hsADC by a coordinate transformation along the x-axis. By determining the intersection $V_{\mathrm{SM},0}$ of the recorded trace with the x-axis via

$$V_{\mathrm{SM},0} = -\frac{V_0}{G} \tag{3.37}$$

one finds the sourced voltage at which the hsADC channel measures a difference of 0 V to the common mode voltage V_{CM}. This value is then subtracted from the actual values of the source meter, leading to the displayed range V_{VSM}.

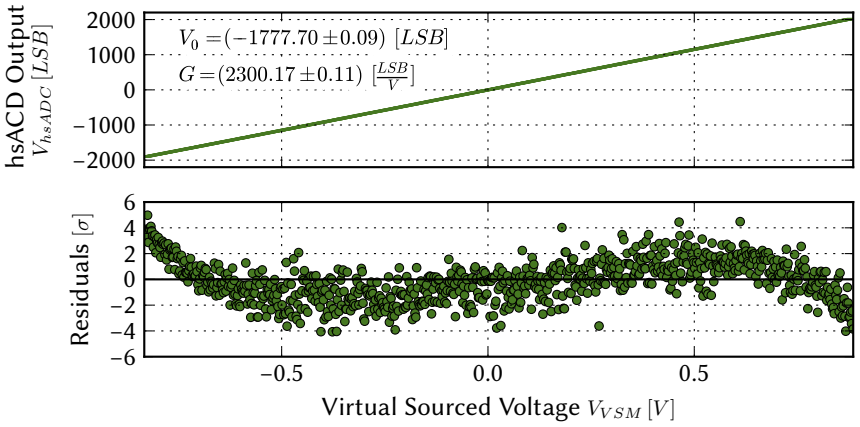

Figure 3.30: CM corrected and transformed hsADC output of TG3 channel 2 in hsADC-internal coordinate system. Top: Output trace with best-fit gain value G. Bottom: Best-fit residuals of the true characteristic curve from the results of the linear least squares fit.

In the lower plot of Figure 3.30, the residuals relating to the linear best-fit can be seen. The shape of the characteristic deviations suggests a fit of higher order[15] as there are clear systematics visible on the boundary areas of the curve with significant deviations larger than $3\,\sigma$ of the error of the mean. Towards the center, the deviations become smaller and lie within the $3\,\sigma$ range, still yielding a point symmetric distribution around $V_{\mathrm{VSM}} = 0\,\mathrm{V}$ though.

A look on the distribution of the residuals in Figure 3.31 enables a first estimate of the systematic error that is to be expected from the linear approximation. With a

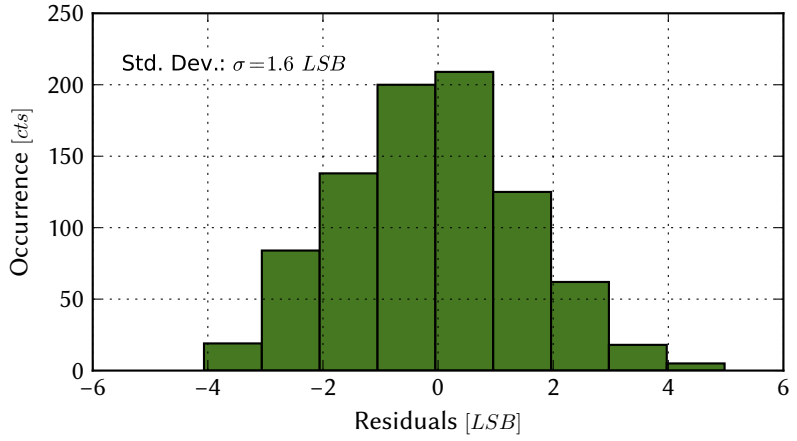

Figure 3.31: Histogram of residuals of TG3 channel 2 hsADC output values from linear least squares fit with polynomial of first order. The spread is nearly symmetrical around zero. The width yields a standard deviation of 1.6 LSB.

standard deviation of $\sigma = 1.6\,\mathrm{LSB}$, an average systematic error of

$$\sigma_{\mathrm{syst}} = 1.6\,\mathrm{LSB} \approx 0.8\,\mathrm{mV} \tag{3.38}$$

is to be expected. However, in order to receive a worst-case estimate, it might again be more reasonable to use the maximum deviation of the linear approximation from the actual characteristic curve as a measure. Hence, the characteristic curve has been fitted with a polynomial of fifth order. The resulting spread of the residuals and the difference to a linear fit can be seen in Figure 3.32.

The spread of the residuals in the upper plot yields a stronger mirror symmetry around zero but the individual deviations of some measured points in the range of 5

[15] Probably third or fifth

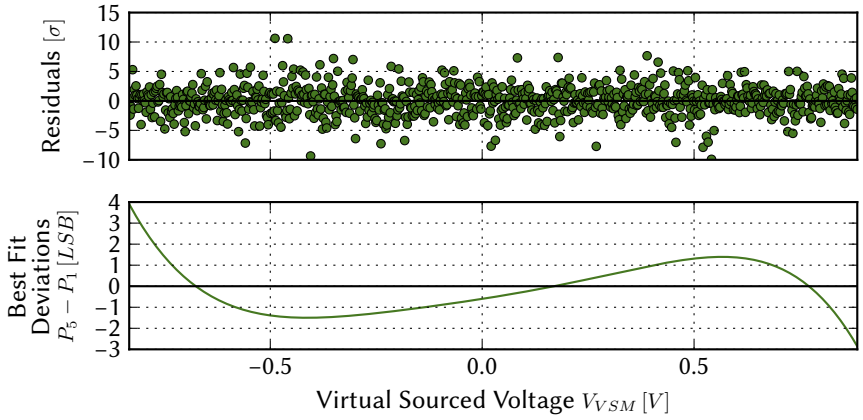

Figure 3.32: Comparison of linear fit with polynomial of fifth order assumed to give a better representation of the characteristic curve of the hsADC. Top: Residuals of polynomial fit of fifth order. Bottom: Difference between fifth order and linear best-fit. The maximum difference is approximately 4 LSB.

to $10\,\sigma$ suggest overfitting. At the boundary areas for high and low V_{VSM}, however, the residuals seem to be randomly and uniformly distributed. This allows to deduce the maximum error from the linear approximation in these areas. The lower plot yields a maximum deviation of approximately 4 LSB. This value will be used as a reference for the upcoming considerations regarding the overall accuracy of the calibration. The necessity of moving to a higher polynomial order in the fit routine again has to be discussed against the background of the long-term stability of the calibration data.

Step 5: Acquisition of hsADC-Internal Offset Values

In the planning phase of the calibration routine for the hsADC, it has initially been assumed that the calibration of data obtained in a measurement with the hsADC would not require an individual offset correction for each channel. The reason for this is that the correction of the common mode influence by subtracting neighboring channel data immediately shifts the output values into the correct coordinate system, referenced to global ANANAS ground. This means that the major offset in the data arising from the differential measurement against the common mode reference voltage is automatically erased. There does, however, remain a small offset in the range of a few LSB which is due to the channel-to-channel variations of the hsADC. This offset will be referenced to as the hsADC-internal offset in the following. An estimated order of the error introduced by the nonconsideration of this offset has already been given in the variations of the different baselines in Figure 3.26, even though that also gain errors could have come into play in this measurement. It is therefore desirable to receive channel-specific offset values $V_{\mathrm{hsADC},0}$ in the coordinate system of the hsADC, thus referenced to the common mode voltage V_{CM}.

It is not possible to measure the absolute offset values $V_{\mathrm{hsADC},0}$ with a common ANANAS board directly due to the lack of knowledge on the true value of the common mode voltage V_{CM}. A workaround for this issue could be achieved by using an ANANAS system with the $50\,\Omega$ input resistors between the analog switch and the hsADC input not assembled[16]. This frontend configuration leads to a floating input of the hsADC channels which are automatically pulled to the common mode voltage V_{CM} via the $5\,\mathrm{k}\Omega$ biasing resistor. Hence, every measurement with the hsADCs on

[16] cf. Figure 1.4

this board reports the internal frontend offsets since both inputs are fixed to the common mode voltage. By reading out 1120 samples for all 48 hsADC channels and averaging over every set of output values, the distribution of offset values $V_{\mathrm{hsADC,0}}$ displayed in Figure 3.33 has been received.

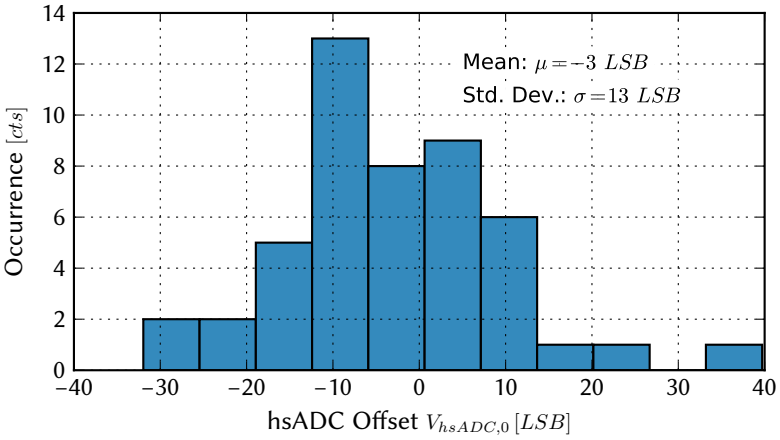

Figure 3.33: Distribution of 48 hsADC-internal offset values $V_{\mathrm{hsADC,0}}$ for an exclusive ANANAS PCB with floating hsADC inputs. The distribution is approximately symmetric around 0 LSB.

The distribution of channel-specific offsets is approximately symmetric around $V_{\mathrm{hsADC,0}} = 0\,\mathrm{LSB}$. Using the theoretical value $1\,\mathrm{LSB} \approx 488\,\mu\mathrm{V}$ a standard deviation of 13 LSB yields a systematic error of roughly 6 mV, if the individual offsets are not taken into account. Keep in mind that the data displayed in Figure 3.33 should be viewed detached from the remaining figures shown in this section as it does *not* refer to the same ANANAS system. It should rather be seen as a motivation of the upcoming procedure.

The symmetry of the distribution of the offset values can be exploited in case the shifted ground dependent offsets along the x-axis $V_{\mathrm{SM,0}}$ yield the same symmetry. In this case, the relative deviation of the individual channel offsets to the mean value can be used to extract the hsADC-internal offset in LSB corresponding to Figure 3.33. The distribution displayed in Figure 3.34 shows the input voltage of the source meter $V_{\mathrm{SM,0}}$ for one of three hsADCs on the ANANAS at which the respective channels return an output value of 0 LSB. It is necessary to distinguish between the different hsADC on the same ANANAS board as they all generate an individual reference voltage V_{CM}. Therefore, the mean $\mu_{V_{\mathrm{SM,0}}}$ of the offset voltages $V_{\mathrm{SM,0}}$ can differ between the three chips even given the same shifted ground voltage.

The following extraction of the offset value has been justified with the approximately symmetric distribution of the voltages $V_{\mathrm{SM,0}}$ around the mean $\mu_{V_{\mathrm{SM,0}}} = 796\,\mathrm{mV}$. Let $V_{\mathrm{SM,i}}$, $\mathrm{i} \in \{1, ..., 48\}$ denote the 48 individual x-axis offsets from the linear fits to the channel-specific data. Then by transformation of equation (3.37) one receives the hsADC-internal offset $V_{\mathrm{hsADC,i}}$ in LSB using the gain factors G_{i} from the linear fits:

$$V_{\mathrm{hsADC,i}} = -V_{\mathrm{SM,i}} \cdot G_{\mathrm{i}}. \tag{3.39}$$

A graphic representation of the offset $V_{\mathrm{hsADC,0}}$ can be seen in Figure 3.35.

The displayed trace has been transformed to the coordinate system of the hsADC. This has been done by shifting the input voltage range V_{SM} by the mean of the x-axis offsets $V_{\mathrm{SM,0}}$ of the hsADC containing the considered channel. Thus, the

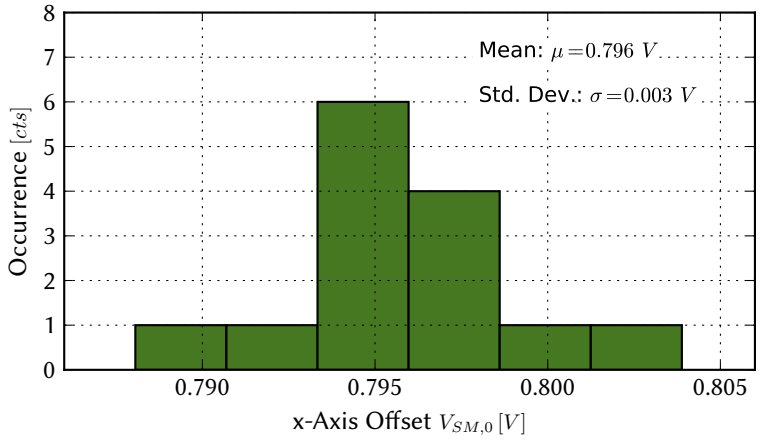

Figure 3.34: Distribution of x-axis offsets $V_{\mathrm{SM},0}$ obtained from linear fits to CM-corrected hsADC data from 16 channels of a single hsADC. Due to the limited amount of channels, the distribution does not reach the sampling density of Figure 3.33. The distribution is approximately symmetric around the mean value.

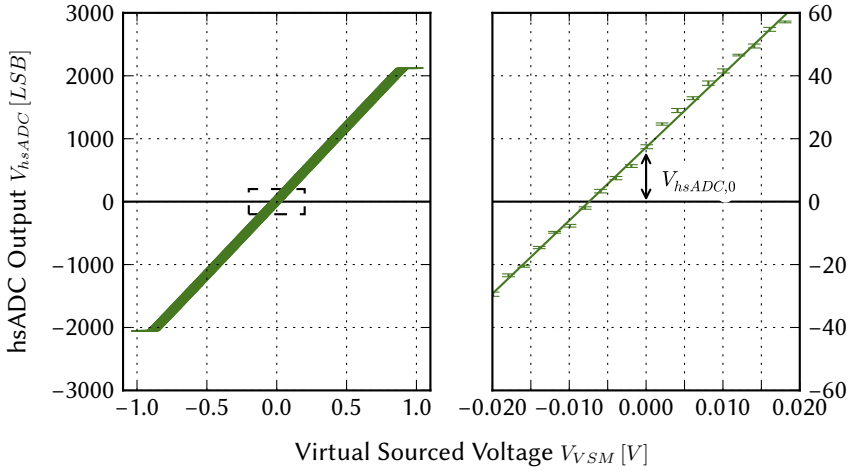

Figure 3.35: Illustration of the hsADC-internal offset $V_{\mathrm{hsADC},0}$ for TG3 channel 2. Left: Complete CM-corrected voltage trace from SM sweep in the coordinate system of the hsADC. Right: Enlarged excerpt of the hsADC output around $V_{\mathrm{VSM}} = 0\,\mathrm{V}$ with linear best-fit. The arrow indicates the channel-specific offset at an input voltage equal to the CM voltage.

remaining offset along the y-coordinate at a common mode referenced input voltage $V_{\mathrm{VSM}} = 0\,\mathrm{V}$ represents the offset in the hsADC-internal coordinate system. Both calibration values, gain and offset, have now been made independent of the shifted ground voltage and are a characteristic solely of the hsADC.

If one aims to use only the information of a single channel in an actual experiment, the measured trace can be referenced to global ground by adding the offset $V_{\mathrm{SM},0}$ to the calibrated output values. However, the intended use of the calibration data obtained with this procedure is to use the correction with the trace of a neighboring channel. This immediately shifts the data to the coordinate system referenced to global ground and also corrects for the common mode variations.

3.3.3 Calibration Quality and Long-Term Stability

In a similar manner to the investigation of the lsADC, the calibration of the hsADC will be examined with regard to its precision and performance over a long time. This includes the analysis of the spread of the individual channels before and after the calibration, a test using a function generator and an oscilloscope and the evaluation of time- and temperature-dependent gain and offset drifts.

Comparison of Pre- and Post-Calibration Data

The baseline measurement in the first step of the acquisition of calibration data has been used to investigate the instant impact of the calibration on the spread of the individual channels at equal input voltages. Every channel should approximately, at least within the precision of the statistical error of the calibration, return the same output value with the baselines being recorded at grounded input.

In the following considerations, the offset error of the individual channels is initially neglected as it has been assumed that all offset variations could be eliminated with the correction over the CM-tracking channels. Therefore, the mean of the 112 samples of each channel in the baseline measurement has only been divided by the respective gain parameter G obtained from the linear fit. In total six rather than three channels have been used for the tracking of the common mode in this calibration routine which are not provided with calibration data. This results in a total number of 42 channels rather than 45 to be visualized. A distribution to be used for comparison has been achieved by multiplication of the baseline mean values with the theoretical hsADC 1 LSB $\approx 488\,\mu V$. The resulting distributions are displayed in Figure 3.36.

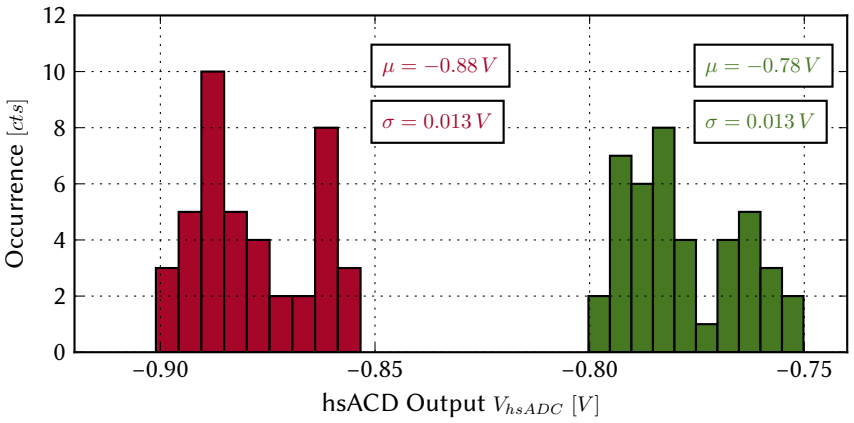

Figure 3.36: Comparison of the baseline spread of 42 hsADC channels at theoretical conversion (Red) and correction with the gain values G obtained from the calibration with a linear fit (Green). The inputs have been pulled to global ground of the ANANAS board for this measurement. A comparable value of the standard deviations for both distributions yields no significant improvement.

Both distributions yield approximately the same standard deviation of 10^{-2} V. Thus, with the exception of a slight shifting of the distributions by approximately 0.1 V, which is due to the adjusted gain value, no significant improvement has been obtained from the correction. This means that the remaining spread has to be referred to the neglected offset correction which has been enhanced by gain errors.

The procedure for the calculation of the hsADC-internal offsets explained in the last step of the calibration routine is able to significantly improve the spread of the calibrated distribution. Let V_{B} be the measured mean baseline value for one of the 42 channels with offset V_{hsADC} and gain G available from the calibration routine. Further the mean value V_{SM} for the x-axis offset has been calculated for a transformation to the global coordinate system. Then, the correction of the mean baseline value has been carried out by application of the calibration data and shifting the result back into the global coordinate system referenced to global ground:

$$V_{\mathrm{hsADC,out}} = \frac{V_{\mathrm{B}} + V_{\mathrm{hsADC}}}{G} + V_{\mathrm{SM}}. \tag{3.40}$$

In order to find comparable data, the ideally converted data set has also been shifted by a theoretically equivalent approach. This has been achieved by adding the approximate common mode voltage V_{CM} to the values with a factor of two due to the voltage divider of source impedance and termination. V_{CM} has been estimated by adding the theoretical shifted ground voltage V_{GS} produced by the DAC with the idle common mode voltage $V_{\mathrm{CM,id}} = 1.6\,\mathrm{V}$ reported by the data sheet [Ins10]. The theoretical shifted ground a voltage has been

$$V_{\mathrm{GS}} = -1.1264\,\mathrm{V} \tag{3.41}$$

resulting in a common mode voltage of

$$V_{\mathrm{CM}} = V_{\mathrm{GS}} + V_{\mathrm{CM,id}} = -1.1264\,\mathrm{V} + 1.6\,\mathrm{V} = 0.4736\,\mathrm{V} \approx 0.47\,\mathrm{V}. \tag{3.42}$$

The distributions depicted in Figure 3.37 have been found with these prerequisites.

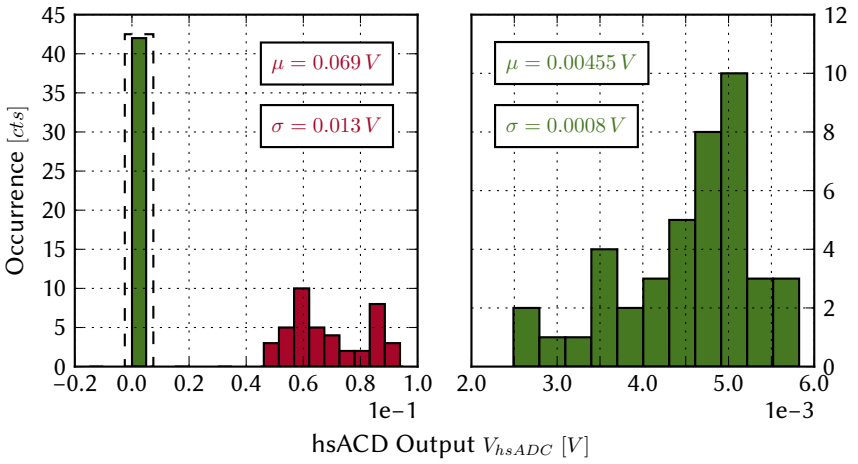

Figure 3.37: Comparison of the baseline spread of 42 hsADC channels at ideal conversion (Red) and correction with the gain values G and input voltage offset $V_{\mathrm{SM},0}$ obtained from the calibration with a linear fit (Green). The spread of the calibrated has been reduced significantly.

The standard deviation of the calibrated data set has decreased by almost two orders of magnitude with the additional offset correction. Further, the absolute offset between the distributions and the expected output of 0 V has improved for the calibrated values. They reach an accuracy of approximately $10^{-3}\,\mathrm{V}$ whereat the uncalibrated data differs on an order of $10^{-2}\,\mathrm{V}$ from the expected value. The remaining offset of approximately 5 mV in the calibrated data set relative to the ideal value 0 V could be due to the deviations from the actual characteristic curve. They are strongest in the boundary areas of the hsADC input range[17].

common mode Correction Examples

In the calibration routine of the hsADC, emphasis has been put onto the correction of the common mode influence on hsADC output used for the acquisition of calibration data. Hence, it is desirable to also eliminate this error in an experiment as the calibration data is only able to correct for the hsADC characteristics and the potential error evoked by the terminating resistor. As outlined in section 2.2, the driven hsADC inputs couple in on the common mode seen by all channels of the same chip over the internal 5 kΩ biasing resistor. Analytically, this should be correctable by tracking the

[17] cf. Figure 3.32

common mode voltage with a dedicated channel for each trigger group. Measurements with the hsADC have been carried out using a function generator [Pac93] and an oscilloscope [LeC08] as reference to investigate the quality of this correction.

In a first measurement, a rectangular signal has been applied to hsADC TG4 channel 6 with the following properties:

- Frequency: $\nu = 10\,\mathrm{kHz}$
- Offset: $V_{0,\mathrm{rec}} = 400\,\mathrm{mV}$
- Peak-to-peak amplitude: $V_{\mathrm{PP,rec}} = 400\,\mathrm{mV}$
- Duty cycle: 60 %

The values $V_{0,\mathrm{rec}}$ and $V_{\mathrm{PP,rec}}$ are referenced to a termination of 50 Ω, thus the effectively applied values are twice as large. Throughout the measurement, only the analog switch leading to TG4 channel 6 has been closed, leaving the remaining channels undriven. For the same trigger group, channel 5 has been read out almost parallel to channel 6 with a deterministic offset of 15 OCP[18] clock cycles arising from the serial handling of the data request commands processed by the FPGA. This phase shift has been considered in the correction with the neighboring trace by shifting the data points by a temporal offset Δt of

$$\Delta t = \frac{15}{\nu_{\mathrm{OCP}}} = 480\,\mathrm{ns} \tag{3.43}$$

with the frequency of the OCP clock $\nu_{\mathrm{OCP}} = 31.25\,\mathrm{MHz}$. An overview over the two measured traces is shown in Figure 3.38.

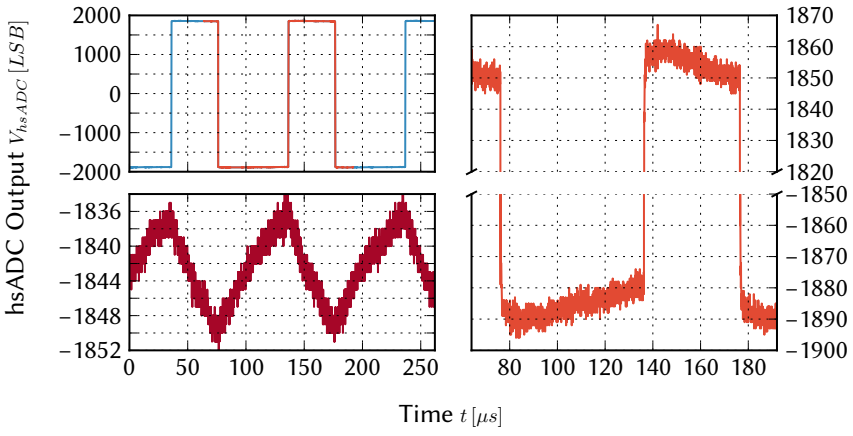

Figure 3.38: Measurement of 60 % duty cycle rectangular stimulus with TG4 channel 6 and parallel CM-tracking with channel 5. Top left: Excerpt of trace on driven channel. Bottom left: Excerpt of trace on CM-tracking channel, phase shifted. Right: Enlarged excerpt of the highlighted orange part in the top left plot for visualization of the CM impact.

The influence of the alternating hsADC input signal on the common mode can be assigned distinctly to the edges of the rectangular stimulus due to the 60 % duty cycle. It is clear to see that the input falsifies the measurement on the same channel that it is applied to by looking at the enlarged excerpt of the plateau areas of the signal.

A calibration of the trace on the driven channel has been performed with the findings on the spreading of calibrated and uncalibrated data. For both, TG4 channels 6 and

[18] open core protocol bus

5, calibration data has been available to be applied to the respective measured traces. Let V_d denote the output of the driven channel and V_n the one corresponding to the neighboring CM-tracking channel. Then, the calibrated output $V_\mathrm{d,cal}$ has been obtained in two different ways:

1. The calibration of the traces considering the gain value G_i, $\mathrm{i} \in \{\mathrm{d}, \mathrm{n}\}$ only:

$$V_\mathrm{d,cal} = \frac{V_\mathrm{d}}{G_\mathrm{d}} - \frac{5100}{5000} \cdot \frac{V_\mathrm{n}}{G_\mathrm{n}}. \tag{3.44}$$

2. The calibration with an additional channel specific hsADC-internal offset correction using the calibration values $V_\mathrm{hsADC,i}$, $\mathrm{i} \in \{\mathrm{d}, \mathrm{n}\}$ in LSB:

$$V_\mathrm{d,cal} = \frac{V_\mathrm{d} + V_\mathrm{hsADC,d}}{G_\mathrm{d}} - \frac{5100}{5000} \cdot \frac{V_\mathrm{n} + V_\mathrm{hsADC,n}}{G_\mathrm{n}}. \tag{3.45}$$

In the second correction, which takes the individual offsets from each channel into account, the shifting to the global coordinate system is immediately addressed by the correction with the neighboring trace. The two selected channels belong to the same trigger group thus are located on the same hsADC. Since the traces carry the same mean offset arising from the common reference voltage supply on the chip, the additional term V_SM in equation (3.40) does not have to be considered. Thus, the second correction is the intended use of the calibration data. In case it is desired to only regard data from a single hsADC channel it is only necessary to convert the data according to equation (3.40) where all parameters are known quantities inherent to the channel or the hsADC that it is located on. However, in this case one would have to take erroneous readouts due to the missing common mode correction into account.

Both approaches result in the traces which can be seen in Figure 3.39.

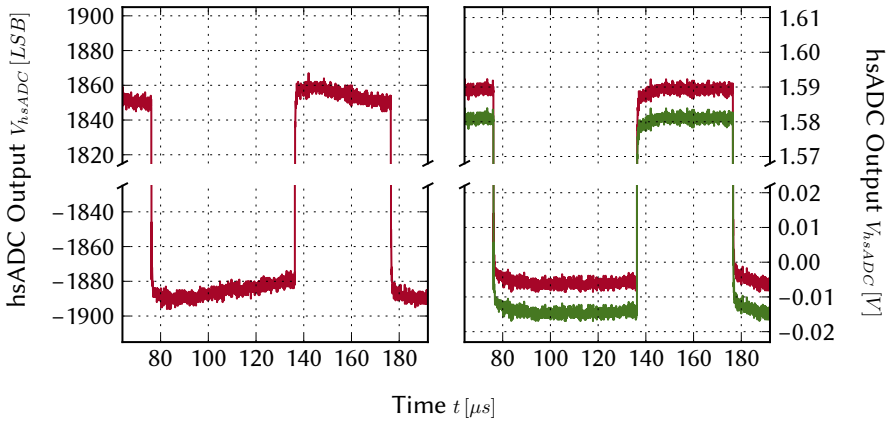

Figure 3.39: Comparison of uncalibrated and calibrated rectangular stimulus using a calibration routine considering offset errors and one that does not. Left: Enlarged, uncalibrated hsADC output. Right: Calibration with gain correction only (Red) and with gain and offset correction respectively (Green).

The ranges for the LSB-referenced hsADC output voltage V_hsADC on the left side and the volt-referenced output on the right side of the plot have been adjusted to match approximately. However, one should not deduce a quantitative relation between the excerpts that arises from the vertical arrangement alone.

By comparing the plateau of the rectangular traces one can see that the observed ramp on the uncorrected trace has been eliminated on both calibrated traces due to the common mode correction. An additional nice feature of the subtraction of the CM-tracking trace is the immediate shifting of the hsADC output values to the global coordinate system referenced to global ground. Hence, the expected range of the rectangular signal corresponding to the signal properties listed before matches for both corrected traces. Both data sets exhibit a slight displacement of the upper and lower signal extremum towards negative values. Here, the trace that has undergone an offset correction undercuts the non-corrected one, leading to values further away from the expected range of 0 V to 1.6 V. It is to be assumed that these deviations arise from the function generator which reports an offset accuracy of ±1 % of the programmed value, ±1 % of the amplitude and an additional uncertainty of ±4 mV for offsets in a range of ±800 mV [Pac93]. This leads to an error of

$$\Delta V_{\text{func},0} = 0.01 \cdot 400\,\text{mV} + 0.01 \cdot 400\,\text{mV} + 4\,\text{mV} = 12\,\text{mV} \tag{3.46}$$

in the offset accuracy with the settings listed before, potentially being larger due to the fact that the error has been calculated from the terminated settings. Taking this error into account, both the offset-corrected and the uncorrected trace are compatible to the expected signal properties.

Thus, in order to make statements about the quality of the offset correction, a comparison measurement of the rectangular stimulus has been carried out using an oscilloscope. The noise on the trace has been reduced by averaging over multiple samples via the trigger functions of the device. All three traces recorded with the oscilloscope and the hsADC, which have undergone different corrections, are displayed in Figure 3.40.

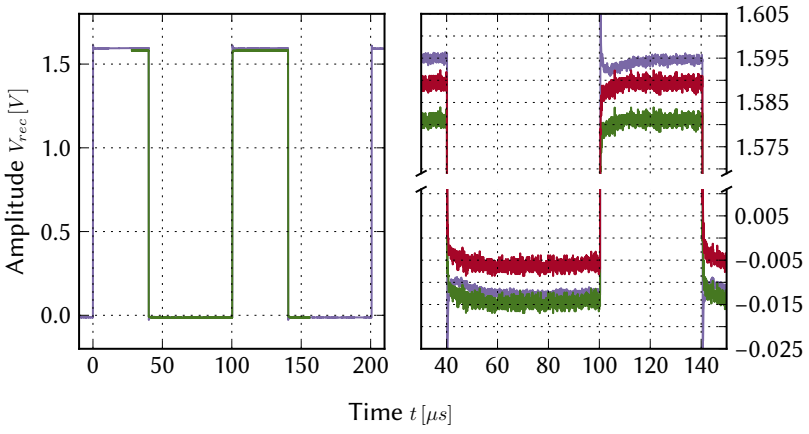

Figure 3.40: Comparison of hsADC TG4 channel 6 output with oscilloscope trace for rectangular stimulus. Left: Large scale display of the oscilloscope signal (Purple) with excerpt of calibrated and offset-corrected hsADC data (Green). Right: Enlarged excerpts of the plateau areas of the rectangular stimuli. Purple: Oscilloscope signal. Red: Calibrated hsADC output without offset correction. Green: Offset-corrected trace.

One can make two important observations with the data displayed above. The first one is that neither the offset-considering nor the non-considering trace match the oscilloscope signal perfectly. However the second one is that at least at the lower extremum the purple and the green trace show almost no difference. Thus, it is possible that the deviations between the oscilloscope signal and the fully corrected green trace at the upper range of the rectangular pulses arise from errors inherent to the oscilloscope. The manual reports a gain accuracy of ±1.5 % of the FSR for resolutions less than 10 mV/div [LeC08]. With a FSR of 800 mV this results in an expected error of

$$\Delta V_{\text{oszi}} = 0.015 \cdot 800\,\text{mV} = 12\,\text{mV}. \tag{3.47}$$

Together with a possible error due to the usage of almost the complete FSR, leading to systematic errors along the boundary areas of the characteristic curve of the hsADC, this could explain the observed differences. A difference in the terminations of hsADC and oscilloscope could also lead to a gain error. It is to conclude that for the best results both the common mode correction and the channel specific offset correction should be carried out.

On a large scale however, the additional offset correction is not noticeable. Either way, the calibration yields a significant improvement over the output values received by a theoretical conversion. Consider the excerpts of a sawtooth-shaped pulse measured with the hsADC and an oscilloscope with DC $50\,\Omega$ coupling displayed in Figure 3.41. The applied signal carried the same properties as the one introduced in section 3.2.3 with the exception of its frequency which has been changed to $\nu = 80\,\text{Hz}$ due to the higher sampling speed of $31.25\,\text{Msps}$ of the hsADC.

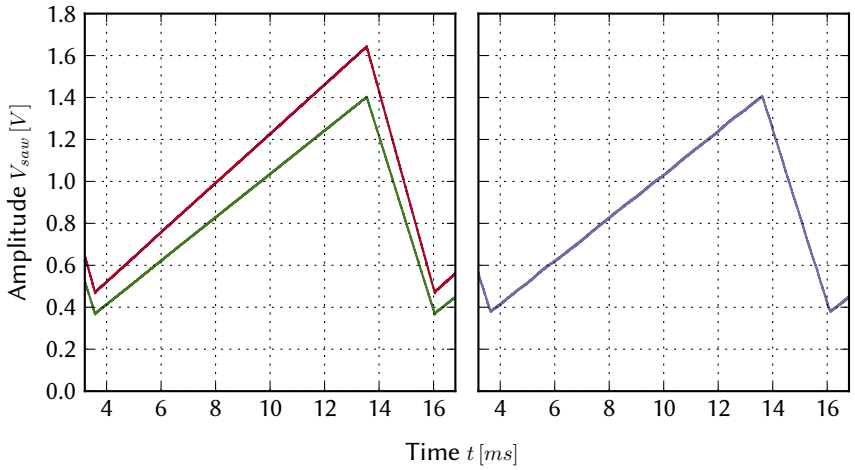

Figure 3.41: Comparison of ideally converted and calibrated hsADC data for TG4 channel 6 output of a sawtooth-shaped input signal. Left: Ideally converted hsADC output trace (Red) and output with calibration according to equation (3.45) (Green). Right: Oscilloscope output used as reference.

The ideal conversion of the data has again been obtained by multiplication of the data with $1\,\text{LSB} \approx 488\,\mu\text{V}$ and addition of the theoretical common mode voltage $V_{\text{CM}} \approx 0.47\,\text{V}$ calculated in equation (3.42). For the acquisition of the calibrated curve, the common mode correction with a trace from a neighboring channel, the gain factor G and the channel specific offsets $V_{\text{hsADC},0}$ from the linear fit have been used according to equation (3.45). The oscilloscope signal in the right plot of Figure 3.41 has been recorded by averaging over multiple samples using the trigger functions of the device. It is to see that the calibrated data significantly exceeds the conversion with theoretical values, matching the oscilloscope in offset and amplitude on a large scale.

Long-Term Stability Investigation

Similar to the examination of long-term effects on the calibration data for the lsADC regular calibration sweeps have been carried out for the hsADC. However, the observed period has been shorter for the hsADC corresponding to two weeks. Over the course of this measurement, gain and offset values for each sweep have been recorded and will be displayed in the following on the basis of the evolution of TG3 channel 2. Further, the temperature during the sweep has again been tracked using the web-based data visualizing tool *Grafana* [Lab18].

In Figure 3.42 the evolution of the offset fit parameter V_0[19] is displayed. Note that this offset does *not* correspond to the one referenced to the coordinate system of the hsADC $V_{\text{hsADC},0}$ because it has been measured against the input voltage V_{SM} in the global coordinate system. Thus, it is a worst-case estimate of the offset drift, also containing the variations of the shifted ground voltage.

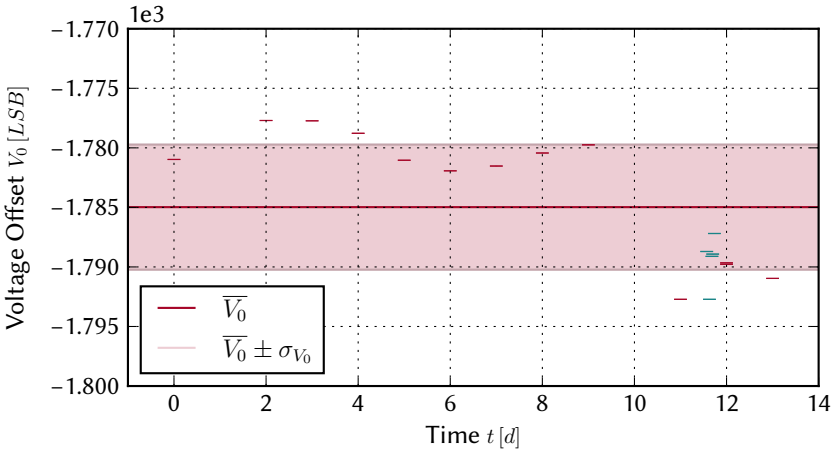

Figure 3.42: Evolution of the voltage offset V_0 over the course of two weeks with $1\,\sigma$ limits. Red: Daily recorded data. Blue: Short-term measurement of five sweeps during approximately four hours. In the range of $t = 0\,\text{d}$ to $8\,\text{d}$ a systematic drift can be observed which looks to be time dependent. Also, a systematic dip can be seen between $t = 9\,\text{d}$ to $11\,\text{d}$.

Displayed as a function of time, the offset V_0 looks to be time dependent when regarding the values in the range of $0\,\text{d}$ to $8\,\text{d}$ since the measured points seem to follow a wavy trace. After $11\,\text{d}$, however, a systematic dip in the measured values is visible. At this point, the shifted ground voltage generated by the DAC has been readjusted and a power cycle of the complete ANANAS board has been performed. Since the offset V_0 does also carry changes in the shifted ground, this might be a reasonable explanation for the observed deviations. Additionally to the long-term measurement a set of five calibration values has been acquired in a short period of time of approximately four hours. These values are highlighted in turquoise and do also exhibit a noticeable variation. The range covered by the $1\,\sigma$ limits is approximately $10\,\text{LSB}$, which corresponds to roughly $5\,\text{mV}$ variation between the limits after conversion with the theoretical hsADC LSB[20].

The variation of the gain value G can be seen in Figure 3.43. The trend of the measured points possesses systematic steps at $t = 4\,\text{d}$, $t = 11\,\text{d}$ and $t = 12\,\text{d}$. At these days, either power cycles of the ANANAS have been performed or the hsADC-internal gain factor has been adjusted. In a short period of approximately four hours, the gain factor has changed only slightly under comparable measuring conditions[21]. The range of values covered by the $1\,\sigma$ limits is approximately $10\,\frac{\text{LSB}}{\text{V}}$, which accumulates to a total error of $10\,\text{mV}$ to be expected over the full $2\,\text{V}$ sweeping range.

The temperature dependency of the calibration values has again been investigated by tracking the intake air temperature of wafer module 17. Offset and gain values have been displayed against each other in Figure 3.44 with the color-coded respective temperature during the calibration sweep. Again, changes in offset and gain exhibit a correlation which, however, is difficult to refer to temperature variations alone. In fact, the impact of temperature dependent variations seems to be small compared to

[19] cf. Figure 3.29
[20] cf. equation (3.26)
[21] Same internal gain factor, no power cycle

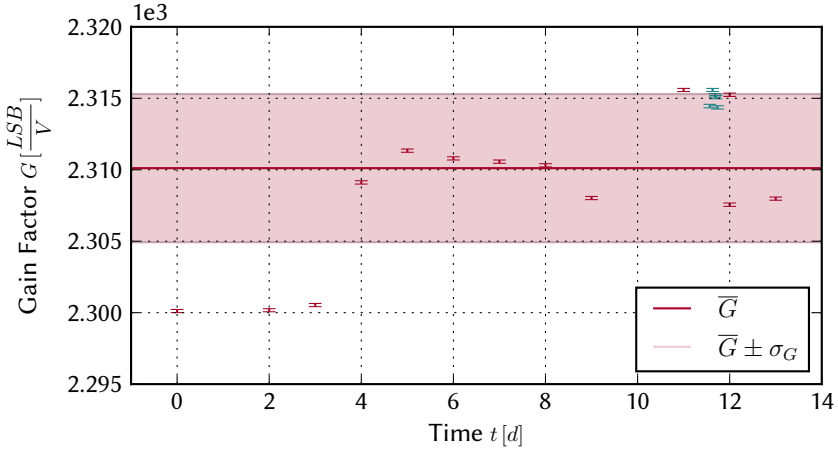

Figure 3.43: Evolution of the gain factor G of TG3 channel 2 with $1\,\sigma$ limits. Red: Data from daily voltage sweeps. Blue: Short-term measurement over the course of four hours. Disregarding the two steps at $t = 4\,\mathrm{d}$ and $t = 11\,\mathrm{d}$, the data exhibits less systematic changes over time compared to the offset in Figure 3.42.

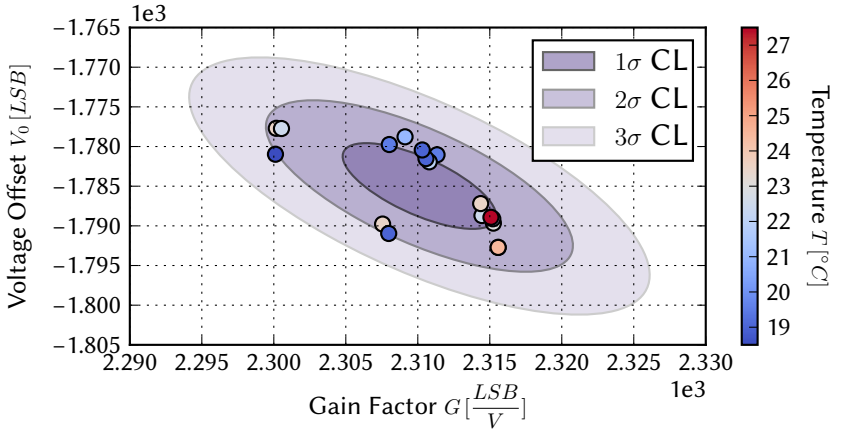

Figure 3.44: Scatter plot of the parameters obtained from a linear fit with color-coded sweeping temperature for hsADC TG3 channel 2. 1, 2 and $3\,\sigma$ confidence limits have been included to allow for an estimate of the maximum variation of the parameters over the course of two weeks.

the formation of distinct groups of two or more values, which are distant from the remaining values and arise due to user-referable changes. The group of values on the lower right side of the plot containing the red dot, which has been measured at a high temperature, corresponds to the short-term measurement over a period of four hours. Major temperature variations have been detected during this measurement, yielding a maximum of approximately 6 °C deviation. Thus, it is to conclude that the user has the most significant impact on the stability of the calibration values by performing power cycles of the board.

For a final quantification of the error evoked in measurements, which have been carried out a maximum of two weeks after the last acquisition of calibration data, the maximum deviation to an ideal characteristic curve with $G = 1$ and $V_0 = 0\,\mathrm{V}$ of the hsADC has been considered. The estimation of the loss of accuracy has been carried out analogous to the evaluation of the lsADC with the exception that the deviations have been referenced to the hsADC-internal coordinate system. The difference D is again calculated via equation (3.20) this time, however, with a different sourced voltage range V_{SM}. Since the hsADC measures the input value differentially against the common mode voltage, the offset errors σ_{V_0} have been varied around the approximate x-axis offset $V_{\mathrm{SM},0}$ occurring for an arbitrary hsADC channel. V_{SM} has been calculated using equation (3.37) with the mean offset value $\overline{V_0}$ and the mean gain $\overline{G}$ displayed in Figure 3.42 and 3.43. This does not exactly match the individual

differences of $V_{\mathrm{SM},0}$ between different channels of the same hsADC, but is only meant as an estimate. Keep in mind that the error of V_0 is a worst-case estimate including the variations of the shifted ground voltage. Then, originating from the approximate x-axis offset $V_{\mathrm{SM},0} = 770\,\mathrm{mV}$, the gain error σ_G is assumed to become stronger the further the sourced voltage V_{SM} deviates from the common mode voltage thus the x-axis offset $V_{\mathrm{SM},0}$. The described approach is pictured in Figure 3.45.

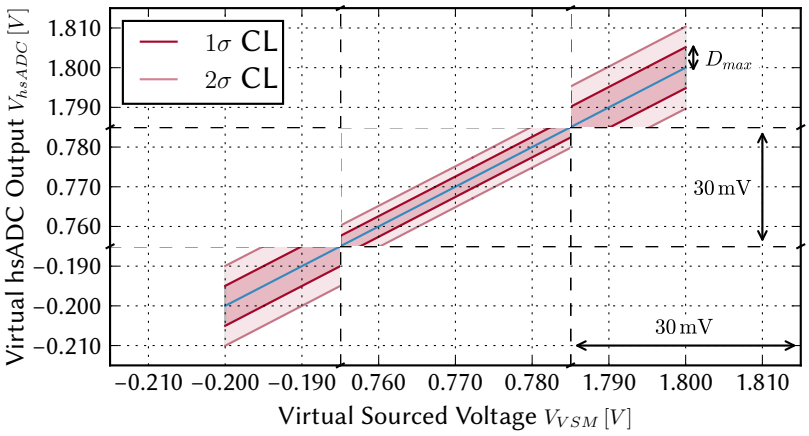

Figure 3.45: Graphical representation of the estimation of a worst-case deviation in a measurement evoked with the hsADC. Deviations arise due to calibration data variations over the course of two weeks. Blue: Ideal characteristic curve with uniform gain and no offset. Dark Red: $1\,\sigma$ envelope starting from $V_{\mathrm{SM},0}$. Light Red: $2\,\sigma$ envelope. The maximum deviation D_{max} is to be expected at the largest difference between input voltage V_{VSM} and the CM estimate.

Equal spacing has been chosen for scaling the axes along the x- and the y-coordinate. This allows to directly compare the size of the deviations from the ideal blue curve in all three relevant sectors of the plot. It is to see that offset and gain error contribute almost equally to the maximum deviation D_{max}. By reading off the value from the plot one finds:

$$D_{\mathrm{max}} \approx 5\,\mathrm{mV}. \tag{3.48}$$

Across the total input range $V_{\mathrm{SM}} = -0.2\,\mathrm{V}$ to $1.8\,\mathrm{V}$ this corresponds to a deviation of

$$\frac{5\,\mathrm{mV}}{2.0\,\mathrm{V}} \approx 0.25\,\%. \tag{3.49}$$

D_{max} can again be converted to a loss of accuracy in LSB using the theoretical value of $1\,\mathrm{LSB} \approx 488\,\mu\mathrm{V}$:

$$D_{\mathrm{max,LSB}} = \frac{D_{\mathrm{max}}}{1\,\mathrm{LSB}} \approx 11\,\mathrm{LSB}. \tag{3.50}$$

The combined error σ_{tot} from the systematic deviation $D_{\mathrm{max,LSB}}$ and the statistical uncertainty of $\sigma_{\mathrm{stat}} \approx 1.1\,\mathrm{LSB}$ for a single measurement with the hsADC is then:

$$\sigma_{\mathrm{tot}} = \sqrt{D^2_{\mathrm{max,LSB}} + \sigma^2_{\mathrm{stat}}} \approx 11.05\,\mathrm{LSB}. \tag{3.51}$$

Thus, the statistical error can be neglected in a measurement in case noise on the input signal has been suppressed sufficiently. This leads to a number X of bits lost in resolution of

$$X = \log_2(\sigma_{\mathrm{tot}}) \approx 3.5\,\mathrm{bit}. \tag{3.52}$$

Further a variation of the shifted ground voltage can be eliminated in a measurement where the common mode influence is corrected with the trace of a CM-tracking channel. Thus, if the settings of the DAC and the hsADC are kept constant, the error is expected to be much smaller. Also, the gain error is not as strong in an

actual experiment due to the comparably smaller membrane voltages. It would then also be possible that the linear approximation of the characteristic curve becomes the main source of error with a maximum deviation of $\sigma_{\text{syst}} = 4\,\text{LSB} \mathrel{\widehat{=}} 2\,\text{mV}$ at the boundary areas of the input voltage range. In this case, a maximum loss of accuracy of

$$\sigma_{\text{tot}} = \sqrt{D_{\text{syst}}^2 + \sigma_{\text{stat}}^2} \approx 4.15\,\text{LSB} \tag{3.53}$$

would be evoked which corresponds to an uncertainty of

$$\frac{4.15\,\text{LSB}}{4096\,\text{LSB}} \approx 0.10\,\%. \tag{3.54}$$

Thus,

$$X = \log_2\left(\sigma_{\text{tot}}\right) \approx 2.1\,\text{bit}. \tag{3.55}$$

For an 12 bit ADC this should be acceptable. Summing up, the best results with the hsADC should be achieved when performing a new calibration after the hsADC-internal gain factor has been changed or the board has undergone a power cycle. Otherwise, a loss of approximately 3 bit in resolution is to be expected.

3.4 HICANN

Even with a full calibration of the ANANAS frontend the accuracy of analog readout is only as good as the matching of source impedance and termination. In the case of the HICANNs on different wafers, a variation of 10 % to 20 % is expected for the value of the source impedance R_{S}[22]. This section will present the results of a measurement of the HICANN source impedances of half the amount of chips on wafer module 17. This is due to the fact that only one ANANAS board has been used, which can be connected to 24 of 48 reticles on the wafer. The total amount of usable HICANNs is further limited by the number of reticles, for which the communication with the FPGA works appropriately. Using the previously acquired calibration data and the measured value of the source impedances, a membrane trace from a single neuron on a HICANN V2 has been recorded and calibrated.

3.4.1 Determination of Source Impedances

For the determination of the HICANN source impedances R_{S} two DC measurements of a constant analog membrane voltage have been carried out with the lsADC. The determination of the 48 terminating resistors R_{T} of the frontend of the ANANAS prototype has been done as a prerequisite for the measurement of the source impedances. It is not possible to apply a voltage sweep with the HICANN as a source and deduce the value of R_{S} from the measured gain value as in the calibration routines presented before. This is due to the fact that the membrane voltage cannot be controlled as precisely as for example the output of the source meter. Thus, averaging over a characteristic input-to-output curve similar to the linear fits performed in the acquisition of calibration data cannot be done. One rather has to rely on one-shot

[22] Personal communication with Joscha Ilmberger and Maurice Güttler

measurements at constant sourced voltages. In section 2.3 it has been outlined that a two-step procedure is required to determine the source impedance. The governing equation is (2.23).

Measurements of a constant membrane voltage with the analog switches both left open and closed have been carried out. This was due to unset and set the termination. The recordings of the traces have been performed with the lsADC on the calibrated ANANAS prototype system attached to the wafer module. In order to achieve a constant membrane voltage, the neuron leak potential has been set to be significantly smaller than the threshold potential. The statistical error of the measurements has been suppressed by averaging over 500 samples per integrator of every channel. Since only the ANANAS master board has been used, which can be connected to 24 different reticles on the wafer, the terminated and unterminated traces from a total of $24 \cdot 8 = 192$ different HICANNs have been recorded. Further, not all HICANNs on the wafer could be turned on. Thus, roughly 120 valid values of R_S could be extracted from this procedure. For the determination of an individual HICANN source impedance the corresponding value of the terminating resistor R_T, the measured voltage without termination $V_\mathrm{lsADC,off}$ and with termination set $V_\mathrm{lsADC,on}$ have been applied to equation (2.23). The resulting values can be seen in Figure 3.46.

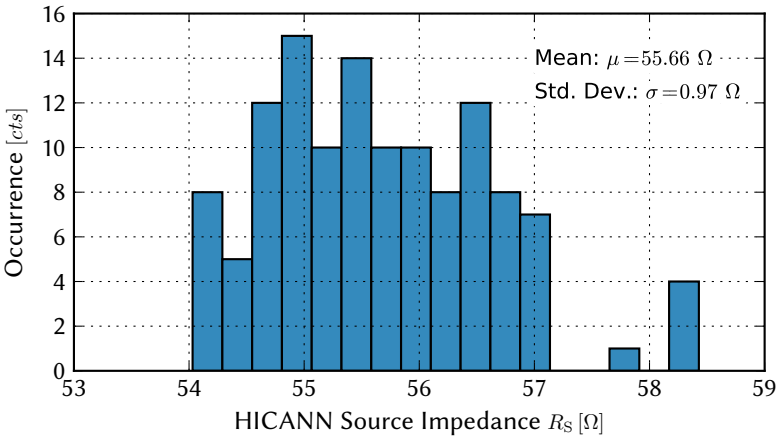

Figure 3.46: Distribution of the source impedances R_S of approximately 120 different HICANNs on wafer module 17. The mean value μ differs from the expected value of 50 Ω by roughly 11 %. Five outliers at $R_\mathrm{S} \approx 58\,\Omega$ could potentially have arisen from strong variations of the production process as they correspond to a specific reticle.

The distribution yields a mean source impedance of $\mu_{R_\mathrm{S}} = 55.66\,\Omega$. A perfect voltage divider of 50 Ω termination and source impedance would result in a gain correction factor of $C_\mathrm{id} = 2$ for the conversion of a voltage measured over the terminating resistor back to the actual input voltage. Compared to this ideal system, the observed mean source impedance value would yield a correction factor of

$$C_\mathrm{meas} = \frac{\mu_{R_\mathrm{S}} + R_\mathrm{T,id}}{R_\mathrm{T,id}} \approx 2.11 \tag{3.56}$$

with a relative error of

$$\frac{\Delta C_\mathrm{meas}}{C_\mathrm{meas}} = \frac{1}{C_\mathrm{meas}} \cdot \frac{\sigma_{R_\mathrm{S}}}{R_\mathrm{T,id}} \approx 0.9\,\% \tag{3.57}$$

under the assumption of an ideal termination $R_\mathrm{T,id} = 50\,\Omega$. Scaling factors for different HICANN V2 chips have already been presented by Sebastian Millner in 2012 [Mil12]. In chapter 4, section 1.3, table 4.1 in the dissertation, scaling factors from

2.14 to 2.32 are listed with an error of less than one percent. These measurements have been carried out for different wafers with different terminating resistor values R_T from the ones measured in this thesis. Thus, one can assume that the observed scaling factor C_meas is consistent with the large part of the listed values within the limits of the measurement uncertainty.

The standard deviation of approximately $0.97\,\Omega$ corresponds to a wafer specific relative error of

$$\frac{\sigma_{R_\mathrm{S}}}{\mu_{R_\mathrm{S}}} = \frac{0.97\,\Omega}{55.66\,\Omega} \approx 1.7\,\%. \tag{3.58}$$

The spread of the histogram in Figure 3.46 has to be compared to the uncertainty of the terminating resistors. It is to discuss whether this error justifies the negligence of the common mode influence on the measurement of the terminating resistors R_T. The distribution of the terminations yielded a standard deviation of $\sigma_{R_\mathrm{T}} = 0.08\,\Omega$, however, a possible influence of a relative error of 1 % of the common mode has been neglected earlier. Taking this into account, the error $\Delta R_\mathrm{T} \approx 0.5\,\Omega$ has been estimated from the deviation of the mean from the expected E series value of $49.9\,\Omega$. This results in a relative error of

$$\frac{\Delta R_\mathrm{T}}{\mu_{R_\mathrm{T}}} = \frac{0.5\,\Omega}{49.9\,\Omega} \approx 1.0\,\%. \tag{3.59}$$

In comparison to the wafer specific spread of the source impedances, this error is not negligible and should be corrected for to obtain high accuracy measurements of the individual R_S.

This is different, however, with regard to the large-scale deviation of $\Delta R_\mathrm{S} = 5.66\,\Omega$ of the mean source impedance with respect to the expected value of $R_\mathrm{S,theo} = 50\,\Omega$:

$$\frac{\Delta R_\mathrm{S}}{R_\mathrm{S,theo}} = \frac{5.66\,\Omega}{50\,\Omega} \approx 11.3\,\%. \tag{3.60}$$

Thus, for the correction of source impedance errors from wafer to wafer the negligence of the common mode influence in R_T should be acceptable as the respective relative error is smaller by one order of magnitude. The deviations to other wafer modules are expected to move in the same range. It would also be possible to only use the mean value of the source impedances μ_{R_S} per wafer for the correction of the membrane traces, if one is not interested in suppressing the relative error lower than 1 % to 2 %. In this case, also the impact of the common mode on the measurement of the terminating resistors could be accepted.

In summary, depending on the desired precision one is interested in to achieve throughout an experiment, the terminations could possibly be calculated more precisely. For comparison of large-scale measurements from neurons of different wafer modules though, only the deviations of the mean source impedances should be relevant.

3.4.2 Membrane Trace Measurement

As a closing application of the acquired calibration data and HICANN source impedances, a membrane trace in the constant firing regime, generated by a single

neuron on wafer module 17, has been recorded with the hsADC on the ANANAS prototype board. The neuron has been set into a state of emitting regular spikes by adjusting the leak potential to be greater than the threshold potential. TG0 channel 4 has been used for measuring the membrane trace while TG0 channel 5 has kept tracking the variations of the common mode voltage. The measured traces have been corrected with offset and gain factors obtained from previous calibration sweeps before subtracting the CM-tracking trace from the spiking one. In order to correct for the imperfect HICANN source impedance, an additional correction factor $Corr$ has been used to scale the calibrated hsADC output $V_{\mathrm{hsADC,cal}}$ after the application of calibration data and the subtraction of the neighboring trace:

$$Corr = \frac{1}{2} \cdot \frac{R_{\mathrm{T}} + R_{\mathrm{S}}}{R_{\mathrm{T}}}, \tag{3.61}$$

where R_{T} is the termination and R_{S} the source impedance. The final ouput values $V_{\mathrm{hsADC,fin}}$ are then calculated with:

$$V_{\mathrm{hsADC,fin}} = V_{\mathrm{hsADC,cal}} \cdot Corr. \tag{3.62}$$

The resulting trace can be seen in Figure 3.47. Additionally, a trace recorded with the current digitizer system has been included for reference.

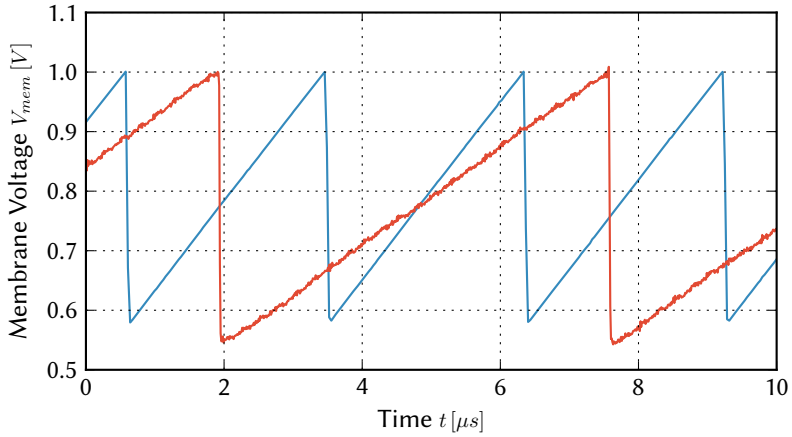

Figure 3.47: Exemplary application of calibration data to a regularly spiking membrane trace recorded on wafer module 17 with hsADC TG0 channel 4. Blue: Trace recorded using the hsADC. Orange: Reference trace recorded with the current digitizer system on a different wafer with different neuron parameters.

Despite the difference in offset due to different leakage and threshold potentials and a different spiking frequency, the trace recorded with the hsADC yields an improvement of the signal-to-noise ratio. This is satisfying as the ANANAS initially aimed to offer a more robust readout of the analog membrane traces.

4 Conclusion and Outlook

So Far...

A full calibration routine for the digital readout of the analog membrane traces of the HICANN has been developed and tested. This includes the calibration of the analog frontend of the ANANAS system, which will replace the current digitizer system assembled on the wafer modules, as well as the determination of the DC source impedances of the HICANN analog readout amplifiers. The calibration of the lsADC as well as the hsADC consists of a voltage sweep with a source meter and a linear approximation of the output values using least squares methods. The performance of the routine has been verified by comparing the calibrated ADC output of signals coming from a function generator with the recorded trace of an oscilloscope. Further, the long-term stability of the calibration data has been investigated over the course of several weeks.

In a period of four weeks after the first acquisition of calibration data and under temperature variations of 17.5 °C to 24.0 °C a maximum error of approximately 0.011 % is to be expected for the lsADC, resulting in a loss of 5.7 bit in total resolution for a single measurement. This includes the statistical error that is to be expected. Since the gain error dominates the uncertainty of the measurements, these deviations are to be expected at high input voltages of 1.8 V, which are usually not reached by the neurons. Thus, the actual loss of accuracy should be significantly smaller and therefore acceptable. It should not be necessary to model the characteristic curve of the lsADC with a polynomial of higher order than a linear fit because the long-term uncertainty dominates the systematic error.

Throughout the calibration of the hsADC the influence of the input voltage on the common mode voltage had to be considered because of erroneous readouts that are evoked by internal biasing resistors. This issue has been addressed by tracking the common mode variations with a dedicated channel and subtracting the trace from the output to be calibrated. In an experiment, this procedure also corrects for differences in the shifted ground settings of a hsADC and immediately references the obtained calibrated output to global ground. Automated calibration routines should strongly benefit from this approach while maintaining an utilization of 42 of in total 48 channels to be used in parallel. Without the solution to the common mode crosstalk presented in this thesis, only three out of 48 channels could be read out in parallel to make sure that one receives trustworthy data. Furthermore, the robustness of the hsADC calibration data has been investigated in the background of long-term stability. A worst-case estimation including disregarded variations of the shifted ground voltage yielded a maximum error of 0.25 % over the FSR of the hsADC. This indication applies to a period of two weeks and a temperature range of 19.0 °C to 27.0 °C. Thus, a maximum loss of resolution of 3.5 bit is to be expected when

not applying the correction with a neighboring channel to the recorded trace and under possible power cycles of the board. This error can be suppressed by using the common mode correction and steadily operating the ANANAS. Then, an uncertainty of 0.10 % at a loss of 2.1 bit in resolution is to be expected.

Ultimately, the examination of the long-term stability of calibration data suggests a regular calibration of the lsADCs at least once per month and at least once every two weeks for the hsADC. This applies under the assumption that the errors listed above can be accepted.

Using the lsADC, all 48 terminating resistors on the ANANAS prototype have been measured. This allowed for an indirect determination of the HICANN source impedances via a two-step measurement with and without the additional 50 Ω terminations applied. The expected deviations of 10 % to 20 % of the mean source impedance could be confirmed by investigating a single wafer, which exhibited a relative error of 11.3 % compared to the expected value. The discrepancy between expected and measured values underlined the necessity of a precise knowledge of the source impedance for the calibration of neuron and synapse parameters.

Still...

The runtime of the lsADC calibration could be scaled down significantly by improving the communication with the device. At the moment, data from different trigger groups is read back serially to guarantee for a stable data stream. A partial parallel readout promises a potential improvement of the runtime by a factor of $\frac{1}{6}$.

Note, that the period of time, which has been observed in total throughout the long-term stability measurements, is a limiting factor to the regularity of the calibration. The stable period of the calibration data could potentially be longer which could be proven by continuing the long-term investigation for an unlimited period of time. Thus, regular calibration sweeps should be carried out in the future to receive a better estimate for the maximum duration in which the calibration data is valid.

For now the temperature dependency of the calibration data has only been tested within the variations of the temperature in the testing room. A measurement in a climate controlled chamber could provide quantifiable findings on the performance of the calibration rather than a qualitative study of the correlation alone. For the calibration of the lsADC this would also allow to test for a wider range of possible temperatures, enabling an investigation under extreme condidtions. The hsADC calibration on the other hand seems to be dictated mainly by long-term drifts.

Due to the limited amount of time, only the concept of the calibration could be proved. Therefore, the already existing code has to be evolved into a fully automated routine in which the user should be able to choose which device is to be calibrated. It would also yield an improvement if the routine could be run from a RaspberryPi because of the enhanced mobility. Additionally, a dedicated cluster node could be cleared, which has been used for the communication with the source meter via USB connection. By the time this thesis has been submitted, the software stack of the ANANAS did not exist. Hence, the calibration routine has been controlled by

working directly on the communication layer of the ANANAS components. This means that the calibration has to be made compatible to the soon existing application programming interface. Then, regular overnight calibration runs could be possible on the testing rack via the open source automation server `Jenkins` [Kaw11].

Finally, the analog test adapter, which has been built for shorting the analog inputs on the test header of the ANANAS, also has to be made more robust to be applicable on a regular basis. An even better approach would be a PCB with switches for individual inputs, allowing for in-system calibration routines.

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Glossary

ADC analog-to-digital converter. 3–6, 8, 9, 16, 17, 19, 20, 26, 34–36, 39, 57, 61

ANANAS ANAlog Network Attached Sampling unit. 3, 5–8, 14–21, 27, 28, 33, 35, 38, 43, 45, 46, 48, 54, 57, 58, 60–63

CM common mode. 3, 11, 13, 39–42, 44, 47–52, 56, 60

DAC digital-to-analog converter. 38, 49, 54, 56

DNL differential non-linearity. 4

FPGA field programmable gate array. 2, 5, 17, 19, 22, 50, 57

FSR full scale range. 4, 10, 20, 36, 42, 52, 53, 61

HICANN High Input Count Analog Neural Network chip. 1–3, 5–10, 14–16, 18, 19, 29, 35, 57–62

hsADC high speed analog-to-digital converter - Texas Instruments *AFE5851*. 5–7, 11–14, 16, 17, 26, 27, 35–57, 60–62

IC integrated circuit. 3, 21

INL integral non-linearity. 4

lsADC low speed analog-to-digital converter - Texas Instruments *DDC264*. 6–11, 15–27, 29–32, 34–36, 38–40, 42, 47, 53, 55, 57, 58, 61, 62

LSB least significant bit. 4, 10, 19, 20, 26, 30, 35, 36, 45, 46, 51, 54, 56

OCP open core protocol bus. 50

PCB printed circuit board. 1, 2, 5, 46, 63

RAM random access memory. 17

SM source meter. 5, 18, 23, 37, 38, 47

TG trigger group. 13, 36–38, 40, 41, 44, 47, 50, 52, 53, 55, 60

VGA variable gain amplifier. 35, 36, 39

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