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INTRINSIC EVOLUTION OF ANALOG ELECTRONIC CIRCUITS USING A CMOS FPTA CHIP

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Abstract. *This paper surveys the research on intrinsic evolution of analog electronic circuits done at the University of Heidelberg. The aims of the project are discussed with reference to the related fields of evolvable hardware and analog design automation. A Field Programmable Transistor Array (FPTA) is used as the substrate for the artificial evolution process. It consists of 16×16 transistor cells fabricated in a $0.6\,\mu$m CMOS process. Static as well as dynamic properties of the programmable transistor array are estimated by characterization measurements of the chip. The chip is embedded in an evolution system consisting of a PC running the evolutionary algorithm and a PCI card that connects the PC to the FPTA and provides the conversion between digital and analog signals. As case studies the quasi dc behavior of different logic gates as well as a Gaussian output characteristic are evolved.*

1 INTRODUCTION

Although digital computation has replaced some of the applications of analog electronics during the last decades, the demand for integrated analog circuits is rather growing than decreasing. First, any useful electronic system has to interact with the real world, which usually involves analog electronic signals. Second, the nature of digital signals is analog. In order to push the technological limits, it is often necessary to take into account this analog nature of digital electronics. For example, the design of Gigabit serial transceivers as used in serial ATA devices is mostly an analog design problem. Unfortunately, the design of analog circuits is very time consuming as it requires the designer to think about any single transistor. At first, a suited topology has to be found. In the next step the parameters of all the circuit components must be optimized, and finally, the resulting circuit has to be laid out. Even worse, because of parasitic resistors and capacitances introduced by the layout, it may be necessary to repeat the process of parameter optimization and layout several times.

The problem of analog synthesis is approached in different ways: On one hand the efforts in the field of electronic design automation recently have lead to several tools that optimize the parameters of a given circuit topology and, in a second step, can translate the resulting circuits into a layout. On the other hand, research is done on the automatic synthesis of both, topology and device sizes within the field of evolvable hardware. Here the usage of hardware-in-the-loop offers the additional perspective of hardware that can automatically adapt to changing problems or environments. The paper briefly overviews both fields and discusses one approach to analog synthesis with a hardware-in-the-loop system that is based on a Field Programmable Transistor Array (FPTA) in greater detail.

2 RELATED WORK

The process of finding an appropriate analog circuit for the problem at hand can be divided into four levels of difficulty (cf. [1]).

1. Local parameter optimization: fine tune the device sizes of a given circuit topology, starting with a working set of circuit parameters.
2. Global parameter optimization: find optimal circuit parameters for a given topology.
3. Topology selection: choose the best out of a given set of predefined topologies and optimize its parameters.
4. Circuit design: invent a circuit that meets the desired specifications from scratch.

2.1 Electronic Design Automation: Commercial Efforts

During the last couple of years commercial tools have become available that have been proven to be capable of synthesizing circuits at the first two of the above listed levels of design automation (e.g. from Neolinear, Inc [2], Analog Design Automation, Inc [3], Barcelona

Design, Inc. [4]). The tools are reported to yield results that are better than or as good as the solutions of experienced designers in less time. However, the setup for the optimization procedure may still require quite some experience. Both, Neolinear, Inc. and Barcelona Design, Inc. provide tools to transform the optimized circuits into a layout automatically, again accelerating the design process considerably.

While the tools of Neolinear, Inc. and Analog Design Automation Inc. use heuristic search methods that draw the input for their cost function from circuit simulations based on the standard simulators of the used design framework, Barcelona Design, Inc. translates the design task to be optimized, the circuit topology and the target process into a mathematical model (more precisely a geometric program) that can be solved numerically.

Since the tools of the former two companies use generic optimization procedures together with standard simulations, they can be used to size any circuit topology suited for the problem and are independent of the target technology. Among the reported test cases are the following examples: The sizing of a high speed operational amplifier consisting of 200 components that had to fulfill 20 design goals [1]. The design was parameterized using 85 design variables (i.e., the a priori knowledge of constraints, e.g., arising from symmetry considerations, were used to decrease the number of design variables). The optimization took 8 hours on 12 Sun Sparc workstations to succeed. In [5], a cluster of 19 Sun workstations was used to find optimal dimensions for a folded cascode operational amplifier featuring 33 MOS transistors described in 13 design variables within 50 minutes.

Compared to these simulator-in-the-loop approaches the tools of Barcelona Design, Inc. use far less computational power. In [6] the 2364 variables of a 12 bit ADC are reported to be optimized within 10 minutes on a 400 MHz Pentium PC. Furthermore the geometric programming approach ensures that the global optimum for the given specification is found, or it proves that the given specification cannot be met. The disadvantage of this technique is that the application of the tool is restricted to topologies and target technologies already preprocessed by the vendor of the tool.

2.2 Evolvable Hardware

Hardware evolution can be either *extrinsic* or *intrinsic*. It is *extrinsic* if the behavior of the phenotype is simulated, and *intrinsic* if hardware-in-the-loop is used to evaluate the fitness of candidate solutions produced by the evolutionary algorithm.

2.2.1 Extrinsic Hardware Evolution

While the above examples indicate that the task of parameter optimization of a given circuit topology can readily be done, research in the field of extrinsic hardware evolution has focused on finding new circuits from scratch. All approaches sketched below use the Spice circuit simulator to evaluate their candidate solutions. Besides using different amounts of computational power and parallelism, they differ in their circuit representation.

John Koza et. al. use Genetic Programming (GP) on a 1000 node Beowulf cluster to tackle a

wide variety of engineering problems (see e.g. [7]). Among the electronic circuits evolved on a transistor level are e.g. filters, computational circuits, amplifiers and temperature sensors. To the authors knowledge the resulting circuits are not as extensively simulated as the examples from the electronic design automation community, nor are they fabricated and tested.

In [8] Jason Lohn proposed a new circuit representation technique for Genetic Algorithms (GAs) somewhat similar to GP with a linear code representation. The genotype consists of commands that drop transistors and connect their terminals. The technique was applied to the design of RCL low pass filters and bipolar amplifiers.

Hajime Shibata proposes three different encoding schemes for GAs allowing to integrate human design intuition into the circuit primitives used [9]. This may not only facilitate the difficult process of analog circuit design but also force the solutions to be better understandable to humans.

2.2.2 Intrinsic Hardware Evolution

Intrinsic hardware evolution is motivated by additional aspects. The circuitry fulfilling a specific function on a reconfigurable device can be adapted (or in the long run could even adapt itself) to a changing environment or varying requirements. Moreover, it may even be able to autonomously recover from faults occurring on its substrate.

The group of Tetsuya Higuchi for example used GAs to calibrate an intermediate frequency G_mC filter by adjusting a total of 39 bias currents [10]. Thereby, the device to device fluctuations inherent to the chip fabrication process are compensated.

One of the first successful examples of intrinsic hardware evolution experiments was the tone discriminator experiment of Adrian Thompson [11]. The task was to find a circuit on an FPGA that could distinguish between square waves of 1 and 10 kHz. Tone discrimination in the range of 100 μs to 1 ms was achieved with components having inherent time constants of nanoseconds. The first solution found was working in an analog manner using parasitic effects of the digital chip.

Reconfigurable analog devices used for intrinsic hardware evolution include Printed Circuit Boards (PCBs) , Field Programmable Analog Arrays (FPAAs) and FPTAs. A summary can be found in [12]. While the architecture of commercially available FPAAs is too coarse grained for transistor level hardware evolution, the proposed PCB system provides a limited complexity.

The group of Adrian Stoica developed three generations of CMOS FPTA chips (More information about this group is available at [13]). The last one, FPTA2, features 64 cells, each containing 14 transistors, programmable capacitors and resistors and photodiodes. By means of 44 switches each of these cells can be configured to form a variety of different building blocks, such as two- or three stage operational amplifier or logarithmic photo detectors [14]. The FPTA chips have been used in a variety of hardware evolution experiments, solving different tasks as e.g., analog filters, a 4 bit DAC and half-wave rectifiers. However, similar to the project proposed in this papers, no circuits of interesting complexity that match today's industry standards have been found yet.

The motivation for the design of the Heidelberg FPTA is threefold: First, it is designed as a search tool to find new analog transistor level circuits. Accordingly, the cells of the FPTA are used as a model for programmable CMOS transistors such that evolved circuits can be understood in terms of simulation and human design experience. The use of hardware-in-the-loop may accelerate the evaluation of candidate solutions while avoiding the simplifications inherent to simulations. Second, the FPTA is a first step towards field evolvable hardware. The device may be used to perform analog tasks that cannot be a priori specified or need the analog circuit to adapt to changing environments. Third, the FPTA can be used as a research tool to learn how to use artificial evolution for the invention of systems with higher complexity from an algorithmic point of view.

3 SYSTEM OVERVIEW

3.1 The Heidelberg FPTA Chip

The FPTA itself consists of an array of 16×16 transistor cells. PMOS and NMOS transistor cells are arranged to form a checkerboard pattern as can be seen on the left hand side of Fig. 1. Each transistor cell - depicted on the right hand side of Fig. 1 - can be configured to act as one

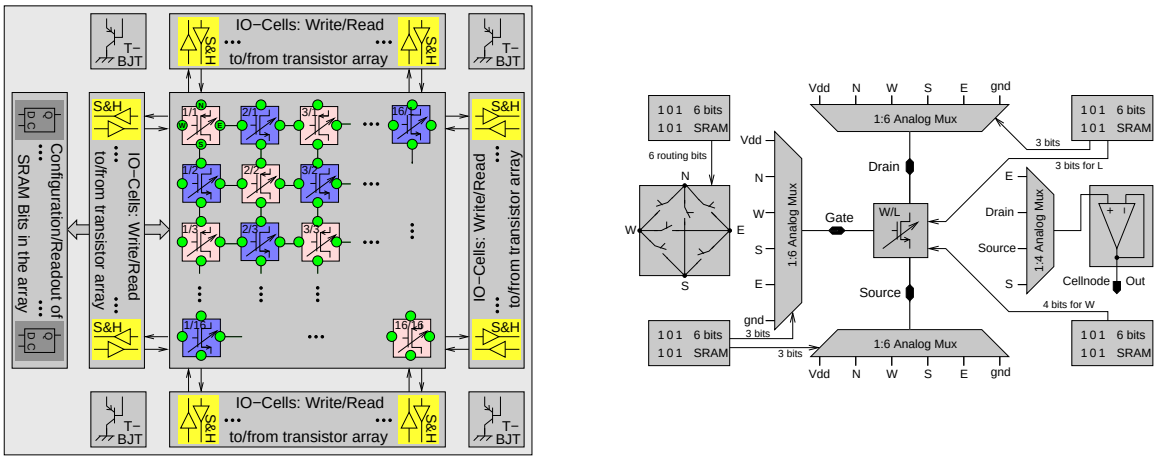


Figure 1: **Left:** Schematic diagram of the FPTA. **Right:** Block diagram of one transistor cell.

single transistor with a programmable channel dimension, where the channel width can take on the values $1, 2, \ldots, 15\,\mu$m and the channel length can be chosen from the values $0.6, 1, 2, 4, 8\,\mu$m. Each of the three transistor terminals can be connected to any of the four edges of each cell. Furthermore, six routing switches allow to route signals through the transistor cell (more information on the implementation of the FPTA can be found in [15] and [16]).

The chip was fabricated in a $0.6\,\mu$m CMOS triple metal double poly process and occupies $33\,\text{mm}^2$ of silicon. The left hand side of Fig. 3 shows a die photo of the FPTA. The configuration information is stored in SRAM cells that are part of the transistor cell. 6144 bits are needed to configure the complete chip. In order to facilitate the analysis of evolved circuits, each transistor

cell allows to read out certain node voltages and thereby to estimate some of the currents flowing through the cell. This is achieved by the operational amplifier depicted in the block diagram of the transistor cell in Fig. 1.

In order to prevent the chip from being destructed by harmful configurations, two precautions have been taken: First, the chip possesses four diodes that allow to read out the die temperature. Second, the metal lines were laid out wider at critical positions to save them from being degraded by electro-migration, or being destroyed completely by excessively high currents.

All 64 boundary cells of the transistor cell matrix can be accessed through an IO-cell. Each IO-cell can be configured to either act as an analog input or output. In input mode, the IO-cells sample the multiplexed analog input of the chip and apply this voltage to the adjacent edge of the neighboring transistor cell until they are updated with a new input voltage. Conversely, in output mode, the IO-cells sample the voltage present at the according transistor cell, which is subsequently multiplexed to the analog output of the chip.

3.2 The Evolution System

The FPTA is embedded in an evolution system which consists of a PC and an FPGA based PCI card interfacing computer and chip. Fig. 2 gives an overview of the system. On the one hand, the PCI card is used to configure the FPTA with the genotypes produced by the evolutionary algorithm, on the other hand, it manages the application of test patterns to the circuits under test. This setup combines the flexibility of software with the speed of hardware: Since the

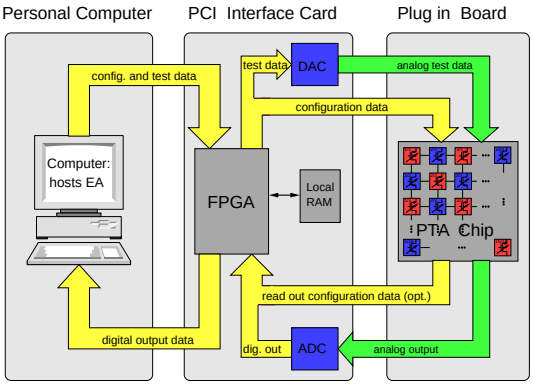


Figure 2: Overview of the evolution system.

system is controlled by software running on a computer, it is relatively easy to change the used algorithms, their used representations, or the formulation of the problem. The FPGA based PCI card makes the system a fast real time test environment that allows high test rates.

4 EXPERIMENTS AND RESULTS

4.1 Characterization of the Substrate

Flexibility usually does not come for free. If they were designed in the same CMOS process, the different transistors that can be realized with each transistor cell of the FPTA would require between 20 to 200 μm^2, yet a transistor cell covers 40 000 μm^2. The switches used to realize the configurability have a finite resistance of about 350 Ω. This deteriorates the output characteristic of the used transistor-switch-combination compared to a genuine transistor characteristic. As can be observed from the right hand side of Fig. 3, the effect is more severe for larger drain currents I_d. Moreover, the gate-source/drain overlap capacitance of all open switches connected

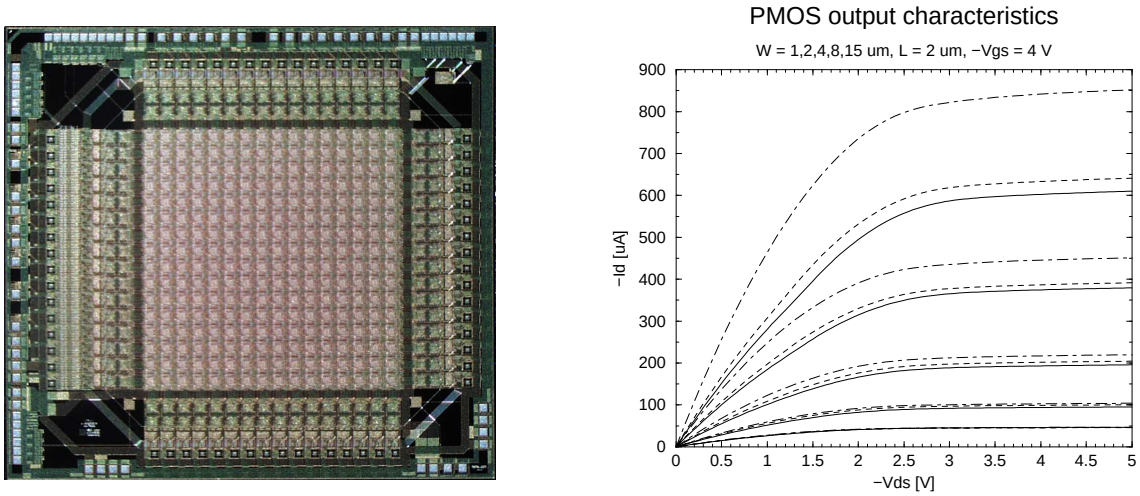


Figure 3: **Left:** Microphotograph of the FPTA. **Right:** Comparison of the measured output characteristics of a PMOS transistor cell (solid line), a simulation including all switches (dashed) and a simulation of plain PMOS transistors (dot-dashed) for different gate lengths.

to one node and the gate-channel capacitances of the closed switches add up together with the capacitances of the comparably long metal lines to form significant parasitic capacitances. Thus, the choice of the switch dimensions is a tradeoff between minimizing the effects of the parasitic resistors and capacitors respectively. Experiments with ring oscillator circuits suggest that the inverter delay for the FPTA transistor cells is larger by about a factor of 100 than for a comparable inverter implemented directly in the used fabrication process [16].

The gate delay calculated from the ring oscillator experiments for the largest W/L ratio possible ($15/0.6\,\mu$m) amounts to 8 ns. Taking into consideration a reasonable maximum for the fitness evaluation time of 10 ms (yielding a test rate of less than 100 individuals per second) the useful frequency range spans from about 1 kHz to 10 MHz, depending on the application.

4.2 Evolution of Quasi DC Behavior

Analog circuits are usually simulated and tested using different test modes: While dc sweeps test the static behavior of the circuit, transient and ac analyses are used to characterize time and frequency response of the device under test. In fact, any real measurement is bound to happen in time. Thus, a true dc test is impossible. As a remedy, the applied test patterns are randomized to prevent the candidate solutions from using any temporal correlation therein. This sort of dc test was used to evolve the *quasi dc* behaviors of logic gates and Gaussian voltage transfer characteristics (V-V curves).

Throughout all experiments a simple GA was used together with truncation selection. The circuit representation in the genotype preserves the transistor cell structure of the FPTA: While the mutation operator is free to change any characteristic of any transistor cell, crossover is restricted to exchanging two-dimensional blocks of transistor cell data. The quadratic deviation of the measured circuit response from the desired target behavior is taken as a fitness criterion. This error function is minimized during the evolution run. In the presented results the achieved errors are scaled to the root mean square error per measured input data point in mV

$$\text{RMS Error} = \sqrt{\frac{\sum_{i=1}^{512}(V_{tar}(i) - V_{out}(i))^2}{512}} \times 1000\,, \tag{1}$$

with the target voltage being a function of two input voltages in the more general case of the logic gates experiments

$$V_{tar} = V_{tar}(V_{in1}, V_{in2})\,. \tag{2}$$

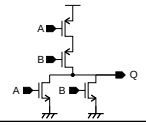
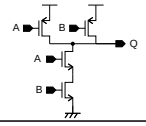
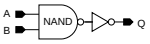
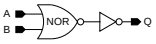
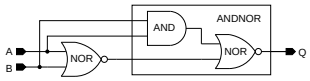
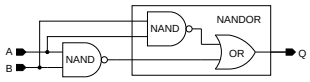
In both experiments the generation size was set to 50 and 512 test points were used. The logic gate experiments ran for 5000 and the Gaussian output characteristic ones for 10000 generations, which took about 30 and 60 minutes respectively.

4.2.1 Logic Gates

In a series of artificial evolution experiments the quasi dc behavior of the six symmetric logic gates NOR, NAND, AND, OR, XOR and XNOR was evolved. A total of 100 runs was performed for each of the gates. The successful solutions were required to respond with the correct output voltage (5 V for a logic one and 0 V for a logic zero) depending on the two input voltages. The input was considered low if it was below 1.7 V and high for voltages higher than 3.3 V. During all runs only 5×5 transistor cells were accessible for the GA.

As can be seen from the histograms in Fig. 4, the difficulty to find good solutions for the different gate types corresponds to the different levels of complexity exhibited by the according textbook solutions: While good solutions to the NOR and NAND problem are found quite frequently, the success rate for the OR and AND gates is considerably lower. In 100 runs, no perfect solution could be obtained neither for the XOR nor for the XNOR.

Fig. 5 compares the measured behavior of the best NAND, AND and XNOR gates evolved to the simulated characteristics of their text book counterparts. The simulation results were

Gate	Implementation	Transistor Count
NOR		4
NAND		4
AND		6
OR		6
XOR		10
XNOR		10

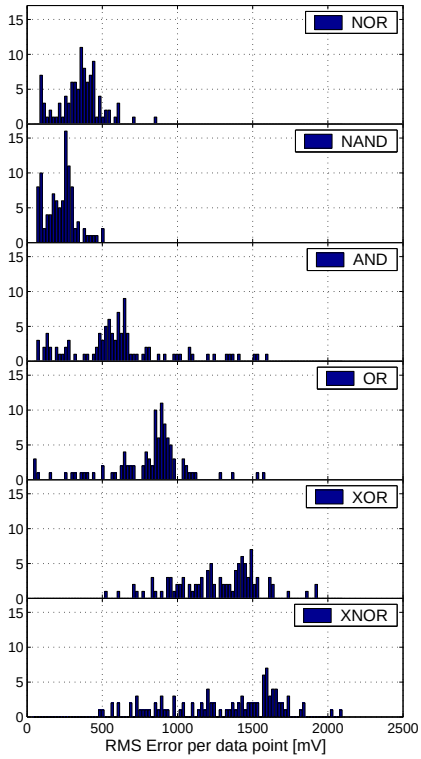


Figure 4: **Left:** Typical CMOS implementations of the 6 logic gates NOR, NAND, AND, OR, XOR and XNOR. **Right:** RMS deviation from the ideal response for 100 evolutions of the dc behavior of these 6 logic gates.

obtained using the same CMOS process the FPTA was fabricated in. The evolved circuits were tested outside of the optimization loop to analyze the stability of the evolved solutions. The tests were repeated on a second FPTA chip. The vast majority of the evolved circuits and in particular the successful ones the plots from Fig. 5 are based on achieved similar RMS errors on both chips, which indicates a minimum of robustness against the device fluctuation inherent to the fabrication process of the chip.

By means of similar experiments focusing on finding symmetrical logic gates the influence of different test pattern application schemes has been investigated. The results indicate that it is a) necessary and b) sufficient to apply the input value pairs in random order to prevent the evolution process from abusing time dependencies inherent to the test patterns (cf. [17]). However, this procedure cannot rule out long term instabilities occurring on time scales larger than the ones used during the evaluation of the circuits.

4.2.2 Gaussian Output Characteristics

In a second series of experiments it is attempted to evolve a circuit that has a Gaussian dc characteristic. Different experiments are carried out, in which the fraction of the chip that can

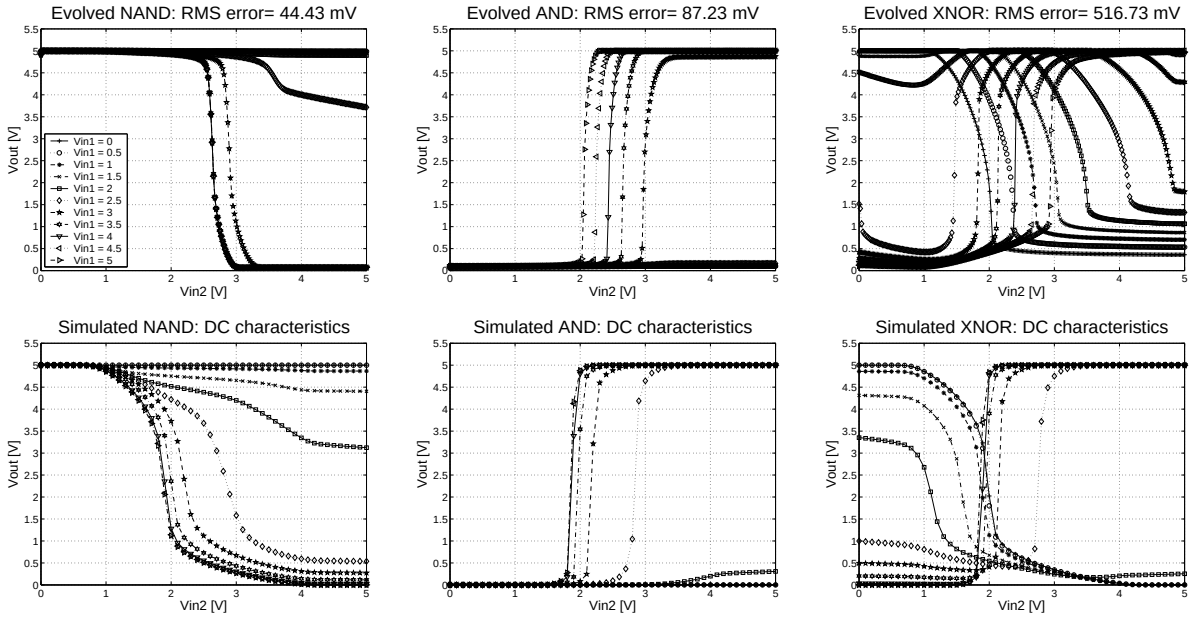


Figure 5: **Top:** Measured performance of the best evolved NAND, AND and XNOR gates. **Bottom:** Simulation results for the NAND, AND and XNOR gates depicted on the left side of Fig. 4. The legend shown in the plot in the upper left corner is used for all 6 plots.

be used by the evolutionary algorithm is varied. For each edge length of the quadratic array available to the GA 10 runs are carried out. The used edge lengths range from 4 to 11. Fig. 6 shows the output characteristics of the best evolved solutions for edge lengths between 4 and 9 cells. On the one hand, many of the obtained circuits match the required output voltages quite closely, but on the other hand, the resulting curves do not exactly follow a Gaussian shape. Being restricted to the same amount of computing time, runs having access to more resources do not necessarily produce better solutions. However, the RMS error for the best solution found for edge length 4 seems to be a bit worse than the best circuits of the other edge lengths.

5 CONCLUSION AND OUTLOOK

Tools that optimize the parameters of a given topology are readily available. They release analog designers from the lengthy process of tweaking transistor dimensions and can be integrated in the usual design flow. Work on the extrinsic evolution of analog transistor level circuits concentrates on improving the circuit representation and how to integrate human design intuition into the optimization procedure. The reported results are promising but lack the verification demanded in industry. Experiments with analog reconfigurable devices demonstrate the feasibility of intrinsic hardware evolution, but also indicate the long way to hardware evolution of circuits that are competitive with human designs.

The Heidelberg FPTA project is one of the few approaches to intrinsic transistor level hardware evolution. Since the chip is based on programmable transistor cells it can be used to find new circuit topologies. However, the configurability of the FPTA entails additional parasitic re-

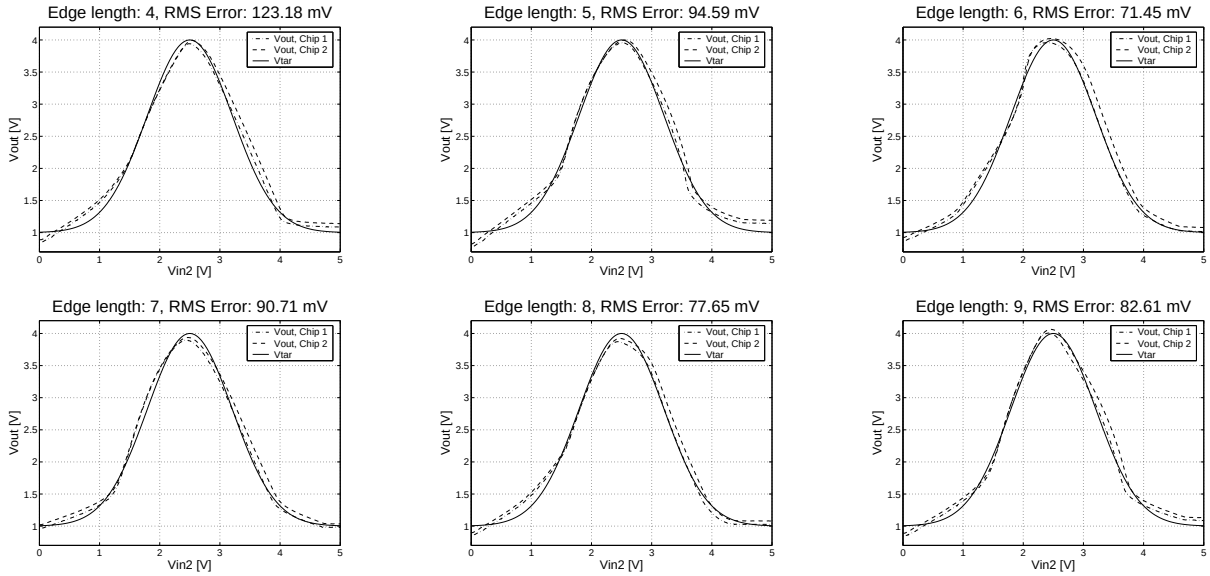


Figure 6: Output characteristic of the best Gaussian circuits for different available array sizes. Chip 1 refers to the chip the circuits were evolved on. The curves denoted with chip 2 illustrate the response of the same circuits tested on a different die.

sistances and capacitances that limit the maximum bandwidth of the transistor array and slightly deteriorate the transistor cell characteristics. In future it is planned to add an interface to the system that allows to simulate and analyze evolved circuits with one of industry's standard circuit simulators. Analysis of the evolved circuits will show to what extend the programmable transistor cells can be used as a transistor model. Differences between simulation and measurement can be further analyzed by simulating the transistor cells including all parasitic effects, an option usually not available for commercial FPAAs.

The two experiments presented show the capability of the system to find solutions to well known problems as well as to more uncommon tasks. The fact that most of the evolved circuits performed equally well on two different dice outside of the optimization loop indicates that they do not rely on details of the particular transistor cells they have been evolved on. In order to enhance complexity and quality of evolvable circuit solutions the optimization procedure will be improved for example by using building blocks or more sophisticated circuit representations that may include prior design knowledge. Eventually, the experiences gathered shall lead to a second generation FPTA.

6 ACKNOWLEDGMENT

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