A learning electronics Chip
A fast approach to hardware evolution with a VLSI transistor array

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Introduction to Evolvable Hardware

Related work

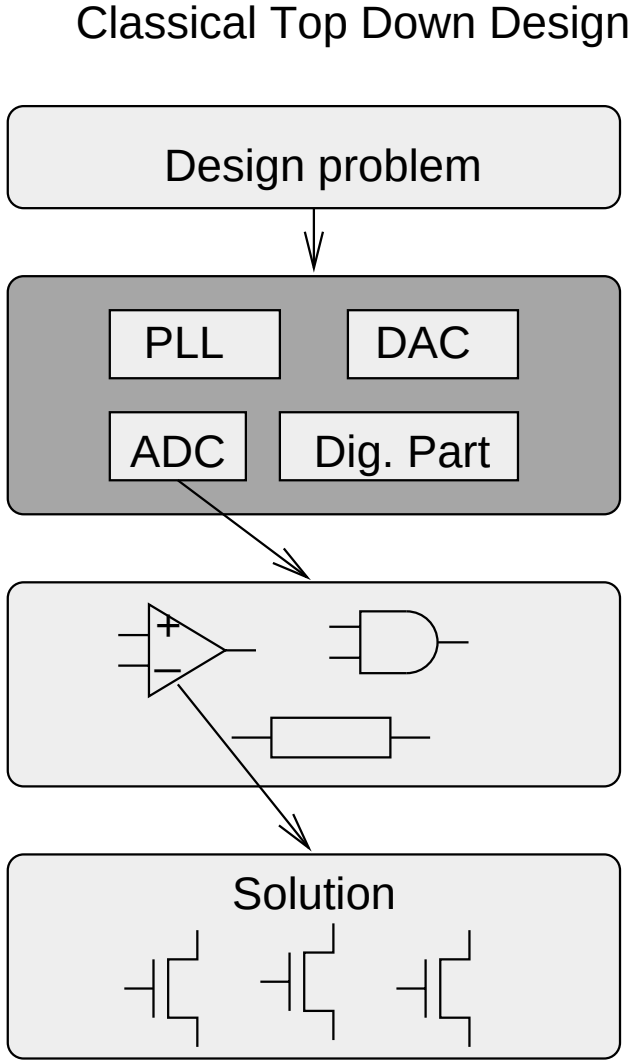
The Programmable Transistor Array (PTA)

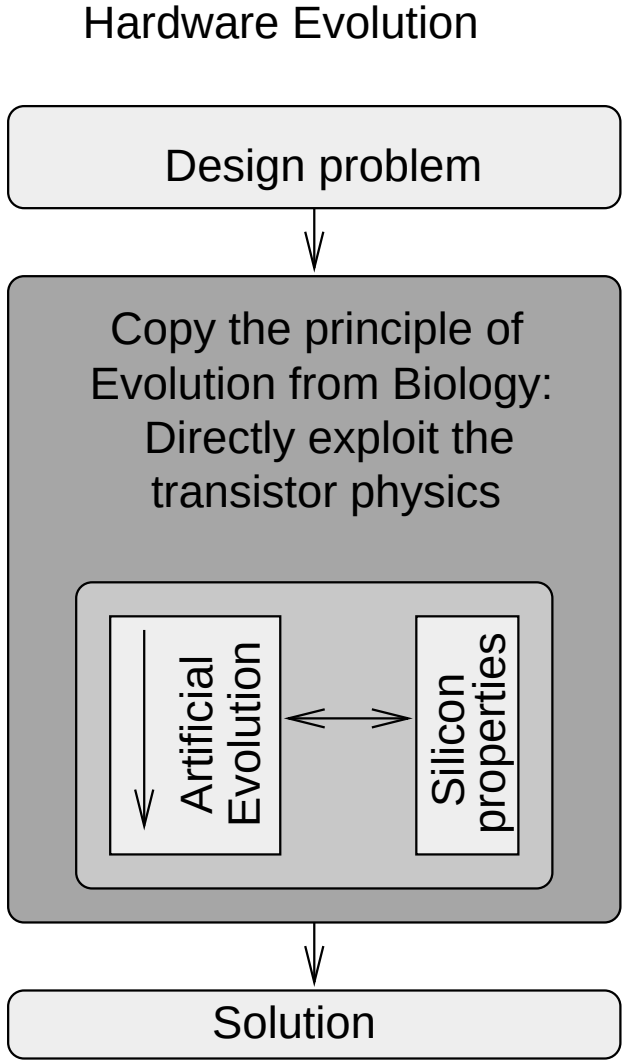
The Evolution System

Simulation results

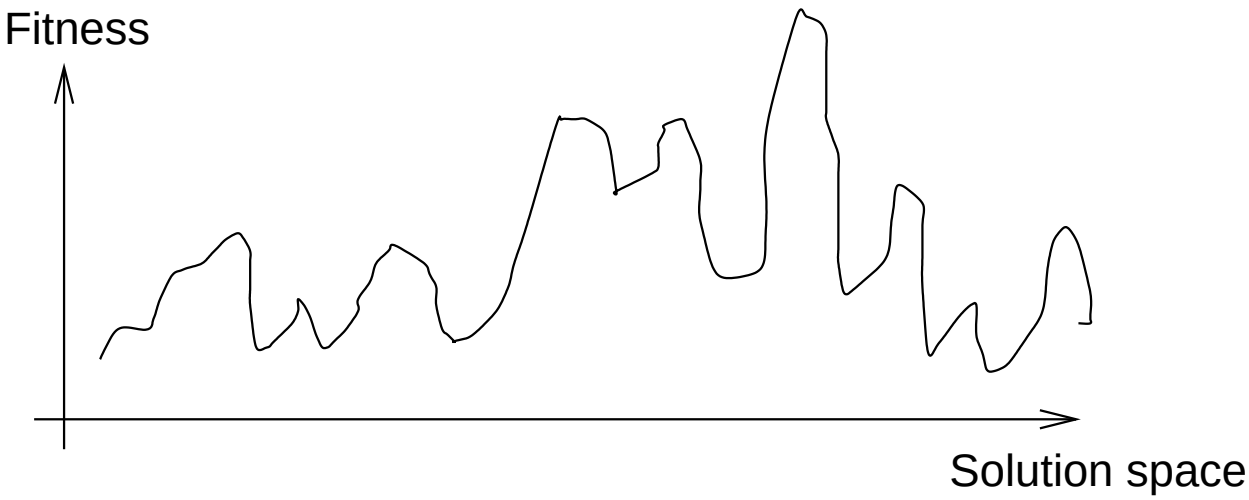
Conclusion and Outlook

Motivation: Different approaches to circuit design





Optimisation problems and NP-hardness



Goal: Find global Maximum/Minimum
Problem: Solution space is too big

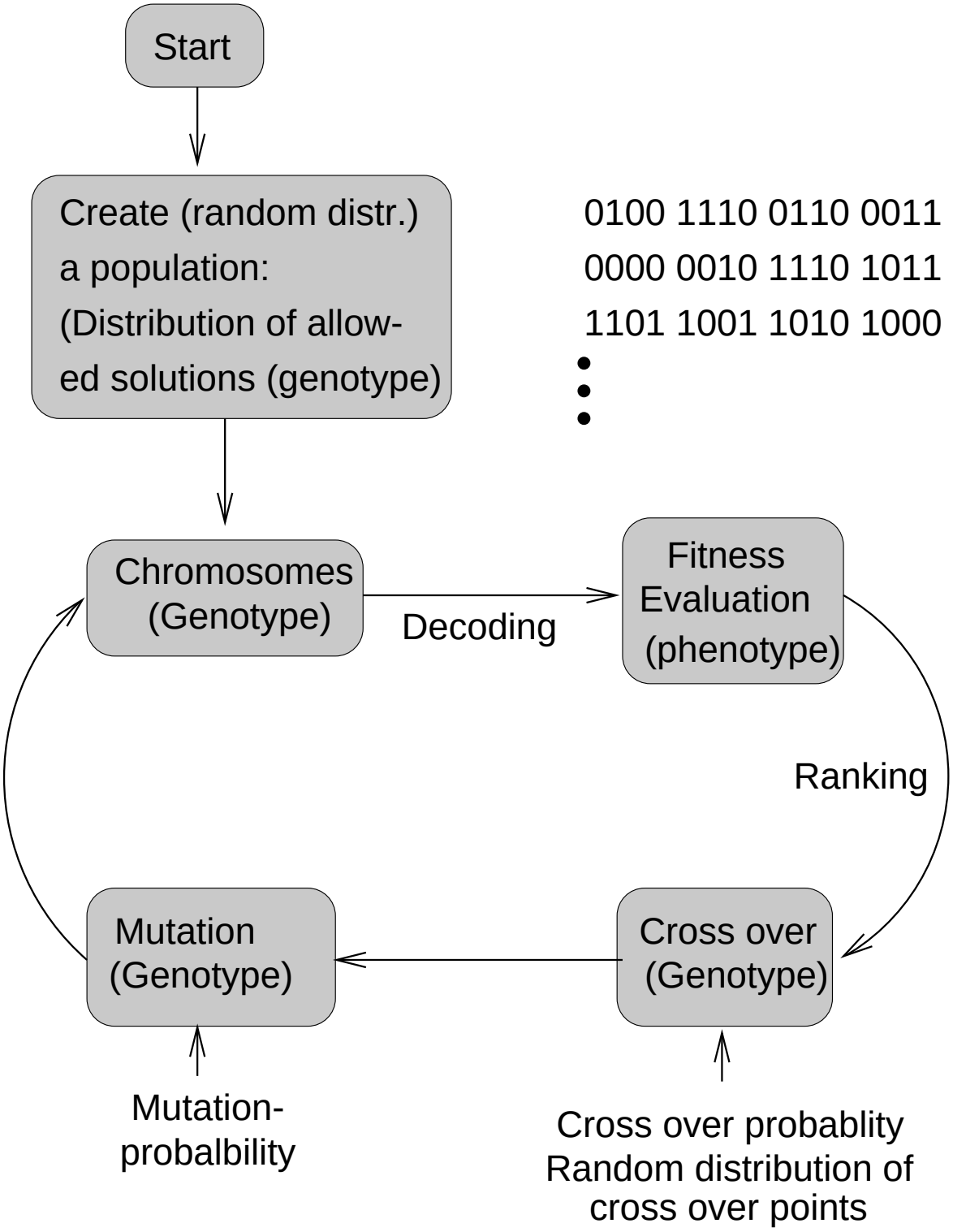
e.g. NP-hard problems: Number of solutions increases exponentially with the number of input parameters (e.g. traveling salesman)

=> Only test small fraction of all possible solutions and seek a good local optimum instead of the global optimum

Typical strategies:

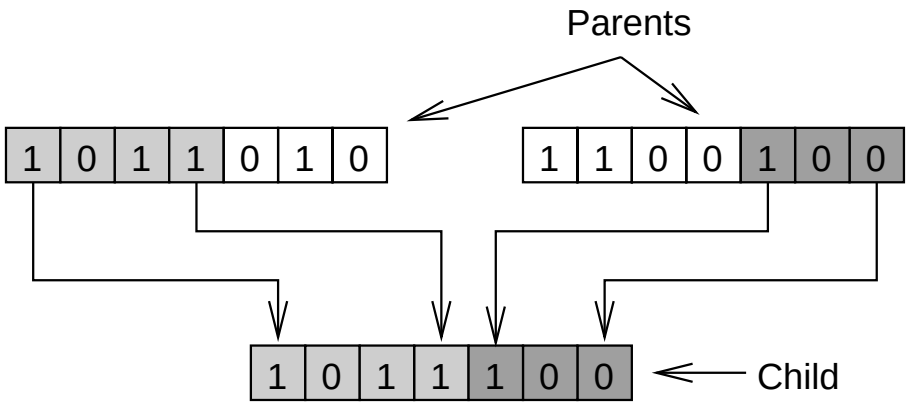
- Hill-Climbing
- Simulated Annealing
- Genetic Algorithms

Genetic Algorithms (2)

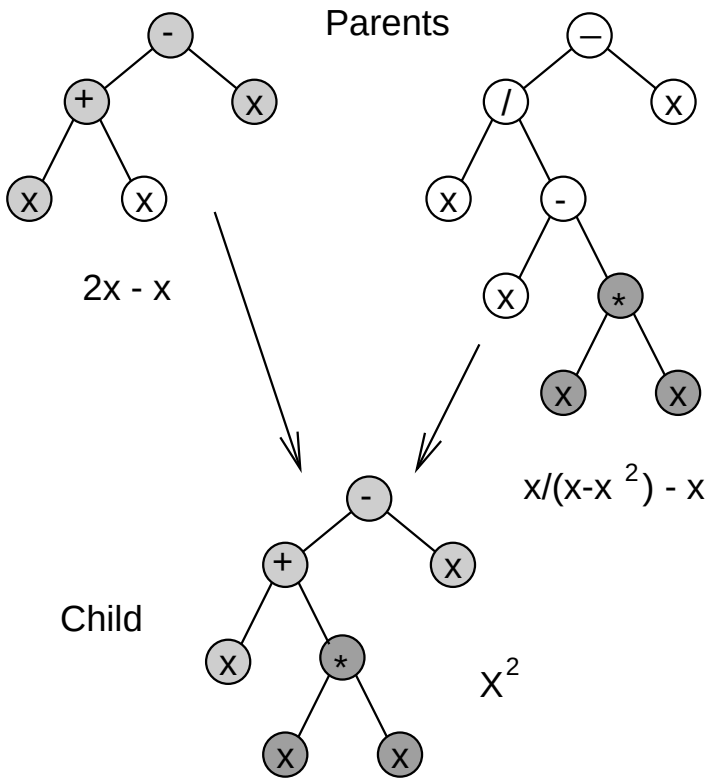


Representations and Crossover (1)

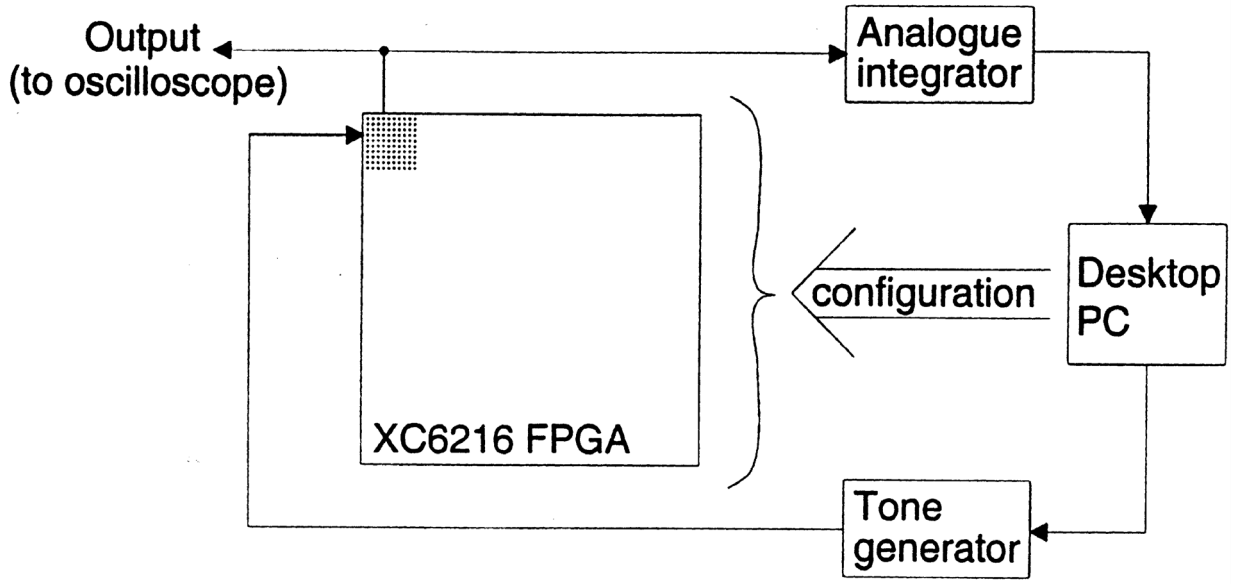
Bit string Representation:



Representation for Genetic Programming (GP)



Example 1: (Experiments of A. Thompson)



Experiment of A. Thompson: in 1st Int. Conf. on Evolvable Systems (ICES96). Springer LNCS

Test pattern: Square waves with different frequencies:

1) 5 x 1 kHz, lasting for 500 ms
2) 5 x 10 kHz, lasting for 500 ms

} in random order

Fitness measurement: output is integrated during the 500ms in which the input signal is presented

$$\text{Fitness} = \left| \sum_{t \varepsilon S_1} i_t - \sum_{t \varepsilon S_{10}} i_t \right|$$

Set of
5 10kHz-tones

i_t : output of the integrator at the end of the integration time

Example 1 (Results of A. Thompson) (2)

Results: 1 Chip, no clock

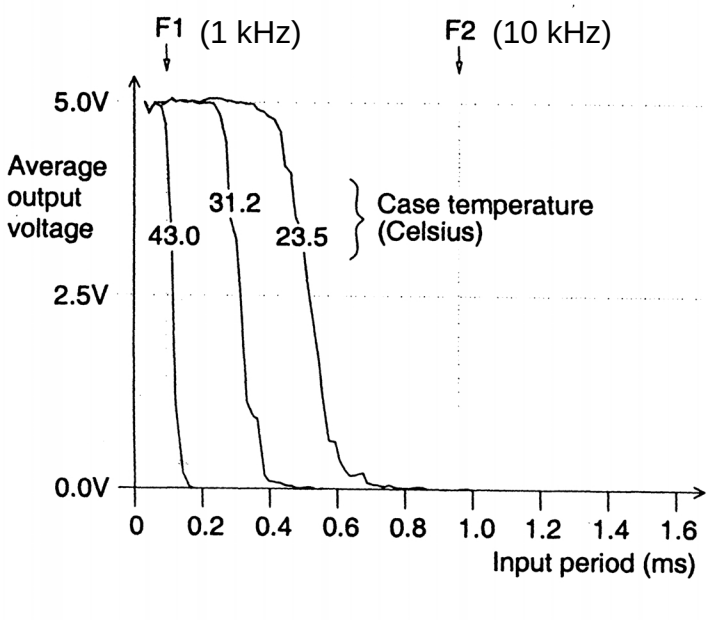
- Perfectly working solution after 5300 generations
  (length of bitstring =1800 bits, population size = 50)

- time for input signal: 5 s

- Time of the whole experiment: More than 2 weeks

- Solution: analog, not digital, but imagine:
  Time constants: FPGA: 2-4 ns, 1 to 10ms for given task

Variation of the discrimination frequency with temperature:



From:Proc. 1st Int. Conf. on Evolvable Systems (ICES96), A. Thompson. Springer LNCS

Example 1 (Results of A. Thompson) (3)

Results: 4 Chip, 6 MHz clock

Task: Evolve circuit robust to variations with regard to variations in the circuits environment.

Conditions of the 4 chips used to evolve the robust circuits:

Chip	Fabrication	Package	Interface	Temperature	PSU	Output load	Position
1	Seiko	PQFP	parallel	in PC	PC's 5V s.m.	-	(37,30)
2	Yamaha	PLCC	serial	ambient	5V lin.	1kΩ	(32,0)
3	Yamaha	PGA	serial	60°C	4.75V s.m.	-	(63,0)
4	Seiko	PGA	serial	−27°C	5.25V s.m.	-	(37,54)

From: Proc. 3rd Int. Conf. on Evolvable Systems (ICES00), A. Thompson, P. Layzell. Springer LNCS

Result:

Digital circuit working for the chips evolved, as well as for 6 chips not used during the evolution process for:
- 50 deg C < T < room temperature

Circuit can be simulated.

Thompson: "Unconstrained evolution can produce circuits beyond the scope of conventional design rules"

Example 2 (Work of Koza et al.)

Extrinsic HW Evolution: Canditate solutions are simulated !

Task: Evolution of a 60 dB amplifier with discete BJTs on a PCB:

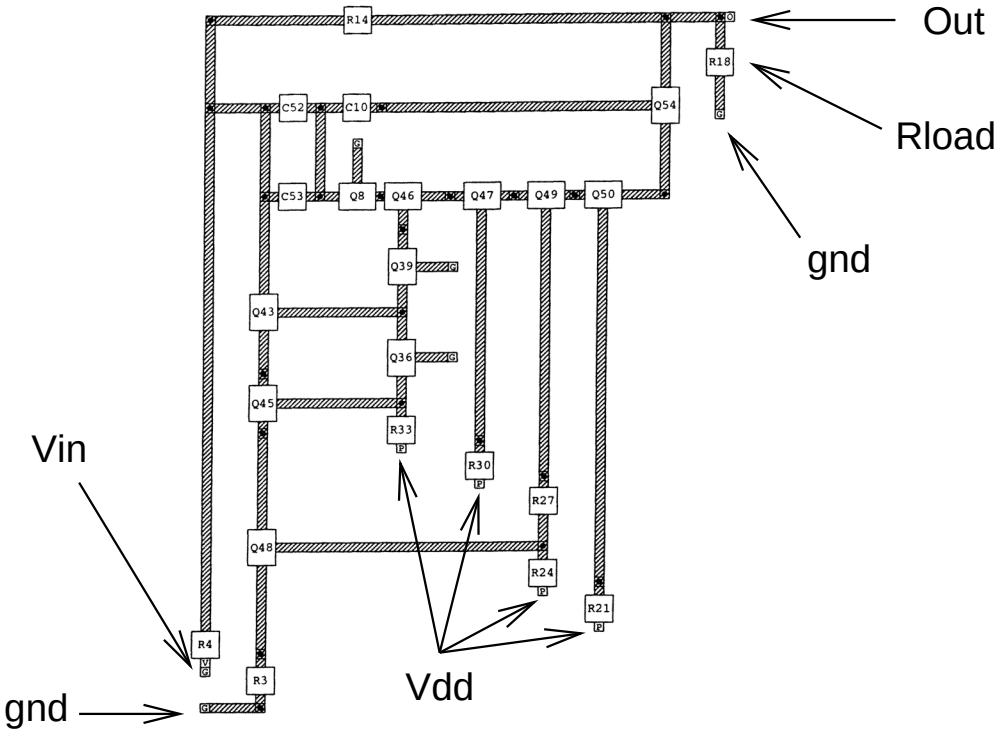
topology device identity Sizing Place & Route

Method: SPICE simulation (5 points) on a cluster of 1000 Pentium II 350 MHz

Fitness included: gain, offset, linearity, occupied area

Population size: M = 10 000 000

Number of generations: 101, best candidate given below

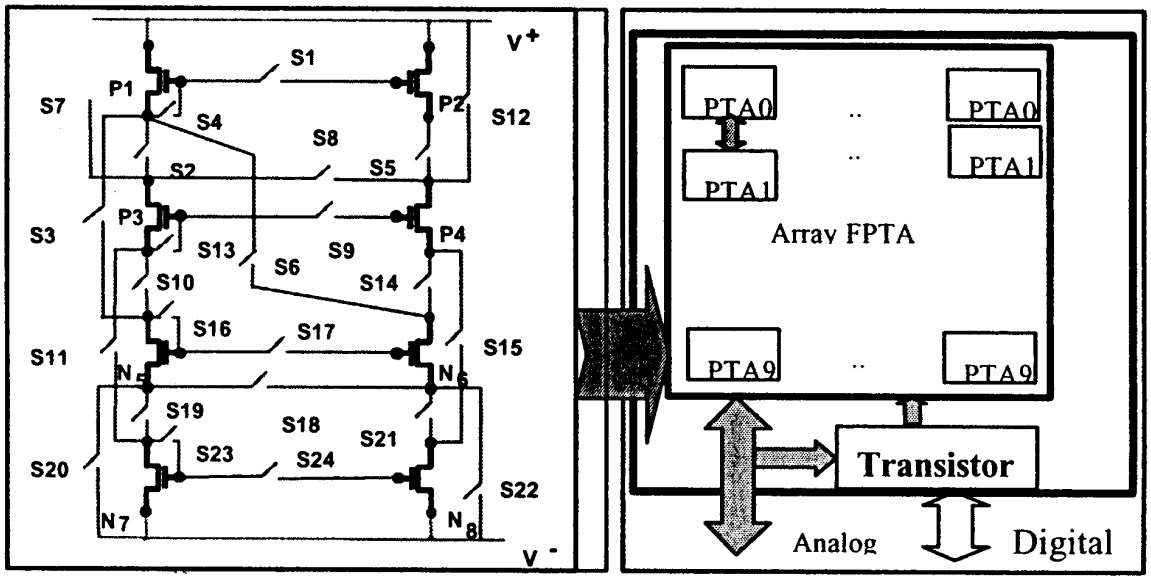


From: Proc. 3rd Int. Conf. on Evolvable Systems (ICES00), J.R. Koza et al. Springer LNCS

Example 3 (Work of Stoica et al.)

Field Programmable Transistor Array (for spacecraft applications)

Left: PTA cell already built Right: array being developed



From: Proc. 3rd Int. Conf. on Evolvable Systems (ICES00), A. Stoica et al. Springer LNCS

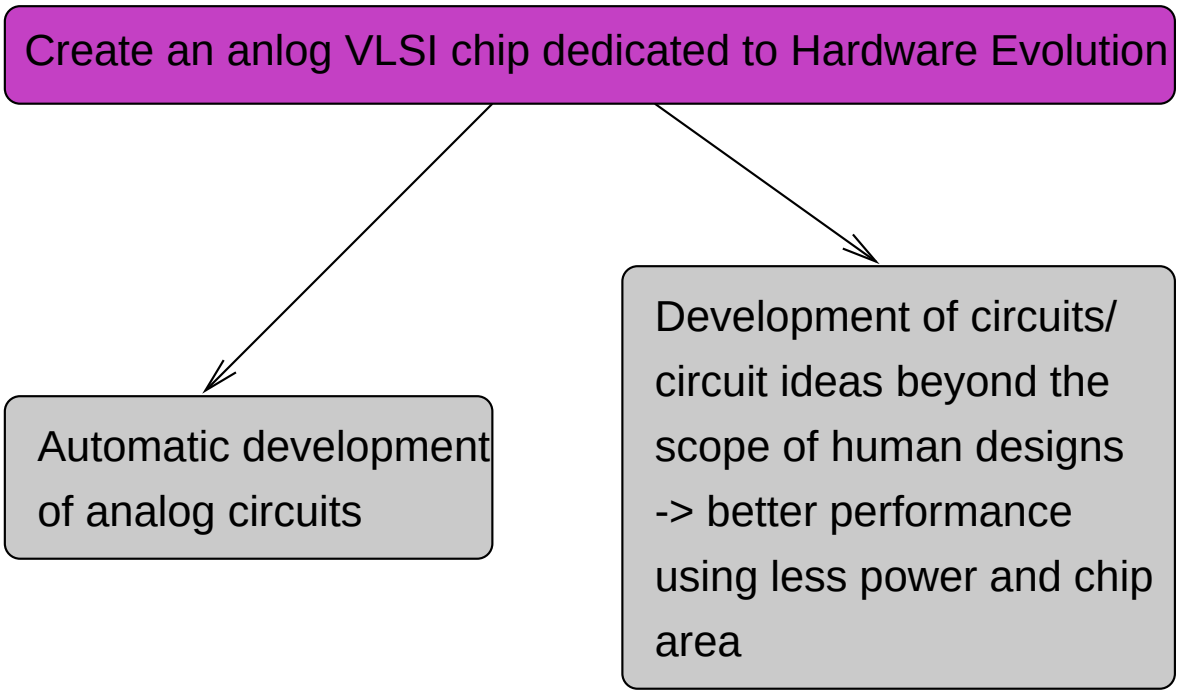
SW evolution on a 256 HP cluster simulating the PTA-cell
HW evolution with the PTA-cell

-> Evolved: - circuit with Gaussian I-V characteristics
- Inverter

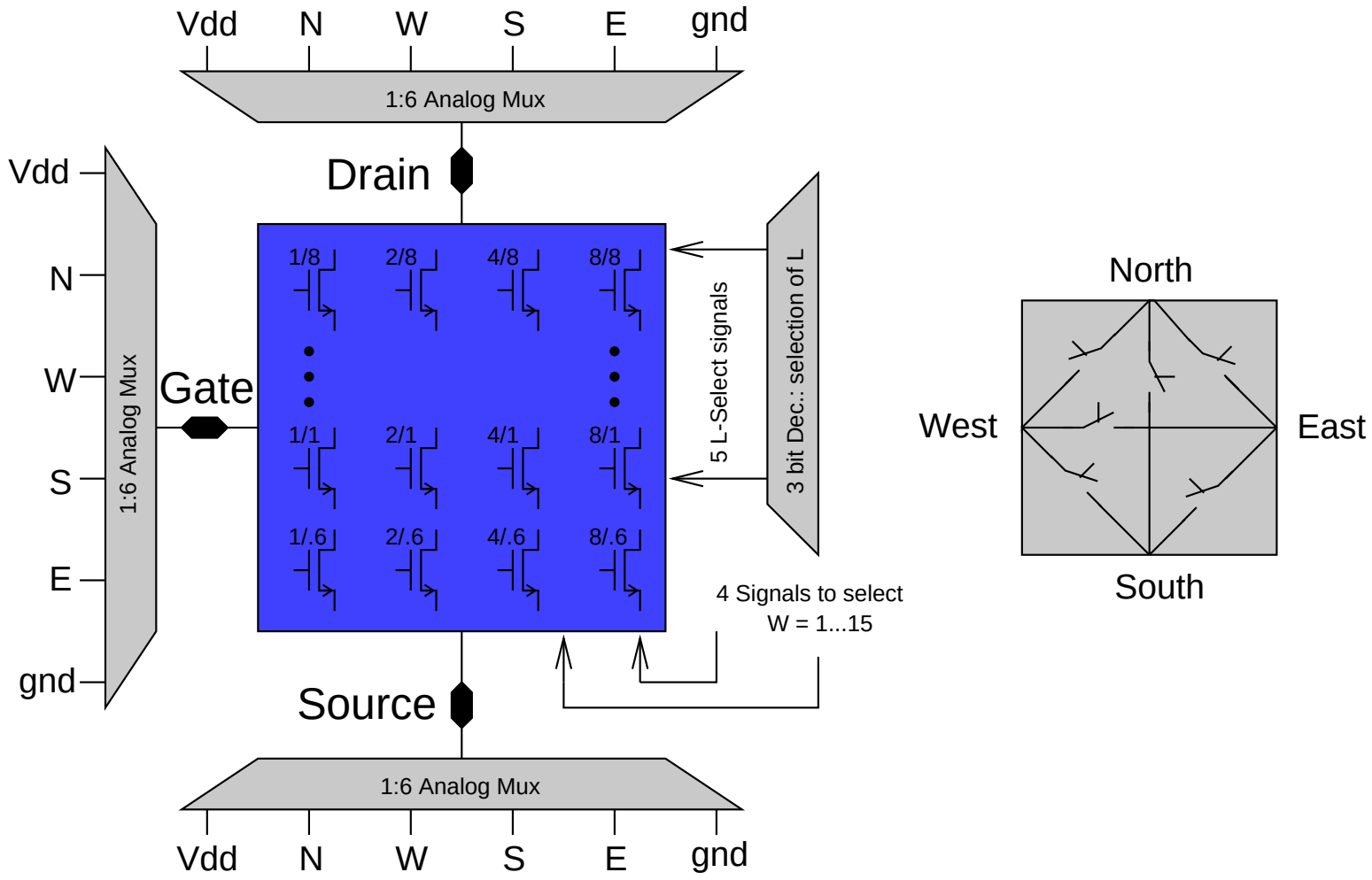
Observation: evolved circuits are not always portable from
one chip to another or
from HW to SW or vice versa

-> A mixture of SW- and HW- evolution is proposed:
-> Mixtrinsic Evolution

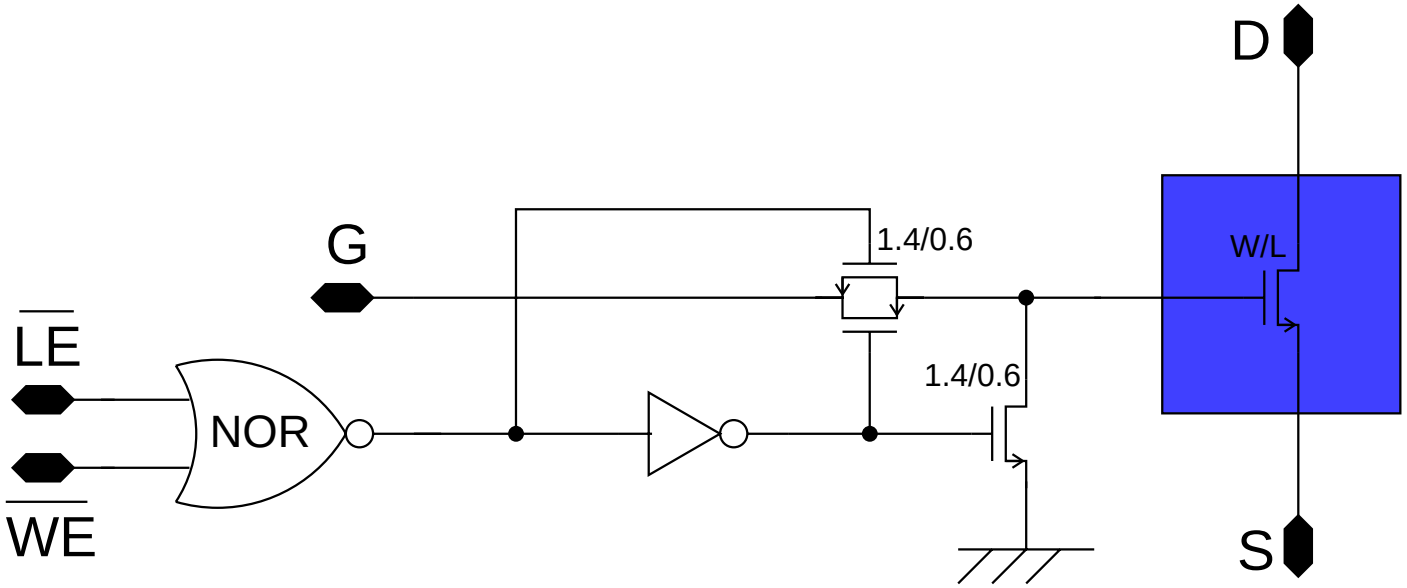
Goals of the project



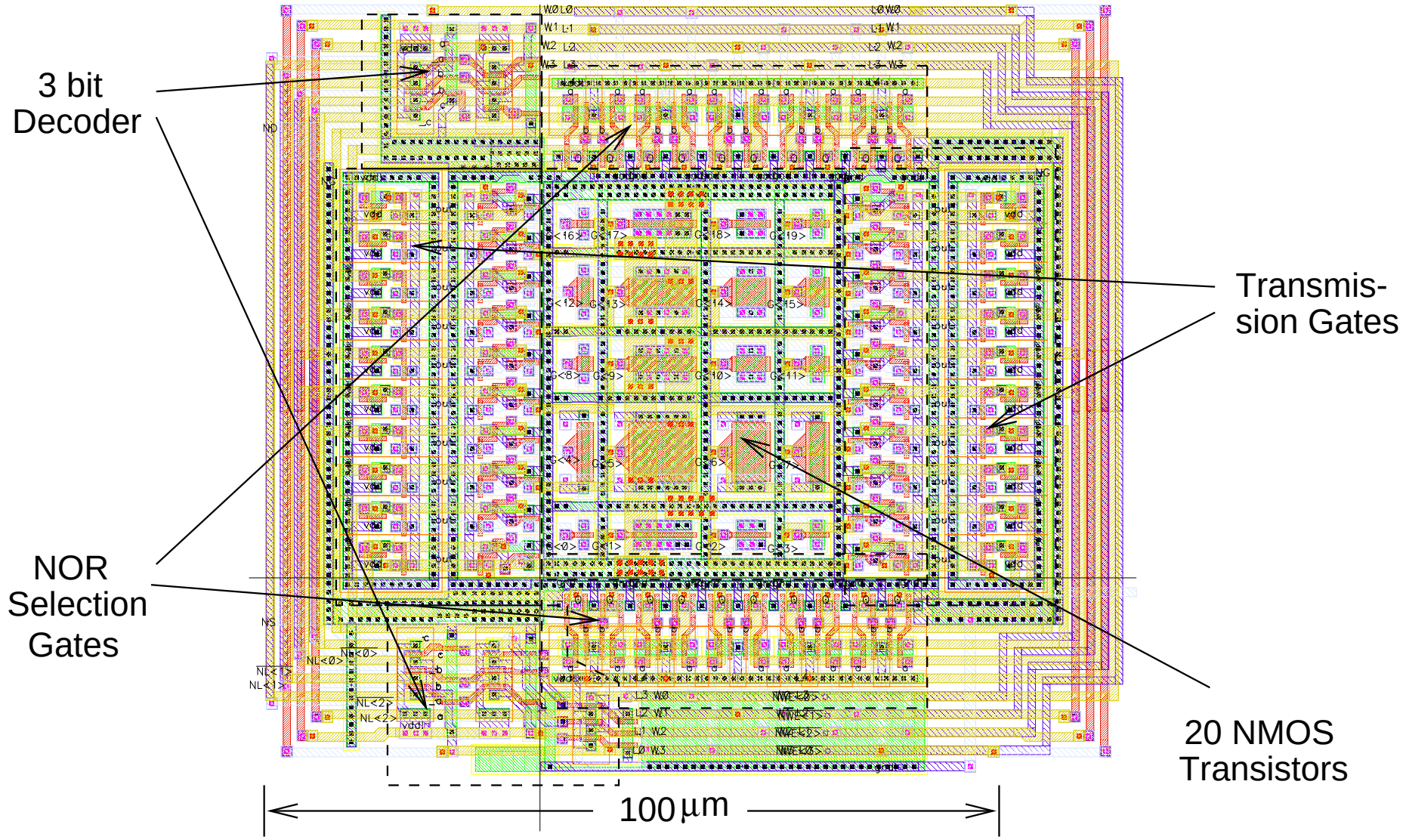
Basic PTA cell (NMOS)



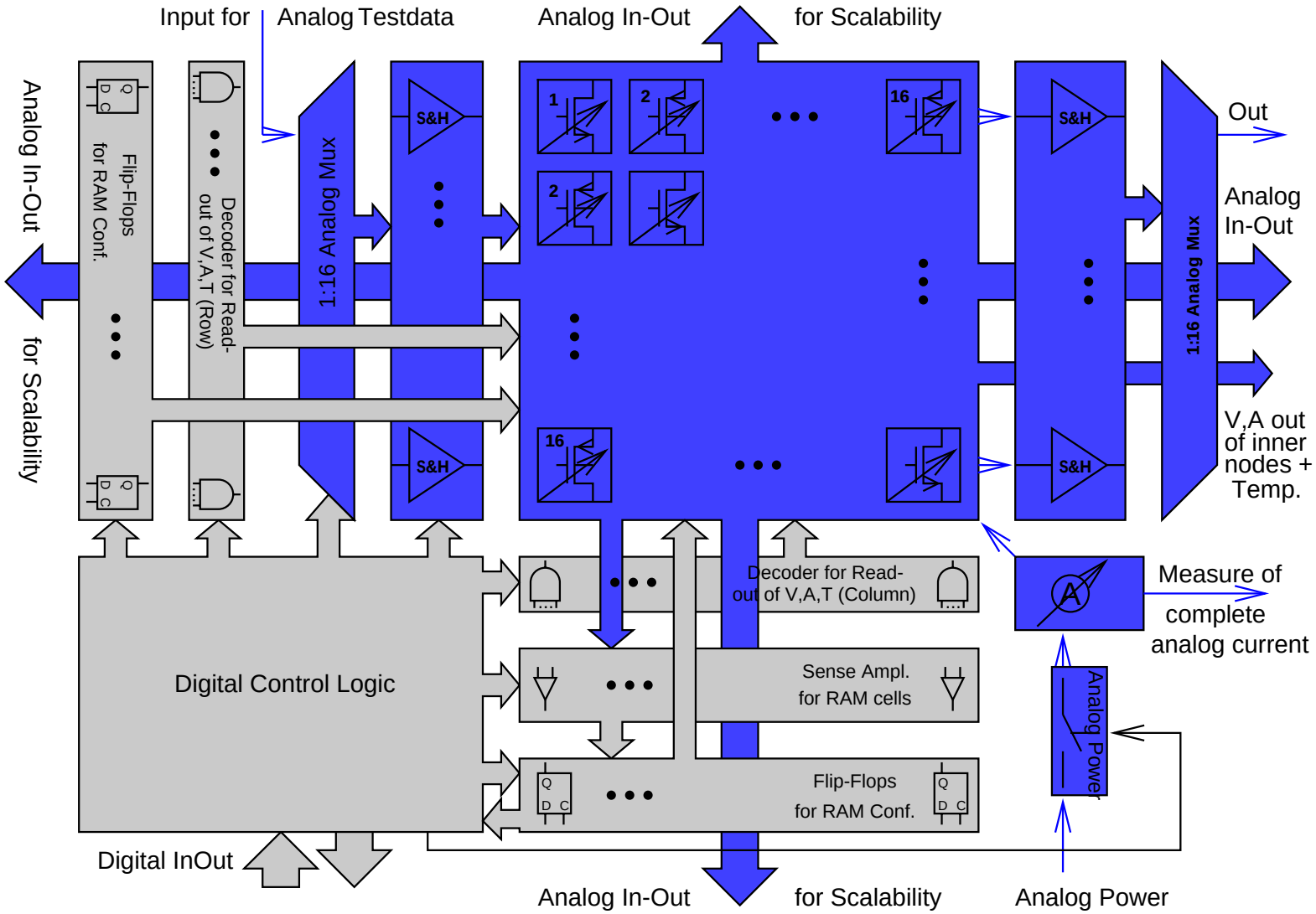
Selecting the transistor with the desired W and L



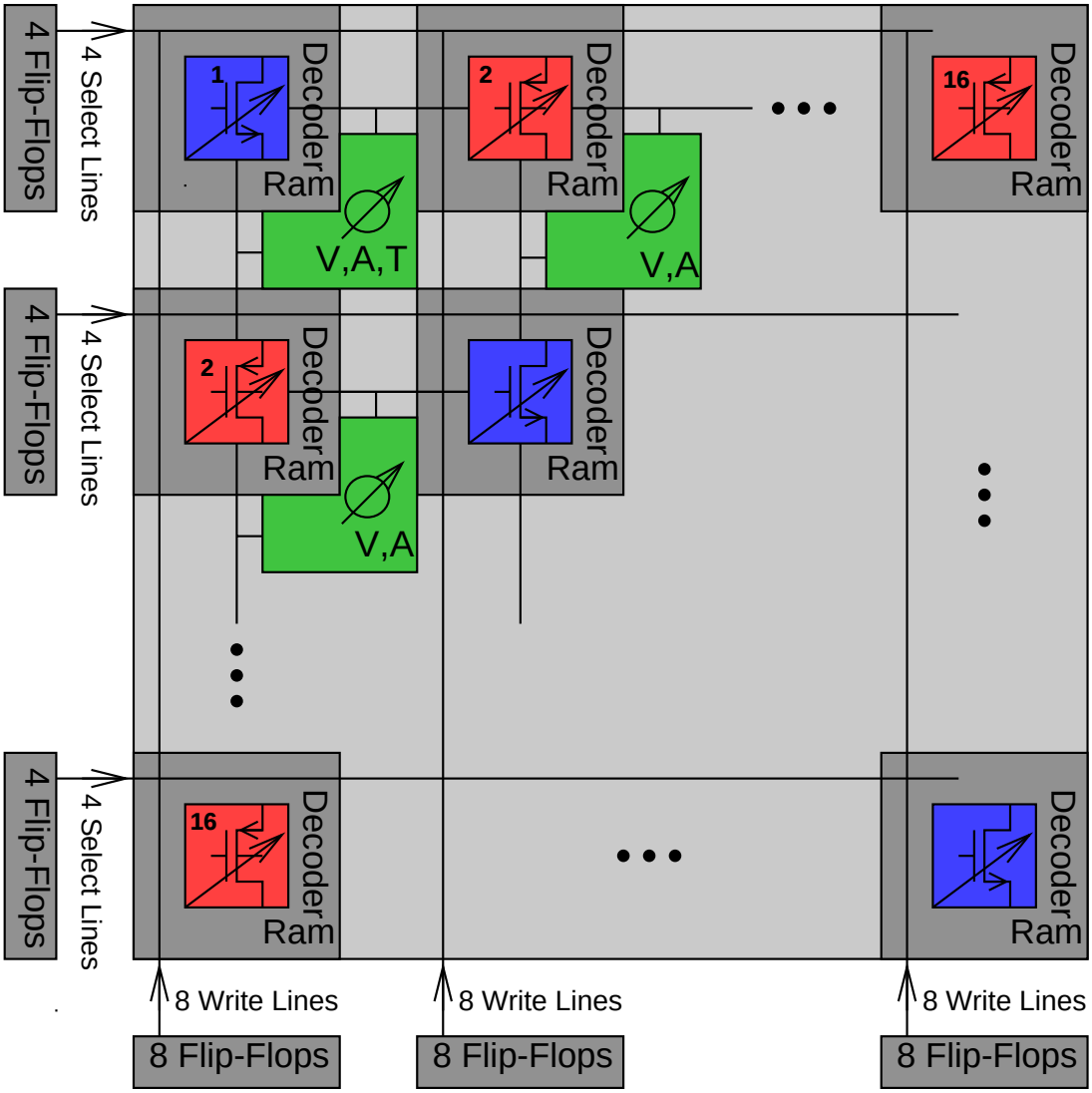
Layout of the programmable Nmos Cell (core part)



Architecture of the PTA-Chip



Array of P- und NMOS transistors



Analog Features of the PTA chip

Monitoring of

- node voltages, intercellular currents and Temperature

Avoiding self destruction

- Wide metal lines -> no electromigration
- Temperature control -> shut power off before overheating

Separate analog power for cells:

-> Low voltage electronics

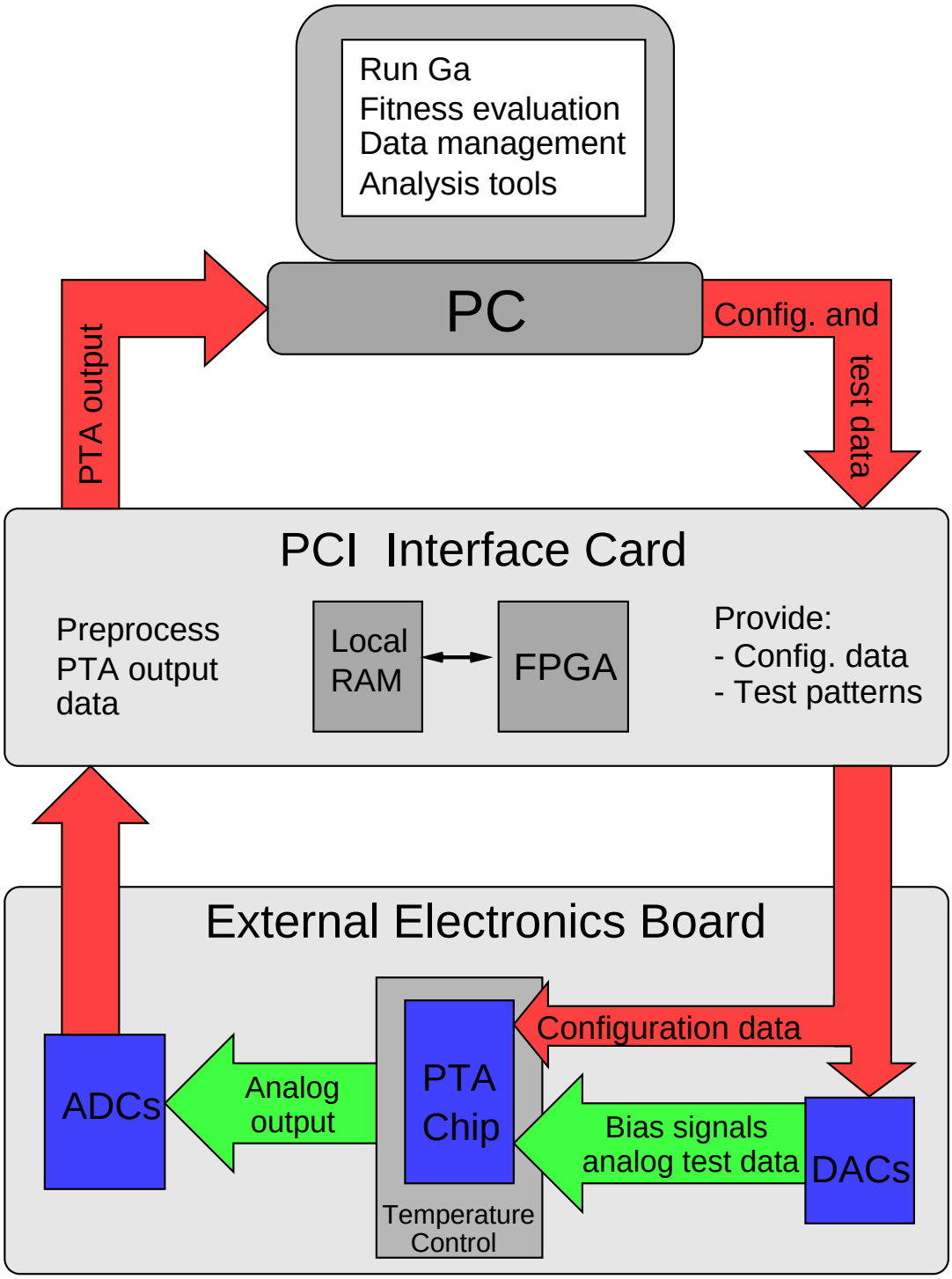
-> Power shut off to protect the chip

Scalability

- All 64 border cells are directly connected to bond pads

-> Get a bigger PTA by bonding together an array of chips

Complete System overview



Features of the System

Scalability

- Software can run on multiprocessor computer
- Use of several PCI boards possible
- One PCI board can serve more than one PTA chip

=> Parallel evolution, e.g. for parallel evolution in different environments => Robustness (c.f. Thompson, ICES 98)

Representation

- Encoding of the circuit into the genotype is known
  => Try out different representations

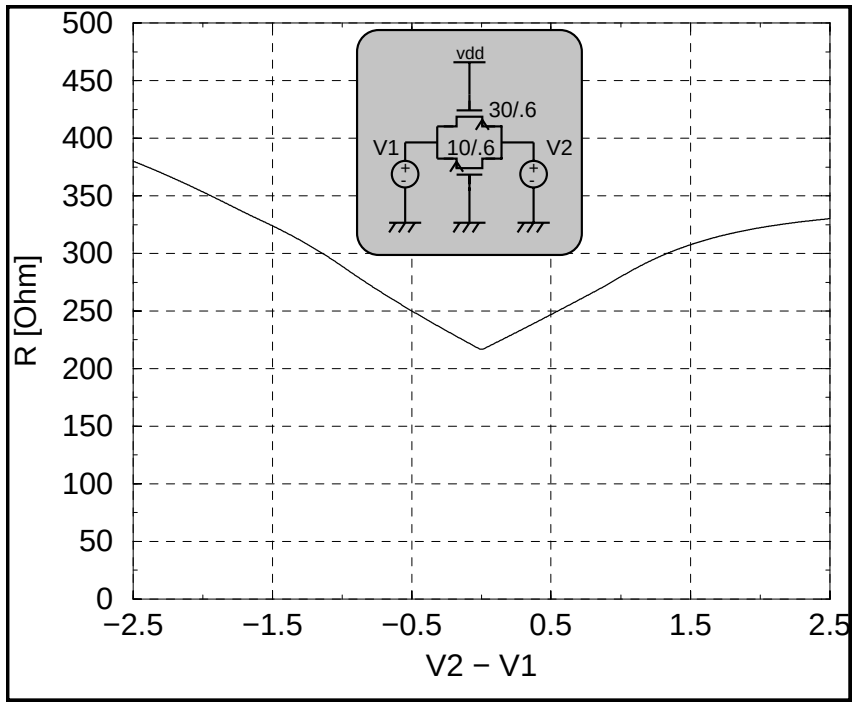
Cycle Time

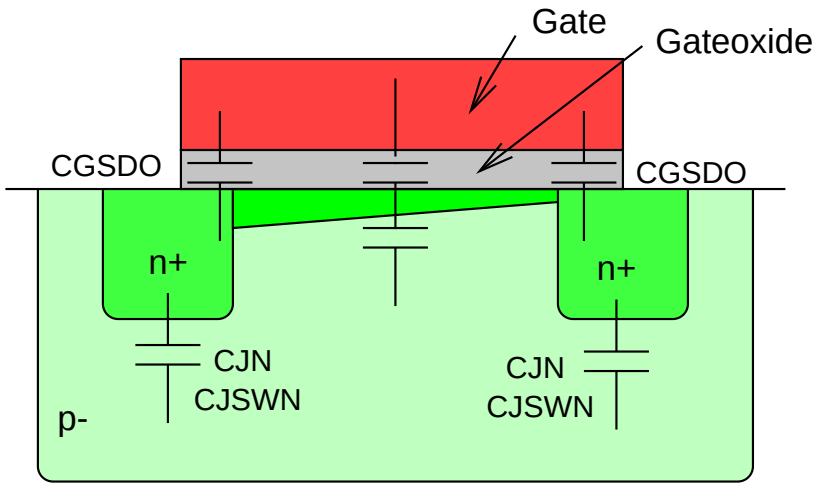
- Goal: Time for the evaluation of 1 Individuum about 10 ms
  (e.g. evaluate 1 generation of 100 indivduums per second !)

  => Time for the configuration about 100 µs

- Length of the configuration bit string: 22 x 256 = 5632 bit
  => Transfer 8bit in parallel with 7 MHz

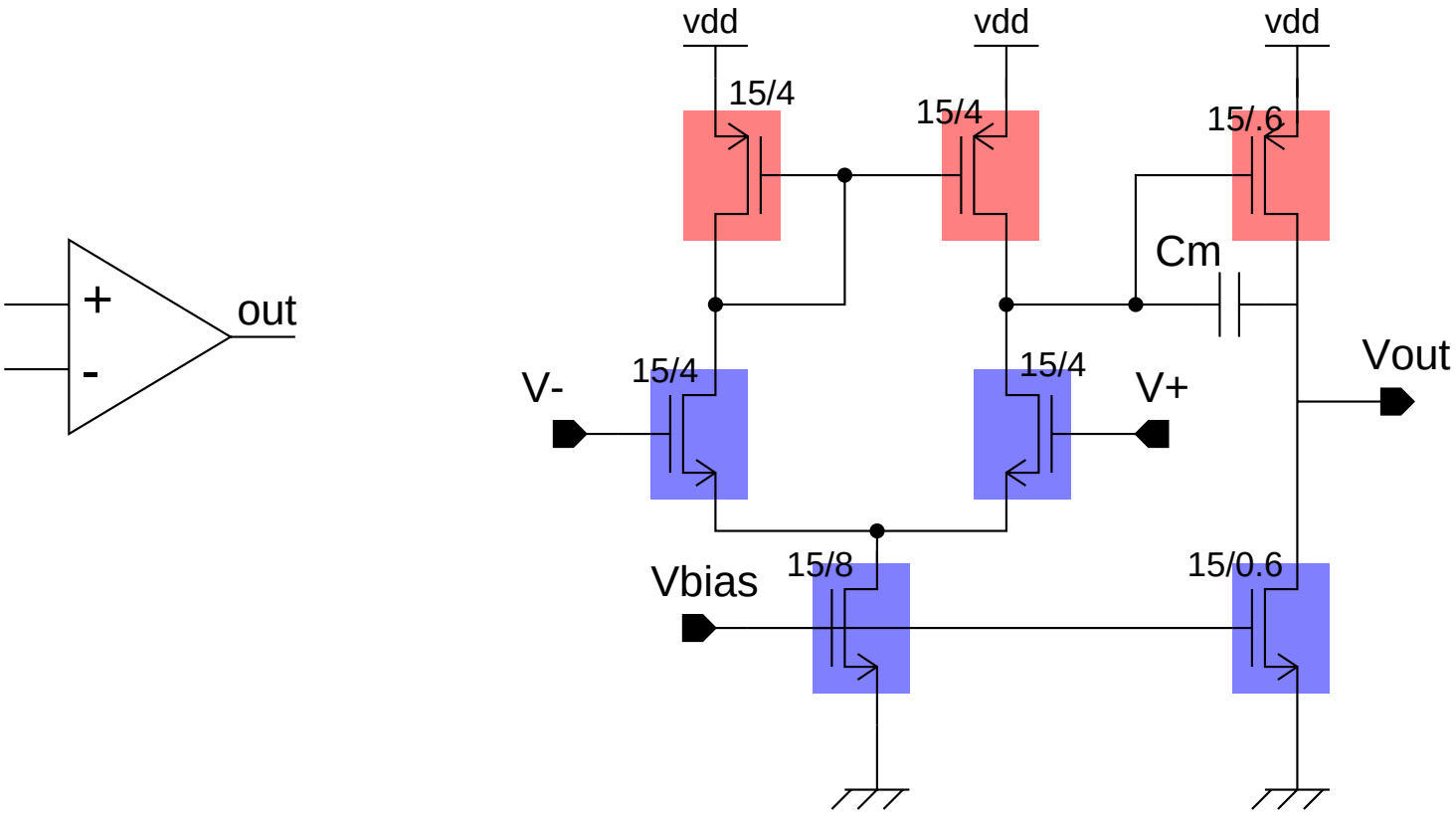
Parasitic properties of the switches





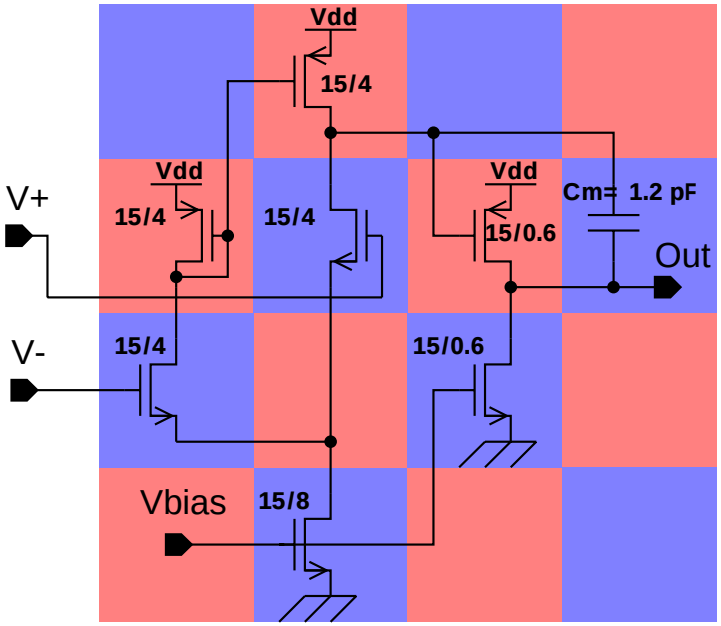
Example: Capacitance at the global Drain or Source: 300 fF
(20 Transmissiongates and 20 shut off gates)

Simple Miller operational amplifier

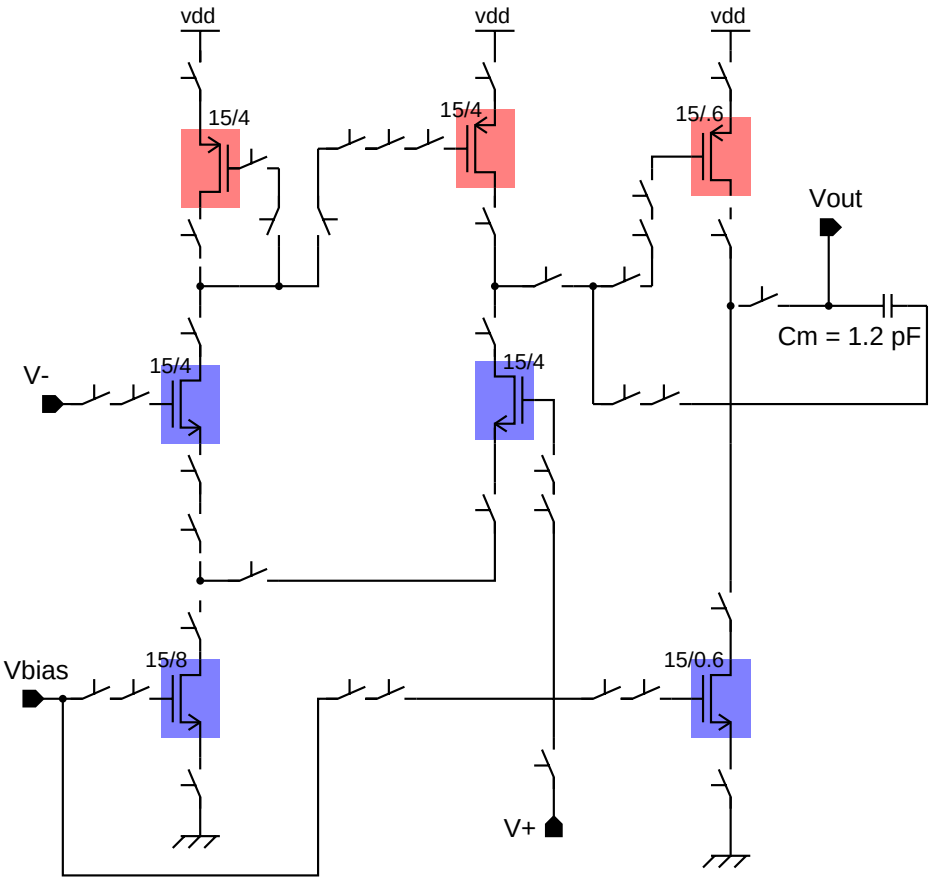


Implementation of the operational amplifier in the transistor array

’Cellop’

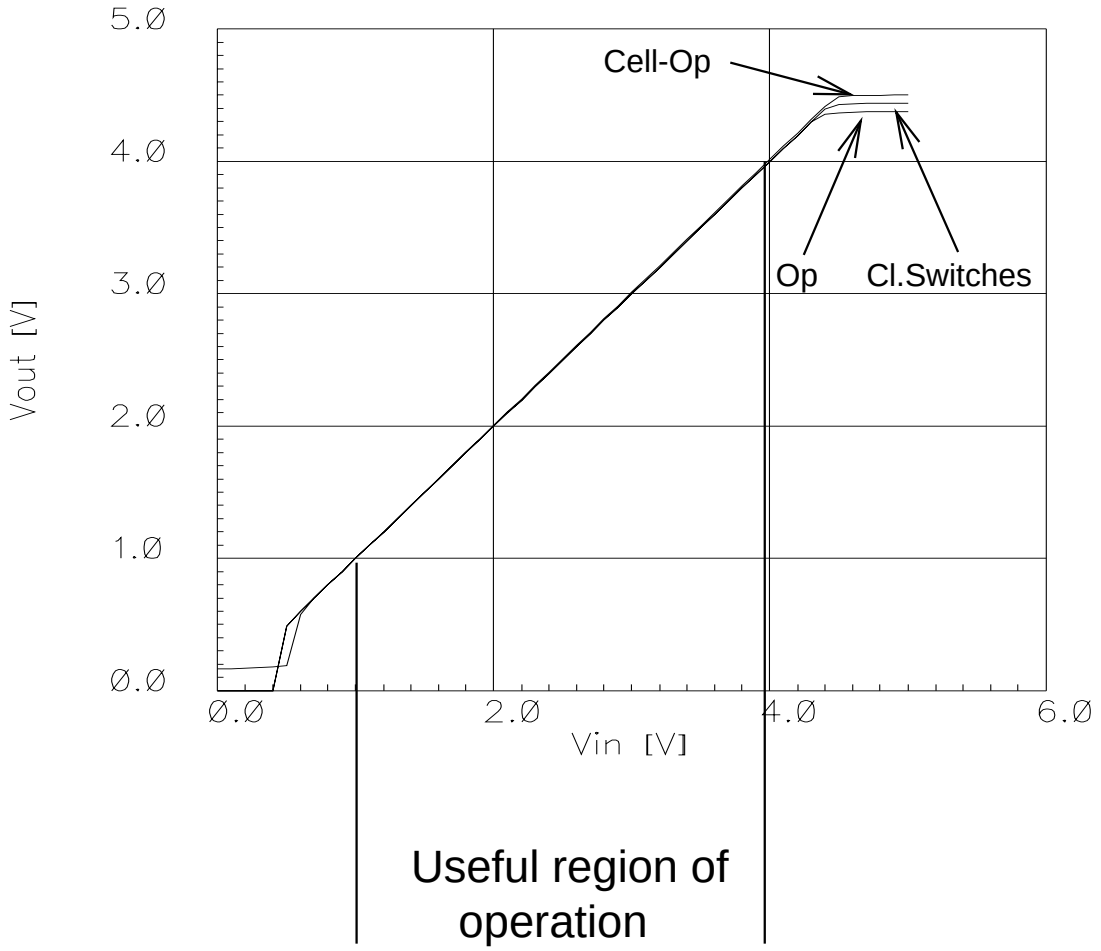


’Cl.Switches’

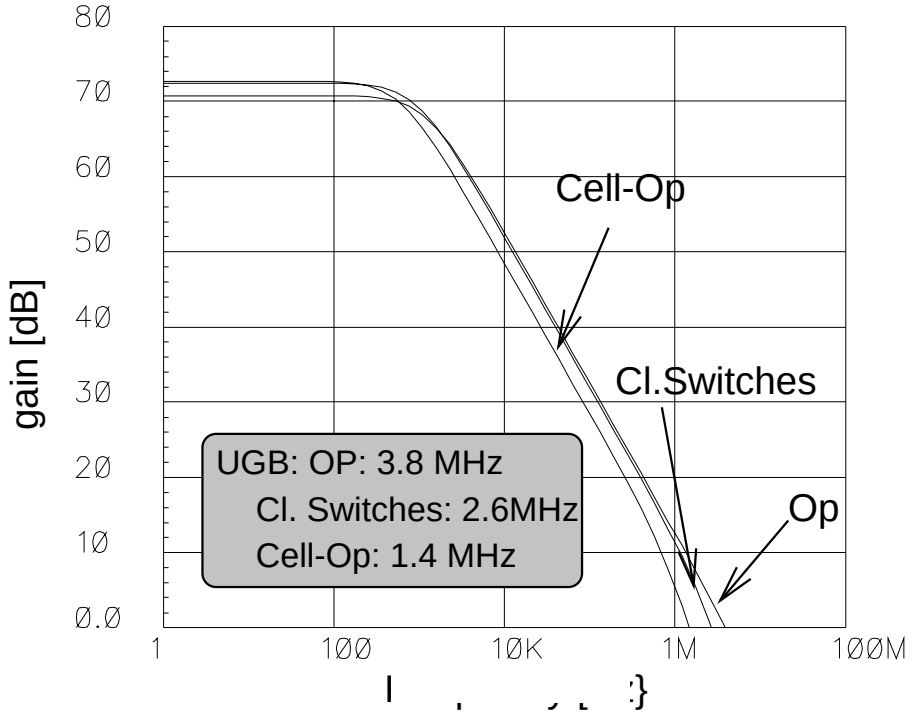


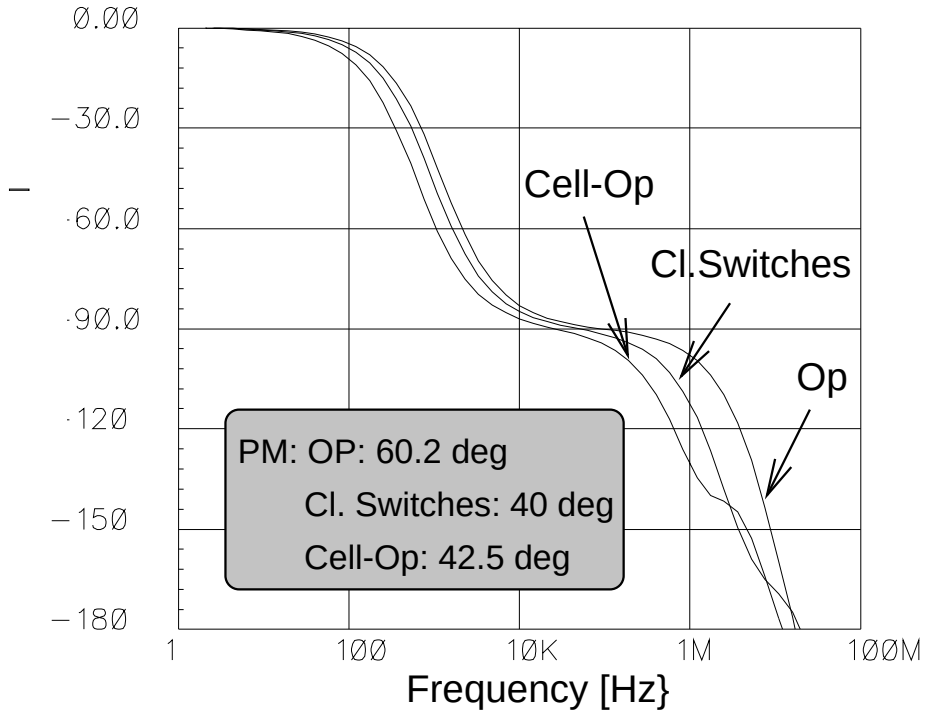
DC-Simulation of the implemented Opamp

Output of the DC Simulation



Simulation of the implemented OP: AC analysis

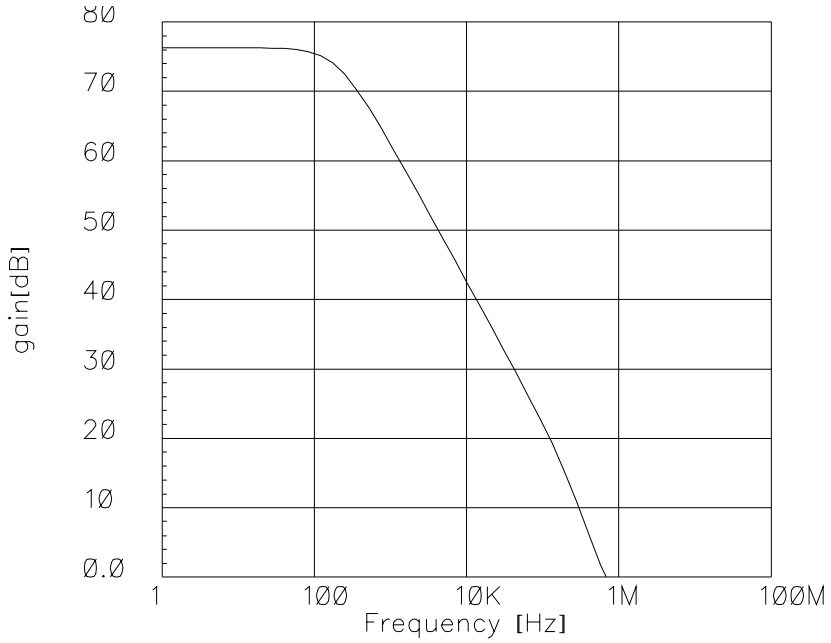


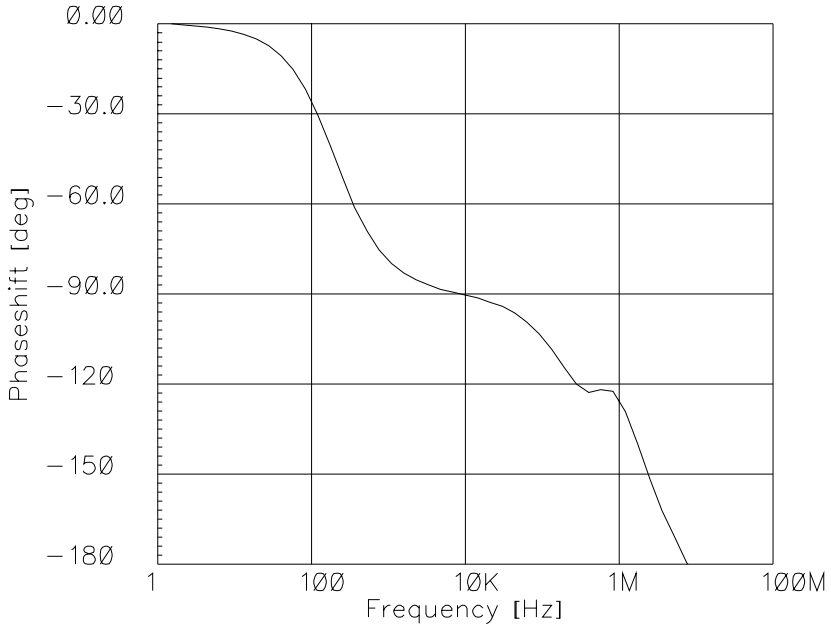


Remember: 60 deg of Phasemargin are recommended !

CellOp: AC analysis: Cm = 500 fF, ibias = 1u ...5u

For different Cm and Ibias, a Phasemargin of ...





... 58 deg is achieved at a Unity gain bandwidth of 675 kHz. Stable, but approx. 5 times slower than the plain Miller Op.

Conclusion

A new platform for hardware evolution based on an FPTA is being designed. Features are

- The PTA chip contains 256 programmable Transistors
- Chip size is approx. 25 mm^2
- Evaluation time per individuum < 10 ms
- PTA useful for Frequencies up to at least 1 MHz
- No precautions are necessary to avoid self destruction of the chip
- System is scalable => Parallel testing of individuums
- Good infrastructure for understanding the evolved circuits
- PTA chips can be produced at low cost

Future plans

- First experiments are planned for autumn 2000
- Parallel Evolution of more than one PTA chip