A 66 × 66 pixels analog edge detection array with digital readout

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Abstract

Edge detection is a common first step in artificial vision systems. Usually this task is performed by computation on digitized data from an analog CCD or CMOS camera. This paper describes an analog approach to edge detection using a kind of resistive fuse algorithm. 66 × 66 pixels are interconnected with their nearest neighbors by a novel combination of switched capacitor resistors and comparators. The chip accepts analog input up to 10 MHz and delivers digital edge data with an internal data rate of 550 Mbyte/s. The typical processing time for one frame is only 2 µs. An integrated digital sequencer with static program memory allows versatile control of the algorithm. The presented chip is especially suited for integration as an analog front end in larger systems, preferable on a single die. It eliminates the need for an analog to digital converter and its high output data rate and programmability make it possible to look at the same image under different aspects more than once.

1. Introduction

The work described in this paper was inspired by the requirements for a mobile image processing unit in a project which develops a tactile vision aid system for blind people [1]. It uses a logarithmic CMOS image sensor as camera with the capability of selectable resolution and random pixel access [2]. The camera and the image processing system should act together interactively to create a virtual image of the real world scenery. The system looks at the scenery with low resolution to aquire a coarse overall impression and to determine the motion of the camera itself. If something changes between adjacent pictures it will aquire the corresponding image data again with a higher resolution.

1.1. Concept of Resistive Fuses

The first step of the image processing is the localisation of spatially correlated changes in the gray scale image, a process abbreviated as edge detection. It is very well suited for parallel computing by processing elements placed on a two dimensional grid because the interesting spatial correlations are mostly local by nature. An algorithm using only the nearest neighbors is the resistive fuse approach. Figure 2 illustrates how it works for the one dimensional case. The voltage sources represent the image data, connected to the network nodes by ordinary resistors. Inbetween the nodes are special resistors possessing a fuse-like behaviour. Their characteristic curve is depicted in figure 1. If the voltage across them reaches $V_{compare}$, the fuse will 'blow' and interrupt the interconnection of the array pixels, stopping the smoothing process of the resistive network at its location [3]. This increases the voltage across the fuse even further, adding a hysteresis which prevents oscillations.

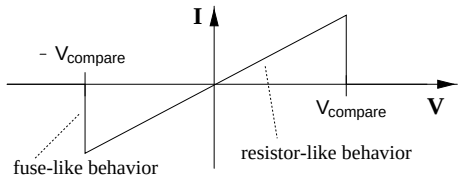

Figure 1. I/V characteristic of a resistive fuse

The resistive fuse algorithm needs a comparison between the absolute value of the difference between adjacent pixels and $V_{compare}$. Also the resistors need to be implemented. Figure 3 gives an impression of the resulting array structure. A standard approach to this are analog continuous time circuits using CMOS transistors in weak inversion mode [4]. But the device mismatch leads to substantial fixed pattern noise. Also these circuits do not deliver the edge information directly, but only the segmented gray scale image. This paper describes a novel implementation using switched capacitor (SC) resistors and clocked sense amplifiers as comparators.

2. Implementation

2.1. Resistive Fuse

Figure 4 shows the implementation of the resistive fuse circuit. Two pixels and one fuse circuit are drawn. The analog storage and the readout part are omitted for simplicity. The nodes labelled with *other cells* are connected to the three remaining neighbors of each pixel. The re-

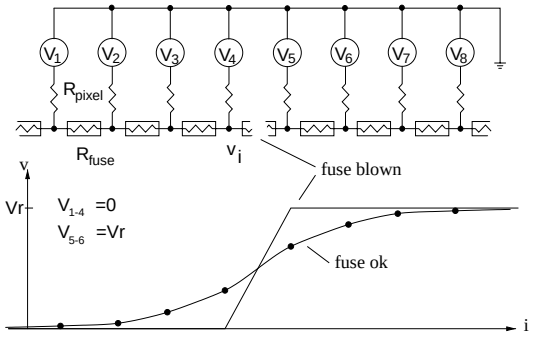

Figure 2. Principle of a resistive fuse array

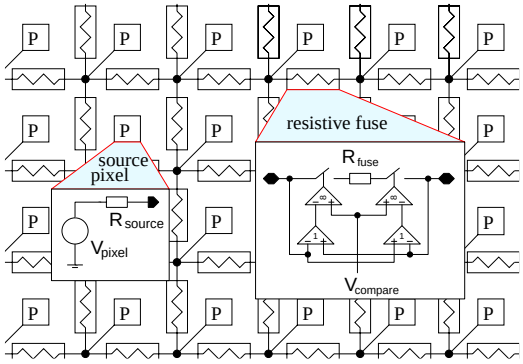

Figure 3. Two dimensional resistive fuse array

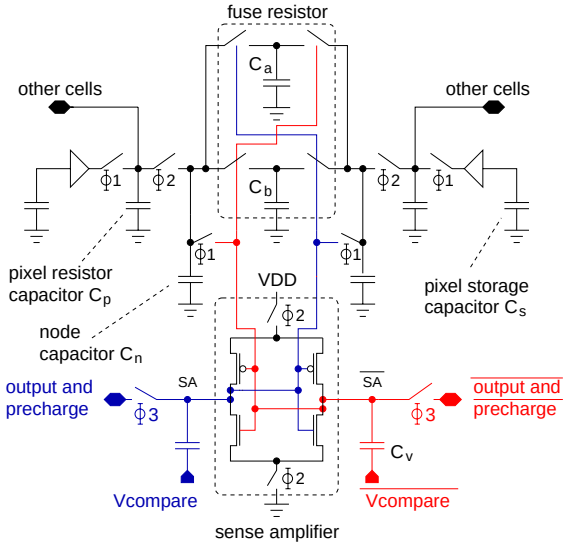

Figure 4. Operation principle of the resistive fuse circuit

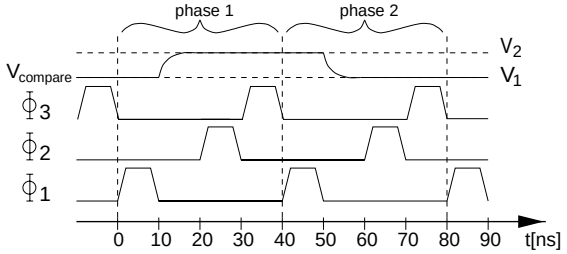

Figure 5. Clock and $V_{compare}$ timing

Table 1. Different $\Delta V'$ combinations

phase 1	phase 2	C_a phase 1/2	fuse
< 0	< 0	right/right	blown $l > r$
< 0	> 0	right/left	ok if $V_1 > V_2$
> 0	< 0	left/right	ok if $V_1 < V_2$
> 0	> 0	left/left	blown $r > l$

sistive fuse is shown in the middle, consisting of the SC resistor and the sense amplifier. The output of the pixel voltage buffer is connected to the surrounding fuses via the pixel resistor (see Figure 3), also implemented in SC technology.

Figure 5 shows the edge detection timing. Two phases of the non-overlapped Clock signals Φ_1, Φ_2 and Φ_3 are needed for one cycle. The *output* and $\overline{output}$ lines are connected to a fixed voltage source providing a precharge voltage. In clock phase Φ_3 it is used to reset the sense amplifiers. The precharge level is choosen to be approximately one transistor threshold voltage higher than the lowest node voltage. Since the fuse resistor switches are NMOS pass transistors, this ensures that no current flows after precharging the sense amplifiers. In Φ_1 the charge on the left and right node capacitors C_n (Q_l, Q_r) is distributed between the gate (and parasitic) capacitances of the sense amplifier (C_g) and the $V_{compare}$ capacitor C_v. The differential input voltage of the sense amplifier $\Delta V = V_{sa} - V_{\overline{sa}}$ becomes ($C_s = C_g + C_v$, $Q_s = C_s \cdot V_{precharge}$):

$$\Delta V = \frac{Q_r + Q_s}{C_n + C_s} - \frac{Q_l + Q_s}{C_n + C_s} = \frac{Q_r - Q_l}{C_n + C_s} \qquad (1)$$

This is independent of both the precharge voltage and any common node voltage level.

After Φ_1 $V_{compare}$ changes from V_1 to V_2 or vice versa, depending on the phase (see Figure 5). $\overline{V_{compare}}$ is the complement, changing from V_2 to V_1 in phase 1. This results in a new differential input voltage for the sense amplifier $\Delta V'$ ($\Delta V_c = |V_1 - V_2|$):

$$\Delta V' = \Delta V + 2\frac{C_v}{C_a + C_v} \cdot \begin{cases} \Delta V_c & \text{in phase 1} \\ -\Delta V_c & \text{in phase 2} \end{cases} \qquad (2)$$

In Φ_2 the sense amplifier is activated and if $\Delta V' > 0$ V_{sa} goes to VDD and $V_{\overline{sa}}$ to GROUND. This connects C_a to the left and C_b to the right node. If $\Delta V' < 0$ the output will be inverted, connecting C_a to the right and C_b to the left. Table 1 shows all four possible combinations of $\Delta V'$ and phase. If $|\Delta V|$ is larger than the right addend of equation 2, the capacitors C_a and C_b will get connected to the same side in both phases, disabling any charge transport across the fuse. In the other case $V_{compare}$ dominates the sense amplifier, making it switch to one side in phase 1 and to the other in phase 2. This leads to C_a and C_b acting like a SC resistor connecting the two nodes. The charge from the pixel capacitor C_p and the four neighboring fuse capacitors C_a or C_b is shared at the node in Φ_2. The next phase starts with the updated charge level

on C_n. Any pattern in the array spreads with a velocity of one node per cycle. Assuming only resistive behavior, its amplitude also reduces exponentially with distance. In the presented implementation the characteristic length is about 4.5 nodes with a clocking scheme as shown in Figure 5. After 10 to 20 cycles the edge detection is finished and the array output is stable.

2.2. Readout

The edge detection cycle can be modified to read out the digital edge data stored in the sense amplifiers in Φ_2. In this case an additional clock cycle is inserted before Φ_3. The precharge voltage is disconnected and only one column of the array gets the Φ_3 clock. The charge on the gates of the sense amplifiers in this column leads to a differential voltage of about 150 mV on the output lines. Two columns of sense amplifiers store this information, one in phase 1, the other in phase 2. The cycle ends with Φ_3 for all columns and enabled precharge voltage drivers. It is also possible to use a burst read out. In this case the data from phase 1 is read out for all columns before phase 2. This needs only 3 clock cycles per column instead of 5 in normal mode, but it is necessary to buffer the edge data because the data of both phases is needed to determine the existence of an edge (see Table 1).
Each pixel has also an analog readout capability. This is mainly for debugging and is implemented by a source follower connected to the node capacitor C_n. The output of every node is multiplexed to a common buffer able to drive off chip loads.

2.3. Pixel Storage

Pixel storage is done by ordinary source follower circuits, buffering the storage capacitor C_s. To compensate the offset and low gain, as well as device mismatch, the analog input is first fed to a sample and hold circuitry (S&H), storing one column of pixel data. The pixel buffer is then connected to one folded cascode input stage per row, forming together an operational amplifier with unity gain. This ensures that the output of the pixel buffer is the same as the value stored in the S&H stage.

2.4. Clock and digital control

On a transistor level, the resistive fuse circuit needs six clock signals. The readout, column driver and $V_{compare}$ circuitry requires an additional 13. 19 different non overlapped clock signals must therefore be generated and distributed across the array. To be flexible in the timing and to modifiy the algorithm (i.e. to change the characteristic length) a RAM based sequencer generates the clock signals synchronously to a main clock produced by an integrated PLL. The sequencer can handle six nested loops and has 84 words of program memory. It is also responsible for storing the analog pixel data and reading back the edge information. The clock buffers convert the synchronous clocks to non-overlapped signals with a digitally adjustable gap to compensate for delay variations in the clock distribution network. On-chip blocking capacitors are used for the array and the clock drivers (about 3 nF). Figure 6 shows a block diagram of the entire chip. For digital communication the chip uses an eight bit bidirectional bus synchronous to the external clock.

Table 2. Chip characteristics and performance summary

Technology	0.6 μm single-poly triple-metal CMOS Process
Die size	4.4×4.3 mm^2
Array cell size	57×48.5 μm^2
Supply voltage	5 V
Power	1 μJ/frame
Sequencer clock	100 MHz
Frame time	2 μs
Analog input range	0.8 to 3.2 V
Edge readout	0.55 GByte/s (internal)
Fixed pattern noise	-40.8 dB (rms)

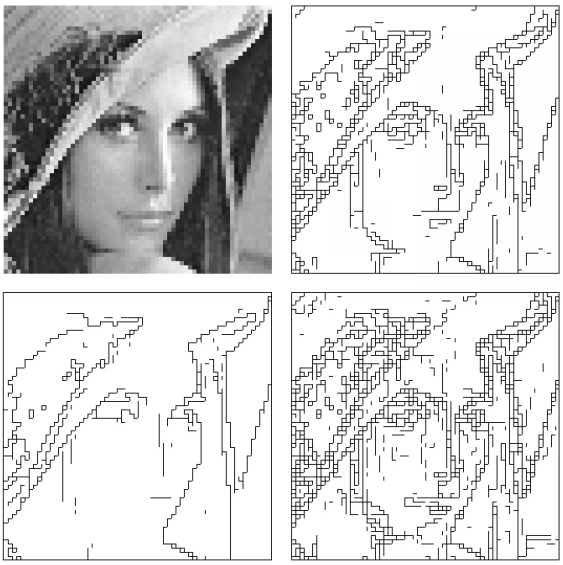

Figure 7. Example of edge detection. Different $V_{compare}$ levels are used (top: medium, bottom left: high, bottom right: low).

3. Experimental Results

Table 2 summarizes the main results. The fixed pattern noise is determined by the number of false edges detected by the chip while decreasing $V_{compare}$ towards zero with a uniform gray background. This number equals the integral of the gaussian as long as not to many fuses are blown.
Figure 7 shows an example picture and the detected edges for three different $V_{compare}$ levels.
In Figure 8 the hysteresis effect of the resistive fuses is shown for a 17×17 pixel^2 square. The level difference between the square and its surrounding is $1/8$ of the to-

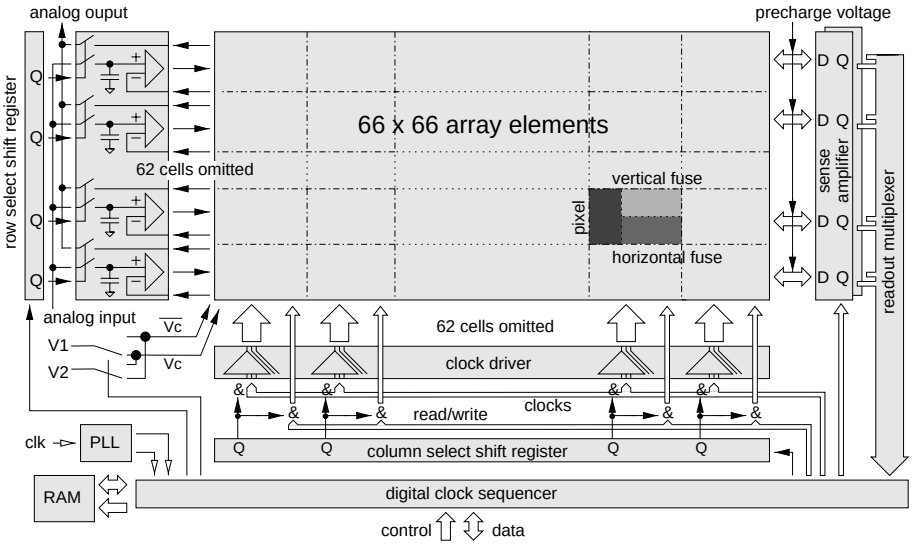

Figure 6. Block diagram of the entire chip

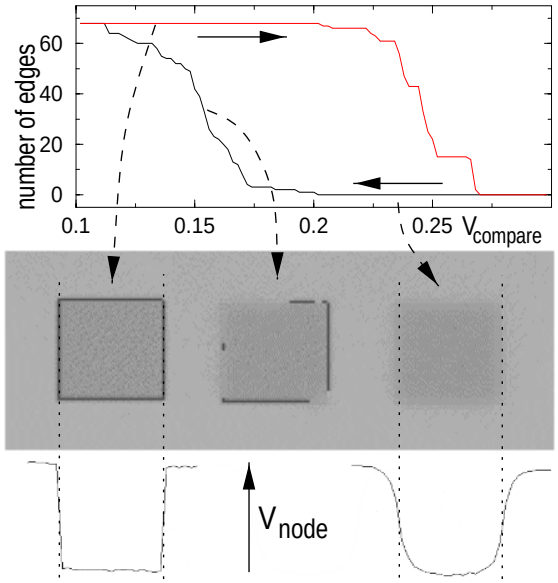

Figure 8. Top: Hysteresis curve of the resistive fuse circuit. Bottom: Node voltages versus pixel position in case of zero and total number of edges.

tal dynamic range. The detected edges are shown below for three different curve points. At the bottom the measured internal node voltages are plotted along a horizontal cutline through the middle of the squares. Corresponding points are depicted by the dotted lines.

4. Conclusion

We have developed an analog resistive fuse edge detection array with 8712 fuses. The fixed pattern noise was kept under control by using a switched capacitor technique. MOS transistors as capacitances allow an exploitation of all the benefits of smaller feature sizes. The dependency on threshold voltage variations is much less than in continuous time implementations working in/near weak inversion. Besides the compare and precharge voltages only digital clock and control signals are needed. The edge data use a very fast charge readout scheme whose parallel outputs can be directly connected to a digital post-processing unit. The presented prototype includes the digital control section to test the performance of the circuit implementation but does not yet make use of its speed. Another interesting outlook could be the combination of the array cells with CMOS photo receptors to avoid the input bottleneck. Together with the fast readout single chip pattern recognition in the μs-timescale is feasible.

5. Acknowledgement

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