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Dipl.–Phys. Wolfgang Fallot-Burghardt
aus Saarbrücken

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A CMOS Mixed-Signal Readout Chip
for the
Microstrip Detectors of HERA-*B*

Gutachter: Prof. Dr. Karl-Tasso Knöpfle

Prof. Dr. Ulrich Straumann

Innerhalb der vorliegenden Doktorarbeit wurden die wesentlichen analogen Teile des CMOS Mixed-Signal Chips HELIX128S-2 entworfen und getestet; dieser Chip dient zur Auslese von Ladungssignalen aus Siliziumstreifen- und Gas-Mikrostreifen-Detektoren, die beim Nachweis von Elementarteilchen beim HERA-B Experiment (DESY, Hamburg) zum Einsatz kommen.
HELIX128S-2 integriert 128 Verstärkerkanäle, bestehend aus einem schnellen (Anstiegszeit ca. 50 ns), rauscharmen (ENC=474 e^{-}+35 e^{-}/pF $\cdot C_{in}$) Ladungsverstärker, der die Vorverstärkung der Strom/Ladungssignale (typisch 4 fC) übernimmt; die langsam abfallenden Vorverstärkersignale werden von einem nachfolgenden Pulsformer in zeitlimitierte Pulse (Abfallzeit $\leq$ 100 ns) umgewandelt, die anschließend mit 10 MHz Abtastrate in einer Kapazitätsmatrix zwischengespeichert werden. Auf ein Level 1 Triggersignal hin, das mit 10 μs Verzögerung erfolgt, werden die Signalwerte durch einen weiteren Ladungsverstärker aus der Matrix ausgelesen, von einem 128 zu 1 Multiplexer auf eine Leitung gemultiplext und von einem schnellen Stromtreiber als Analogwerte ausgegeben (max. 40 MHz); hierbei erfolgt die Auslese der Matrixwerte totzeitfrei, d. h. ohne den Schreibvorgang zu stören. Zum schnellen Nachweis eines getroffenen Streifens generiert ein hinter dem Pulsformer angebrachter, kapazitiv gekoppelter Komparator (Schwelle gemeinsam für alle Komparatoren) ein digitales Signal, das zu vieren verodert als Open-Drain Signal zur Verfügung gestellt wird. Die Breite der Verstärkerkanäle darf wegen des Siliziumstreifenabstandes 50 μm nicht überschreiten und beträgt bei dem vorgestellten Chip 42.2 μm; die Größe des Chips beträgt 14.39 mm $\times$ 6.15 mm. Durch konsequenten Einsatz von Stromspiegeln mit konstantem Referenzstrom wird eine moderate Strahlenhärte ($\leq$ 200 krad) erreicht.
Der entwickelte Chip erfüllt die vorgegebenen Spezifikationen; neben dem HERA-B-Experiment wird er auch beim ZEUS-Experiment (DESY) eingesetzt werden.

In the context of this dissertation the major part of the analog circuitry of the CMOS mixed-signal chip HELIX128S-2 has been developed and tested; it serves for the readout of charge signals from silicon-strip and microstrip gas-chamber detectors to be installed for the detection of elementary particles at the HERA-B experiment (DESY, Hamburg).
HELIX128S-2 integrates 128 amplifier channels, consisting of a fast (rise time approx. 50 ns), low-noise (ENC=474 e^{-}+35 e^{-}/pF $\cdot C_{in}$) charge amplifier which integrates the current/charge-signals (typically 4 fC); the slowly decaying preamplifier output signals are converted by a subsequent pulse shaper into time-limited pulses (decay time $\leq$ 100 ns), which are stored at 10 MHz sucessively in a capacitor array ("pipeline"). In the event of a level one trigger which arrives with a delay of 10 μs, the signal values are read out from the pipeline by a resetable charge amplifier; this happens without introducing dead time, i. e. the write-operation is not affected. The signals from different channels are multiplexed by a 128 to 1 multiplexer onto one bus line and are put out as analog values by a fast current buffer (max. 40 MHz). Additionally, each channel is equipped with an AC-coupled comparator behind the preamplifier/shaper. All comparators share a common threshold, the output of four neighbouring comparators being ORed and brought off-chip as open drain signals. The width of an amplifier channel may not exceed 50 μm due to the silicon strip pitch and amounts to 42.2 μm; the chip's overall size is 14.39 mm $\times$ 6.15 mm. By the use of current mirrors with constant reference current a moderate radiation hardness is obtained ($\leq$ 200 krad).
The chip developed fulfills the given specifications of HERA-B; it will also be employed by the ZEUS-experiment (DESY).

Contents

Chapter 1

Introduction

Symmetries and conservation laws are important objects of physical research. For example the electromagnetic interaction is invariant w. r. t. charge conjugation[1] C or parity transformation[2] P. From the invariance of physical systems follow important physical laws like the Coulomb-law of electrical force.

The weak interaction, however, violates C-symmetry as well as P-symmetry. The combined CP-symmetry was assumed to be conserved by weak interaction, until in 1964 CP-symmetry violation was observed in the decay of neutral K^0-mesons, too [Berg92, Na89, Povh96].

The experiment HERA-B [HB94/95, Hof93, SP97] will examine CP-violation in the decay of neutral B-mesons. In this decay a unique possibility exists to verify a theoretical explanation of CP-violation which has been introduced by M. Kobayashi and T. Maskawa [KM73]. They discovered that under certain circumstances the weak interaction would automatically cause CP-violation if there were at least 6 quarks.

B-mesons will be produced with a fixed-target experiment at the HERA proton storage-ring at DESY (Deutsches Elektronensynchrotron), Hamburg. When the high-energetic protons collide with the fixed target, neutral B-mesons are created by strong interaction, which decay (with small probability) according to

$$B^0 \to J/\Psi\, K_s^0 \to l^+ l^- \pi^+ \pi^- \qquad \overline{B^0} \to J/\Psi\, K_s^0 \to l^+ l^- \pi^+ \pi^-$$

which is reffered to as the "golden channel". If CP-symmetry was violated, B^0 and $\overline{B^0}$ would decay into the CP-eigenstate $J/\Psi\, K_s^0$ with different probabilities (rates). The distinction between a B^0- and a $\overline{B^0}$-decay is achieved by "flavour tagging": because a b-quark is always created together with a $\overline{b}$-quark, there exists a second B-meson carrying the complementary flavour of the B^0- resp. $\overline{B^0}$-meson under investigation. Since b-quark and $\overline{b}$-quark carry different electrical charge, it is possible to conclude the quark-flavour from the charge of the second B-meson's decay products.

The major challenge of the experiment is the discovery of the above described decay in a large background of competing events; at the HERA proton-energy of 830 GeV B^0-mesons are produced in only one out of $1.3 \cdot 10^6$ collisions. Furthermore, the "gold-plated"

[1] a particle is substituted by its anti-particle
[2] space reflection

decay occurs only for one out of 2.3·10^4 created B^0-mesons. The detector contributes according to estimations another factor of 10 due to unavoidable insufficiencies.

Considering all factors approx. 3·10^{11} collisions have to be examined in order to identify one B^0-decay into the golden channel; to make a quantitative statement about the intensity of CP-volation approx. 7000 $B^0/\overline{B^0}$-decays must be collected, which leads to a collision rate of 30 MHz (at one year of data taking). This implies that – since the frequency of proton bunches is 10 MHz – at average 3-4 collisions have to take place per bunch crossing. It becomes evident that the construction of the particle detector and the trigger is an ambitious undertaking.

1.1 HERA-B Detector

The HERA-B detector [HB94/95] (fig. 1.1) is a magnetic spectrometer; its main tasks are the identification of the particles created in the collision, a measurement of their momentum (for this a precise particle track measurement is essential), their energy and the determination of their point of nascence.

The $B^0/\overline{B^0}$ mesons are produced by collision of a proton beam at a fixed target consisting of aluminium resp. copper ribbons which are located such that protons of the beam-halo (i. e. from the outer, less populated beam region) interact at 40 MHz rate. After generation in the ribbons, B-mesons move approx. 9 mm, before they decay. The decay vertex resolution required to study CP-violation is typically 10% of this value. The *silicon vertex detector (SVD)* [Knö95] which is located directly behind the target, has to find these displaced (w. r. t. the ribbons) B-decay vertices. The SVD will be discussed in further detail in section 1.2.

A central component of the HERA-B detector is the *dipole magnet* which creates a magnetic field behind the SVD approx. 4.5 m apart from the target. Due to the (momentum-dependent) Lorentz-force tracks of charged particles are bent which enables measurement of the particles' momentum. A particular challenge is the shielding of the electron beam which also traverses the magnet field. The electrical field may not exceed a few hundred Gauss inside the electron beam pipe. The problem is overcome by use of highly permeable steel as passive shielding and an active shielding of magnetic coils counteracting the dipole field.

The *inner tracker detector* [Schm97] measures particle tracks near the proton beam pipe; it covers an angle from 10 mrad up to 20-25 cm distance from the beam pipe and is located along the beam axis from behind the SVD to approx. 13 m behind the target. It is made of microstrip gas chambers (MSGCs) (chapt. 3) which are positioned in ten super layers each consisting of two to eight layers of chambers with angles of $0°$ and $\pm 5°$ w. r. t. the vertical. The four chambers of a layer (one in each quadrant) overlap for better efficiency and for better relative alignment. The inner tracker detector has a total of approx. 135 000 channels to be read out, and - since it has to deliver fast information on hit channels for the level 1 trigger - approx. 18400 trigger output signals.

The *outer tracker detector* [Kap96] covers the larger angles starting from the outer edge of the inner tracker up to 200 mrad from the beam axis. Proportional drift chambers (see chapt. 3) with circular or hexagonal cross section and a mixture based on CF_4 as fill gas will be taken for particle detection. The minimum diameter has been chosen to be 5 mm due to the danger of high voltage flash-over and due to the resolution distortion near the anode wire. The wire positioning should be precise to approx. 100 μm in order not to deteriorate the intrinsic resolution of the chambers. The total number of channels will be 96000.

The *ring image Čerenkov detector (RICH)* [Kriz98] uses the Čerenkov-effect: elementary particles emit visible or UV-photons when traveling a medium with a velocity higher than that of light. The radiatior gas chosen is C_4F_{10}. The aperture of the light cone depends on the particle velocity and can be used together with a measurement of the particle's momentum or energy for determination of the particle's mass and hence for identification; at HERA-B it is mainly used for the identification of kaons. By proper design of a spherical mirror the cones are projected as rings onto a photon detection plane. The single photon detection is achieved by an array of multi-anode photomultipliers (quantum efficiency max. 20 %); the Hamamatsu H6568 photomultiplier under investigation has a bialkali photocathode with the anode divided into 16 pads of 4 mm $\times$ 4 mm each. The 12-stage, metal-foil dynode system allows for good single photoelectron resolution. The total number of channels will be in the order of 40000.

The *electromagnetic calorimeter (ECAL)* [Gol95] which is located 13.25 m from the target serves for the energy measurement of photons in the range of 5 to 200 GeV and for the separation of hadronic particles from leptons; the ECAL contributes to the level 1 trigger. A shashlik-calorimeter with tungsten resp. lead absorber plates alternating with scintillator plates has been chosen; the position resolution is between 1.1 mm close to the beam axis and 10 mm at larger angles. Photons are absorbed inside the alternating structure giving rise to showers of electrons, positrons and secondary photons. The energy delivered to the scintillating layers is transfered to visible light and amplified using photmultipliers or photo-diodes. A total of 6500 channels has to be read out from the ECAL.

A *transition radiation detector (TRD)* [Sav96] enables further meson/hadron-lepton separation (in particular pions shall be separated from electrons). When traversing an interface of materials of different refractive indices, elementary particles emit transition radiation in the soft x-ray region; the energy distribution depends on the particle type. In the TRD the transitions are achieved by alternating radiator/chamber-layers (36 layers in total). The photons are created when the particle exits the radiator and are detected by the proportional chambers. For the radiators polyethylene-foam resp. fibres are under investigation; the proportional chambers are filled with a gas mixture based on krypton. A total of 77000 channels has to be read out.

The *muon-chambers* [Zai98] are located at the end of the HERA-B-detector and serve for the identification of muons to be used in the level 1 trigger decision. Prior to the muon-chambers an absorber made of iron and concrete filters all particles beside muons created in the target-collision. Similar to the tracker detectors the muon-chambers consist of four super-layers, the first two with $0°$ and $\pm15°$-orientation to the vertical, the last with only $0°$ orientation. The muon-chamber-layers are composed of gas-pixel-detectors (10 mm $\times$ 10 mm) in the central region and multiwire proportional chambers resp. proportional chambers with cathode-pad readout in the outer region. The fill gas to be used is a mixture based on argon. A total of 29500 channels must be read out.

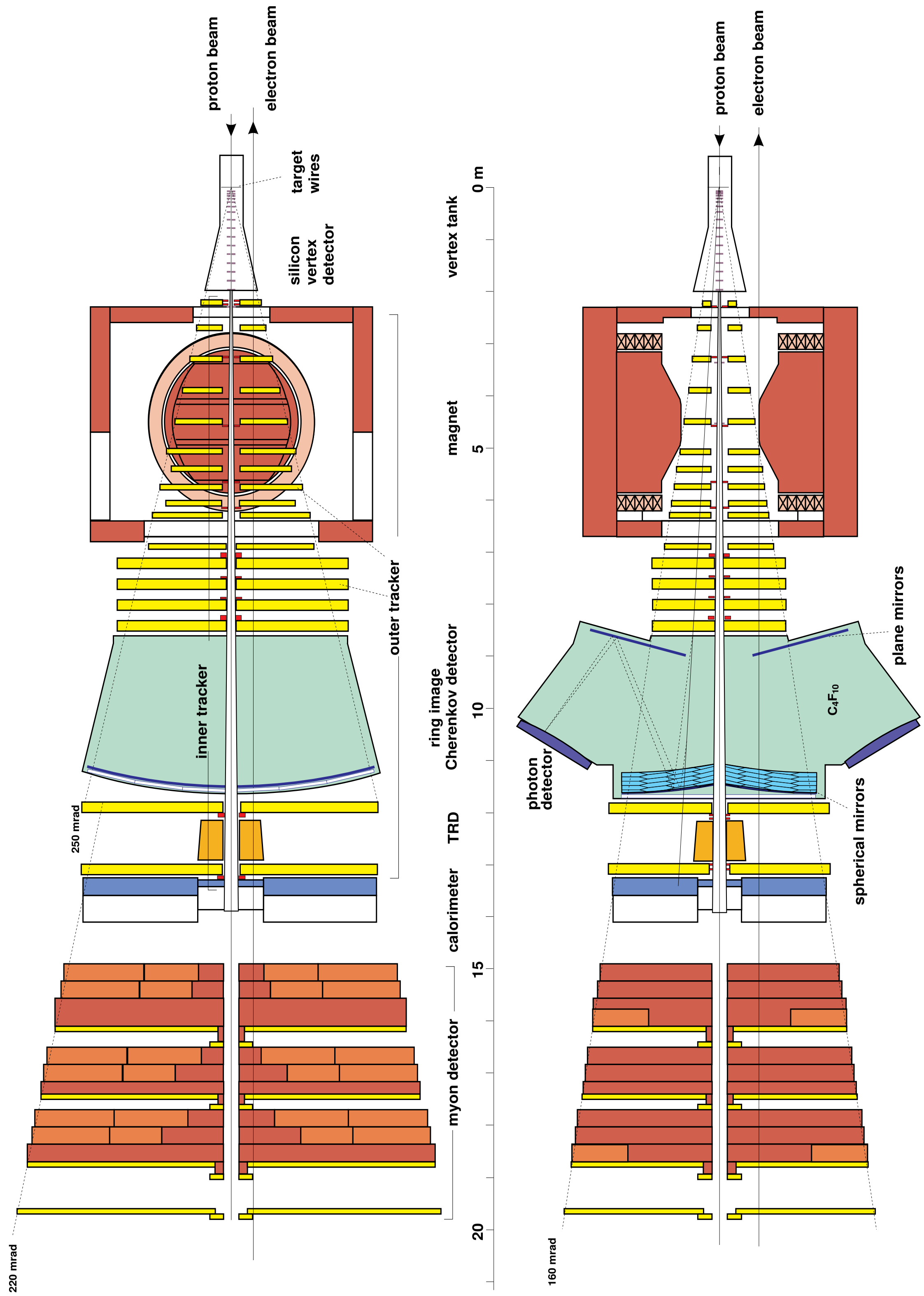


Figure 1.1: HERA-B detector [HB94/95]

1.2 Silicon Vertex Detector (SVD)

The silicon vertex detector (SVD) [Knö95] being one of the subdetectors of HERA-B supplied with the HELIX128S-2-readout chip shall be discussed in greater detail. It is the SVD's task to find the displaced B-meson decay vertices with a resolution of 500 μm in z (beam)-direction and 25 μm in transversal direction. The SVD comprises a total of 165000 channels. The following treatment has been taken from [Knö95].

1.2.1 Geometrical Layout

The ultimate limit of resolution of any vertex detector system is given by multiple scattering in the material between track vertex and the first point of the track measurement (i. e. not by the detector granularity itself !). Since the particles are created inside an evacuated beam pipe, the particles' path when traversing the pipe has to be minimized. As solution to this problem a "roman pot" [Rom1] configuration has been chosen where the beam pipe is folded around the detector planes (Fig. 1.2a)).

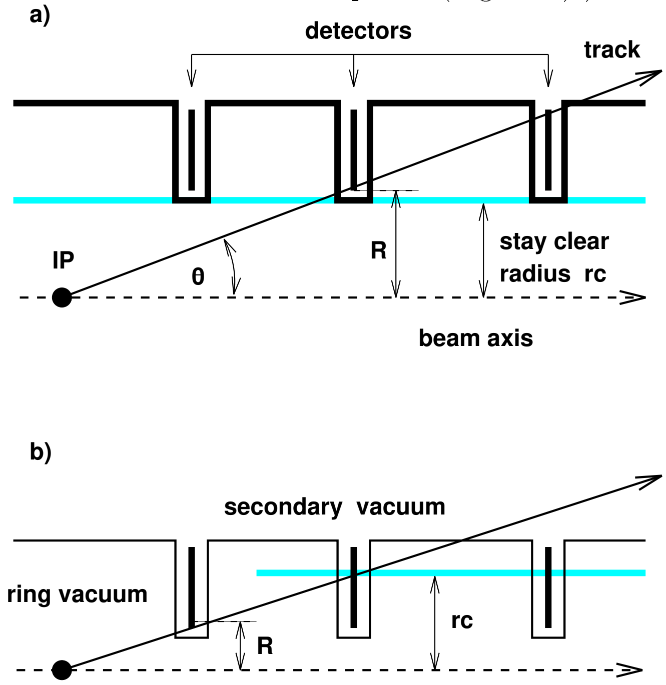


Figure 1.2: a) Schematic layout of a forward vertex detector based on a roman pot system, i.e. a 'folded' beam pipe; b) A mobile roman pot system can be moved closer to the beam during data taking [Knö95].

Now, the particles hit the "pipe" almost perpendiculary so that the effective thickness of the wall material is minimized. Further reduction of the multiple scattering has been achieved by placing the detectors in a secondary vacuum so that the windows of the pot system could be chosen as thin as 100μm.

Fig. 1.3 shows the vertex detector to comprise 7 superlayers positioned between the wire targets (z = -55 mm and 0 mm) and the dipole magnet at z = 2.3 m. Its angular coverage is consistent with the overall HERA-B-detector's acceptance from 10 mrad polar angle

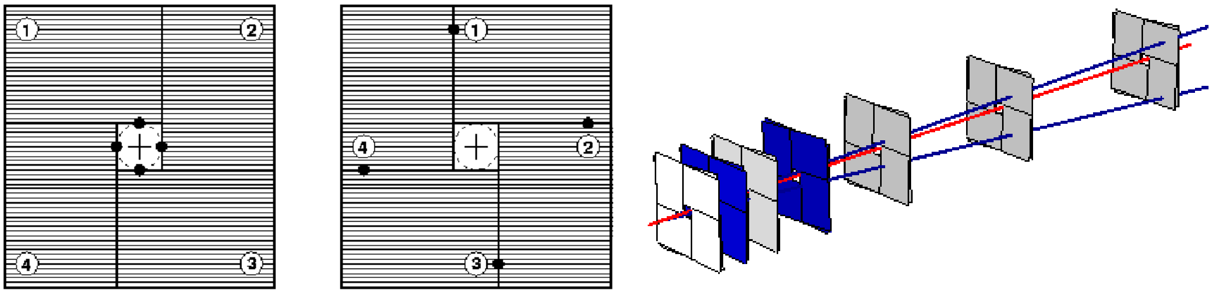


Figure 1.3: Left: alternative detector arrangements to reduce radiation damage to innermost detector regions; right: schematic 3-d plot of the SVD's 7 superlayers [Knö95]

(to the beam axis) to about 200 mrad corresponding to 90% of 4π in the center of mass system.

The individual detector planes of a superlayer (fig. 1.4) consist out of two double-sided detector elements which provide four views, $\pm 2.5^\circ$ and $90^\circ \pm 2.5^\circ$. Each detector element has a sensitive area of 50×70 mm^2 so that it can be cut from a 4" wafer. The segmentation into quadrants allows the choice of two different detector arrangements which will be exploited to stagger the support posts of subsequent superlayers, and to rotate detector positions in order to distribute the radiation load over a larger detector area (fig. 1.3). During fills these elements will be retracted to safe positions as shown in fig. 1.4

1.2.2 Radiation Damage

The radiation environment at HERA-B is described by a flux of particles which is, at a fixed perpendicular distance R to the beam axis, approximately independent of polar angle, and which falls off with $1/R^2$. The innermost edges of the silicon detectors will be exposed to a fluence of typically $3 \cdot 10^{14}$ particles, mostly relativistic pions, per 10^7 seconds year. So far, no silicon vertex detector has ever been operated up to such a fluence, but intense research on radiation damage carried out by [Riech96] and in the context of LHC and SSC projects is indicating that silicon microstrip detectors of appropriate design can indeed tolerate such a fluence. The limiting factor is primarily not the increase of leakage current since the shot noise contribution is optimized by adequate signal filtering, but rather the change of effective doping concentration far beyond type inversion. Due to the permanent creation of acceptor-like defects, the bias voltage required for full depletion of a a 280μ thick silicon strip detector will be by far more than 200 V which is currently considered to be the limit for safe operation of these devices. Possible solutions to this problem include the use of thinner detectors (depletion voltages scale with the square of detector thickness), the implementation of novel guard ring structures, appropriate cooling of detectors to $\leq 10^\circ$C in order to take advantage of beneficial annealing while avoiding the detrimental reverse annealing effects, as well as

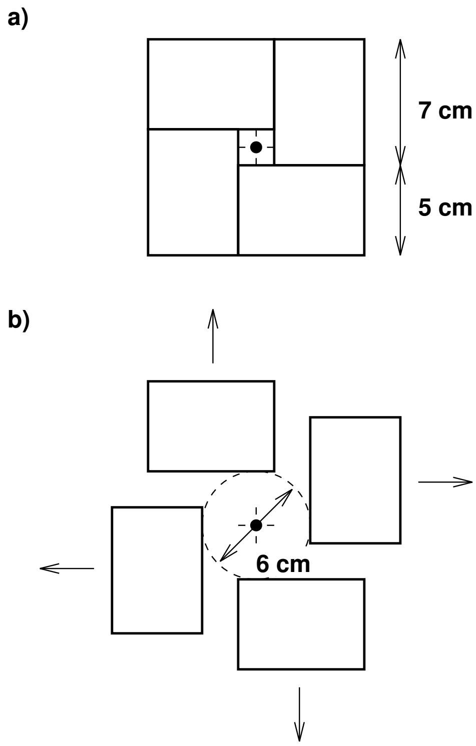


Figure 1.4: Arrangement of the 4 detector elements in a sublayer of the SVD: a) wafer positions at run time, b) wafers withdrawn during the beam filling process; arrows point towards readout chips and mounting structures. - The alternative detector arrangement w.r.t. a) is obtained by a 5 cm clockwise shift of wafers in horizontal respective vertical directions (see fig. 1.3)[Knö95].

rotation of detector positions at HERA-B to distribute the radiation load over a larger detector area.

1.2.3 Electronic Readout

Efficient processing of the vertex detector's 165 000 channel's has to rely on custom-made VLSI readout chips. Chip size and readout pitch must be compatible with the 50 μm readout pitch of silicon strip detectors (chapt. 2).

The basic functionality of the targeted chip can be summarized as follows: The charge generated by elementary particles inside silicon strip detectors must be amplified and successively stored in a ring buffer; in event of a (delayed) level one trigger the signal value associated to the trigger must be retrieved from the ring buffer and be transferred to the optical link. As a surplus the chip would also be suitable for the readout of microstrip gas chambers (chapt. 3).

The major specifications for the chip performance are constrained by [HB94/95]

- the expected signal charge of 5900 electrons per channel (worst case)
- the bunch crossing frequency of 10 MHz
- the level one trigger latency of $\approx$ 10 μs

- the level one trigger frequency of ≈ 100 kHz (this indicates 25 ns readout time per channel, if 256 channels have to be transferred in the given time window accounting for the statistical occurrence of the trigger)
- the anticipated effects from the radiation damage to the silicon detectors

The requirements on the HERA-B vertex detector readout closely ressemble those of the future ATLAS [ATL94] and CMS [CMS94] tracking detectors (both at CERN, Geneva). The development of the HELIX128S-2-frontend chip [Fal95-1, Fal95-2, Fal96, Fal97-2, Feu96, Tru97] (AMS 0.8 μm-process [AMS95-2]) could therefore profit largely from the architecture developed by the CERN-research group "RD20" [RD20-1, RD20-2, RD20-3, RD20-4].

128 detector channels are handled by one HELIX128S-2-frontend chip. The channel architecture consists of a low noise charge-amplifier with subsequent shaper of approx. 50 ns peaking time the output of which is sampled at 10 MHz and stored in a 128 cell deep analog pipeline to await the level one trigger-decision. In the event of a level one trigger, the appropriate analog samples of 128 detector channels are multiplexed to one serial output line. Occuring concurrently with data sampling, readout is practically dead-timeless.

The time-multiplexed output signals of the frontend chips will be transmitted via optical analog fiber links to the counting room where subdetector specific readout boards will represent the interface to the detector wide data acquisition system. With regard to the vertex detector system, the minimum functionality of these readout boards comprises digitization and adequate buffering of the data received. Further desirable features include pedestal subtraction, common baseline shift correction, cluster finding and sparsification, as well as data formatting.

1.2.4 Mechanics and Engineering

The principal engineering problem encountered at HERA-B was to design a mechanical system that would take into account the various, sometimes rather contradictory requirements: retractable detector arrangement, invariant alignment of detectors over extended distance - within subgroups at least, low-mass support structure within the geometrical acceptance, and negligible impact on HERA's proton ring vacuum.

The detector system including the target wire assemblies are contained in a vacuum vessel (fig. 1.5) with an exit window and an integrated tapering beam pipe for the rest of the HERA-B experiment at one end and a connection to the standard beam line system at the other. The overall length of the vessel is about 2.5 m and its maximum radius is 58 cm. The exit window is kept as thin as possible, i.e. about 3 mm if fabricated of aluminium. The silicon wafers are maintained at a secondary vacuum of 10^{-6} mbar and the main stainless steel vessel at 10^{-8} mbar. The complete system is mounted on a vibration dampened platform, and the thermal and humidity environment has to be stabilized.

Each quadrant of a superlayer is contained in a removable pot assembly that can be displaced individually in lateral direction to the beam by an external motorized mobile bearing unit. The wafers of the three superlayers next to the target wires are contained in a single pot. The 125μm thick aluminium shielding caps separate secondary and primary

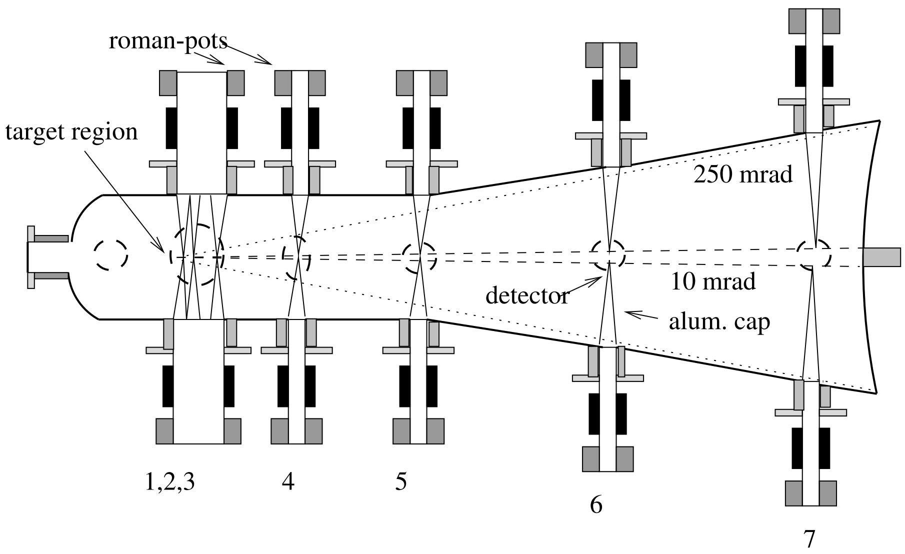


Figure 1.5: Silicon vertex detector tank [Knö95]

vacumm and serve as protection against rf interference from the beam. Detectors and readout chips are cooled via separate cooling paths connected to cooling blocks located outside the acceptance cone. Desirable heat drain materials are characterized by a maximum product of radiation length and thermal conductivity.

1.2.5 Alignment

While the final detector positions will be established by software alignment using the actual tracks from the proton-wire collisions, sufficiently fast convergence of this procedure is only guaranteed if the relative locations of the detector wafers are know with adequate accuracy even after the periodic repositioning cycles. A novel long distance laser alignment system has been chosen to accomplish this task [BKW95]. The positions of pots along each quadrant row will be continously monitored by using collimated laser beams as alignment references and semi-transparent optical position sensors being attached to the pots. At an active area of 2×2 cm^2, these sensors are reported to deliver both the x and y coordinates with a precision on the order of 1 μm which, if achieved also in field, would be clearly superior to any mechanical reference system exposed to varying forces and temperatures.

Chapter 2

Silicon Detectors

When elementary particles or photons interact with silicon material, charge carriers of opposite polarity (electrons, holes) are created; collecting and measuring the generated charge gives a measure for the incident particle's location and energy loss.

The processes involved resemble the interaction of particles with gases. There are, however, quantitative differences between the interaction of ionizing radiation with a semiconductor material and with a gas resp. a fluid. First, the energy necessary to generate an electron-hole pair in silicon amounts to approx. 3.6 eV, whereas there are (at average) 30 eV necessary in a gas. Secondly, the absorption of silicon (density 2.3 g/cm^3) is considerably higher than that of gases with densities (depending on the gas pressure) of 10^{-3} to 10^{-1} g/cm^3.

From a technical point of view, silicon as detector material is an attractive choice, since semiconductor processing is a well developed technology for the fabrication of integrated circuits. Silicon wafers of high purity can be obtained at comparably low cost; photolithographical methods can be employed to build electrode structures on top of the substrate.

The physical properties of silicon in combination with the technical aspects offer the possibility to construct particle detectors with high spatial and energy resolution as well as fast timing.

2.1 Charge Creation

When traversing silicon the ionizing particle transfers energy and momentum to the crystal lattice and electrons. Two different mechanisms can be separated:

1. Crystal vibrations (phonons) are excited by (mainly) momentum transfer; this effect is not desired, since phonons cannot be detected by means of electrical amplifiers

2. Electron-hole pairs are created by excitation of electrons from the valence band to the conduction band.

We will furtheron concentrate on the second mechanism. Neglecting channeling-, Čerenkov- and transition radiation as well as high energy transfer processes (δ-electrons) the mean energy loss per unit path length $<\frac{dE}{dx}>$ (also called stopping power) of a charged particle can be described by the Bethe formula [Beth33]

$$<\frac{dE}{dx}>= -\frac{4\pi q^4 z^2 nZ}{m_e v^2}\left\{\ln\left[\frac{2m_e v^2}{I(1-\beta^)}\right]-\beta^2\right\} \quad . \tag{2.1}$$

v particle velocity

$\beta = v/c$

z charge of incident particle

n atom density of medium

Z atomic number of medium

I average ionization potential (I_{Si}=172 eV)

m_e electron rest mass

q electron charge

The ionization potential to be used in the Bethe-formula is the value for the primary ionization processes when energy and momentum is transferred mainly to electrons of inner shells of the silicon atoms. It can be seen from eq. (2.1) that the energy loss increases at low particle velocities with $1/v^2$; if a particle stops in a material, most of its total energy is delivered at the very end of its track (Bragg-peak).

The distribution of the energy loss per unit path length $\frac{dE}{dx}$ is approximated by the Landau-distribution [Lan44]. The Landau-distribution is asymmetrical with a high-energetic tail the latter being due to occasional high energy transfer to single electrons (δ-electrons). δ-electrons ultimately limit the resolution of silicon strip detectors since they can travel several dozens of μm delivering energy to valence-band electrons before they finally stop (resp. escape the detector volume).

The variance of the Landau-distribution is considerably smaller than the so-called $\sqrt{N}$-error of counting processes (which is subject to the Poisson distribution). It can be therefore be inferred that the ionization events along the track are not statistically independent. Since the Landau-distribution is often not at hand, a phenomenologic number F (the so-called Fano-factor) has been introduced [Kno97] which makes it possible to refer the variation observed to the Poisson-distribution:

$$\mathrm{var}(Q) = \sigma^2(Q) = F < Q >= F\frac{< E >}{\epsilon} \tag{2.2}$$

$< Q >$ average charge delivered in the detector

$< E >$ average energy delivered in the detector

ϵ=3.6 eV energy to create one electron-hole pair

F Fano-factor

For a Poisson-distribution the Fano-factor would be 1; for silicon the Fano-factor varies between 0.084 and 0.143.

For a minimum ionizing particle (MIP) of elementary charge q like a 1-2 MeV electron the average energy loss per unit path length in silicon amounts to $<\frac{dE}{dx}>\approx$ 390 eV/μm [PDG84] or 110 electron-hole-pairs per μm. The most probable energy loss (note the asymmetry of the Landau-distribution) is 290 eV/μm corresponding to 82 electron-hole-pairs per μm yielding 88 keV or 24600 electron-hole-pairs in a 300 μm silicon detector.

Hence, the average energy ϵ for lifting an electron into the conduction band is approx. 3.6 eV which is larger than the bandgap of 1.12 eV.

Electrons and holes can recombine again creating photons and phonons; to separate the electron-hole pairs an external voltage is applied to the detector electrodes. However, with *homogenous* silicon being a semiconducting material, application of a high voltage would cause a significant current to flow due to the thermally excited electrons in the conduction band which would superimpose on the charge signal by elementary particles (the same argument holds for electronic silicon material).

By doping of the silicon spatially inhomogenous charge carrier densities are created; by appropriate order of the layers (pn-junction) and external biasing the thermally induced current is suppressed and measurements at room temperature can be performed.

atomic mass	28.09 amu
crystal lattice	diamond
lattice constant	5.43 Å
relative dielectric constant ϵ_r	11.9
breakdown field strength	aprox. 3 $\cdot 10^5$ V/cm
bandgap (300 K)	1.12 eV
intrinsic charge carrier density (300 K)	1.45 $\cdot 10^{10}$ cm^{-3}
n-substrate doping concentration	1.5-2 $\cdot 10^{12}$ cm^{-3}
electron mobility μ_n (300K)	1380 cm^2/(Vs)
electron diffusion constant D_n (300K)	approx. 35 cm^2/s
hole mobility μ_p (300K)	450 cm^2/(Vs)
hole diffusion constant D_n (300K)	approx. 11 cm^2/s

Table 2.1: Physical properties of detector silicon [Sze81]

Doping is achieved by addition of certain impurities. Some of the silicon atoms in the crystal lattice are replaced by atoms of different elements; when adding phosphorus or arsenic ("donors"), each of which contributes five electrons, a loosely bound excess electron not involved in bonds to the neighbour atoms is created, which easily is excited into the conduction band. The material becomes conductive for electrons and is called n-type.

Adding atoms with three electrons ("acceptors") like boron or aluminium to the silicon substrate introduces vacancies (or holes) in the valence band. The material becomes conductive for holes and is called p-type.

At the junction of p-doped and n-doped silicon regions a diffusion current flows due to the difference of charge carrier concentrations; a current of electrons flows from the n-type region to the p-type region and vice versa (see fig. 2.1 a)). This double flow produces a double layer of static positive and negative charge on both sides of the junction fig. 2.1 b), setting up a potential difference V_D across the junction (fig. 2.1 c)). In equilibrium, diffusion current and field induced current are equal; due to recombination of the free charge carriers nearly no free charge carriers exist in the junction region. It is important to recognize that this depletion layer is the only ionization sensitive volume of a detector since only there an electrical field is present.

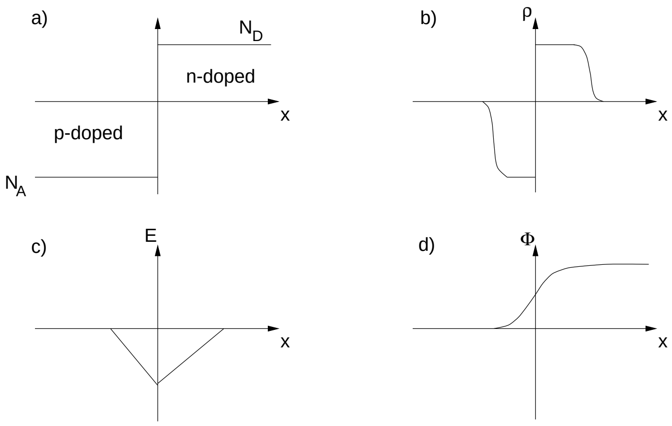


Figure 2.1: Pn-junction in thermal equilibrium: a) doping profile, b) space charge density ρ c) electrical field E, d) potential Φ

Applying externally a voltage of the same polarity as V_D (reverse bias), the depletion zone increases into the n- and p-doped regions depending on doping- and charge carrier concentrations. The depth of the depleted layer is given by [AM81]

$$d_{n,p} = \sqrt{\frac{2\epsilon_0\epsilon_r(V_0 - V_D)}{q(n_D + n_A)}\frac{n_A}{n_D}} \quad . \tag{2.3}$$

$d_{n,p}$ depth of depletion layer in n- resp. p-doped regions

n_A acceptor concentration

n_D donor concentration

$\epsilon_0\epsilon_r$ dielectric constant of silicon

$q = 1.6 \cdot 10^{-16}$ C electron charge

V_0 external voltage

For $n_A \gg n_D$, $V_0 \gg V_D$ and with the specific resistivity

$$\rho_n = (q\mu_n n_D)^{-1} \tag{2.4}$$

μ_n electron mobility

eq. (2.3) becomes

$$d_n = \sqrt{\frac{2\epsilon_0\epsilon_r V_0}{q n_D}} = \sqrt{2\epsilon_0\epsilon_r\mu_n\rho_n V_0} \quad . \tag{2.5}$$

The depletion depth increases with the square root of the reverse voltage V_0 applied; the larger the purity resp. the resistivity ρ_n of a silicon substrate the easier large depetion depths can be reached. Typically one uses voltages V_0 of 40V-140V to deplete high ohmic substrates of 300 μm. At these voltages the wafer substrate is almost completely depleted and the whole detector depth becomes sensitive to ionizing radiation. Due to the pn-junction mechanism there is only a small diode leakage current flowing.

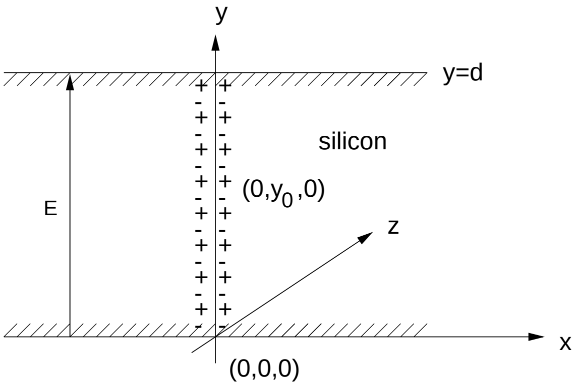


Figure 2.2: Silicon detector (schematic); a particle traverses the detector along the line $x = z = 0$. The drift of an electron-hole pair created at (0,y_0,0) is discussed in the text.

2.2 Signal Charge Transport

When a minimum ionizing particle traverses the silicon detector at $t = 0$ along the line $x = z = 0$, it creates a cylinder of electron-hole pairs of approx. 0.1 μm radius (fig. 2.2) [Kno97].

By applying an external field the electrons and holes are separated and drift to the electrodes. By induction a current is induced on the electrodes through the moving charges; it should be emphasized that the induction current obtained at the electrodes is sustained only during the charge migration inside the capacitor volume; once a charge has reached the electrode, the current goes to zero again. The total current is a superposition of the currents created by electrons and holes.

The electrical field inside the fully depleted detector (fig. 2.2) can be obtained by solution of the Poisson-equation and (in this first-order model) consists only of a y-component [Bel83]

$$E_y(y) = \left[\frac{V_0 - V_D}{d} + \frac{2yV_D}{d^2}\right] \tag{2.6}$$

which can be simplified for $V_0 \gg V_D$ to the simple capacitor formula (2.7) [Kno97]

$$E_y(y) = \frac{V_0}{d} = E_0 \quad . \tag{2.7}$$

The charge migration $y(t)$ now is obtained by integration of

$$dt = \frac{dy_{n,p}}{v_{n,p}} = \frac{dy_{n,p}}{\mu_{n,p}E_0} \tag{2.8}$$

yielding

$$y_{n,p}(t) = \pm\mu_{n,p}E_0t + y_0 \tag{2.9}$$

where (0,y_0,0) denotes the place of creation of the electron-hole pair. E_0 is assumed to be constant, i. e. we assume the induced voltage dV_0 due to the charge drift to be small w. r. t. the detector voltage V_0.

The drift time $t_{n,p}(y_0)$ of an electron/hole to the anode/cathode plane at $y = 0$ resp. $y = d$ is simply given by

$$\begin{aligned} t_n(y_0) &= \frac{y_0}{v_n} = \frac{y_0}{\mu_n E_0} = \frac{y_0 d}{\mu_n V_0} \\ t_p(y_0) &= \frac{d - y_0}{v_p} = \frac{d - y_0}{\mu_p E_0} = \frac{(d - y_0)d}{\mu_p V_0} \quad . \end{aligned} \tag{2.10}$$

The potential energy dW/dy per unit path length delivered by the motion of a charge Q is given by

$$dW = QE_y(y)\,dy = QE_0\,dy \quad . \tag{2.11}$$

This energy must come at the expense of the energy stored on the detector capacitance (we assume the detector to be floating)

$$dW = d(\frac{1}{2}CV_0^2) = CV_0\,dV_0 = V_0\,dQ_{ind} \tag{2.12}$$

where dQ_{ind} is the induced charge at the electrodes.

The induced charge $Q_{ind}(t)$ can be obtained by equating eq. (2.11) and (2.12)

$$\frac{dQ_{ind-n,p}}{dy} = \frac{Q_{n,p}}{d} \quad . \tag{2.13}$$

By integration we obtain

$$Q_{ind-n+p} = q(\frac{v_n}{d}t + \frac{v_p}{d}t) \tag{2.14}$$

for the combined electron-hole current. Eq. (2.14) holds for the case that both electrons and holes contribute to the current, i. e. none of them has already reached an electrode. By substitution of the drift times eq. (2.10) into eq. (2.14) the totally induced charge $Q_{ind-n+p}$ is found to be equal the charge Q produced by ionization.

The current is easily derived by dividing eq. (2.14) by t

$$I_{ind-n+p} = \frac{q}{d}(v_n + v_p) \tag{2.15}$$

which holds when both sorts of charge carriers contribute. Thus, the current delivered by the planar detector is constant in time and is zero at latest after the hole collection time $t_p(y_0 = 0)$. For V_0=100V and a 300 μm thick silicon detector $t_p(y_0 = 0)$ is 20 ns. Experimental evidence of the charge collection time inside silicon strip detectors [Ru94] yields that 90% of the charge is collected within 12 ns for 100 V of detector bias, which drops to 7 ns for 300 V.

In the following chapters we will approximate the current pulses delivered by the silicon detector as δ-shaped without comitting a large error (e. g. the preamplifier risetime equals $\approx$ 50 ns). A schematic plot of the current for various ionization loacations in the silicon detector is given in fig. 2.3

The total movement of the charge created along the particle track in the detector is superimposed by the field-independent diffusion parallel to the electrode plates and the field-induced drift in y-direction as given by eq. (2.15); by appropriate substitution and integration one can obtain the drift time distribution resp. the induced current as well as the spatial distribution of the signal charge at the electrodes.

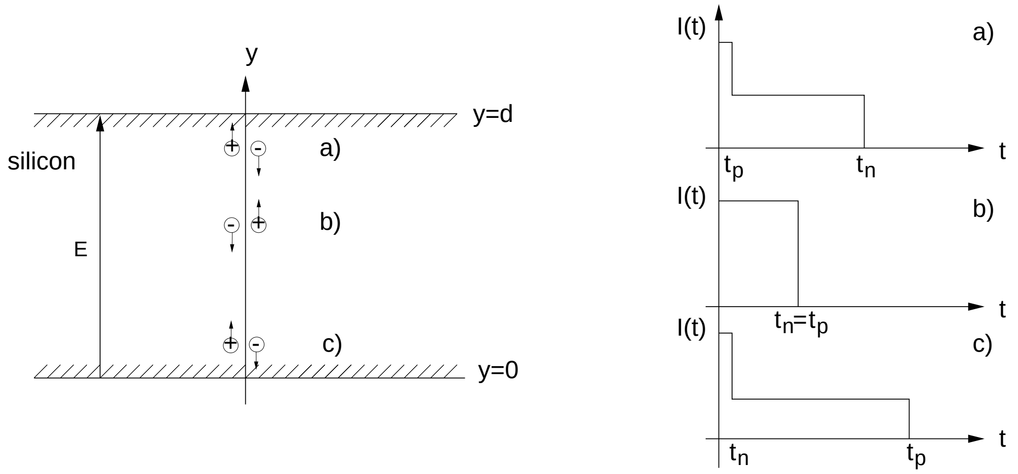


Figure 2.3: Current induced at the electrodes by drift of an electron-hole pair in the detector; a), b), and c) denote the different ionization locations. The current is zero at latest after the collection time for a hole created at the anode (y_0=0).

2.3 Silicon Strip Detector

Position sensitive detectors aim at measuring the point in one or two dimensions where a particle crosses the detector. Two principles are currently employed:

1. By segmentation of the p- resp. n-implantations the overall detector area is subdivided into many single diodes. With a particle crossing such a detector only the strips in the neighbourhood of the track collect charge. By appropriate weighting the spot of the particle incidence can be determined (siliccn strip detector, pixel detector).

2. By appropriate geometry of the electrode implantations the electrical field can be formed such that the signal charge drifts to a single electrode. By measuring the drift time the distance of the particle track to this electrode can be determined (silicon drift chamber).

On silicon strip detectors, which follow the first principle, strip-like p^+-implantations (the "+" denotes a heavy dotation) are located perpendicularly to the drawing plane in fig. 2.4, each of them being read out by an own amplifier channel. The low-input-impedance amplifier keeps the p^+-implantations at ground potential. The reverse bias voltage is applied to the n^+-implantation on the detector back side.

Assuming a point-like (in the x-z plane) signal-charge distribution the position resolution σ obtainable depends only on the strip-spacing b [Lutz87] (also referred to as binary readout resolution):

$$\sigma = \frac{b}{\sqrt{12}} \tag{2.16}$$

If the charge cloud created by an ionizing particle reaches two or more strips, a center-of-gravity interpolation can determine the coordinate of the point of particle incidence;

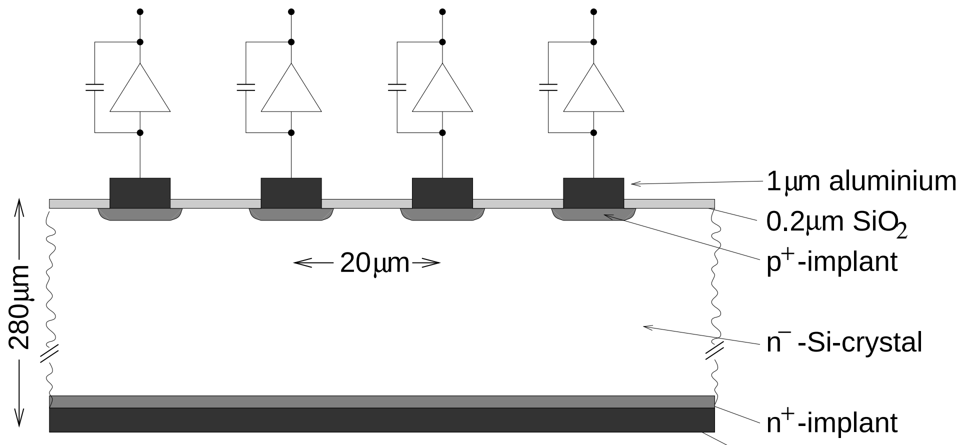


Figure 2.4: Single-sided strip-detector [Klei92]

with the optimistic assumption of a rectangular charge distribution of width b (i. e. the strip-spacing) and the signal-to-noise ratio S/N of the detector/electronics system one obtains [Lutz87]

$$\sigma^2 = \left(\frac{b}{\mathrm{S/N}}\right)^2 \sum_{i=1}^{n} \left(\frac{x_1 - x}{b} + (i-1)\right)^2 \quad . \tag{2.17}$$

S/N signal-to-noise ratio

x calculated center-of-gravity

i strip index

n, $n \geq 2$ number of strips used in the calculation of the center-of-gravity

x_1 first strip used in the calculation

It follows that the optimum resolution is obtained when the signal of only two adjacent strips is evaluated; in this case and for a particle crossing in the middle of two strips eq. (2.17) simplifies to

$$\sigma^2 = \frac{b^2}{2 \cdot (\mathrm{S/N})^2} \quad . \tag{2.18}$$

For a strip spacing $b = 25\mu$m and a signal-to-noise ratio S/N=20 formula (2.18) gives a spatial resolution of 0.88 μm (this was obtained under the optimistic assumption of a charge cloud of width b). In practical operation 10 μm is already considered to be a good value.

To reach high position resolution very small strip spacings are necessary which leads to high numbers of electronics channels. By using capacitive charge sharing [Kötz85] of adjacent strips this number can be decreased at little resolution degradation (fig. 2.5). In this scheme every n-th diode strip (n=2..5) is connected to an amplifier channel. By use of a high-ohmic connection the non-connected strips are kept on equal potential to assure a homogenous field distribution in the detector and a linear charge sharing.

Traverses a particle the detector at the non-connected strip B, the generated charge Q is collected at the corresponding diode strip. Due to the inter-strip capacitances C_S mirror charges are created at points A and E, where they are measured. Neglecting the backplane capacitances C_D the mirror charges obtained are $Q_A = 3/4Q$ and $Q_B = 1/4Q$.

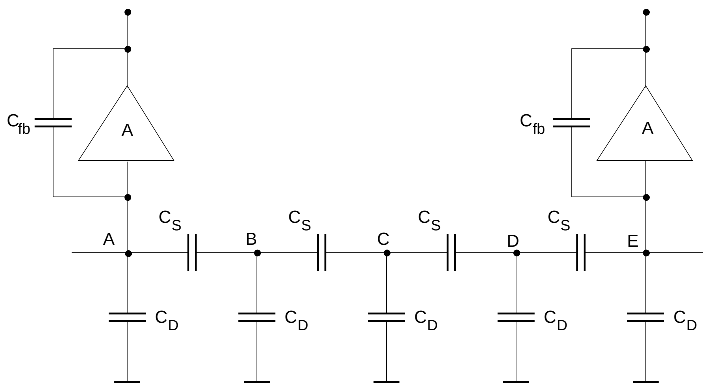


Figure 2.5: Capacitive charge sharing: every 4th strip is connected to a charge amplifier with input capacitance $A \cdot C_{fb}$. If a charge Q is put on node B, mirror charges can be obtained at nodes A and E where Q_A/Q_E=3. $Q_A + Q_E < Q$ due to "charge loss" on the C_D's [Bau90].

Hence by the use of capacitive charge sharing the charge distribution after ionization is broadened and fewer amplifier channels are needed.

Fig. 2.6 shows the double-sided strip-detectors as used in the HERA-B silicon vertex-detector [Bis93, Riech98]. Strip-like electrodes have been implanted on both front- and back-plane; the p^+-doped strips on the so-called p-side of the detector form a pn-junction with the n^--doped substrate; the n^+-doped strips on the n-side which are rotated by 90 ° w. r. t. the strips on the p-side, form an ohmic contact to the n-substrate. By biasing the n^+-strips with a positive high voltage w. r. t. the p^+-strips, a detector depletion can be achieved as in the case of the single-sided detector.

At the n-side additional p-stop implants are necessary to operate the detector safely; this is due to the fact that the always present positive oxide charge in the silicon dioxide layer at the detector surface causes an n-inversion layer beneath (in analogy to MOSFET inversion) which causes a conductive path between adjacent n^+-strips; this effect worsens during the life time of the detector since the oxide charge augments during irradiation (this is also well known from MOSFET-physics). The p-stops introduce a reverse biased pn-junction decoupling the n^+-strips.

The detector depicted in fig. 2.6 is an AC-coupled detector, i. e. there is an oxide-layer between metallic contact and implant (MOS-structure); the advantage is that diode leakage currents do not flow into the amplifier inputs causing saturation. In the present design the coupling capacitances are 140 pF on the p-side and 100 pF on the n-side [Abt98]. An additional silicon nitride layer reduces the probability of shorts increasing the yield of "good" strips. In order to provide a DC-path for the detector biasing polysilicon resistors in the MΩ-range (see also fig. 2.7) connect the strips to the bias lines.

A (large signal) electrical model is given in fig. 2.7 (cf. appendix B); the charge/current generated by a particle is assumed to flow completely through a single n^+- and p^+-strip. Fig. 2.8 shows the small signal model without the noise sources (these will be added in chapt. 4). Since the current through n^+- and p^+-strip is equal, the combined system can be separated applying circuit regrouping techniques. It is interesting to notice that the capacitance C_{inter} between the signal-carrying n^+- and p^+-strip is doubled. This

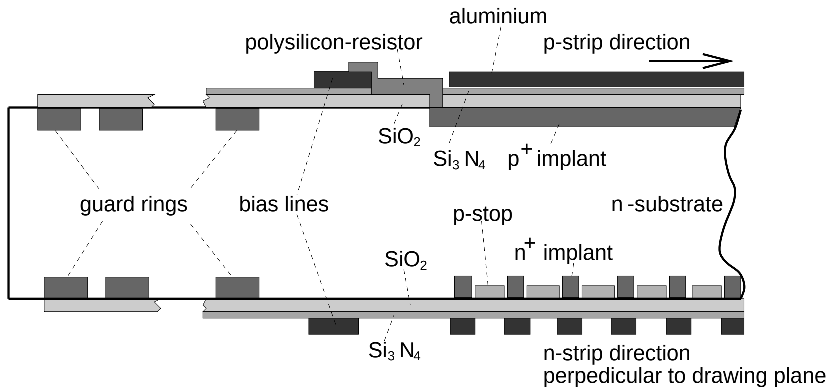


Figure 2.6: AC-coupled double-sided strip-detector [Riech98]

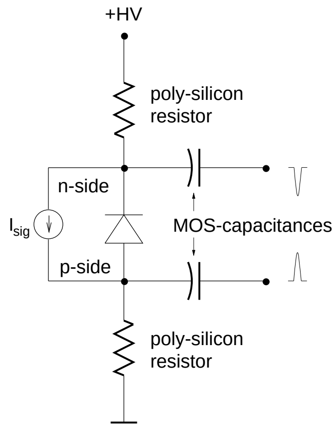


Figure 2.7: Large signal model of a single diode on a double-sided strip-detector; in principle every n^+-strip forms a diode with every p^+-strip.

might worry the experienced reader, since, as we will see in chapt. 4, the serial noise of a charge amplifier is proportional to the input capacitance. However, because C_{inter} is only a very small fraction of the total capacitance of a strip (in particular, a strip has the same C_{inter} to all (n-1) strips of the opposite detector side), this effect is negligible. The impedance looking into the bias resistor R_{bias} in parallel to the strip capacitance $\approx C_{det}$ should be much larger than the impedance looking into the couple capacitor C_c in series with the amplifier input impedance; if this condition is fulfilled, one can obtain nearly the full AC-current at the amplifier input. AC- vs. DC-coupled detectors are discussed from the noise point of view in chapter 4.

The silicon strip detectors used at HERA-B have a total active area of 50×70 mm^2 with 1280 strips of pitch 54.6 μm on the n-side and 1024 strips of pitch 51.7 μm on the p-side.

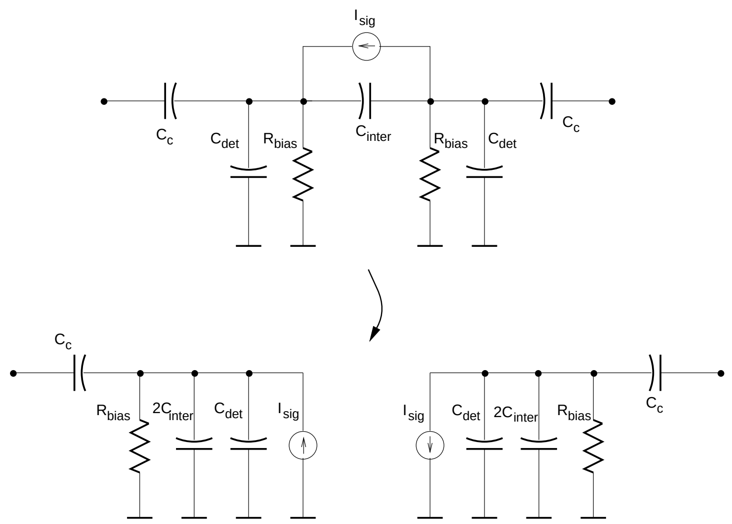


Figure 2.8: Small signal model of fig. 2.7; the silicon detector can be modelled by an AC-coupled current signal source with capacitive and resistive output impedance. The noise sources are not included in this figure.

Chapter 3

Gaseous Detectors

Several of the oldest and widely used types of radiation detectors are based on the effects produced when a charged particle passes through a gas. Ionization and excitation of gas molecules are the primary processes observed along the path of the particle. The majority of detectors exploits the second effect sensing the created charge.

Ion chambers are the simplest of all gas-filled detectors. The operation is based on collection of the charges created by direct ionization within the sensitive detector gas volume by means of an electrical field.

Proportional counters vary the simple principle in so far that they make use of the effect of gas multiplication. By applying large fields to the gas volume electron/ion avalanches are produced due to secondary ionization. In multiwire proportional counters multiple anode wires are used to introduce a spatial resolution. Electrons formed by ionization of the gas drift toward the nearest wire where avalanches are formed in the surrounding high-field region.

Microstrip gas detectors (MSGCs) [Schm97] use metallic traces on a glass substrate as anodes; the major advantage w. r. t. anode wires lies in the enhanced position resolution which can reach 100 μm or less. Silicon strip detectors as described in the previous chapter with strip widthes approaching 100 μm region have a too high capacitance per strip - this is deleterious for the noise of the electronic amplification. Furthermore, MSGCs can be produced in large sizes (glass substrate!)

3.1 Ionization Process in Gases

When a fast charged particle passes through a gas, both excited molecules and ionized molecules are created along its path. The Bethe formula eq. (2.1) describes as in the case of a solid detector the mean energy loss per path length of a charged particle. As within the silicon detector, more than the gas molecule's ionization energy has to be consumed at average to create an electron-ion pair (e. g. excitation is a competing process). In most gases of interest the ionization energy is between 10 and 20 eV; the average energy required to produce an ion pair lies between 26.4 eV (argon) and 41.3 eV (helium) for the most common gases (table 3.1) [Kno97].

Ionization produces mainly free electrons and positively ionized molecules (ions). At low values of the electrical field, the electrons and ions simply move along the electrical

gas	fast electrons	alpha particles
Ar	26.4 eV	26.3 eV
He	41.3 eV	42.7 eV
H_2	36.5 eV	36.4 eV
N_2	34.8 eV	36.4 eV
Air	33.8 eV	35.1 eV
O_2	30.8 eV	32.3 eV
CH_4	27.3 eV	29.1 eV

Table 3.1: Average energy required to produce an electron-ion-pair for fast electrons and alpha particles [Kno97]

field lines to the electrodes. During the drift of the electrons and ions, many collisions occur with neutral gas molecules. Because of their low mobility, positive ions accept very little kinetic energy between collisions. Free electrons, on the other hand, are easily accelerated by the applied field and may have significant energy when undergoing such a collision. If the electrical field strength exceeds a certain threshold value (app. 10^6 V/m in most gases), the energy acquired by the electrons suffices to create another electron-ion pair in collision. The electrons liberated by this secondary ionization process are accelerated, too, and may again ionize molecules - an avalanche arises. Under proper conditions, the number of secondary events can be kept proportional to the number of primary ions formed. Consequently, the demands imposed on the electrical amplification are greatly reduced.

Thus, a typical signal from a proportional counter is developed in a two stage-process: the incident particle creates a number of primary electron-ion pairs which drift towards the corresponding electrodes; when an electron reaches the high-field region around the anode, it creates an avalanche.

The average charge Q produced by a proportional counter can be expressed by

$$Q = nqM \tag{3.1}$$

where n ist the number of primary electron-ion pairs, q is the electron charge, and M is the gas multiplication factor. Due to the much lower mass densitiy of gases w. r. t. solids n is considerably lower than in silicon detectors ($n \approx 7$ per mm for Ar:DME (50:50) at atmospheric pressure).

The electron multiplication factor M depends on the gas, on the gas pressure, and on the applied electrical field; the Diethorn-formula [Diet56] is a widely used expression for M in proportional counters with cylinder geometry:

$$\ln M = \frac{V}{\ln(b/a)} \frac{\ln 2}{\Delta V} \ln\left(\frac{V}{paK \ln(a/b)}\right) \tag{3.2}$$

V applied high-voltage

a anode radius

b cathode radius

p gas pressure

ΔV,K gas parameters

Neglecting the slowly varying last ln-term in eq. (3.2) M depends on the applied voltage V in an exponential manner. M usually lies in the region of several thousands.

The distribution in charge amplitude Q for values $n > 20$ can be approximated by a Gauss-distributian; its standard deviation can be obtained by [Kno97]

$$(\frac{\sigma Q}{Q})^2 = \frac{1}{n}(F + b) \tag{3.3}$$

where F is the Fano-factor (typical values of 0.05-0.2) and b is the parameter from the Polya-distribution that characterizes the avalanche statistics (typical value of 0.4-0.7). Hence, the overall variance is determined mainly by the fluctuations in avalanche size and to a minor extent by the number of primary electron-hole pairs. For a value of n=25 and a pure argon filling (F=0.17, b=0.50) a S/N of approx. 6.1 can be expected which is considerably worse than the intrinsic resolution of a silicon detector.

Because gas multiplication relies on free electron movement, the fill gas must not exhibit appreciable electronegativity (i. e. electron attachment affinity); noble gases are therefore most often used as filling gases. Proportional counters must be designed with provision to maintain the purity of the gas; impurities, especially oxygen, can decrease significantly the life time of free eletrons in the gas. However, a "quench" gas is often added to the main gas. The task of this additional gas is to absorb visible and UV-photons which are created by de-excitation of gas molecules excited during the avalanche formation. If the photons were not absorbed, they could create free electrons elsewhere (e. g. in the counter wall or in gas impurities) and a loss of proportionality, time and space information could result due to creation of displaced (and delayed) excess avalanches. It has been found that the addition of polyatomic gases like methane (CH_4) to many of the fill gases absorbs the photons in a non-ionizing manner.

3.2 Signal Charge Transport

Virtually all the charge generated within a proportional counter as the MSGC originates within the avalanche region, regardless of where the original ion pairs are formed. One therefore has to distinguish the drift time of the free electrons required to travel from the position of nascense to the region of multiplication and the multiplication time required from the onset of the avalanche to its completion. The drift time is normally much greater than the multiplication time and varies depending on the distance of the original ion pair from the high-field region around the anode.

The electrical field distribution (fig. 3.3) inside the MSGC-detector volume lies somewhere between the conditions encountered in a planar detector as the silicon strip detector and the one encountered in a proportional counter with cylindrical geometry. The derivation of charge motion, induced charge, and collection time given in chapter 2 for a silicon detector can be transfered to the planar proportional counter with hardly any change; in the following we want to deduce the corresponding equations for the case of cylindrical geometry in an analogous manner. Simulation results for an actual microstrip gas chamber will be presented in the next section.

The electrical field E inside an cylinder capacitor is given by

$$E(r) = \frac{V_0}{\ln(b/a)r} = \frac{E_0}{r} \quad . \tag{3.4}$$

a, b inner,outer cylinder radius

V_0 potential difference between inner and outer cylinder

Because most of the ions and electrons are created very close to the anode, the bulk of the output pulse is attributable to drift of the positive ions. The drift velocity v_+ of the positive ions is given by

$$v_+(r) = \frac{\mu}{p} E(r) = \frac{\mu}{p} \frac{E_0}{r} \tag{3.5}$$

where p ist the gas pressure. Thus the drift velocity depends on the radial position - near the anode wire it is highest and decreases radially $\propto 1/r$. Note the slightly different definition of the ion mobility inside a gas w. r. t. electrons/holes in solids.

By integration of the law of motion

$$\int_a^{r(t)} \frac{dr}{v_+(r)} = \int_0^t dt \tag{3.6}$$

the radial path $r(t)$ can be obtained

$$r(t) = \sqrt{2 \frac{\mu_+}{p} E_0 t + a^2} \tag{3.7}$$

where we assumed the charge motion to have started at the wire diameter a. The collection time t_+ can be obtained by equating eq. (3.7) to b and is given by

$$t_+ = \frac{(b^2 - a^2) p \ln(a/b)}{2\mu_+ V_0} \quad . \tag{3.8}$$

The collection time thus depends on the the electrode separation, the applied voltage,the hole mobility and the gas pressure.

The potential energy dW/dr per path length delivered by the motion of a charge Q is given by

$$dW = QE(r)\, dr = Q \frac{E_0}{r}\, dr \quad . \tag{3.9}$$

This energy must come at the expense of the energy stored on the detector capacitance

$$dW = d(\frac{1}{2} C V_0^2) = C V_0\, dV_0 = V_0\, dQ_{ind} \tag{3.10}$$

where dQ_{ind} is the induced charge at the electrodes.

The induced charge $Q_{ind}(t)$ can be obtained by equating eq. (3.9) and (3.10)

$$\frac{dQ_{ind}}{dr} = \frac{Q}{V_0} \frac{E_0}{r} \tag{3.11}$$

and integration yields

$$Q_{ind}(t) = \frac{Q}{V_0} E_0 \ln(\frac{r(t)}{a}) \quad . \tag{3.12}$$

When the ion finally arrives at the cathode cylinder electrode ($r(t) = b$), the induced charge equals the charge created by the avalanche process ($Q_{ind} = Q$).

The current pulse is given by the derivation of eq. (3.12) w. r. t. t and is given by

$$I_{ind}(t) = \frac{Q}{V_0} E_0 \frac{\dot{r}(t)}{r(t)} \quad . \tag{3.13}$$

$\dot{r}(t)/r(t)$ is proportional to $1/t$ for sufficiently small wire diameters a - the current pulses created in a cylinder geometry hence have a $1/t$-like decay behaviour.

Fig. 3.1 shows schematically the values $r(t)$, $Q_{ind}(t)$, and $I_{ind}(t)$ vs. time.

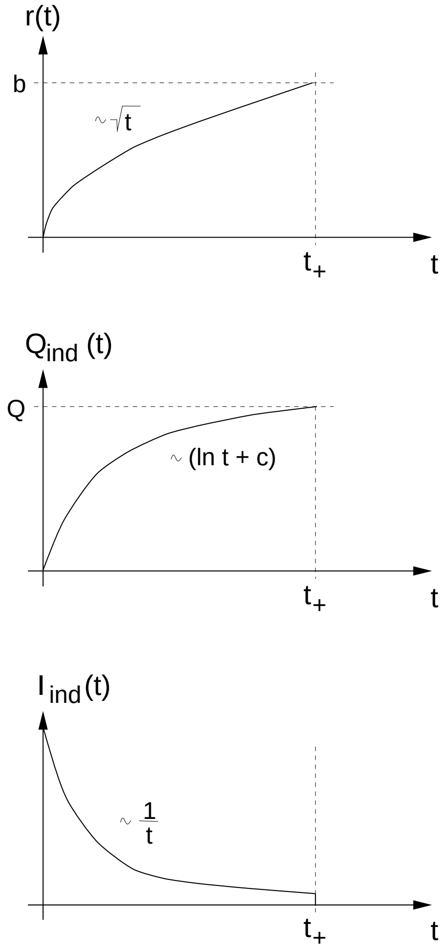


Figure 3.1: Drift of a positive ion Q in a cylindrical proportional counter: path $r(t)$, induced charge $Q_{ind}(t)$, and induced current $I_{ind}(t)$ vs. time

3.3 Microstrip Gas Chamber (MSGC)

Fig. 3.2 shows a cross-section of a MSGC [Beck96]. On the lower substrate narrow anode strips alternate with broader cathode strips. A glass wafer serves as the mechanical carrier providing a plane surface. Since the intrinsic conductivity of glass (and hence

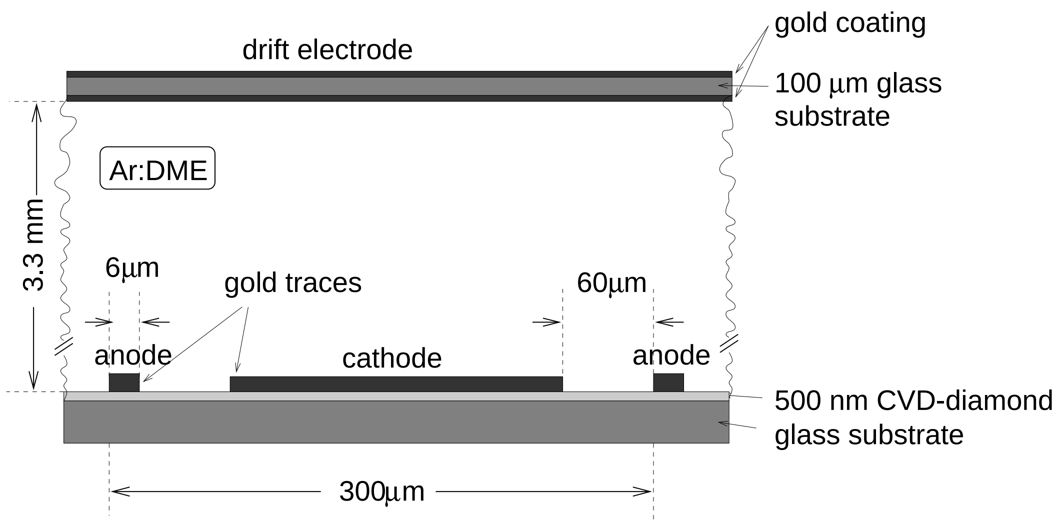


Figure 3.2: Crossection of a microstrip gas chamber (MSGC) [Beck96]

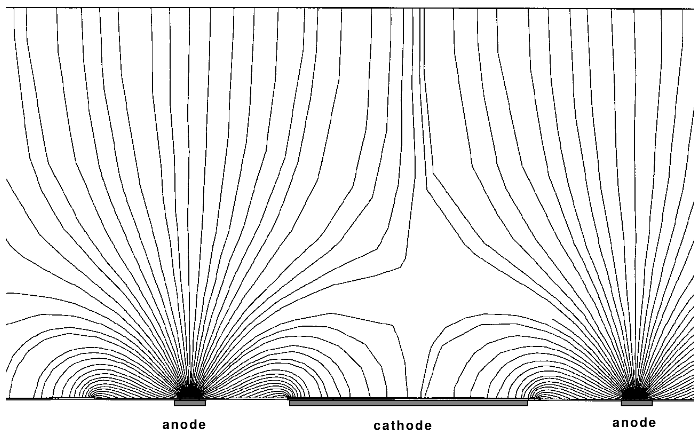


Figure 3.3: Electrical field inside a MSGC [Bre97]: electrons/ions move along the field lines to the electrodes. The densely spaced field lines around the anodes indicate a high field strength.

the electrical field) depends on the badly defined and alterable ion distribution in the glass, a diamond coating covers the glass substrate providing a small finite electronic conductivity ($10^{14} - 10^{16}\,\Omega$/square). The electrodes are made of metal (e. g. gold) which are placed on top of the CVD-diamond-layer by photolithography. A pitch of 300 μm has been selected for the HERA-B-application. Above the bottom substrate a gas layer of approx. 3.3 mm forms the active detection volume. The drift electrode is a gold-coated thin glass plate which at the same time serves as the top enclosure of the gas cavity.

The fill gas used is a 50:50 mixture of argon and the quench gas DME ($(CH_3)_2)O$) at ambient pressure. DME as polyatomic molecule has many excited states (vibration, rotation) and absorbs UV-photons over a wide band. The DME, however, can also be excited by electron collisions thus removing energy from the free electrons. Argon being a monoatomic gas exhibits comparably few excitation states and thus enhances the electrons' free path length. The chamber is operated at a gas multiplication of $\approx$

2500.

In a variant an additional foil ("gas electron multiplier") has been introduced at half height of the drift volume in parallel to the glass planes to provide electron multiplication prior to the multiplication in the anode region. Thus, the gas gain resp. the field between anode and cathode can be reduced and the susceptibility to sparks between cathode- and anode-strips induced by heavy ionizing particles (e. g. alpha-particles) decreases.

In operation the drift electrode is set to V_0 = - 3 kV yielding a drift field of E_0=10 kV/cm (fig. 3.3 [Bre97]). The ion drift velocity v_+ in the Ar-DME gas mixture is approx. 60 μm/ns; thus the maximum possible drift time t_+ is 55 ns which lies in the order of the readout amplifier's shaper time. The voltage applied at the cathode V_1= -630 V provides an anode-cathode field of approx. 100 kV/cm. The anode strips are kept on ground potential by the attached low-impedance charge amplifier input. The total capacitance of an anode strip of 30 cm length is in the range of 10-20 pF.

When a minimum ionizing particle (see chapt. 2) traverses the gas, so-called ionization clusters, each of them consisting of 2-3 electron-ion pairs, are created. In the 3.3mm thick Ar-DME gas-mixture of atmospheric pressure at average 32 electron-ion pairs are generated, the most probable number being 22 (Landau-distribution !). The electrons drift to the high field-region around the anode, where they give rise to a (most probable) signal amplitude of 55000 electrons, which is roughly twice the value obtained with 300 μm silicon detectors.

The position resolution obtained with MSGCs can be calculated in first order according to eq. (2.16) to be $\approx$ 87 μm.

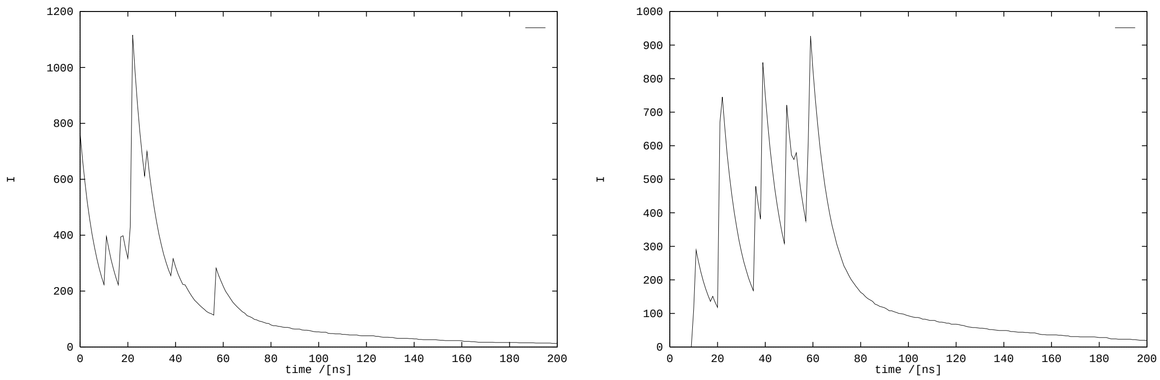


Figure 3.4: Time behaviour of anode currents delivered by a 3.3 mm drift-space MSGC for a traversing MIP particle (simulation) [Lang96]; the current is given in arbitrary units.

Fig. 3.4 [Lang96] shows the time-resolved current delivered by a 3.3 mm drift-space MSGC in response to a MIP-particle; current peaks can be observed when the electrons belonging to a cluster reach the anode region and generate an avalanche; the maximum drift time is approx. 60ns in accordance with the expectation. The $1/t$-decay of the current pulses gives evidence that the field strength decreases with $1/r$ near the anode region (cf. eq. (3.13)).

The MSGC's (electrical) small signal model equals the one of the silicon strip detector (fig. 2.8) with the coupling capacitor being omitted.

Chapter 4

Noise in Amplifiers

Statistical signal fluctuations are generally called noise with reference to the sound audible when feeding a "noisy" signal to an acoustic indicating instrument such as a loudspeaker. Noise denotes ultimately the quality of analog systems such as sensors, communication-links, or entertainment electronics. Noise in electronic devices arises from various mechanisms; the most important ones will be described from a phenomenological point of view in this chapter.

Two sources of statistical variances can be distinguished for particle detector systems: first, the charge deposition of ionizing particles in a detector is subject to the so called $\sqrt{N}$ noise, where N denotes the number of created electron-hole resp. electron-ion pairs (cf. chapt. 2), secondly, noise is introduced by the subsequent electronic amplification stages. In the following, we will focus on detector readout electronics and hence on the "electronic" noise of a detector system.

In a systematic approach the noise performance of voltage-, current-, and charge amplifiers is discussed. The voltage sensitive amplifier is well known from text books; however, for a number of applications current- and charge amplifiers are better suited. This might not immediately be evident since every current is accompanied by a voltage and vice versa; the reason is that many sensors primarily generate a current, which is directly (or integrated) proportional to the physical quantity to measure; the voltage might depend on internal or external boundary conditions [Fal97-1, Her93, Hey92].

Current amplifiers are used in cassette tape-heads, in the readout of ionisation chambers or Geiger tubes or in combination with photodiodes in a multitude of applications (optocouplers, barcode scanners, CD-players ...). The current delivered by the sensors mentioned is directly proportional to the flux of incident light photons. Current amplifiers have recently been introduced into high energy physics for the readout of particle detectors [Dab94, Jar96, RD2-93], especially for very shortly shaped signals, where the transimpedance resistor's shot noise does not matter, and for environments with a high signal repetition rate, where saturation of the (integrating) charge amplifier becomes a problem.

Charge amplifiers are used for the readout of detectors built of semiconductor or gaseous materials for spectroscopic measurements or for the position measurement of ionizing particles. Precise charge measurement is required since the charge deposited by a particle in a detector material is directly proportional to the energy transferred by the particle;

in multi-strip detectors a sub-pitch resolution can be reached by forming the center-of-gravity of the charge deposited in adjacent stripes. The voltage thus created is not a good quantity to measure because it depends on the detector capacitance which is badly defined depending on bias voltage or temperature.

In this chapter we present the architectures of voltage-, current-, and charge-amplifiers; the noise performance and the transfer function (in the time domain) are developed. The focus of the discussion will be put on sources with resistive and capacitive signal impedances as found in radiation detection sensors; inductive sources as found e. g. in AM/FM-systems and magnetic storage devices are not covered. The unavoidable bondwire inductances ($\approx$ 10 nH) cause resonances with the stray capacitances ($<$ 1 pF) in the GHz frequency range - and are beyond the bandwidth of the amplifiers considered.

Furthermore we will comment on the use of voltage- and current amplifiers for charge measurement; despite the drawbacks mentioned above sometimes it can be favourable not to use a charge amplifier.

4.1 Physical Noise Models

Noise is characterized by statistical variations of a voltage or a current from a value, which is often referred to as the "true signal". Since we want to restrict the discussion onto the noise in this context, the signal value is set to zero in the following. The time average of the voltage hence becomes zero; a measure for the magnitude of the noise is the mean of the squared voltage

$$\mathrm{var}\, v = \sigma^2\, v = \overline{v^2} = \lim_{T\to\infty} \frac{1}{2T} \int\limits_{-T}^{T} v^2\, dt \qquad [\mathrm{in}\ \mathrm{V}^2] \quad . \tag{4.1}$$

Noise phenomena are also treated in the frequency domain; one defines the (unilateral) spectral noise density $w(\nu)$ according to [Hin96, Mül89]

$$\overline{v^2} = \int\limits_{0}^{\infty} w(\nu)\, d\nu \qquad [\mathrm{in}\ \mathrm{V}^2] \quad . \tag{4.2}$$

Iwhere $w(\nu) = 0$ for $\nu < 0$. $w(\nu)$ must not be confused with the weighting function $w(\tau)$ which will be introduced in chapt. 5.

Noise arises due to different effects:

Thermal Noise originates from the statistical fluctuation of the charge distribution in a conductor, which is caused by the temperature movement of the charge carriers. Therefore a noise voltage between the ends of the conductor resp. resistor can be observed.

According to Johnson and Nyquist [John28, Nyq28] the mean squared noise voltage of a resistor is given by

$$\overline{v^2} = 4kTR\Delta\nu \qquad [\mathrm{in}\ \mathrm{V}^2] \quad . \tag{4.3}$$

$k = 1,38 \cdot 10^{23}$J/K, T absolute temperature [K]
$\Delta\nu$ system bandwidth [Hz]
R resistance [Ω]

Dividing eq. (4.3) by $\Delta\nu$ yields directly the spectral noise density $w(\nu) = \overline{v^2}/\Delta\nu$; the thermal noise shows a white behaviour, i. e. the spectral noise density is independent of frequency.

The calculation of the noise density for an arbitrary (i. e. also non-white) noise makes use of the autocorrelation function which is defined as

$$\rho(\tau) = \lim_{T\to\infty} \frac{1}{2T} \int_{-T}^{T} v(t)v(t+\tau)\,dt \qquad [\text{in V}^2] \quad . \tag{4.4}$$

The autocorrelation function gives a measure of how much the voltages correlate at two points of time distance τ.

Comparison with eq. (4.1) yields $\rho(0) = \sigma^2\, v = \overline{v^2}$. The Fourier transform of $\rho(\tau)$ yields directly the spectral noise density $w(\nu)$

$$w(\nu) = 2 \int_{-\infty}^{\infty} \rho(\tau)\, e^{-j\omega\tau}\, d\tau \tag{4.5}$$

where the factor of 2 is due to using the unilateral noise density.

This can be seen by taking the inverse (unilateral) Fourier transform

$$\rho(\tau) = \int_{0}^{\infty} w(\nu)\, \cos(2\pi\nu\tau)\, d\nu \quad . \tag{4.6}$$

Substituting $\tau = 0$ in eq. (4.6) yields again eq. (4.2). Eqs. (4.5) and (4.6) are called the Wiener-Khintchine equations.

The equivalent circuit of a noisy resistor (fig. 4.1) is a noiseless resistor of the same value in series with a noise voltage source $w(\nu) = 4kTR$ or in parallel with a noise current source of spectrum $w_i(\nu) = 4kT/R$.

Shot noise is caused by the discrete nature of the charge carriers when traversing a voltage threshold; it can be imagined as "pattering" of electrons and holes, i. e. the charge carriers of a "DC-current" pass the threshold with temporal fluctuations (mathematically speaking: it occurs a Poisson process). Voltage thresholds can be found at pn-junctions or in vacuum-tubes.

The variance of the current is given by

$$\sigma^2\, i = \overline{(i - I_0)^2} = \overline{i^2} - I_0^2 = 2qI_0\Delta\nu \qquad [\text{in A}^2] \quad . \tag{4.7}$$

$q = 1,6 \cdot 10^{-19}$C (elementary charge)
I_0 DC current
$\Delta\nu$ system bandwidth

The shot noise is white as the thermal noise. In the equivalent circuit the shot noise is modeled by a noise current source (fig. 4.1) in parallel to the DC-current I_0.

In addition to the above mentioned noise types *flicker noise* or 1/f-noise is present in active devices like transistors and many passive components; it is characterized by the $1/\nu^x$-dependency of its spectral noise density, where x is close to 1. Systematic research

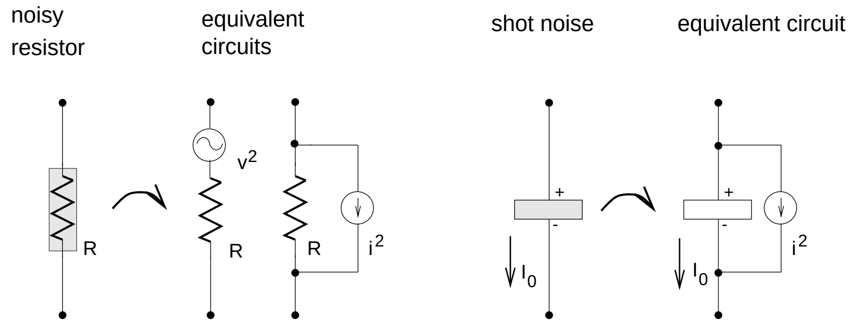


Figure 4.1: Equivalent circuit of noisy resistor (left) and of current shot noise (right)

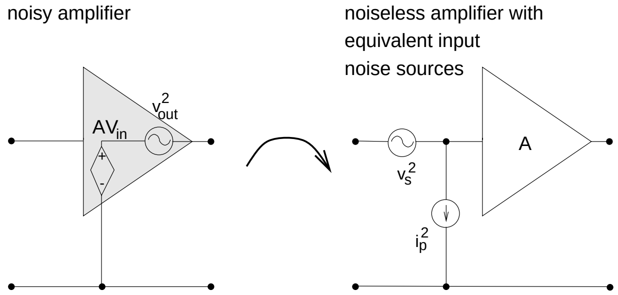


Figure 4.2: Noisy amplifier can be modelled by a noiseless amplifier and two equivalent input noise sources.

unveils that many parameters determine the 1/f-noise; e. g. the quality of surfaces and interfaces have been found to play an important part.

Amplifiers being composed of active and passive devices exhibit output noise with the input both shorted to ground and floating (the internal operation is assumed to be unaffected thereby); therefore, the noisy amplifier can be replaced in the equivalent circuit (fig. 4.2) by a noiseless amplifier with two equivalent input noise sources - a noise voltage source v_s^2 located in series with the input and a noise current source i_p^2 located in parallel. The two noise sources can be partly (or even completely) correlated.

The value of v_s^2 can be determined by shorting the input to ground; the noise apparent at the output is due to v_s^2 only (i_p^2 is shorted); in analogy i_p^2 can be determined by opening the input, since then v_s^2 is floating and the noise at the amplifier output is caused by i_p^2 only.

When studying a system consisting of signal source, amplifiers and filters the transfer functions of each noise source distributed in the system to the output has to be determined (i. e. the output referred noise for a given noise source), and the single contributions are added up in quarature for statistically independent noise sources. In the more general case of statistically dependent noise sources the total output noise voltage is determined according to eq. (4.8) (for the case of two sources)

$$\sigma_{tot}^2 = \sigma_1^2 + \sigma_2^2 + 2\sigma_1\sigma_2 \operatorname{corr}(1,2) \tag{4.8}$$

where corr(1,2) denotes the correlation coefficient of the noise sources.

Since usually the system noise has to be compared to an input signal, the output noise

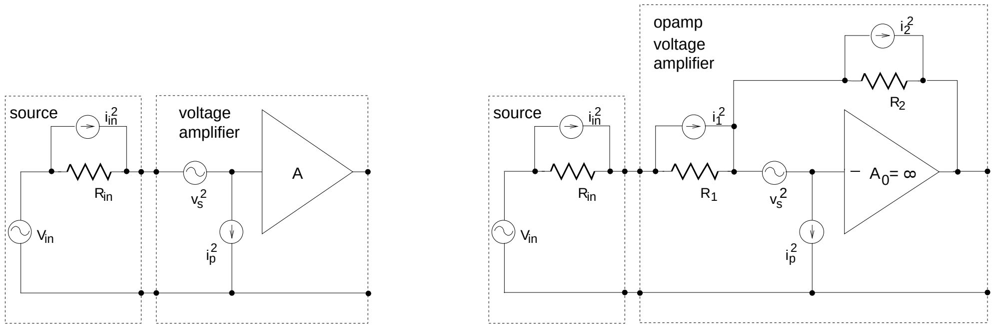


Figure 4.3: Left: signal source and idealized voltage amplifier; right: source and voltage amplifier built around an open loop gain cell (equivalent to an opamp-circuit with the noninverting input grounded)

is calculated back to the input by dividing the output noise with the signal transfer function - thus signal and noise can immediately be compared.

In the following, unless otherwise noted, v^2, i^2 und q^2 will always denote the spectral quantities $w(\nu)$, $w_i(\nu)$ and $w_q(\nu)$ (units V^2/Hz, A^2/Hz C^2/Hz) referred to the input.

4.2 Voltage Amplifier

4.2.1 Resistive Source Impedance

Voltage amplifiers with resistive sources (fig. 4.3) are commonly discussed in text books and are widely used in practice. A signal source V_{in} with source impedance delivers a voltage which is amplified by the idealized voltage amplifier on the left hand side in fig. 4.3 with the two noise sources v_s^2 and i_p^2 (see sect. 4.1). For an infinite input impedance the output voltage is trivially given by

$$V_{out} = AV_{in} \quad . \tag{4.9}$$

V_{out} output voltage
V_{in} signal voltage
A amplification

The (spectral) input equivalent noise voltage v_{ineq}^2 can be calculated in a strictly forward manner to be

$$v_{ineq}^2 = R_{in}^2(i_{in}^2 + i_p^2) + v_s^2 = 4kTR_{in} + R_{in}^2 i_p^2 + v_s^2 \quad [\text{in } \mathrm{V}^2/\mathrm{Hz}] \quad . \tag{4.10}$$

v_{ineq} equivalent noise voltage (in $\mathrm{V}/\sqrt{\mathrm{Hz}}$)
v_s (in $\mathrm{V}/\sqrt{\mathrm{Hz}}$), i_p (in $\mathrm{A}/\sqrt{\mathrm{Hz}}$) input noise voltage/current of amplifier
R_{in} signal source impedance
$k = 1,38 \cdot 10^{23}\mathrm{J/K}$, T absolute temperature

The first term describes the thermal noise of the source impedance. The last two terms are due to the amplifier's noise sources and can be influenced by proper choice of the voltage noise v_s^2 and the current noise i_p^2 (i. e. by selection of an opamp or by design of an appropriate amplifier); usually one chooses $v_s^2 = R_{in}^2 i_p^2$ so that the serial voltage noise equals the parallel noise current's voltage drop at R_{in}; due to the summation of the contributions in quadrature the reduction of only one out of v_s or i_p is not sufficient. It is obvious that the source impedance R_{in} determines the fundamentally achievable noise limit, both by its own thermal noise and indirectly by the voltage drop of i_p.

The right hand side of fig. 4.3 shows a practical voltage amplifier built around an ideal open loop gain cell (i. e. an inverting amplifier with gain ∞ without any phase degradation, or in other words, an ideal opamp with the noninverting input on ground). It should be emphasized that the opamp-circuit in inverting configuration *loads* the input voltage with the resistance R_1 thus introducing a dependency on the source impedance R_{in}, yielding for the gain (notation as in fig. 4.3 on the right)

$$V_{out} = -\frac{R_2}{R_{in} + R_1} V_{in} \quad . \tag{4.11}$$

Therefore, for delicate source voltages usually the non-inverting configuration is preferred to the inverting amplifier of fig. 4.3. The (spectral) input equivalent noise voltage v_{ineq}^2 becomes

$$v_{ineq}^2 = 4kT(R_{in}+R_1+\frac{(R_{in}+R_1)^2}{R_2})+(R_{in}+R_1)^2 i_p^2+v_s^2(1+\frac{R_{in}+R_1}{R_2})^2 \quad [\text{in V}^2/\text{Hz}] \quad . \tag{4.12}$$

The first term describes the thermal noise of the resistors (with the newly-added resistors R_1 and R_2); the last two terms are due to the amplifier noise sources v_s^2 und i_p^2; compared to eq. (4.10) the voltage drop of i_p at R_1 and a contribution of v_s due to the feedback have to be added.

If an opamp with a differential input stage is used for the above open loop amplifier, the noninverting input's noise sources have to be taken into account, yielding an additional term v_s^{+2} in eq. (4.12). Consequently, when designing amplifiers in very noise critical environments, a differential stage is not advisable; in discrete circuits a separate input transistor can be inserted in front of the opamp delivering enough preamplification to render the opamp noise negligible; since the noise of the noninverting input is not relevant for the principle to be discussed, it will be omitted in the following.

4.2.2 Resistive and Capacitive Source Impedance

A very tutorial example to consider is the voltage amplifier with a resistive and capacitive input signal (fig. 4.4) [Zwi87]. For the sake of simplicity the ideal voltage amplifier of fig. 4.3 has been used again for this calculation.

The voltage gain becomes

$$V_{out} = \frac{A}{1 + j\omega R_{in} C_{in}} V_{in} = \frac{A}{1 + j\omega \tau_{RC}} V_{in} \tag{4.13}$$

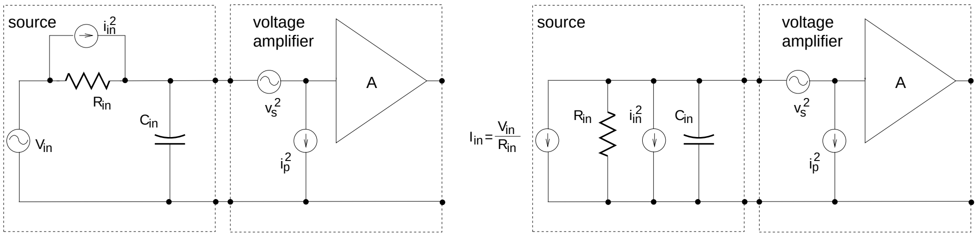


Figure 4.4: Left: voltage amplifier with resistive and capacitive signal source; right: the voltage source has been transformed into a current source.

i. e. the input signal sees a low pass as intuitively would have been expected. For completeness we give eq. 4.13 in the time domain (a description of the convolution function is given in the next chapter):

$$V_{out}(t) = \int_{-\infty}^{\infty} A e^{-\tau/\tau_{RC}} V_{in}(t-\tau)\, d\tau \tag{4.14}$$

The input equivalent noise amounts to

$$v_{ineq}^2 = 4kTR_{in} + R_{in}^2 i_p^2 + v_s^2 |1 + j\omega R_{in} C_{in}|^2 \quad [\text{in V}^2/\text{Hz}] \quad . \tag{4.15}$$

The contributions of the signal impedance's thermal noise and the parallel noise current source remain unchanged but the serial voltage contribution rises with frequency - this is due to an effect which is called "gain peaking" which will reappear when discussing the current amplifier. Gain peaking can simply be explained by different bandwidths for V_{in} and v_s; V_{in} sees a lowpass whereas v_s sitting directly on the amplifier input sees the full amplifier bandwidth for not too low frequencies.

Bandwith limitation in order to decrease noise should therefore always be applied after the first amplifier stage.

4.2.3 Charge Measurement with a Voltage Amplifier

A voltage amplifier can be also used for measuring charge by simply collecting the charge on a capacitor (e. g. the detector capacitance) and measuring the resulting voltage (fig. 4.4). The amplifier's input impedance is assumed to be infinite; since the source impedances of radiation detector systems are usually large, we transform the voltage source into its Thevenin's equivalent (fig. 4.4 right).

If discharging of C_{in} via R_{in} is too slow, a reset switch or a smaller discharge resistor has to be implemented to restore the baseline again. The problem of pulse pile up will be treated in greater detail in section 4.4.2 when we discuss the dedicated charge amplifier's application to silicon strip detectors.

The transfer voltage for the system given in fig. 4.4 (not accounting for the discharge) is given by

$$V_{out} = -\frac{A \int I_{in} dt}{C_{in}} = -\frac{A Q_{in}}{C_{in}} \quad . \tag{4.16}$$

It should be noted here that the output voltage depends on the value of C_{in}, which is not very well defined in general. The input equivalent noise, now given in units of charge, can be easily calculated to be

$$q_{ineq}^2 = 4kT \frac{1}{R_{in}|j\omega|^2} + \frac{i_p^2}{|j\omega|^2} + v_s^2 C_{in}^2 \quad [\text{in C}^2/\text{Hz}] \quad . \tag{4.17}$$

The first terms with the $1/|j\omega|^2$ dependency are often referred to as parallel noise - this will be discussed in greater detail in section 4.4. The last term denotes the serial noise contribution which is proportional to C_{in}^2. When comparing eq. (4.17) to eq. (4.24) it is worth to notice that the serial noise does not depend on the feedback capacitance C_{fb} as is found in the corresponding expression of the charge amplifier since it does not exist in the voltage amplifier design. The voltage amplifier accordingly offers an advantage for small input capacitances (e. g. the CCD readout makes use of a voltage amplifier [Dam81, Dam83]).

4.3 Current Amplifier

4.3.1 Resistive and Capacitive Source Impedance

A widely used method to measure currents uses the voltage drop of the current measured across a resistor (often called shunt). However, the drawback of this method is the dependency on the value of the source impedance (in general $R_{in}||C_{in}$), being the larger, the bigger the used shunt is. Therefore, shunts larger than 50 Ω are hardly ever used.

Fig. 4.5 shows a current amplifier (also called transconductance amplifier), which features (given an ideal open loop amplifier) an optimum input impedance of 0 Ω. Parallel impedances are then shortend and the entire signal current flows into the current amplifier being guided away over the feedback resistor. The source is modelled as a current source with the (parallel) resistive and capacitive source impedances R_{in} and C_{in} (the dashed encircled noise current source i_{sn}^2 denotes the shot noise of a photodiode's leakage current; this will be dicussed in the example later).

The current amplification is simply given by

$$V_{out} = -R_{fb} I_{in} \quad . \tag{4.18}$$

The input equivalent noise is given according to the amplifier's nature as a current noise (notations refer to fig. 4.5):

$$i_{ineq}^2 = 4kT \frac{1}{R_{fb}||R_{in}} + i_p^2 + \frac{v_s^2}{|(R_{fb}||R_{in}||\frac{1}{j\omega C_{in}})|^2} \quad [\text{in A}^2/\text{Hz}] \quad . \tag{4.19}$$

The first term denominates the thermal noise of the resistances, the following terms describe the noise caused by the amplifier noise sources at the input. The reader should

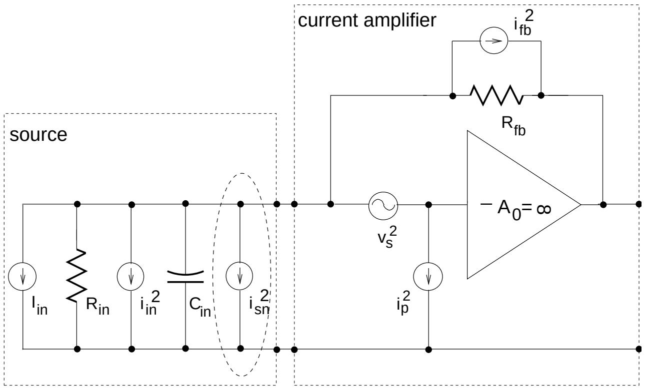


Figure 4.5: Current amplifier; the source is modelled as an ideal current source with a resistive and capacitive output impedance in parallel. i_{sn}^2 denominates the shot noise of a photodiode's leakage current.

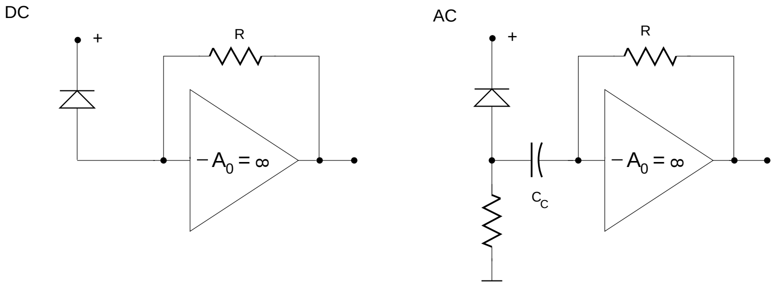


Figure 4.6: DC/AC-coupled photodiodes

note, that the input capacitance does not lower the noise by filtering, but that the v_s term increases with frequency due to the denominator which diverges for $\nu \to \infty$, because $\frac{1}{j\omega C_{in}}$ dominates the resulting value of the parallel impedances. In practice, this effect can often be neglected due to limitied bandwith of the used opamp (stability!).

4.3.2 Example: Photodiodes

Photodiodes are generally read out with current amplifiers [Grae95, Rein93, Rein96], since the generated photocurrent is directly proportional to the number of incident (better: absorbed) photons. The mechanism of photocurrent generation in photodiodes equals the one in silicon strip detectors; a detailed discussion has been given in chapter 2. In fast sensor applications the circuits depicted in fig. 4.6 are mostly employed. Using DC-coupling the photocurrent flows directly into the amplifier; when applying AC-coupling the current flows over a couple capacitor. In the case of DC-coupling the resistor R_{in} in fig. 4.5 is infinite, in case of AC-coupling R_{in} equals the bias resistor. Thus, the DC-coupling is the implementation with a lower noise, but leakage currents cause amplifier offsets with the danger of a limitation of the dynamic range.

The small signal equivalent circuit of the photodiode exhibits an additional parallel noise

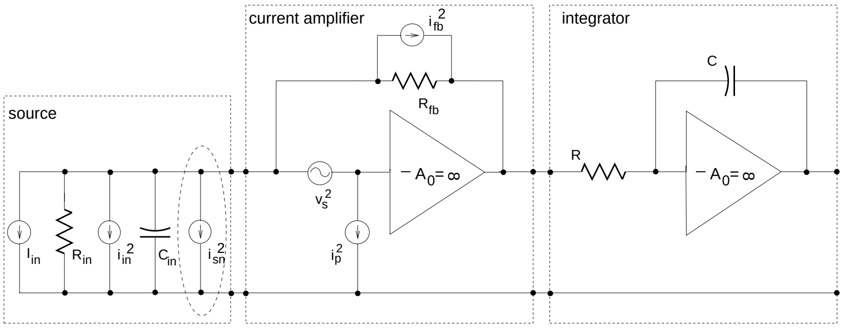


Figure 4.7: Current amplifier with subsequent integrating stage

current source i_{sn}^2 (fig. 4.5) for the shot noise of the diode leakage current (also called dark current).

For DC-coupling the input equivalent current noise equals

$$i_{ineq}^2 = 4kT\frac{1}{R_{fb}} + i_{sn}^2 + i_p^2 + \frac{v_s^2}{|(R_{fb}||\frac{1}{j\omega C_{in}})|^2} \quad [\text{in A}^2/\text{Hz}] \tag{4.20}$$

with

$i_{sn}^2 = 2qI$ shotnoise of the diode's leakage current I

As mentioned before, the diode capacitance C_{in} is of big importance since the last term in eq. (4.20) increases with frequency. Therefore, low noise voltage opamps should be employed in general for use with high capacitance diodes.

4.3.3 Charge Measurement with a Current Amplifier

A current amplifier can be used in order to measure charge by using a second voltage integrating stage behind the transimpedance amplifier (fig. 4.7).

The output voltage behind both stages is given by

$$V_{out} = -\frac{R_{fb}}{RC}\int I_{in}dt = -\frac{R_{fb}}{RC}Q_{in} \tag{4.21}$$

and is independent of the input capacitances (this is again due to the zero input impedance). The input equivalent noise assuming the integrating stage to be noiseless can be calculated to be

$$q_{ineq}^2 = 4kT\frac{1}{(R_{in}||R_{fb})|j\omega|^2} + \frac{i_p^2}{|j\omega|^2} + \frac{v_s^2}{R_{fb}^2|j\omega|^2} + v_s^2C_{in}^2 \quad [\text{in C}^2/\text{Hz}] \quad . \tag{4.22}$$

When comparing eq. (4.22) to eq. (4.24) we notice that the term $v_s^2C_{fb}^2$ has been replaced by $\frac{v_s^2}{R_{fb}^2|j\omega|^2}$, i. e. a serial noise contribution in case of the pure charge amplifier has become a parallel one. However, this term usually can be neglected w. r. t. the first term (thermal noise of R_{in} and R_{fb}). On the other hand, due to the gain constraint R_{fb} can often not

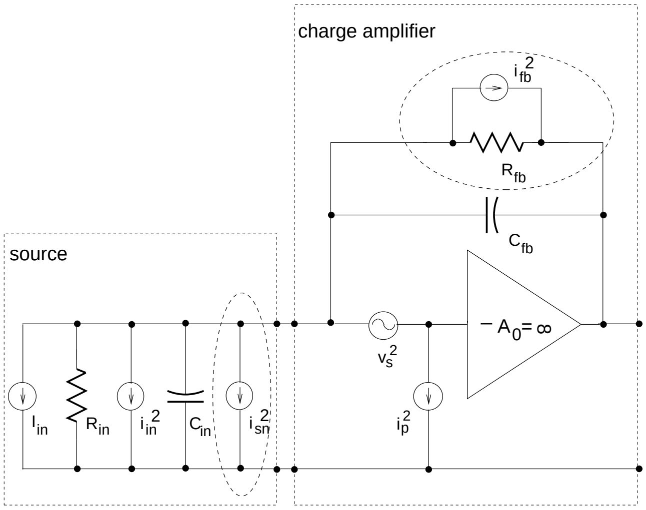


Figure 4.8: Idealized charge amplifier with source (capacitive and resistive output impedance); in a real world circuit the encircled noise sources have to be added.

be chosen as big as usual parallel resistances are, so that the parallel noise increases as compared to a pure charge amplifier solution.

Hence no obvious advantage of this concept as compared to the conventional charge amplifier (sect. 4.4) can be encountered. Current amplifiers used to measure charge have lately been presented in high energy physics [Dab94, Jar96, RD2-93] - often in combination with bipolar input stages; bipolar transistors exhibit a larger transconductance g_m causing lower values of the noise voltage source v_s; the base current shot noise which has to be taken into account as a parallel noise current source is overlayed by the noise of the feedback resistor. The reason is that for very small shaping times of $\tau < 20$ ns (see next section) the noise penalty due to the parallel noise is small, but the space consumption of a bipolar input transistor is considerably less than that of an optimum matched MOS transistor.

A detailed investigation of current amplifiers together with bipolar input transistors is given in chapt. 7.

4.4 Charge Amplifier

4.4.1 Parallel Resistive and Capacitance Source Impedance

A "quick and dirty" method to measure charge is to simply collect the charge on a capacitor and measure the voltage $V = Q/C$ (see section 4.2.3) . This method, however, depends on the value of the signal capacitance C_{in}, since a charge division takes place between signal capacitance and measuring capacitor. The circuit shown in fig. 4.8 avoids this drawback. By using a capacitor in the feedback of an open loop amplifier the input node stays - like in the case of the current amplifier - "virtually" on ground potential, or in other words, the input impedance is 0 Ω (better: $C_{in} = \infty$ F). Thus, all the charge delivered by the source is "drawn" onto C_{fb}, and, since the capacitor's left side potential is kept fixed, the voltage due to the charged feedback capacitor can be obtained at the output.

For the transfer functions holds

$$V_{out} = -\int I_{in} dt / C_{fb} = -Q_{in}/C_{fb} \quad . \tag{4.23}$$

As in the previous section the source is modelled as a current source with parallel resistive and capacitive impedance (in semiconductor detectors a parallel current noise source i_{sn} has to be added in analogy to the photodiode case). Strictly speaking the circuit depicted in fig. 4.8 is not stable - the output response to a δ like current input pulse will be a voltage step (without ever returning to the baseline). Therefore, in general a reset switch across the feedback capacitor, which is periodically closed, or a big resistor which steadily discharges the capacitor are used (the latter drawn in fig. 4.8 enclosed by a dashed circle). Both approaches introduce drawbacks: A switched charge amplifier suffers from serial noise (see sect. 6.1.1) and introduces dead time (in other words, it must be known when the pulses arrive), employing a discharge resistor causes extra parallel noise and the problem of pulse stacking, when a previous pulse has not completely decayed (refer to section 4.4.2).

The input equivalent noise is given in units of charge and amounts for the configuration shown in fig. 4.8 (without the encircled components) to

$$q_{ineq}^2 = 4kT \frac{1}{R_{in}|j\omega|^2} + \frac{i_p^2}{|j\omega|^2} + v_s^2 (C_{in} + C_{fb})^2 \quad [\text{in } \mathrm{C}^2/\mathrm{Hz}] \quad . \tag{4.24}$$

The first two terms (also called parallel noise) are due to the parallel noise current sources and exhibit a strong increase at low frequencies ($1/\nu^2$); the contribution due to the serial voltage noise source (often called the serial noise) increases proportional to the square of the input capacitance (by taking the square root of eq. (4.24) we get the "famous" C proportionality of the serial noise)

4.4.2 Example: Radiation Detectors

A classical field for the application of charge sensitive amplifiers is the detection of x- or γ-photons and ionizing particles (e. g. fast electrons, ions etc.) with semiconductor or gaseous detectors. The current pulses generated in silicon strip detectors (see chapter 2) by ionizing particles are δ-shaped with pulse widths of approx. 10 nanoseconds [Ru94], whereas gas detectors resp. proportional counters have a much larger time-distribtion easily extending into the μs-regime [Kno97].

Taking into account the shot noise of the detector leakage current noise and the thermal noise of the feedback resistor (fig. 4.8) the spectral input equivalent noise charge becomes

$$q_{ineq}^2 = 4kT \frac{1}{(R_{fb}||R_{in})|j\omega|^2} + \frac{i_{sn}^2}{|j\omega|^2} + \frac{i_p^2}{|j\omega|^2} + v_s^2 (C_{in} + C_{fb})^2 \quad [\text{in } \mathrm{C}^2/\mathrm{Hz}] \quad . \tag{4.25}$$

In chapters 2 and 3 the silicon strip detectors of the silicon vertex detector (SVD) and the microstrip gas chambers of the inner tracker detector of the HERA-B experiment have been outlined as prototypes of position sensing elementary particle detectors. These

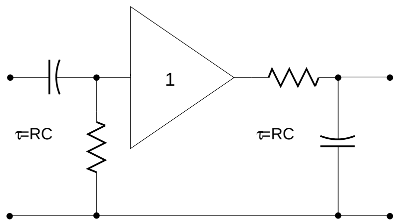


Figure 4.9: CR-RC-band pass filter which forms ("shapes") the signals behind the charge amplifier

detectors with strip readout pitches of 50 μm resp. 200μm can only be handled by integrated circuitry, whereas in a lot of other applications (e. g. spectroscopy) the space constraints are much more relaxed. Severe requirements are imposed on size, power consumption, and channel-to-channel homogenity for multi-channel readout electronics.

The feedback resistor R_{fb} (encircled with a dashed line in fig. 4.8) enables continous operation by steadily discharging the feedback capacitor causing the amplifier output to return to the baseline; thus, the resulting output signal does not equal strictly the integral of the input current (fig. 4.10) anymore. This would not mean a major problem taking into account the nearly δ-shaped current pulses when sampling quickly after the voltage edge (it would look differently with current signals distributed in time).

However, provided, new charge pulses arrived during the discharge, the corresponding voltage step would sit on top of the previous one (fig. 4.10). If the amplitude was sampled directly at the amplifier output, its value would depend on history. On the other hand, the feedback resistor cannot be selected too small to minimize the discharge time $\tau = RC$ without deteriorating the parallel noise as becomes obvious from eq. (4.25).

Therefore, pulse shaping filters are employed (other methods are discussed in chapt. 6) which transform the signals delivered by the charge amplifier into well defined and time limited pulses w. r. t. the expected rate.

Limitation of the output pulses in time and filtering the noise spectrum ($1/\nu^2$ behaviour of the parallel noise) require the use of a high pass filter (i. e. supression of low frequencies), general bandwidth limitation leads to a low pass filter. Both requirements imply the use of a band pass. Another requirement in pulse technique is a linear phase-frequency relationship to avoid ringing (this is equivalent to a frequency constant group velocity); this is a peculiar property of Bessel-filters.

As a very simple band pass filter, which satisfies the Bessel filter condition, the CR-RC filter has become widely spread [Hal53, Rad88, Gou72]. It consists of a CR-high pass, followed by a buffer and a RC-low pass of the same time constant (see fig. 4.9). The high pass "detects" only the voltage steps, the background caused by earlier signals is suppressed. The step response in fig. 4.10 shows that CR-RC shaping yields the desired effects. It should be pointed out that the presented concept enables a *continous* operation of the system (i. e. no switching is required); however, the danger of saturation of the charge amplifier remains (depending on the value of the discharge resistor and the average signal rate), since the different pulses at the preamplifier output will still be stacked on top of each other.

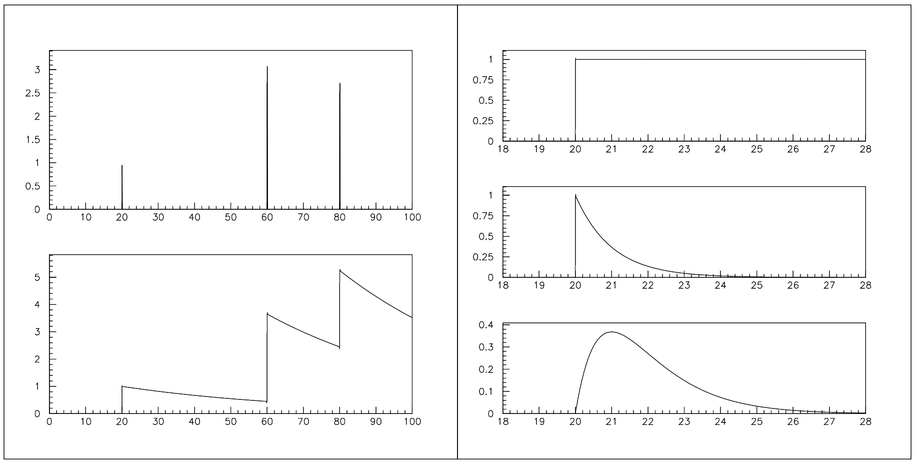


Figure 4.10: Left upper corner: current pulses delivered by a semiconductor detector; below: signal from output of charge amplifier with a large discharge resistor in the feedback; right from top to bottom: output pulse of charge amplifier, signal behind high pass, signal at CR-RC-filter output; the time axis in all pictures is divided in units of τ.

The pulse shape at the filter output is called semigaussian and follows the equation

$$V = V_{out}\frac{t}{\tau}e^{-t/\tau} = \frac{1}{C_{fb}}\frac{t}{\tau}e^{-t/\tau}Q_{in} \quad . \tag{4.26}$$

$\tau = RC$ time constant of high and low pass
V_{out} output voltage of charge amplifier
C_{fb} feedback capacitor of charge amplifier

The amplitude is directly proportional to the charge injected at the charge amplifier' s input.

The calculation of the spectral [in C^2/Hz] respectively the total [in C] input equivalent noise using a CR-RC filter will be performed in sect. 6.1.2 and 7.2; nevertheless it shall be reported here that there exists an optimum time constant τ for the CR-RC filter that minimizes noise. For this τ (noise corner time constant) which is in the μs-regime for usual silicon detectors the serial noise equals the parallel noise. Choosing the time constant bigger causes the total noise to increase due to the $1/\nu^2$-spectrum of the parallel noise even if the capacitance dependent serial noise diminishes (due to the summation in quadrature). The effect described is a peculiar property of a charge amplifier and contradicts intuition that longer measurement intervals should improve a result.

For the silicon strip detector described in chapter 2 with a strip capacitance of approx. 15pF noise values of 400 electrons ($6,4 \cdot 10^{-17}$ C) can be reached at room temperature with a filter time constant of 1μs; using cooled CCDs, as e. g. employed in astronomical applications noise values of 10 electrons due to the small input capacitance have been reported [Dam81].

In chapter 6 there will be detailed calculations and analysis of different signal processing concepts which are currently on the market including detailed comparison of advantages and drawbacks.

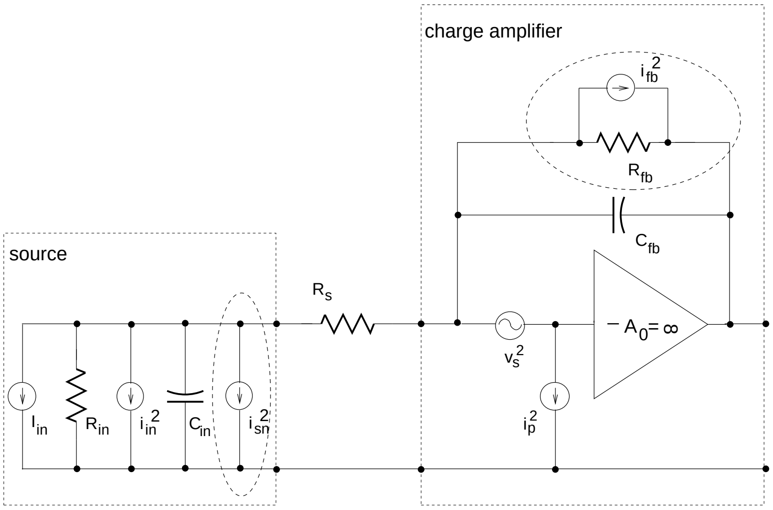


Figure 4.11: Charge amplifier with source (capacitive and resistive output impedance) and protection resistor; in a real world circuit the encircled noise sources have to be added.

4.4.3 Serial Resistive Source Impedance

In gaseous chambers which are usually operated at voltages of several hundreds of volts sparking between the high-voltage drift-electrode and the sensing electrodes (to which the amplifiers are connected) may happen from time to time. Due to the conducting channel in the gas the high voltage is shorted for a short while to the amplifier input which usually leads to destruction of the corresponding amplifier channel.

A series resistor in combination with protection-diodes (from the amplifier input to the chip's power rails) can be used as input protection. Unfortunately, the series resistor at the input node causes additional noise (see fig. 4.11).

Calculating the transfer function (neglecting the discharge resistor R_{fb}) yields

$$V_{out} = -\frac{1}{1+\frac{R_s}{R_{in}}}\frac{Q_{in}}{C_{fb}} + \frac{1}{1+\frac{R_s}{R_{in}}}\frac{1}{C_{fb}}\int_0^\infty e^{-\frac{\tau}{C_{in}(R_{in}||R_s)}} I_{in}(t-\tau)d\tau \quad . \tag{4.27}$$

Hence, the output signal does not equal exactly the total charge of the input current pulse anymore, but it also depends on the time behaviour of the input current. Eq. (4.27) can be interpreted such that a δ-current pulse charges the input capacitance at once (no charge arrives at the feedback capacitance and hence the output remains at the baseline) which discharges via the resistors R_{in} and R_s to ground and to the virtual ground input node of the charge amplifier, respectively. Only the current flowing through R_s contributes to the output voltage, thus explaining the deficit of the finally (after $t > 3(R_{in}||R_s)C_{in}$) reached voltage

$$V_{out} = -\frac{1}{1+\frac{R_s}{R_{in}}}\frac{Q_{in}}{C_{fb}} \quad . \tag{4.28}$$

Since usually $(R_{in}||R_s)C_{in} \approx$ ns falls in the range of the amplifier's internal rise time we neglect the integral term for the noise calculation. If we furthermore assume $R_{in} \gg R_s$

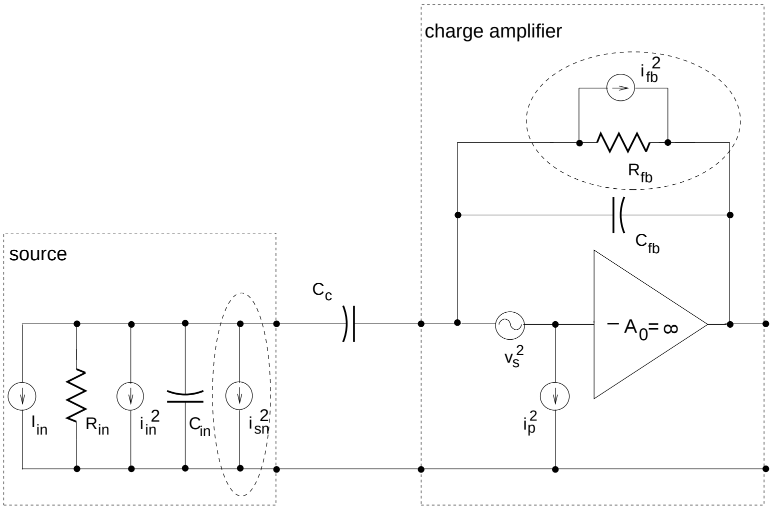


Figure 4.12: AC-coupled charge amplifier with source (capacitive and resistive output impedance); in a real world circuit the encircled noise sources have to be added.

(i. e. no charge deficit) we arrive at

$$q_{ineq}^2 = 4kT\frac{1}{R_{fb}|j\omega|^2} + \frac{i_p^2}{|j\omega|^2} + v_s^2(C_{in}+C_{fb})^2 + 4kTR_sC_{in}^2 \qquad [\text{in C}^2/\text{Hz}] \quad . \tag{4.29}$$

The last term in equation (4.29) indicates the contribution by the thermal noise of the series resistor. Since it transforms to the charge amplifier's output in practically the same manner as v_s^2 (in particular it contributes to the serial noise), the amplifier's serial noise voltage is often replaced by an "equivalent noise resistor" in literature to denote this contribution (see also next chapter). $4kTR_s$ should be lower than the amplifier's v_s^2 to avoid excess noise.

4.4.4 AC-Coupled Charge Amplifier

In the sections above only "DC-coupled" amplifiers with a galvanic (low ohmic) connection between source and amplifying device have been introduced; due to its widespread use we will in the following discuss the "AC-coupled amplifier" with a couple capacitor between source and amplifier. AC-coupled amplifiers do not suffer from leakage current induced baseline shifts (in a DC coupled charge amplifier a static input current creates a voltage drop $V_{out} = R_{fb}I_{leak}$ over the feedback resistor which is visible as offset output voltage). The voltage gain of the the configuration shown in fig. 4.12 is

$$V_{out} = -\frac{1}{1+\frac{C_{in}}{C_c}}\frac{Q_{in}}{C_{fb}} \quad . \tag{4.30}$$

Eq. (4.30) is similiar to eq. (4.28) indicating a charge deficit (which is due to the reduced input capacitance $= C_c$ of the AC-coupled charge amplifier); the total charge delivered by the source is distributed between C_{in} and C_c with the latter only contributing to the voltage output.

It is obvious from eq. (4.30) that the couple capacitance should be as large as possible to minimize the impact of the generally not well defined C_{in} on the system gain (this statements also holds true when taking into account the noise behaviour as discussed in the following). The input equivalent noise of the AC coupled amplifier (fig. 4.12) can be calculated to be

$$q_{ineq}^2 = 4kT\frac{1}{R_{in}|j\omega|^2} + \frac{(1+\frac{C_{in}}{C_c})^2}{|j\omega|^2}i_p^2 + v_s^2\Big[C_{fb}(1+\frac{C_{in}}{C_c}) + C_{in}\Big]^2 \quad [\text{in C}^2/\text{Hz}] \quad . \tag{4.31}$$

Eqs. (4.30) and (4.31) simplify to eqs. (4.23) and (4.24) when letting $C_c \to \infty$

We observe an increase of both the serial and parallel noise term due to the charge loss. In the MOSFET case where i_p^2 and v_s^2 are 100 % correlated (refer to eq. (B.4) on page 188) it is mainly the serial noise which increases. The parallel noise due to R_{fb} is not included in eq. (4.31); it is also scaled by the factor $(1+\frac{C_{in}}{C_c})^2$ and does not contribute significantly for peaktimes under the noise corner time constant.

For a bipolar input transistor it is mainly the parallel noise due to i_p^2 which increases following directly from eq. (4.31); i_p^2 is mainly determined by the base current shot noise.

Chapter 5

Analog Signal Processing - Basics

Many physical systems exhibit a linear and time independent correlation between input and output. These so called time invariant filters [1] can easily be described both in time and frequency-domain. Despite of the commonness of frequency based noise examination we will assess different pulse-processing methods on the market in chapter 6 using noise analysis in the *time*-domain; this is due to convenience since we partly will follow the literature [Ted94] but dealing with noise in the time-domain is also more intuitive in impulse technique since the pulse response $h(t)$ can directly be related to the noise performance of a system.

There are, however, filters with time-varying parameters which cannot be described by pulse response $h(t)$ anymore (which subsequently could be transformed into a transfer function in frequency-domain). Neither can the frequency-domain transfer characteristic be set up directly from the network elements.

An example for such a filter is the resetable charge amplifier where the reset effectively changes the transfer function of the system. In such cases, there is no way to circumvent the time-domain weighting function $w(\tau)$ (see definition 5.6, for time-invariant filters $w(\tau) = h(t - \tau)$) in order to assess the filter noise performance. The weighting function could be Fourier-transformed and noise analysis could be performed the usual way, but it is often simpler to stay in the time-domain and perform noise analysis here. We will treat the CR-RC-shaper in both formalisms in sect. 6.1.2 and sect. 7.2. to demonstrate the validity and ease of time-based noise assessment.

The perhaps most significant advantage of time based noise calculus is the ability to handle nonstationary periods (e. g. after switching on a circuit the "full" noise is not apparent immediately). Nonstationary phenomena, however, will not be exploited in the described filter architectures.

The most important drawback of time-domain calculation is that 1/f-noise cannot be handled. If 1/f-noise is supposed to be determined for a time-variant filter, the weighting function $w(\tau)$ has to be transfered into frequency domain and then the usual procedure has to be performed as mentioned above.

The content of this chapter bases largely on the theoretical work published in [Bal56, Bert96, Dav70, Gou72, Hin96, Rad64, Rad67, Rad88, Ted94, Ziel70] and especially on the summary given in [Sel96].

[1] by "filter" we understand amplifiers as well as filters in a narrow sense

5.1 Time Invariant Filters

For time invariant filters, the impulse response is a mere function of the time difference between the input signal and the output voltage, i. e. there exists no dependency on absolute time.

5.1.1 Frequency Domain

In his study of vibrating strings, Daniel Bernoulli (1700-1782) first used the idea that any periodic function can be represented as a series of harmonically related sinusoidal components. However, this analysis-technique was widely accepted only after Jean Fourier's publication in 1822 of his systematic study of such representations.

The idea of the Fourier transformation is the following [Mal86]: A time function is decomposed into a spectrum of periodical functions of the form $e^{j\omega t}$. When inputting such functions to linear systems, they will only by multiplied by a (complex) amplitude factor depending on the frequency ω. This can easily be seen from the following equation

$$g(t) = \int_{-\infty}^{\infty} e^{j\omega\tau} h(t-\tau)\, d\tau = \int_{-\infty}^{\infty} e^{j\omega(t-\tau)} h(\tau)\, d\tau = e^{j\omega t} \int_{-\infty}^{\infty} h(\tau) e^{-j\omega\tau}\, d\tau = e^{j\omega t} H(\omega) \quad . \tag{5.1}$$

The last term $\int h(\tau)e^{-j\omega t}\, d\tau$ depends only on frequency ω of the input function, and not on time t anymore. Thus, it can be rewritten as $H(\omega)$. In fact, $H(\omega)$ which is called the transfer function, is already the Fourier transform of $h(t)$. $H(\omega)$ can usually be calculated directly from the circuit network. As known from complex network theory the absolute value $|H(\omega)|$ describes the amplificaton of an input signal of frequency ω. $\tan\phi = \frac{\mathrm{Im}(H(\omega))}{\mathrm{Re}(H(\omega))}$ describes the phase shift introduced by the system.

The (exponential) Fourier transformation $\mathcal{F}$ is defined by eq. (5.2) and eq. (5.3):

$$\mathcal{F}(f(t)) = F(\omega) = \int_{-\infty}^{\infty} f(t) e^{-j\omega t}\, dt \tag{5.2}$$

$$\mathcal{F}^{-1}(F(\omega)) = f(t) = \frac{1}{2\pi} \int_{-\infty}^{\infty} F(\omega) e^{j\omega t}\, d\omega \tag{5.3}$$

In analogy to the treatment in the time-domain the transfer properties of a linear, time-invariant system can be expressed in the frequency domain by

$$G(\omega) = S(\omega) H(\omega) \quad . \tag{5.4}$$

$G(\omega)$ frequency spectrum at filter output

$S(\omega)$ signal frequency spectrum at filter input

$H(\omega)$ filter transfer function in frequency domain

We tacitly employed the Forier transform and the concept of frequency already in chapt. 4 where we discussed the noise performance of various amplifiers in the frequency domain.

5.1.2 Time Domain

Every signal $s(t)$ can be decomposed into a "spectrum" of δ-pulses with the weighting function $s(\tau)$ as shown in eq. (5.5). The integral in eq. (5.5) is also called a *convolution* integral with $s(t)$ convoluted with $\delta(t)$ (or vice versa).

$$s(t) = \int\limits_{-\infty}^{\infty} s(\tau)\delta(t-\tau)\,d\tau = \int\limits_{-\infty}^{\infty} s(t-\tau)\delta(\tau)\,d\tau \quad . \tag{5.5}$$

If the response of a linear, time invariant system to a δ-pulse is $h(t)$, the system output to $s(t)$ can be described by

$$g(t) = \int\limits_{-\infty}^{\infty} s(\tau)h(t-\tau)\,d\tau = \int\limits_{-\infty}^{\infty} s(\tau)w(\tau)\,d\tau \quad . \tag{5.6}$$

We denote the δ pulse response of the filter by $h(t)$; the corresponding *weighting function* is defined by $w(\tau) = h(t-\tau)$ and is a time reflected copy of $h(t)$ shifted by the time of observation t. Due to their related nature both terms are often used as synonyms in literature. We will try to notify the difference by the naming $h(t)$ resp. $w(\tau)$.

Eq. (5.4) should be compared to the convolution integral (5.6); the Fourier transformation transfers a convolution in the time domain into a simple product in the frequency domain.

We consider in the following *current* input signals $s(t)$ and *voltage* output signals $g(t)$ - thus the unit of $h(t)$ becomes $[\mathrm{F}^{-1}]$. The integral is carried out between $t = -\infty$ and ∞; however, for reasons of causality $h(t) = 0$ for $t < 0$; in a real system also $h(t) \to 0$ for $t \to \infty$ holds.

Fig. 5.1 illustrates equation (5.6) and the meaning of $h(t)$; we have added the noise sources found in a typical capacitive detector system; noise is introduced into the system due to three mechanisms (see also chapt. 4): parallel noise arises due to detector leakage shot-noise i_{sn}^2 and R_p's thermal noise (R_p summarizes all parallel resistors and the amplifier's parallel noise current source), serial noise is caused by the thermal noise of R_s (equivalent to amplifier's serial noise voltage according to eq. (4.29)).

Shot-Noise in the Time Domain

Devices with a voltage barrier like diodes behave as sources of current noise. In a diode the barrier allows current pulses in one direction with a Poisson distribution in time.

The derivation following is an illustrative interpretation of Carson's theorem [Ziel70]. A charge δq applied to the circuit at time τ produces an output voltage of $\delta q h(t-\tau)$ at time t where $h(t-\tau)$ describes the *current*-to-voltage response of the circuit (the input impedance is assumed to be 0 Ω). The output of the shot noise $s(\tau)$ source can be divided into time intervals of length $\delta\tau$, each with charge δq. To receive the total output voltage at time t, all the separate output voltage contributions δq produced by charges in the individual time intervals have to be summed. Of course δq differs for each interval.

To get an measure of the fluctuations of δq, it is assumed that within each interval $[\tau, \tau + \delta\tau]$ there are many charge pulses of size e (electron charge). There is a mean rate

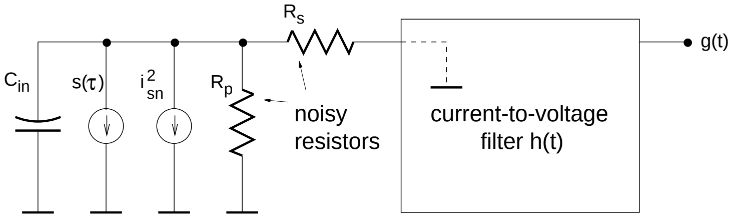


Figure 5.1: Filter with current-voltage transfer function $h(t)$; parallel noise arises due to detector leakage shot-noise i^2_{sn} and R_p's thermal noise, serial noise is caused by the thermal noise of R_s.

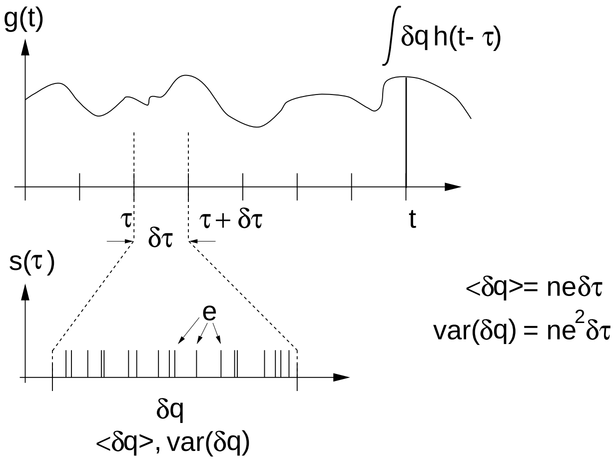


Figure 5.2: Shot noise originates from discrete charge carriers passing a "barrier" like a diode junction. The noise is viewed using a filter characterized by $h(t)$ resp. $H(\omega)$.

of n electrons/second so there will be an average of $n\delta\tau$ pulses per interval $[\tau, \tau + \delta\tau]$; the average charge in the interval will be $ne\delta\tau$.

The mean voltage at the ouput is given by integrating the mean charges with the appropriate weighting (with $ne = I_0$ mean current):

$$g(t) = \int_{-\infty}^{t_0} neh(t-\tau)\, d\tau = I_0 \int_{-\infty}^{t_0} h(t-\tau)\, d\tau \tag{5.7}$$

Eq. (5.9) describes the filter output voltage $g(t)$ at time t of a system switched on at t_0 (the upper integration limit can be set to ∞ since $h(t) = 0$ for $t < 0$. Hence the circuit behaviour can also be studied during the "warm up" of a circuit. For the stationary case, we have to set $t_0 = -\infty$ (in practice it would suffice to go back by Δt with $h(t) = 0$ for $t > \Delta t$).

However, we are more interested into the variance $(\text{var}\, g)(t)$. From Poisson statistics follows for the variance of δq

$$\text{var}\,(\delta q) = ne^2\delta\tau \quad . \tag{5.8}$$

By "propagating" the input variance to the output of the filter (taking into account that the variance is transformed by the square of the transfer function) we receive

$$(\text{var} g)\,(t) = (\sigma^2 g)(t) = \int_{t_0}^{\infty} ne^2 h^2(t-\tau)\, d\tau = \frac{1}{2}\,(2eI_0) \int_{t_0}^{\infty} h^2(t-\tau)\, d\tau \quad . \tag{5.9}$$

Frequently the integral (5.9) is expressed in the simplified but less instructive form by rearrangement of the integration range

$$(\sigma^2 g)(t) = \frac{1}{2}\,(2eI_0) \int_{\tau=-\infty}^{\tau=t-t_0} h^2(\tau)\, d\tau \quad . \tag{5.10}$$

To cross check eq. (5.9) with the value expected from frequency domain calculation we assume the stationary case setting the upper integration limit to ∞:

$$(\sigma^2\, g)(\infty) := \sigma^2\, g = \frac{1}{2}\,(2eI_0) \int_{-\infty}^{\infty} h^2(\tau)\, d\tau \tag{5.11}$$

By employing twice the inverse Fourier transformation (see sect. 5.1.1)

$$h(t) = \frac{1}{2\pi} \int_{-\infty}^{\infty} H(\omega) e^{j\omega t}\, d\omega \tag{5.12}$$

and going over to the unilateral spectral noise density we obtain

$$\sigma^2\, g = \frac{1}{2\pi}\,(2eI_0) \int_0^{\infty} |H(\omega)|^2\, d\omega = 2eI_0 \int_0^{\infty} |H(2\pi\nu)|^2\, d\nu \tag{5.13}$$

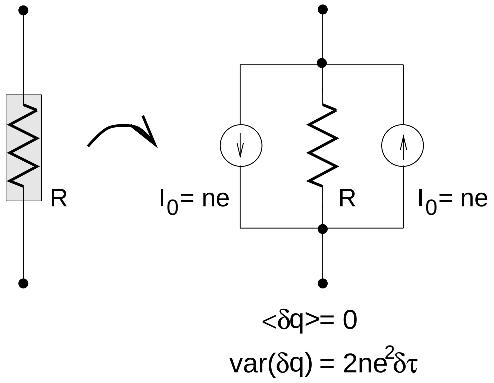


Figure 5.3: A (parallel) noisy resistor is modelled by a noiseless resistor with two antiparallel current sources with equal mean currents. The variance of charge per time slot $[\tau, \tau + \delta\tau]$ of each current source is $\mathrm{var}(\delta q) = ne^2\delta\tau$.

which is also known as Parseval's theorem [BS88]. Eq. (5.13) is exactly what we expect from the frequency domain calculation when feeding shot noise given by

$$\sigma^2\, i = \overline{i^2} - I_0^2 = 2qI_0\Delta\nu \qquad [\text{in A}^2] \tag{5.14}$$

into a filter with the current-voltage transfer function $H(\omega)$.

In order to calculate the response of a certain time invariant system to a noise source at the input, both equations (5.7) and (5.13) can be used.

Thermal Noise in the Time Domain

Thermal noise (see also sect. 4.1) is caused by the thermal motion of charge carriers in conductors/resistors. For the calculation of the system output noise in the time domain when connecting a resistor to the filter input, we apply the following model:

The thermal noise of a resistor R_p is modelled by two antiparallel current sources in parallel to the noiseless resistor, which have equal mean currents; the variance of charge per time slot $[\tau, \tau + \delta\tau]$ of each current source I_0 is $\mathrm{var}(\delta q_i) = ne^2\delta\tau$. Thus, the total variance of both current sources adds up to

$$\mathrm{var}(\delta q) = 2ne^2\delta\tau \quad . \tag{5.15}$$

The problem now is, that - since there is no DC current observable - we cannot determine the mean rate electrons/second n. By investigations on the thermal motion of charge carriers using statistical thermodynamics [John28, Nyq28] it can be shown that

$$n = \frac{kT}{Re^2} \tag{5.16}$$

$k = 1.38 \cdot 10^{23}$J/K, T absolute temperature
R resistance, $e = 1.6 \cdot 10^{-19}$ electron charge

and the variance at the filter output becomes

$$(\mathrm{var}\, g)(t) = (\sigma^2\, g)(t) = \int_{t_0}^{\infty} 2ne^2 h^2(t-\tau)\, d\tau = \frac{1}{2}\left(\frac{4kT}{R_p}\right)\int_{t_0}^{\infty} h^2(t-\tau)\, d\tau \quad . \tag{5.17}$$

Eq. (5.17) describes the noise for a parallel input resistor; in principle the resistor would have to be included in the weighting function $h(t)$; however, for a zero Ohm filter input impedance the resistor does not have any impact on the transfer characteristic $h(t)$.

For completeness the noise calculated with eq. (5.17) is cross checked with the noise from frequency domain study. We assume again the stationary case and rearrange the integration range as in eq. (5.10):

$$(\sigma^2 g)(t) = \frac{1}{2}\left(\frac{4kT}{R}\right)\int_{\tau=-\infty}^{\tau=t-t_0} h^2(\tau)\, d\tau \tag{5.18}$$

In the stationary case eq. (5.18) becomes

$$\sigma^2\, g = \frac{1}{2}\left(\frac{4kT}{R}\right)\int_{-\infty}^{\infty} h^2(\tau)\, d\tau \tag{5.19}$$

and from employing twice the inverse Fourier transformation we obtain

$$\sigma^2\, g = \frac{1}{2\pi}\left(\frac{4kT}{R}\right)\int_{0}^{\infty} |H(\omega)|^2\, d\omega = \frac{4kT}{R}\int_{0}^{\infty} |H(2\pi\nu)|^2\, d\nu \quad . \tag{5.20}$$

Eq. (5.20) thus is compatible with the Nyquist-formula (4.3)

$$\sigma^2 v = \overline{v^2} = 4kTR\Delta\nu \quad [\text{in V}^2] \quad \text{resp.} \quad \sigma^2 i = \overline{i^2} = \frac{4kT}{R}\Delta\nu \quad [\text{in A}^2] \quad .$$

In order to calculate the noise arising from a resistor R_s in *series* to the input of a network, we transfer the two current sources to two (noisy) antiparallel voltage sources of value $V_0 = R_s I_0 = R_s ne$ with n as defined in eq. (5.16) (see fig. 5.4).

The average of the two voltages cancels, but the variance of the voltage-time products per time slot becomes

$$R_s^2 \mathrm{var}(\delta q) = 2R_s^2 ne^2 \delta\tau \quad . \tag{5.21}$$

Equation (5.21) is the equivalent of eq. (5.15) and gives the variance in terms of resistance $\times$ charge resp. voltage $\times$ time which serves mathematically as input to a voltage-voltage transfer function.

Unfortunately, we only know the filter response to a (parallel) current input; therefore we have to calculate the system response for a voltage applied in series to the filter input. Taking into account the input capacitance C_{in}, a serial voltage source V_s causes a current

$$i_{in} = C_{in}\frac{dV_s}{dt} \tag{5.22}$$

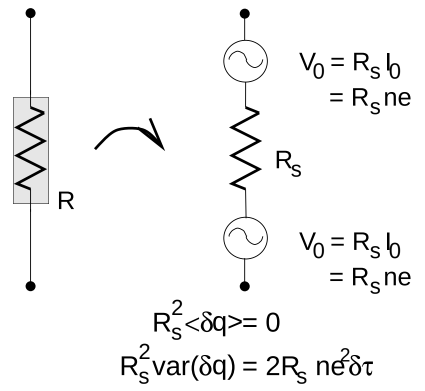


Figure 5.4: A (serial) noisy resistor is modelled by a noiseless resistor with two antiparallel voltage sources in series, which have equal mean voltages. The variance of the voltage-time products per time slot $[\tau, \tau + \delta\tau]$ of each voltage source is $R_s^2 \mathrm{var}(\delta q) = R_s^2 n e^2 \delta\tau$.

to flow into the "filter" $h(t)$ (neglecting the impact of R_s). In other words, a serial δ-voltage pulse causes a filter input current of $C_{in}\dot{\delta}(t)$.

For an arbitrary voltage V_s in series with the filter input we obtain for the voltage at the system output

$$\begin{aligned} g(t) &= \int_{-\infty}^{\infty} i_{in}(\tau) h(t-\tau)\, d\tau \\ &= \int_{-\infty}^{\infty} C_{in} \frac{dV_s}{d\tau}(\tau) h(t-\tau)\, d\tau \\ &= \Big[C_{in} V_s(\tau) h(t-\tau) \Big]_{\tau=-\infty}^{\tau=\infty} - \int_{-\infty}^{\infty} C_{in} V_s(\tau) \dot{h}(t-\tau)\, d\tau \\ &= -\int_{-\infty}^{\infty} C_{in} V_s(\tau) \dot{h}(t-\tau)\, d\tau \end{aligned} \tag{5.23}$$

The stem function term is assumed to be zero due to $h(-\infty) = h(\infty) = 0$ (which is generally true for real system).

Eq. (5.23) can be interpreted in such a way that $C_{in}\dot{h}(t)$ is the *voltage*-voltage-transfer function of a filter characterized by a *current*-voltage transfer function $h(t)$ with a capacitive input load C_{in}.

How does $R_s^2 \mathrm{var}(\delta q)$ propagate to the filter output ? Again we integrate over all relevant "voltage-time" products $R_s^2 \mathrm{var}(\delta q)$ between t_0 and t (resp. ∞):

$$(\mathrm{var}\, g)(t) = (\sigma^2\, g)(t) = \int_{t_0}^{\infty} C_{in}^2\, 2R_s^2 n e^2\, \dot{h}^2(t-\tau)\, d\tau \tag{5.24}$$

Substituting n from eq. (5.16) yields

$$(\mathrm{var}\, g)(t) = (\sigma^2\, g)(t) = \frac{1}{2} C_{in}^2\, (4kTR_s) \int_{t_0}^{\infty} \dot{h}^2(t-\tau)\, d\tau \quad . \tag{5.25}$$

Rearrangement of the integration range yields

$$(\sigma^2\, g)(t) = \frac{1}{2} C_{in}^2\, (4kTR_s) \int_{\tau=-\infty}^{\tau=t-t_0} \dot{h}^2(\tau)\, d\tau \tag{5.26}$$

and in the stationary case

$$\sigma^2\, g = \frac{1}{2} C_{in}^2\, (4kTR_s) \int_{-\infty}^{\infty} \dot{h}^2(\tau)\, d\tau \quad . \tag{5.27}$$

Refering to the discussion of the charge amplifier with series resistance in sect. 4.4.3 it becomes immediately clear that we can use formula (5.27) also for the description of the amplifier's inherent serial noise. The equivalent noise resistance is related to the input transistor's transconductance g_m via

$$R_{s,eq} = \frac{2}{3g_m} \quad . \tag{5.28}$$

To compare the result achieved in eq. (5.27) to a frequency domain analysis we have to take the derivative of the Fourier transform

$$\frac{dh}{dt}(t) = \frac{1}{2\pi} \int_{-\infty}^{\infty} j\omega H(\omega) e^{j\omega t}\, d\omega \tag{5.29}$$

and substitute it into eq. (5.27) yielding (after transition to the unilateral spectral noise density)

$$\sigma^2\, g = \frac{1}{2\pi}\, C_{in}^2\, (4kTR_s) \int_{0}^{\infty} |j\omega H(\omega)|^2\, d\omega \quad . \tag{5.30}$$

With the Fourier transform of eq. (5.22)

$$I_{in}(\omega) = j\omega C_{in} V_s(\omega) \tag{5.31}$$

and defining from this the voltage-voltage frequency response of the filter under consideration

$$H^{\circ}(\omega) := j\omega C_{in} H(\omega) \tag{5.32}$$

we obtain from eq. (5.30)

$$\sigma^2\, g = \frac{1}{2\pi}\,(4kTR_s)\int\limits_0^\infty |H^\circ(\omega)|^2\, d\omega = (4kTR_s)\int\limits_0^\infty |H^\circ(2\pi\nu)|^2\, d\nu \quad . \tag{5.33}$$

Eq. (5.33) describes the voltage noise at the filter output due to an input voltage noise $\sigma^2\, v = 4kTR_s\Delta\nu$, thus confirming our result from time domain calculation.

It should be noted again that the time domain eqs. (5.9), (5.17), and (5.25) are more general than the frequency domain equations obtained by application of Parseval's theorem since they cover nonstationary processes as well. The 1/f-noise (sect. 4.1), however, can only be handled for stationary processes.

5.2 Time Variant Filters

5.2.1 Frequency Domain

As already mentioned in the introduction to this chapter, the handling of the general time variant filter in the frequency domain looses its attractivity. The popularity of the frequency based method stems from the fact that using network theory the transfer function can immediately be deduced in frequency domain. This advantage, however, is lost with the general time variant filters, since now a filter can can be described only by the generalized weighting function $w(\tau)$ which will be introduced in the following subsection. Hence, a Fourier transformation always has to be performed, before the noise integral can be carried out. For non-white noises as 1/f-noise, this is the only method to calculate the noise performance of the filter.

Most of the pulse processing architectures (but not the resetable charge amplifier) discussed in chapter 6 can also be completely calculated in frequency domain since they rely only on single or multiple sampling of an otherwise time invariant filter [Kur96]. The phase difference between different samples on the same filter is accounted for by the phase factor $e^{-j\omega\Delta t}$ according to

$$\mathcal{F}(f(t-\Delta t)) = e^{-j\omega\Delta t}\mathcal{F}(f(t)) = F(\omega)e^{-j\omega\Delta t} \quad . \tag{5.34}$$

In the case where the above mentioned method cannot be applied and where the Fourier-integral exists - the weighting function $w(\tau)$ is usually absolutely integrable, i. e.

$$\int\limits_{-\infty}^{\infty} |w(\tau)|\, d\tau < \infty \tag{5.35}$$

it can be easier to use the tabular Laplace-transform to transfer the weighting function first and later substitute $s \mapsto j\omega$.

5.2.2 Time Domain

In the previous section on time invariant filters we characterized a system by its voltage response $h(t)$ to an input current pulse $\delta(\tau = 0)$. $w(\tau) = h(t-\tau)$ can immediately be used as *weighting* function for an input signal $s(\tau)$ (where t denotes the time of observation); often this pulse is sampled at a fixed time (e. g. at the pulse peak time $t = \hat{t}$). We want to generalize this concept now recalling the very fundamental meaning of a weighting function as described in section 5.1.2: The weighting function $h(t-\tau)$ describes the filter output $g(t)$ due to a δ-pulse ocurring at time τ. We replace the limited term "filter output" by "measurement value"; this becomes clear, if we think about the system transforming a δ-pulse to a measurement value as a rather complex one, including operations like switching, sampling, resetting, conventional filtering etc. .

It should be pointed out that in a general time variant filter the pulse response at the output can be quite different from the weighting function.

To illustrate the concept consider the following example (fig. 5.5) [Ted94]: A system consists of a continous filter with a triangular impulse response

$$[\mathrm{F}] \cdot h(t) = \begin{cases} \frac{t}{t_{top}} & : \quad 0 < t < t_{top} \\ 1 - \frac{t}{t_{top}} & : \quad t_{top} < t < 2t_{top} \\ 0 & : \quad \text{else} \end{cases} \quad . \tag{5.36}$$

The output of the "triangle" filter is integrated by a short time integrator from $t = 0$ to $t = T_{int}$ with $T_{int} = 2t_{top}$.

The integration value is the result $w(\tau)$ of the measurement. The overall weighting function can be determined graphically according to fig. 5.5 by moving the triangle origin from $\tau = -\infty$ to $\tau = +\infty$. The triangle area lying inside the integration period is the measurement value $w(\tau)$; $w(\tau)$ of course depends on the time of arrival τ of the δ-pulse.

The overall weighting function as plotted in fig. 5.5 is given by

$$[\mathrm{F\,s}] \cdot w(\tau) = \begin{cases} \frac{1}{2}\frac{(2t_{top}-\tau)^2}{t_{top}} & : \quad -2t_{top} < \tau < -t_{top} \\ \frac{1}{2}t_{top} + \frac{1}{2}\frac{\tau^2}{t_{top}} & : \quad -t_{top} < \tau < 0 \\ \frac{1}{2}t_{top} - \frac{1}{2}\frac{\tau^2}{t_{top}} & : \quad 0 < \tau < t_{top} \\ \frac{1}{2}\frac{(2t_{top}-\tau)^2}{t_{top}} & : \quad t_{top} < \tau < 2t_{top} \\ 0 & : \quad \text{else} \end{cases} \quad . \tag{5.37}$$

Noise

The noise behaviour of the time variant filter is calculated the same way as in the time invariant case: the impact of the $\mathrm{var}(\delta q)$ on the measurement value's variance $\mathrm{var}\, g$ has to be determined; the derivation can be carried out in analogy to subsection 5.1.2 by simply replacing $h(t-\tau)$ by $w(\tau)$. Thus, we can easily generalize the noise analysis to the time variant filter case. Furthermore, we will normalize $w(\tau)$ to the filter signal gain to directly give the input equivalent noise ENC (Equivalent Noise Charge) in [C] or [q] (elementary charge):

$$w_n(\tau) = \frac{w(\tau)}{w(\tau^{sig})} \quad [\text{unit } 1] \tag{5.38}$$

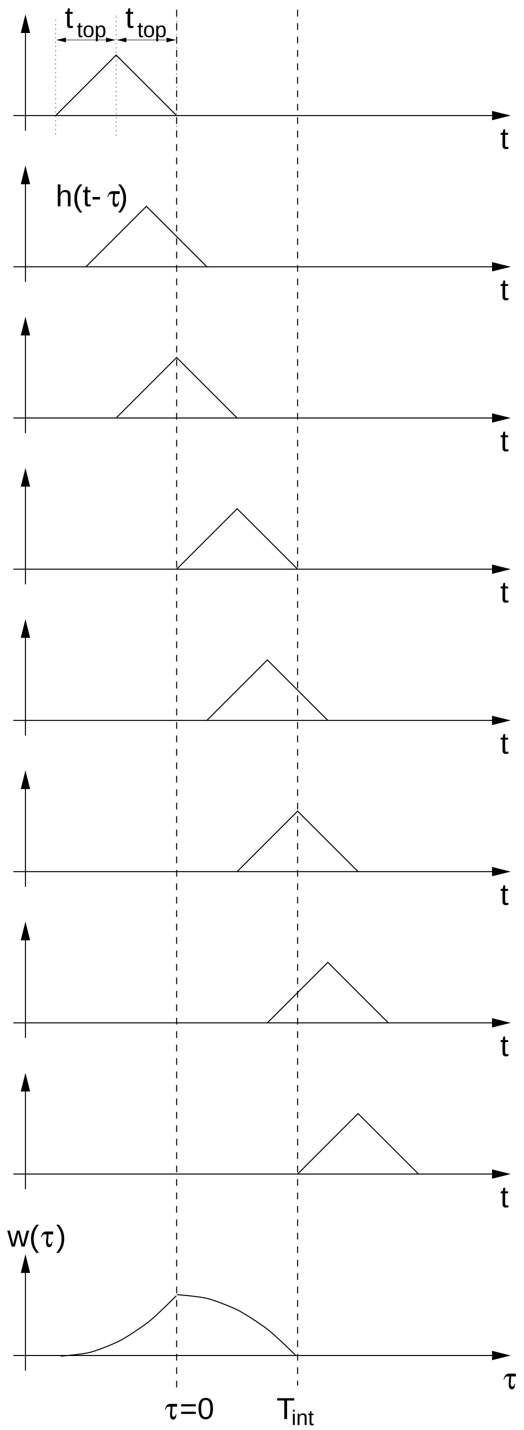


Figure 5.5: Time variant filter consisting of a time-invariant triangle-filter and a subsequent short time integrator. The overall weighting function (measurement function) is developed by determination of the triangle area lying inside the integration period [Ted94].

with $w(\tau^{sig})$ denoting the normalization factor given by the filter gain to a signal arriving at time τ^{sig}. In future we will omitt the subscript "n" and always refer to the normalized weighting function as described in eq. 5.38.

The parallel noise can be expressed to be

$$\mathrm{ENC}_p^2(t_0) = \frac{1}{2}\left(2eI_0 + \frac{4kT}{R_p}\right)\int_{t_0}^{\infty} w^2(\tau)\,d\tau \quad . \tag{5.39}$$

In the stationary case with the system switched on at $t_0 = -\infty$ we get

$$\mathrm{ENC}_p^2 = \frac{1}{2}\left(2eI_0 + \frac{4kT}{R_p}\right)\int_{-\infty}^{\infty} w^2(\tau)\,d\tau \quad . \tag{5.40}$$

The serial noise is obtained the same way

$$\mathrm{ENC}_s^2(t_0) = \frac{1}{2}C_{in}^2\,(4kTR_s)\int_{t_0}^{\infty} \dot{w}^2(\tau)\,d\tau \tag{5.41}$$

and for the stationary case holds

$$\mathrm{ENC}_s^2 = \frac{1}{2}C_{in}^2\,(4kTR_s)\int_{-\infty}^{\infty} \dot{w}^2(\tau)\,d\tau \quad . \tag{5.42}$$

Using the theoretical fundamentals developed in this chapter we will assess all (to the author's knowledge) of the currently applied pulse processing techniques in terms of their noise behaviour in the following chapter 6.

Chapter 6

Analog Signal Processing - Application to Impulse-Technique

The charge sensitive amplifier delivers a voltage step at the output in response to a δ-current pulse - in other words a finite (in time) excitation produces an infinite response in time. The most important task of any subsequent signal processing therefore is the transformation into a pulse of finite duration or - more generally - the convolution with a weighting function of finite duration. Furthermore, the processing architecture should not deteriorate the S/N-ratio as present behind the charge amplifier - we will see that this only can be fulfilled by the "optimum" pulse processing scheme discussed in sect. 6.4. The optimum pulse processing method is not realizable without some effort and time consumption; therefore in this chapter the noise performance of various signal processing architectures as employed in real world are discussed.

We will compare several methods evaluating single, double, and manifold sampling techniques with respect to their noise and rate behaviour. A time domain analysis will be used, which is more illustrative and general than the commonly employed frequency domain methods; however, most of the presented architectures can also be calculated completely in the frequency domain (by use of the phase factor $e^{-j\omega\Delta t}$). We will omit the 1/f-noise due to its vanishing impact at integration periods of less than 100 ns.

In the following we assume a single pole (i. e. a RC lowpass) behaviour for every amplifier stage with the exception of two pole systems as the CR-RC shaper architecture (which specifiy explicitely a slower time behavior). This is due to two reasons: First, as has been shown in chapter 5, the serial noise contribution is proportional to $\dot{w}^2(t)$; thus, in order to avoid squared δ-functions, the system response must not be instantaneous to an input signal. Secondly, in order to make a fair comparison of rate behaviour, we have to take into account the finite risetimes of the stages involved.

6.1 Single Sampling

6.1.1 Sampling at Charge Amplifier Output

Single sampling of the output of a resetable charge amplifier as described in sect. 6.1.1 is probably the simplest approach conceivable (see fig. 6.1). The reset-signal is released

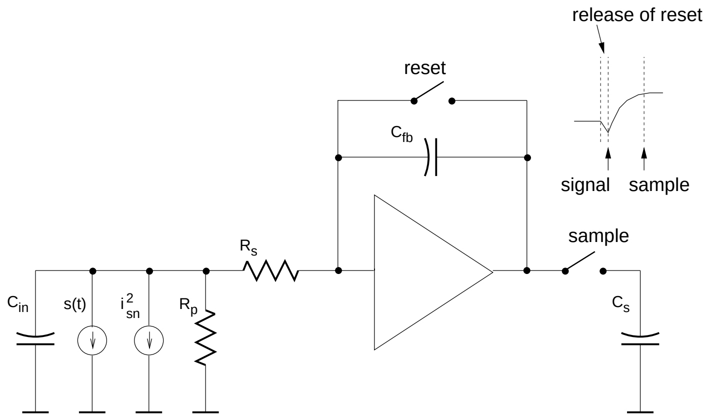


Figure 6.1: Single voltage sampling architecture: the charge amplifier output is sampled when it has reached 90% of the final value.

before arrival of the signal; the output voltage after the release of reset, however, suffers from strong variations as will be pointed out in the following.

The transition from the reset state to the active period is assumed to happen linearly during a short (w. r. t. τ_{amp}) time span Δt_{res} given mainly by the steepness of the digital reset signal. One can imagine that during this period the switch'es resistance is not zero yet, so that in the transition region a sensitivity to input signals persists. In principle the amplifier maintains a very limited sensitivity to input current even during reset ($V_{out} = I_{in}(R_{on}||1/(j\omega C_{fb}))$) - this will be neglected.

After the release of reset the current signal is integrated on the feedback capacitance; as response to a δ-pulse the amplifier output rises with a time constant τ_{amp}.

The weighting function $w(\tau)$ is given by

$$w(\tau) = \begin{cases} 1 + \frac{\tau}{\Delta t_{Res}} & : \quad -\Delta t_{Res} < \tau < 0 \\ \frac{1}{A}\left(1 - e^{-\frac{\tau - T}{\tau_{amp}}}\right) & : \quad 0 < \tau < T \\ 0 & : \quad \text{else} \end{cases} \tag{6.1}$$

and its derivative $\dot{w}(\tau)$ by

$$\dot{w}(\tau) = \begin{cases} \frac{1}{\Delta t} & : \quad -\Delta t_{Res} < \tau < 0 \\ -\frac{1}{A}e^{\frac{\tau - T}{\tau_{amp}}} & : \quad 0 < \tau < T \\ 0 & : \quad \text{else} \end{cases} \quad . \tag{6.2}$$

The normalization factor A equals

$$A = \left(1 - e^{-\frac{T}{\tau_{amp}}}\right) \quad . \tag{6.3}$$

In Fig. 6.2 $w(\tau)$ and $\dot{w}(\tau)$ are plotted where the signal is assumed to arrive at $t = 0$ immediately after the reset. We restricted the amplifier rise to 90% of the maximum end value; this is fulfilled for $T = 2.3\tau$.

The parallel noise using eq. (5.40) becomes

$$\begin{aligned}\mathrm{ENC}_p^2 &= \frac{1}{2}\left(2eI_0 + \frac{4kT}{R_p}\right)\int_{-\infty}^{\infty} w^2(\tau)\,d\tau \\ &= \frac{1}{2}\left(2eI_0 + \frac{4kT}{R_p}\right)\left[\frac{1}{3}\Delta t_{res} + \frac{1}{A^2}(-\frac{3}{2}\tau - \frac{1}{2}\tau e^{-2T/\tau}\right. \\ &\quad \left. +2\tau e^{-T/\tau} + T)\right] \qquad (6.4)\end{aligned}$$

If we let $\Delta t_{Res} \to 0$ and set $T = 2.3\tau_{amp}$ we obtain

$$\mathrm{ENC}_p^2 = \frac{1}{2}\left(2eI_0 + \frac{4kT}{R_p}\right) 1.230\,\tau_{amp} \quad . \qquad (6.5)$$

For the serial noise we obtain according to eq. (5.42)

$$\begin{aligned}\mathrm{ENC}_s^2 &= \frac{1}{2}C_{in}^2\,(4kTR_s)\int_{-\infty}^{\infty} \dot{w}^2(\tau)\,d\tau \\ &= \frac{1}{2}C_{in}^2\,(4kTR_s)\left[\frac{1}{\Delta t_{res}} + \frac{\tau}{2A^2}(1 - e^{-2T/\tau})\right] \\ &\xrightarrow{\Delta t_{res}\to 0} \infty \qquad (6.6)\end{aligned}$$

As we now can see from eq. (6.6) ENC_s^2 diverges for $\Delta t_{res} \to 0$! This result might be surprising, and it ought to serve as a warning of the naive employment of time variant filters (we regard the resetable charge amplifier already as filter) !

The result of eq. (6.6) follows directly from calculus; how can we understand the result by intuition ?

A serial voltage source delivers a "unit" current pulse of $C_{in}\dot{\delta}(t)$ into the low impedance amplifier input for an input capacitance C_{in} (refer to eq. (5.22) on page 65 and the following remark). $\dot{\delta}(t)$ can be imagined as a positive δ-pulse immediately followed by a negative one. When moving $\dot{\delta}(t)$-type pulses on the time axis, the filter response is always very strong when there is a large value of $\dot{h}(t)$ because the positive and the negative part of the dotted δ-pulse become amplified asymmetrically. Thus, the serial noise contribution is biggest for large $\dot{w}(t)$ whereas the parallel contribution is maximal for large $w(t)$. Having an infinitely fast rise in the transfer function makes the serial noise integral diverge. In other words after a fast reset the voltage at the amplifier output is quite uncertain. This is not the result of charge injections or other non-idealities but it follows directly from the amplifier's integrating property.

Other pulse-processing architectures discussed later (e. g. the double correlated sampling) may also feature a reset of the charge amplifier; however, they all "mask" the steep turn on edge of the charge amplifier awakening from the reset state in their transfer function.

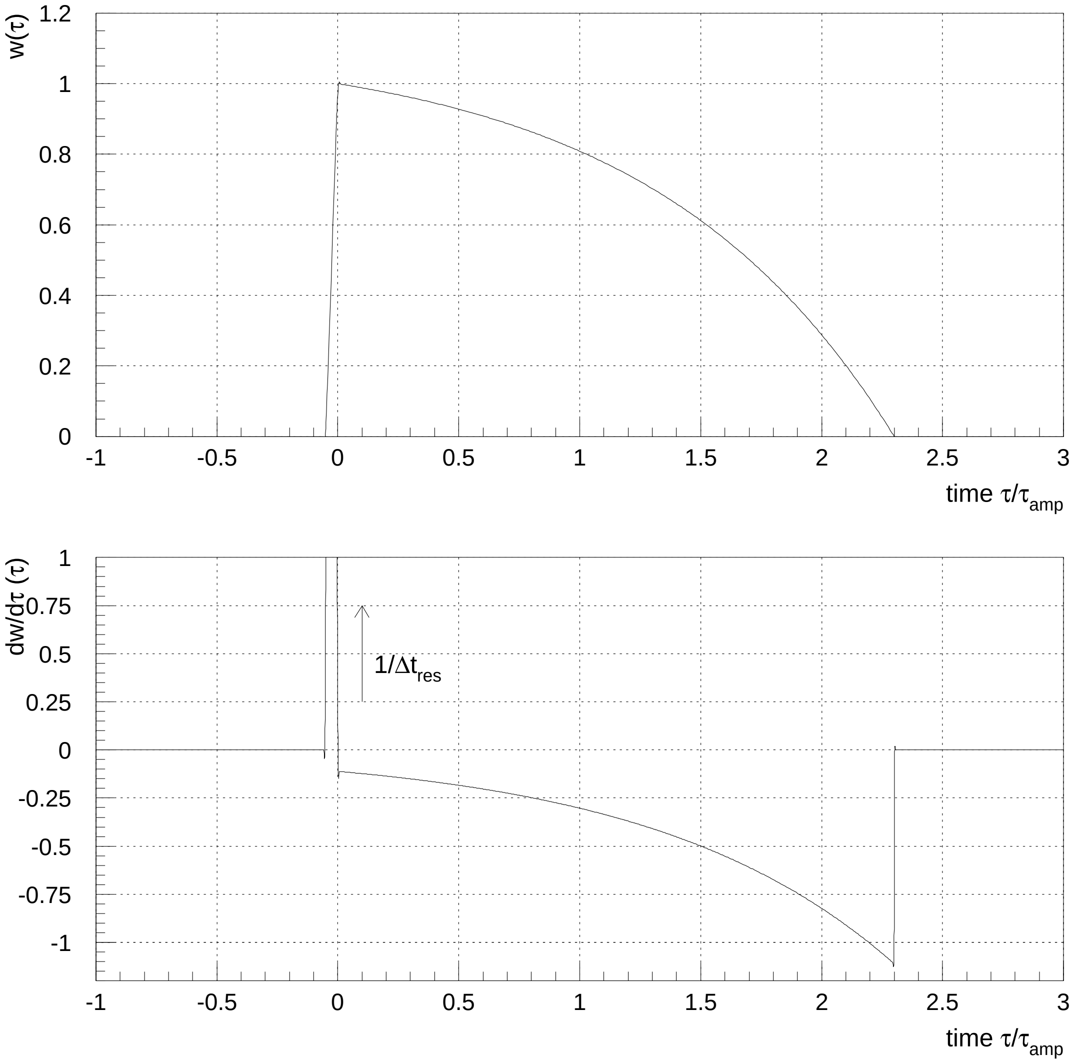


Figure 6.2: Weighting function $w(\tau)$ and its derivative $\dot{w}(\tau)$ vs. time τ of signal arrival for single voltage sampling with reset. For $\Delta t_{res} \to 0$ the dotted weighting function becomes infinite at $\Delta t_{res} < \tau < 0$.

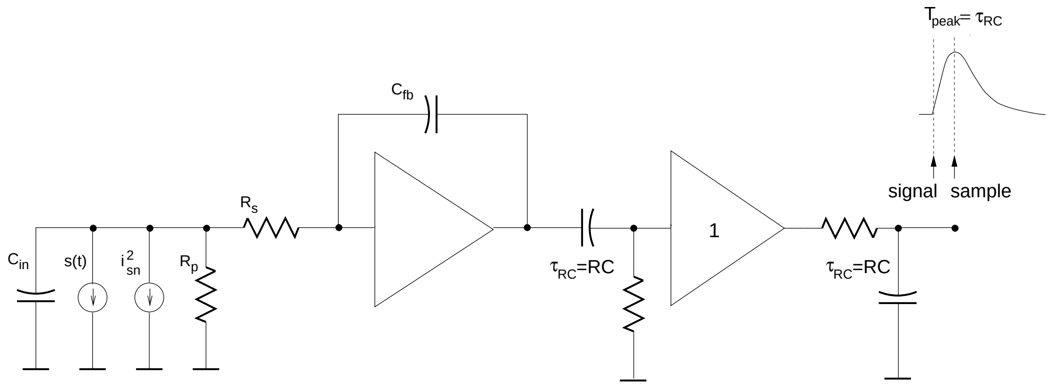


Figure 6.3: Single sampling at output of CR-RC-filter; sampling is performed at pulse peak.

In the HELIX128S-2 architecture a resetable charge amplifier is used for the readout of the pipeline. We will address its noise contribution to the overall system noise in the dedicated chapter 8.

6.1.2 Sampling at CR-RC Filter Output

CR-(RC)^n-filters are widely used with charge amplifiers for practically all purposes [Beu90, CS91, Com96, Nyg92, Hal53, Hu95, HN95, Kno97, Ort95]. A CR-(RC)^n-filter consists of a CR-high pass and n RC-low passes of the same time constant each separated from each other by an ideal buffer (see fig. 6.3 for $n = 1$).

CR-(RC)^n-filters satisfy the Bessel-filter condition $\phi(\omega) = \omega \cdot t$ with the phase-transfer function $\phi(\omega)$. This expresses that the filter transit time is independent from frequency (resp. the filter group velocity v_g is constant). Obviously the Bessel property is very important in impulse processing technique to avoid ringing. The normalized weighting function of a CR-(RC)^n filter is

$$w(\tau) = e^n \left(\frac{T_{peak} - \tau}{T_{peak}} \right)^n e^{-n(T_{peak}-\tau)/T_{peak}} \tag{6.7}$$

$T_{peak} = \tau_{RC}$ pulse peak time
$\tau_{RC} = RC$ time constant of high and low passes

which can be obtained from the impulse response by time reversal and positive shift of t as given in fig. 6.4.

A thorough evaluation of the noise behaviour of a semi gaussian shaper of arbitrary order n is given in [CS91]; parallel and 1/f-noise decrease with increasing filter order n, but the serial noise increases due to the steeper falling edge of the pulse. Consequently, an optimum shaper filter order exists for a given detector and amplifier configuration.

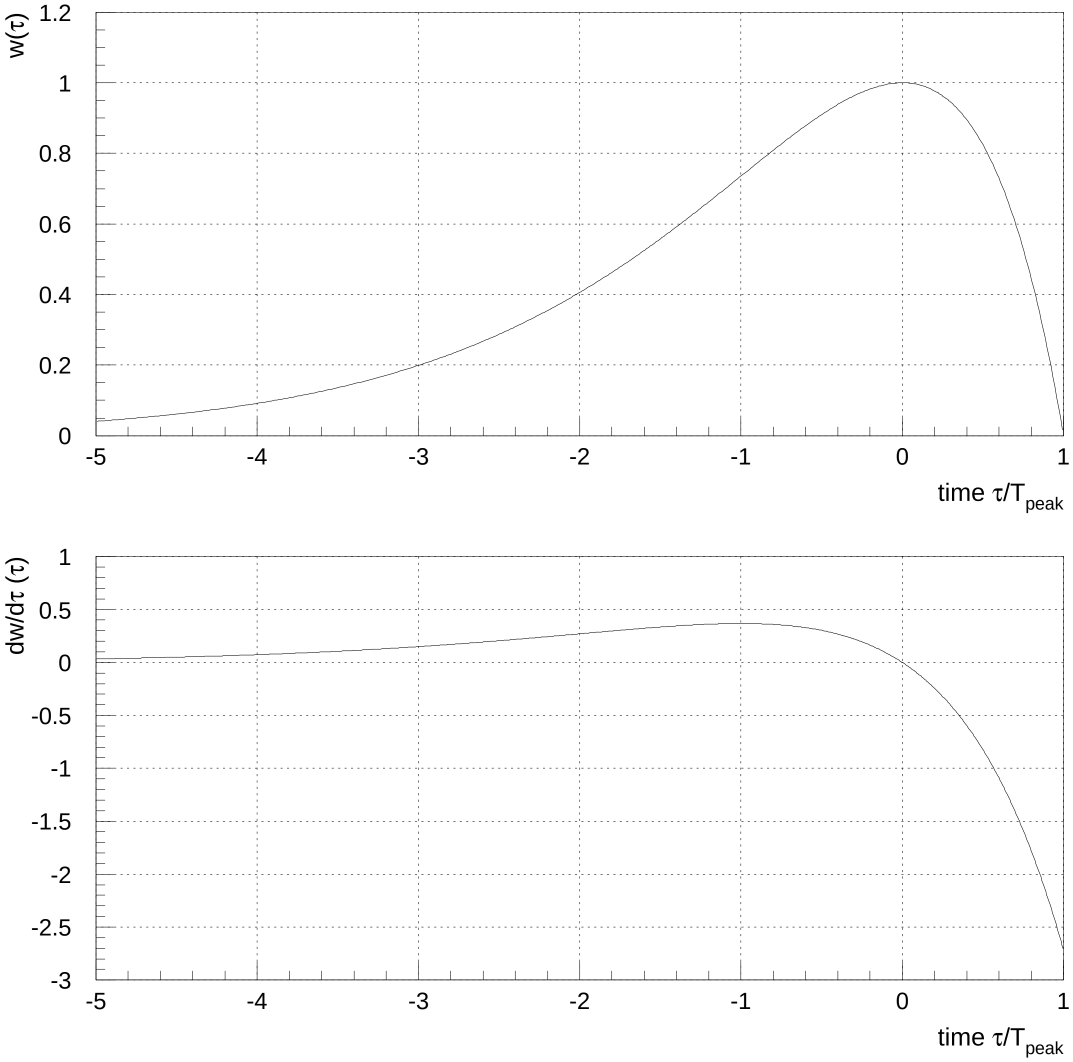


Figure 6.4: Weighting function $w(\tau)$ and its derivative $\dot{w}(\tau)$ vs. time τ of signal arrival for (single) sampling at peak of semigaussian pulse

For completeness we give the (normalized) frequency-domain transfer characteristic of the semi gaussian shaper of arbitrary order n [CS91]

$$H(\omega) = \frac{e^n n!}{n^n} \frac{j\omega\tau_{RC}}{1 + j\omega\tau_{RC}} \left[\frac{1}{1 + j\omega\tau_{RC}}\right]^n \quad . \tag{6.8}$$

In the following, we will focus on the simplest semi gaussian shaper, i. e. the CR-RC-filter (n=1) given by the weighting function

$$w(\tau) = e \left(\frac{T_{peak} - \tau}{T_{peak}}\right) e^{-(T_{peak}-\tau)/T_{peak}} \quad . \tag{6.9}$$

The time differentiated weighting function is given by

$$\dot{w}(\tau) = e \left(\frac{T_{peak} - \tau}{T_{peak}}\right) e^{-(T_{peak}-\tau)/T_{peak}} \left[\frac{1}{T_{peak} - \tau} - \frac{1}{T_{peak}}\right] \quad . \tag{6.10}$$

By calculating the integrals we obtain for the parallel noise

$$\begin{aligned} \mathrm{ENC}_p^2 &= \frac{1}{2}\left(2eI_0 + \frac{4kT}{R_p}\right)\frac{e^2 T_{peak}}{4} \\ &= \frac{1}{2}\left(2eI_0 + \frac{4kT}{R_p}\right) 1.847\, T_{peak} && (6.11) \\ & && (6.12) \end{aligned}$$

and for the serial noise

$$\begin{aligned} \mathrm{ENC}_s^2 &= \frac{1}{2} C_{in}^2 \,(4kTR_s) \frac{e^2}{4T_{peak}} \\ &= \frac{1}{2} C_{in}^2 \,(4kTR_s) \frac{1.847}{T_{peak}} \quad . && (6.13) \\ & && (6.14) \end{aligned}$$

6.2 Double Correlated Sampling

In the previously described processing methods the baseline was restored after an incoming signal either by reset or by the use of a filter (high pass); the output voltage hence is inherently refered to the baseline (the value of which is known from the readout in absence of an input signal). A different method denoted as "double correlated sampling" [Anz86, Hor93, Kur96] removes the baseline value by sampling twice - once before and once after arrival of the signal. The two samples are subsequently subtracted and read out. The reset-switch of the charge amplifier is optional and does not affect the noise performance; in practice experiment requirements will decide whether to reset the charge amplifier or whether a large feedback resistance in parallel is to be chosen.

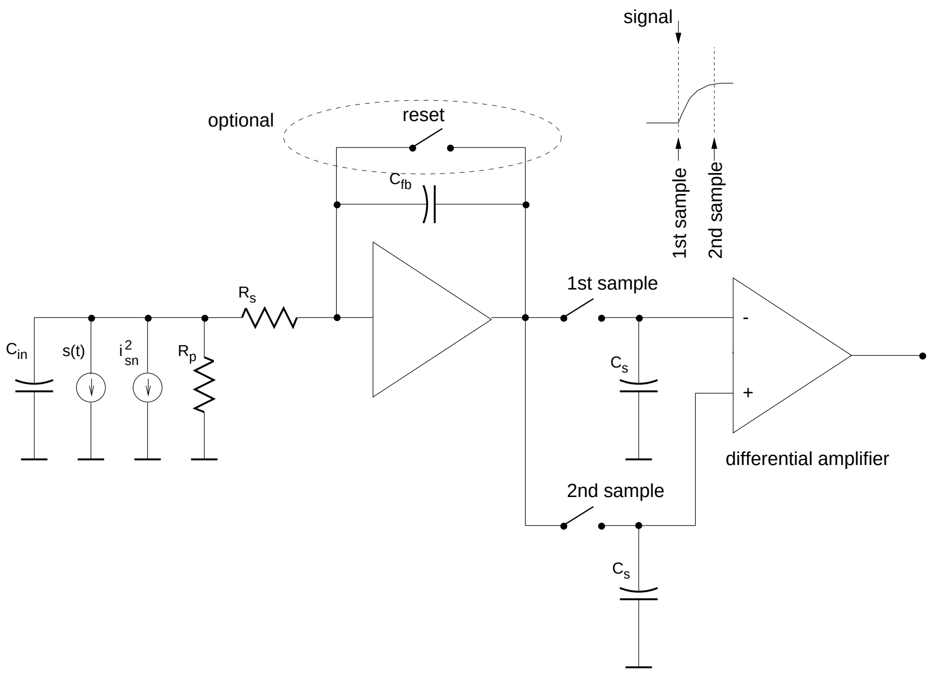


Figure 6.5: Double correlated voltage sampling architecture: the charge amplifier output is sampled twice - once before and once after the arrival of the signal the difference being taken as result. The reset is optional.

6.2.1 Sampling at Charge Amplifier Output

In the first variant the double correlated sampling takes place directly at the charge amplifier output (fig. 6.5). The charge amplifier output voltage is sampled and stored subsequently on two capacitors.

We can set up the weighting function as in the previous examples by moving the incoming signal in time and observing the result; it is plotted in fig. 6.6.

The weighting function $w(t)$ is given by

$$w(\tau) = \begin{cases} e^{\tau/\tau_{amp}} & : \quad \tau < 0 \\ \frac{1}{A}(1 - e^{\frac{\tau - T}{\tau_{amp}}}) & : \quad 0 < \tau < T \\ 0 & : \quad \text{else} \end{cases} \quad . \tag{6.15}$$

The normalization factor A equals

$$A = 1 - e^{-T/\tau_{amp}} \quad . \tag{6.16}$$

The derivation $\dot{w}(t)$ is given by

$$\dot{w}(\tau) = \begin{cases} e^{-\frac{\tau}{\tau_{amp}}} & : \quad \tau < 0 \\ -\frac{1}{A\tau_{amp}} e^{\frac{\tau - T}{\tau_{amp}}} & : \quad 0 < \tau < T \\ 0 & : \quad \text{else} \end{cases} \quad . \tag{6.17}$$

Calculating the parallel noise with the assumption $T = 2.3\tau_{amp}$ yields

$$\mathrm{ENC}_p^2 = \frac{1}{2}\left(2eI_0 + \frac{4kT}{R_p}\right) 1.725\,\tau_{amp} \tag{6.18}$$

and for the serial noise

$$\mathrm{ENC}_s^2 = \frac{1}{2}C_{in}^2\,(4kTR_s)\frac{1.106}{\tau_{amp}} \quad . \tag{6.19}$$

6.2.2 Sampling at CR-RC filter output

An alternative method would be to sample twice at the output of a convential CR-RC -shaper - once before the signal arrives (at the foot of the shaped pulse) and once on the peak of the pulse (fig. 6.7). Hence, the samples are spaced by the peak time T_{peak} of the semigaussian shaper.

We can set up the weighting function and its derivative as in the previous sections (fig. 6.8):

$$w(\tau) = \begin{cases} \frac{1}{A}\frac{T_{peak}-\tau}{T_{peak}}e^{-(T_{peak}-\tau)/T_{peak}} + \frac{1}{A}\frac{\tau}{T_{peak}}e^{\tau/T_{peak}} & : \ \tau < 0 \\ \frac{1}{A}\frac{T_{peak}-\tau}{T_{peak}}e^{-(T_{peak}-\tau)/T_{peak}} & : \ 0 < \tau < T_{peak} \\ 0 & : \ \text{else} \end{cases} \tag{6.20}$$

The normalization factor A equals

$$A = \frac{1}{e} \quad . \tag{6.21}$$

The derivative is given by

$$\dot{w}(\tau) = \begin{cases} -\frac{1}{AT_{peak}}e^{-(T_{peak}-\tau)/T_{peak}} + \frac{1}{A}\frac{T_{peak}-\tau}{T_{peak}^2}e^{-(T_{peak}-\tau)/T_{peak}} & \\ \quad +\frac{1}{AT_{peak}}e^{\tau/T_{peak}} + \frac{\tau}{AT_{peak}^2}e^{\tau/T_{peak}} & : \ \tau < 0 \\ -\frac{1}{AT_{peak}}e^{-(T_{peak}-\tau)/T_{peak}} + \frac{1}{A}\frac{T_{peak}-\tau}{T_{peak}^2}e^{-(T_{peak}-\tau)/T_{peak}} & : \ 0 < \tau < T_{peak} \\ 0 & : \ \text{else} \end{cases} \quad . \tag{6.22}$$

Solving the integrals for parallel and serial noise one obtains

$$\begin{aligned} \mathrm{ENC}_p^2 &= \frac{1}{2}\left(2eI_0 + \frac{4kT}{R_p}\right)\frac{e(e-2)T_{peak}}{2} \\ &= \frac{1}{2}\left(2eI_0 + \frac{4kT}{R_p}\right) 0.976\,T_{peak} \end{aligned} \tag{6.23}$$

(6.24)

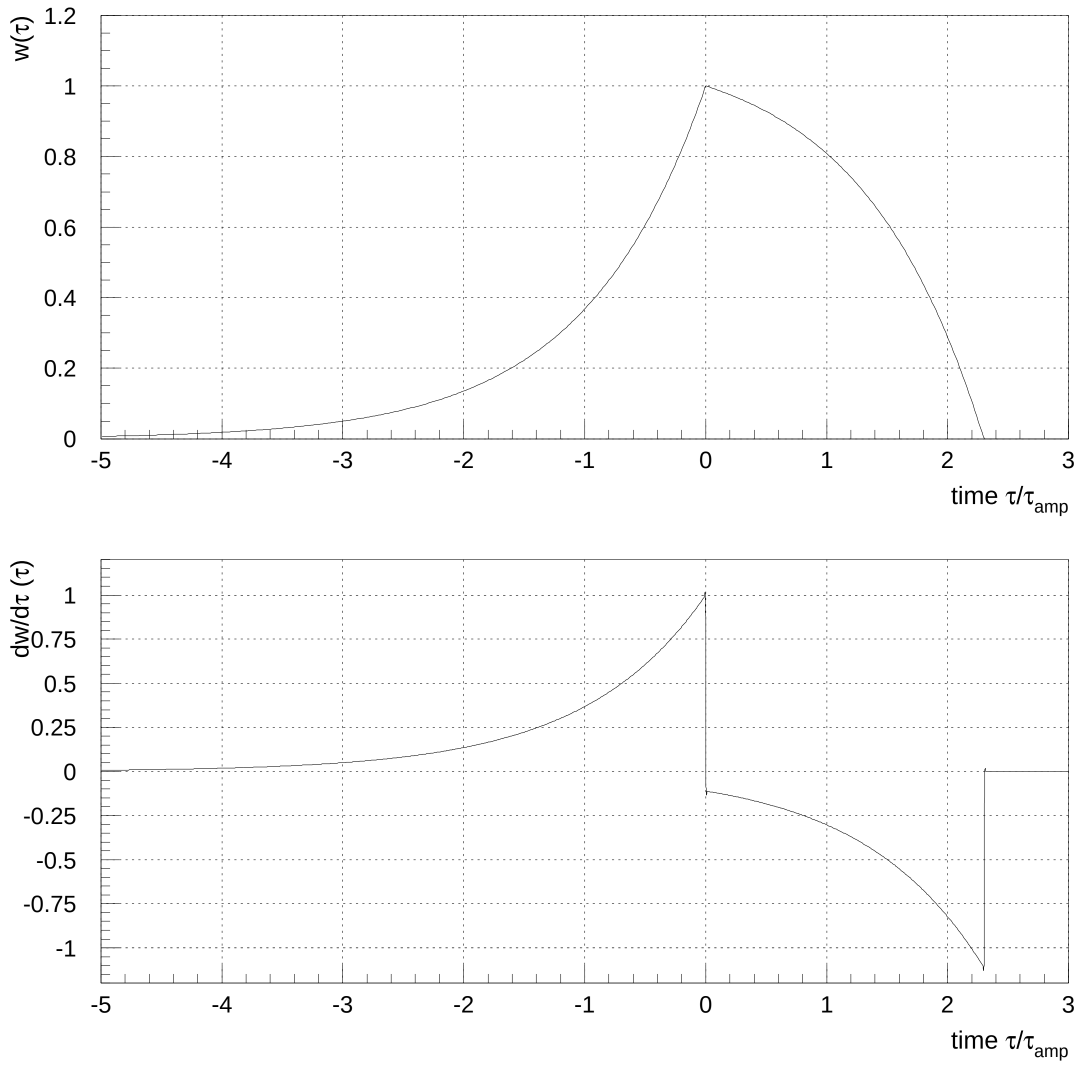


Figure 6.6: Weighting function $w(\tau)$ and its derivative $\dot{w}(\tau)$ vs. time τ of signal arrival for double correlated voltage sampling

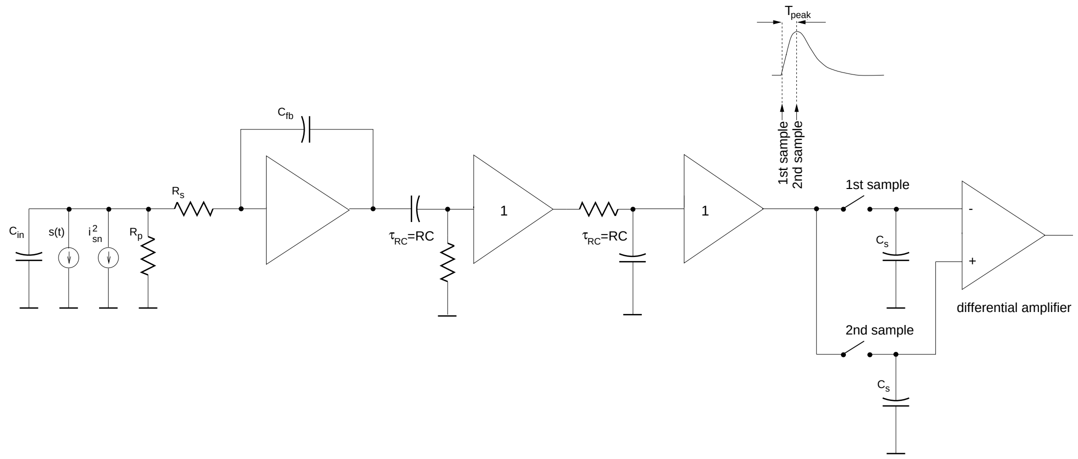


Figure 6.7: Double correlated voltage sampling architecture: the shaper output is sampled twice - once before and once at the peak of the shaped signal with the difference being taken as result.

and

$$\begin{aligned} \mathrm{ENC}_s^2 &= \frac{1}{2} C_{in}^2 \, (4kTR_s) \frac{e^2}{2T_{peak}} \\ &= \frac{1}{2} C_{in}^2 \, (4kTR_s) \frac{3.695}{T_{peak}} \end{aligned} \tag{6.25}$$

(6.26)

6.3 Multiple Correlated Sampling

6.3.1 Sampling at Charge Amplifier Output

Multiple correlated sampling at the charge amplifier output was developed in order to minimize noise by introducing some degree of averaging [Hof84, Lutz88]. Essentially, multiple sampling is an extension of the double correlated sampling scheme. We will discuss the quadruple sampling; in this scheme it is sampled twice before the charge amplifier has undergone its rise and twice after (fig. 6.10). The multiple correlated sampling is relatively time consuming, which makes it difficult to employ in modern high energy physics experiments with signal rates approaching 40 MHz.

The weighting function is given by (see also fig. 6.9)

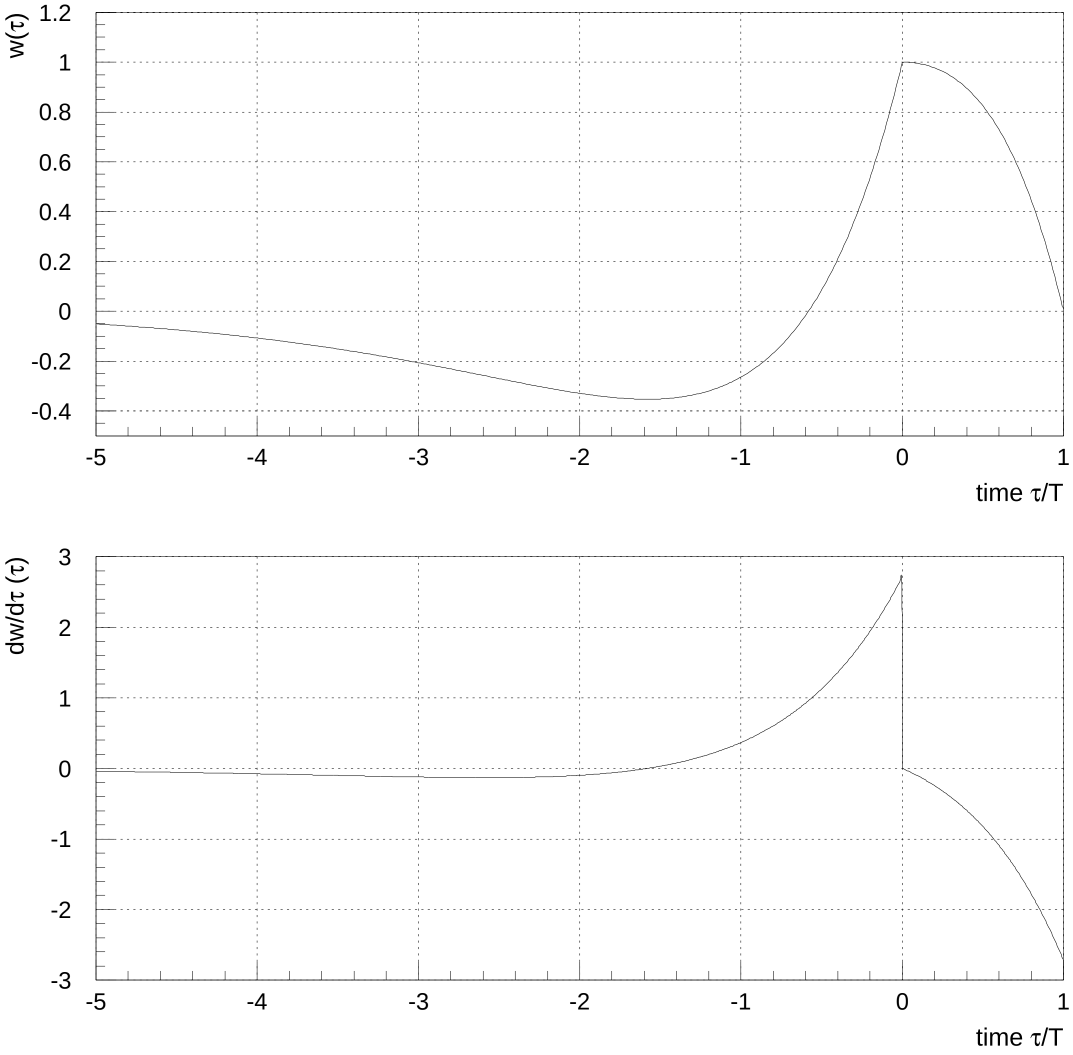


Figure 6.8: Weighting function $w(\tau)$ and its derivative $\dot{w}(\tau)$ vs. time τ of signal arrival for double correlated sampling behind CR-RC-shaper

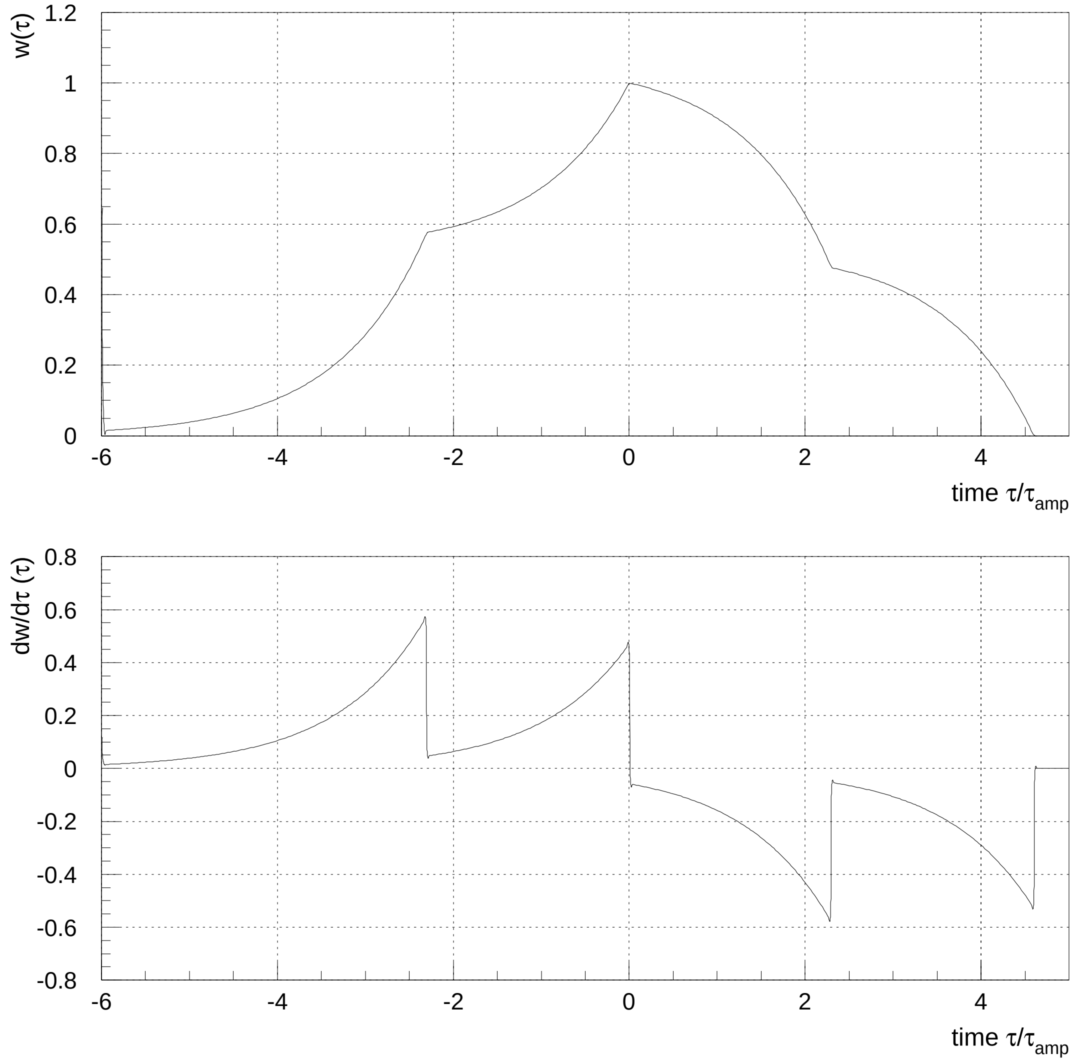


Figure 6.9: Weighting function $w(\tau)$ and its derivative $\dot{w}(\tau)$ vs. time τ of signal arrival for quadruple correlated voltage sampling at charge amplifier output

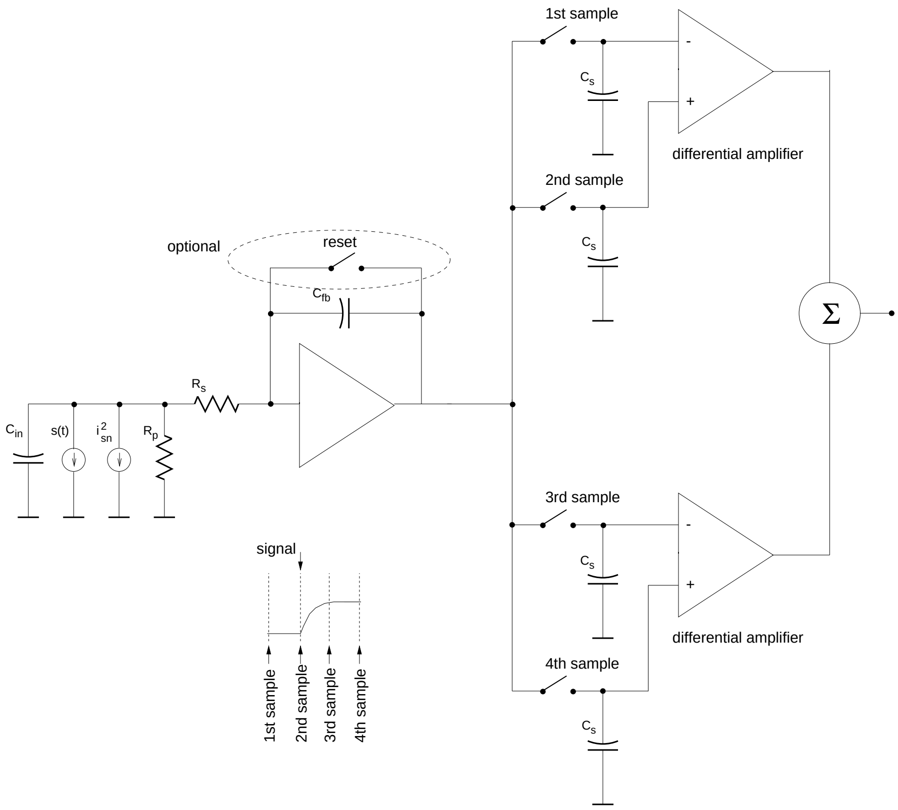


Figure 6.10: Quadruple correlated voltage sampling at charge amplifier output; sample 3 and 4 are subtracted from sample 1 and 2.

$$
w(\tau) = \begin{cases} -\frac{1}{2A} e^{-\frac{T-\tau}{\tau_{amp}}} \left(1 + e^{\frac{T}{2\tau_{amp}}} - e^{\frac{T}{\tau_{amp}}} - e^{\frac{3T}{2\tau_{amp}}}\right) & : \quad \tau < -1/2T \\ \frac{1}{2A} \left[1 - e^{-\frac{T-\tau}{\tau_{amp}}} \left(1 + e^{\frac{T}{2\tau_{amp}}} - e^{\frac{T}{\tau_{amp}}}\right)\right] & : \quad -1/2T < \tau < 0 \\ \frac{1}{2A} \left[2 - e^{-\frac{T-\tau}{\tau_{amp}}} \left(1 + e^{\frac{T}{2\tau_{amp}}}\right)\right] & : \quad 0 < \tau < T/2 \\ \frac{1}{2A} \left(1 - e^{-\frac{T-\tau}{\tau_{amp}}}\right) & : \quad T/2 < \tau < T \\ 0 & : \quad \text{else} \end{cases} \quad . \tag{6.27}
$$

The normalization factor A equals

$$
A = \frac{1}{2} \left(2 - e^{-T/\tau_{amp}} - e^{-\frac{T}{2\tau_{amp}}}\right) \quad . \tag{6.28}
$$

The derivation is given by

$$
\dot{w}(\tau) = \begin{cases} -\frac{1}{2A\tau_{amp}} e^{-\frac{T-\tau}{\tau_{amp}}} \left(1 + e^{\frac{T}{2\tau_{amp}}} - e^{\frac{T}{\tau_{amp}}} - e^{\frac{3T}{2\tau_{amp}}}\right) & : \quad \tau < -1/2T \\ -\frac{1}{2A\tau_{amp}} \left[e^{-\frac{T-\tau}{\tau_{amp}}} \left(1 + e^{\frac{T}{2\tau_{amp}}} - e^{\frac{T}{\tau_{amp}}}\right)\right] & : \quad -1/2T < \tau < 0 \\ -\frac{1}{2A\tau_{amp}} \left[e^{-\frac{T-\tau}{\tau_{amp}}} \left(1 + e^{\frac{T}{2\tau_{amp}}}\right)\right] & : \quad 0 < \tau < T/2 \\ -\frac{1}{2A\tau_{amp}} e^{-\frac{T-\tau}{\tau_{amp}}} & : \quad T/2 < \tau < T \\ 0 & : \quad \text{else} \end{cases} \quad . \tag{6.29}
$$

Solving the integrals one receives for the parallel noise

$$
\text{ENC}_p^2 = \frac{1}{2} \left(2eI_0 + \frac{4kT}{R_p}\right) 3.282\, \tau_{amp} \tag{6.30}
$$

and

$$
\text{ENC}_s^2 = \frac{1}{2} C_{in}^2 \,(4kTR_s) \frac{0.582}{\tau_{amp}} \quad . \tag{6.31}
$$

6.3.2 Sampling at CR-RC Filter Output (Deconvolution)

The deconvolution method [RD20-1, RD20-2, RD20-3, RD20-4] has been developed relatively late w. r. t. the others mentioned before; the output of the CR-RC-filter is sampled three times consecutively and the samples are summed up with specific weights to give the final result.

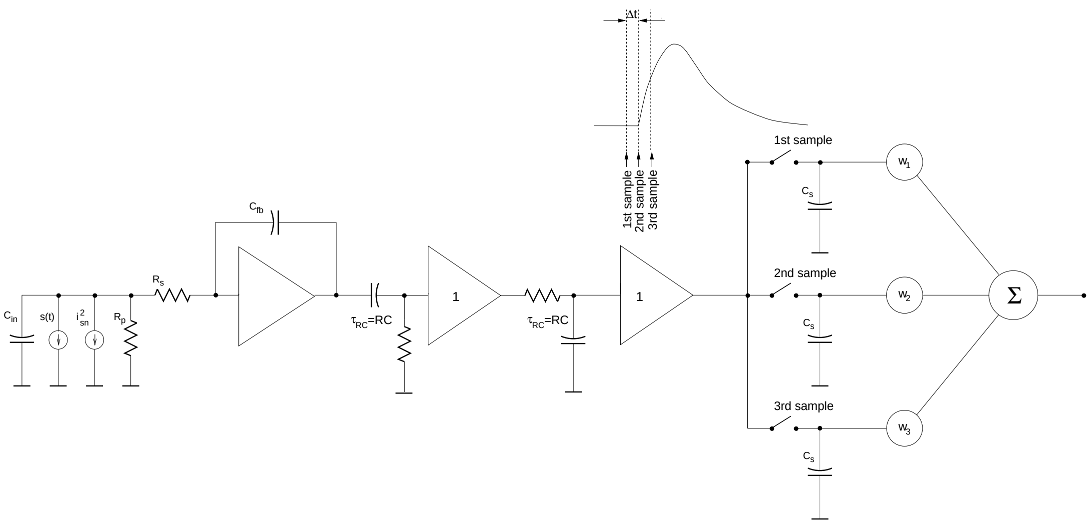


Figure 6.11: Deconvolution architecture: the shaper output is sampled three times and the samples are summed up with specific weights to give the final result.

The deconvolution method has been developed for the Large Hadron Collider experiments at CERN; due to the high bunch crossing frequency (40 MHz) the weighting function's extension in time should be as restricted as possible to avoid ambiguities when relating a signal to the corresponding bunch crossing. The deconvolution method offers the possibility to contract the relatively extended weighting function of a CR-RC-shaper (peaktime T_{peak}, fig. 6.4) to only 2/3 T_{peak}; if one admits overlap of the flanks (sampling happens at the weighting function's peak) a time resolution of 1/3 T_{peak} can be achieved. Thus, in spite of using a relatively large T_{peak}=75 ns for the shaper (which can be done easily with CMOS), subsequent bunch crossings can be separated.

Deconvolution bases on the recognition that applying an inverse shaping and a differentiation to the shaper output should retrieve the original signal - which is a δ-function and hence "very" limited in time. To perform this mathematical operation the shaper output is sampled at fixed intervals and fed to a FIR-filter (finite inpulse response filter). Hence, the continous-time equation

$$g(t) = \int_{-\infty}^{\infty} h(t-\tau)s(\tau)\,d\tau = \int_{-\infty}^{\infty} w(\tau)s(\tau)\,d\tau \tag{6.32}$$

becomes a matrix equation

$$G_i = \sum_j W_{ij} S_j \tag{6.33}$$

where the (G_1,G_2,$G_3 \cdots$) denote the values of the shaper output voltage $g(t)$ sampled with the rate $1/\Delta t$.

With $V = W^{-1}$ we can write

$$S_i = \sum_j V_{ij} G_j = \sum_{j,k} V_{ij} W_{jk} S_k \tag{6.34}$$

to retrieve the original signal S.

For reasons of causality, V as well as W are lower triangular matrices of the form

$$\begin{pmatrix} X1 & 0 & 0 & 0 & \cdots \\ X2 & X1 & 0 & 0 & \cdots \\ X3 & X2 & X1 & 0 & \cdots \\ \vdots & \vdots & \vdots & \vdots & \cdots \end{pmatrix} \tag{6.35}$$

with $X = V$ or $X = W$.

For the semigaussian CR-RC-filter only three entries in the deconvolution matrix V are nonzero which are given by

$$\begin{aligned} V_1 &= \frac{e^{\Delta t/T_{peak}-1}}{\Delta t/T_{peak}} \\ V_2 &= -2\frac{e^{-1}}{\Delta t/T_{peak}} \\ V_3 &= \frac{e^{-\Delta t/T_{peak}-1}}{\Delta t/T_{peak}} \quad . \end{aligned} \tag{6.36}$$

For $\Delta t/T_{peak}$=1/3 the weights become V_1=1.5403, V_2=-2.2073, and V_3=0.7908, respectively.

The overall weighting function W^{tot} is given by

$$W_{ij}^{tot} = \sum_k V_{ik} W_{kj} \tag{6.37}$$

which is to be applied to the sampled input signal (S_1,S_2,$S_3 \cdots$).

To calculate the noise performance we assume the input signal $s(t)$ to be continous in time and do the sampling at the shaper output; summing together these samples (G_1,G_2,$G_3 \cdots$) with the appropriate weights V_i yields the (continous) overall weighting function (see also fig. 6.12)

$$w^{tot}(\tau) = \begin{cases} (1+\frac{\tau}{\Delta t})e^{\frac{1}{3}\frac{\tau}{\Delta t}} & : \quad -\Delta t < \tau < 0 \\ (1-\frac{\tau}{\Delta t})e^{\frac{1}{3}\frac{\tau}{\Delta t}} & : \quad 0 < \tau < \Delta t \\ 0 & : \quad \text{else} \end{cases} \quad . \tag{6.38}$$

The derivation yields

$$\dot{w}^{tot}(\tau) = \begin{cases} \frac{4\Delta t+\tau}{(\Delta t)^2}e^{\frac{1}{3}\frac{\tau}{\Delta t}} & : \quad -\Delta t < \tau < 0 \\ -\frac{2\Delta t+\tau}{(\Delta t)^2}e^{\frac{1}{3}\frac{\tau}{\Delta t}} & : \quad 0 < \tau < \Delta t \\ 0 & : \quad \text{else} \end{cases} \quad . \tag{6.39}$$

Fig. 6.12 shows $w^{tot}(\tau)$ and $\dot{w}^{tot}(\tau)$.

Integrating the square of the weighting function resp. of its derivative yields

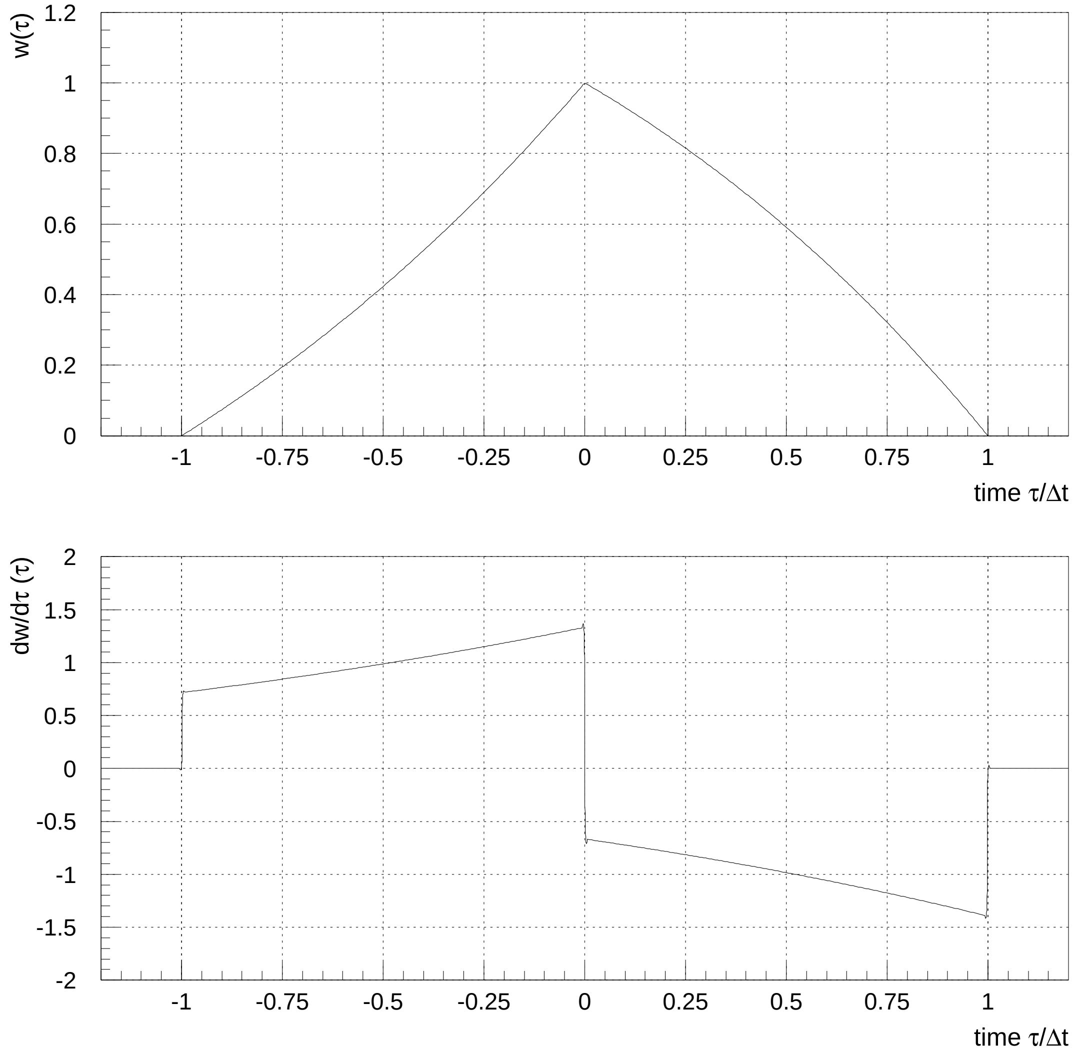


Figure 6.12: Weighting function $w(\tau)$ and its derivative $\dot{w}(\tau)$ vs. time τ of signal arrival for deconvolution of CR-RC-shaping; Δt denotes the sampling interval. The peak of the shaped pulse takes place at T_{peak}=3Δt [RD20-2].

for the parallel noise

$$
\begin{aligned}
\mathrm{ENC}_p^2 &= \frac{1}{2}\left(2eI_0 + \frac{4kT}{R_p}\right)\frac{9}{4}(3e^{\frac{2}{3}} - 4 - 3e^{-\frac{2}{3}})\,\Delta t \\
&= \frac{1}{2}\left(2eI_0 + \frac{4kT}{R_p}\right) 0.6816\,\Delta t
\end{aligned}
\tag{6.40}
$$

and for the serial noise

$$
\begin{aligned}
\mathrm{ENC}_s^2 &= \frac{1}{2}C_{in}^2\,(4kTR_s)\frac{1}{4}(3e^{\frac{2}{3}} + 4 - 3e^{-\frac{2}{3}})\,\Delta t \\
&= \frac{1}{2}C_{in}^2\,(4kTR_s)\frac{2.076}{\Delta t}
\end{aligned}
\tag{6.41}
$$

6.4 Optimum Pulse Processing

As we have seen in the previous treatments, filtering can alter the signal-to-noise ratio of a system (assuming the filter itself to be noiseless). The question arises, naturally, whether there is an optimum signal shaping yielding the best signal-to-noise ratio.

Bode and Shannon [BS50] studied the optimum network to determine an unknown signal with optimum precision. In the underlying case, however, the signal shape is well known, but the amplitude has to be measured with highest possible precision.

We will follow the deduction of Halbach [Hal53] which we can simplify by use of the preparations made in sect. 5.

The optimum filter ($h(t)$ resp. $H(\omega)$) transfers the charge amplifier output signal $s(t)$ according to

$$
g(t) = \int_{-\infty}^{\infty} s(t-\tau)h(\tau)\,d\tau \quad . \tag{6.42}
$$

The noise spectrum $N^2(\omega)$ is transfered to the filter output according to

$$
\sigma^2\,g = \frac{1}{2\pi}\int_{-\infty}^{\infty} N^2(\omega)|H(\omega)|^2\,d\omega \tag{6.43}
$$

where we have assumed the spectral noise density to be bilateral for ease of calculation. The unilateral spectral density is twice this value.

The signal-to-noise ratio is given as the ratio of signal amplitude (at the time of sampling) to the total signal variance:

$$
\left(\frac{\mathrm{S}}{\mathrm{N}}\right)^2 = \frac{g^2(t)}{\sigma^2\,g} \tag{6.44}
$$

The task is to maximize eq. (6.44) finding the optimum filter function $h(t)$ resp. $H(\omega)$.

We split the filter $H(\omega)$ according to

$$
H(\omega) = H_2(\omega)H_1(\omega) \tag{6.45}
$$

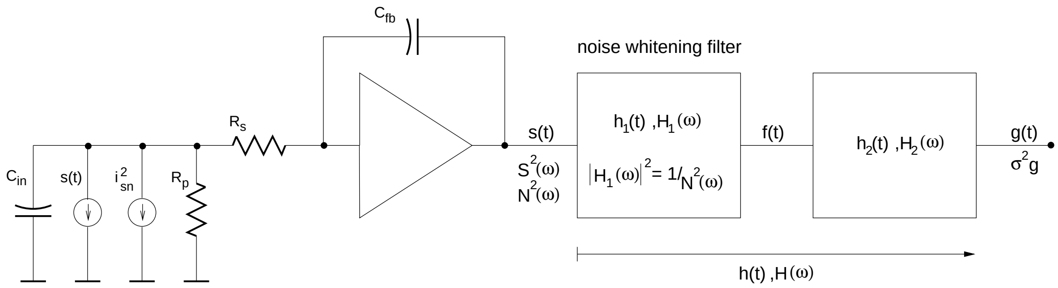


Figure 6.13: Signal processing architecture for optimum signal processing

and use $H_1(\omega)$ as a noise-whitening filter, i. e. the noise spectrum behind $H_1(\omega)$ be flat. $H_1(\omega)$ is given by

$$|H_1(\omega)|^2 = \frac{1}{N^2(\omega)} \quad . \tag{6.46}$$

We will later give $H_1(\omega)$ explicitely; at this point it may suffice that a filter $H_1(\omega)$ exists which transforms the noise spectrum behind the preamplifier into a white one.

The impulse response $h(t)$ of the overall filter can be written as

$$h(t) = \int_{-\infty}^{\infty} h_1(\tau) h_2(t-\tau)\, d\tau \tag{6.47}$$

and the signal at the filter output

$$g(t) = \int_{-\infty}^{\infty}\int_{-\infty}^{\infty} s(t-\tau_1) h_1(\tau_2) h_2(\tau_1-\tau_2)\, d\tau_1\, d\tau_2 \quad . \tag{6.48}$$

The signal transformed by filter $h_1(t)$ only is given by

$$f(t) = \int_{-\infty}^{\infty} s(t-\tau) h_1(\tau)\, d\tau \tag{6.49}$$

so that we can rewrite eq. (6.48)

$$g(t) = \int_{-\infty}^{\infty} f(t-\tau) h_2(\tau)\, d\tau \quad . \tag{6.50}$$

Due to eq. (6.46) the noise integral eq. (6.43) can be rewritten

$$\sigma^2 g = \frac{1}{2\pi} \int_{-\infty}^{\infty} |H_2(\omega)|^2\, d\omega \quad . \tag{6.51}$$

Using Parseval's identity (for the bilateral case) we can rewrite eq. (6.51) as

$$\sigma^2\, g = \int_{-\infty}^{\infty} h_2^2(\tau)\, d\tau \quad . \tag{6.52}$$

We rewrite eq. (6.44) using eqs. (6.47) and (6.52)

$$\left(\frac{\mathrm{S}}{\mathrm{N}}\right)^2 = \frac{g^2(t)}{\sigma^2\, g} = \frac{\left[\int_{-\infty}^{\infty} f(t-\tau) h_2(\tau)\, d\tau\right]^2}{\int_{-\infty}^{\infty} h_2^2(\tau)\, d\tau} \quad . \tag{6.53}$$

Minimizing eq. (6.53) by appropriate choice of $h_2(\tau)$ can be done using variation calculus. Function $h_2^{min}(\tau)$ minimizes eq. (6.53) if for every function $k(\tau)$ there exists a real number ϵ_0 so that

$$\left(\frac{\mathrm{S}}{\mathrm{N}}\right)^2 \left(h_2^{min}(\tau) + \epsilon k(\tau)\right) \geq \left(\frac{\mathrm{S}}{\mathrm{N}}\right)^2 \left(h_2^{min}(\tau)\right) \tag{6.54}$$

for all ϵ with $|\epsilon| < \epsilon_0$.
Using differential calculus $h_2^{min}(\tau)$ is determined by

$$\frac{d}{d\epsilon} \left(\frac{\mathrm{S}}{\mathrm{N}}\right)^2 \left(h_2^{min}(\tau) + \epsilon k(\tau)\right)\Big|_{\epsilon=0} = 0 \tag{6.55}$$

for all $k(\tau)$.
We obtain

$$\left(g'(t) - \frac{g(t)}{\sigma^2\, g} (\sigma^2\, g)'\right)\Big|_{\epsilon=0} = 0 \tag{6.56}$$

(the prime denotes differentiation w. r. t. ϵ).
The differentiations yield

$$g'(t)\big|_{\epsilon=0} = \int_{-\infty}^{\infty} f(t-\tau) k(\tau)\, d\tau \tag{6.57}$$

and

$$(\sigma^2\, g)'\Big|_{\epsilon=0} = \int_{-\infty}^{\infty} h_2(\tau) g(\tau)\, d\tau \quad . \tag{6.58}$$

Substituting eqs. (6.57) and (6.58) into eq. (6.56) and writing everything into one integral yields

$$\int_{-\infty}^{\infty} \left[f(t-\tau) - \frac{g(t)}{\sigma^2\, g} h_2(\tau)\right] k(\tau)\, d\tau = 0 \quad . \tag{6.59}$$

$g(t)$ and σ^2 are constants w. r. t. the integration variable τ and do not contain $k(\tau)$ anymore ($\epsilon = 0$). Since eq. (6.59) has to be fulfilled for every value of $k(\tau)$, the term in brackets has to be identically zero. Thus, $h_2^{min}(t)$ is determined to be

$$h_2^{min}(\tau) \propto f(t-\tau) \quad . \tag{6.60}$$

Hence, the impulse response $h_2^{min}(\tau)$ is simply the time-reversed and shifted impulse response of the $h_1(\tau)$-transformed signal $s(t)$.

The derivation of the noise-whitening filter remains. The noise spectrum behind the charge sensitive amplifier has been calculated in eq. (4.24); neglecting the 1/f-noise it can be written in the simplified form

$$N^2(\omega) = A + \frac{B}{\omega^2} = \frac{1}{|H(\omega)|^2} \tag{6.61}$$

with the A-term due to the serial noise and the B/ω^2-term due to parallel noise. Hence

$$|H(\omega)|^2 = \frac{1}{A}\frac{\tau_c^2\omega^2}{1+\tau_c^2\omega^2} = \frac{1}{A}\left|\frac{j\omega\tau_c}{1+j\omega\tau_c}\right|^2 \tag{6.62}$$

where $\tau_c^2 = A/B$ gives the square of the noise corner time constant. Eq. (6.62) describes the transfer function of a CR-high pass.

We want to determine $f(t)$. The incoming signal $s_0(t)$ from a silicon detector is (w. r. t. the other system time constants) assumed to be given by $s_0(t) = \delta(t)$ (normalized); integrated by the charge amplifier we obtain

$$s(t) = u(t) = \begin{cases} 0 & : \quad t < 0 \\ 1 & : \quad t \geq 0 \end{cases} \tag{6.63}$$

where $u(t)$ is the step function. The response of the CR-high pass to a step function is given by

$$f(t) = \begin{cases} 0 & : \quad t < 0 \\ e^{-t/\tau_c} & : \quad t \geq 0 \end{cases} \tag{6.64}$$

and hence

$$h_2^{min}(\tau) = \begin{cases} e^{(\tau-t)/\tau_c} & : \quad \tau \leq t \\ 0 & : \quad \tau > t \end{cases} \tag{6.65}$$

where t is the time of observation.

$h_2^{min}(\tau)$ extends to infinite negative times; in principle causality requires that $h_2^{min}(\tau)$ must be 0 for $\tau < 0$. If the measurement time t is moved to large positive values (e. g. $t > 3\tau_c$) little error is introduced by cutting the tail at negative times. For the noise comparison, however, it has to be kept in mind that the optimum S/N-ratio can only be achieved with infinite measurement time.

$h_2^{min}(\tau)$ could in principle be generated by subtracting two exponential rises with different carriers, but this would imply that the output of two unstable systems would have to be subtracted. Therefore, $h_2^{min}(\tau)$ cannot be realized with a simple active RC-filter. Radeka [Rad64] proposes an architecture using a function generator generating $w_2^{min}(\tau)$, which is multiplied with the output of the noise-whitening filter $f(\tau)$ and the product is put to a gated-integrator (in principle a direct mapping of the convolution integral into hardware); the system needs to know the time of signal arrival, so it would fit to the conditions of storage ring experiments (of course the time restrictions have to be obeyed). The whole scheme could also be implemented by the use of digital signal-processing.

For the noise evaluation we must set up the overall (starting from the current pulse delivered by the detector) transfer function $h^{tot}(t)$ which is given by the convolution of $f(t)$ and $h_2^{min}(t)$:

$$h^{tot}(t) = \int_{-\infty}^{\infty} f(\tau) h_2^{min}(t-\tau)\, d\tau \tag{6.66}$$

The weighting function is given by (see fig. 6.14)

$$w^{tot}(\tau) = \begin{cases} e^{\tau/\tau_c} & : \quad \tau < 0 \\ e^{-\tau/\tau_c} & : \quad \tau > 0 \end{cases} \tag{6.67}$$

where τ_c is the noise corner time constant of the charge amplifier resp. the time constant of the noise-whitening CR-high pass.

The derivation is given by

$$\dot{w}^{tot}(\tau) = \begin{cases} \frac{1}{\tau_c} e^{\tau/\tau_c} & : \quad \tau < 0 \\ -\frac{1}{\tau_c} e^{-\tau/\tau_c} & : \quad \tau > 0 \end{cases} \quad . \tag{6.68}$$

The noise integrals are easily carried out and yield

for the parallel noise

$$\mathrm{ENC}_p^2 = \frac{1}{2}\left(2eI_0 + \frac{4kT}{R_p}\right)\tau_c \tag{6.69}$$

and for the serial noise

$$\mathrm{ENC}_s^2 = \frac{1}{2} C_{in}^2 \,(4kTR_s)\frac{1}{\tau_c} \quad . \tag{6.70}$$

In eq. (6.46) a specific choice for $H_1(\omega)$ was made and $H_2(\omega)$ was optimized w. r. t. this choice. To prove that there cannot be a better filter with another $H_1(\omega)$ we insert eq. (6.60) into eq. (6.53) which yields for the S/N-ratio behind the filter

$$\left(\frac{\mathrm{S}}{\mathrm{N}}\right)^2 = \int_{-\infty}^{\infty} f^2(\tau)\, d\tau \quad . \tag{6.71}$$

With Parseval's identity, the Fourier-transform of eq. (6.49) and eq. (6.46) we obtain

$$\left(\frac{\mathrm{S}}{\mathrm{N}}\right)^2 = \int_{-\infty}^{\infty} S^2(\omega)|H_1(\omega)|^2\, d\omega = \int_{-\infty}^{\infty} \frac{S^2(\omega)}{N^2(\omega)}\, d\omega \tag{6.72}$$

which gives the S/N-ratio at the filter input. In other words, the S/N-ratio at the overall filter output is the same as at the filter input; hence there cannot be another filter having a better noise performance as the one deduced above.

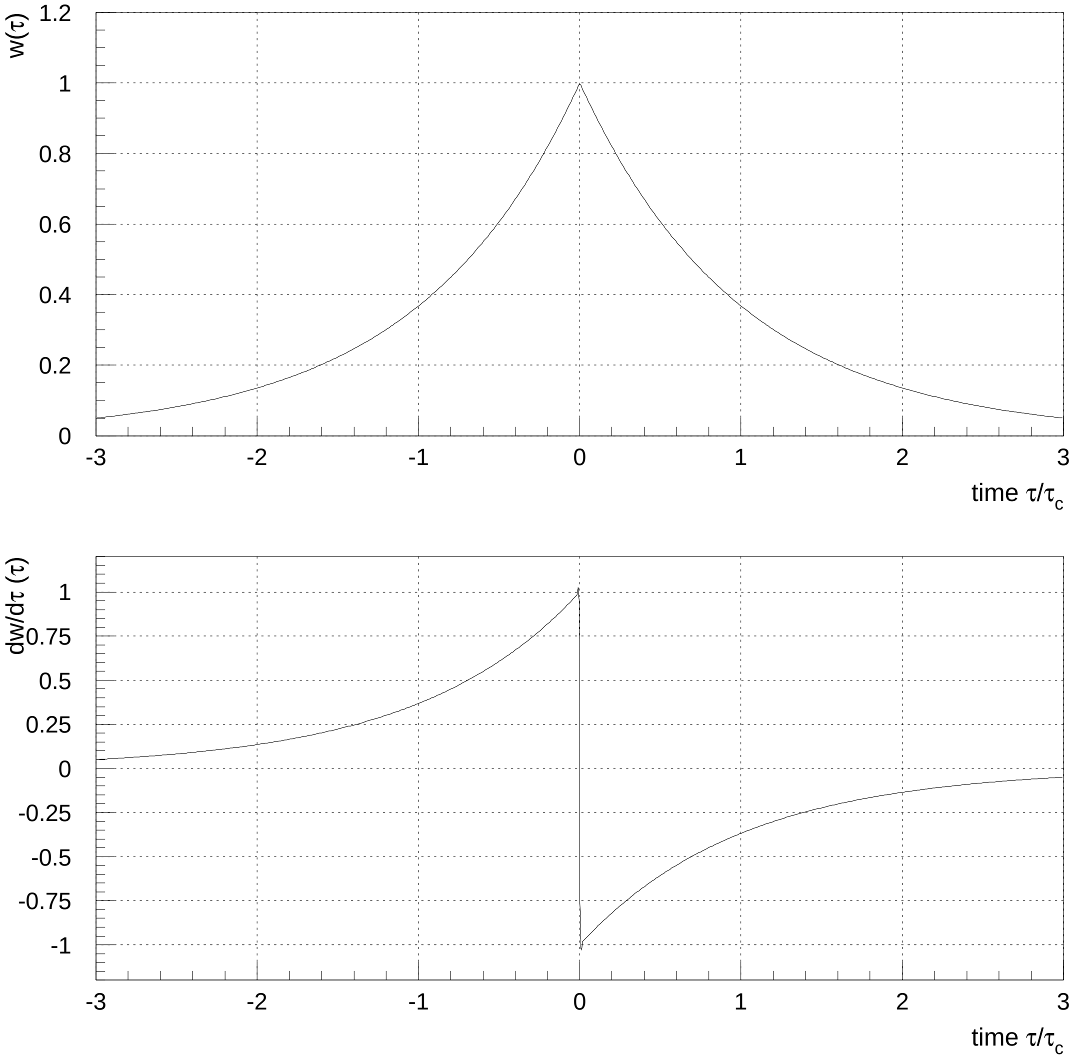


Figure 6.14: Weighting function $w(\tau)$ and its derivative $\dot{w}(\tau)$ vs. time τ of signal arrival for optimum filter ("cusp"). τ_c denotes the time constant of the noise-whitening CR-filter.

	parallel	serial	time consumpt.
single sampling charge amp. outp.	$\frac{i_p^2}{2} \cdot 1.230\,\tau_{amp}$	∞	$2.30\,\tau_{amp}$
single sampling shaper outp.	$\frac{i_p^2}{2} \cdot 1.847\,T_{peak}$	$\frac{v_s^2}{2} C_{in}^2 \cdot 1.847/T_{peak}$	$3.89\,T_{peak}$
doubl. corr. sampling charge amp. outp.	$\frac{i_p^2}{2} \cdot 1.725\,\tau_{amp}$	$\frac{v_s^2}{2} C_{in}^2 \cdot 1.106/\tau_{amp}$	$2.30\,\tau_{amp}$
doubl. corr. sampling shaper outp.	$\frac{i_p^2}{2} \cdot 0.9760\,T_{peak}$	$\frac{v_s^2}{2} C_{in}^2 \cdot 3.695/T_{peak}$	$4.10\,T_{peak}$
quadr. corr. sampling charge amp. outp.	$\frac{i_p^2}{2} \cdot 3.282\,\tau_{amp}$	$\frac{v_s^2}{2} C_{in}^2 \cdot 0.5820/\tau_{amp}$	$4.60\,\tau_{amp}$
deconvolution	$\frac{i_p^2}{2} \cdot 0.6816\,\Delta t$	$\frac{v_s^2}{2} C_{in}^2 \cdot 2.076/\Delta t$	$0.867\,\Delta t$
optim. proc.	$\frac{i_p^2}{2} \cdot \tau_c$	$\frac{v_s^2}{2} C_{in}^2 \cdot 1/\tau_c$	$2.30\,\tau_c$

Table 6.1: Summary of ENC^2 values of various customary pulse processing architectures as presented in the previous chapter; $i_p^2 = 2eI_0 + \frac{4kT}{R_p}$, $v_s^2 = 4kTR_s$

6.5 Comparison of concepts

In table 6.1 we summarize the squared noise performance in terms of the architecture related time constants. We included the optimum noise processing into table 6.1; it has to be stated, however, that τ_c cannot be adjusted freely to adapt to a given integration time, but τ_c is the noise corner time constant given by the serial and parallel noise sources of the system.

For comparison of the previously presented architectures we have to normalize the results obtained w. r. t. the time consumption needed. Therefore, in the last column of table 6.1 we have given the time consumption of the related signal processing method; we demand the signal to be decayed to 10 % of the maximum value before the next signal is measured (this equals the time between the (negative) τ with $|w(\tau)| = 0.1$ and the weighting function's peak at $\tau = 0$ for all architectures but the resetable charge amplifier). A 10 % error is naturally not satisfactory for a high resolution spectroscopy system, but is an acceptable compromise for many particle physics detector systems. If the error is to be decreased further, the time-refered performance of the shaper (single/double sampling) looses most, the sampling methods at the charge amplifier output perform better, and the deconvolution method performs almost unaffected.

Table 6.2 gives the noise performance with common measurement time T_{meas} enforced. In principle serial and parallel noise should both be considered in a fair comparison of the architectures; however, since we deal mainly with measurement times of 100 ns or below (i. e. $T_{meas} \ll \tau_c$) we furtheron regard only the serial noise performance.

As can be seen immediately, the deconvolution method performs best. Its weighting function reaches the peak in a uniform manner (with almost constant slope); this is favorable because – since the square of $\dot{w}(t)$ enters into the serial noise – regions of higher slope (as apparent with the other weighting functions) give rise to increased serial

	parallel	serial
single sampling charge amp. outp.	$\frac{i_p^2}{2} \cdot 0.535\, T_{meas}$	∞
single sampling shaper outp.	$\frac{i_p^2}{2} \cdot 0.475\, T_{meas}$	$\frac{v_s^2}{2} C_{in}^2 \cdot 7.18/T_{meas}$
doubl. corr. sampling charge amp. outp.	$\frac{i_p^2}{2} \cdot 0.750\, T_{meas}$	$\frac{v_s^2}{2} C_{in}^2 \cdot 2.54/T_{meas}$
doubl. corr. sampling shaper outp.	$\frac{i_p^2}{2} \cdot 0.238\, T_{meas}$	$\frac{v_s^2}{2} C_{in}^2 \cdot 15.15/T_{meas}$
quadr. corr. sampling charge amp. outp.	$\frac{i_p^2}{2} \cdot 0.713\, T_{meas}$	$\frac{v_s^2}{2} C_{in}^2 \cdot 2.68/T_{meas}$
deconvolution	$\frac{i_p^2}{2} \cdot 0.786\, T_{meas}$	$\frac{v_s^2}{2} C_{in}^2 \cdot 1.80/T_{meas}$

Table 6.2: ENC^2 values of various customary pulse processing architectures with common measurement time T_{meas} enforced; $i_p^2 = 2eI_0 + \frac{4kT}{R_p}$, $v_s^2 = 4kTR_s$

noise. An ideal triangular weighting function performs best if there was only serial noise present; the serial noise for the triangular filter (for 0 % error) is $\frac{v_s^2}{2} C_{in}^2 \cdot 2/T_{meas}$, which has to be compared to $\frac{v_s^2}{2} C_{in}^2 \cdot 2.076/T_{meas}$ for the deconvolution method. With the 10 % error criterium both methods even perform equally well ($\mathrm{ENC}_s^2 = \frac{v_s^2}{2} C_{in}^2 \cdot 1.80/T_{meas}$). The deconvolution method thus is very close to the optimum processing for serial noise.

The deconvolution method is superior to all other real world circuits; unfortunately, the realization as a switched-capacitor filter is relatively complex and the processing time has to be taken into account. In the present realization [Fre95] the dead time is considerable since every sample may be used only once for processing; thus a signal in one bunch crossing prohibits the evaluation of the following two bunch crossings. If we include this dead time into the measurement time for a fair comparison (i. e. $T_{meas} = 3\Delta t$), we come to an $\mathrm{ENC}_s^2 = \frac{v_s^2}{2} C_{in}^2 \cdot 6.23/T_{meas}$ which is hardly any better than the value obtained with single sampling of the shaper output. Futhermore, due to the very pronounced peak timing jitter of the sampling w. r. t. the signal arrival acts detrimental. Due to the large effort (SC-filter !) required and due to the dead time the deconvolution method was not selected for HELIX128S-2.

The correlated sampling methods directly at the charge amplifier's output perform second best. The effort for the quadruple voltage sampling does not pay off, so that we will restrict discussion to the double correlated voltage sampling. Double correlated sampling can be implemented with little effort; it has to be admitted, however, that for $T_{meas} = 2.30\tau_{amp}$ every sample has to be used twice (i. e. as "signal" sample and as "reference" sample) which may cause additional circuitry. If a sample reuse cannot be achieved (hence $T_{meas} = 4.60\tau_{amp}$), the time-refered serial noise rises to $\mathrm{ENC}_s^2 = \frac{1}{2} C_{in}^2 \cdot 5.09/T_{meas}$. Thus, referred to the double correlated sampling without sample reuse, single sampling of the semigaussian shaper output performs only slightly worse – the (unsquared) ENC's differ by 19 %.

In the HELIX128S-2 chip single sampling at a shaper output was employed. This was done due to the fact that semigaussian shaping is a very well established method [Beu90, CS91, Com96, Nyg92, Hal53, Hu95, HN95, Kno97, Ort95] getting along with a single sampling clock; digital signals can be kept far from the amplifier inputs; there is, however, the difficulty to design a shaper with a well defined shape (without undershoot) and peak time.

With double correlated sampling digital signals in close distance to the charge amplifier may couple to its very sensitive input. Also, since all amplification is already needed at the charge amplifier output, it may be difficult to reach the necessary rise time.

Chapter 7

Integrated Charge Amplifier Design

7.1 Stability and Bandwidth

7.1.1 Introduction

The issue of stability is often underestimated when designing charge amplifiers - this is due to the fact that the feedback capacitor *Miller-compensates* the amplifier (there will be more on this subject) thus stabilizing its response. This nice feature unfortunately does not hold for current amplifiers which are now widely discussed in high energy physics. It should be kept in mind, however, that all other considerations only make sense if stability in a system is provided.

The following general treatment of stability follows the excellent treatment of Laker and Sansen [San94, p. 200 ff].

Stability denotes a system state in which all bounded excitations produce bounded response. This means in other words that the output of a stable circuit cannot diverge (i. e. go to a limit given by the power supplies) for an input of limited amplitude. Neither can a stable circuit sustain oscillations in the absence of a source. Passive RLC networks are stable by nature since they do not contain energy sources (i. e. the input signal energy denotes an upper limit for the output signal energy). Active circuits, on the other hand, contain energy sources that can combine constructively with the input or each other to cause the output to diverge or oscillate. A circuit has to be stable for all frequency ranges (since excitations can happen at all frequencies); it does not have to be stable for all values of input or output impedances since those are usually fixed. Even if a feedback system is stable, its response to transient excitations can be unsatisfactory (e. g. damped oscillation).

Fig. 7.1 shows the block diagram of a basic feedback circuit. Solving the corresponding equation system in the domain of the Laplace-transform

$$\begin{array}{lrcl} \text{I.} & V_{out}(s) & = & A(s) \cdot V_e(s) \\ \text{II.} & V_{fb}(s) & = & H(s) \cdot V_{out}(s) \\ \text{III.} & V_e(s) & = & V_{in}(s) - V_{fb}(s) \end{array} \tag{7.1}$$

yields

$$V_{out}(s) = \frac{A(s)}{1 + A(s)H(s)} V_{in}(s) := \frac{A(s)}{1 + T(s)} V_{in}(s) := A_{CL}(s)V_{in}(s) \quad . \tag{7.2}$$

$A(s)$ (frequency dependent) open-loop gain
$H(s)$ feedback factor
$V_{in}(s)$, $V_{out}(s)$, $V_{fb}(s)$, and $V_e(s)$ source, output, feedback, and error voltages signals w. r. t. ground
A_{CL} closed loop gain
$T(s)$ loop gain

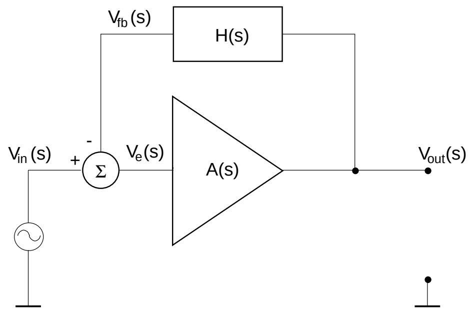


Figure 7.1: Basic feedback circuit

Since $A(s)$ usually is big for the frequeny range of interest, the error voltage $V_e(s)$ becomes small. The poles of the feedback system transfer function are defined by the characteristic equation (7.3).

$$1 + A(s)H(s) = 1 + T(s) = 0 \quad . \tag{7.3}$$

For a stable closed-loop system, all roots must lie in the left-half s-plane (Im(s)<0).

Besides the effort of factoring a high order polynomial (which is nowadays simplified by the use of symbolic calculation programs), the result offers little indication as to the margins by which stability is achieved. To achieve more insight into the stability margin we can rewrite eq. (7.2) in the frequency domain (i. e. in the domain of the Fourier transform) by substituting $s = j\omega$:

$$V_{out}(j\omega) = \frac{A(j\omega)}{1 + A(j\omega)H(j\omega)} V_{in}(j\omega) := \frac{A(j\omega)}{1 + T(j\omega)} V_{in}(j\omega) \tag{7.4}$$

For $\phi(T(j\omega))$ =-180° the loop-gain becomes negative (and real), and the feedback is positive. If then $|T(j\omega)| < 1$, $A_{CL}(j\omega) > A(j\omega)$, but the system is still stable. For $|T(j\omega)| = 1$, the closed loop gain becomes infinite and the system becomes unstable; it oscillates at the corresponding frequency ω. For $|T(j\omega)| > 1$ the oscillation will grow in amplitude, until it is finally limited by some nonlinearity.

7.1.2 Current Amplifier

We start with a revision of the current amplifier w. r. t. stability. Special focus of the discussion will be put on the pole location and particularly on the impact of poles of the open-loop amplifier cell on stability.

Consider fig. 7.2. For the determination of the open-loop gain $A(s)$ and the feedback factor $H(s)$ we regroup the circuit taking into consideration input and output impedances. The resulting circuit is plotted in fig. 7.3.

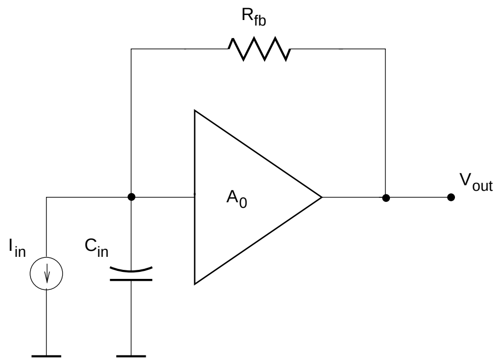


Figure 7.2: Current amplifier with capacitive source impedance

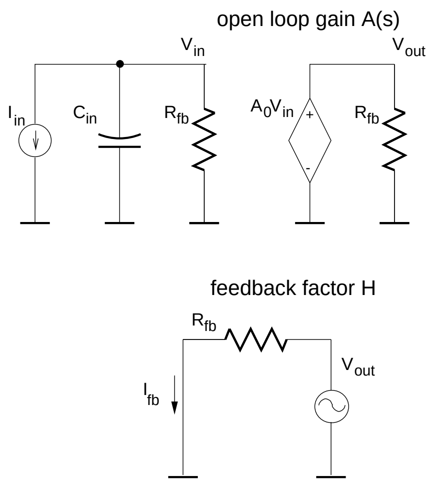


Figure 7.3: Current amplifier regrouped to determine A(s) and H(s); shunt-shunt feedback is employed.

Let us assume the open-loop amplifier to be pole-free, $A_0(s) = A_0$. In a straight forward calculation the resulting open-loop gain (which has to take into account the input impedances) becomes

$$A(s) = \frac{A_0 R_{fb}}{1 + sC_{in}R_{fb}} = \frac{A_0 R_{fb}}{1 + s/\omega_0} \quad . \tag{7.5}$$

Due to the capacitive source impedance a pole at the amplifier input arises. Note that the open loop gain has the unit $[\Omega]$ since it transduces an input current into an output voltage. The feedback factor $H(s)$ is independent from frequency

$$H = \frac{1}{R_{fb}} \tag{7.6}$$

with the unit $[1/\Omega]$. Calculation of the closed-loop gain yields

$$A_{CL} = \frac{A(s)}{1 + A(s)H(s)} = \frac{\frac{A_0}{1+A_0} R_{fb}}{1 + s\frac{C_{in} R_{fb}}{1+A_0}} = \frac{\frac{A_0}{1+A_0} R_{fb}}{1 + s/\omega_0'} \tag{7.7}$$

with $\omega_0' = (1 + A_0)\omega_0$. Hence, the open-loop pole is shifted along the negative real axis to a higher (negative) value (see fig. 7.4), i. e. we observe the well-known phenomenon of bandwith extension by employing negative feedback to a system. Another very desirable feature is that the gain is almost independent from A_0 due to $A_0/(1 + A_0) \approx 1$. Thus the closed loop gain can be made almost only dependent on a passive component (i. e. a resistor) which is less prone to manufacturing tolerances, temperature, and aging. Since the pole never can leave the left-half s-plane for any value of H, we conclude that a current amplifier with no pole in the open-loop cell is stable under all circumstances. This can also be seen from the phase shift never exceeding -90°; in consequence, the system never reaches the point of positive feedback. The step response of the zero-pole

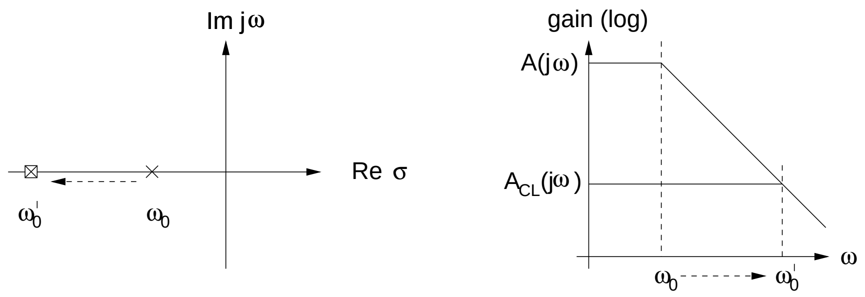


Figure 7.4: Effect of feedback on pole location and closed loop gain for current amplifier with capacitive source and zero-pole (infinite bandwidth) open loop core cell

current amplifier thus is simply given by an exponential rise (fig. 7.5) with the time constant $\tau = 1/\omega_0'$:

$$f(t) = R_{fb}(1 - e^{-t/\tau}) \tag{7.8}$$

A zero pole open-loop cell, however, is physically impossible implying an infinite bandwidth.

Next, we want to discuss a single-pole gain cell. We assume the additional pole to arise at the amplifier's output, i. e. we replace the output voltage source in fig. 7.3 by a more realistic current source with high source impedance R_{load} (fig. 7.6). The open-loop gain cell thus becomes a transadmittance cell.

The open-loop transfer function including the input- and output impedances is given by

$$A(s) = \frac{A_0 R_{fb} R_{out}}{(1 + sC_{in}R_{fb})(1 + sC_{load}R_{out})} = \frac{A_0 R_{fb} R_{out}}{(1 + s/\omega_1)(1 + s/\omega_2)} \tag{7.9}$$

with $R_{out} = R_{fb}||R_{load} \approx R_{fb}$ and with H(s) being again

$$H = \frac{1}{R_{fb}} \quad . \tag{7.10}$$

We assume the two poles of the open-loop transfer function to be spaced widely apart such that the input pole is the dominant one ($C_{in} \approx$ 10pF, C_{load} some 100 fF). For

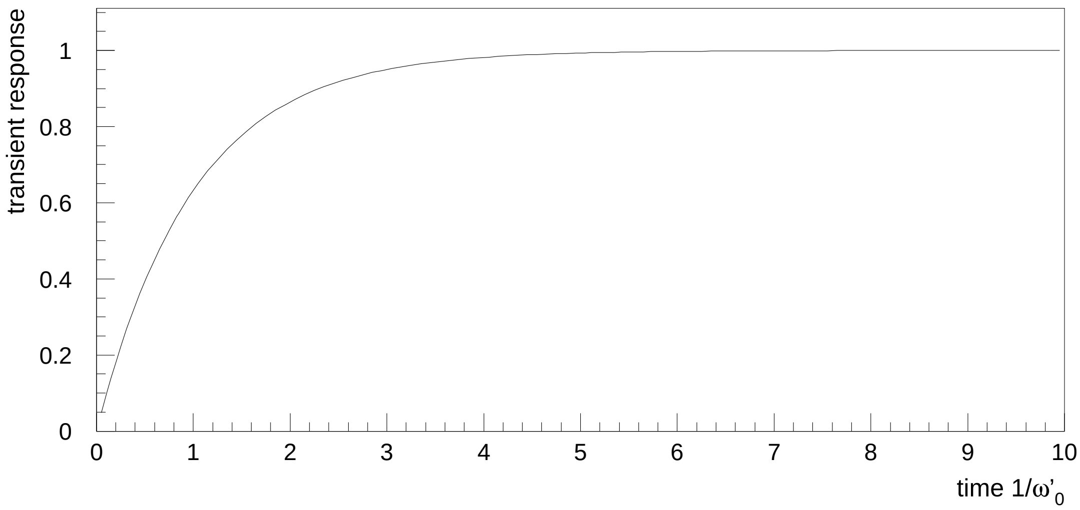


Figure 7.5: Step response of the current amplifier with zero pole open loop gain cell; $\omega_0' = (1 + A_0)\omega_0$

$s \gg \omega_1$ which is usually the case eq. (7.9) becomes

$$A(s) \approx \frac{A_0 R_{fb} R_{out} \omega_1}{s(1 + s/\omega_2)} \quad . \tag{7.11}$$

The closed-loop transfer function is given by inserting eq. (7.9) into eq. (7.2) yielding

$$A_{CL}(s) = \frac{A_0 R_{fb} R_{out} \omega_1 \omega_2}{1 + B(s)/R_{fb}} \tag{7.12}$$

with

$$\begin{aligned} 1 + B(s)/R_{fb} &= s^2 + s(\omega_1 + \omega_2) + (1 + A_0 R_{out})\omega_1\omega_2 \\ &= (s + \omega_1')(s + \omega_2') \quad . \end{aligned} \tag{7.13}$$

The closed loop pole locations are given by

$$\omega_1', \omega_2' = \frac{1}{2}(\omega_1 + \omega_2) \pm \frac{1}{2}\sqrt{(\omega_1 + \omega_2)^2 - 4(1 + A_0 R_{out})\omega_1\omega_2} \quad . \tag{7.14}$$

The locations of the poles are plotted in fig. 7.7. This plot is referred to as root locus diagram. For small $A_0 R_{out}$ there are two poles lying on the real negative axis of the s-plane (close to ω_1 and ω_2, respectively). As $A_0 R_{out}$ increases, the poles ω_1', ω_2' move toward each other and become coincident for the root in eq. (7.14) being zero. Further increasing $A_0 R_{out}$ leads to complex conjugate poles. Since the poles remain in the left-half s-plane for all values of $A_0 R_{out}$, the system is stable. However, the transient response has to be considered. Fig. 7.8 shows the step response of the system for different values of the dampfing factor ζ defined by

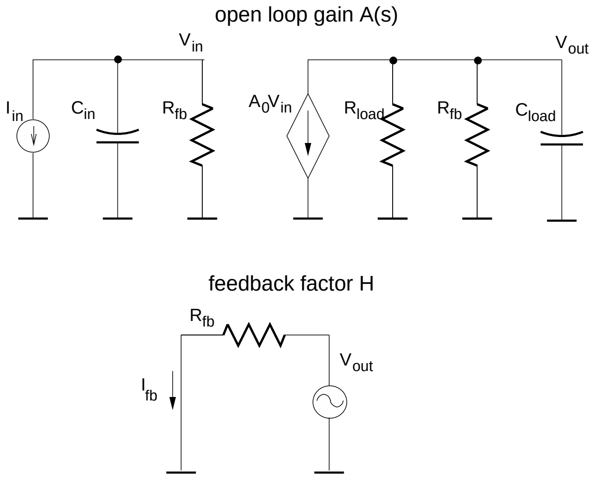


Figure 7.6: Current amplifier with single-pole open-loop gain cell

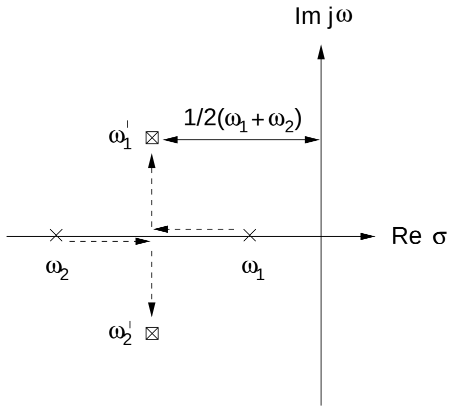


Figure 7.7: Effect of feedback on pole location of a current amplifier with capacitive source and single-pole open loop gain cell

$$\zeta = \frac{1}{2}\frac{\omega_1 + \omega_2}{\sqrt{(1 + A_0 R_{out})\omega_1\omega_2}} \quad . \tag{7.15}$$

The time axis of plot 7.8 is given by $1/\Omega_0$ with $\Omega_0 = \sqrt{(1 + A_0 R_{out})\omega_1\omega_2}$. The system response is said to be underdamped for $\zeta < 1$, for $\zeta = 1$ the system is critically damped. For $\zeta > 1$ which is not plotted in fig. 7.8 the system is said to be overdamped and the rise time increases with increasing ζ.

We want to determine the risetime for the critically damped current amplifier. For $\zeta = 1$ $\omega_1' = \omega_2' = 1/2(\omega_1 + \omega_2)$, i. e. the closed-loop transfer function

$$A_{CL}^{crit}(s) = \frac{A_0 R_{fb} R_{out}\omega_1\omega_2}{(s + \omega_1')^2} \tag{7.16}$$

has a double real pole with

$$\begin{aligned}\omega_1' &= \frac{1}{2}(\omega_1 + \omega_2)\\ &= \frac{1}{2}(\frac{1}{C_{in}R_{fb}} + \frac{1}{C_{load}R_{out}})\end{aligned}$$

$$\approx \frac{1}{2R_{fb}(C_{in} \oplus C_{load})} \tag{7.17}$$

where $\oplus$ denotes the series connection of capacitances. The risetime (10%-90%) is given by

$$t_{rise} = 3.6/\omega_1' = 7.2 \cdot R_{fb}(C_{in} \oplus C_{load}) \quad . \tag{7.18}$$

The risetime of the current amplifier depends only on feedback resistance and the load (=output) capacitance and thus is independent on the gain-cell's characteristic itself (if C_{load} is determined by the next stage's input capacitance); for R_{fb}=100 kΩ and C_{load}=100 fF one achieves t_{rise}=72 ns. This is very slow although a small load capacitance has been chosen. If the current amplifier's performance has to be sped up, a buffer stage driving the feedback current has to be introduced behind the gain stage.

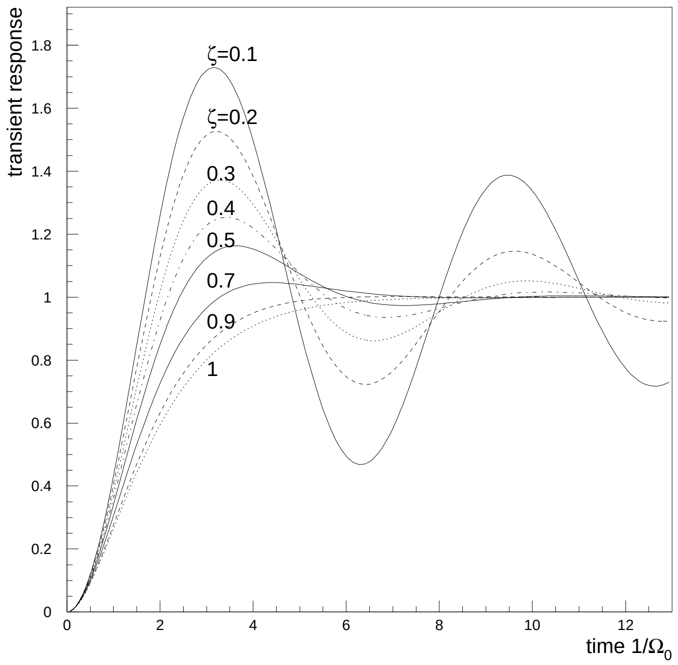


Figure 7.8: Step response of the current amplifier with one pole open loop gain cell (plus one input pole due to capacitive type source); $\Omega_0 = \sqrt{(1 + A_0 R_{out})\omega_1\omega_2}$

It becomes obvious that the transient behaviour of a current amplifier with a single pole in its core cell can already be unsatisfactoy due to the extra pole at the input node rendering the current amplifier with capacitive source effectively to a two-pole system.

For the inspection of a two-pole open loop gain cell respectively a three-pole system we refer the reader to [San94, p. 211 ff]. The additional pole worsens the phase shift resulting in more serious stability problems and even can render the system unstable.

7.1.3 Charge Amplifier

The charge amplifier is a transimpedance amplifier as the previously described current amplifier. However, due to the capacitive feedback the input pole is avoided, and the stability issue is greatly relieved as to the current amplifier. We start the discussion with the charge amplifier built around an zero-pole open loop voltage amplifier cell (fig. 7.9). As done in the subsection before we split the system into the forward open-loop path (including the loading by the feedback) and the feedback path to determine open-loop gain $A(s)$ and feedback factor $H(s)$ (see fig. 7.10).

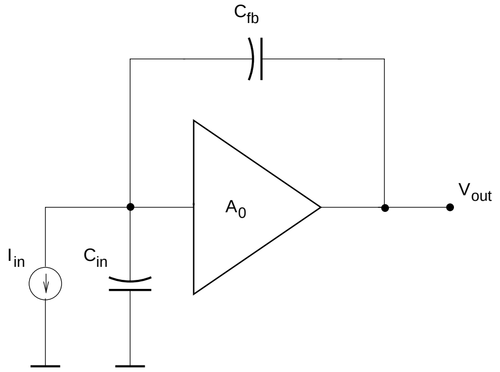


Figure 7.9: Charge amplifier

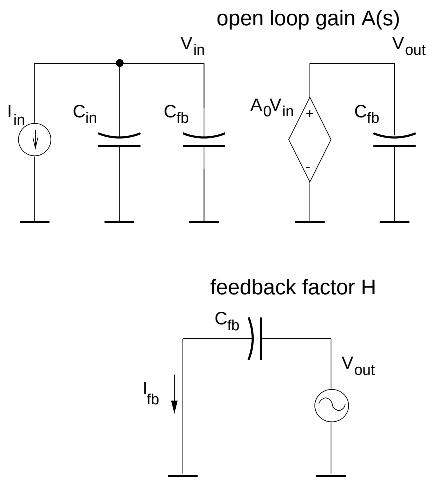


Figure 7.10: Charge amplifier feedback circuit

We obtain

$$A(s) = \frac{A_0}{s(C_{in} + C_{fb})} = \frac{A_0}{sC_{in,tot}} \tag{7.19}$$

and

$$H(s) = sC_{fb} \quad . \tag{7.20}$$

The closed loop gain becomes

$$A_{CL}(s) = \frac{1}{sC_{fb}(1 + 1/A_0) + sC_{in}/A_0} \approx \frac{1}{sC_{fb}} \quad . \tag{7.21}$$

We observe one pole located at the origin as expected for an integrator. We know, that the imaginary axis forms the stability boundary, and indeed, an integrator is unstable (and therefore some means of reset must be provided). This is, however, a feature which lies within the nature of an integrator itself and has nothing to do with the unstability described before. The response to a δ-current pulse of the zero pole charge amplifier is an ideal step.

Next, we want to consider a single pole amplifier cell, i. e. we replace the output voltage source by a current source with RC-load. (fig. 7.11)

The corresponding open-loop amplifier characteristic is given by

$$A_0(s) = \frac{A_0 R_{load}}{1 + sC_{load}R_{load}} \quad . \tag{7.22}$$

The open-loop transfer function hence becomes

$$A(s) = \frac{A_0 R_{load}}{s(C_{in} + C_{fb})(1 + sC_{out}R_{load})} = \frac{A_0 R_{load}}{s(C_{in} + C_{fb})(1 + s/\omega_1)} \tag{7.23}$$

with $C_{out} = C_{load} + C_{fb}$. $H(s)$ again is given by

$$H(s) = sC_{fb} \quad . \tag{7.24}$$

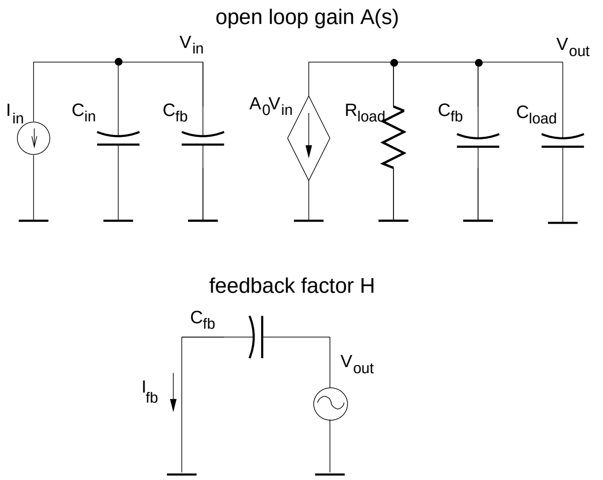


Figure 7.11: Charge amplifier with capacitive source and pole at the amplifier output

Assuming that $Re(s) \gg \omega_1$ the closed loop gain can be found to be

$$A_{CL} = \frac{1}{sC_{fb}(1 + s\frac{C_{in,tot}C_{out}}{A_0 C_{fb}})} = \frac{1}{sC_{fb}(1 + s/\omega_1')} \quad . \tag{7.25}$$

Beside the integrating pole we now observe a second pole

$$\omega_1' = \frac{A_0 C_{fb}}{C_{in,tot}C_{out}} = \text{GBW}\frac{C_{fb}}{C_{in,tot}} \tag{7.26}$$

appearing on the negative real axis. GBW denotes the gain-bandwidth product of the open loop amplifier cell (including the loading of the feedback circuit) and is defined as the product of low frequency gain $A_0 R_{load}$ and the amplifier output pole $(R_{load}C_{out})^{-1}$ (in rad/s).

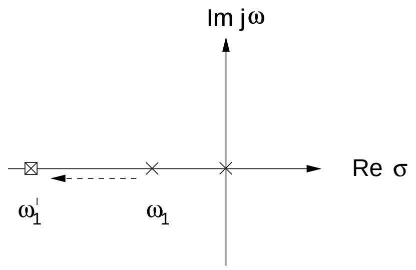


Figure 7.12: Effect of feedback on the pole location for a charge amplifier with a single-pole open loop gain cell

Thus, as in the case of the current amplifier, the pole of the open-loop gain cell ω_1 is shifted to the left (to higher negative values) by the effect of the feedback (see fig. 7.12). The pole given by (7.26) will show up throughout chapter 8 when we discuss the charge sensitive amplifiers in the HELIX128-S2 readout chip.

The response to an input delta pulse is given by an exponential rise

$$f(t) = \frac{1}{C_{fb}}(1 - e^{-t/\tau}) \tag{7.27}$$

where $\tau = 1/\omega_1'$ (see fig. 7.5).

The risetime of the charge amplifier with single-pole amplifier cell is given by

$$t_{rise} = 2.2/\omega_1' = \frac{2.2}{\mathrm{GBW}} \frac{C_{in,tot}}{C_{fb}} \quad . \tag{7.28}$$

For some typical values refer to the Helix-preamplifier discussion in chapt. 8.2. Eq. (7.28) has to be compared to eq. (7.18) of the one-pole gain-cell current amplifier amplifier.

It might be interesting to consider the maximum speed obtainable with a charge amplifier: by increasing C_{fb}, C_{out} can be made approximately C_{fb} (see also the stability discussion below). The minimum rise time is then given by

$$t_{rise,min} = \frac{2.2C_{in}}{A_0} = \frac{2.2C_{in}}{g_m} \tag{7.29}$$

with g_m the transconductance of the input transistor. For a risetime of 10 ns at C_{in}=20 pF g_m must be 4.4 mV/A which is well obtainable with MOS transistors.

It can be concluded, that for capacitive feedback as employed in a charge sensitive amplifier with single-pole core cell we don't run into any oscillation problem as in the case of the current amplifier. A two-pole open loop transfer characteristic is needed in case of a charge amplifier to drive the poles off the real axis (or cause an oscillatory behaviour).

The precondition for stable operation of such a system can be inferred from the well-known stability condition for voltage amplifiers with resistive feedback. We note that the stability of a voltage amplifier where $R_1 \rightarrow C_{in}$ and $R_2 \rightarrow C_{fb}$ has been substituted (notation as in fig. 4.3 right) must be the same as the one of the charge amplifier (since we only re-interprete the same circuit). The voltage division by the capacitive divider is frequency-independent as with a resistive divider, i. e. the circuit is indeed a voltage amplifier.

For unity-gain operation (gain defined by C_{in}/C_{fb}) the nondominant pole must be located well above the gain-bandwidth-product (a factor of 1.22 is sufficient for a right-hand-plane zero at infinity ($\geq 10\cdot$ GBW) to obtain a 45 % phase margin [AH87]). The charge sensitive preamplifier described in sect. 8.2 operates with "gains" of approx. 10..50 depending on the attached detector capacitance and hence needs not fulfill the tight unity-gain-condition; its phase margin is easily made approx. 90° 8.. A more formal deduction of a charge amplifier's stability using microwave theory (Rollet stability factor [MG92]) can be found in [Ike96].

7.2 Charge Amplifier Noise in Detail

In a good design the overall noise is only determined by the input transistor as first amplification stage and the pulse processing architecture. Therefore, the noise performance can be calculated without further knowledge of the details of the amplifier architecture.

Since we consider the conventional CR-RC-shaping circuit, the noise evaluation can also be performed in the frequency domain which has the additional advantage that the 1/f-noise can be handled. Therefore, we will use the frequency domain for the following calculation of noise in a charge amplifier with both a MOSFET and a bipolar input transistor. The results can be compared to those obtained with the time domain approach. Furthermore, we will deduce the noise matching conditions which yield the optimum noise performance for a charge amplifier with MOS or bipolar input transistor.

In fig. 7.13 we replot the amplifier model from fig. 4.8 in chapter 4 with the shaper added.

The detector is modeled by a current source with parallel capacitive and ohmic output impedance. Detector leakage current causes shot noise i_{sn}^2. The input transistor noise is given by the input equivalent noise sources v_s^2 and i_p^2. The feedback resistor contributes another parallel noise current i_{fb}^2. In the following we will omit the noise of the detector bias resistor which is needed for AC-coupling.

The input equivalent noise has been calculated in eq. (4.24) resp. in eq. (4.25) and is repeated for convenience in eq. (7.30) with the correlation term added:

$$q_{ineq}^2 = \frac{4kT}{R_{fb}|j\omega|^2}+\frac{i_{sn}^2}{|j\omega|^2}+\frac{i_p^2}{|j\omega|^2}+v_s^2(C_{in}+C_{fb})^2+2\frac{i_p}{|j\omega|}v_s(C_{in}+C_{fb})\mathrm{corr}(i_p,v_s) \quad [\text{in C}^2/\text{Hz}] \quad . \tag{7.30}$$

7.2.1 MOS Input Transistor

In case of a MOSFET input transistor we have to pay attention to the correlation of the two input sources i_p^2 and v_s^2 which are 100 % correlated (neglecting the gate resistance noise, eq. (B.4)) according to

$$v_s = \frac{1}{|j\omega|(C_{gs}+C_{gd})}i_p \quad . \tag{7.31}$$

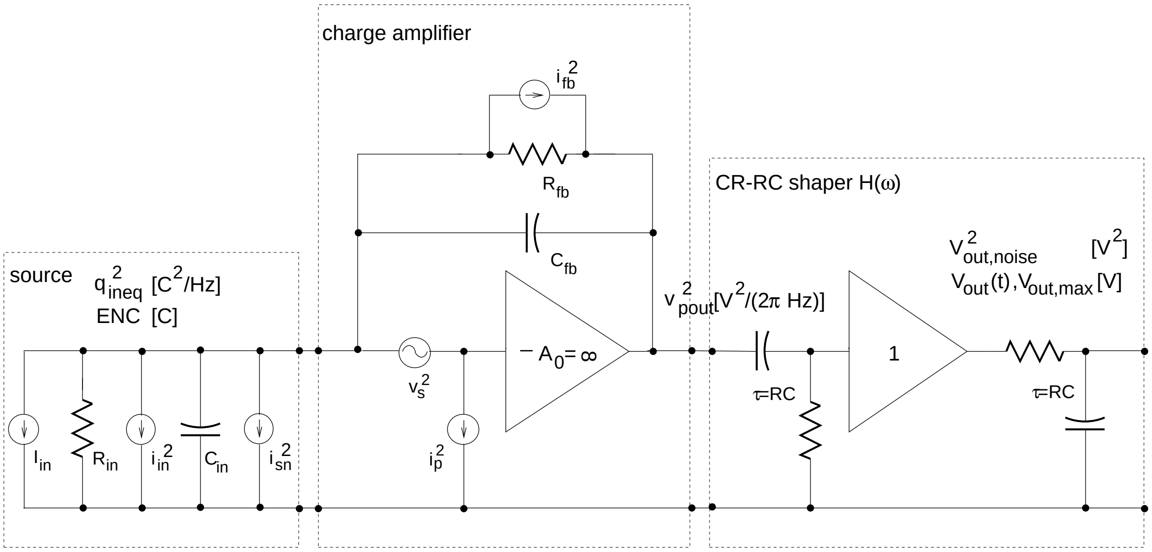


Figure 7.13: Charge amplifier (including all noise sources) with semi-Gaussian CR-RC shaper; the shaper is assumed to be noiseless.

Thus, we can rewrite eq. (7.30) to be [Nyg92]

$$q_{ineq}^2 = \left(\frac{4kT}{R_{fb}} + i_{sn}^2 \right) \frac{1}{|j\omega|^2} + v_s^2 (C_{gs} + C_{gd} + C_{in} + C_{fb})^2 \quad [\text{in C}^2/\text{Hz}] \quad . \tag{7.32}$$

The shot noise i_{sn}^2 in eq. (7.32) is given by

$$i_{sn}^2 = 2qI_0 \quad [\text{in A}^2/\text{Hz}] \quad . \tag{7.33}$$

I_0 detector leakage current

$q = 1.6 \cdot 10^{-19}$C elementary charge

The noise source v_s^2 is given by

$$v_s^2 = \frac{8kT(1+\eta)}{3g_m} + \frac{K_F}{2\mu_0 C_{ox}^2 W L \nu} \quad [\text{in V}^2/\text{Hz}] \quad . \tag{7.34}$$

g_m transistor transconductance

$\eta = g_{mbs}/g_m$ ratio of bulk-source transconductance to (gate) transistor transconductance

C_{ox} oxide capacitance per unit area

W,L MOSFET channel's width and length

K_F flicker noise coefficient

μ_0 channel charge carrier mobility

$k = 1,38 \cdot 10^{23}$J/K, T absolute temperature

Until now the noise spectrum was given "per frequency ν". Going over to a ω-referred noise density and refering the noise charge density q_{ineq}^2 to the output of the charge amplifier yields

$$v_{pout}^2(\omega) = \frac{1}{2\pi}\left(\frac{4kT}{R_{fb}} + i_{sn}^2\right)\frac{1}{C_{fb}^2|j\omega|^2} + \frac{1}{2\pi}v_s^2\frac{(C_{gs}+C_{gd}+C_{in}+C_{fb})^2}{C_{fb}^2} \quad . \tag{7.35}$$

The first term with the $1/|j\omega|^2$ dependency is due to the parallel noise current sources related to the detector leakage current and the feedback resistor; the second term gives the noise contribution due to the (serial) transistor noise. The charge amplifier output noise spectrum is filtered by the shaper circuit as indicated in fig. 7.13; the semi-gaussian shaper consists of a CR-high pass followed by a RC-low pass where we assume that no loading happens. The transfer function of the shaper can directly be inferred from fig. 7.13 and is given by

$$H(\omega) = \left(\frac{j\omega\tau}{1+j\omega\tau}\right)\left(\frac{1}{1+j\omega\tau}\right) \tag{7.36}$$

resp.

$$|H(\omega)| = \frac{\omega\tau}{1+\omega^2\tau^2} \tag{7.37}$$

where $\tau = RC$ is the common time constant of high- and low pass. The noise spectrum behind the shaper thus becomes $v_{pout}^2(\omega)|H(\omega)|^2$; to obtain the output noise voltage we have to integrate the noise density over all frequencies

$$V_{out,noise}^2 = \int_0^\infty v_{pout}^2(\omega)|H(\omega)|^2\,d\omega \quad [\text{in V}^2] \quad . \tag{7.38}$$

To refer the output voltage to an input charge we calculate the pulse response of the overall system depicted in fig. 7.13 to a δ-current pulse with a total charge of Q_{in} yielding

$$V_{out}(t) = \frac{Q_{in}}{C_{fb}}\frac{te^{-\frac{t}{\tau}}}{\tau} \quad . \tag{7.39}$$

The pulse peak (see e. g. section 4.4.2) behind the pulse shaper happens at time τ after the current δ-pulse; its value equals

$$V_{out,max} = \frac{Q_{in}}{eC_{fb}} \quad . \tag{7.40}$$

The equivalent noise charge (ENC) then becomes

$$\text{ENC}_{tot}^2 = \frac{V_{out,noise}^2}{V_{out,max}^2}Q_{in}^2 = e^2C_{fb}^2\int_0^\infty v_{pout}^2(\omega)|H(\omega)|^2\,d\omega \quad [\text{in C}^2] \quad . \tag{7.41}$$

For better insight we will apply the integral (7.41) individually to the terms of eq. (7.35). The noise contribution of the charge amplifier feedback resistor R_{fb} gives

$$\text{ENC}_{Rfb}^2 = \frac{e^2\tau}{8}\left(\frac{4kT}{R_{fb}}\right) \quad . \tag{7.42}$$

The shot noise of the detector diode leakage current I_0 gives a contribution

$$\text{ENC}_{sn}^2 = \frac{e^2\tau}{8}(2qI_0) \quad . \tag{7.43}$$

The parallel noise contributions ENC^2 due to R_{fb} and I_0 are proportional to the shaper peak time τ; this can be understood from the noise spectrum behind the preamplifier rising proportionally to $1/\omega^2$ towards lower frequencies.

The serial noise contributions are due to the input transistor and can be separated into the (white) channel thermal noise

$$\mathrm{ENC}_{th}^2 = \frac{e^2}{8\tau}\left(\frac{8kT(1+\eta)}{3g_m}\right) C_{in,tot}^2 \tag{7.44}$$

with the abbreviation $C_{in,tot} = C_{gs} + C_{gd} + C_{in} + C_{fb}$ for the total input capacitance. The channel thermal noise increases with decreasing shaper time τ; hence the impact of τ on the serial noise is just opposite to that on the parallel noise. A trade-off has to be found when choosing the shaper time (if the shaper time is not restricted by the expected pulse rate).

The 1/f-noise gives rise to

$$\mathrm{ENC}_{1/f}^2 = \frac{e^2}{2}\left(\frac{K_F}{2\mu_0 C_{ox}^2 WL}\right) C_{in,tot}^2 \quad . \tag{7.45}$$

Hence, the 1/f-noise is independent of the shaper time; this behaviour can be understood intuitively by shifting a bandpass filter (since the shaper is nothing but a bandpass) with infinitely steep stop/pass-band transition with lower and upper limit frequency having a constant *logarithmic* distance over the 1/f-noise spectrum; the integral $\int_a^b 1/f\, df = \ln b - \ln a$ remains unaffected by the absolute center frequency of the filter.

Further noise sources as gate-resistance or bulk-resistance noise sometimes found in literature [Jin85, Jin86] are usually not of practical importance.

Since all noise sources are statistically independent, the total ENC_{tot}^2 is given by

$$\mathrm{ENC}_{tot}^2 = \mathrm{ENC}_{Rfb}^2 + \mathrm{ENC}_{sn}^2 + \mathrm{ENC}_{th}^2 + \mathrm{ENC}_{1/f}^2 \quad . \tag{7.46}$$

In fig. 7.14 we plot the various ENCs in electrons vs. shaper time τ for a charge amplifier with pmos input device. We assumed the detector leakage current to be 10nA and the detector capacitance to be 20 pF (feedback capacitance C_{fb}=500 fF, C_{gd}=500 fF). The drain current has been set to 200 μA, L to be 0.8μm, and W was chosen to be of optimum width (eq. (7.48)) W=5.89mm yielding g_m=10.2 mA/V. The flicker noise was chosen to be the one of the AMS 0.8μm CMOS process.

First of all it can observed that the 1/f-noise contribution is practically negligible ($\mathrm{ENC}_{1/f}$ = 62.5e$^-$) for the AMS 0.8 μm-process. It should be noticed here that AMS uses the slightly different HSPICE (NLEV=0) model where the 1/f-noise is given by

$$v_{1/f}^2 = \frac{2\pi KF\, I_d^{AF}}{C_{ox} L^2 \omega g_m^2}; \tag{7.47}$$

with the parameters AF=1.61 and KF=0.466·10^{-26}. The flicker noise corner frequency (i. e. the frequency at which the flicker noise equals the thermal noise) lies as low as 32 kHz for the input transistor. Since it can be assumed that progress will tend to further reduce this value, it can be concluded that flicker noise does not play any role for the design of charge amplifiers in modern mixed-signal CMOS processes anymore.

The minimum of ENC$_{tot}$ occurs for the given example at 507ns with ENC$_{tot}$ = 348 e$^-$. For τ=50ns the ENC$_{tot}$ equals 778 e$^-$.

It might be interesting to consider the case of an nmos transistor; then the 1/f-noise ENC$_{1/f}$=126e$^-$ is only slightly higher (even if $KF_{nmos} \approx 6KF_{pmos}$) since g_m is higher due to the mobility of electrons in the inversion channel. Then, the minimum occurs at τ=398ns with ENC$_{tot}$=325 e$^-$ and for τ=50ns ENC$_{tot}$=610 e$^-$. Thus, the nmos transistor is more favourable as input device due to its bigger g_m; however, for the Helix2.1 preamplifier a pmos input transistor was chosen due to its better radiation hardness.

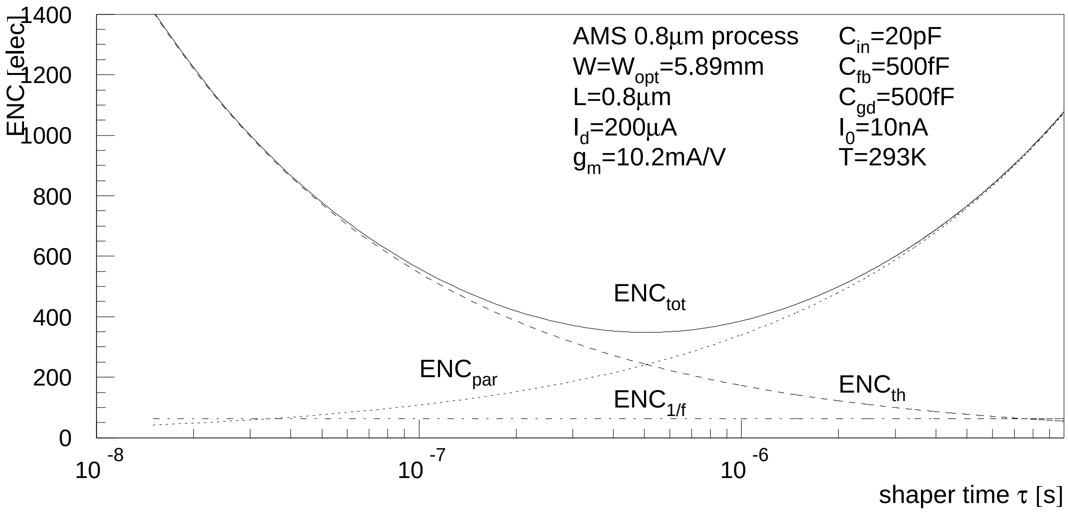


Figure 7.14: ENC (Equivalent noise charge) of the charge amplifier with pmos input; the parameters of importance are given in the picture.

Noise Optimization

Based on the equations derived in the previous subsection it is possible to deduce the conditions to minimize noise under special given constraints. In principle, the designer has four degrees of freedom in a CMOS design to achieve minimum noise performance: The input transistor's dimensions W and L, the drain current I_d, and the shaper time constant τ.

The value of I_0 (detector leakage current) and of R_{fb} (preamplifier feedback resistor) are usually not included in this optimization, since I_0 should be minimized (by choice of a "good" detector and – where possible – by avoiding radiation damage [Riech96]) and R_{fb} is to be maximized depending on AC/DC-coupling of the detector resp. the value of I_0 (since in case of DC-coupling I_0 flows over R_{fb} which can drive the preamplifier output to the rails). The drain current I_d should be maximized to minimize the serial noise contribution ($g_m \propto \sqrt{I_d}$) within the boundaries given by the maximum power consumption.

Looking closer at the serial noise terms eq. (7.44) and (7.45) and considering $g_m \propto \sqrt{\frac{W}{L}}$ and $C_{gs} \propto WL$, it becomes clear that an optimum $W = W(L)$ must exist that minimizes ENC_{th}; the same holds true for the 1/f-noise $\mathrm{ENC}_{1/f}$. The optimum width W of the input transistor cannot be determined in a closed form [CS91] for both thermal noise and 1/f-noise together, but it can be done separately. Inserting $g_m = \sqrt{2\mu_0 C_{ox} I_d W/L}$ and $C_{gs} = 2/3WLC_{ox}$ into eq. (7.44) and taking the derivative w. r. t. W yields

$$W_{opt,th} = \frac{C_{in} + C_{fb} + C_{gd}}{2LC_{ox}} \quad . \tag{7.48}$$

The same procedure delivers for the 1/f-noise

$$W_{opt,1/f} = 3\frac{C_{in} + C_{fb} + C_{gd}}{2LC_{ox}} = 3W_{opt,th} \quad . \tag{7.49}$$

Depending on the amount of 1/f-noise encountered for a given process and given shaper time τ, a value in between the two extremes given by eqs. (7.48) and (7.49) has to be chosen. It should, however, be pointed out, that for shaper times below 100 ns the 1/f-noise is absolutely negligible.

The shaper time τ appears in both serial and parallel noise terms. The serial thermal noise is inversely proportional to the shaper time τ, the parallel noise is proportional to τ, and the 1/f-noise is independent of it. Thus, a τ exists for which ENC_{tot} is minimized; derivation w. r. t. τ and equation to zero yields

$$\tau_c = C_{in,tot}\sqrt{\frac{8kT/(3g_m)}{2qI_0 + 4kT/R_{fb}}} \quad . \tag{7.50}$$

For τ_c (also called noise-corner time-constant) the contributions ENC^2_{th} and ENC^2_{Rfb}+ENC^2_{I0} are equal.

7.2.2 Bipolar Input Transistor

BICMOS processes offer both bipolar transistors and MOS transistors; due to their better drive capability (larger g_m, higher f_t) bipolar stages have become popular for very high-speed silicon strip-detector readout. In the following we want to examine the noise behaviour of a frontend using a bipolar transistor and compare it to the MOS transistor case as determined analytically in the previous section.

The input equivalent noise sources of the bipolar transistor are given by eq. (B.7) in appendix B and are repeated for convenience:

$$\begin{aligned} v_s^2 &= 4kT(r_b + \frac{1/2}{g_m}) \quad [\text{in V}^2/\text{Hz}] \\ i_p^2 &= i_b^2 + \frac{i_c^2}{|\beta_{AC}|^2} \\ &= 2eI_b + \frac{2eI_c}{|\beta_{AC}|^2} \quad [\text{in A}^2/\text{Hz}] \end{aligned} \tag{7.51}$$

where we assume both input voltage sources to be uncorrelated (see app. B). We insert eq. (7.51) into formula (7.30). We will not repeat all the steps as done in the MOS case, but will restrict ourselves to the final contributions of the individual noise sources.

The noise contribution of the charge amplifier feedback resistor R_{fb} (naturally) remains unaffected

$$\mathrm{ENC}^2_{Rfb} = \frac{e^2\tau}{8}\left(\frac{4kT}{R_{fb}}\right) \quad . \tag{7.52}$$

The same is valid for the shot noise of the detector diode leakage current I_0

$$\mathrm{ENC}^2_{I0} = \frac{e^2\tau}{8}\left(2qI_0\right) \quad . \tag{7.53}$$

The base current $I_b = I_c/\beta \approx I_c/\beta_{AC}$ gives rise to a shot noise contribution

$$\mathrm{ENC}^2_{Ib} = \frac{e^2\tau}{8}\left(\frac{2qI_c}{\beta}\right) \quad . \tag{7.54}$$

and the collector current yields

$$\mathrm{ENC}^2_{Ic} = \frac{e^2\tau}{8}\left(\frac{2qI_c}{\beta^2}\right) = \frac{1}{\beta}\mathrm{ENC}^2_{Ib} \quad . \tag{7.55}$$

and hence is negligible w. r. t. the base current shot noise.

The serial noise contributions are given by the collector current contribution

$$\mathrm{ENC}^2_{Ic,s} = \frac{e^2}{8\tau}\left(\frac{2kT}{g_m}\right)(C_{in}+C_{fb})^2 = \frac{e^2}{8\tau}\left(\frac{2(kT)^2}{qI_c}\right)(C_{in}+C_{fb})^2 \tag{7.56}$$

where we inserted for the transconductance

$$g_m = \frac{qI_c}{kt} \tag{7.57}$$

and the base resistance noise given by

$$\mathrm{ENC}^2_{rb} = \frac{e^2}{8\tau}\left(4kTr_b\right)(C_{in}+C_{fb})^2 \quad . \tag{7.58}$$

Since we assume all noise sources to be statistically independent, the total ENC^2_{tot} is given by

$$ENC^2_{tot} = \mathrm{ENC}^2_{Rfb} + \mathrm{ENC}^2_{I0} + \mathrm{ENC}^2_{Ib} + \mathrm{ENC}^2_{Ic} + \mathrm{ENC}^2_{Ic,s} + \mathrm{ENC}^2_{rb} \quad . \tag{7.59}$$

In fig. 7.15 we plot the various ENCs in electrons vs. shaper time τ for a charge amplifier with a bipolar input device. For better oversight we combined the parallel and serial noise sources together ($ENC^2_{par} = \mathrm{ENC}^2_{Rfb} + \mathrm{ENC}^2_{I0} + \mathrm{ENC}^2_{Ib} + \mathrm{ENC}^2_{Ic}$, $\mathrm{ENC}^2_{ser} = \mathrm{ENC}^2_{Ic,s} + \mathrm{ENC}^2_{rb}$). The parallel noise is dominated by the base current shot noise.

As in the previous section, we assumed the detector leakage current to be 10nA and the detector capacitance to be 20 pF; the base resistance of the input transistor was set to 30 Ω and β=100. The collector current I_c was chosen to follow the shaper time τ according to eq. (7.60) (i. e. for τ=50 ns $I_{c,opt}$=103 μA, for τ=10 ns $I_{c,opt}$=518 μA).

The minimum of ENC_{tot} occurs for the given example at 252ns with ENC_{tot} = 1122 e$^-$. For τ=50ns the ENC_{tot} equals 1164 e$^-$ at an optimum collector current of 103μA. These values are considerably worse than the ones achieved with the MOSFET.

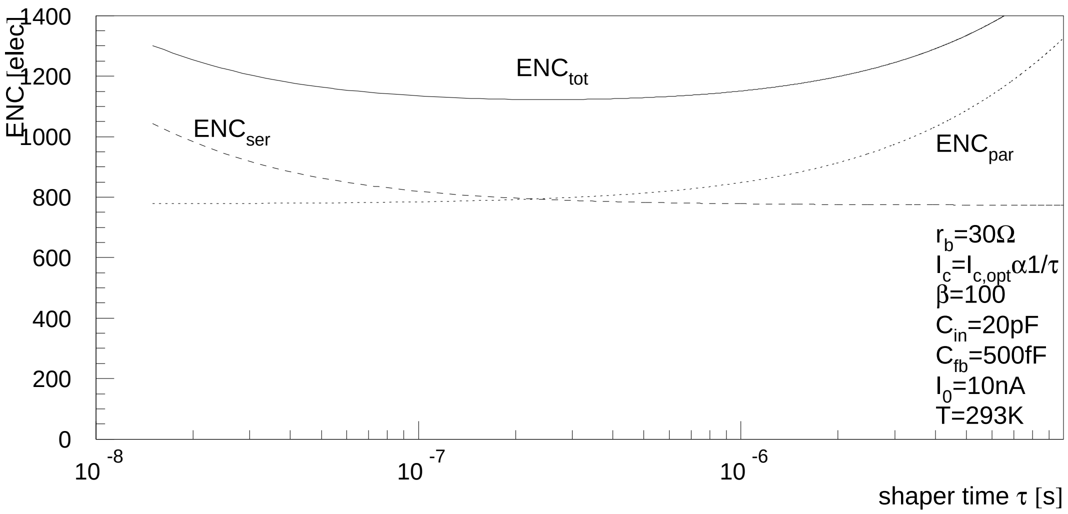


Figure 7.15: ENC (Equivalent noise charge) of the charge amplifier with bipolar input transistor with the parameters as given in the picture; the collector current is adapted to τ to achieve optimum noise performance.

It has to be noted, that a MOS input transistor of optimum width consumes much more space. The MOS amplifier does not necessarily consume more power even if in the example the drain current was set to twice the optimum collector current for a peaking time of 50ns. For a pmos with optimum width and I_d=100μA, ENC_{tot}=922 e$^-$ which is still below the value of 1164 e$^-$ for the bipolar transistor.

For shaper times smaller than 20ns the bipolar transistor in the example of fig. 7.15 takes over at steadily increasing collector current: at τ=10 ns $I_{c,opt}$=518μA is needed to achieve ENC_{tot}=1392 e$^-$. The drain current of the MOS transistor in the example of fig. 7.14 was set to 200 μA; admitting the same drain current $I_d = 518\mu$A the pmos version reaches 1362 e$^-$ which is still better than the bipolar value, and the nmos would even perform better ! A comparison of the ENCs of MOS vs. bipolar input transistor is given in fig. 7.16 where the MOS transistor's drain current has been chosen equal to the bipolar transistor's collector current to normalize w. r. t. power consumption.

Therefore, we conclude that the bipolar transistor's performance is principally inferior to the one achievable with a MOS transistor of optimum-width. This holds even for the lowest peaking times of interest.

Noise Optimization

It becomes immediately clear, that the transistor capacitances do not play any role in the bipolar amplifier noise performance; this is obviously true from the results obtained from eqs. (7.52) to (7.55) as results of the approximations made. How can this be better understood ? We look at the MOS transistor case: for an open gate the input equivalent noise current alone has to give rise to the drain noise current by definition (cf. appendix

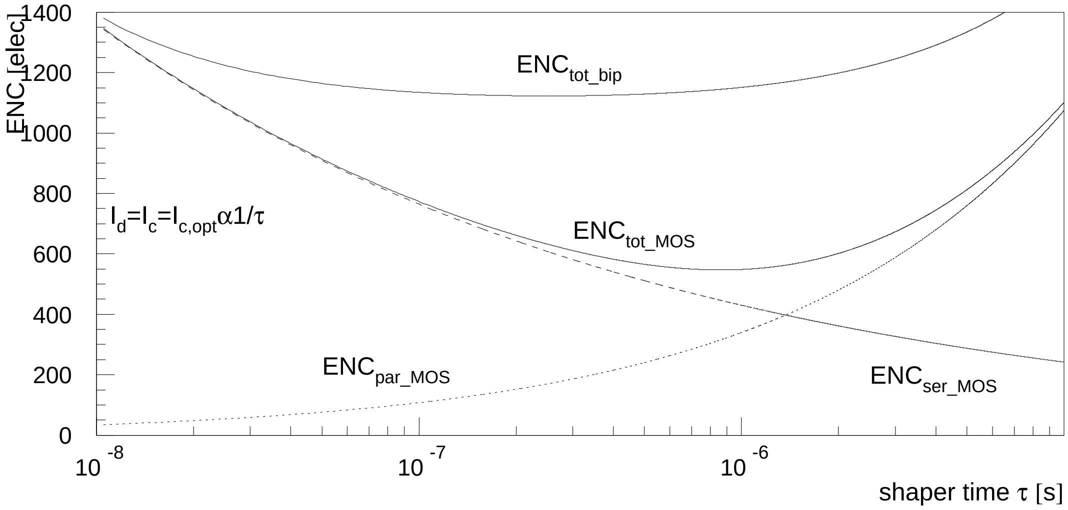


Figure 7.16: ENC (Equivalent noise charge) of charge amplifier with MOS and bipolar input transistor of equal drain/collector currents; other parameters equal those of figs. 7.15 and 7.14. The drain/collector current follows τ according to fig. 7.17.

B). Since the ohmic input resistance is infinite, the input noise current flows via C_{gs} and C_{gd} thus introducing a noise dependency on the transistor geometry.

For the case of the bipolar transistor the input impedance is not infinite, so that the input pole moves away from zero; for the freqencies usually under consideration $\omega < 1/(r_\pi(C_\pi + C_\mu)$ (cf. appendix B) the input noise current is independent from the capacitances C_π and C_μ but flows via r_π to ground; for frequencies beyond $1/(r_\pi(C_\pi + C_\mu)$ (as is the case of small shaper times) the input equivalent noise current due to the collector shot noise rises in an analogous manner as in the MOSFET case; however, the collector current shot noise contribution to the total input current noise is negligible as compared to the base current shot noise.

Since the current gain β is more or less constant for usual operating conditions and is mainly determined by the process, base resistance r_b and - more important - collector current I_c remain to be optimized by the designer. From eq. (7.58) it is clear that r_b should be as small as possible which is a task to be accomplished by good layout (number of base contacts, multiple emitters).

For the collector current a trade-off must be found between the requirements as imposed by eq. (7.54) and eq. (7.56). The optimum collector current hence is obtained by taking the derivative w. r. t. I_c and is given by

$$I_{c,opt} = \sqrt{\beta}(C_{in} + C_{fb})\frac{kT}{q\tau} \quad . \tag{7.60}$$

Hence, the optimum value of I_c depends on the shaper time τ exhibiting a fundamental difference to the MOSFET case where the optimization was independent of the shaper characteristic. For smaller shaping times more collector current is needed to keep the serial noise due to the collector current shot-noise constant.

The shaper time can be optimized in analogy to the MOSFET case; we obtain

$$\tau_c = C_{in,tot}\sqrt{\frac{4kT(r_b + 1/(2g_m))}{2qI_0 + 4kT/R_{fb} + 2qI_c/\beta + 2qI_c/\beta^2}} \quad . \tag{7.61}$$

Due to the much higher parallel noise sources of the bipolar transistor the noise-corner time-constant τ_c lies considerably under the value of the MOSFET transistor.

In fig. 7.17 the optimum collector current according to eq. (7.60) is plotted vs. shaper time. For τ=50 ns $I_{c,opt}$=103 μA, for τ=10 ns $I_{c,opt}$=518 μA. The transistor parameters as given in the plot equal those of fig. 7.15.

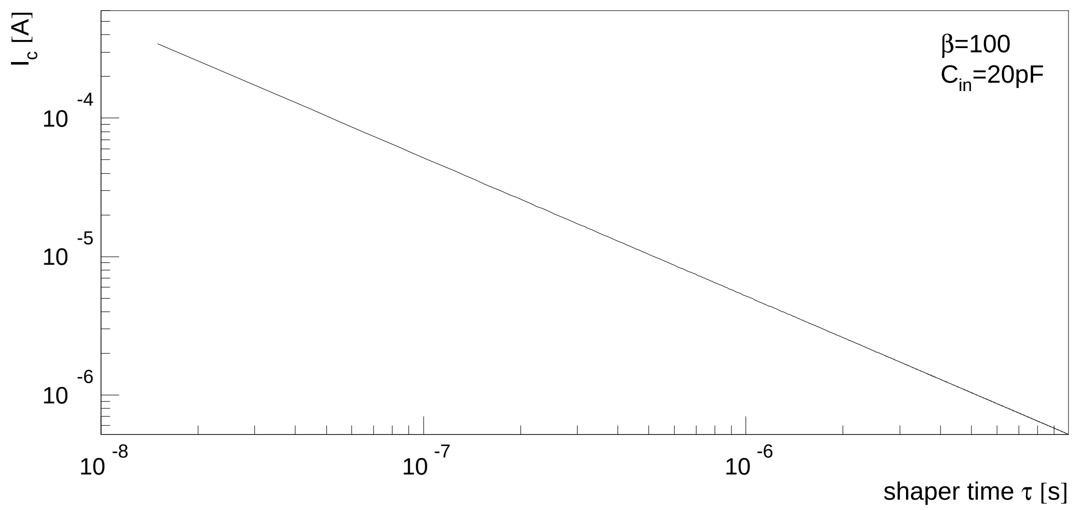


Figure 7.17: Optimum collector current $I_{c,opt}$ vs. shaper time τ for a bipolar input transistor

Current Amplifier

Recently current amplifiers with bipolar input transistors and a subsequent integrating stage have been introduced. As we have shown previously in this section, the current amplifier is more prone to instability than the charge amplifier. The spectral noise density of such an "ansatz" with the amplification and the integration splitted into two stages has been calculated in sect. 4.3.3 and is repeated here for convenience:

$$q_{ineq}^2 = 4kT\frac{1}{R_{fb}|j\omega|^2} + \frac{i_p^2}{|j\omega|^2} + \frac{v_s^2}{R_{fb}^2|j\omega|^2} + v_s^2C_{in}^2 \quad [\text{in C}^2/\text{Hz}] \tag{7.62}$$

From the first term in eq. (7.62) we observe that the feedback resistor contributes to the parallel noise as in the charge amplifier case, but with the current amplifier the value of R_{fb} lies considerably lower due to the gain requirement. In eq. (7.62) the charge amplifier term $v_s^2C_{fb}^2$ has been replaced by $\frac{v_s^2}{R_{fb}^2|j\omega|^2}$, i. e. a former serial noise contribution has become parallel. This term is alway neglectable as compared to the first term, since the equivalent series resistance R_{ser} given by $v_s^2 = 4kTR_{ser}$ is always in the (100-200)Ω range, whereas the feedback resistance R_{fb} as determined by the transconductance requirement is $\approx 100k\Omega$.

For the current amplifier with following integrating stage we conclude that the noise performance is always worse as the one obtained with a charge amplifier due to the lower value of R_{fb}. The current amplifier has become popular together with bipolar input transistors where the higher parallel noise due to the feedback resistor is partially "masked" by the base current shot-noise. Nevertheless, stability resp. speed and noise performance are less favorable than the one achievable with the single stage charge amplifier solution.

The current amplifier with following integrating stage can become interesting when the input current signals are too large to be directly integrated onto a capacitor; then the current can be down-divided and integrated in the subsequent stage; in this case the higher parallel noise is of minor importance.

Chapter 8

The HELIX Chip-Family

8.1 Introduction

HELIX128S-2 [Fal95-1, Fal95-2, Fal96, Fal97-2, Feu96, Tru97] is an analog readout-chip for silicon microstrip detectors and microstrip gaseous chambers specially suited to the needs of the HERA-B experiment; it has been manufactured in the 0.8 μm-CMOS process of AMS [AMS95-2]. The architecture has been inferred from the CERN-research group "RD20" [RD20-1, RD20-2, RD20-3, RD20-4] where the deconvolution processing circuit (cf. chapt. 6.3.2) has been abandonned, and where a comparator has been added behind each preamplifier/shaper.

HELIX128S-2 integrates 128 channels with low noise charge sensitive preamplifier/shapers (also called frontend) whose outputs are sampled (nominal sampling clock frequency 10.4 MHz) into an analog pipeline with a maximum storage space of 128 sampling values (see fig. 8.1). The decay-time of the shaped pulse has to be less than 96 ns (i. e. 1/10.4 MHz) to guarantee that a sample value is unaffected by a previous pulse - hence a pulse peak-time of approx. 50 ns with semi-gaussian shaping is required. Behind the preamplifier/shaper, each channel is equipped with an AC-coupled comparator. All comparators share a common threshold, the output of four neighbouring comparators being ORed and brought offchip.

Each cell of the pipeline is connected via a switch to the *write*-line (i. e. the frontend output) and via a switch to the *read*-line leading to the pipeline readout amplifier. The operation of the switches is controlled by a standard cell logic block; it receives incoming triggers, indicating interesting events w. r. t. the physics goal of HERA-B, tags the corresponding pipeline column (the cells corresponding to a common point of time reside in a column of the pipeline array) such that it is not overwritten by new data and stores the column number in a FIFO (max. eight events).

The oldest FIFO number indicates the pipeline column to be read out: the corresponding cells are switched to the *read*-lines and the charge is transferred to the pipeline readout amplifier; the read-operation is done concurrently from the write-operation. The pipeline readout amplifier loads a 128+8 to 1 analog multiplexer; 8 channels encoding the pipeline column the current event has been stored in, have been added to the multiplexer and appear as trailer in the analog multiplex-signal. The multiplexer operates at maximally 40 MHz making use of a cascaded architecture; its output signal is fed to

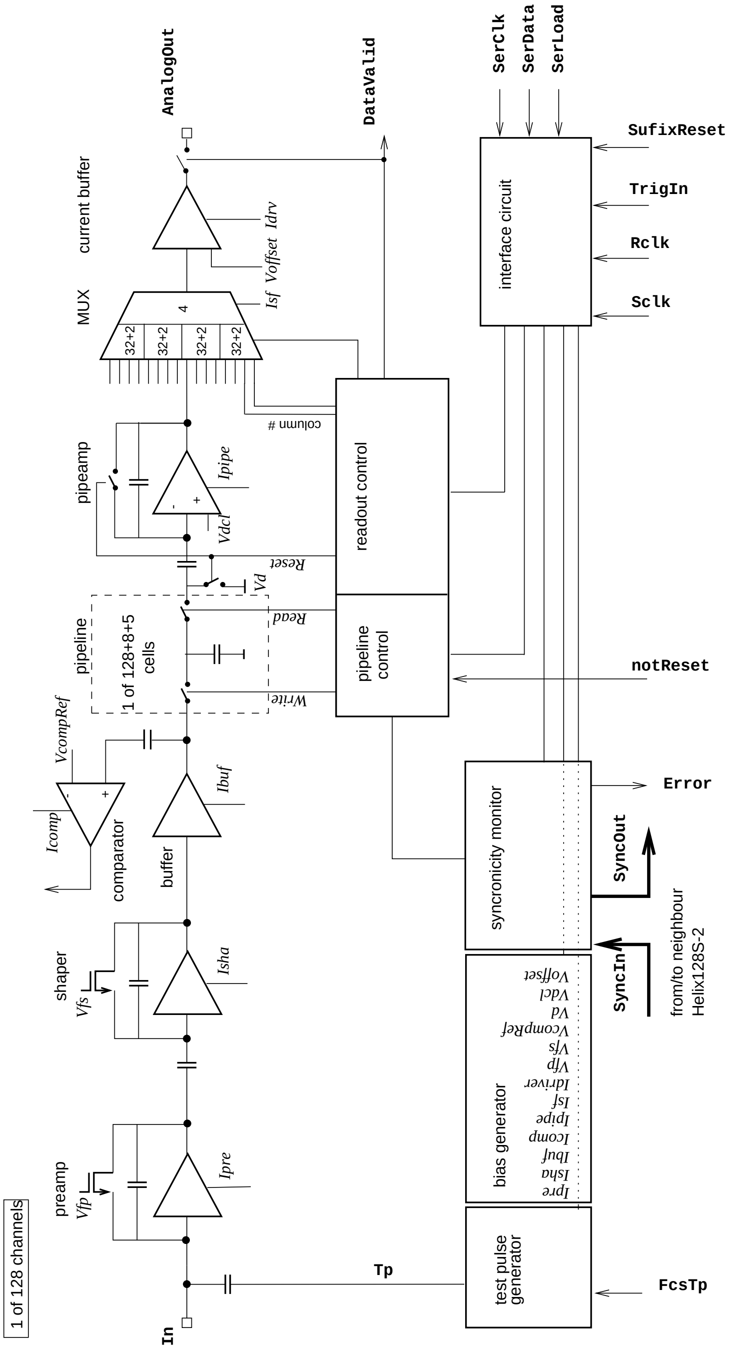


Figure 8.1: Block diagram of HELIX128S-2; the charge delivered by the detector is amplified by a preamplifier/shaper with its output sampled into the pipeline. A charge sensitive pipeline readout amplifier (the "pipeamp"), an analog multiplexer and a current buffer form the backend stages of the design. Bias settings of the chip can be programmed via a serial interface. Incoming triggers are handled by the pipeline control logic.

a low-power current output buffer which converts the voltage- to a current-signal; two chips can be daisy-chained and read out within 6.4 μs.

Since the chip has to withstand a considerable radiation dose of approx. 1-2 kGy during its lifetime, constant-current biasing has been excessively adopted for the various amplifier stages. Thus, the radiation-induced threshold-voltage shifts [AMS94, FWS88, Gov88] can be compensated.

However, due to radiation-induced mobility degradation, stages might become too noisy or too slow [Fal93, Fal94]. Therefore, current DACs are provided in the bias generating section to permit adjustment of the corresponding amplifier bias currents. Some amplifiers need bias voltages as well which are generated by programmable voltage DACs. The digital circuitry on the chip based on AMS standard cells is expected to withstand the expected dose (cf. [Dau88, Fal93, Fal94]).

Programming of the DAC-registers is done via the serial interface of three lines; a proprietary protocol has been developed (cf. the user manual in appendix D). The only further signals to be applied to the chip are the sampling clock `Sclk` (can also be created internally from the `Rclk`), the readout clock `Rclk` governing the multiplex-signal frequency, the trigger and a reset-signal.

To match the pitch of the silicon microstrip detectors an overall pitch of 50 μm can be obtained by placing Helix128S-2 chips side by side (the internal pitch of the fourfold staggered input pads is 41.4 μm, see fig. 8.2); the chip's size is 14.39 mm $\times$ 6.15 mm. The 128 input pads are located at the front of the chip w. r. t. the detector (the bottom side in fig. 8.2) while all pins necessary to operate the chip, i. e. power supply, digital control lines and analog output, are located at the rear side. The chip's trigger output pads are placed at the right side due to the relaxed space requirements of the HERA-B Inner Tracking Detector which makes use of the comparator information.

Above the input pads the frontend (preamplifier/shaper, buffer) and the comparator are visible, the latter with its fanout to the chips's right side. The regular block above the frontend part is the pipeline array of 129 x 141 capacitor cells; the pipeline control logic block is located at the right. Next follow the pipeline readout amplifier, analog multiplexer, and current buffer which form the backend stages of the signal chain. A column of "core pads" for testability reasons denotes the transition to the SUFIX-part with the serial interface at the right and the voltage and current DACs at the left.

The HELIX-chip has been developed in several submissions, starting in May '95 with the submission of a frontend consisting of a charge sensitive amplifier (CSA), a pulse shaper and a source follower in the AMS 1.2 μm CMOS process. Due to a somewhat increased shaper time ($\approx$ 100 ns) a renewed version was immediately submitted - called Helix 1.1 which remained for a long time the "workhorse" of the lab. HELIX 32 marked a new milestone integrating for the first time a complete system in a 32 channel version on a chip. HELIX 128 followed in april '97 with the transition from the AMS 1.2μm to the AMS 0.8μm process which became necessary by the scaled up pipeline control logics. SUFIX - a support and control chip for HELIX - was submitted in Oct. '96 to generate and adjust the analog bias voltages and currents. In parallel a new frontend - called Helix 2/2.1 - and a modified output buffer were submitted and worked well, so that a completely overworked analog (and digital) 128 channel chip was submitted in March '97, called HELIX128S-2, also incorporating the SUFIX part.

The Helix frontend has been submitted in different versions on different chips. In table 8.1 the architecture characteristics are compared; series resistances have been added on

Helix 1.1 and Helix 1.2 as input protection enforced by break down phenomena (sparks) inside the microstrip gas chambers.

Due to the success of the project, the HELIX-chip which had been originally designed for the HERA-B experiment, has also been selected for the micro-vertex-detector upgrade of the ZEUS-experiment (DESY). Further DESY-experiments (H1,HERMES) currently consider the use of a modified version, so that in little time from now all major DESY-experiments could very well be equipped with the HELIX-chip in the one or the other version. Based on the HELIX-experience, the joint ASIC-laboratory of MPI für Kernphysik and Universität Heidelberg and the Dutch national institute for nuclear and high-energy physics NIKHEF (Amsterdam) have made a commitment to develop a new readout chip for the LHC-B experiment at CERN.

In this chapter we will restrict ourselves to HELIX128S-2; the modificated versions HELIX128S-2.1, HELIX128S-2.2, and HELIX128S-2.3 are described in appendix C.

	Helix 1	Helix 1.1	Helix 1.2	Helix 2	Helix2.1
W/L [μm/μm]	1517/1.2[1]	1517/1.2[1]	1517/1.2[1]	3026/1.2	3034/0.8
g_m	2.46 mA/V	3.5mA/V	3.5mA/V	4.86mA/V	6.28 mA/V
drain curr.	90 μA	180 μA	180 μA	180 μA	180 μA
feedback cap. (C_{fb})	1pF	1pF	740fF	360fF	342fF
peak time	95-130ns	55-80ns	45-75ns	60-100ns	50-90ns
series res.	0Ω	493Ω	320Ω	0Ω	0Ω
equiv. noise res.	271Ω	190Ω	190Ω	137Ω	106Ω

Table 8.1: Design features of the various frontends

[1]Extractor extracts waffle transistor of geometrical width=1.2μm with width=1.33μm

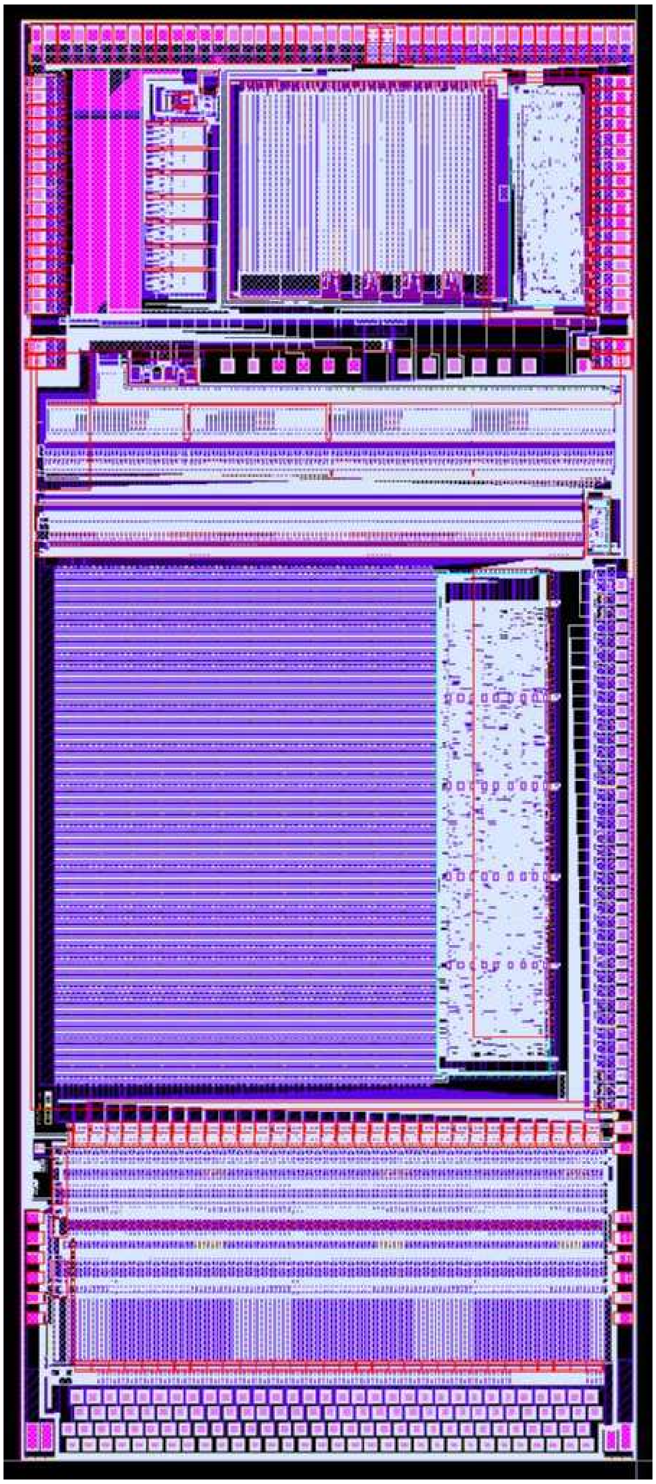


Figure 8.2: Layout of HELIX128S-2 (14.39 mm × 6.15 mm); from bottom to top: fourfold staggered rows of input pads, frontend with large input transistor, comparator with fanout to the chips's right side, pipeline array of 129 x 141 capacitor cells (beside the pipeline control logic), pipeline readout amplifier and analog multiplexer, column of "core pads" for testability, SUFIX-part with serial interface (right), voltage and current DACs to the left; all control pads (but not for the comparator) are located at the rear (i. e. top) side.

8.2 Frontend - Preamplifier

The task of the preamplifier can be summarized as follows: it integrates the current delivered by the source (silicon strip or microstrip gaseous detector), thereby minimizing the impact of the source capacitance, which is achieved by a low input impedance. The current signal, which can be approximated by a δ-like function (in case of the strip detector) gives rise to a voltage step Q_{in}/C_{fb} at the charge amplifier's output, where Q_{in} denotes the current integral and C_{fb} the feedback capacitance.

The design of the charge sensitive preamplifier plays a crucial role on the overall performance of the readout system. The noise performance of the chip is almost solely determined by the preamplifier (and the way of shaping). Furthermore, a good share of the overall chip power has to be dissipated in the preamplifier to achieve low noise and fast response times. Apart from the low noise requirement the charge amplifier must have a sufficiently fast output rise time. This is particularly important for the HERA-B reqirements with high counting rates requiring short peaking times (implying also sufficiently fast preamplifier operation).

The fast δ–like input currents imply a very broad frequency distribution which extends beyond the amplifier bandwidth. Therefore, the input node voltage will leave its quiescent voltage shortly for δ–like input currents due to the reduced open-loop gain at high frequencies (this corresponds to an increased input impedance - the low input impedance needs the reaction time of the feedback loop); it is important to notice that no "ballistic" deficit arises since the charge on the input node cannot disappear due to the source's high impedance characteristic, i. e. after the preamplifier's rise time the full voltage can be taken from the output.

The general noise issues applying to a charge sensitive amplifier can be dicussed without a precise knowledge of the used architecture assuming all of the noise being produced by the input transistor (either MOS or bipolar). This calculation including the comparison of MOS vs. bipolar has been done in chapt. 7.2.

8.2.1 Small Signal Model

To study the behaviour of the preamplifier a small signal model of the preamplifier (fig. 8.7) is plotted in fig. 8.3. The cascode configuration of the schematic has been dropped in the small signal model for simplicity; g_m denotes the input transistor's transconductance and C_{tr} its gate-source plus gate-drain capacitance; C_l is given by the sum of the C_{dg}'s and the C_{db}'s of M3 and M4, respectively. R_l is the drain-source resistance r_{ds} of M4 (the resistance looking into M3 is much higher due to the cascode circuit). The feedback capacitor C_{fb} equals C1 and R_{fb} equals the on-resistance of M7 which operates in the triode (linear) region.

The straight forward calculation of the current-to-voltage transfer function is easily carried out (see also [CS91]) assuming $g_m R_{out} \gg 1$ with $R_{out} = R_{fb} \| R_l$ and is given by

$$v_{out}(s) = -\frac{g_m}{\frac{g_m}{R_{fb}} + s g_m C_{fb} + s^2 C_{in} C_{out}} i_{in}(s) \tag{8.1}$$

with $C_{out} = C_{fb} + C_l$, $C_{in} = C_{det} + C_{tr} + C_{fb}$. Equation 8.1 is a second order (in s) transfer function (notation as in fig. 8.3). The values for the preamplifier described can be found in table 8.2.

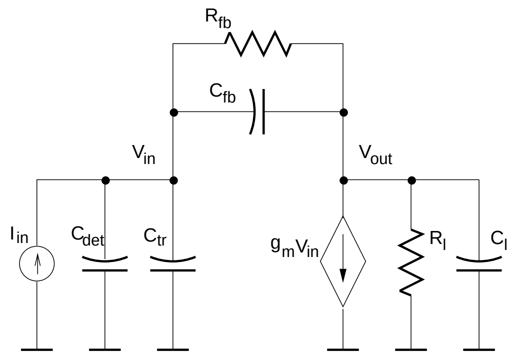


Figure 8.3: Small signal model of preamplifier; the values to be inserted are given in table 8.2.

By replacing s=$2\pi j\nu$ in eq. (8.1) and taking the absolute value we obtain the frequency transfer function $v_{out}/i_{in}(\nu)$ in fig. 8.4; in the range between ν_{p1} and ν_{p2} the preamplifier integrates current according to $v_{out} = i_{in}/(sC_{fb}) = q_{in}/C_{fb}$. At the dominant pole's ω_{p1} origin the feedback resistor breaks with the feedback capacitance hence denoting the point of proper integration operation (at very low frequencies the amplifier looks like a transresistance amplifier).

Under the assumption that the poles are widely spread, the pole positions are given by

$$\begin{aligned}
\omega_{p1} &= -\frac{1}{\tau_1} = -\frac{1}{R_{fb}C_{fb}} \\
\omega_{p2} &= -\frac{1}{\tau_2} = -\frac{g_m C_{fb}}{C_{in}C_{out}} = -\mathrm{GBW}\frac{C_{fb}}{C_{in}}
\end{aligned} \tag{8.2}$$

The first pole is given by the time constant $R_{fb}C_{fb}$ of the feedback components determining the continous reset time; the second pole is the result of the capacitive feedback (chapt. 7.1.3).

The achieved GBW (2.84 rad/ns or 453 MHz) is quite remarkable for CMOS; the fastest video opamp of AMS features a 50 MHz GBW product. However, the preamplifier open-loop cell is not unity-gain stable since the nondominant cascode pole at approx. 40 MHz lies (considerably) below 1.22·GBW. However, with a preamplifier "voltage gain" (given by C_{in}/C_{fb}, see chapt. 7.1) of 10...50, the phase margin amounts to a minimum of 89° and hence is more than sufficient.

By inverse Laplace transformation the time domain response can be obtained. The input current is approximated by a Dirac δ-pulse $I(t) = Q\delta(t)$ with an integrated area of Q. Thus, the output signal in the time domain becomes

$$v_{out}(t) \approx \frac{Q\tau_1}{C_{fb}(\tau_1 - \tau_2)}(e^{-\frac{t}{\tau_1}} - e^{-\frac{t}{\tau_2}}) \quad . \tag{8.3}$$

Since in all practical cases $\tau_2 \ll \tau_1$, this expression represents an exponential rising step with a slowly decaying tail as introduced by the DC feedback path. The output voltage

g_m	6.28 mV/A	ν_{p1}	15.5 kHz
C_{det}	20 pF	ν_{p2}	6.6 MHz
C_{tr}	2.92 pF	ν_{z1}	200 kHz
C_{fb}	342 fF	τ_1	10.2μs
R_{fb}	30 MΩ	τ_2	23.9ns
R_l	2.06 MΩ	t_r	52.6ns
C_l	1.86 pF	$v_0 = R_l g_m$	12940
C_{in}	23.26 pF	GBW	453 MHz
C_{out}	2.20 pF		

Table 8.2: Small signal values of preamplifier; the values in the table are taken from SPECTRE model 2 equations.

in response to a charge of 1 fF is shown in fig. 8.5 with $\tau_1 = 10.2\mu$s, $\tau_2 = 23.9$ ns as found in the preamplifier. It should be noticed here, that C_l includes the couple capacitance to the subsequent shaper stage; so no further loading takes place.

The rise time (10% to 90%) is determined by time constant τ_2 and can be calculated from eq. (8.2) by

$$t_r = 2.2 \cdot \tau_2 = 2.2 \cdot \frac{C_{in}}{\mathrm{GBW} C_{fb}} \tag{8.4}$$

i. e. the rise time can be minimized by a small total input capacitances, a large feedback capacitance and a large gain-bandwidth amplifier.

The input impedance of the charge amplifier can be calculated to be (assuming $s \gg 1/(R_{fb}C_{out})$ and $g_m \gg 1/R_{out}, sC_{fb}$)

$$Z_{in}(s) = \frac{v_{in}}{i_{in}}(s) = \frac{1}{R_{out}} \frac{1 + sR_{out}C_{out}}{\frac{g_m}{R_{fb}} + sg_mC_{fb} + s^2C_{in}C_{out}} \quad . \tag{8.5}$$

We observe a zero at

$$\omega_z = -\frac{1}{R_{out}C_{out}} \quad . \tag{8.6}$$

The pole positions are identical to those obtained for the transfer functions and are given by

$$\begin{aligned} \omega_{p1} &= -\frac{1}{C_{fb}R_{fb}} \\ \omega_{p2} &= -\frac{g_mC_{fb}}{C_{in}C_{out}} = -\frac{\mathrm{GBW}C_{fb}}{C_{in}} \quad . \end{aligned} \tag{8.7}$$

The input impedance for frequencies below ν_{p1} is purely ohmic and equals

$$Z_{in}^{ohm1} = \frac{R_{fb}}{g_mR_l} = \frac{R_{fb}}{v_0} \approx 13.2k\Omega \tag{8.8}$$

i. e. as in the case of a current amplifier the input impedance is given by feedback resistance divided by the open loop gain.

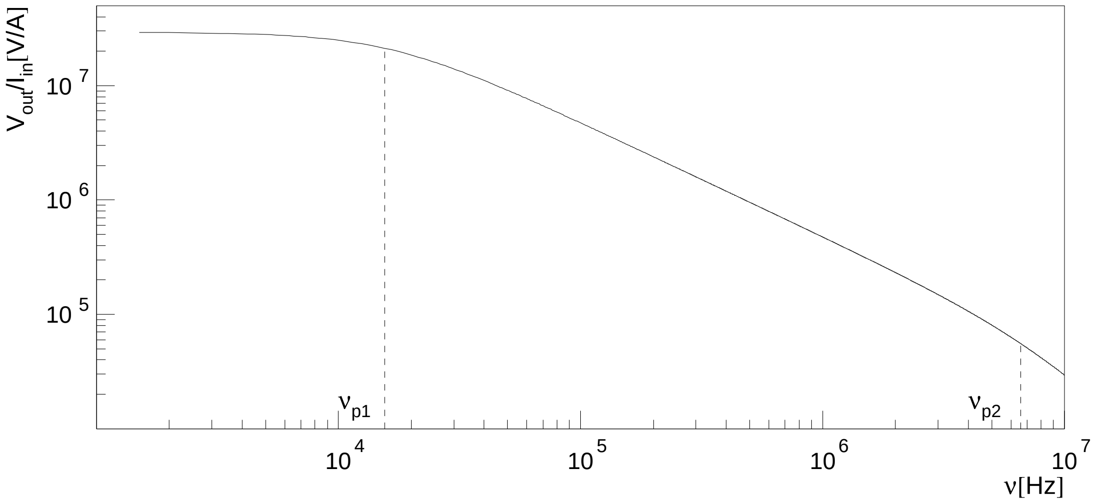


Figure 8.4: Bode-plot of transfer function $v_{out}/i_{in}(\nu)$; in the range between ν_{p1} and ν_{p2} the preamp integrates current. The gain is given by $v_{out} = i_{in}/(sC_{fb}) = q_{in}/C_{fb}$.

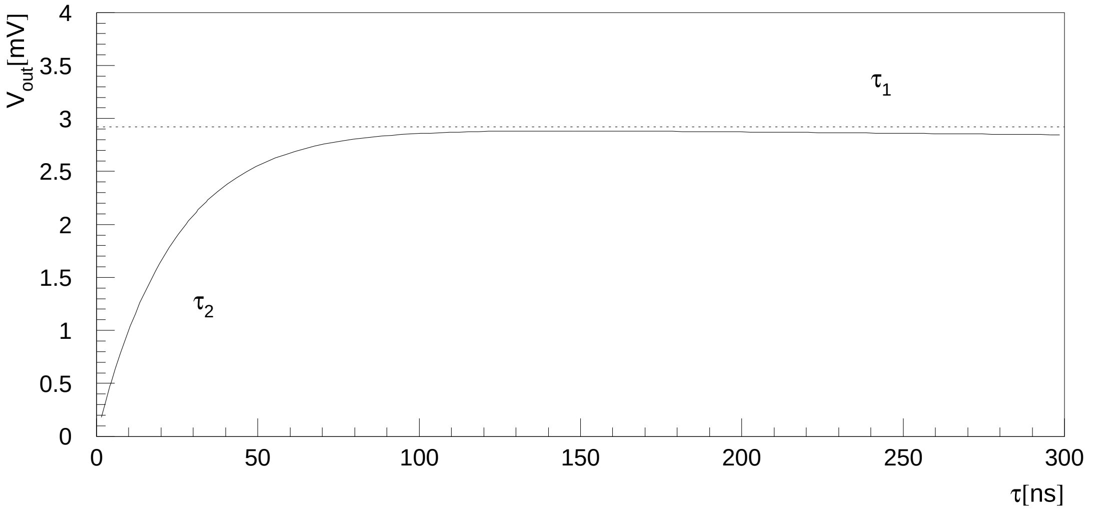


Figure 8.5: Preamplifier response to a δ-like current pulse of 1fF charge; the rise is determined by τ_2. τ_1 is the time constant of the exponential discharge of the feedback resistor C_{fb} via R_{fb}.

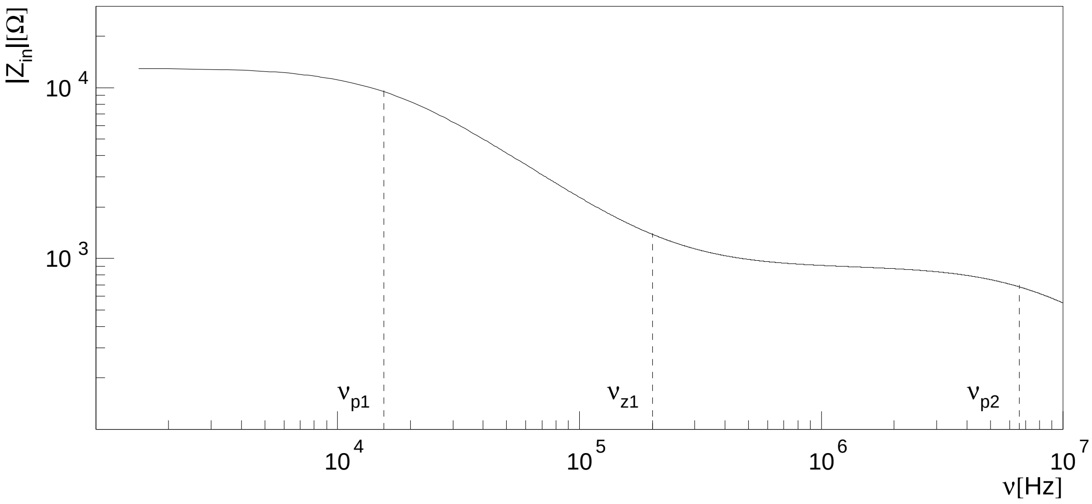


Figure 8.6: Bode-plot of input impedance; in the range between ν_{p1} and ν_{z1} the input impedance is capacitive with $C_{in} = v_0 C_{fb}$. For signal frequencies between ν_{z1} and ν_{p2} the input impedance is ohmic: $R_{in} = \tau_2/C_{in}$.

The input impedance in the range between ν_{p1} (15.5kHz) and ν_{z1} (200 kHz) can be appoximated by

$$Z_{in}^{int}(s) = \frac{1}{s g_m R_l C_{fb}} = \frac{1}{s v_0 C_{fb}} \quad . \tag{8.9}$$

Hence, the input impedance equals the feedback capacitance multiplied with the open loop gain. This feature is a very desired one since due to $v_0 C_{fb} \gg C_{det}$ nearly no charge division takes place in this frequency range - all charge generated in the detector is "drawn" to the amplifier feedback capacitance.

At $\omega_z = -1/(R_{out} C_{out})$ the input impedance becomes again ohmic with

$$Z_{in}^{ohm2} = \frac{C_{out}}{g_m C_{fb}} = \frac{\tau_2}{C_{in}} \quad \approx 1020\Omega \tag{8.10}$$

wich is due to the fact that the load impedance becomes capacitive and the voltage division between C_{fb} and C_{out} becomes frequency independent. Z_{in}^{ohm2} is directly linked to the preamplifier risetime (=2.2 τ_2) via eq. (8.10). Hence input resistance and amplifier risetime are equivalent manifestations of the gain cell's-GBW. As is know from the transfer function, the amplifier is in integrating mode in the second ohmic region.

8.2.2 Schematic

Fig. 8.7 shows the preamplifier schematic (cf. also [HN95]). For the open loop gain cell the well-known folded cascode configuration has been chosen [Beu90, Nyg92]. If a common source amplifier was used as gain cell, the gate-drain capacitance of the (usually large) input transistor would lie in parallel to the feedback capacitance and hence would would limit the realizability (and the predictability) of the otherwise well adjustable

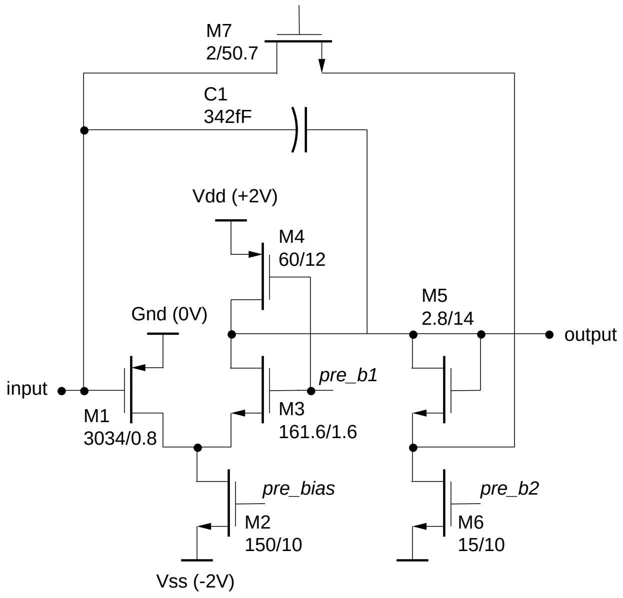


Figure 8.7: Preamplifier; width W and length L (in μm) are given for each transistor in the schematic.

gain (fig. 8.8). Therefore, the gate-drain capacitance of the input transistor has to be eliminated by using a cascode circuit.

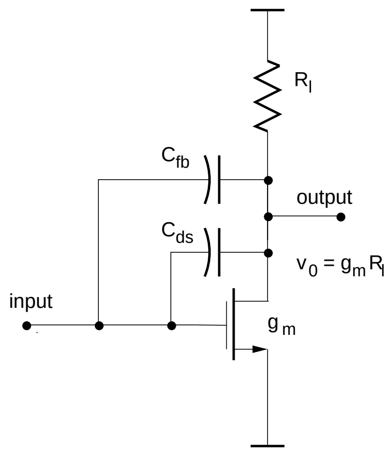


Figure 8.8: Integrator with a simple common-source amplifier as gain cell; the gain depends on the gate-drain capacitance of the input transistor.

Note that bandwidth is *not* the reason for using the cascode circuit in a charge amplifier as it is often found in literature - quite on the contrary a large feedback capacitance speeds up the amplifier's response (eq. (8.4)). The folded cascode has been selected in favour of the straight cascode due to a larger load impedance having less current in the load branch ($r_{ds} \propto 1/I_d$) causing a higher open-loop gain, and due to its reduced power consumption, since the large input transistor current is shunted to ground (and not to Vdd).

In the introduction of this section it has been stated that the noise performance is given

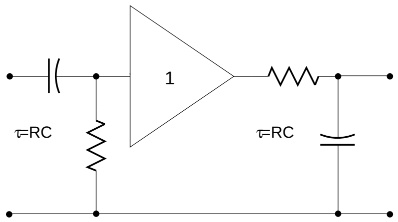


Figure 8.9: Idealized CR-RC-shaper which forms ("shapes") the signals behind the charge amplifier

by the input transistor only. In fact, the noise contributions of all other transistors in the architecture (besides the feedback transistor contributing to the parallel noise) are all negligible w. r. t. the huge input transistor. We can motivate this shortly by recalling the drain noise current density (disregarding the 1/f-noise)

$$i_{d,n}^2 = \frac{8kTg_m(1+\eta)}{3} \qquad [\text{in A}^2/\text{Hz}] \tag{8.11}$$

which is proportional to a transistor's g_m. At the output node the noise currents of all transistors add up in quadrature (besides M3 and M5 whose sources are "degenerated" and contribute even less). Hence, the overall noise current which is converted to an output noise voltage at the load impedance, is determined only by the input transistor's noise current with its large g_m-value.

The *input referred* noise is given by dividing the total drain noise current by g_m^2 of the input transistor. The noise voltage v_s^2 obtained is proportional to $1/g_m$ since the total noise current is dominated by the input transistor - thus a large input transistor g_m is favorable to achieve low noise.

The slope of the serial thermal ENC$_{th}$ vs. C_{in} can be calculated according to eq. (7.44) to be 35.9 e$^-$/pF (shaper peaktime 48 ns); the result from simulation is 287e$^-$+33.2e$^-$/pF (47 ns) with all bias lines filtered. The discrepancy is due to an increase in shaper time with capacitance in the simulation (fig. 9.3).

8.3 Frontend - Pulse Shaper

Pulse shaping filters are employed (other methods are discussed in chapt. 6) to transform the voltage step delivered by the integrating preamplifier into a well defined and time limited pulse w. r. t. to the expected rate. Limitation of the output pulses in time and the noise spectrum ($1/f^2$ behaviour of the parallel noise) require a low frequency suppression, general bandwidth limitation leads to a low pass filter. Both requirements together imply the use of a band pass.

Another requirement for the pulse shaping filter is a linear phase-frequency relationship to avoid ringing (this is equivalent to a frequency constant group velocity) which is a peculiar property of Bessel-filters. Ringing or undershoot should be avoided since it increases the settling time and the serial noise contribution (cf. chapter 6).

As a very simple filter, which satifies the Bessel filter condition, the CR-RC filter has become widely spread [Beu90, CS91, Com96, Nyg92, Hal53, Hu95, HN95, Kno97, Ort95].

A semi-passive implementation consists of a CR-high pass, followed by a buffer and a RC-low pass of the same time constant (see fig. 8.9). The high pass "detects" only the voltage steps, the background caused by earlier signals is suppressed. The "easiest" implementation is unfortunately not very practical in CMOS technology due to the (relatively) large capacitor or resistor values needed (τ=50ns=1pF$\cdot$50kΩ); however, it comes into reach for the very fast time constants discussed here. Also, the pulse peak time which equals the common time constant τ of high- and lowpass, should often be made adjustable to react to radiation induced changes in the preamplifier and the detector. Therefore, usually an active g_m-C filter circuit is used to generate the required poles.

In building the shaper different design tasks have to be dealt with: the pulse peak time has to lie in a window around 50ns to comply with the 100ns bunch crossing rate of HERA-B; the pulse shape should be free from undershoot to minimize the noise and the time consumption. Furthermore, from the noise point of view, a small shaper gain is desirable because then the preamp gain can be maximized - and the shaper noise contribution becomes negligible. However, the preamplifier gain must not be increased too much since then it would become too slow according to eq. (8.2). Also from the noise point of view, the value of the total feedback resistance R'_{fb} (parallel noise) and the input transistor g_m (serial noise) should be large. Linearity is a much bigger issue for the shaper than for the preamplifier due to its much bigger output swing. To achieve maximum linearity the design of the feedback transistors M5 and M7 in fig. 8.10 is crucial because these "resistors" change their value for large swings. Of course, the core cell transistors should stay in saturation for the whole dynamic range.

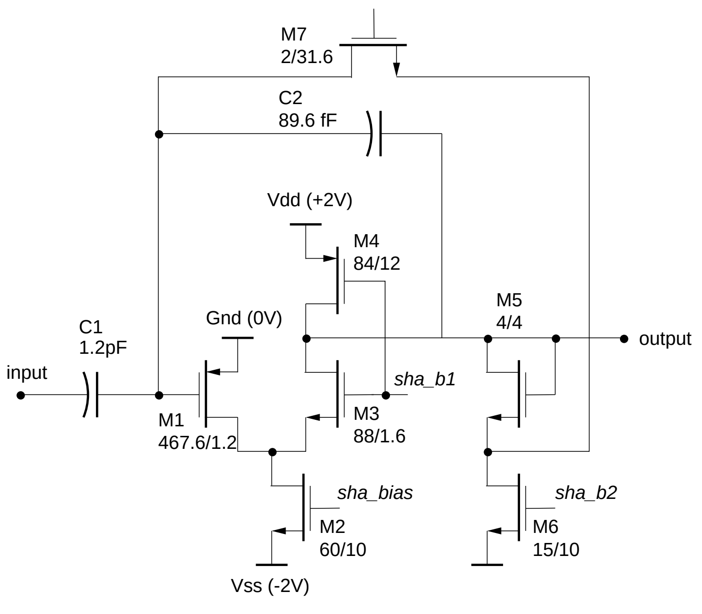


Figure 8.10: Shaper

The required shaper transfer function has been realized by the circuit depicted in fig. 8.10.

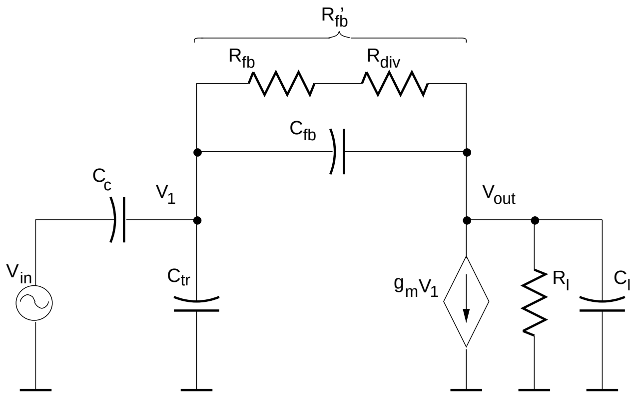


Figure 8.11: Small signal model of shaper; the actual values taken from the SPICE model 2 are given in table 8.3.

8.3.1 Small Signal Model

The small signal model can be inferred from the schematic in fig. 8.10 similarly to the preamplifier case and is plotted in fig. 8.11. Differing from the preamplifier case, we explicitely take M5 into account ($R_{div} = 1/g_m$ of transistor M5), since R_{fb} is now considerably smaller than in the preamplifier. Calculating the gain from the small signal model with the approximation $g_m \gg (1/R_{fb} + sC_{fb})$ yields

$$\begin{aligned} v_{out}(s) &= -\frac{s g_m C_c}{s^2(C_{fb}^2 - C_{in}C_{out}) + s(\frac{2C_{fb}-C_{in}-C_{out}}{R'_{fb}} - g_m C_{fb} - \frac{C_{in}}{R_l}) + \frac{1}{R'_{fb}}(\frac{1}{R_{out}} - g_m)} v_{in}(s) \\ &= A(s) v_{in}(s) \end{aligned} \tag{8.12}$$

with

g_m transconductance of input transistor M1

$C_{in} = C_c + C_{tr} + C_{fb}$ total input capacitance

$C_{tr} = C_{gs} + C_{gd}$ of input transistor M1 (no Miller effect assumed)

$C_{out} = C_l + C_{fb}$ total output capacitance

$R'_{fb} = R_{fb} + R_{div}$ total feedback resistance

$R_{div} = 1/g_m$ of transistor M5

$R_{out} = R'_{fb}||R_l$ total resistance at output node

$R_l = r_{ds}$ of transistor M4

The numerical of the shaper are given in table 8.3. The small peak time given in table is due to the absence of all parasitic effects and due to the assumption of an infinite bandwidth preamplifier. The (open loop) dominant pole of the shaper is associated with node V_1 (fig. 8.11) so that the gain-bandwidth product GBW is given by

$$\mathrm{GBW} = \frac{v_0}{R'_{fb} C_{in}} = \frac{g_m}{C_{in}} \quad . \tag{8.13}$$

g_m	1.33mA/V	$s_z/(2\pi)$	0
C_c	1.20pF	$s_{p1}/(2\pi)$	(-7.87 +j 5.20) MHz
C_{tr}	1.61pF	$s_{p1}/(2\pi)$	(-7.87 -j 5.20) MHz
C_{fb}	90f	t_{peak}	17.9 ns
C_l	177f	ν_{max}	8.89 MHz
R'_{fb}	292kΩ	$v_0 = g_m R'_{fb}$	390
R_l	6.57MΩ	GBW	75 MHz

Table 8.3: Shaper small signal parameters

Eq. (8.12) can be expressed as

$$v_{out} = -\frac{s}{(s+\beta)^2 + \alpha^2} v_{in} \tag{8.14}$$

which denotes a one-zero two-pole transfer function plotted in fig. 8.12.

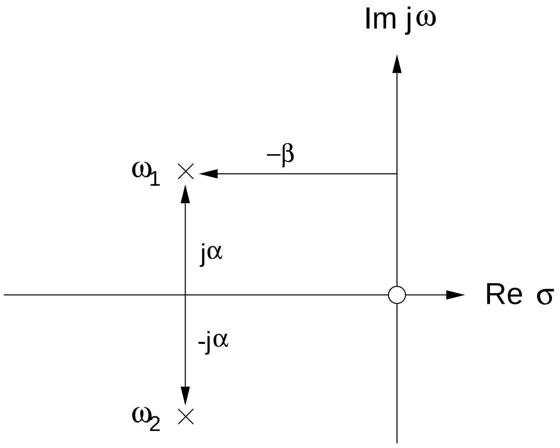


Figure 8.12: Pole-zero diagram of the shaper

The inverse Laplace transformation for a function of the type

$$v_{out} = \frac{s}{(s+\beta)^2 + \alpha^2} \cdot \frac{1}{s} \tag{8.15}$$

– $v_{in}(s) = -1/s$ is the Laplace transformation of a step function and hence a first-order approximation of the preamplifier output voltage – equals

$$v_{out}(t) = \frac{1}{\alpha} \sin(\alpha t) e^{-\beta t} \tag{8.16}$$

which indicates an undershoot (see fig. 8.13) due to the negative sine half-wave. A transfer function of the type

$$v_{out} = \frac{s}{(s+\beta)^2} \cdot \frac{1}{s} \tag{8.17}$$

gives an ideal pulse response in the time domain of

$$v_{out}(t) = te^{-\beta t} \tag{8.18}$$

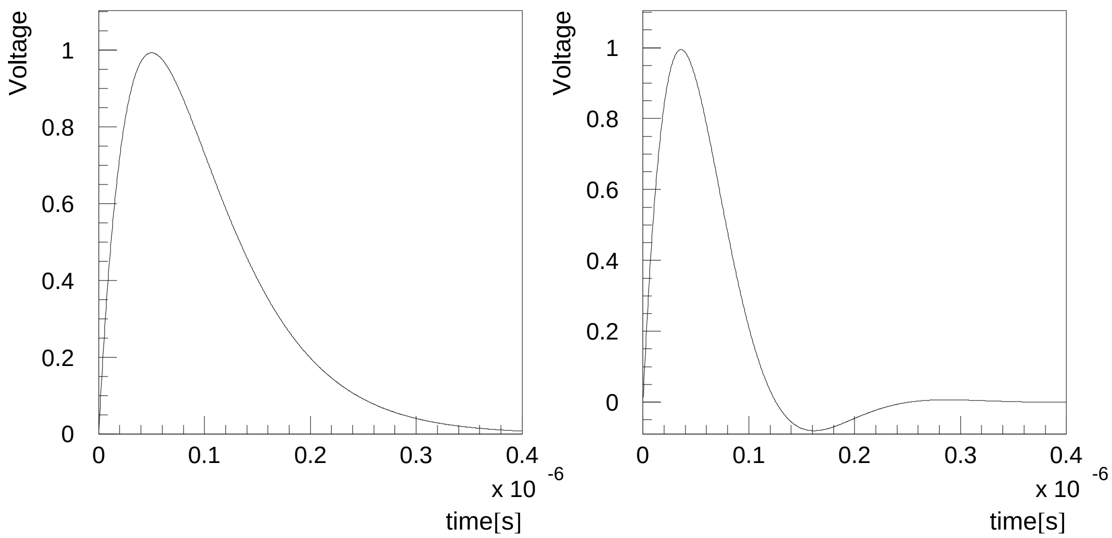


Figure 8.13: Left: ideal semi-gaussian pulse $v_{out}(t) = te^{-\beta t}$; right: pulse shape with undershoot $v_{out}(t) = \frac{1}{\alpha}\sin(\alpha t)e^{-\beta t}$ (α=1/50ns, β=1/40ns)

which is called to be a semi-gaussian pulse (fig. 8.13). The pulse peak occurs at time τ=1/β, which equals the common time constant τ of high- and lowpass.

By comparing eq. (8.17) with eq. (8.12) it can be deduced that in the ideal case the denominator polynome in equation (8.12) has a double real pole; this holds true for

$$R_l = \frac{C_{in}R'_{fb}}{(2C_{fb} - C_{in} - C_{out}) - g_m R'_{fb} C_{fb} + 2\sqrt{(C_{fb}^2 - C_{in}C_{out})g_m R'_{fb}}} \quad . \tag{8.19}$$

Eq. (8.19) gives an analytical expression for the R_l value to be chosen for an ideal semi-gaussian pulse shape.

After having chosen a circuit configuration (and the corresponding small signal model) the transistor geometries have to be selected in consideration of the design goals mentioned at the beginning of the section. A full analytical solution to the problem is not particularly attractive, so a graphical method has been developed to find a good set of parameters. Beginning with a start parameter set gain, peak time, and the ideal R_l are plotted against each of the parameters C_c, g_m, R'_{fb}, and C_{fb}. Gain (at the pulse peak) and peak time can in principle be determined by equating the time derivative of the inverse Laplace transformed eq. (8.12) to zero

$$\frac{d}{dt}\left[\mathcal{L}^{-1}A(s)\frac{1}{s}\right] = 0 \quad . \tag{8.20}$$

Unfortunately this task fails even with the help of a symbolic mathematics program [Mapl96]. Therefore assuming that the final shaper is designed to run near the ideal case of a double pole the "ideal" gain (eq. (8.21), i. e. when the "ideal" load resistance as given in eq. (8.19) was inserted, and the corresponding peak time (eq. (8.22)) were plotted in fig. 8.14:

$$\text{gain} = \frac{2/e \cdot g_m C_c}{2\frac{C_{fb}}{R_{fb}} - g_m C_{fb} + \frac{C_{in}}{R_{out}} - \frac{C_{out}}{R_{fb}}} \tag{8.21}$$

$$\text{peak time} = 2\frac{C_{fb}^2 - C_{in}C_{out}}{\frac{C_{fb}}{R_{fb}} - g_m C_{fb} + \frac{C_{in}}{R_{out}} - \frac{C_{out}}{R_{fb}}} \tag{8.22}$$

Fig. 8.14 shows the flow of gain, peak time and ideal load resistance around the design point (i. e. the finally chosen parameters) indicated by the vertical line. Since the actual load resistance R_l is in the MΩ regime (not largely variable for the chosen circuit configuration) being always larger than the ideal resistance the design goal of an undershoot-free shaper translates to maximizing the ideal load resistance. Therefore, the right column in fig. 8.14 gives the relevance of each parameter to the pulse undershoot. In an iterative approach it has been attempted to bring the gain to a (not too) low level, maximize R'_{fb} and g_m while keeping the peak time to $\approx$ 50 ns.

Some plots in fig. 8.14 can be motivated by simple considerations: the gain drops with increasing feedback capacitance as for an ideal charge amplifier; the peak time then increases due to the large time constant $R'_{fb}C_{fb}$; however, the peak time changes not as much as would naively be expected. In contrary, the feedback resistance R'_{fb} changes the peak time highly and leaves the shaper gain almost unaffected. Increasing g_m does not increase the gain very much (since it is mainly determined by the feedback) and decreases the peak time (by analogy to the rise time of a charge amplifier).

The shaper transfer function in the frequency domain is plotted in fig. 8.15 with the parameters as given in table 8.3. For low frequencies the transfer function rises proportionally to frequency ν due to the shaper zero; for high frequencies the transfer function approaches asymptotically a $1/\nu$ flow. For an ideal semi-gaussian pulse the maximum is reached at the inverse of the peak time according to

$$t_{peak} = \frac{1}{\omega_{max}} \quad . \tag{8.23}$$

Fig. 8.16 shows the calculated results (eq. (8.12)) of the small signal model in the time domain in comparison to the simulated results. We introduced two physically motivated additional "parameters" to make the calculated pulse better approximate the simulated one. This is a legal approach since the small signal model is a first-order approximation; its major task is to prove insight into the circuit.

First, since the cascode node has to charge up (a minor effect not included in the small signal model), an effective input transistor g_m(eff.)=0.86 $\cdot$ g_m has been used (only this portion of input current variation is dynamically mirrored to the load branch). Secondly, an additional output capacitance of 500fF accounts for all capacitances at nodes not covered by the small signal model (which assigns capacitances only to the folded cascode's input and output node).

On the left-hand side of fig. 8.16 the calculated shaper response

$$v_{out} = 37.7[\text{mV}] \exp(-t/202.3[\text{ns}]) \sin(t/30.6[\text{ns}]) \tag{8.24}$$

to a voltage step of 1mV is plotted (solid line); a small undershoot indicates that condition eq. (8.19) could not be exactly fulfilled (in fact the "ideal" R_l for the shaper parameters (table 8.3) equals app. 58 kΩ). The dashed line shows the simulated shaper response without parasitic capacitances and with the amplifier offset subtracted. The gain and the peak time of the simulated pulse are very well described by the small signal model with the simulated tail exceeding the calulated one.

On the right hand side the overall response of preamplifer *and* shaper is plotted (note: without output buffer) against the time. The solid line gives the calculated pulse response to 1 MIP again; the preamplifier was modelled according to eq. (8.1) with the pole ω_{p1} omitted, i. e. with a one-pole rise behaviour (t_{rise}=30.4 ns at $C_{det} = 0$). By inverse Laplace transformation of the resulting 3-pole 1-zero transfer function one receives for a 1 MIP stimulation (24000 electrons)

$$\begin{aligned} v_{out} &= 627.2[\mathrm{mV}]\exp(-t/13.8[\mathrm{ns}]) \\ &\quad +442.1[\mathrm{mV}]\exp(-t/20.2[\mathrm{ns}])\sin(t/30.6[\mathrm{ns}]) \\ &\quad -627.9[\mathrm{mV}]\exp(-t/20.2[\mathrm{ns}])\cos(t/30.6[\mathrm{ns}]) \qquad (8.25) \end{aligned}$$

The dashed line shows the simulated response again; the dotted line gives the simulated response with all parasitic capacitances included. Due to the preamplifier pole the overall pulse shape deviates from the ideal semi-gaussian shape as plotted in fig. 8.13; the pulse shape becomes more symmetric which is a very desired feature from the noise point of view (see section 6). Hence it clearly can be seen that the target shaper time (in the small signal consideration) must be in the 20ns regime to come to a final value of appr. 50ns.

Another focus of the shaper design was linearity. A $\pm$10 MIP range corresponds to $\pm$ 650mV or a total of 1.3V at the shaper output. This range has to be accomplished using nonlinear resistors in the feedback ! In principle the feedback network's DC-behaviour can be modelled by the circuit plotted in fig. 8.17. For convenience conductances have been plotted rather than the corresponding resistances. G_1 corresponds to the drain-source resistance of feedback transistor M7, G_2 to $1/g_m$ of M5.

When setting $V_{in} \equiv 0$ the following large signal equation system can be set up:

$$\begin{aligned} G_1 &= 2\beta_1(V_g - V_1 - V_{th}) && \text{for neg. pulses} \\ G_1 &= 2\beta_1(V_g - V_{th}) && \text{for pos. pulses} \\ G_2 &= \frac{\beta_2(V_{out} - V_1 - V_{th})^2}{V_{out} - V_1} \\ V_{out} &= \frac{I_0}{G_2} + V_1 && (8.26) \end{aligned}$$

I_0 is the current drawn by M6 from the output; since the input node is high ohmic no current flows through G_1 in the static case. For a constant pulse shape the combined feedback conductance $G_1 + G_2$ should be constant for all values of V_{out}; in the static model this condition is identically fulfilled for *positive* pulses, since then either of the conductances remains unchanged; for negative pulses G_2 remains constant (drain current always equals I_0), but since $V_1 < V_{in}$ the node V_1 becomes the source of M7 and thus G_1 depends on V_{out}.

Unfortunately the dynamic case is more complicated, since current has to flow through G_1 to charge the feedback capacitance and the input capacitance. This current is supplied by V_{out} so that M5's (=G_2) drain current changes; by iterative simulations the W/L value of G_2 has been selected such that for negative pulses the relative changes of G_1 and G_2 cancel, so that $G_1 + G_2$ remains approximately constant. For positive pulses the relative G_2 change is smaller; since $G_1 > G_2$ the sum $G_1 + G_2$ remains almost constant. Fig. 8.18 shows the simulated dynamic range of preamplifier and shaper demonstrating the excellent linearity of the feedback network.

The shaped signal is supposed to be written onto the pipeline capacitor; unfortunately the shaper output impedance does not allow to drive the pipeline capacitances directly. Likewise, changes of the pipeline capacitances (either the hold capacitor or the parasitic capacitance of the write-line) would directly influence the pulse shape - which is not a wanted feature concerning design modularity. Furthermore constant current slewing can become an issue; increasing the shaper bias current would also lead to an unwanted change in pulse shape.

The output impedance derived from the small signal model (fig. 8.11) with the same assumptions made for eq. (8.12) is given by eq. (8.27)

$$v_{out} = \frac{1/R'_{fb} + sC_{in}}{s^2(C_{fb}^2 - C_{in}C_{out}) + s(\frac{2C_{fb} - C_{in} - C_{out}}{R'_{fb}} - g_m C_{fb} - \frac{C_{in}}{R_l}) + \frac{1}{R'_{fb}}(\frac{1}{R_{out}} - g_m)} i_{out} \tag{8.27}$$

and is plotted in fig. 8.19. For low frequencies the shaper output impedance remains well under 1 kΩ and is uncritical; it rises at the zero's break frequency $1/(R'_{fb}C_{in})$ proportionally to frequency (thus exhibits an inductive behaviour); this inductance together with (a large) load capacitance can create an oscillatory behaviour of the shaper (this behaviour can also be deduced directly by setting up the small signal transfer function with a large load capacitance); in other words the ideal R_l drops with increasing C_l (*not* plotted in fig. 8.14). Thus, from the output impedance it can be deduced another time that the shaper circuit is prone to instability and has to be carefully designed to minimize under/overshoot.

For the interesting signal band around the peak (≈ 10 MHz) the output impedance rises up to a peak value of 23kΩ which is untolerable given a total capacitance of 3 pF to drive. The reason for the similiar behaviour of closed loop gain and output impedance is that both are linked together very closely for the series-shunt feedback employed within the shaper by the factor open loop gain/load impedance ([San94, p. 190]).

For the reasons mentioned a separate buffer has to be designed to drive the pipeline capacitance.

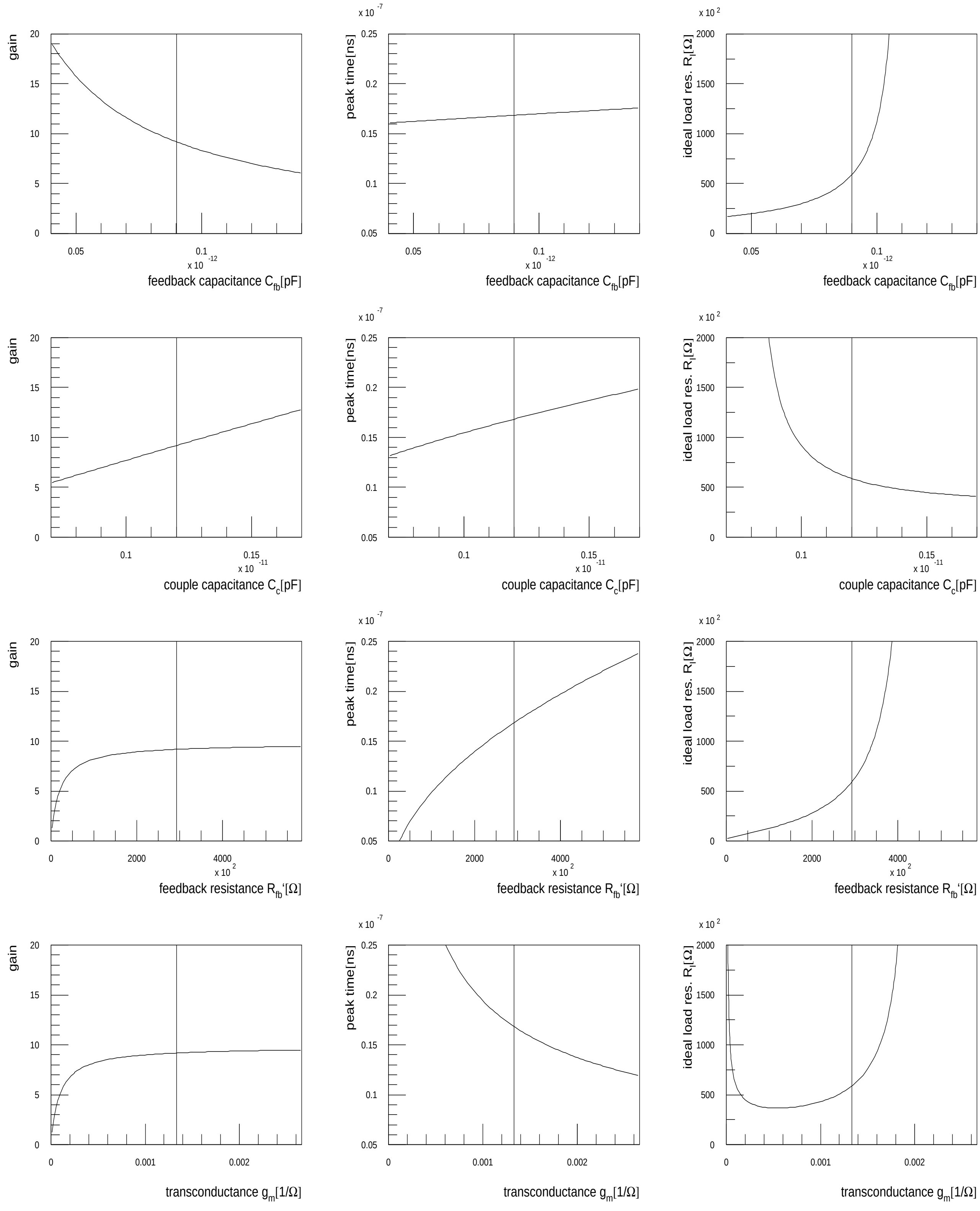


Figure 8.14: Dependency of shaper gain, peak time, and ideal load resistance on feedback capacitance C_{fb}, couple capacitance C_c, feedback resistance R_{fb} and input transistor transconductance g_m; vertical lines indicate the chosen design value.

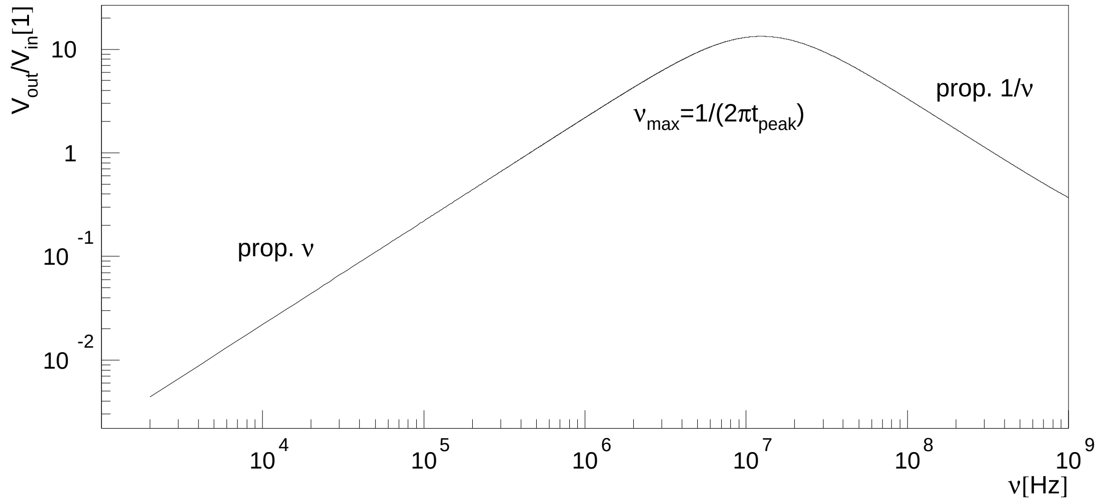


Figure 8.15: Bode-plot of the shaper transfer function $v_{out}/v_{in}(\nu)$; for an ideal semi-gaussian shaper the maximum occurs at $(2\pi t_{peak})^{-1}$.

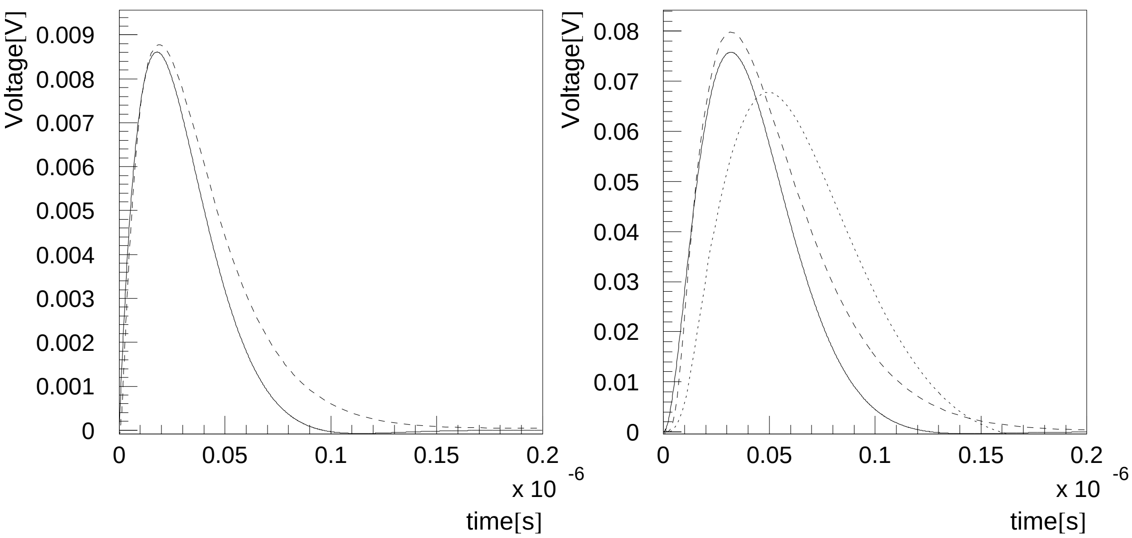


Figure 8.16: Left: solid line: calculated shaper response from the small signal model to a 1mV step function; dashed line: simulated shaper response (without parasitic capacitances); right: solid line: calculated pulse response of the combined preamplifier *and* shaper to 1 MIP; preamplifier rise time 30.4 ns ($C_{det} = 0$), dashed line: simulated response, dotted line: simulated response with all parasitic capacitances included

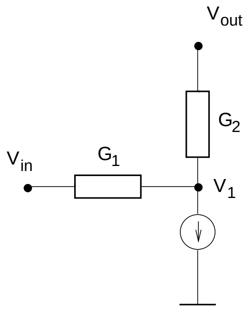


Figure 8.17: Large signal model of the shaper feedback network

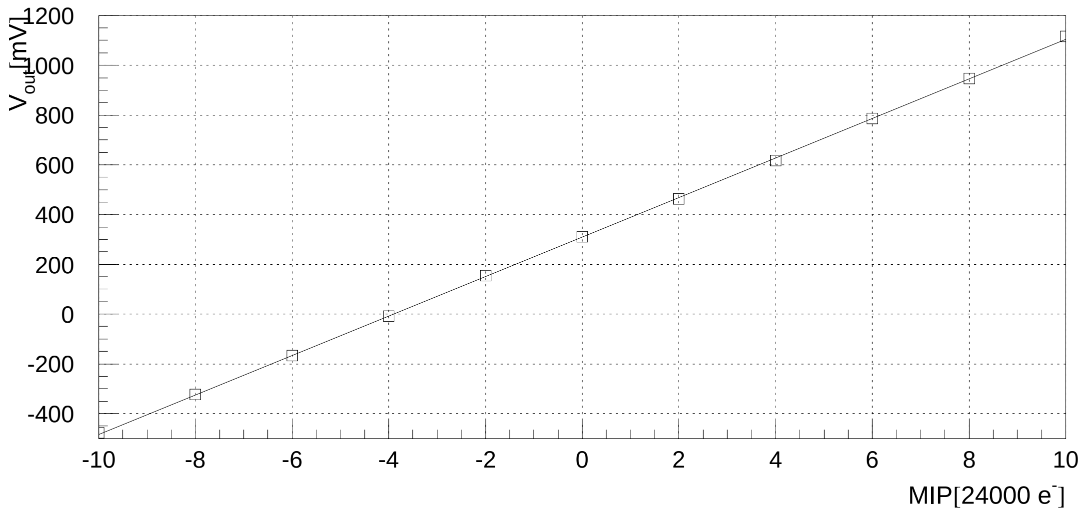


Figure 8.18: Simulated (without parasitics) linearity of combined preamplifier and shaper

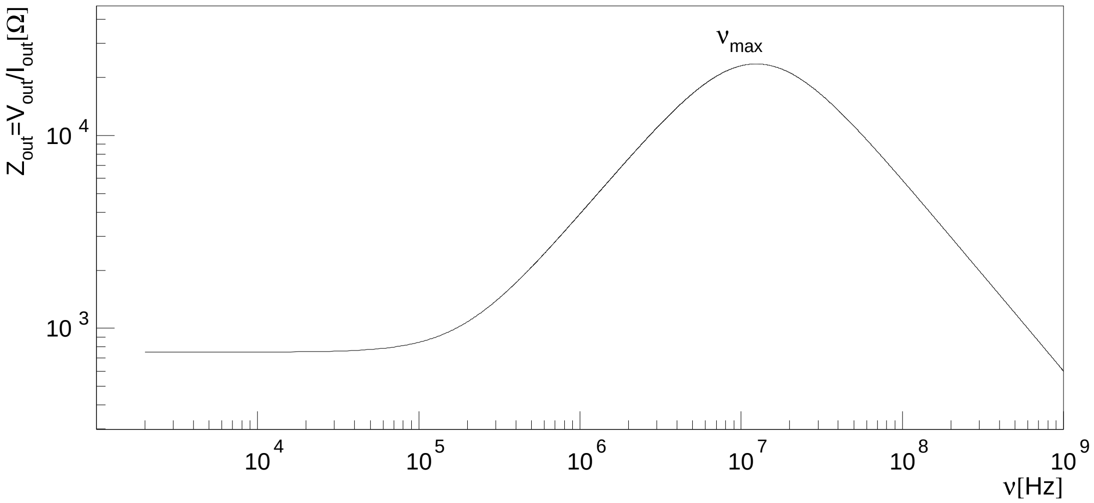


Figure 8.19: Bode-plot of the shaper output impedance $v_{out}/i_{out}(\nu)$

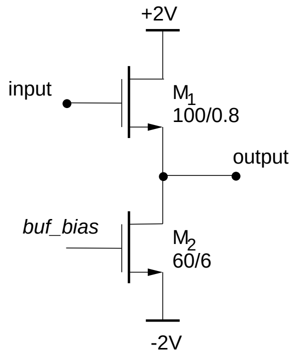


Figure 8.20: Frontend buffer schematic

8.4 Frontend - Buffer

The frontend buffer must drive the pipeline capacitance C_h=850fF, the parasitic capacitance of the *write*-line C_{para}=2.05 pF, and the discriminator input capacitance C_{discr}=59 fF [Gla97]. It has been realized as a simple source follower. A schematic is plotted in fig. 8.20; the corresponding small signal model is a typical text-book problem (see e. g. [AH87]) and is not repeated here. The pole is located at approximately

$$\omega_p = -\frac{g_m}{C_{out}} \tag{8.28}$$

where g_m denotes M1's transconductance and C_{out} the summed capacitances of the output node to ground. Table 8.4 gives a summary of the small signal values.

g_{m1}	1.53mA/V
g_{mbs1}	264μA/V
r_{ds1}	86.6 kΩ
r_{ds2}	1.16 MΩ
C_{out}	3.07 pF
ν_p	79.3 MHz
t_r	4.4 ns
gain	0.846

Table 8.4: Frontend-Buffer small signal parameters

The nmos-source follower's negative output drive capability is determined by M2's drain current of 100 μA; therefore for negative transitions one has to consider the slew rate

$$\frac{\Delta V}{\Delta t} = \frac{I_d}{C_{out}} \approx 32.5\frac{\text{mV}}{\text{ns}} = 1.63\frac{\text{V}}{50\text{ns}} \tag{8.29}$$

which is sufficient given the dynamic range of approx. 1.1 V and the 50 ns sample-time.

8.5 Discriminator

The inner tracker detector of HERA-B must derive a fast trigger signal indicating a hit channel. The comparator developed by Boris Glass [Gla97] for this purpose is located directly behind the frontend in the analog signal path (see also [Bau96, Com96, Hu95]). The comparator outputs are lead to the bottom side of the chip. Major design goals were the resolution (i. e. a high gain of the differential pair), the comparator speed and the offset voltage homogenity (since all comparators share the same threshold voltage); furthermore the offset variations of the frontends should be accounted for. An AC-coupled differential pair circuit with a subsequent common source circuit was chosen for this purpose (fig. 8.21).

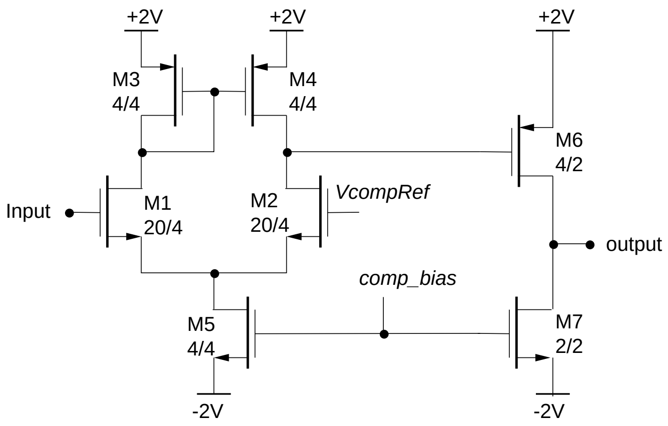


Figure 8.21: Comparator schematic [Gla97]

A small signal model is plotted in fig. 8.22

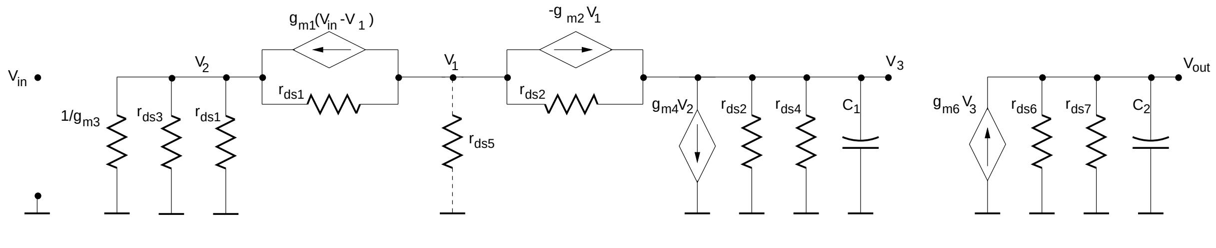


Figure 8.22: Comparator small signal model [Gla97]; C_1 and C_2 denote the total capacitance on the two nodes, respectively. Since transistor M5 is in the linear region, r_{ds5} reaches a fairly low value.

The calculation of the small signal gain is straight forward [Gla97, AH87, San94] and yields

$$\begin{aligned} v_{out} &= \alpha\left(\frac{g_{m1}}{g_{ds2}+g_{ds4}}\right)\left(\frac{g_{m6}}{g_{ds6}+g_{ds7}}\right)\frac{1}{(1+\frac{C_1}{g_{ds2}+g_{ds4}}s)(1+\frac{C_2}{g_{ds6}+g_{ds7}}s)}v_{in} \\ &= \frac{v_0}{(1+\tau_1 s)(1+\tau_2 s)}v_{in} \end{aligned} \tag{8.30}$$

i. e. the product of the low frequency gain with the two poles due to the capacitors C_1 and C_2. Transistor M5 is in the linear region around the comparator trip point so that the M5 on-resistance has to be accounted for and the gain decreases by a factor of

$$\alpha = \frac{r_{on5} \parallel 1/g_{m2}}{r_{on5} \parallel 1/g_{m2} + 1/g_{m1}} \quad . \tag{8.31}$$

For a high-impedance current source α equals 1/2 (unipolar mode of operation, i. e. the reference input is kept at fixed potential), α decreases for r_{on5} decreasing.

There is a difficulty which transistor parameters are to be substitued into eq. (8.30): e. g. for a negative output transition transistors M4 and M7 soon go into the linear range reducing the gain (but improving the time constants). In the tables we will therefore both give the values for the comparator with all transistors (but M5) in saturation and the values for a negative output transition with M4 and M7 in the linear region. The first case happens around the trip point and gives a measure for the input voltage resolution, whereas the second case is valid for most of the transition and hence gives a measure for the output rise time.

	Satur.	Lin.		Satur.	Lin.
$g_{m1} = g_{m2}$	76.8 μA/V	76.8 μA/V	C_2	106 fF	159 fF
g_{m6}	22.1 μA/V	22.1 μA/V	τ_1	21.7ns	2.9ns
$g_{ds2} + g_{ds4}$	0.772 μA/V	9.7 μA/V	τ_2	466ns	2.0ns
$g_{ds6} + g_{ds7}$	0.228 μA/V	78.7 μA/V	α	0.35	0.35
r_{on5}	15 kΩ	15 kΩ	v_0	3360	0.78 (!)
C_1	16.8 fF	27.9 fF			

Table 8.5: Small signal parameters of the comparator [Gla97] with all transistors (apart from M5) in saturation and for a negative output transition with M4 and M7 in the linear region

When the load transistors M4 and M7 enter the linear region, the corresponding resistances drop dramatically and the gain decreases to less than unity; due to the small output resistances the time constants τ_1 and τ_2 reach values in the 2ns region.

Resolution denotes the input voltage interval which causes the comparator output to make a low-to-high or high-to-low transition. Two input voltages differing by more than the input voltage resolution can be discriminated with a proper set threshold voltage. In the given example the input voltage resolution is determined by the conditions around the comparator trip voltage where all transistors (beside M5) are in saturation and hence the value of v_0=3360 (table 8.5) is relevant. In principle the input voltage resolution is determined by the overall gain of all stages up to the point where the signal is observed. Since the output signals of the circuit depicted in fig. 8.21 pass through a couple of digital standard cells with further amplification before they are observed at the chip's trigger outputs, in fact the effective gain is bigger than the one calculated in table 8.5. Hence, resolution is of less concern as compared to the propagation delay of the discriminator.

Time walk or propagation delay is the delay from the time an input passes the threshold to the time an output is valid. In the present case the input signals are shaped pulses with a peak time of 50 ns and a (possible) repetition rate of 10 MHz (100ns) making it extremely important that the comparator reacts fast enough in clear correlation to a bunch crossing. Therefore, the position of the poles in eq. (8.30) is of great importance (assuming that slewing is no problem). Once the input discrimination is done and the comparator starts its (negative output) transition, M4 and M7 enter the linear range and the voltage gain is decreased; due to the fast time constants the negative slewing occurs at maximum speed. For positive output transitions M2 and M6 enter the linear region with even lower resistance values. Thus, the comparators combines maximum voltage resolution with minimum rise time.

Substituting v_{in} in eq. (8.30) by 1/s (i. e. applying a voltage step to the comparator input) and inverse Laplace transformation yields

$$v_{out}(t) = \frac{v_0}{\tau_1 - \tau_2}\left[\tau_1(1 - e^{-t/\tau_1}) - \tau_2(1 - e^{-t/\tau_2})\right] \quad . \tag{8.32}$$

Eq. (8.32) describes an overlay of a positive exponential rise determined by the larger time constant τ_1 with a negative rise determined by the time constant τ_2. v_0 is the finally reached value. The time constants to be substituted into eq. (8.32) are given by the last column in table 8.5. The overall rise time is given by the larger time constant τ_1 and equals app. 3 ns. The (large signal) slew rate of the comparator is uncritical as for all transitions either of the output transistors goes out of saturation so that (constant current) slewing does not happen (charging happens via a passive resistance).

Matching is another focus of the design. The drain current deviation of nmos- and pmos transistors (which includes threshold, mobility and geometric mismatches) with equal gate voltage in close neighbourhood has been measured [AMS95-1] to be depending on the transistor parameters W and L according to

$$\frac{\sigma I_d}{I_d} = \frac{\alpha_1}{W} + \frac{\alpha_2}{L} \quad . \tag{8.33}$$

nmos	$\alpha_1 = 5.02 \cdot 10^{-2}\mu$m	$\alpha_2 = 3.94 \cdot 10^{-2}\mu$m
pmos	$\alpha_1 = 13.45 \cdot 10^{-2}\mu$m	$\alpha_2 = 3.61 \cdot 10^{-2}\mu$m

Table 8.6: nmos- and pmos drain current variation parameters [AMS95-1]

Hence, it is favorable to use devices with large dimensions W and L (as would be intuitively expected); nmos-transistors match better (especially at small transistor widthes). For the comparator discussed a nmos transistor pair with W=20μm and L=4μm has been chosen as input transistors; the load is realized by a pmos transistor pair of $W = L = 4\mu$m.

It is evident that matching is limited by the pmos load transistor pair due to its smaller width and due to the higher α_1-value of pmos-transistors. We can directly refer the load transistor's-drain current variations via g_m to the transistor input according to

$$\sigma V_{in} = (\frac{\sigma I_d}{I_d})\frac{I_d}{g_m} = (\frac{\alpha_1}{W} + \frac{\alpha_2}{L})\frac{I_d}{g_m} \quad . \tag{8.34}$$

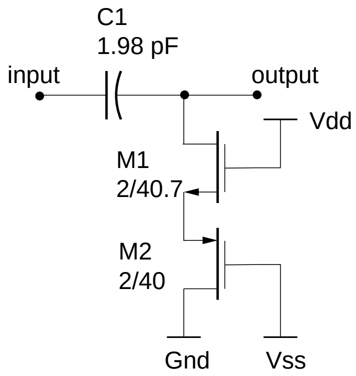


Figure 8.23: AC-coupling of the comparator: two long transistors biased in the triode region are used to form the large (nonlinear) resistor.

Thus, for the M1/M2 drain current of 30 μA the input voltage variation equals 16.6 mV which has to be compared to a signal of 60mV/MIP (from simulation).

The frontend channel offset variation is supressed by AC-coupling of the inputs. AC-coupling is not a very compatible technique with the CMOS process (otherwise one would not have to care about pedestals !). This is due to the fact that capacitances of more than 10 pF can hardly be integrated; the same holds true for poly layer resistors (resistance/square = 27 Ω) of more than a few kΩ. Thus, the maximum time constant reached is in the 50ns regime corresponding to a minimum transit frequency of 3 MHz; this would indicate that the AC coupling would differentiate in most of the signal band frequencies. Therefore, two transistors in the triode region with long channel length L (fig. 8.23) have been chosen to realize the large transistor (R$\geq$ 2MΩ).

For the successful running of the HERA-B experiment an excellent trigger efficiency in combination with an outstanding noise hit rejection is vital. A Monte-Carlo study of a comparator's "fire rate" for a given threshold setting w. r. t. noise has been performed in [Ike95].

8.6 Pipeline

The pipeline (designed by M. Feuerstack-Raible) is a 129 x 141 array of sample & hold switches and capacitors; it serves for the intermediate storage of event data until the arrival of the level 1 trigger (after 10 μs latency). The frontend output voltage is sampled synchronously to the HERA bunch-crossing frequency of 10.4 MHz into the pipeline (approx. 50 ns after the physical event at the peak of the shaped pulse). The latency of 10 μs translates to 104 events which have to be accommodated in the pipeline.

The administration of the various switches is accomplished by the pipeline control logic. This logic receives the sampling clock *Sclk* in phase to the HERA bunch crossings as well as incoming triggers and tags corresonding columns of the pipeline such that they are not overwritten by new data before they are read out. A write pointer scans over the pipeline columns incremented by *Sclk*. After `notReset` is set to +2 V, the pointer starts its walk at column 0, the one nearest to the frontend, wrapping around at column number 140 = 128 + 8 + 5 - 1. With 141 pipeline columns the maximum latency is

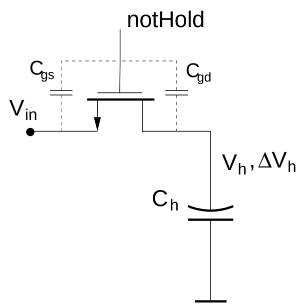


Figure 8.24: Simple sample & hold stage

128 events (8 columns are reserved for the multievent buffer, 5 events account for the readout duration of an event). Sampling the output of the preamplifier/shaper to the storage capacitor is enabled during the high period of *Sclk*, the trailing edge determining the held frontend output value.

A trigger pointer follows the write pointer with the specified latency. When a trigger occurs, the column number which is currently pointed at by the trigger pointer is stored into the FIFO and marked to be read out. The "oldest" number within the FIFO adresses the pipeline column to be loaded into the readout multiplexer. Up to eight level 1 triggers can be accepted (before one event is read out and the corresponding FIFO register is cleared). If no trigger arrives for a given pipeline column, the data will be overwritten when the trigger pointer passes by the next time. The pipeline logic thus independent read/write-operation.

A major concern at the beginning of the design was "crosstalk" in the pipeline. Indeed, the disconnected pipeline capacitors form the highest ohmic node in the analog signal chain. A possible scenario of "crosstalk" would be the charge injection via the switch transistors due to the *read*- and *write* signals. This effect remains negligible, as will be demonstrated in the following. A schematic of a single capacitor cell is plotted in fig. 8.25; minimum size transistors (W=2μm, L=0.8μm) are used to switch the capacitor to the read- or the write-line, respectively.

Since the clock signal undergoes a very large clock transition, it can couple from gate to source or drain via the associated parasitic capacitances. The effect of charge injection is particulary important for the opening switch since the injected charge will remain on the hold capacitor falsifying the sampled value.

For the simple sample & hold stage in fig. 8.24 the voltage change on the hold capacitor due to the switch signal is given by

$$\Delta V_h = \left(\frac{C_{gd}}{C_h + C_{gd}}\right)\min[(V_{in} + V_{th}), (V_h + V_{th})] \quad . \tag{8.35}$$

This can be understood as follows: When the trailing signal edge (in case of a nmos-transistor) occurs, the switch is initially still conducting, so that no charge is injected, since the low ohmic connection (though becoming worse) still persists. Once the digital signal reaches V_{source}+V_{th}, the switch is opened and charge injection to the hold-capacitor occurs for the rest of the transition. V_{source} is the source voltage of the switch transistor, i. e. the minimum of V_{in} or V_h. For the case of a rising input voltage this effect simply introduces a small deviation from the unity gain of the sample & hold stage, but for a falling input voltage the change of voltage becomes noncorrelated to the sampled voltage and has to be considered as a distortion. In the present case, the digital edges are assumed to be a lot steeper than any changes on the analog signal lines, so that $V_{in} = V_h$ and eq. (8.35) reduces to

$$\Delta V_h = \frac{C_{gd}}{C_h + C_{gd}}(V_h + V_{th}) \quad . \tag{8.36}$$

The calculation of the switching actions for the readout of an event in the pipeline is cumbersome. Three switching transitions happen (see also figs. 8.25 and 8.26). In the following calculation the bulk effect's impact on the switch'es threshold voltages has been neglected.

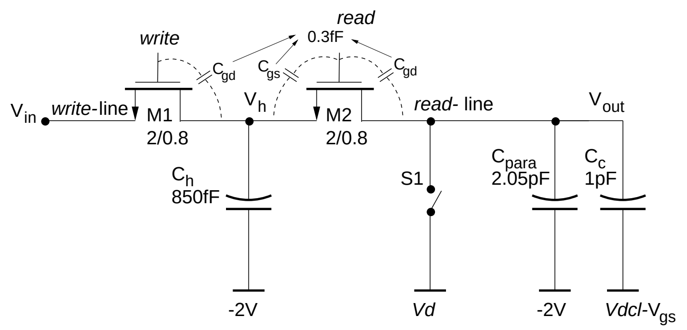


Figure 8.25: Schematic of a single pipeline cell plus readout capacitances

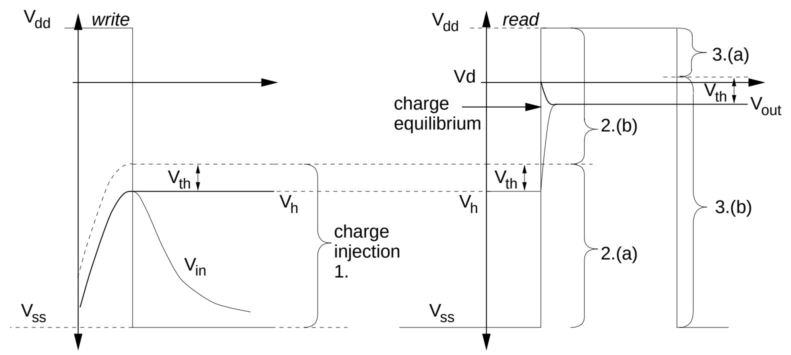


Figure 8.26: Charge injection in the pipeline: the digital signal transitions are plotted on top of the hold-capacitor voltage. The brackets indicate the different switching phases.

1. End of the write-cycle: the write-switch M1 opens. The hold-capacitor voltage $V_h = V_{in}$ is altered by the negative *write*-signal transition. The read-switch M2 is non-conducting, the voltage V_{out} is Vd (S1 is a compensated transmission gate and is assumed to be free from charge injection).

$$V_{h1} = V_{in} - \frac{C_{gd}\,(V_{in} + V_{th} - V_{ss})}{C_h + C_{gd}} \tag{8.37}$$

2. (a) The first phase of the positive *read*-signal transition: M2 is still non-conducting. Hence, C_h and $C_{para} + C_c$ are separately pulsed. A complication: now V_{source} is changed by the transition itself, since there is no connection to a low ohmic voltage. M1 is open (non-conducting).

$$V_{h2a} = \frac{V_{h1} + \dfrac{C_{gd}\,(\,V_{th} - V_{ss}\,)}{C_h + C_{gd}}}{1 - \dfrac{C_{gd}}{C_h + C_{gd}}} \tag{8.38}$$

$$V_{out2a} = \frac{C_{gd}\,(\,V_{h2a} + V_{th} - V_{ss}\,)}{C_c} + C_{para} + C_{gd} + Vd \tag{8.39}$$

(b) The second phase of the *read* transition: M2 has closed now, and a charge equilibrium between C_h and $C_{para} + C_c$ results; for the rest of the transition charge injection occurs to $C_h + C_{para} + C_c$.

$$V_{equi} = \frac{C_h\,V_{h2a} + (\,C_{para} + C_c\,)\,V_{out2a}}{C_h + C_{para} + C_c} \tag{8.40}$$

$$V_{out2b} = 2\,\frac{C_{gd}\,(\,V_{dd} - 2\,V_{ss} + V_{h2a} + V_{th}\,)}{C_h + C_c + C_{para} + 2\,C_{gd}} + V_{equi} \tag{8.41}$$

3. (a) The read-operation ends. In the first phase of the trailing transitions at M2's gate, M2 is still closed, so $C_h + C_{para} + C_c$ are pulsed, and the switch'es source voltage is affected by the transition itself again.

$$V_{out3a} = \frac{V_{out2b} - 2\,\dfrac{C_{gd}\,(\,V_{dd} - V_{ss} - V_{th}\,)}{C_h + C_c + C_{para} + 2\,C_{gd}}}{1 - 2\,\dfrac{C_{gd}}{C_h + C_c + C_{para} + 2\,C_{gd}}} \tag{8.42}$$

(b) M2 is opened now, and charge is injected to $C_{para} + C_c$ (we are only interested in the output voltage).

$$V_{out3b} = V_{out3a} - \frac{C_{gd}\,(\,V_{out3a} + V_{th}\,)}{C_c + C_{para} + C_{gd}} \tag{8.43}$$

The above formulas have to be substituted subsuccessively into eq. (8.43). Unfortunately the result does not provide insight into the problem's nature anymore. By substituting the values the output voltage accounts to

$$V_{out3b} = 0.958 \cdot 10^{-3} + 0.2210\,V_{in} \quad . \tag{8.44}$$

which has to be compared to the ideal equilibrium voltage (see eq. (8.48))

$$\begin{aligned} V_{out} &= \frac{C_h\,V_{in} + (\,C_{para} + Cc\,)\;Vd}{C_h + C_{para} + Cc} \\ &= 0.2208\,V_{in} \quad . \end{aligned} \tag{8.45}$$

Vd is set to 0 in the above considerations. Hence, a small offset of less than 1mV and an increase (sic!) of gain dV_{out}/dV_{in} of 0.11 % result by the switching, which can be neglected.

The very important topic of cell-to-cell variations (along a row) will be discussed in section 8.7.

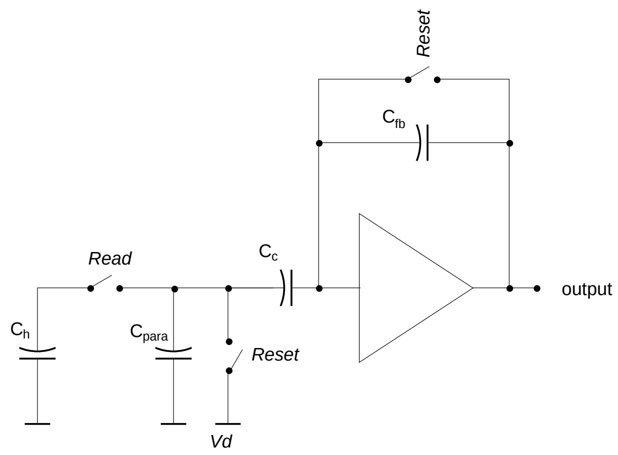


Figure 8.27: Pipeline readout amplifier

8.7 Pipeline Readout Amplifier ("pipeamp")

The pipeline readout amplifier (fig. 8.27) is a resetable AC-coupled charge amplifier designated to read out the charge from the pipeline storage capacitors. The pipeamp is set to its correct operation point by a reset signal unlike the preamplifier which runs continously due to the (large) feedback resistor.

In chapter 6.1.1 the serial noise of the resetable charge amplifier has been found to diverge for $\Delta t_{res} \to 0$, since the weighting function suffers from a steep transition (i. e. change in sensitivity) corresponding to the release of the reset (see fig. 6.2). Calculating the serial noise of the pipeamp for a reset transition Δt_{res}=2ns (this is a rather conservative assumption) using formula (6.6) we obtain ENC$_s$=1440 electrons. Fortunately, the charge gain from frontend input to pipeline capacitor cell is given by 50 mV $\cdot$ 850 fF /MIP $\approx$ 11, so that the overall input referred noise contribution of the pipeamp accounts to only 130 electrons, which is negligible as compared to the frontend noise. Thus, the noise requirements for the pipeline amplifier are greatly relaxed with respect to those of the input amplifier. It might be interesting to notice that the charge gain from detector to pipeline capacitor of the APV5-chip [Fre95, HR96] was considerably smaller so that this chip suffered from a pipeamp noise-contribution. It shall be emphasized again that the serial noise depends heavily on Δt_{res}; a 1ns reset transition would increase the ENC$_s$ by a factor of $\sqrt{2}$.

During the reset-phase the pipeamp output is shorted to the input via a small resistance; the charge sensitive amplifier is thereby transformed into a current sensitive amplifier. The calculation of the loop-gain and the phase-margin is not carried out here; the loop-gain at low frequencies amounts to approx. 6 only due to the small resistance of the reset-switch; the phase-margin amounts to 50 °.

The signals controlling the pipeline charge readout are plotted in fig. 8.28. During the *reset*-signal the pipeline read line and the pipeline amplifier are resetted by closing of the corresponding switches (fig. 8.27). After a pause of one *Sclk*-cycle the read-switch is closed and the hold-capacitor is connected to the pipeamp. After another 2 *Sclk* cycles (=200 ns) the pipeamp output is sampled into the multiplexer.

When a readout has been triggered, the pipeline capacitor C_h discharges via the switches' on-resistance to the parasitic read line capacitance C_{para} resp. to the amplifier input's

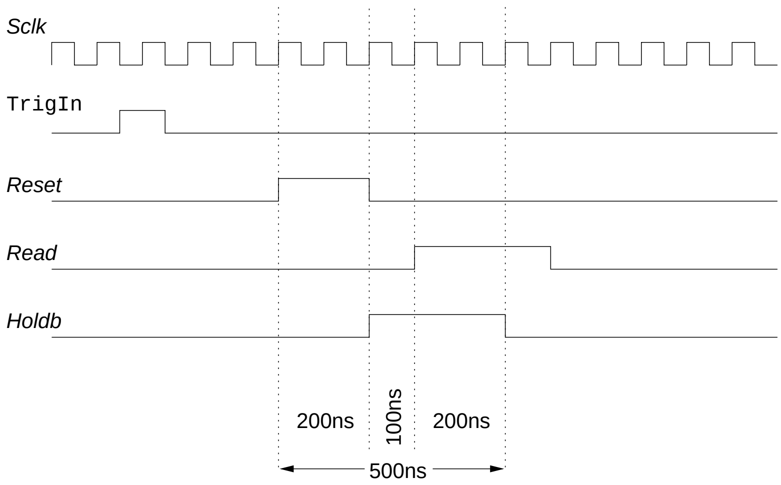


Figure 8.28: Readout cycle of the pipeline

couple capacitor C_c (the physical values are given in table 8.7). At first sight the time behaviour of the discharge process is unclear given the switch'es relatively large on-resistance of 5.27 kΩ.

The time behaviour of the current flowing can be calculated from fig. 8.29 assuming a constant on-resistance of the read-switch. C_c is connected to the "virtual ground" of the pipeamp.

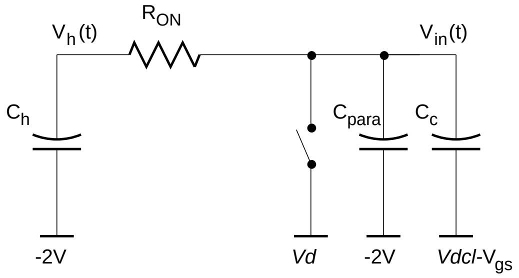


Figure 8.29: Capacitances attributed to the read-line; C_c is connected to the "virtual ground" of the pipeamp ($\approx$ $Vdcl$-V_{gs}). Vd is the reset potential.

Solving the differential equation system

$$\begin{array}{lrcl} \text{I.} & V_h(t) - V_{in}(t) & = & -R_{ON} C_h \dfrac{dV_h}{dt}(t) \\ \text{II.} & V_h(t) - V_{in}(t) & = & R_{ON}(C_c + C_{para}) \dfrac{dV_{in}}{dt(t)} \end{array} \tag{8.46}$$

yields

$$\begin{array}{rcl} V_h(t) & = & (V_h - V_{equi}) e^{-t/\tau} + V_{equi} \\ V_{in}(t) & = & -\dfrac{C_h (V_h - V_{equi})}{C_c + C_{para}} e^{-t/\tau} + V_{equi} \\ \text{and} \quad V_h & = & V_h(t=0) \end{array} \tag{8.47}$$

for the voltages on the hold-capacitance and the amplifier input, respectively. V_{equi} designates the voltage of the charge equilibrium reached and accounts to

$$V_{equi} = \frac{C_h V_h + (C_{para} + C_c)\, Vd}{C_h + C_{para} + C_c} \quad . \tag{8.48}$$

The time constant τ is given by

$$\tau = \frac{R_{ON}}{\frac{1}{C_h} + \frac{1}{C_{para}+C_c}} = R_{ON}(C_h \oplus (C_c + C_{para})) \tag{8.49}$$

implying a 10% -90% risetime $t_{rise} = 2.2 \cdot \tau \approx 7.7$ns. $\oplus$ denotes the series connection of capacitors.

The corresponding current pulse is given by

$$I_{in}(t) = \frac{V_h - V_{in}}{R_{ON}} = \frac{V_h - V_{equi}}{R_{ON}}(1 + \frac{C_h}{C_c + C_{para}})e^{-t/\tau} \quad . \tag{8.50}$$

Consequently, the rise time of the overall system pipeline – read-switch – pipeline amplifier is determined by the amplifier rise time.

The small signal model of the pipeline amplifier is plotted in fig. 8.30 and is obtained in analogy to the preamplifier case. Solving for the output voltage assuming $g_m R_l \gg 1$ and $C_{fb} < C_{tr} < C_c < C_l$ one receives

$$v_{out}(s) = -\frac{1/C_{fb} - s/g_m}{s\left(1 + \frac{C_l(C_{fb}+C_{tr})}{C_{fb}g_m} s\right)} i_{in}(s) \quad . \tag{8.51}$$

For frequencies up to several hundred MHz the numerator is approximately constant, and the amplifier response to a δ-like current pulse can be inferred from the inverse Laplace-transformation of a function of the type

$$F(s) = \frac{1}{s(1+\tau s)} \quad \overset{\mathcal{F}^{-1}}{\Longrightarrow} \quad f(t) = 1 - e^{-\frac{t}{\tau}} \quad . \tag{8.52}$$

Hence, the rise-time of the pipeline amplifier can be deduced to be

$$t_{rise} = 2.2\tau = 2.2\frac{C_l(C_{fb} + C_{tr})}{C_{fb}g_m} = 2.2\frac{C_{in}}{\mathrm{GBW}C_{fb}} \approx 55\text{ns} \tag{8.53}$$

with $C_{in} = C_{fb} + C_{tr}$ and GBW the gain-bandwidth as defined in section 8.2. The values used are given in table 8.7. The load capacitance C_l includes the parasitic line capacitance of a fanthrough line with maximum length, the hold capacitor of the multiplexer sample & hold stage and the input capacitance of the subsequent source follower. Note that the pole location given by eq. (8.52) equals ω_{p2} given in eq. (8.2) for the preamplifier; thus, the rise-time is not affected by the AC-coupling. The charge gain of the pipeamp after the rise time elapsed can be deduced from eq. (8.51) and eq. (8.52) and amounts to

$$v_{out} = -\frac{1}{C_{fb}} q_{in} \quad . \tag{8.54}$$

It is, however, more interesting to refer the gain to the initial pipeline capacitor voltage V_h which is directly related to the frontend output voltage:

$$v_{out} = -\frac{1}{C_{fb}}\frac{C_h C_c}{C_h + C_{para} + C_c} v_h \approx -1.15 v_h \tag{8.55}$$

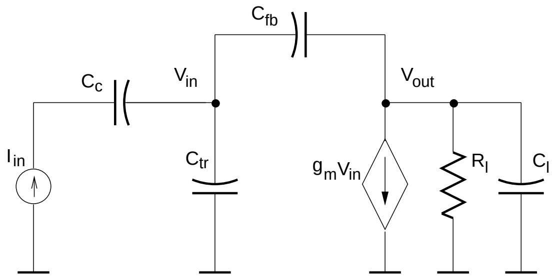


Figure 8.30: Small signal model of pipeline readout amplifier

R_{ON}(read-switch)	5.27kΩ	C_l	2.9pF
g_m	473 μA/V	ν_{p1}	6.4 MHz
C_c	996 fF	τ_1	25 ns
C_{tr}	520 fF	t_r	55 ns
C_{fb}	192 fF	$v_0 = R_l g_m$	106
R_l	224 kΩ	GBW	30.0 MHz

Table 8.7: Small signal values of pipeline amplifier; values are taken from SPECTRE model 2 equations.

It may surprise that an AC-coupled amplifier has been chosen; a DC-coupled charge amplifier with shift of the output voltage as used for the preamplifier would be the natural choice – no extra biases would be needed (for the present AC-coupled amplifier 2 low-impedance bias voltages are required). However, if the input transistor's source (= *Vdcl*) was set to ground, the input node (including the read-line's parasitic capacitance and the hold capacitor) would be pulled down to -V_{GS} of the input transistor (approx. -1.1V). The output voltage would go as low as -1.4V given the frontend offset voltage of ≈-0.8 V and for a feedback capacitor of 850fF, the latter necessary to achieve a gain of one according to

$$v_{out} = -\frac{C_h}{C_{fb}} v_h \quad . \tag{8.56}$$

Given a gain of 50 mV/MIP, +10 MIP would result in an amplifier output voltage of -1.9V which is too close to the -2 V supply voltage. In principle the problem could be solved with a variable *Vdcl* voltage alone, but it turns out that for reasons of cell-to-cell variations it is preferable to AC-couple the amplifier (which requires a second low-impedance voltage).

Fig. 8.31 shows the detailed schematic of the AC-coupled pipeline readout amplifier. A folded cascode has been used again as the open loop gain cell. The "pipeamp" is set into operation by a reset signal; *Vd* and *Vdcl* are set such that the voltages at the gate of M1 and the amplifier output ≈ *Vd*. Hence, capacitors C1 and C2 are discharged (at different *Vd* and *Vdcl* settings, a change of output offset voltage would occur).

The large signal output voltage (including offset voltages) of the AC-coupled charge

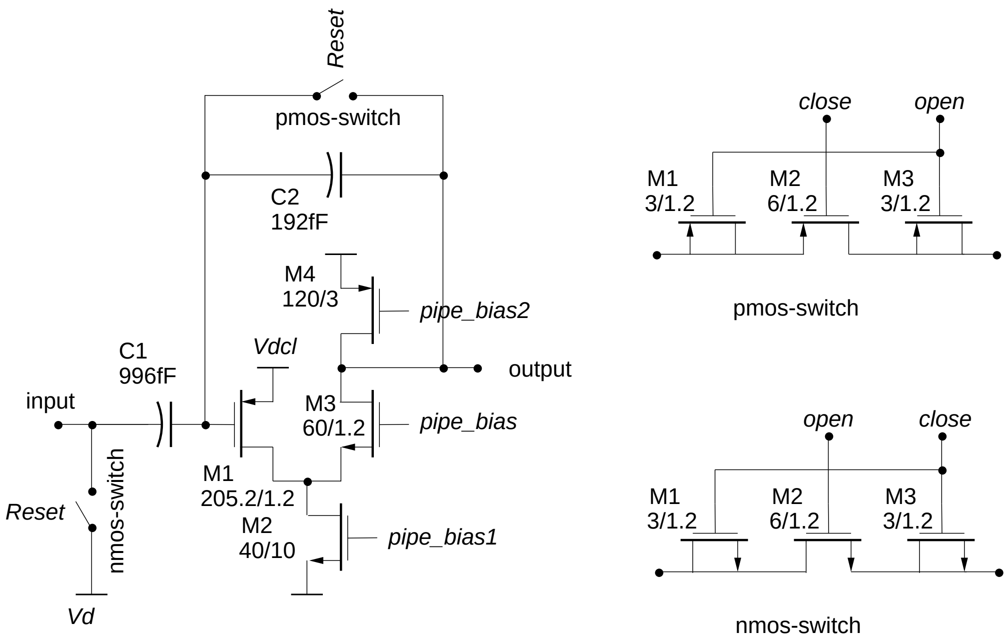


Figure 8.31: Detailed pipeline readout amplifier schematic; the pipeline readout amplifier is a resetable AC-coupled charge amplifier.

amplifier is expressed by equation (8.58)

$$\begin{aligned} V_{out} &= Vdcl - Vgs - \frac{C_c}{C_{fb}}(V_{equi} - Vd) \\ &= Vdcl - Vgs + \frac{C_c C_h (Vd - V_h)}{C_{fb}(C_h + C_{para} + C_c)} \qquad (8.57) \\ &\approx Vdcl - 1.1[V] + 1.15(Vd - V_h) \qquad (8.58) \end{aligned}$$

with the equilibrium voltage as given in equation (8.48). V_h denotes the pipeline capacitor resp. frontend buffer offset voltage of $\approx$ -840mV. Note that the small signal gain given in eq. 8.55 can be obtained by differentiating equation (8.58) to V_h. Vd and $Vdcl$ introduce 2 degrees of freedom to adjust the output offset which can be used in case of radiation damage. $Vdcl$ shifts the output voltage directly, whereas Vd influences the value of the charge equilibrium obtained on the read line.

The switching noise is compensated by the use of half-size dummy transistors at either end of the switch; see section 8.8 for a discussion of the principle.

The sizing of the transistors is mainly determined by open-loop-gain (v=100 being "ordinary") and linearity (especially M4). In both the M1 branch and the M3/M4 load branch a DC current of 25 μA flows, which generates a sufficient input transistor g_m as well as enough current to charge up the load capacitance. The latter point is a large signal consideration and shall be examined more thoroughly in the following: The rise time calculated above in the small signal model holds only true when the maximum slew rate is not exceeded. When the output voltage is lowered, the discharge current of the load capacitance has to take its way through M3 and M2. The current through M2 is fixed by the *pipe_bias1* gate voltage, but M1 will draw less current so that the maximum discharge current is (almost) 50 μA. When the output voltage has to be largely increased, M1 will draw almost the entire 50 μA sourced by M2 by pulling up its drain node. The load capacitance can then be charged up via the drain current of M4 with at most 25 μA. Hence, the output drive strength is asymmetrical; negative output transitions can more easily be accomplished than positive ones. The corresponding output slew rate can be calculated according to

$$\frac{dV_{out}}{dt} = \frac{I}{C} \tag{8.59}$$

and equals 1.72V/100ns for negative transitions and 0.86V/100ns for positive transitions. A transition from +10 to −10 MIP corresponds to a 1.1 V rise at the pipeline amplifier output which can be done in approx. 130 ns and hence lies safely inside the 200 ns read-interval.

Since the frontend output *voltage* is sampled into the pipeline but the *charge* is read out, any variation of the pipeline capacitance immediately affects the output value. This effect can partially be circumvented by use of a voltage amplifier with high input impedance; however, a capacitance dependence remains since charge sharing with the parasitic readout line happens (introducing a dependency on the variation of the parasitic capacitance). Pure charge in – charge out systems [Ted94] do not suffer from capacitance variations at all.

On HELIX128S-2 a middle course has been steered: The value of the couple capacitor has been selected to be 1 pF indicating a large input impedance. According to eq. (8.60) the relative sensitivity to pipeline capacitor changes (approx. 0.17% expected from [AMS95-1]) thus accounts to 75 %; hence the effect of pipeline capacitor variations is even further diminished.

$$\frac{\Delta V_{out}}{V_{out}} = \left(1 - \frac{C_h}{C_h + C_{para} + C_c}\right) \frac{\Delta C_h}{C_h} \approx 75\% \frac{\Delta C_h}{C_h} \tag{8.60}$$

V_{out} pipeline amplifier output voltage

C_h pipeline capacitor 850 fF

C_{para} parasitic read line capacitance $\approx$ 2 pF

C_c couple capacitance 1 pF

There is a price to pay for the enhanced homogenity along a channel. The sensitivity to the parasitic line capacitance is given by eq. (8.61) and amounts to 52 % (with a low impedance input charge amplifier this value would be zero). However, since the parasitic line capacitance is a distributed quantity and process variations over the chip's longitudinal coordinate are already averaged, the variations $\Delta C_{para}/C_{para}$ are believed to be small.

$$\frac{\Delta V_{out}}{V_{out}} = -\frac{C_{para}}{C_h + C_{para} + C_c} \frac{\Delta C_{para}}{C_{para}} \approx 52\% \frac{\Delta C_{para}}{C_{para}} \tag{8.61}$$

8.8 Multiplexer

The silicon vertex detector (SVD) of HERA-B comprises appr. 100000 channels; a similiar number of channels is to be found in the inner tracker detector. It becomes obvious that a means of multiplexing has to be provided to deal with this tremendous amount of channels. The number of channels to be multiplexed is determined by the first level trigger rate of 100 kHz indicating a maximum time of 10 μs to deliver the channel data to the subsequent stage. 256 channels (or 2 chips) multiplexed at a frequency of 40 MHz gives a readout time of 6.4 μs and is the targeted mode of operation (with 30 MHz as fallback solution) [HB94/95].

However, a 40 MHz 128:1 multiplexer is not easily implemented in CMOS technology. A 2.4 μm METAL1 bus line of length $128 \cdot 41.2\ \mu\text{m} = 5.27$ mm has already a parasitic capacitance of 2.3 pF (from CADENCE extraction); however, a bigger part of 16.6 pF comes from the drain-bulk and drain-gate capacitances of the 128 connected switches (having a W/L of $140\mu\text{m}/1.2\mu\text{m}$ to give an on-resistance of 80 Ω). In order to achieve a 20 ns rise time the combined resistance of switch and buffer output resistance must not exceed 480 Ω - a difficult task to accomplish in CMOS without the use of feedback.

Therefore, a two stage multiplexer (fig. 8.32) has been designed: four multiplexers in the first stage each dealing with only a quarter of the 128+8 channels (8 extra channels encoding the pipeline column number) "premultiplex" the channels at a reduced speed of 10 MHz in parallel, followed by a second stage mux multiplexing the four outputs of the first stage muxes together at the final rate of 40 MHz. By means of a permutation fanthrough a reordering of the channels is avoided.

Fig. 8.33 shows the pulse drains controlling the cascaded multiplexer. After the initial *tokenin*-signal from the pipeline control logic, *token* signals are generated for the shift registers of the four first stage multiplexers and the second stage multiplexer which consequently start operation. Mux1 and Mux2 (the uppermost muxes in fig. 8.32) of the first stage deliver the muxed voltages synchronously to *Clk*, mux 3 and 4 synchronously to *notClk*. The output lines of mux 1 and 3 may charge up for 27.5 ns until they are switched to the 40 MHz-output by the second stage mux with another 25ns time-window, in case of mux 2 and 4 the output may slew 52.5 ns (+25ns). Therefore, a more costly creation of four different 10 MHz clocks with 25 ns shift between each other for the first stage multiplexers has been considered to be unnecessary.

For the sample & hold stage a transmisson gate (i. e. a pmos and nmos switch in parallel) has been chosen with each of the switch transistors compensated by two half size dummy transistors.

Since the clock signal undergoes a very large clock transition, it can easily couple from gate to source or drain via the associated parasitic capacitances. The effect of charge injection is particulary important for the opening switch since the injected charge will remain on the hold capacitor falsifying the sampled value.

For the simple sample & hold stage in fig. 8.35 the voltage change on the hold capacitor due to the switch signal is given by

$$\Delta V_h = (\frac{C_{gd}}{C_h + C_{gd}})\min[(V_{in} + V_{th}), (V_h + V_{th})] \quad . \tag{8.62}$$

(see also the treatment in chapt. 8.6).

It is possible to (at least partially) cancel the feedthrough by use of dummy transistors with the drain and source attached to the signal line and the gate attached to an inverse switch signal. This principle has been used extensively in the multiplexer to minimize the effect of switching feedthrough. The dummy transistors serve as capacitors; by applying an inverse switch signal to the gate charge of inverse polarity is injected on either side of the opening switch transistor.

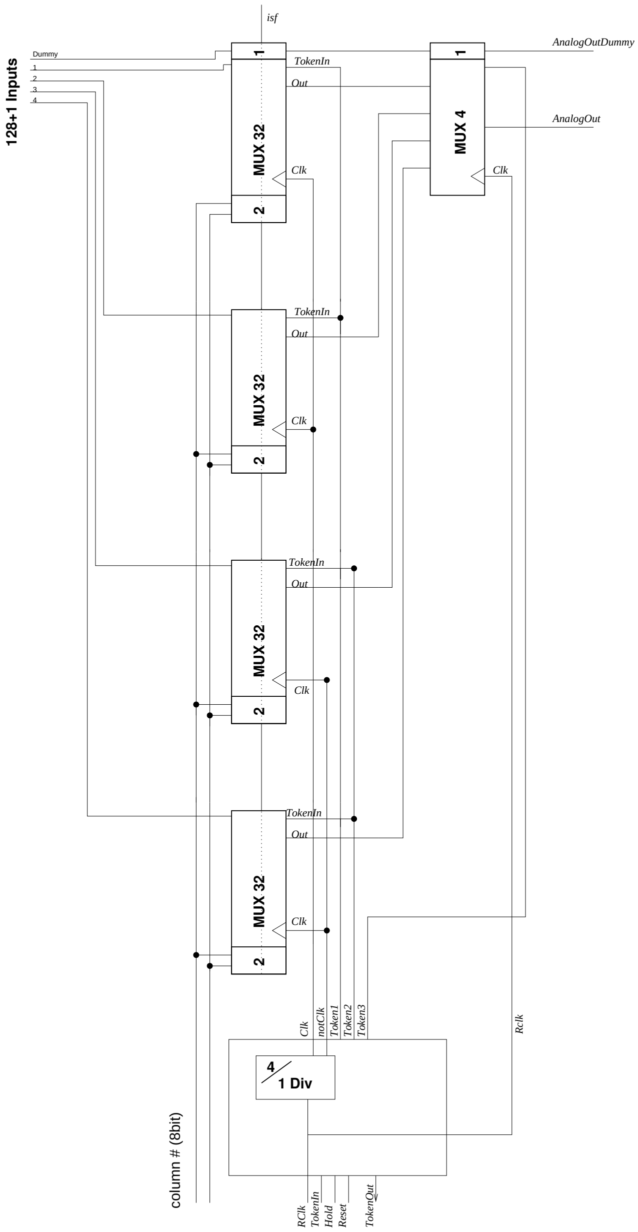


Figure 8.32: Cascaded 128 channel multiplexer; four 32+2 muxes in the first stage "premultiplex" the signal at 10 MHz; the final stage mux runs at full 40 MHz speed.

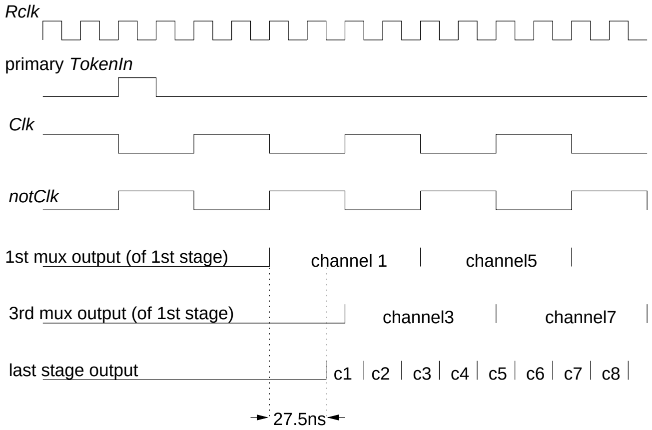


Figure 8.33: Timing diagram of the cascaded multiplexer; Mux 1 and 2 of first stage run with Clk, mux 3 and 4 with the inverted notClk. The second stage multiplexer runs at full output speed and simply switches the precharged first stage bus lines to the output.

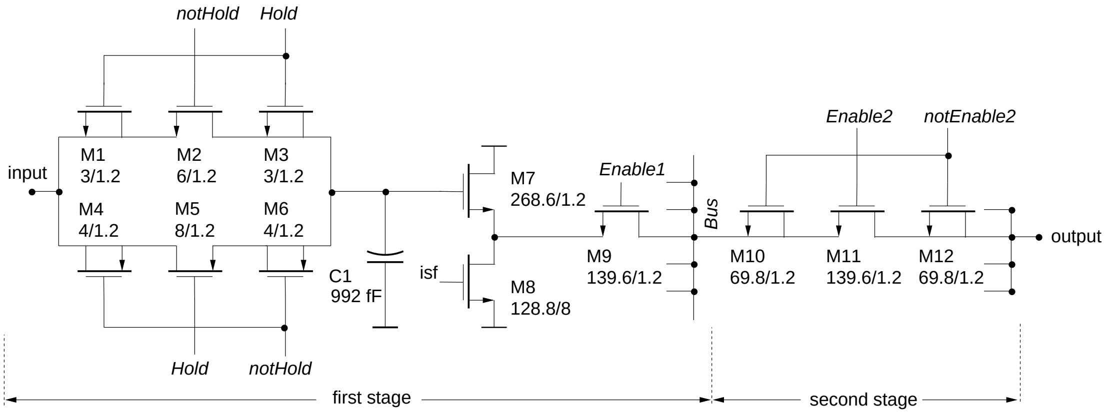


Figure 8.34: Detailed schematic of cascaded multiplexer; the first stage muxes consist of a sample & hold circuit and a source follower; the second stage multiplexer consists of switches only

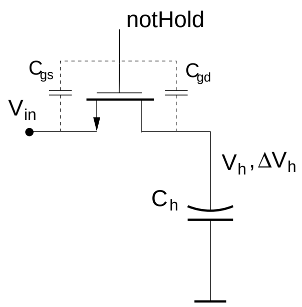


Figure 8.35: Simple sample & hold stage

Approaching 40 MHz, switching feedthrough becomes also important when closing switches since the attributed time constants approach 25 ns; thus, injected charge (which appears at once) can substantially delay the settling of the signal on the analog bus line.

The hold capacitor is buffered by a nmos-source follower (design by J. Kaplon [Kap95]) which has to drive the total bus capacitance which consists of the drain-bulk and drain-gate capacitances of the 34 connected switches (4.41 pF) and the parasitic line capacitance (610 fF). The output pole (including the switches on-resistance of 80 Ω) lies at 54.8 MHz indicating a 10% to 90% rise time of 6.4 ns. Table 8.8 gives a summary of the small signal values (nomenclature as in section 8.4).

g_{m1}	2.00 mA/V
g_{mbs1}	343 μA/V
r_{ds1}	93.2 kΩ
r_{ds2}	1.67 MΩ
C_{out}	5.02 pF
r_{on}	80 Ω
ν_p	54.8 MHz
t_r	6.4 ns
gain	0.85

Table 8.8: Small signal parameters of the MUX-source follower

The slew rate for negative transitions is given by 32.5 mV/ns as in the case of the frontend buffer which is more than sufficient for the 100 ns rise time given.

The second stage multiplexer simply consists of switches and dummy switches (see fig. 8.34).

8.9 Current Buffer

The current buffer at the end of the readout chain has to drive the line up to the receiver which is (in the case of the SVD) located on the vacuum vessel flanch approx. 1m away. Due to several transitions in the line topology (line on hybrid, trace on Kapton cable, coax cable) the designer cannot necessarily assume a perfect matched transmission line with a well defined wave impedance. For voltage buffers using feedback a load of capacitive type (like a not perfecly matched coax cable) can lead to further negative phase shift and to oscillation. Furthermore voltage buffers consume a large amount of power in order to create a small output resistance, good large signal behaviour and high bandwidth.

For the Helix128S-2 a different approach has been chosen. A current type output buffer was designed which achieves a high bandwidth with comparably low power. The analog signal is modulated on a DC output current of appr. 630 μA which is received by a transimpedance receiver.

The current buffer circuit is shown in fig. 8.36. The voltage type input signal from the multiplexer is fed to the noninverting input of a differential amplifier. The inverting input V_{offset} can be adjusted via the corresponding SUFIX register to change the output

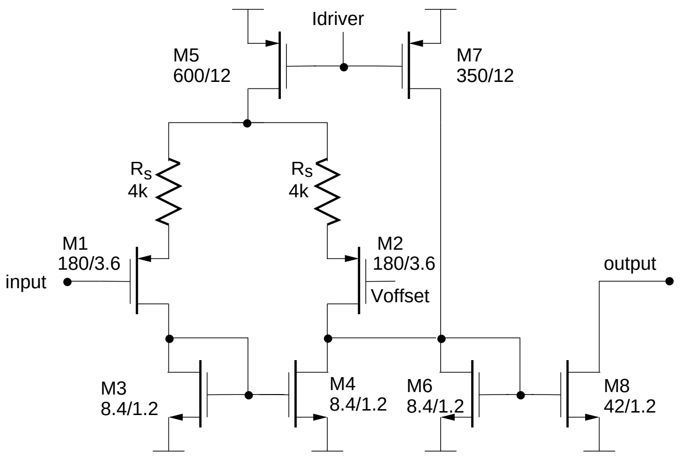


Figure 8.36: Current Buffer

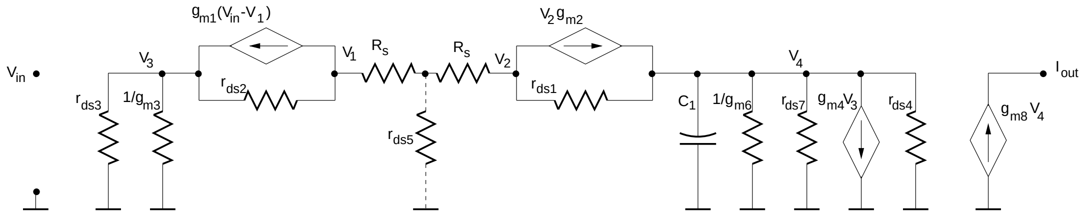


Figure 8.37: Small signal model of current buffer

offset current and to adjust for changes of the input DC level due to process variations or radiation damage.

The current through M5 is set to be 180 μA causing 90 μA to flow in either side of the differential pair configuartion for symmetrical gate biases of M1 and M2. For a signal applied the difference current is collected from the drain of M2 by the low impedance diode connected transistor M6 and mirrored by a factor of 5 to the output. The current through M6 and M7 is slightly detuned from 90 μA to be appr. 105μA; this does not influence the large signal "compatibility" of the differential pair and the M6/M7 current path, but gives a higher offset current giving some reserve for large negative swings of the output signal. The sizing of M5 and M7 is mainly motivated by the linearity range (the input offset voltage of M1 resp. M2 is relatively high) and the implementation of good current sources, whereas the sizing of R_s and M1/M2 is mainly determined by gain (see eq. (8.63)) and linearity. The M6 W/L-ratio is also driven by the gain; M3 and M4 follow M6 to provide large signal matching.

From the small signal model in fig. 8.37 the gain (transconductance) can be calculated to be (with $r_{dsi} \gg 1/g_{mj}$ for all i,j).

$$i_{out}(s) = \frac{2g_{m8}g_{m1}}{g_{m6}(2g_{m1}R_s+1)(1+sC_1/g_{m6})}v_{in}(s) \quad . \tag{8.63}$$

None of the r_{dsi} appear in the transfer function; this is due to the fact that diode connected transistors (with resistances $1/g_{mj}$) lie in parallel at every node. Due to the absence of high impedance nodes a high bandwidth can be reached. In the small signal model only the dominant pole at the node 4 at $\omega_{p1} = g_{m6}/C_1$ is considered; however, the poles on the other nodes lie in close proximity due to comparable values of the g_{mj} and the C_k; this can be seen also from the phase shift in simulation. The dominant pole lies at $\nu_{p1} = 57.3$MHz (simulation 67 MHz) implying a rise time of 6 ns.

The overall low frequency transconductance calculated from eq. 8.37 gives $i_{out}/v_{in} = 1.12mA/V$, the exact solution of the small signal model yields $i_{out}/v_{in} = 0.94mA/V$ as compared to 0.91mA/V in simulation.

$g_{m1} = g_{m2}$	0.504 mA/V	g_{m8}	1.79 mA/V
g_{m3}	0.3 mA/V	ν_{p1}	57.3 MHz
g_{m6}	0.312 mA/V	t_r	6 ns
R_s	4 kΩ	i_{out}/v_{in}	1.12 mA/V
C_1	786 fF		

Table 8.9: Small signal values of the current buffer; values are taken from SPECTRE model 2 equations.

Despite of its usefulness for the calculation of gain and bandwidth, the small signal model inherently cannot give any information on the linearity range of a circuit. The latter, however, has to be considered due to the "built-in" MOSFET square law relation between input voltage (minus threshold voltage) and output current [Tor85].

To make an estimation of the linearity error, we consider a somewhat simplified system consisting of a transistor with source degeneration resistor R_s (left circuit in fig. 8.38). Solving

$$I_d = \beta(V_{gs} - V_{th})^2 = \beta(V_{in} - R_s I_d - V_{th})^2 \tag{8.64}$$

yields

$$I_d = \frac{1 + 2\beta R_s(V_{in} - V_{th}) - \sqrt{1 + 4\beta R_s(V_{in} - V_{th})}}{2\beta R_s^2} \tag{8.65}$$

and $V_s = R_s I_d$. Note that $R_s I_d$ equals the output voltage of a source follower (which is used as frontend buffer and in the multiplexer), but in the present case we obtain the current signal from the transistor drain.

The linear term of the Taylor expansion of eq. (8.65) around the operation point V_g is

$$\frac{\partial I_d}{\partial V_{in}}(V_g) = \frac{\sqrt{1 + 4\beta R_s(V_g - V_{th})} - 1}{R_s\sqrt{1 + 4\beta R_s(V_g - V_{th})}} \approx 140[\mu\text{A/V}] \tag{8.66}$$

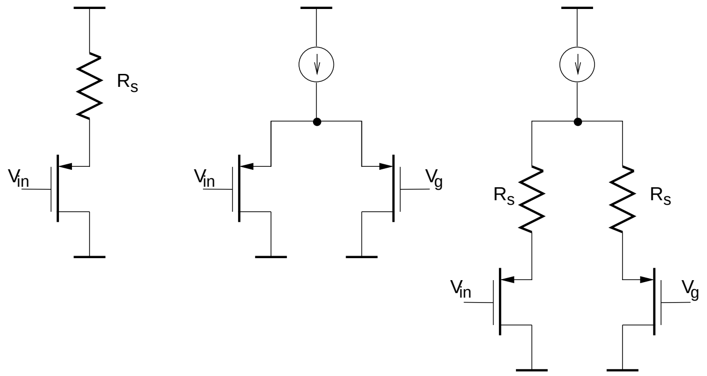


Figure 8.38: Left: transistor with source degeneration (source follower configuration); the source resistance "linearizes" the square law voltage-current relation of the MOSFET. Middle: differential transistor stage; the differential configuration also enhances linearity. Right: differential transistor stage with source degeneration for optimum linearity

as compared to the linear term of the Taylor expansion of the MOSFET transistor in common-source configuration

$$\frac{\partial I_d}{\partial V_{in}}(V_g) = 2\sqrt{\beta I_{d0}} \approx 505[\mu\mathrm{A/V}] \quad . \tag{8.67}$$

Hence, for the bias conditions in the circuit under consideration the gain is decreased by the feedback by a factor of 3.6.

The square term of the Taylor expansion of eq. (8.65) is

$$\frac{1}{2}\frac{\partial^2 I_d}{\partial V_{in}^2}(V_g) = \frac{1}{2}\frac{\beta}{(\sqrt{1+4\beta R_s(V_g - V_{th})})^3} \approx 62[\mu\mathrm{A/V^2}] \tag{8.68}$$

and has to be compared to the square term of the MOSFET equation expansion

$$\frac{1}{2}\frac{\partial^2 I_d}{\partial V_{in}^2}(V_g) = \beta \approx 710[\mu\mathrm{A/V^2}] \tag{8.69}$$

for the underlying circuit. Hence, the square term contribution is decreased by a factor of 11.5; the "linearity improvement" thus equals ≈ 3.

Secondly, the differential configuration itself enhances linearity. Both transistors in the differential stage (middle of fig. 8.38) exhibit equal changes of I_d with opposite sign. Since they share a common source node, the source voltage at the current source's output adjusts to such a value that the gate-source voltage change of the on-biased input transistor remains slightly under half the applied gate voltage change (if the MOSFET equation was linear, exactly half of the voltage change at the input transistor should be seen at the common source node). Dealing with the problem in a mathematical manner, one has to solve the corresponding large signal equation system

$$I_{d1} \;=\; \beta(V_{gs} - V_{th})^2 = \beta(V_{in} - V_{th})^2$$

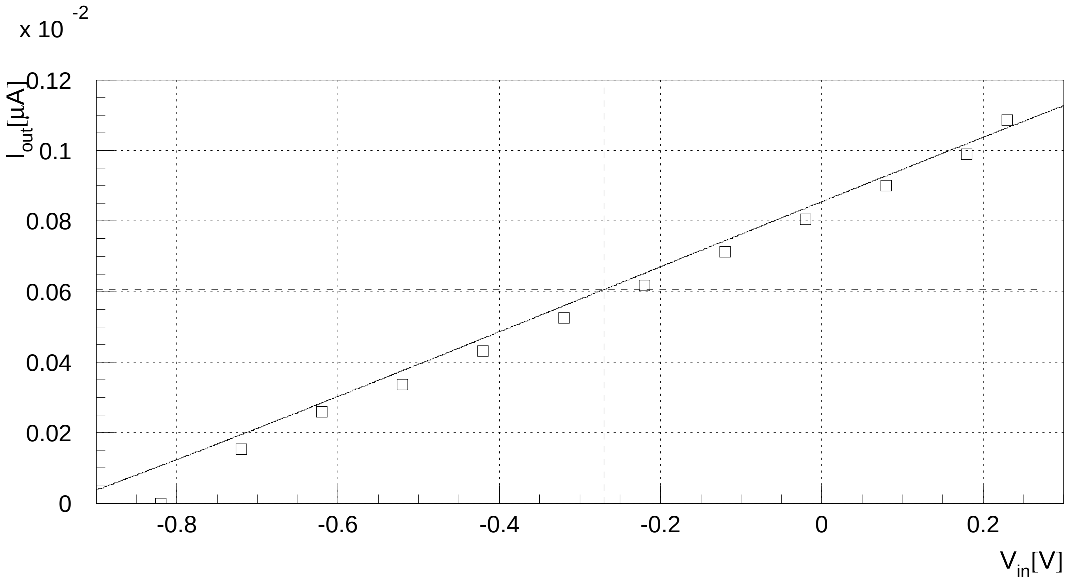


Figure 8.39: Simulated (drawn line) and measured (points) output current vs. input voltage for current buffer at the given operation point

$$\begin{aligned} I_{d2} &= \beta(V_{gs} - V_{th})^2 = \beta(V_g - V_{th})^2 \\ I_d &= I_{d1} + I_{d2} \end{aligned} \tag{8.70}$$

(8.71)

Taylor series expansion of I_{d1} around V_g yields

$$I_{d1} = \frac{I_d}{2} + \sqrt{\frac{\beta I_d}{2}}(V_{in} - V_g) + \mathcal{O}((V_{in} - V_g)^3) \tag{8.72}$$

i. e. the coefficient of the square term vanishes indicating only a third order contribution. It is interesting to notice that applying a signal in a differential manner to inverting *and* noninverting input of a differential pair does not remove the square term contribution of the output current [Kim96].

Calculating the large signal drain current output response of the right configuration of fig. 8.38 becomes cumbersome, and we rather refer to the simulation of the buffer output current. Both effects described before effectively linearize the buffer response. Fig. 8.39 shows the results of simulation and measurement for this configuration.

The negative feedback via the source resistor R_s manifests itself by the input transistor's source voltage V_1. Calculating the voltage V_1 in the small signal model yields (with the same approximations as used before)

$$v_1 = \frac{1}{2}\frac{1 + 2g_{m2}R_s}{1 + g_{m2}R_s}v_{in} \approx \frac{5}{6} \cdot V_{in} = 0.83V_{in} \quad . \tag{8.73}$$

The source voltage v_1 "follows" the gate voltage v_{in} i. e. only 1/6 of the input voltage change accounts to the gate-source-voltage change of input transistor M2.

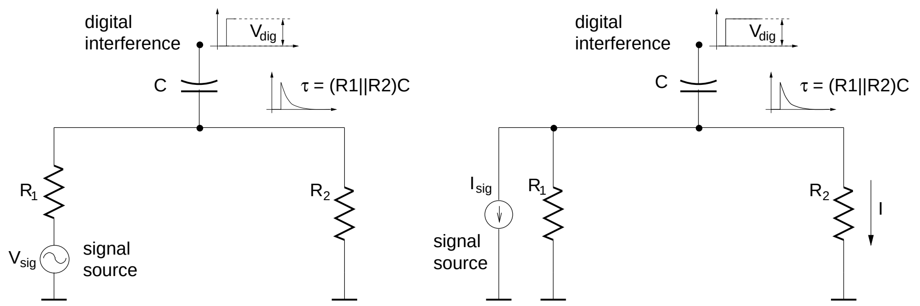


Figure 8.40: Crosstalk to a transmission line driven by voltage output (left) and by a current output (right)

Finally, we want to address the issue of susceptibility to digital interference. We want to restrict ourselves to the case of coupling due to electrical fields, since magnetic crosstalk of (usually) 50 Hz is far away from the signal band and can easily be subtracted as "common mode".

The interference by electrical fields can be modeled by a digital transition coupling to the transmission line over a stray capacitance C. By simple analysis of the voltage buffer driven line in fig. 8.40 (left) one obtains for the signal voltage delivered

$$V_{out,s} = \frac{R_2}{R_1 + R_2} V_{sig} = \frac{R_1 \parallel R_2}{R_1} V_{sig} \tag{8.74}$$

and for the interference

$$V_{out,n} = e^{-t/\tau} V_{dig} \quad \text{with} \quad \tau = (R_1 \parallel R_2)\, C \quad . \tag{8.75}$$

For the signal-to-noise ration we integrate the exponentially decaying pulse from 0 to $+\infty$ assuming a mean rate of n digital transitions. Hence, the signal-to-noise ratio becomes

$$\frac{\mathrm{S}}{\mathrm{N}} = n \frac{R_1 \parallel R_2}{n \tau R_1} \frac{V_{sig}}{V_{dig}} = \frac{1}{n R_1 C} \frac{V_{sig}}{V_{dig}} \quad . \tag{8.76}$$

In the case of the current output buffer the signal current delivered to the receiver equals

$$I_{out,s} = \frac{R_1}{R_1 + R_2} I_{sig} = \frac{R_1 \parallel R_2}{R_2} I_{sig} \tag{8.77}$$

and the interference

$$I_{out,n} = e^{-t/\tau} \frac{V_{dig}}{R_2} \quad \text{with} \quad \tau = (R_1 \parallel R_2)\, C \quad . \tag{8.78}$$

The signal-to-noise ratio amounts to

$$\frac{\mathrm{S}}{\mathrm{N}} = \frac{R_1 \parallel R_2}{n \tau} \frac{I_{sig}}{V_{dig}} = \frac{1}{n C} \frac{I_{sig}}{V_{dig}} \quad . \tag{8.79}$$

On Helix128 (predecessor of Helix128S-2) a voltage buffer was used: for (R_1=5 Ω,V_{sig}= 63 mV/MIP, V_{dig}= 4 V) we obtain S/N=$3.15 \cdot 10^{-3}/nC$, for the Helix128S-2 current buffer with interference from LVDS signals (I_{sig}= 56 μA/MIP, V_{dig}= 175 mV) we get S/N=$3.2 \cdot 10^{-4}/nC$. Hence, even when using lower swing digital signals the susceptibility to crosstalk increases by a factor of 10.

From eq. (8.79) it becomes clear that a different termination scheme with lower impedance level would not result in any improvement. Indeed, nothing helps but reducing stray capacitances and digital signals and/or raising the signal level. Both analog line and digital signals should be laid out differentially. The increased susceptibility is the price to pay for running with current signals.

Chapter 9

Measurement Results

9.1 Frontend

The Helix2.1-frontend (sect. 8.2 - 8.4) used in HELIX128S-2.x has been submitted earlier on a separate chip where its output has been directly acessible to measurement. Fig. 9.1 shows the variation of the pulse shape with the gate-voltage *vfs* of the shaper's feedback transistor. The pulse is almost undershoot-free indicating only a minor imaginary contribution to the pole-value. Gain and peak time can be controlled by *vfs* to account for process variations or radiation damage.

The strong impact of the peak time is well predicted by calculation (fig. 8.14), but the gain increase with falling *vfs*-voltage is stronger developed than expected. Compare fig. 9.1 also to the simulated and calculated response as plotted in fig. 8.16. The gain measured (47 mV) is somewhat smaller than the one expected from simulation (59.6 mV).

Fig. 9.2 shows the measured pulse shape at different *Isha* (i. e. shaper bias current) settings. It is clearly visible that the undershoot decreases with rising *Isha*. This can be well explained by referring to fig. 8.14: the load "resistor's" value decreases, at the same time g_m of the shaper input transistor rises indicating a higher "ideal" load resistor value, i. e. the deviation between real load resistor value and ideal one diminishes. Thus, the imaginary pole contribution shrinks and less undershoot results.

The peak time dependency can be explained as well from fig. 8.14 but the gain predicted by eq. (8.21) resp. fig. 8.14 is wrong. The reason is that the load "resistor's" decrease is not accounted for in the formula (actually it assumes the ideal load resistance given by eq. (8.19) to be inserted in the gain-cell which *increases* as mentioned above). A smaller load resistor, however, indicates a smaller gain as observed experimentally.

Fig. 9.3 shows the flow of gain and peak time vs. external input capacitance C_{in} (simulated/measured). The gain decreases with increasing input capacitance since the preamplifier risetime goes up with increasing input capacitance according to eq. (8.10); the convolution with the shaper weighting function yields a lower gain. The gain decreases, however, more than is expected from the simulation; this means according to eq. (8.10) that one or more of the values making up Z_{in}^{ohm2} must deviate from the simulation value. This does *not* affect the noise unless g_m is the cause of the deviation (eq. (7.44)).

The increase in peak time vs. capacitance is rather gentle; the measured values lie higher than the simulated ones confirming the somewhat slower risetime of the preamplifier

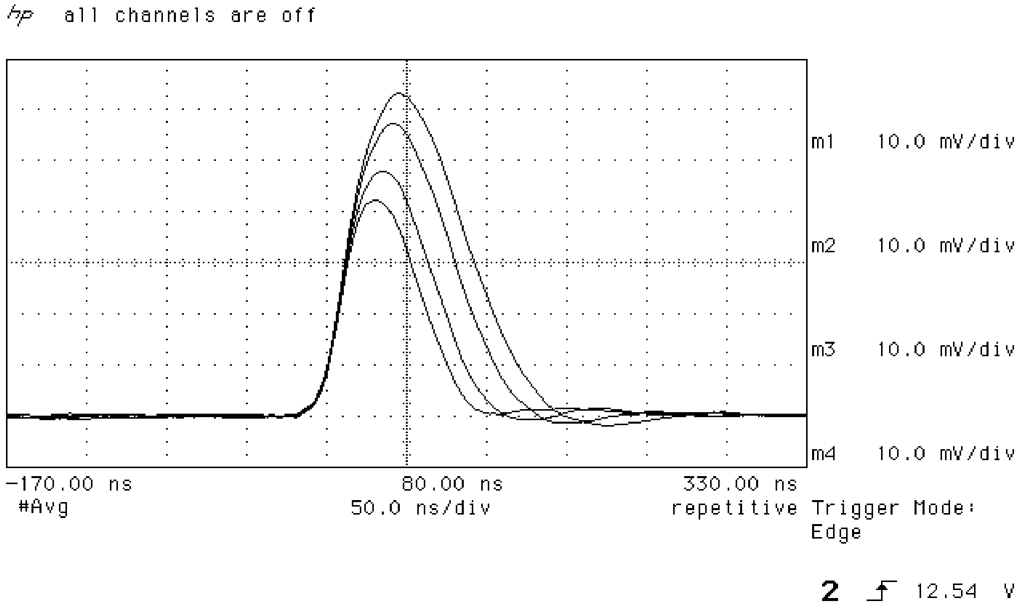


Figure 9.1: Impact of *Vfs* on Helix2.1-frontend's pulse shape; from top to bottom: *Vfs* = 0.8 V, 1 V, 1.5 V, and 2 V

w. r. t. expectation. Under experimental conditions, where detectors like the double-sided strip-detector described in chapt. 2 with different values of C_{in} are used, the peak time may be adjusted by tuning of I_{pre} according to eq. (8.2) ($g_m \propto \sqrt{I_{pre}}$).

9.2 Discriminator

Fig. 9.4 shows the comparator offsets measured for 48 comparator channels spread over three IDEFIX test-chips. It is clearly visible that the deviation observed (assuming all points to be inside a 3σ band yields σ=4 mV) is much smaller than the expected standard deviation of 16.6 mV which follows from the AMS-process parameters [AMS95-1]. Unfortunately measurements do not often reveal such pleasant surprises. It remains to be seen, though, how reproducible these values are for chips from different production batches. Since the trigger threshold can be programmed individually for every chip, inter-chip process variations can be compensated for in later operation if necessary.

9.3 Overall Chip Performance

Fig. 9.5 shows the multiplex-signal `AnalogOut`−`AnalogOutDummy` of HELIX128S-2.2 operating at 20/40 Mhz `Sclk/Rclk` frequency measured at 1.5 kΩ transimpedance. The analog "data frame" consists of 128 amplifier channels + 8 channels encoding the pipeline column number. Charge signals have been injected into six channels which are visible as peaks. Fig. 9.6 shows a detail of the data frame around a channel carrying a 4 MIP signal. The channel borders are marked by small furrows. The signal channel's plateau

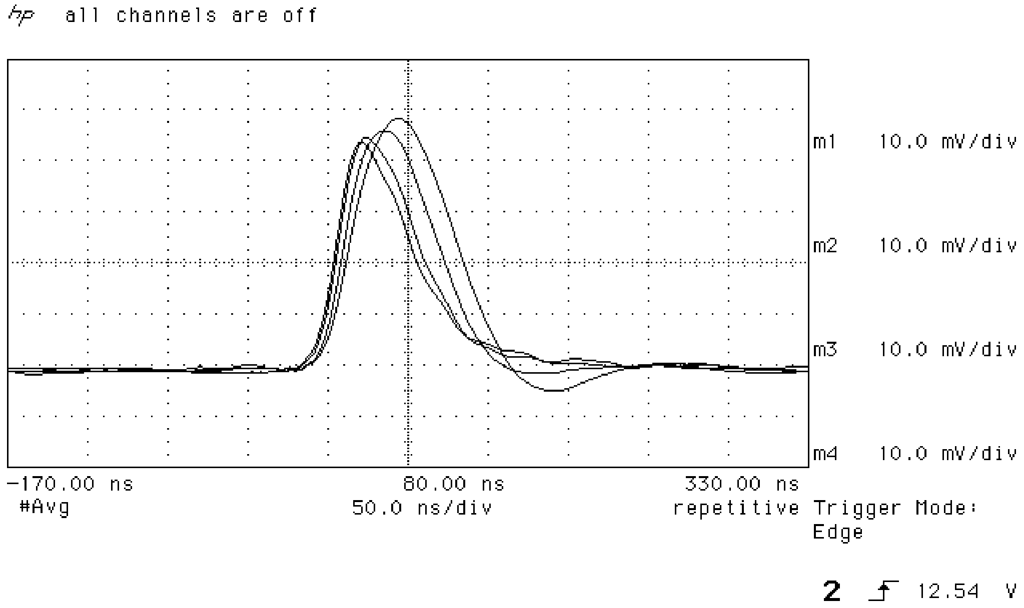


Figure 9.2: Impact of *Isha* on Helix2.1-frontend's pulse shape: from slowest to fastest pulse: *Isha* = 60 μA, 100 μA, 200 μA, and 300 μA

is well developed; unfortunately, the following channel's value seems to be affected. One observes two phenomena in fig. 9.6 which are not yet completely understood: first, there exists an asymmetry between the rise time of approx. 6.5 ns and the falltime of approx. 13ns. This is, however, sufficient given the 25 ns time window at 40 MHz readout frequency. Secondly, pairwise crosstalk between channels (2n,2n+1) of approx. 8 % is observed which has been found to be almost *independent* of `Rclk`. Even if the pattern follows an asymmetry in the pipeline, the origin is not yet clear. Refer also to the section "Known Problems" of the User Manual, appendix D.

The overall linearity of HELIX128S-2 (fig. 9.7) has been measured at low *Sclk*-frequency to avoid the dynamic range limitation described at the beginning of this chapter. The linearity deviation is less then 10 μA (resp. 1%) over the entire range of -10 to 10 MIP. Of course the slightly smaller frontend gain helps to achieve this figure. It can be concluded that the linearity range is fully satisfactory for both silicon and microstrip gas detectors. The linearity measurement has to be repeated for HELIX128S-2.2 due to the modified components of the analog signal chain.

Fig. 9.8 shows the noise performance (ENC) vs. input capacitance of HELIX128S-2.1 from measurement and simulation. The measured noise ENC=474 e^{-}+35 e^{-}/pF $\cdot C_{in}$ (I_{pre} = 200μA, t_{peak}=50 ns, best value obtained so far [Sex98-1]) has a comparable slope as the simulated value ENC=287 e^{-}+35 e^{-}/pF $\cdot C_{in}$, but a 187 e^{-} higher offset value. The value measured thus indicates a higher input capacitance than expected; it is emphasized that the measured result cannot be explained with noise from a later stage or with parallel noise (since this would imply a deviation from the strict linearity observed) or a too low input transistor transconductance g_m or some other noise source in the preamplifier (since this would increase the slope). 187 e^{-} correspond to 5 pF of additional input capacitance.

A thorough investigation of the input capacitances not covered by the simulation yields ≈700 fF of pad capacitance, ≈90 fF due to the protection diodes (the leakage current being 1.3 fA resp. 5.3 fA) and another 93 fF resp. 186 fF due to the the test-pulse couple capacitors. Thus, an additional input capacitance of ≈1 pF can be explained from the layout. The origin of the rest of the input capacitance is unclear.

HELIX128S-2.1 has been found to be relatively radiation weak; the reason for this behaviour has been found to be the pipeamp (again !). The HELIX128S-2.2 irradiation test therefore has been eagerly expected. Currently (end of april) the chip performs well after 150 krad where some of the bias settings have to be adjusted [Tru98].

9.4 Conclusion

The characterization of HELIX128S-2.2 is not yet fully terminated. However, with HELIX128S-2.2 the major problems encountered with HELIX128S-2.0/2.1 – keywords digital circuitry, pipeline readout amplifier offset, reduced radiation hardness, comparator crosstalk – have been successfully tackled.

The minor flaws encountered by now – pairwise channel crosstalk, fall time of current buffer close to the 40 MHz limit, non-differential output line, loss of a few triggers due to an unhandled condition in the logic – do not inhibit the use of the chip in the HERA-B experiment.

Important measurements to be redone for HELIX128S-2.2 are linearity, pipeline homogenity, and noise. Especially the latter constitutes a stubborn problem; since it reappears periodically, a low-noise measurement site should be installed making use of professional noise reduction techniques (e. g. [Ott88]).

The silicon vertex detector and the inner tracker detector of HERA-B will be equipped with HELIX128S-2.2 in 1999; inspection of the first 10 wafers delivered by AMS indicates a remarkable yield of well above 50 % [Sex98-2]. Thus, after three years of development, the HELIX-project is drawing to a successful close.

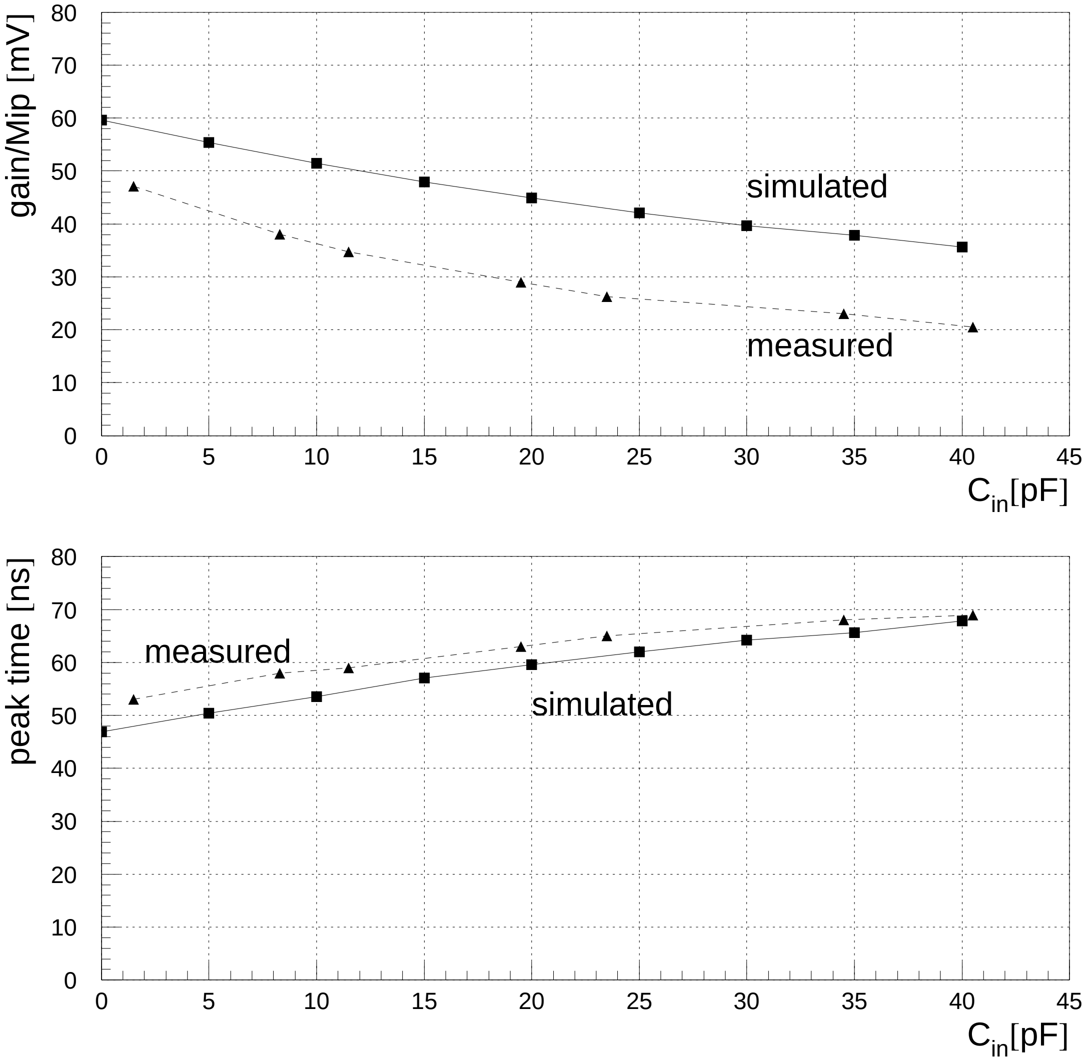


Figure 9.3: Gain and peak time vs. external input capacitance (simulated/measured); the measured gain and input impedance are lower than expected from simulation [Sac98].

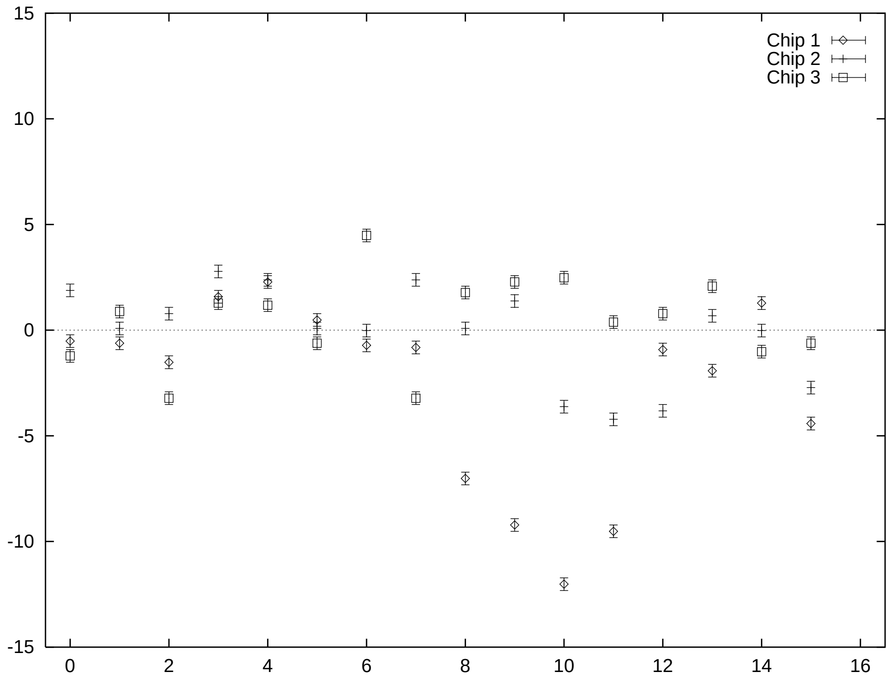


Figure 9.4: Comparator offset variations measured on three IDEFIX test chips with 16 channels each [Gla97]

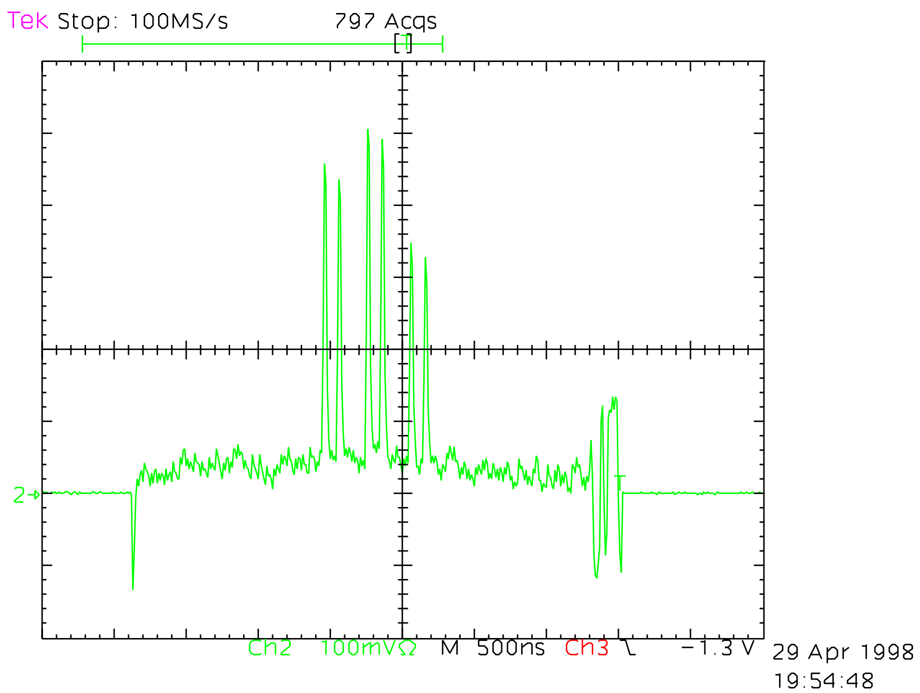


Figure 9.5: Analog multiplex-signal `AnalogOut-AnalogOutDummy` of HELIX128S2.2 (40 MHz `Rclk`); charge signals have been injected into six channels [Tru98].

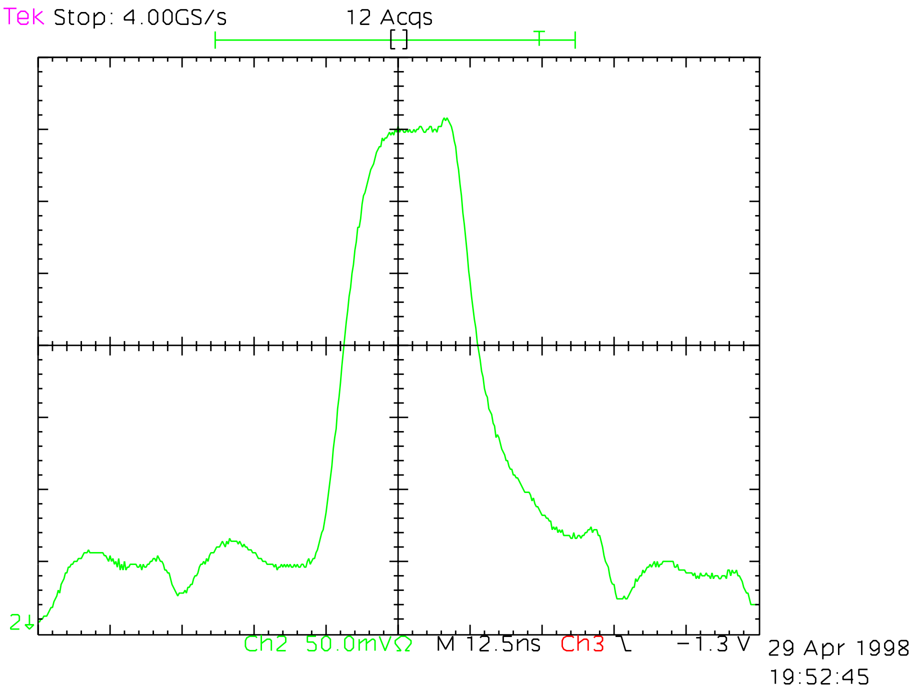


Figure 9.6: Analog multiplex-signal *AnalogOut-AnalogOutDummy* of HELIX128S2.2 (40 MHz `Rclk`); one channel carries a 4 MIP-signal [Tru98].

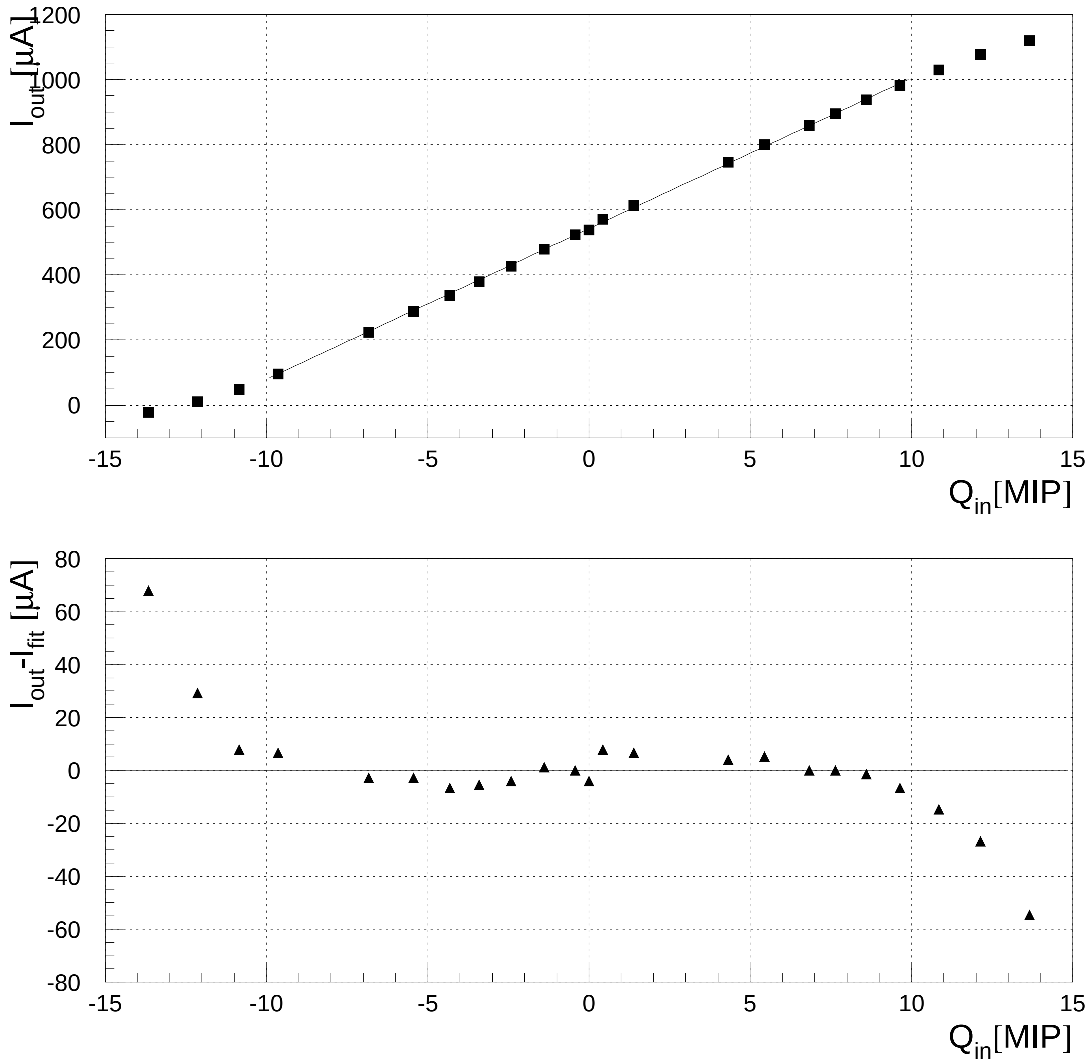


Figure 9.7: Measured linearity of HELIX128S-2 at low `Sclk`-frequency

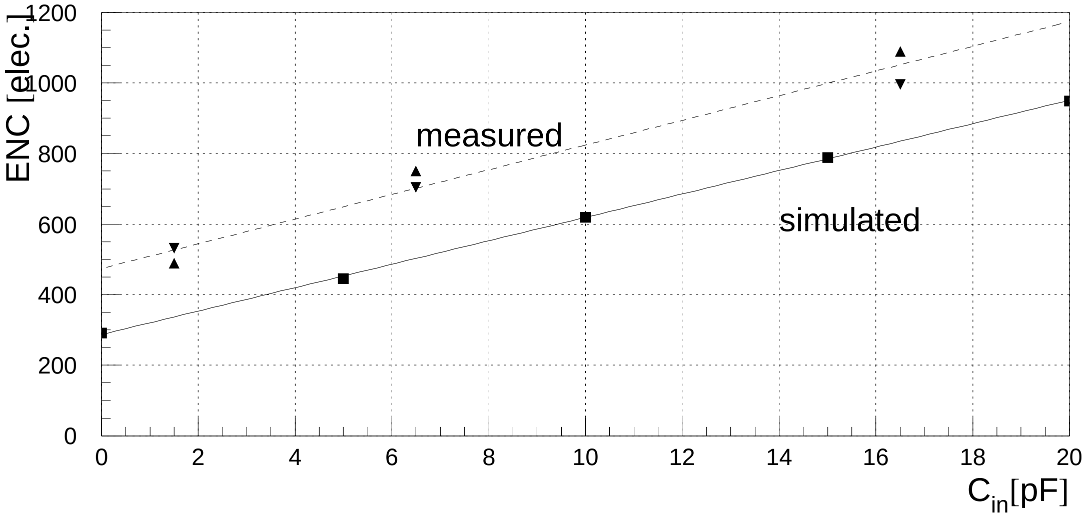


Figure 9.8: Equivalent noise charge (ENC) vs. external input capacitance (simulated/measured) of HELIX128S-2.1; the measured slope (best value obtained so far [Sex98-1]) coincides with the slope from simulation and calculation, but the offset indicates an additional capacitance at the input.

Appendix A

Laplace-Transformation

It is a substantial drawback of the Fourier-tranformation (chapt. 5.1.1) that the Fourier-integral does not converge for technically interesting signals like the Heaviside-step function $U(t)$ [Hin96, Hol73, WS93] defined by

$$U(t) = \begin{cases} 0 & : \quad t < 0 \\ 1 & : \quad t \geq 0 \end{cases} \quad . \tag{A.1}$$

However, the Fourier-integral exists for a function $f_\sigma(t)$ which is created from a function $f(t)$ according to

$$f_\sigma(t) = e^{-\sigma t} U(t) f(t) \tag{A.2}$$

for all $\sigma > \gamma$ if $f(t)$ belongs to the set (also called signal space)

$$S_\gamma = \{f | f \text{ piecewise continous}; |f(t)| < K e^{\gamma t} \text{ for all } t; K, \gamma \text{ real}\} \quad . \tag{A.3}$$

In other words, $f(t)$ must be bounded by an exponential function $Ke^{\gamma t}$ for some real numbers K, γ.

Thus, σ can be chosen such that the Fourier-Integral of $f_\sigma(t)$

$$\mathcal{F}(f_\sigma(t)) = \mathcal{F}(e^{-\sigma t} U(t) f(t)) = \int_0^\infty f(t) e^{-(\sigma + j\omega)t} \, dt \tag{A.4}$$

exists, and one defines the Laplace-tranformation $\mathcal{L}$ of $f(t)$ inside the integral's convergence region C

$$C = \{s | s = \sigma + j\omega; \ \mathrm{Re}(s) = \sigma > \gamma\} \tag{A.5}$$

to be

$$\begin{aligned} \mathcal{L}: \ S_\gamma &\rightarrow S^*_\gamma \\ \mathcal{L}(f(t)) &= \mathcal{F}(f_\sigma(t)) \end{aligned} \tag{A.6}$$

where S^*_γ is defined as the image signal space of S_γ according to

$$S^*_\gamma = \left\{ F | F(s) = \int_0^\infty f(t) e^{-st} \, dt, f \in S_\gamma \right\} \quad . \tag{A.7}$$

As in the case of the Fourier-transformation, function $f(t)$ and the Laplace-transform $\mathcal{L}(f(t))$ form a pair

$$\begin{aligned}
\mathcal{L}(f(t)) &= F(s) = \int_0^\infty f(t)e^{-st}\,dt \\
\mathcal{L}^{-1}(F(s)) &= f(t) = \frac{1}{2\pi j}\int_0^\infty F(s)e^{st}\,ds
\end{aligned} \tag{A.8}$$

where $s = \sigma + j\omega$.

In the following tables some calculation rules and the most common Laplace-transform pairs are given.

$f(t)$	$F(s)$
$\alpha f(t) + \beta g(t)$	$\alpha F(s) + \beta G(s)$
$f(t-\tau)$	$e^{-s\tau}F(s)$
$e^{-at}f(t)$	$F(s+a)$
$f(at)$	$\frac{1}{a}F(\frac{s}{a})$
$\dot{f}(t)$	$sF(s) - f(+0)$
$\int_0^t f(\tau)\,d\tau$	$\frac{1}{s}F(s)$
$\int_0^t f(\tau)g(t-\tau)\,d\tau$	$F(s)G(s)$

Table A.1: Calculation rules for the Laplace-transform

$f(t)$	$F(s)$	$f(t)$	$F(s)$
$\delta(t)$	1	$\sin(at)$	$\frac{a}{s^2+a^2}$
$1 \quad (= U(t))$	$\frac{1}{s}$	$\cos(at)$	$\frac{s}{s^2+a^2}$
t	$\frac{1}{s^2}$	$e^{at}\sin(bt)$	$\frac{b}{(p-a)^2+b^2}$
e^{at}	$\frac{1}{p-a}$	$e^{at}\cos(bt)$	$\frac{s-a}{(p-a)^2+b^2}$
te^{at}	$\frac{1}{(p-a)^2}$	$\frac{1}{\sqrt{\pi t}}$	$\frac{1}{\sqrt{s}}$
$\frac{t^{n-1}}{(n-1)!}e^{at}$	$\frac{1}{(p-a)^n}$	$2\sqrt{\frac{t}{\pi}}$	$\frac{1}{s\sqrt{s}}$

Table A.2: Laplace-transform of the most commonly used functions

It is a good exercise for the reader to remember the location of the poles and zeros of the Laplace-transforms; thus, when analysing a transfer function, the time response can be immediately inferred.

Appendix B

Small Signal Analysis

Analog circuit design [AH87, GT96, San94, San98] relies on analytical understanding of the behaviour of circuits consisting of active and passive devices. In a first step, first-order models must be used to evaluate circuit performance. Ideally, analytical expressions can be derived for the quantities of interest (gain, bandwidth, noise etc.).

In a later step, more detailed models including second-order effects can be used to verify the assumptions made; this step in designing a circuit is called simulation and is achieved by computer programs (e. g. SPICE). These models - although very precise - are not suitable for hand calculations due to their complex nature.

SPICE can use different models for a given physical device. It is the task of the semiconductor company to provide the device parameters to be inserted into a transistor model (e. g. AMS supports the MOS models 2,6, and 15). Accurate modelling is much more important in analog circuits than in digital ones. In fact, it is one of the major issues of state-of-the-art processes to obtain good models of devices. This is still aggravated by shrinking process geometries rendering the extraction of good parameters more complicated.

In this chapter we will present the "simple" first-order models used in the treatment of amplifiers throughout chapter 8. Typically, one uses in hand calculation two different models for a given device, the second one ("small signal model") being a linear approximation of the first one ("large signal model").

Most active elements of a circuit behave in a nonlinear way (see e. g. the MOS transistor transfer characteristics given below). A model that describes the device behaviour over a wide range of voltage and current conditions is called a *large signal model* (see e. g. eq. (B.1)).

The *small signal model* is obtained by Taylor expansion of the voltages and currents involved in the device w. r. t. each other. Only the coefficients of the linear expansion terms are considered since only first order dependencies are of interest. Usually the dependencies of dimension [Ω] or [$1/\Omega$] are plotted into a schematic as plotted e. g. in fig. B.2. Usually, the (independent) noise sources are added as well.

In the *small signal analysis* of a circuit all transistors and other nonlinear elements are replaced by their small signal model. Small signal analysis thus predicts the circuit performance only for small excitations. Excitation in this sense refers not only to voltages or currents, but can also include device variations. Typical subjects to be examined by a small signal analysis are gain, input or output resistance, common mode suppression etc. . We denote small signal quantities by lower case letters while large signal quantities are written using capital letters.

The basic rules for the transition from a schematic to a small signal schematic are given below; small signal substitutions and calculations are carried out throughout chapter 8.

1. determination of the operation points of transistors, diodes and other nonlinear elements using large signal models
2. substitution of devices by their small signal models using the parameters at the (large signal) bias condition determined in step 1
3. all fixed sources like power lines or bias currents are set to zero (only changes are of interest)
4. all controlled sources with static control voltage or current are set to zero (see step 3)
5. simplification of network where possible to simplify calculations

By use of Kirchhoff's laws the small signal schematic can be solved by hand or by the use of symbolic circuit calculation programs [Som95].

B.1 MOSFET

B.1.1 Basics

MOSFET stands for metal-oxide-semiconductor field-effect transistor [AH87]; the first part of the name denotes the order of physical layers which make up a transistor of this type. The structure of an n-channel MOS transistor on a p-subtrate technology (as the AMS CMOS technology) is shown below in fig. B.1. The n-channel device is formed with two heavily doped n^+-regions diffused into a lighter doped p^- material called the substrate (or bulk). The two n^--regions are called drain and source, and are separated by a distance L (channel length). At the surface between the drain and the source lies a gate electrode that is separated from the silicon by a thin dielectric material (silicon dioxide). The width W of the gate electrode determines the width of the underlying conducting channel (at appropriate gate voltage).

For a p-substrate technology, all nmos-transistor bulks are identical; pmos transistors which are built identically to nmos-transistors but with all dopings reversed (n dotation $\Rightarrow$ p-dotation) are located in n-wells which have to be separately contacted; the wells of different PMOS transistors can be put to individual potentials.

With all four terminals of an nmos-transistors grounded, a depletion region is formed between the n^+-source/drain-implants and the p^--substrate; correspondingly, the source-drain resistance is very large ($\approx 10^{12}$ Ω). When a positive potential is applied to the gate with respect to the source, positive charge accumulates on the gate and negative charge in the substrate under the gate (i. e. the gate-oxide capacitance WLC_{ox} is charged). When the gate-source voltage V_{gs} exceeds a certain threshold voltage V_{th}, the p-type silicon material under the gate becomes n-type so that an n-conducting channel is formed

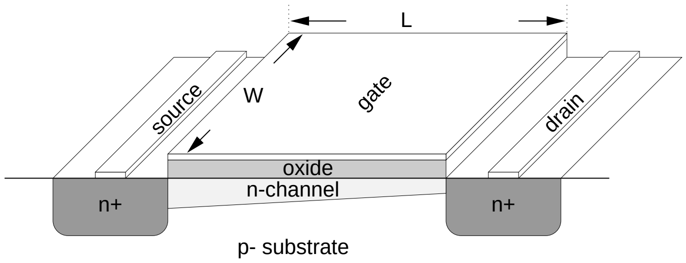


Figure B.1: Physical structure of a nmos-transistor [San94]

between drain and source. This phenomenon is known as strong inversion. Now a drain current I_d flows between the two terminals. For relatively small drain-source voltages ($0 < V_{ds} < V_{gs} - V_{th} = V_{Sat}$) the channel behaviour is ohmic; if V_{ds} exceeds V_{Sat}, the depletion layer between drain and bulk (which form a reverse biased pn-junction) extends into the conducting channel and forces a constant current behaviour independent of any further increase of drain voltage. In analog circuits MOS transistors are most often operated in this region called the saturation region.

B.1.2 Large Signal Model

The large signal model describes the MOS transistor's behaviour for all bias conditions; depending on the gate-source voltage V_{gs} and the drain-source voltage V_{ds} three modes of operation can be distinguished [AH87, San94]: cutoff for $V_{gs} < V_{Th}$, ohmic region for $V_{gs} > V_{th}$ and $0 < V_{ds} < V_{Sat}$, and saturation region for $V_{gs} > V_{th}$ and $V_{ds} > V_{Sat}$. The drain current for these conditions is given by

$$I_d = \begin{cases} \approx 0 & & V_{gs} < V_{Th} \\ \frac{W}{L}\overline{\mu}_n C_{ox}\left[(V_{gs} - V_{th})V_{ds} - \frac{V_{ds}^2}{2}\right] & 0 < V_{ds} < V_{Sat} & \\ & & V_{gs} > V_{Th} \\ \frac{W}{L}\overline{\mu}_n C_{Ox}(V_{gs} - V_{th})^2 & V_{ds} > V_{sat} & \end{cases} . \tag{B.1}$$

W,L MOS transistor channel's width and length

μ_0 mobility of charge carriers in channel

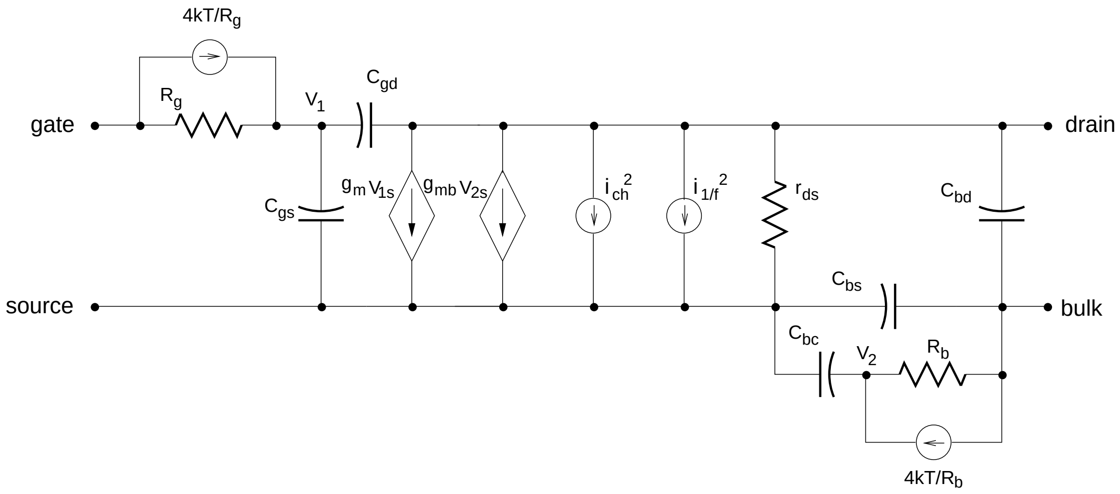
C_{ox} oxide capacitance per unit area

V_{gs} gate-source voltage

V_{th} threshold voltage

I_d (large signal) drain current

For $V_{gs} > V_{th}$ and $0 < V_{ds} < V_{Sat}$ the MOS transistor channel exhibits a linear or ohmic behaviour, i. e. $I_d \propto V_{ds}$ (apart from the square term contribution); this region of operation is also called the triode region. In the saturation region with $V_{gs} > V_{th}$ and $V_{ds} > V_{Sat}$ the drain current I_d depends solely on the square of $V_{gs} - V_{th}$; I_d does not exhibit (at this level of description) a dependency on the drain-source voltage V_{ds} (i. e. the drain terminal acts as a current source).



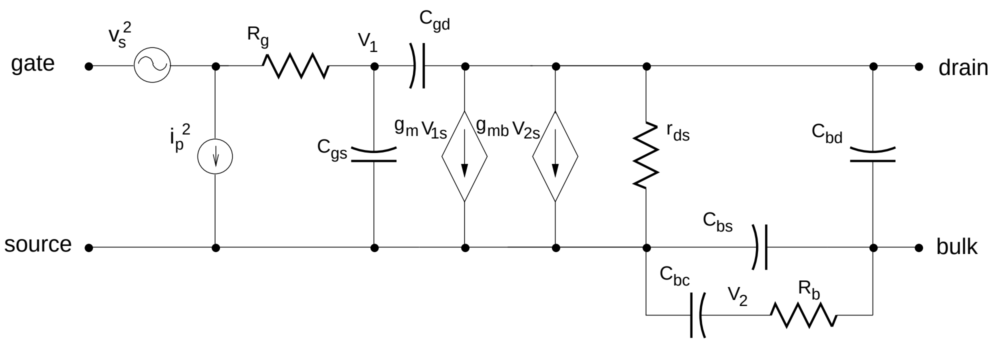


Figure B.2: MOS transistor small signal model; above: noise sources at their physical origin; bottom: equivalent input noise generators [CS91]

B.1.3 Small Signal Model

After the DC (large signal) condition of a MOS transistor in a given circuit has been determined, further analysis is carried out using the small signal model which is valid for a limited range of voltages.

Fig. B.2 shows ths small signal model of the MOS transistor [CS91]. Bluntly speaking, the MOS transisor can be characterized as a *voltage controlled current source* of transconductance $g_m = i_d/v_{gs}$ (note the small signal notation), where the gate terminal serves as the main controlling terminal. Besides the gate the bulk node has also impact on the transistor channel; the associated bulk source transconductance g_{mb} (which is roughly a factor of 10 smaller then g_m) lies in parallel. The output impedance r_{ds} (as for current sources) lies in parallel to the current sources and describes the EARLY effect, i. e. the tansistor's deviation from an ideal current source. Capacitances can be infered from the physical location of the terminals; one distinguishes bulk junction capacitances (between bulk and source/drain) which are usually depending on the operation condition and geometric overlap capacitances (like all gate-related capacitances); for a detailed description of the nature of capacitances the reader is referred to the literature [AH87]. The biggest capacitance encountered is the gate-oxide capacitance, 2/3 of which are usually attributed to the gate-source capacitance in saturation. The values of the elements used in the MOS small signal model B.2 are given in table B.1 together with a definition.

g_m	$\frac{\partial I_d}{\partial V_{gs}}$	$\approx \sqrt{2\mu_0 C_{ox} \frac{W}{L} I_d}$
		$\approx 2\mu_0 C_{ox} \frac{W}{L}(V_{gs} - V_{th})$
r_{ds}	$\frac{\partial I_d}{\partial V_{ds}}$	$\approx \frac{1}{\lambda I_d}$
i^2_{ch}	indep.	$\frac{8kTg_m(1+\eta)}{3}$
$i^2_{1/f}$	indep.	$\frac{K_F I_d}{\nu C_{ox} L^2}$

Table B.1: Small signal model parameters of MOS transistor (cf. fig. B.2); r_{ds} small signal drain resistance, λ channel lenght modulation parameter, η ratio of bulk-transconductance g_{mb} to gate-transconductance g_m, K_F flicker-noise coefficient; the capacitor values are more complicated and can be looked up [AH87, p. 105 ff.].

The main MOS noise sources are the (white) channel thermal noise which arises from the channel resistance according to Nyquist, and the 1/f noise whith a 1/f-frequency behaviour. Of minor importance are the gate and the bulk resistance noise which can be kept small by proper layout. An implication of the (physically) motivated noise model in fig. B.2 is that the noise current observed at the transistor drain does not depend on the impedances seen at the transistor input (with exception of the gate resistance noise); in particular "AC-shorting" and "AC-opening" the input (when the transistor stays in saturation) does not cause any change in the output noise current.

In general, the noise performance of every two port network can be represented by two equivalent input noise generators v_s^2 and i_p^2 which are located in series resp. in parallel of the network, which is then assumed to be noiseless [CS91, Zwi87]. This interpretation is valid for any source impedance provided that the correlation between both noise generators is taken into account. With MOS transistors the input noise current i_p^2 is often neglected in literature which is a good approximation for low frequencies and low input impedances; for higher frequencies as well as higher input impedances (both applies for typical high energy physics applications) this assumption is not valid.

The MOS transistor representation using input noise generators is depicted at the bottom of fig. B.2 [CS91]. The four independent noise sources from the upper schematic of fig. B.2 are now represented by the two equivalent input noise generators v_s^2 and i_p^2. The input noise sources can be determined as follows: First, input and output are shorted for either small signal model in fig. B.2; the total output current noise is equated to obtain v_p^2. Secondly, both circuit inputs are opened, the output is shorted, and the total output current noise is equated to obtain i_p^2. The input noise generators found from this

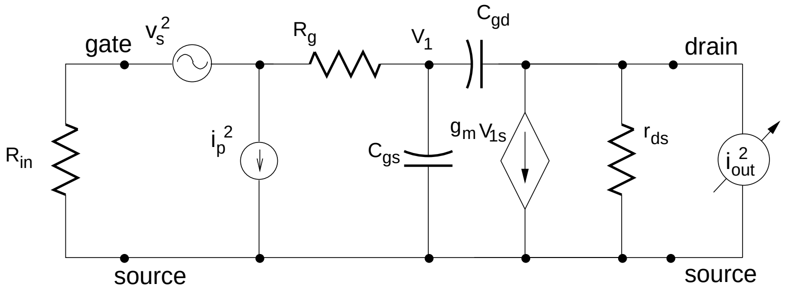


Figure B.3: calculation of output current noise with a finite source impedance using the MOS transistor small signal model of fig. B.2; the bulk capacitances do not enter into the transfer function since drain and source are shorted. The gate resistance R_g is neglected.

procedure equal

$$
\begin{aligned}
v_s^2 &= \frac{i_{ch}^2 + i_{1/f}^2 + i_{br}^2}{|g_m|^2} + 4kTR_g \\
i_p^2 &= |j\omega(C_{gs} + C_{gd})|^2 \frac{i_{ch}^2 + i_{1/f}^2 + i_{br}^2}{|g_m|^2}
\end{aligned}
\tag{B.2}
$$

where the noise sources are quantitatively given in table B.1. Since the input equivalent noise generators depend on the same set of noise sources disregarding the (usually neglectable) gate resistance noise they are perfectly correlated which has to be taken into account when considering the noise behaviour of a general case.

From the top schematic in fig. B.2 follows that the drain current noise does not depend on the input impedance (neglecting R_g). To prove this statement we calculate the total output current noise for an input impedance R_{in} between the two extremes of 0 resp. ∞ Ω (fig. B.3) using the input eqivalent noise sources from the bottom schematic of fig. B.2.

This yields

$$
i_{out}^2 = \left(\frac{g_m}{1 + \omega(C_{gs} + C_{gd})R_{in}} v_s + \frac{g_m R_{in}}{1 + \omega(C_{gs} + C_{gd})R_{in}} i_p \right)^2 \quad . \tag{B.3}
$$

R_{in} denotes the input impedance (assumed to be noiseless).

Since (neglecting the gate resistance noise) the parallel current and the serial voltage noise generators are related by

$$
v_s = \frac{1}{|j\omega|(C_{gs} + C_{gd})} i_p \tag{B.4}
$$

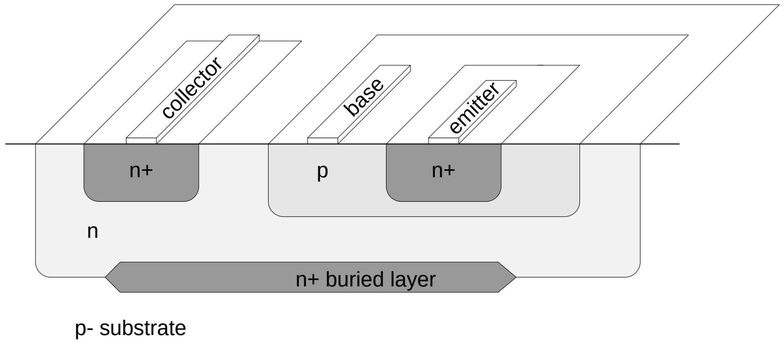


Figure B.4: Physical structure of a vertical bipolar transistor [San94]

the total noise is given by

$$i_{out}^2 = g_m^2 v_s^2 \tag{B.5}$$

which is independent from the input impedance seen. Thus, our model describes well the physical reality.

B.2 Bipolar Transistor

Bipolar transistors are famous for their good noise behaviour. This reputation stems from their lower flicker-noise w. r. t. MOS transistors and from the lower serial noise obtainable due to their higher transconductance; in voltage amplifiers with low-ohmic sources parallel noise plays a minor role (cf. eq. (4.10)). In high-ohmic sources and at frequencies above the flicker noise, however, MOS transistors take over.

Since in chapt. 7 we compare the noise behaviour of a charge amplifier with MOS resp. bipolar input transistor, we want to give a short introduction into the bipolar transistor physics. It shall be remarked that certain bipolar transistors are also available in typical CMOS processes (but they suffer from certain limitations).

B.2.1 Basics

Bipolar transistors have lost their leading role in microelectronic circuits to MOS transistors; MOS transistors can provide higher density and allow low-power logic, but bipolar transistors can operate at higher frequencies and provide less noise than MOS transistors at low frequencies.

Fig. B.4 shows a cross section through a vertical bipolar npn transistor [San94]. The collector current in such a transistor flows from the buried layer at the bottom over the base to the emitter in vertical direction. The collector consists of an n^+-buried layer which is an n-epitaxial layer of constant doping level, and an n^+-contact at the surface. The base has a very small width (typically 0.5 to 0.8 μm); its doping concentration is medium. The emitter forms the uppermost layer and consists of a heavily doped n^+-layer of several μm width. Thus, the bipolar transistor can be imagined to consist of 2 pn-junctions of reversed polarities in series.

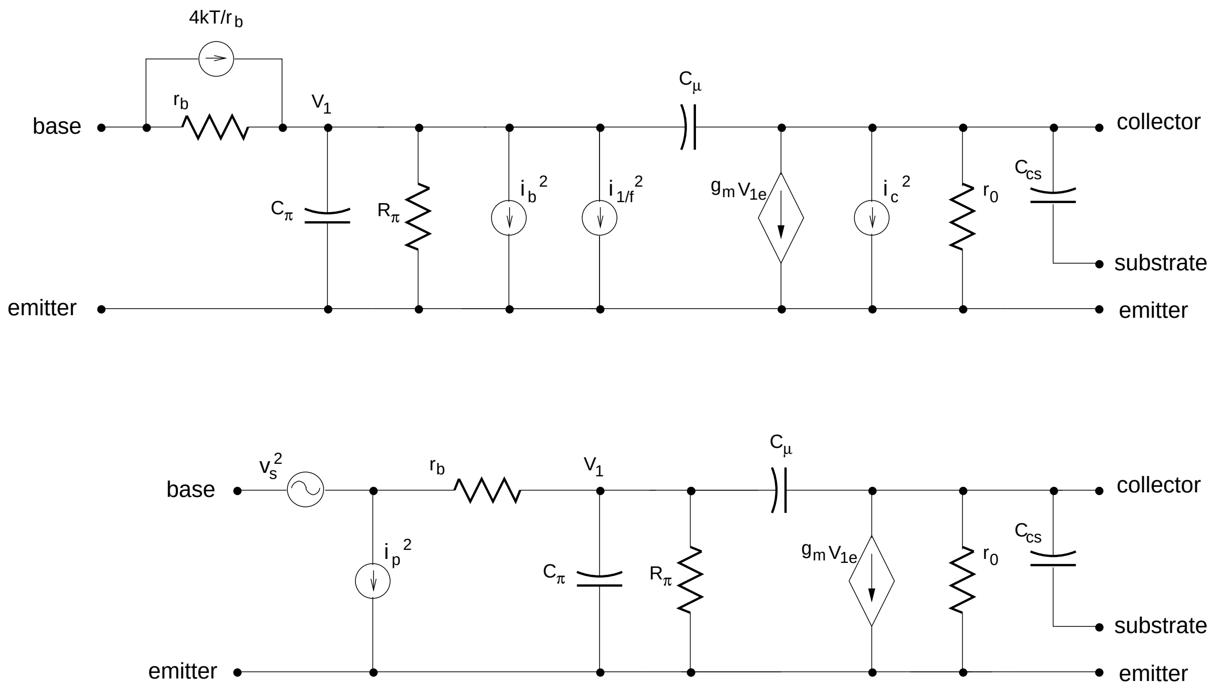


Figure B.5: Bipolar transistor small signal model; top: noise sources at their physical origin; bottom: equivalent input noise generators [CS91]

Electrons in the emitter in the first pn-junction diffuse through the very narrow base region to the base-collector junction. Only few electrons are lost in the base due to recombination. At the base-collector junction the electrons are swept to the collector by the electrical field. This collector current can be controlled by the emitter-base-voltage. Thus, in contrast to the MOS transistor transistor where the drain current I_d is dominated by drift due to an electrical field in the channel, the collector current is mainly determined by diffusion.

B.2.2 Large Signal Model

The collector current is given by [San94, p. 98]

$$I_c = I_s \exp\left(\frac{V_{be}}{kT/q}\right) \quad . \tag{B.6}$$

V_{be} base-emitter voltage

$k = 1.38 \cdot 10^{23}$J/K, T absolute temperature

q=1.6$\cdot$10^{-19} C, electron charge

$I_s = A_e j_s$ saturation current

A_e emitter area

j_s saturation current density

B.2.3 Small Signal Model

The hybrid-π small signal model of the bipolar transistor is shown in fig. B.5. Its parameters are given in table B.2. Differently from the MOS transistor the input impedance of the bipolar transistor is quite low (typical values are $r_\pi \approx$ n$\cdot$ 10 kΩ). Also differently from the MOS case, the transconductance g_m is proportional to the collector current (as compared to the square root behaviour of the MOS transistor). The current gain β_{AC} for typical dotations $\approx$ 100; as a rule of thumb the value of kT/q is 26mV at room temperature. The output impedance r_0 due to the EARLY effect is inversely proportional to the collector current flowing

g_m	$\frac{\partial I_c}{\partial V_{be}}$	$\frac{I_c}{kT/q}$
r_π	$\frac{\partial V_{be}}{\partial I_b}\|_{r_b=0}$	$\frac{\beta_{AC}}{g_m}$
β_{AC}	$\frac{\partial I_c}{\partial I_b}$	
r_0	$\frac{\partial I_c}{\partial V_{ce}}$	$\frac{V_E}{I_c}$
i_b^2	indep.	$2qI_b$
$i_{1/f}^2$	indep.	$\frac{K_f I_b}{A_e \nu}$
i_c^2	indep.	$2qI_c$

Table B.2: Small signal model parameters of bipolar transistor (cf. fig. B.5); I_c collector current, I_b base current, r_π small signal base-emitter resistance (without base contact resistance), r_b base contact resistance, β_{AC} AC-current amplification, r_0 small signal collector resistance, K_f flicker noise coefficient, q electron charge, A_e emitter area; the capacitance values are more complicated and can be looked up e. g. in [San94, p. 120 ff].

The noise sources are due to different physical noise sources. As an ohmic resistance the base resistance r_b exhibits thermal noise; r_b is given by the sum of the intrinsic and extrinsic base resistances; the first denotes the resistance of the lightly doped base region underneath the emitter, whereas the latter gives the resistance from the base contact to said region. Since the bipolar transistor consists of two pn-junctions, both base current and collector current suffer from shot noise (i_b^2 resp. i_c^2). 1/f-noise is also present in the bipolar transistor (although the corner frequency lies considerably below the one of the MOS transistor); it is usually modelled as current source in parallel to the base current.

The input noise generators can be determined by analogy to the MOS transistor case and are given by [CS91]

$$\begin{aligned} v_s^2 &= (i_b^2 + i_{1/f}^2) r_b^2 + 4kT(r_b + \frac{1/2}{g_m}) \\ i_p^2 &= i_b^2 + i_{1/f}^2 + \frac{i_c^2}{|\beta_{AC}|^2}\left|1 + j\frac{\omega}{\omega_\beta}\right|^2 \\ \omega_\beta &= \frac{1}{r_\pi(C_\pi + C_\mu)} \end{aligned} \tag{B.7}$$

In these equations, it has been assumed that $r_\pi \gg r_b$ and $\omega < 1/(r_b(C_\pi + C_\mu)$.

The term $4kT(\frac{1/2}{g_m})$ in v_s^2 is due to the collector shot noise i_c^2; thus i_c^2 appears in both input noise generators; the same holds true for $i_b^2 + i_{1/f}^2$ and thus correlation effects between v_s^2 and i_p^2 have to be considered. A more thorough consideration ([CS91]) shows that for very low frequencies where the 1/f-noise dominates and for very high frequencies $\omega > 1/(r_b(C_\pi + C_\mu))$ the correlation reaches unity. For medium frequencies following a widely accepted approximation ([CS91]) the correlation will be neglected which results in dramatic simplification of the noise calculation in chapt. 7.2.2.

For frequencies below ω_β eqs. (B.7) simplify to

$$\begin{aligned} v_s^2 &= 4kT(r_b + \frac{1/2}{g_m})\Delta\nu \\ i_p^2 &= i_b^2 + \frac{i_c^2}{|\beta_{AC}|^2} \end{aligned} \tag{B.8}$$

where we also dropped the noise voltage created at r_b and the 1/f base current noise. It has to be stated that the assumption $\omega < \omega_\beta$ is not strictly fulfilled in the treatment of chapt. 7.2.2; however, since the i_c^2-term is much smaller than i_b^2, the error made is small.

Appendix C

HELIX128S-2.x-Genealogy

C.1 HELIX128S-2

The analog signal path of HELIX128S-2 has been extensively described in chapt. 8. Being the first chip of a new generation, HELIX128S-2 suffers from a number of errors and limitations; a list of known problems is given in the manual (appendix D). In the following we address the problems arising from the analog part.

HELIX128S-2 suffers from a limitation in dynamic range due to the fact that the offset voltage at the pipline amplifier output is wrong. The reason is (cf. also fig. 8.26) that the charge equilibrium obtained by reading out a pipeline cell has been chosen differently from the reset voltage level Vd. Thus, at every read and reset cycle the voltage on the read-line and – correspondingly – the pipeline amplifier output undergoes large transitions. Since this happens for all channels in parallel, the *pipe_bias* and *pipe_bias2* lines (fig. 8.31) are pulsed via 129 $\times$ the gate-drain capacitances of transistors M3 and M4, respectively. Thus, an additional negative feedback is introduced which inhibits the rise of the amplifier output in the given time window. By attributing more time for both the reset- and the read-cycle (fig. 8.28) this problem can successfully be tackled; this is, however, not a viable solution for the experiment.

The comparator circuit has been found to produce significant crosstalk when operating on Helix128-2; the crosstalk arises from feedback via the power supply lines and via the open-collector discriminator outputs at the chip's bottom side to the amplifier inputs.

C.2 HELIX128S-2.1

HELIX128S-2.1 has emerged from HELIX128S-2 by a metal/poly mask redesign and differs basically in the digital circuitry. In the analog circuitry, two properties have been changed w. r. t. HELIX128S-2: first, the voltage levels encoding the pipeline column number in the readout have been changed to more favorable values; secondly, the voltage resolution of the comparator threshold has been improved by a factor of 10.

HELIX128S-2.1 is the first chip of the HELIX-family which will be used in greater scale at the HERA-B experiment. Despite of its functionality on principle some problems remain which could be overcome by the successor HELIX128S-2.2.

C.3 HELIX128S-2.2

To dispose of the voltage transitions around the pipeline readout amplifier, a voltage level shifter circuit similar to the one employed in the preamplifier and shaper circuits has been designed (fig. C.1).

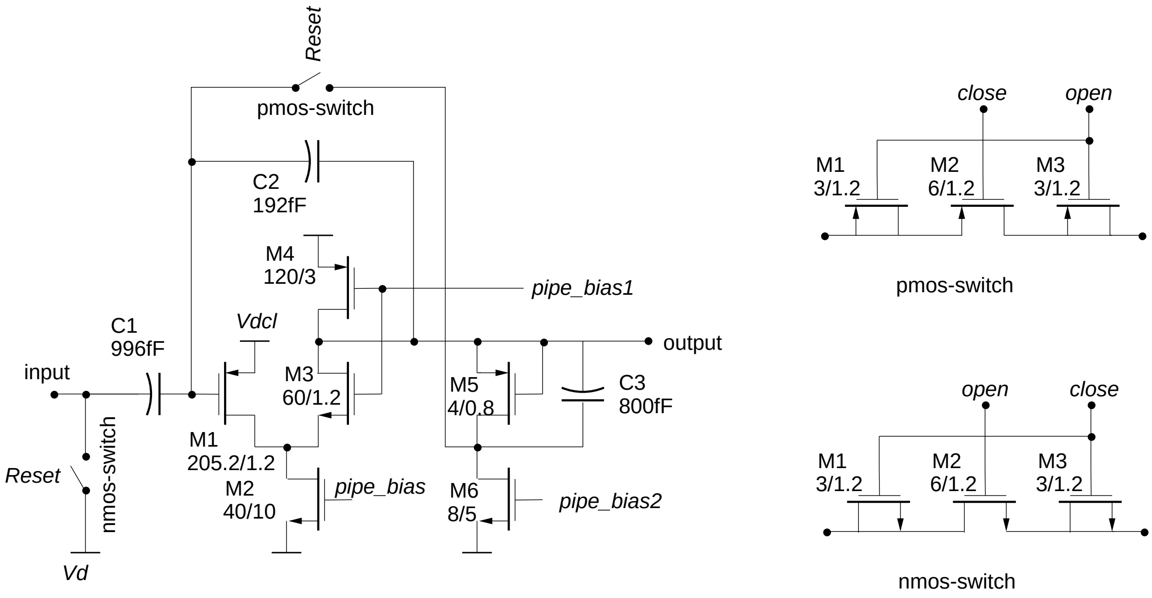


Figure C.1: Schematic of pipeline readout amplifier of HELIX128S-2.2; in analogy to the preamplifier and shaper a level shifter provides a different offset removing the level transitions in the absence of a signal. The feed-forward capacitor C3 has been added to minimize the additional phase shift by the level shift network.

During reset the pipeamp input is shorted to the drain of the diode-connected transistor M5, which lies approx. 1 V below the pipeamp output voltage and hence close to the gate-voltage of M1 for properly chosen *Vdcl*. Thus, no voltage transition takes place due to the reset-operation. At the end of the reset, the feedback capacitance C_{fb} is precharged to the correct (w. r. t. the following stages) output offset voltage. The folded cascode and the gain-determining capacitances C_{fb} and C_c have remained unchanged.

A point of concern is the susceptibility of the current buffer signals to digital interference (cf. sect. 8.9). To tackle this problem, LVDS-pads [Klu98] (low voltage differential signals) with 350 mV differential voltage-swing have been implemented on HELIX128S-2.2. Also, the gain of the current signals has been increased by a factor of 5. The schematic of the modified currentbuffer is plotted in fig. C.2. Transistor M8's width has been increased by a factor of 5 w. r. t. the HELIX128S-2-version. Since its gate-source capacitance increases accordingly, the drain-capacitance of M7 has been halved admitting a twice as big EARLY-effect; the associated deterioration of linearity due to signal current loss through M7 is negligible. Thus, capacitance C_1 (fig. 8.37) increases only by approx. 50 % indicating a rise time of 9 ns.

Both measures – lower swing digital signals and larger current signals – improve the signal-to-interference ratio of HELIX128S-2.2. The figure-of merit w. r. t. the first-generation Helix128 using a voltage output (chapter 8.9) has increased to 0.5. By use

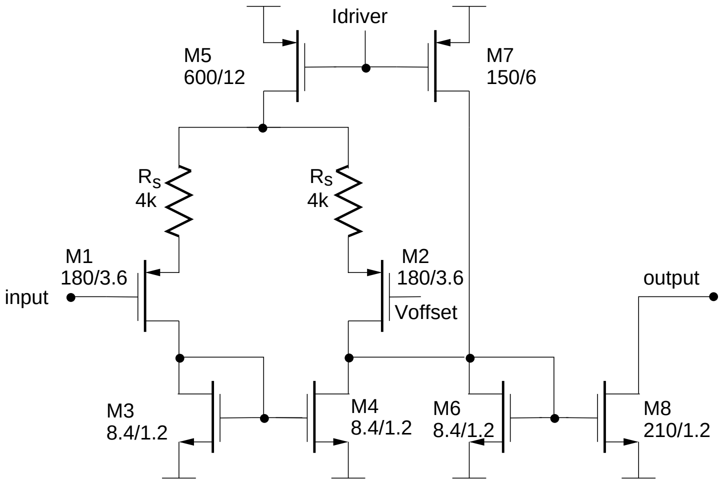


Figure C.2: Schematic of current buffer of HELIX128S-2.2/2.3

of a true differential output (i. e. `AnalogOutDummy` would have to be replaced by an inversed copy of `AnalogOut`) this figure could be made 1.

The comparator power and signal routing has been improved: Separate pads have been added for the power supply of the 32 open-drain comparator output pads. Power pads for the internal comparator-circuit have been implemented on both the upper and the lower side of the chip; the ground used in the AC-coupling has been separated from the preamplifier ground. The `CompClck` makes use of LVDS-levels.

In the SUFIX-part the voltage DACs have been redesigned for lower space consumption (R-2R ladder-DACs).

C.4 HELIX128S-2.3

HELIX128S-2.3 is a derivation of HELIX128S-2.2 with another pipeline readout amplifier (fig. C.3); it was immediately submitted after HELIX128S-2.2. The HELIX128S-2.2-pipeamp re-employs the old (and successful) design used inside Helix128 with certain modifications to adapt it to the new environment. The folded cascode has been mirrored w. r. t. the circuit employed on HELIX128S-2, i. e. nmos-transistors have been replaced by pmos-transistors and vice versa. The offset voltage at the folded cascode's output is quite low and has to be shifted up by a subsequent source follower which also supplies the slewing current. As an advantage of this circuit the phase-margin in the reset-phase is not deteriorated by an extra delay in the level-shifting network, which is located *outside* the feedback-loop. This advantage, however, is compensated by the larger value of the coupling capacitance C_c (14.6 pF !). This can be understood as follows: The feedback transfer function $H(s)$ has a low-pass characteristic in the reset-phase characterized by the phase degradation

$$\tan \phi = -\omega R_{on} C_c \tag{C.1}$$

where R_{on} is the on-resistance of the reset switch. Due to the larger value of the coupling capacitor a bigger negative phase-shift ϕ is introduced by $H(s)$ (maximally 90 °). A discussion of C_c's impact on the pipeline capacitance variations has been given in chapt. 8.7. The feedback capacitance C_{fb} has been chosen to fulfill the gain requirement.

Nonlinearites of the source-follower are not equalized by feedback in this circuit.

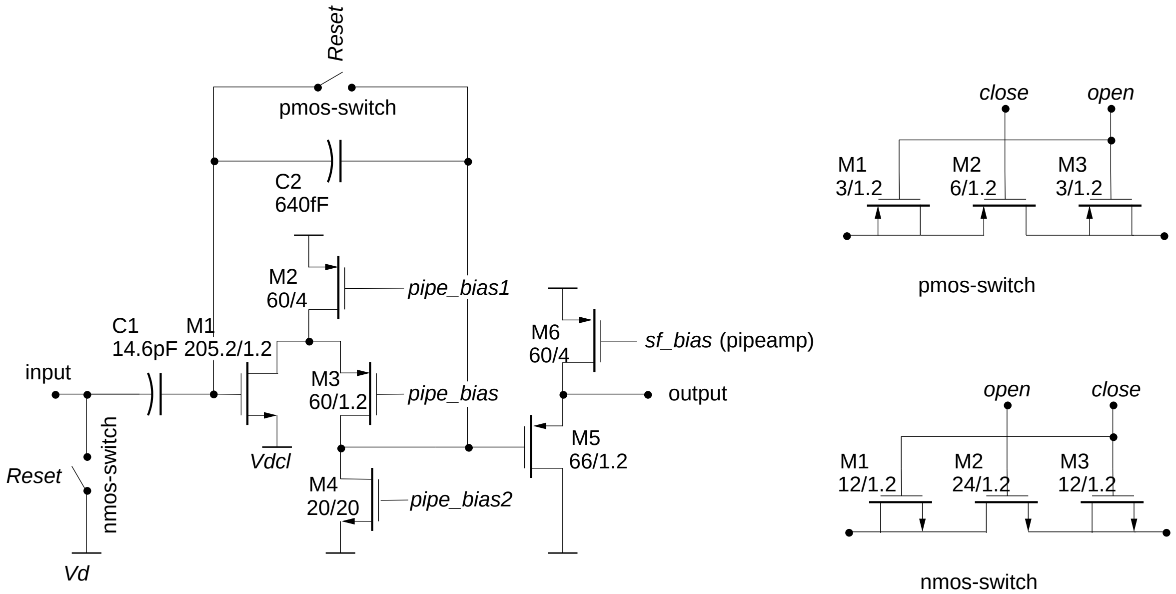


Figure C.3: Schematic of pipeline readout amplifier of HELIX128S-2.3; the folded cascode is mirrored w. r. t. the previous versions. The capacitance values have been increased, and a source follower serves as level shifting stage.

Appendix D

Helix128-2.x[1] User Manual

27.04.1998, Proprietary version [2]

Wolfgang Fallot-Burghardt, Edgar Sexauer, Ulrich Trunk
Max-Planck-Institut für Kernphysik, Heidelberg
Martin Feuerstack-Raible, Boris Glass
Physikalisches Institut der Universität Heidelberg, Heidelberg
Ruud Kluit
NIKHEF, Amsterdam

[1] identical to "HELIX128S-2.x"

[2] The up-to-date version can be obtained from M. Feuerstack-Raible, feuersta@asic.uni-heidelberg.de

Abstract

Helix128-2 and its variants 2.1, 2.2, and 2.3 are analog readout chips for silicon microstrip detectors and microstrip gaseous chambers manufactured in the 0.8μm-CMOS process of AMS. The chips integrate 128 channels with low noise charge sensitive preamplifier/shapers whose outputs are sampled into an analog pipeline with a maximum latency of 128 sampling intervals. A pipeline readout amplifier, a fast 40MHz multiplexer and a 40MHz current buffer form the backend stages of the designs. Additionally, each channel is equipped with an AC-coupled comparator behind the preamplifier/shaper. All comparators share a common threshold, the output of four neighbouring comparators being ORed and brought offchip.

The bias settings and various other parameters are programmable via a serial line protocol. The chips provide monitoring functionality and the ability to report error conditions.

Contents

List of Tables

D.1 Important note

This manual describes different versions of the second generation of the Helix readout-chip; the chips developed so far differ in some details, especially concerning pad layout and electrical specification of some control signals. The Helix128-2 (sometimes also called Helix128-2.0) chip is the first in this line; Helix128-2.1 emerged from it by a metal/poly mask redesign.

Helix128-2.2 is an improved version making use of a modified pipeline readout amplifier; it is equipped with LVDS line receivers for some control lines and with a pad layout that will make it compatible with a fail safe token scheme which will be implemented in future. Finally, Helix128-2.3 is a modification of Helix128-2.2 with yet another pipeline readout amplifier.

The name Helix128-2 is used throughout this manual when describing features that are common to all versions of the chip.

D.2 Analog Signal Processing Architecture

Helix128-2 is an analog readout chip for silicon microstrip detectors and microstrip gaseous chambers specially suited to the needs of the HERA-B experiment [1]. Major electrical specifications are a 10MHz sampling clock frequency (i. e. the bunch crossing frequency) implying a shaper peaking time in the 50 ns regime, a storage time depth of about 10μs to comply with the first level trigger latency, the ability to store up to eight events to equalize statistical trigger fluctuations and the complete deadtimeless readout of the detectors in 10μs due to the mean second level trigger rate of 100kHz. Further demands are lowest possible total system noise and a moderate radiation tolerance of $\leq$2kGy.

To cope with the tremendous amount of detector channels 128 channels are integrated per chip with 41.4μm pitch of input pads as imposed by the silicon strip detector pitch.

D.2.1 Overview

Helix128-2 contains 128 channels (see fig. D.1), each consisting of

- a low noise charge sensitive preamplifier for signals of both polarities. It is implemented as a folded cascode amplifier circuit with a 342 fF feedback capacitor yielding a gain of 11.2 mV/$\mathrm{MIP_{Si}}$ (1 $\mathrm{MIP_{Si}}$=24000 electrons).
- a CR-RC shaper forming a semigaussian pulse with a peak time of 50... 70ns.
- a buffer amplifier driving the internal pipeline write line and the pipeline cell.
- a comparator circuit indicating hit channels, the output of four neighbouring channels being ORed and brought offchip via open drain outputs.
- an analog pipeline consisting of 128+8+5 capacitors resulting in a maximum latency of 128 events and a multievent buffer capable of storing up to eight triggered events (time slots)
- a switched charge sensitive pipeline readout amplifier.

A cascaded 128+8+1 channel multiplexer and a current output buffer are provided for the fast serial readout of the analog data and the 8 bit pipeline column number.

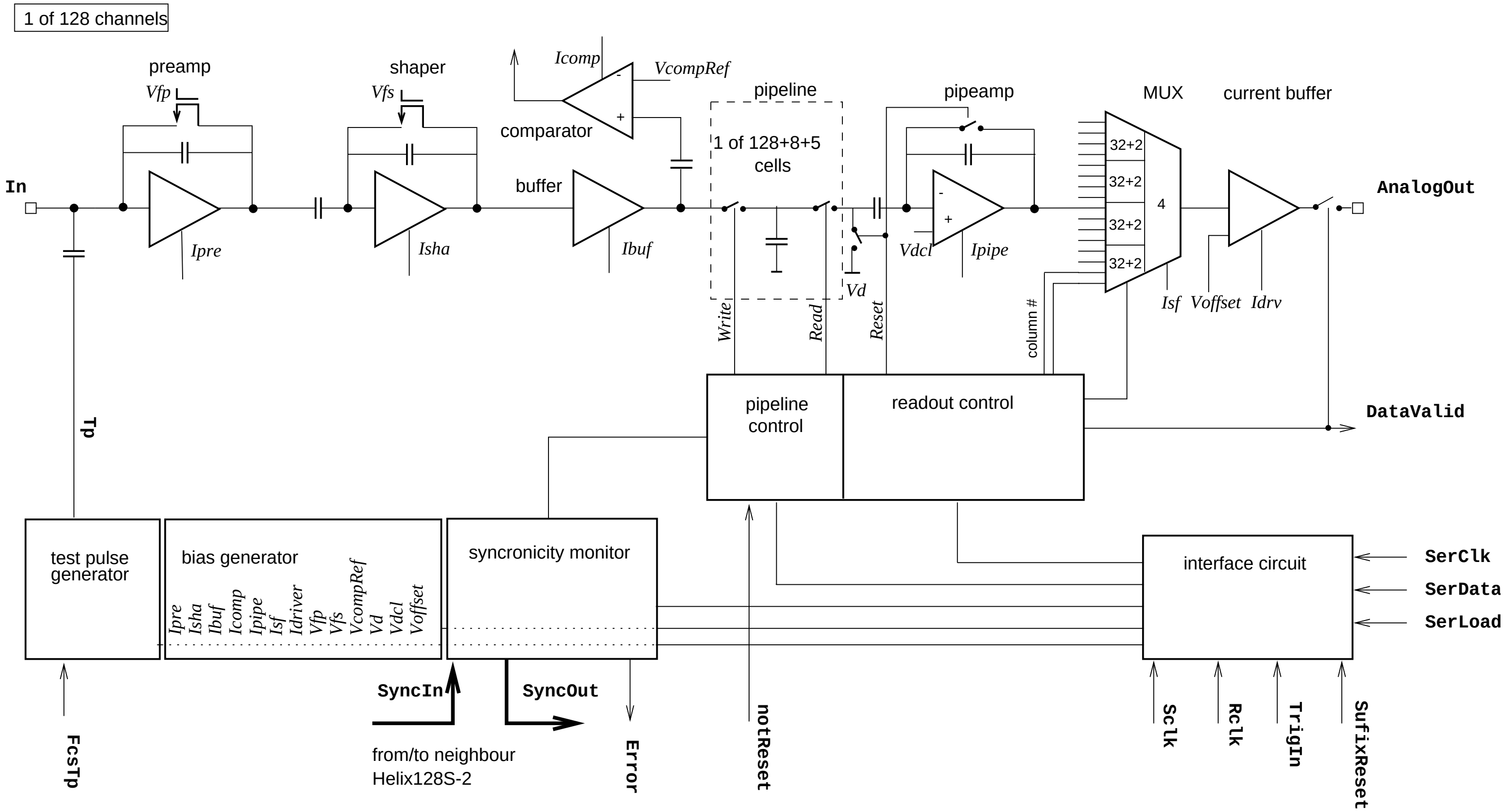


Figure D.1: Schematic diagram of Helix128-2

The operation points of all Helix128-2 amplifier stages can be adjusted via programming of corresponding DAC registers. We will outline radiation compensation strategies which ensure proper operation up to the demanded dose of HERA-B. Further explanation of the suggested strategies can be found in [4] and [5].

D.2.2 The frontend (Helix2.1)

Helix128-2 uses the Helix2.1 frontend (fig. D.2) which has been carefully optimized with respect to noise, pulse shape (peak time and undershoot), linearity, space and power consumption. More detailed descriptions can be found in [2] and [3].

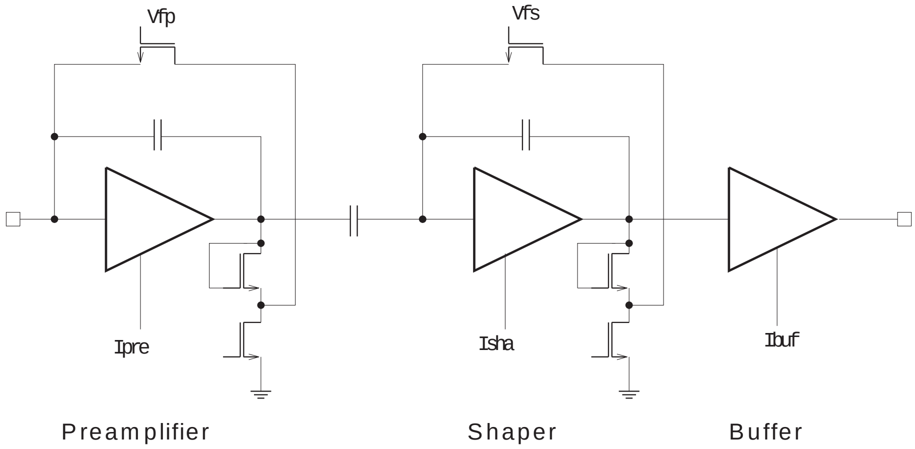


Figure D.2: Helix2.1 frontend

To set the frontend operation mode and to compensate for radiation damage the frontend bias voltages and currents (not to be confused with the power supplies +2V,0V,−2V) may be adjusted via programming of the corresponding DAC registers as explained in section D.3. The nominal values are listed in table D.1.

- *Ipre* sets the preamplifier bias current. With *Ipre* being above a threshold of $\approx 100\mu$A no impact on the peak time is observed [6]. A higher *Ipre* current reduces noise, so that a noise degradation of the preamplifier due to decrease of the g_m of the input transistor can be cured by increasing this current (at the cost of power consumption).

- *Isha* sets the shaper bias current. *Isha* influences the shaper core cell "load resistor" leading to a smaller undershoot for higher currents. Also, the peak-time decreases (see fig. D.3) with rising *Isha*. *Isha* should be kept constant under irradiation (pulse degradation should be adjusted basically by *Vfs*).

- *Ibuf* sets the buffer bias current. It hould be kept constant. If the buffer becomes too slow by a decrease of g_m (this can be observed e. g. by changing pulse heights at different `Sclk` frequencies), *Ibuf* can be increased.

- *Vfp* controls the value of the preamplifier feedback resistance. It should be as low as possible for optimum noise performance. *Vfp* should be decreased

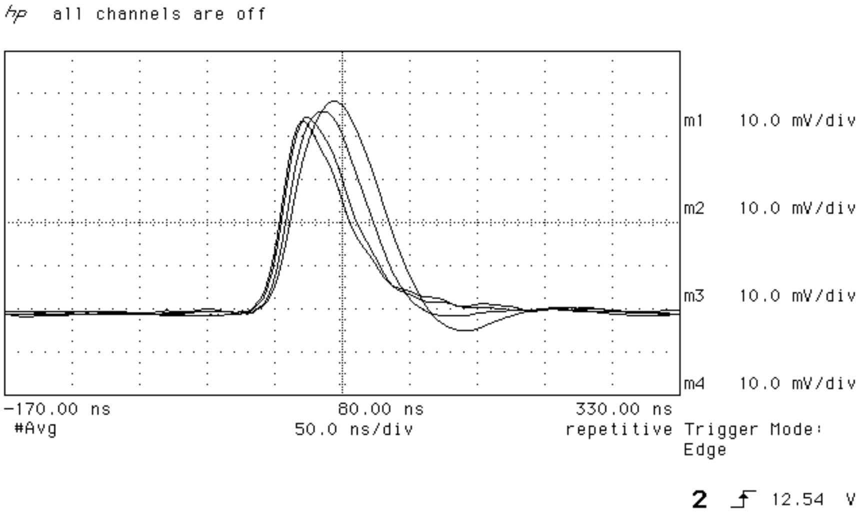


Figure D.3: Impact of *Isha* on pulse shape: from slowest to fastest pulse: *Isha*=60μA,100μA,200μA, and 300μA

continously during irradiation, so that the preamplifier operates slighly above the *Vfp* cutoff edge (for DC coupled detectors this value can be quite large).

- *Vfs* controls the value of the shaper feedback resistance and thus determines the discharge of the shaper feedback capacitor (see fig. D.4). *Vfs* should be decreased *continously* during irradiation, so that the peak time remains constant.

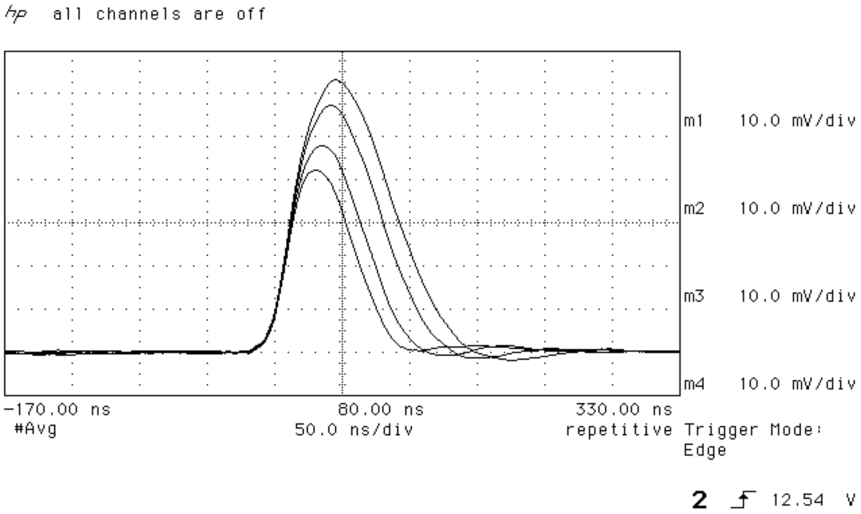


Figure D.4: Impact of *Vfs* on pulse shape: from outside to inside *Vfs*=0.8V,1V,1.5V, and 2V

Name	Nominal value and dec. reg. cont.	Irradiation compensation
Ipre	200μA=80	$\Rightarrow\Uparrow$
Isha	100μA=40	$\Rightarrow$
Ibuf	100μA=40	$\Rightarrow\Uparrow$
Icomp	50μA=20	$\Rightarrow\Uparrow$
Ipipe (Helix128-2.0...2.2)	50..100μA=20..40	$\Rightarrow$
Ipipe (Helix128-2.3)	20μA=8	$\Rightarrow$
Isf	100μA=40	$\Rightarrow\Uparrow$
Idriver	90μA=36	$\Rightarrow$
Vfp	0.2V=71	$\Downarrow$
Vfs	1.5V=113	$\Downarrow$
VcompRef	$\pm$20mV=71	$\Rightarrow$
Vdcl (Helix128-2.0...2.2)	1V=97	$\Rightarrow$
Vdcl (Helix128-2.3)	$-$1.1V=97	$\Rightarrow$
Vd (Helix128-2.0,2.1)	0V=65	$\Downarrow$
Vd (Helix128-2.2,2.3)	$-$840mV=65	$\Downarrow$
Voffset	$-$0.3V=55	$\Rightarrow\Uparrow$

Table D.1: Nominal values of analog bias voltages and currents and suggested radiation compensation strategies; $\Rightarrow$ indicates no change, $\Downarrow$/$\Uparrow$ suggests negative/positive adjusting of the corresponding bias. Since the LSB of the 8bit wide voltage value registers is ignored the corresponding values must be multiplied by 2.

D.2.3 The comparator

The comparator (fig. D.5) with programmable signal polarity is located behind the frontend to detect hit channels. To supress frontend pedestal fluctuations the comparator has been AC-coupled with a large time constant. The output of four neighbouring channels is ORed, latched on the positive edge of `CompClk` and brought offchip as open drain signals `notCompOut`$\langle$`31...0`$\rangle$ which can drive 4mA at maximum [3].

In case of radiation damage the following strategy is recommended:

- *VcompRef* controls the comparator threshold level (1 $\mathrm{MIP_{Si}} \approx$ 50mV peak height, so a value of 20mV is a good start to detect MIP signals[4]); due to the AC-coupling this level is independent from radiation induced frontend baseline shifts and so it should not be altered.
- *Icomp* sets the comparator bias current. It can be increased slightly under irradiation (however, no strong effects expected)

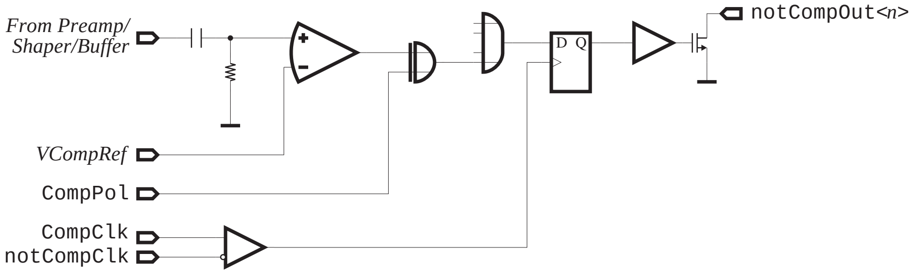


Figure D.5: AC-coupled comparator

D.2.4 The pipeline

The frontend outputs are stored in a sample&hold capacitor array of $129 \times (128 + 8 + 5)$ cells. Each cell capacitor (850 fF) is connected by a *read* switch to the *read line* (frontend output), and by a *write* switch to the *write line* leading to the pipeline readout amplifier ("pipeamp") (fig. D.1). The switches are controlled by the pipeline logic which is explained in more detail in section D.3.1.

The charge stored per $\mathrm{MIP_{Si}}$ is $\approx$ 260.000 electrons implying a charge gain of 11, so that the noise requirements on the pipeamp are relatively relaxed.

D.2.5 The pipeline readout amplifier ("pipeamp")

The pipeline readout amplifier is a switched charge sensitive amplifier (fig. D.6). Before operation the internal reset signal is applied thus discharging the two capacitances (for clearness assume *Vdcl*= *Vd*). After the reset the pipeamp is sensitive

[3] This enables logically "OR"ing several comparator outputs by connecting them to a common drain resistor.

[4] cf. also appendix D.5

to the pipeline capacitor charge; since the node at the inverting input stays on constant potential, the charge transfer between the two capacitors causes a related voltage on the output when coupling charge to the input.

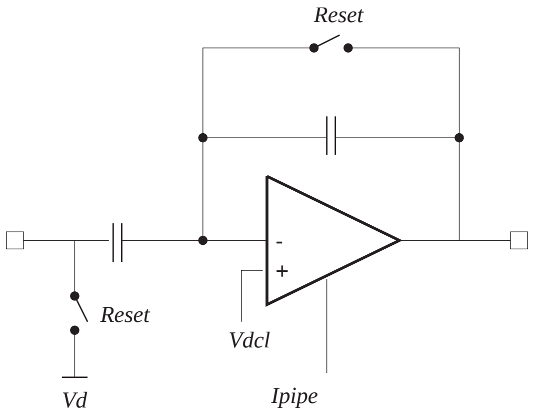


Figure D.6: Pipeline readout amplifier: a switched charge sensitive amplifier

The following strategy is recommended in case of radiation damage:

- *Vd* controls the reset level; it should follow the frontend baseline shift, i. e. it should be countinously diminished.
- *Vdcl* controls the folded cascode "ground" level; it should be adjusted after the *Vd* adjustment such that the channel output offsets equal aproximately the pipeline column number's mean value in the readout figure.
- *Ipipe* sets the pipeamp bias current. It should be kept constant.

D.2.6 The multiplexer

The multiplexer (fig. D.7) has been implemented using a cascaded architecture, i. e. in the first stage four 34 channel multiplexers operate at a fourth of the `Rclk` rate with a second stage at full `Rclk` speed. This approach would lead to a reordering of the channel numbers. Thus, to equalize this effect a permutation fan through has been implemented so that the channels arrive at the output in their geometrical order. The multiplexer first stage consists of a buffered sample&hold circuit with the drive strength controlled by *Isf*.

In case of radiation damage the following strategy is recommended:

- *Isf* should be kept constant; if the buffer becomes too slow by a decrease of g_m, (this can be observed e. g. by changing pulse heights at different `Rclk` frequencies) *Isf* can be increased.

As can be seen from fig. D.7 8 bits denominating the pipeline column the current event has been stored in are "weaven" into the multiplexer, appearing as trailer in the analog output (fig. D.9).

D.2.7 The current buffer

The current buffer is a differential voltage input/single current output ("transconductance") amplifier (fig. D.8) that converts the voltage signals delivered by the multiplexer. Linearity is achieved by a current feedback topology. The two multiplexer output voltages *AnalogOut* and *AnalogOutDummy* are amplified by two separate buffers sharing the common reference voltage *Voffset*. In case of radiation damage

- *Idriver* should be kept constant.
- *Voffset* should be adjusted so that the output offset current stays constant (probably the level must be raised).

Figure D.9 shows how the chip outputs its data after receiving a trigger. Synchronously to the falling edge of `RClk` data are asserted, indicated by `DataValid` going low. The current output signals `AnalogOut` and `AnalogOutDummy` are plotted as they can be observed at the chip output shorted to ground. The 128 amplifier channels are output channel 0 first, followed by channel 1 etc. up to channel 127. Analog data are followed immediately by an 8 bit trailer showing the pipeline column number the event has been stored in. This number is coded LSB first, a "1" bit coded as $\approx$+2 $\mathrm{MIP_{Si}}$, a "0" bit as $\approx$-2 $\mathrm{MIP_{Si}}$. `AnalogOutDummy` should be subtracted from `AnalogOut` to cancel offset, common mode and clock feed through.

D.2.8 The analog receiver circuit

The current signals delivered on `AnalogOut` and `AnalogOutDummy` should be received by a fast (bandwidth 100 MHz) transimpedance amplifier to make use of the full 40 MHz drive capability of the onchip current buffer and subtracted from each other to reduce common mode interference. The schematic depicted in fig. D.10 shows the suggested receiver circuit. The gain delivered at 1.5kΩ transimpedance is $\approx$ 85mV/$\mathrm{MIP_{Si}}$ (Helix128S-2/2.1) resp. 425mV/$\mathrm{MIP_{Si}}$ (Helix128S-2.2/2.3). The 50 Ω resistors at the inputs were chosen to terminate properly a 50 Ω cable. The Comlinear CLC 401 opamp features a high bandwidth and the ability to handle large voltage gains (voltage gain = 30 in the suggested configuration).

D.3 Digital Control Circuitry

In the predecessor version to the chip described, HELIX128 [7], the digital control circuitry necessary to operate according to the experimental requirements has been splitted between the HELIX128 itself and the support and control chip SUFIX [8]. In the present version, this separation was abandonned and all functions could be merged into Helix128-2.

D.3.1 The pipeline and readout control logic

The pipeline control logic (see fig. D.1) receives incoming triggers via the interface circuit and tags the corresponding columns of the capacitor storage array such that they are not overwritten by new data before they are read out.

A write pointer scans over the pipeline columns incremented by the sampling clock *Sclk* which can be either internally generated from the `Rclk` or taken from the `Sclk` pad (refer to section D.3.4). After `notReset` is set to +2 V, the pointer starts its walk at column 0, the one nearest to the frontend, wrapping around at column number 140 = 128 + 8 + 5 - 1. Sampling the output of the preamplifier/shaper to the storage capacitor is enabled during the high period of `Sclk`, the falling edge determining the held frontend output value.[5]

With the latency specified by the content of the *Latency* register the trigger pointer follows the write pointer. When a trigger occurs (indicated by a high `TrigIn` signal at the rising edge of `Sclk`, see fig. D.11), the column number which is currently pointed at by the trigger pointer is stored into a FIFO and marked to be read out. The FIFO has a storage capacity of eight numbers.

The “oldest” number within the FIFO is loaded into the read pointer which adresses the column of the storage capacitor array to be loaded into the readout multiplexer. Loading the multiplexer is a multi-stage process: it takes 2 *Sclk* cycles to reset the readout line and the pipeamp, followed by 1 *Sclk* cycle break and another 2 *Sclk* cycles to read the data with the pipeamp until its output is stored by the readout multiplexer. After this period the multiplexer is ready to transmit data.

The condition for the multiplexer to start transmission once it has loaded data is given by a high `TransmitEnable`, a high `MultiplexerEnable` and the presence of a token (as explained in section D.3.6).

After transmission of data the chip immediately starts loading data from the next tagged column into the multiplexer. In parallel, the chip watches its `ReturnTokenIn` line. When this is high during a falling edge of `Rclk`, the previous pipeline column is untagged thus being available for writing again. Thus, since all chips in a daisy chain share the *ReturnToken* line, the synchronicity of pipeline operation is maintained even in daisy chain operation.

[5] Since the risetime of the preamplifier/shaper is about 50ns, the high period of the external `Sclk` should be of the same value.

D.3.2 The bias current sources

The various bias currents of the analog stages described in section 1 are generated by 8 bit digital to analog converters which are controlled by registers of the same name. The conversion slope of the DACs is 2.5μA/LSB with a register value of 0 corresponding to zero output current. To achieve correct operation of the bias generator circuit, a reference current of 100μA must be flowing into the `IrefIn` pad which can be generated either by an external source or by using the internal reference current generator. When using the latter, `IrefOut` has to be bonded directly to `IrefIn` and a resistor of $20k\Omega$ must be connected from `Rref` to `Vssa` (-2V).

D.3.3 The control voltage sources

The control voltage sources are generated by DACs with a resolution of 7 bits (Helix128-2/2.1) resp. 8 bits (Helix128-2.2/2.3), working from rail to rail (i.e. from $-2V$ to $+2V$); the slope provided is $\approx$ 31 mV/LSB (Helix128-2/2.1) resp. 15 mV/LSB (Helix128-2.2/2.3). The voltage DACs are controlled by the registers of the same name with the LSBs of the 8 bit wide registers ignored (Helix128-2/2.1). A register setting of 0 corresponds to an output voltage of -2V.

D.3.4 The sampling clock generator

In the following we discuss the sampling clock *Sclk* ruling the pipeline operation. This clock should not be confused with the comparator's `CompClk` clock described in sect. D.2.3 (both run at 10 MHz in the HERA-B experiment; both try to catch the maximum pulse height of the shaped frontend pulse but, however, the sampling transitions of the two clock should be slightly detuned to avoid mutual interference).

The falling edge of the sampling clock determines the sampling point of time, i. e. when the frontend outputs are sampled into the pipeline column "on duty". The sampling clock (nominally 10Mhz) *Sclk* can be either applied to the `Sclk` input pad or generated internally from `Rclk`. Therefore the lower four bits of the *ClkDiv* register hold the ratio of the `Rclk` (readout) and *Sclk* (sampling) clocks. Valid values are 0-15. If the content of $ClkDiv = 0$, the signal applied to the `Sclk` input pad is used for sampling. The internally generated *Sclk* will have its first **rising edge** synchronously with the **fourth rising edge** of `Rclk` following the **rising edge** of `notReset`. This behaviour is illustrated in Fig. D.12. The duty cycle of the internally generated *Sclk* signal is 50%.

D.3.5 The starter circuit

Helix128-2 features two different resets: first, `SufixReset` resets all the registers as described in table D.4 but, however, leaves the pipeline and multiplexer operation unaffected. Applying a `SufixReset` signal after power up is not mandatory since the internal registers should wake up atomatically in the 0 state. `notReset`, on the other hand, only resets the pipeline pointers (described in the following) and the readout multiplexer control circuitry. By activating `notReset`, which may be done asynchronously, an undefined state in the pipeline or in the multiplexer can be corrected without the need of reprogramming all internal bias registers. For an initial reset we recommend to first perform `SufixReset` and `notReset`, then release the `SufixReset` and load the internal registers as described in section D.3.9, and finally release `notReset` by setting it to +2 V. The adjustment of the pipeline delay according to the desired trigger latency is done by programming the *Latency* register. To illustrate this feature, we repeat the pipeline operation for convenience (see section D.3.1 for a detailed discussion): immediately after releasing the active low `notReset` (synchronously to the rising edge of `Sclk`) the write pointer starts walking over the pipeline incremented by `Sclk`. The pipeline column the `write pointer` currently points at stores the frontend output voltage at the falling edge of `Sclk`. The trigger pointer as the second pointer controlling the pipeline points to the pipeline column to be read out if a trigger on `TrigIn` was given. The start of the pipeline trigger pointer is delayed with respect to the start of the write pointer by the number of `Sclk` cycles specified in the *Latency* register thus determining the latency of the pipeline.

D.3.6 The readout

Daisy chain mode

Helix128-2 chips can be daisy-chained in order to save cost in following stages. A diagram of several Helix128-2.0/2.1 chips in a daisy chain is given in fig. D.13. The following discussion holds for Helix128-2.0/2.1; Helix128-2.2/2.3 makes use of an identical scheme but with reversed token direction (i. e. the chips in a daisy-chain are read out from top to bottom). Failsafe token pads as well as pads for a reversed-polarity token have been added for compatibility with the future Helix128-3.0.

The first or leading Helix128-2 in the daisy chain generates the primary token at the output of `SufixTokenOut`. By bonding `SufixTokenOut` to `SufixTokenIn` on the first chip the token is transferred to the readout multiplexer which starts transmitting the analog values on the common analog busses (the outputs of chips not posessing the token are switched to high ohmic). After the final values of chip #1's analog data the token is output on `HelixTokenOut` of chip #1 to `HelixTokenIn` of chip #2. Upon receipt the second chip's multiplexer starts sending data since the `HelixTokenIn` and `SufixTokenIn` pads are internally connected (the `SufixTokenIn` pad has been added for ease of bonding). By bonding from `HelixTokenOut` to `ReturnTokenIn` on the daisy chain's last chip the *token* is fed into the token return path thus being directly transferred to the leading chip of the chain (since `ReturnTokenIn` and `ReturnTokenOut` are internally connected). By receipt of the returning token the leading chip is signaled the end of the transmission. The signal on the common output bus is illustrated in fig. D.14.

If only a single chip is operated, `SufixTokenOut` must be bonded to `SufixTokenIn` and `HelixTokenOut` to `ReturnTokenIn`.

TokenDelay

The content of the *TokenDelay* register determines the duration in `RClk` cycles the leading Helix128-2 waits before it starts sending the next event's analog data after having received the return token from the previous readout. Thus, a regular delay in processing of the sent data can be accounted for (see fig. D.14). The delay is achieved by holding back the `SufixTokenOut` token output of the leading Helix128-2. A value of 0 indicates immediate sending of the next event. In case of single chip operation the delay as specified in the *TokenDelay* register is added to the time which is needed to load the multiplexer.

`TransmitEnable`

A sudden busy condition of the data receiving stage can be flagged to Helix128-2 by pulling low `TransmitEnable`; it then stops transmitting data and starts again when `TransmitEnable` is pulled up (this condition is checked at the falling `Rclk` edge). `TransmitEnable` is internally pulled up to +2 V.

D.3.7 The synchronicity monitor

The synchronicity monitor circuit checks the signals of neighbouring Helix128-2 chips to assure synchronous operation. For this purpose, internal signals *TrigMon* and *WriteMon* are generated when the write pointer resp. the trigger pointer passes by column 0 of the pipeline. The synchronicity monitor checks the simultaneous occurrence of these internal signals as well as of the `DataValid` signals with the ones received on `SyncIn`<*i*>. `SyncOut`<*i*> signals are generated depending on the comparison result according to table D.2. The `DataValid` check, naturally, has to be abandonned in daisy chain operation mode.

Using a differential architecture both missing and wrong monitor pulses can be detected. If a deviation occurres, an error signal on `Error` is generated, which should be collected from the last chip in the synchronicity chain.

The content of the *SyncCtrl* register determines the behaviour of the `SyncOut<0:5>` and `Error` signals. A description is given in Tab. D.3.

signal name	logic dependency	comment
SyncOut<0>	*TrigMon* & SyncIn<0>	*wired and* of all *TrigMon* signals
SyncOut<1>	!*TrigMon* & SyncIn<1>	*active low wired or* of all *TrigMon* signals
SyncOut<2>	*writeMon* & SyncIn<2>	*wired and* of all *TrigMon* signals
SyncOut<3>	!*writeMon* & SyncIn<3>	*active low wired or* of all *writeMon* signals
SyncOut<4>	DataValid & SyncIn<4>	*wired and* of all DataValid signals
SyncOut<5>	!DataValid & SyncIn<5>	*active low wired or* of all DataValid signals

Table D.2: Dependencies of the SyncIn<5:0> and SyncOut<5:0> signals

D.3.8 The test pulse circuit

At the rising edge of a signal applied to the FcsTp pad, a charge equivalent to

- $\approx +1$ $\mathrm{MIP_{Si}}$ is injected into the inputs of the channels 1, 5, 9, 13 ...,
- $\approx +0.5$ $\mathrm{MIP_{Si}}$ into channels 2, 6, 10, 14 ...,
- ≈ -0.5 $\mathrm{MIP_{Si}}$ into channels 3, 7, 11, 15 ... and
- ≈ -1 $\mathrm{MIP_{Si}}$ into channels 4, 8, 12, 16 ....

with $+1MIP_{\mathrm{Si}}$ being equivalent to a charge of 24.000 electrons.

Thus, with an appropriate trigger a stairway-like readout figure is generated . The polarity of the injected charge toggles after each application (i.e. -1 $\mathrm{MIP_{Si}}$ is injected into channels 1, 5, 9, 13 ... for an even number of test pulses).

D.3.9 The serial interface

The programming of the Helix128-2's internal registers is achieved via a simple serial interface of three lines. In Helix128-2.0/2.1 the three signals involved are SerClk, SerData, and SerLoad, in Helix128-2.2/2.3 SerClk has been merged with Rclk and SerData with TrigIn. Thus, in the latter case, programming of the registers will give rise to multiple triggers; it is therefore recommended to keep notReset low during programming. The following explanation applies to Helix128-2.0/2.1, but is easily extended to the new scheme by making the above stated substitution.

During programming of the chip Rclk and SerClk must run continously. A 20 bit word is applied according to the Helix128-2 data frame (fig. D.15) on the SerData line synchronously to SerClk (fig. D.16). The end of the word is signaled to Helix128-2 by activating SerLoad; note that SerClk must continue running at least one more cycle.

bit number	function if cleared (*0*)	function if set (*1*)
7 (MSB)	`Error` pin in latch mode (i.e. signal remains high after occurrence of an error	`Error` pin in transient mode (i.e. it becomes active only during the existence of an error condition)
6	`Error` signal is generated from `Sync<0:1>` (i.e. *TrigMon*) signals	`Sync<0:1>` (i.e. *TrigMon*) is ignored for the `Error` signal
5	`Error` signal is generated from `Sync<2:3>` (i.e. *writeMon*) signals	`Sync<2:3>` (i.e. *writeMon*) is ignored for the `Error` signal
4	`Error` signal is generated from `Sync<4:5>` (i.e. `DataValid`) signals	`Sync<4:5>` (i.e. `DataValid`) is ignored for the `Error` signal
3	`SyncOut<0:1>` signal is generated from `SyncIn<0:1>` and *TrigMon* signals	`SyncOut<0:1>` = `SyncIn<0:1>` (i.e. *TrigMon* of this Helix128-2 does not contribute to `SyncOut<0:1>`)
2	`SyncOut<2:3>` signal is generated from `SyncIn<2:3>` and *writeMon* signals	`SyncOut<2:3>` = `SyncIn<2:3>` (i.e. *writeMon* of this Helix128-2 does not contribute to `SyncOut<2:3>`)
1	`SyncOut<4:5>` signal is generated from `SyncIn<4:5>` and `DataValid` signals	`SyncOut<4:5>` = `SyncIn<4:5>` (i.e. `DataValid` of this Helix128-2 does not contribute to `SyncOut<2:3>`)
0 (LSB)	`Error` = *0* (i.e. reset `Error`, only useful if bit #7 = *0*)	`Error` = *1* (i.e. set `Error`, only useful if bit #7 = *0*)

Table D.3: Flags of the *SyncReg* register

A Helix128-2 serial data frame consists of the following components:

- The *broadcast* or *common set bit*; if set, the chip address decoding is overridden and the register is set to the specified value.
- The *chip address*; the 6 bits of the chip address are compared to the signals of the `ID<5:0>` pads. If they do not match, the following bits are ignored (unless the *broadcast bit* has been set).
- The *register address*; the 5 bits specify the address of the register to be written to.
- The *data* word; the 8 bits contain the value the specified register is set to.

Data are written into the chip with the MSB first. Tab. D.4 shows the map of the register addresses.

Register address (*HEX*)	(*BIN*)	(*DEC*)	Register name
01	00001	01	*Ipre*
02	00010	02	*Isha*
03	00011	03	*Ibuf*
04	00100	04	*Icomp*
05	00101	05	*Ipipe*
06	00110	06	*Isf*
07	00111	07	*Idriver*
08	01000	08	*Vfp*
09	01001	09	*Vfs*
0A	01010	10	*VcompRef*
0B	01011	11	*Vd*
0C	01100	12	*Vdcl*
0D	01101	13	*Voffset*
11	10001	17	*Latency*
12	10010	18	*SyncReg*
13	10011	19	*ClkDiv*
14	10100	20	*TokenDelay*

Table D.4: Helix128-2 register map

D.3.10 Last but not least

`FifoFull`

The active high `FifoFull` flag is set when all eight slots in the event buffer are occupied; in this case Helix128-2 does not accept any further triggers and the corresponding events will be lost.

`MuxDisable`

`MuxDisable` is out of use.

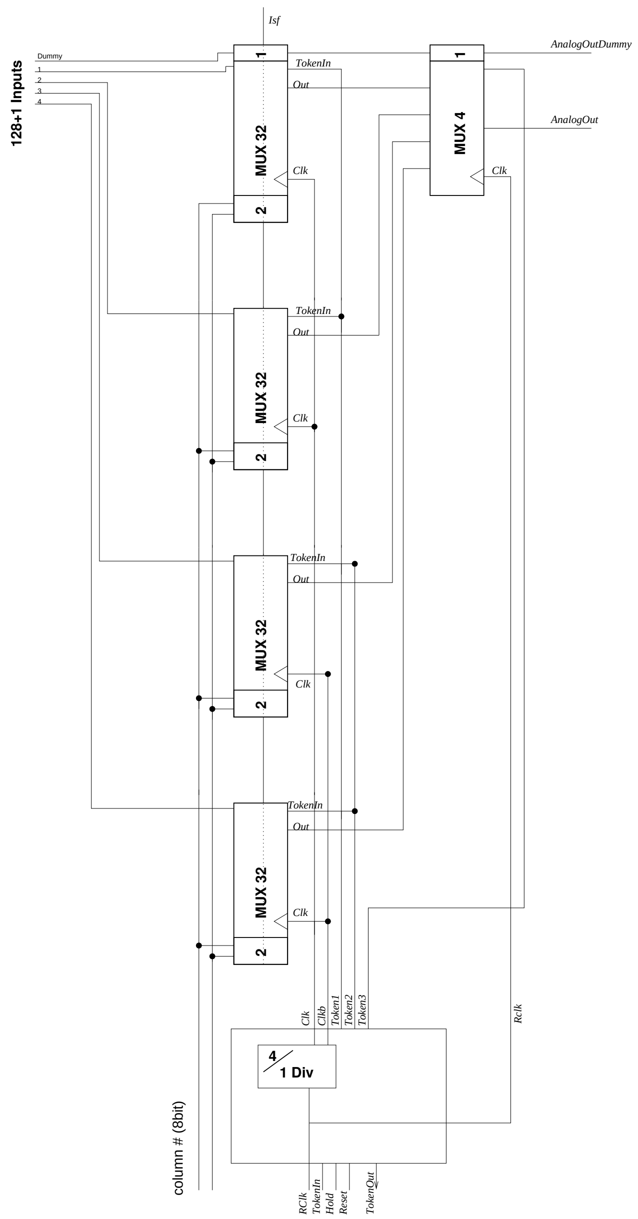


Figure D.7: Cascaded 128+8+1 channel multiplexer

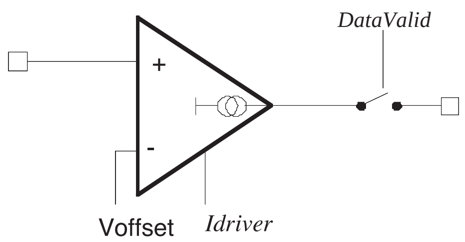


Figure D.8: Current buffer

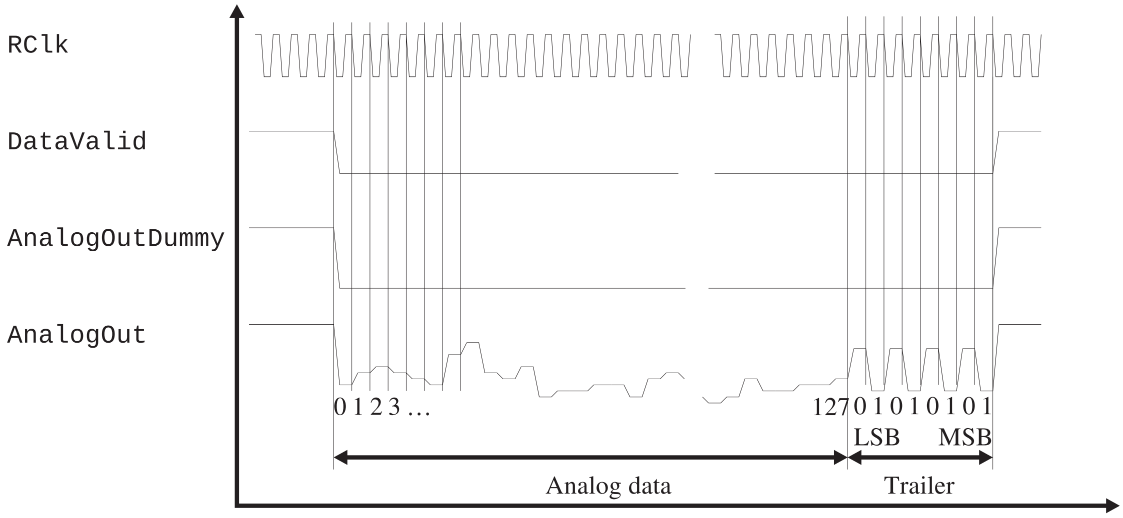


Figure D.9: Format of a readout burst

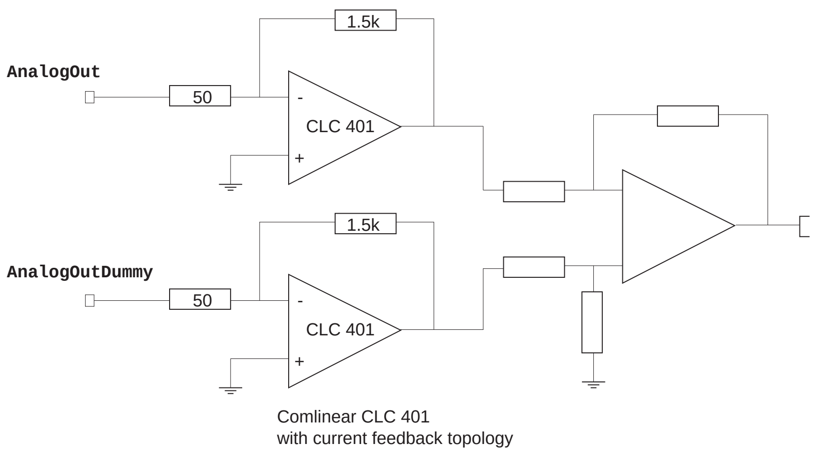


Figure D.10: Suggested receiver circuit for the analog signals **AnalogOut** and **AnalogOutDummy**

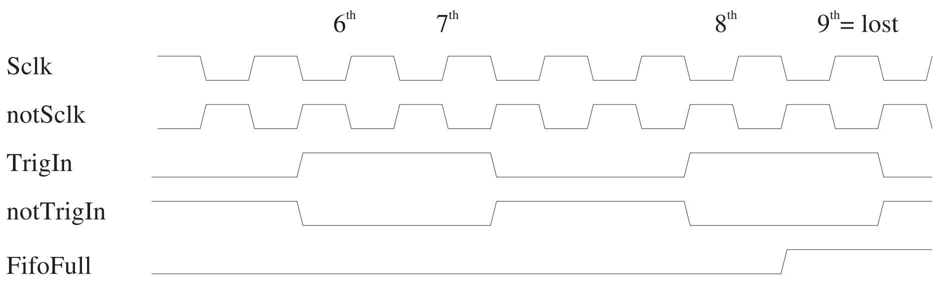


Figure D.11: Sampling of the `TrigIn`-signal occurs at the rising edge of `Sclk`. If more than 8 triggers are given in fast sequence, the derandomizing buffer flows over signalling "`FifoFull`".

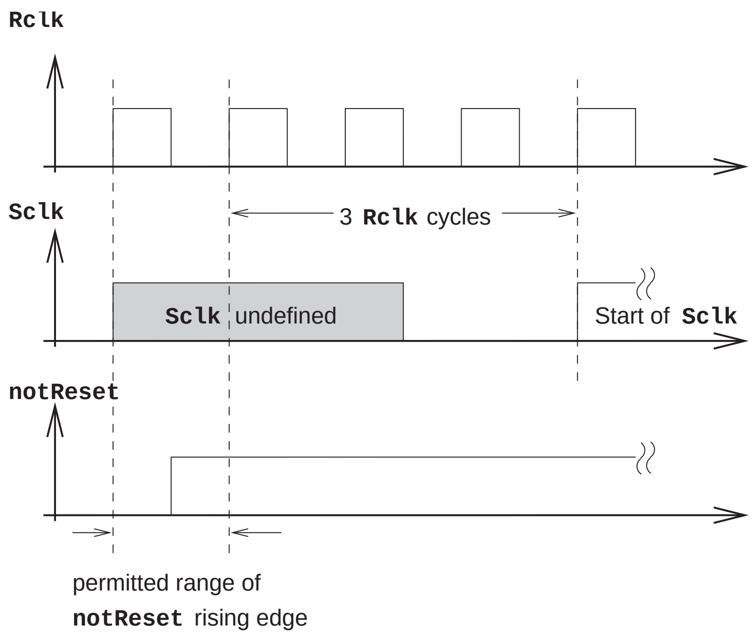


Figure D.12: `Sclk` initialization for `Clockdiv` $\neq 0$

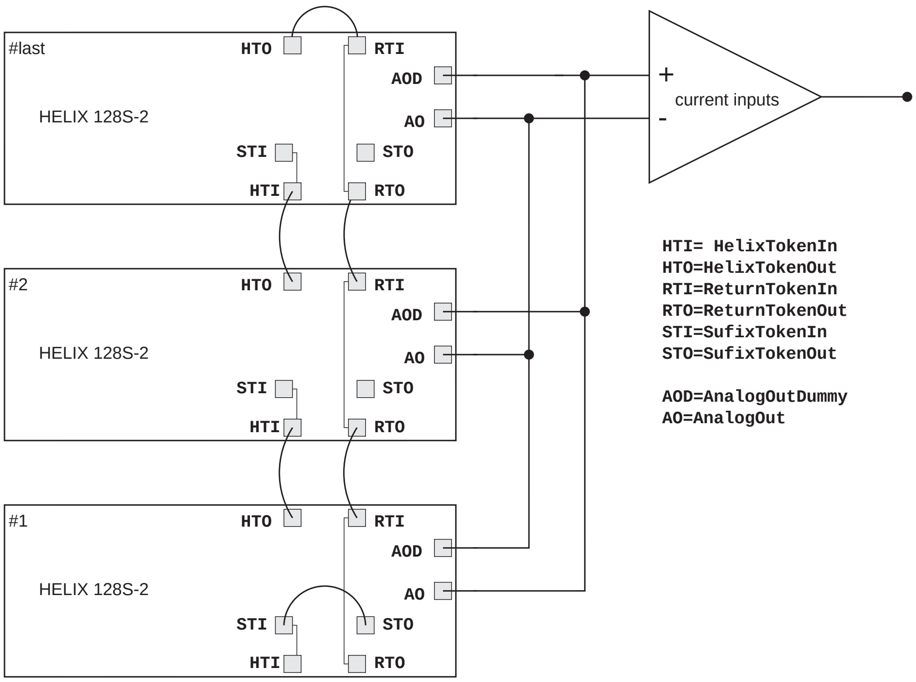


Figure D.13: Helix128-2.0/2.1 in daisy chain mode; with Helix128-2.2/2.3 the token circulates in opposite direction (i. e. counter-clockwise).

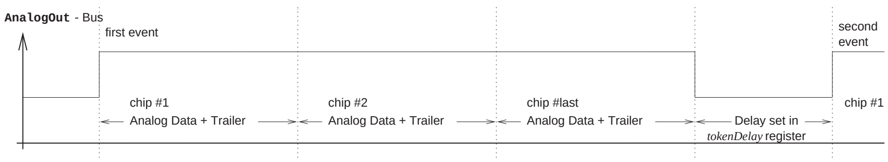


Figure D.14: Analog current signal on the `AnalogOut` bus for the daisy chain illustrated in fig. D.13

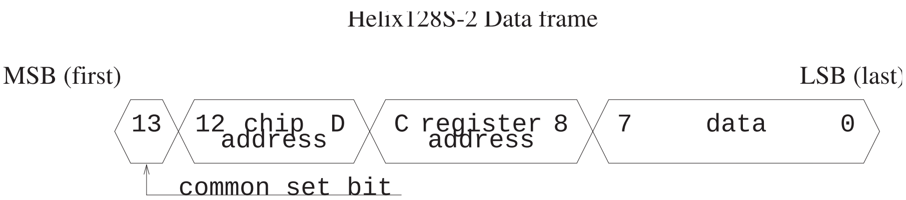


Figure D.15: Data format of the Helix128-2 chip

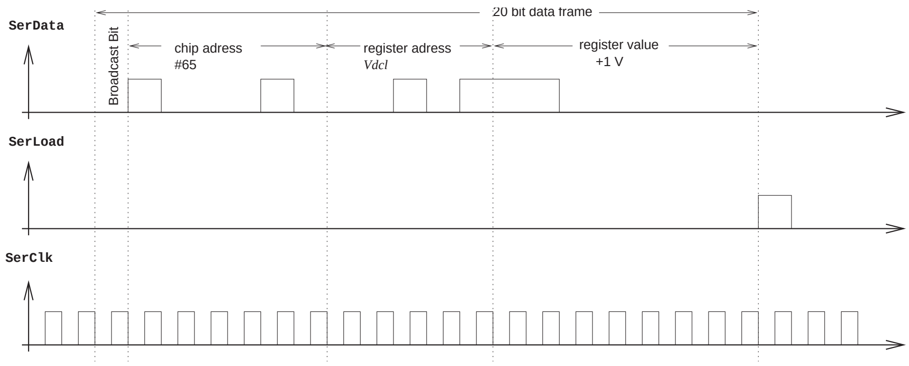


Figure D.16: Serial interface timing (Helix128S-2.0/2.1); substituting `SerClk` by `Rclk` and `SerData` by `TrigIn` gives the programming sequence of Helix128S-2.2/2.3. In the example plotted the $Vdcl$ bias voltage is set to its nominal (Helix128-2.0/2.1/2.2) value of $+1$V.

D.4 Appendix: Pad Description

To match the pitch of 50μm silicon microstrip detectors an overall pitch of 50μm can be obtained by placing Helix128-2 chips side by side. The 128 analog input pads are located at the front of the chip w. r. t. the detector (see fig. D.17) while all pins necessary to operate the chip, i. e. power supply, digital control lines and analog output, are located at the rear side. The chip's trigger output pads are placed at the bottom side (with the input pads left) due to the relaxed space requirements of the HERA-B Inner Tracking Detector which makes use of the comparator information. Digital signals are categorized as outlined in table D.5. For a description of the analog pads refer to the text.

All pads have been given reference numbers. Counting starts with the uppermost pad of the front (i. e. detector) side (with the input pads left) and continues with the peripheral pads counterclockwise around the chip. Finally, the probe pads in the chip's interior are counted from bottom to top. For the geometrical location refer to figure D.17 on page 45 (Helix128-2), fig. D.18 on page 46 (Helix128-2.1), and fig. D.19 on page 47 (Helix128-2.2/2.3).

D.4.1 Front pads

The analog input pads and some analog supply pads are located at the front side of Helix128-2. The input pads are staggered fourfold with a pitch of 41.4μm. A description is given for Helix128-2.0 and Helix128-2.1 in table D.6 on page 32, a description for Helix128-2.2/2.3 can be found in table D.7 on page 32.

D.4.2 Bottom pads

The bottom pads of Helix128-2.0/2.1 are explained in table D.8 on page 33. The bottom pads of Helix128-2.2/2.3 are explained in table D.9 and D.10 on page 34 and 35, respectively.

Type	Description
input	Digital CMOS input operating at -2V...+2V supply.
output	Digital CMOS output operating at -2V...+2V supply.
input (int. pulldown)	Digital CMOS input operating at -2V...+2V supply with internal pulldown resistor.
input (int. pullup)	Digital CMOS input operating at -2V...+2V supply with internal pullup resistor.
output (open drain)	Digital open drain output operating at -2V...+2V supply.
LVDS-input	Low voltage differential CMOS input ($\Delta V_{Sig,notSig} \geq$ 350 mV)

Table D.5: Electrical specification of digital input and output pads

Ref. no.	Pin name	Type	Description
1	`Vdda`	supply	positive analog supply voltage (+2V)
2	`Vssa`	supply	negative analog supply voltage (−2V)
3	`In`⟨0⟩	analog input	input of channel 0
4	`In`⟨1⟩	analog input	input of channel 1
5	`In`⟨2⟩	analog input	input of channel 2
6-128	⋮	⋮	⋮
129	`In`⟨126⟩	analog input	input of channel 126
130	`In`⟨127⟩	analog input	input of channel 127
131,132	`Gnda`	supply	analog ground (0V)

Table D.6: Pads on the front side of Helix128-2.0/2.1. The first pad in the table corresponds to the uppermost pad of the front side (looking at the chip with the frontside left). The geometrical locations throughout the manual will always be referred to this orientation.

Ref. no.	Pin name	Type	Description
1	`Vdda`	supply	positive analog supply voltage (+2V)
2	`Vssa`	supply	negative analog supply voltage (−2V)
2a	`InTest`	input	analog input pad for test channel
3	`In`⟨0⟩	analog input	input of channel 0
4	`In`⟨1⟩	analog input	input of channel 1
5	`In`⟨2⟩	analog input	input of channel 2
6-128	⋮	⋮	⋮
129	`In`⟨126⟩	analog input	input of channel 126
130	`In`⟨127⟩	analog input	input of channel 127
131,132	`Gnda`	supply	analog ground (0V)

Table D.7: Pads on the front side of Helix128-2.2/2.3. The first pad in the table corresponds to the uppermost pad of the front side (looking at the chip having the frontside left). The geometrical locations throughout the manual will always be referred to this orientation.

Ref. no.	Pin name	Type	Description
133,134	Gnda	supply	analog ground (0V)
135,136	Vssa	supply	negative analog supply voltage (-2V)
137,138	Vdda	supply	positive analog supply voltage (+2V)
139	VssComp	supply	negative supply voltage for comparator (-2V)
140	VddComp	supply	positive supply voltage for comparator (+2V)
141	notCompClk	input	active low comparator dummy clock
142	CompClk	input	active high comparator clock
143	CompPol	input	polarity switch for comparator +2V$\Rightarrow$ detection of positive signals
144	notCompOut⟨31⟩	output (open drain)	ORed active low output of comparators on channels 127...124
145	notCompOut⟨30⟩	output (open drain)	ORed active low output of comparators on channels 123...120
146-173	⋮	⋮	⋮
174	notCompOut⟨1⟩	output (open drain)	ORed active low output of comparators on channels 7...4
175	notCompOut⟨0⟩	output (open drain)	ORed active low output of comparators on channels 3...0
176	MuxDisable	input (int. pulldown)	Out of use
177	TransmitEnable	input (int. pullup)	-2V disables analog data transmission
178	FifoFull	output	indicates readout fifo overflow.
179	HelixTokenIn	input	to be connected to pad no. 257 HelixTokenOut of predecessing Helix128-2.0/2.1 if the chip is nonleading in a daisy chain (not to be connected for single chip operation and if the chip is the first in a daisy chain)
180	ReturnTokenOut	output	to be connected to pad no. 256 ReturnTokenIn of predecessing Helix128-2.0/2.1 if the chip is nonleading in a daisy chain (not to be connected for single chip operation and if the chip is the first in a daisy chain)
181	SyncIn⟨0⟩	input (int. pullup)	synchronicity monitoring input from neighbouring Helix128-2.0/2.1
182	SyncIn⟨1⟩	input (int. pullup)	"
183-185	⋮	⋮	⋮
186	SyncIn⟨5⟩	input (int. pullup)	"
187-197	n. c.		

Table D.8: Pads on the bottom side of Helix128-2.0/2.1. The first pad in the table corresponds to the very left hand pad of the bottom side (with the frontside left).

Ref. no.	Pin name	Type	Description
133,134	`Gnda`	supply	analog ground (0V)
135,136	`Vssa`	supply	negative analog supply voltage (-2V)
137,138	`Vdda`	supply	positive analog supply voltage (+2V)
138a	`GndComp`	supply	Reference voltage for comparators' AC coupling
139	`VssComp`	supply	negative supply voltage for comparator (-2V)
140	`VddComp`	supply	positive supply voltage for comparator (+2V)
141	`CompClk`	input	active high comparator dummy clock
142	`notCompClk`	LVDS-input	active low comparator clock
143	`CompPol`	LVDS-input	polarity switch for comparator +2V$\Rightarrow$ detection of positive signals
144	`notCompOut`$\langle$31$\rangle$	output (open drain)	ORed active low output of comparators on channels 127. . . 124
145	`notCompOut`$\langle$30$\rangle$	output (open drain)	ORed active low output of comparators on channels 123. . . 120
146-173	⋮	⋮	⋮
174	`notCompOut`$\langle$1$\rangle$	output (open drain)	ORed active low output of comparators on channels 7. . . 4
175	`notCompOut`$\langle$0$\rangle$	output (open drain)	ORed active low output of comparators on channels 3. . . 0
176	`VssComp`	supply	-2V supply for `notCompOut`$\langle$1$\rangle$
177	`TransmitEnable`	input (int. pullup)	-2V disables analog data transmission
178	`FifoFull`	output	indicates readout fifo overflow.
178a	`VssComp`	supply	-2V supply for `notCompOut`$\langle$1$\rangle$

Table D.9: Pads on the bottom side of Helix128-2.2/2.3. The first pad in the table corresponds to the very left hand pad of the bottom side (with the frontside left). See table D.10 for pads 179. . .197a.

Ref. no.	Pin name	Type	Description
179	`notHelixTokenOut`	output	Reserved for future use
180	`notReturnTokenIn`	input	Reserved for future use
180a	`ReturnTokenIn`	input	return path token input; must be bonded to pad no. 187 `HelixTokenOut` if the chip is the last in the daisy chain and for single chip operation (otherwise bonded to pad no. 257a `ReturnTokenOut` of following chip in the daisy chain)
181	`SyncIn`$\langle 0\rangle$	input (int. pullup)	synchronicity monitoring input from neighbouring Helix128-2.2/2.3
182	`SyncIn`$\langle 1\rangle$	input (int. pullup)	“
183-185	$\vdots$	$\vdots$	$\vdots$
186	`SyncIn`$\langle 5\rangle$	input (int. pullup)	“
187	`HelixTokenOut`	output	must be bonded to pad no. 180a `ReturnTokenIn` if the chip is the last in the daisy chain and for single chip operation (otherwise bonded to pad no. 251 `HelixTokenIn` of following chip in the daisy chain)
188	`notFailsafe-HelixTokenOut`	output	Reserved for future use
189	`notFailsafe-ReturnTokenIn`	input	Reserved for future use
190	`Failsafe-ReturnTokenIn`	input	Reserved for future use
191	`Failsafe-HelixTokenOut`	output	Reserved for future use
192	n. c.		
193-197a			Removed

Table D.10: Pads on the bottom side of Helix128-2.2/2.3 (continued). The first pad in the table corresponds to the very left hand pad of the bottom side (with the frontside left). See table D.9 for pads 133…178a.

D.4.3 Rear pads

The pads on the rear side of Helix128-2.x are placed in a 140μm pitch. A description of the pads of Helix128-2.0 is given in table D.11 on page 37, of Helix128-2.1 in table D.12 on page 38, and of Helix128-2.2 in table D.13on page 39.

Ref. no.	Pin name	Type	Description
240	`Vddg`	supply	positive pad guard supply voltage (+2V)
239,238	`Vddd`	supply	positive digital supply voltage (+2V)
237-234	`Vdda`	supply	positive analog supply voltage (+2V)
233-230	`Vssa`	supply	negative analog supply voltage (−2V)
229,228	`Vssd`	supply	negative digital supply voltage (−2V)
227	`Vssg`	supply	negative pad guard supply voltage (−2V)
226	`Rref`	output	to be connected to external resistor (20kΩ) if internal reference current source is used.
225	`IrefOut`	output	output of internal reference current source
224	`IrefIn`	input	reference current input for internal current DAC; may either be connected to an external reference current source or to the `IrefOut` pin, if internal reference current source is to be used
223	`Voffset`	blocking outp.	should be connected to external blocking capacitor
222	`Idriver`	blocking outp.	"
221	`Vdcl`	blocking outp.	"
220	`Vd`	blocking outp.	"
219	`VcompRef`	blocking outp.	"
218	`AnalogOutDummy`	output	dummy serial analog output, should be subtracted from `AnalogOut`
217	`AnalogOut`	output	serial analog output
216,215	`n.c.`	n.c.	not connected
214	`Id⟨0⟩`	input (int. pulldown)	active high chip id adress
213-209	⋮	⋮	⋮
209	`Id⟨5⟩`	input (int. pulldown)	"
208	`FcsTp`	input	digital test pulse input; the rising edge signals moment of charge injection
207	`SufixReset`	input (int. pulldown)	active high reset signal for bias generator and controller part
206	`notReset`	input	active low pipeline reset signal
205	`DataValid`	output	active high signal indicating valid data on `analogOutDummy` and `analogOut`
204	`Error`	output	active high signal indicating an error condition on the chip
203	`SerLoad`	input	active high load signal for serial line interface
202	`SerData`	input	active high data signal for serial line interface
201	`TrigIn`	input	active high readout trigger input
200	`SerClk`	input	active high clock of serial line interface
199	`Rclk`	input	active high readout clock for data multiplexer
198	`Sclk`	input	active high sampling clock; the falling edge signals the sampling point of time

Table D.11: Pads on the rear side of Helix128-2.0. The first pad in the table corresponds to the uppermost pad of the chip's rear side (with the frontside left).

Ref. no.	Pin name	Type	Description
240	`Vddg`	supply	positive pad guard supply voltage (+2V)
239,238	`Vddd`	supply	positive digital supply voltage (+2V)
237-234	`Vdda`	supply	positive analog supply voltage (+2V)
233-230	`Vssa`	supply	negative analog supply voltage (-2V)
229,228	`Vssd`	supply	negative digital supply voltage (-2V)
227	`Vssg`	supply	negative pad guard supply voltage (-2V)
226	`Rref`	output	to be connected to external resistor (20kΩ) if internal reference current source is used.
225	`IrefOut`	output	output of internal reference current source
224	`IrefIn`	input	reference current input for internal current DAC; may either be connected to an external reference current source or to the `IrefOut` pin, if internal reference current source is to be used
223	`Voffset`	block. outp.	should be connected to external blocking capacitor
222	`Idriver`	block. outp.	"
221	`Vdcl`	block. outp.	"
220	`Vd`	block. outp.	"
219	`VcompRef`	block. outp.	"
218	`AnalogOut-Dummy`	output	dummy serial analog output, should be subtracted from `AnalogOut`
217	`AnalogOut`	output	serial analog output
216	`Id⟨0⟩`	input (int. pulldown)	active high chip id adress
215-211	⋮	⋮	⋮
211	`Id⟨5⟩`	input (int. pulldown)	"
210	`FcsTp`	input	digital test pulse input; the rising edge signals moment of charge injection
209	`SufixReset`	input (int. pulldown)	active high reset signal for bias generator and controller part
208	`notReset`	input	active low pipeline reset signal
207	`DataValid`	output	active high signal indicating valid data on `analogOutDummy` and `analogOut`
206	`Error`	output	active high signal indicating an error condition on the chip
205	`SerLoad`	input	active high load signal for serial line interface
204	`SerData`	input	active high data signal for serial line interface
203	`TrigIn`	input	active high readout trigger input
202	`SerClk`	input	active high clock of serial line interface
201	`notRclk`	input	active low readout clock for data multiplexer
200	`Rclk`	input	active high readout clock for data multiplexer
199	`notSclk`	input	active low sampling clock; the rising edge signals the sampling point of time
198	`Sclk`	input	active high sampling clock; the falling edge signals the sampling point of time

Table D.12: Pads on the rear side of Helix128-2.1. The first pad in the table corresponds to the uppermost pad of the chip's rear side (with the frontside left).

Ref. no.	Pin name	Type	Description
240	`Vddg`	supply	positive pad guard supply voltage (+2V)
239,238	`Vddd`	supply	positive digital supply voltage (+2V)
237-234	`Vdda`	supply	positive analog supply voltage (+2V)
233-230	`Vssa`	supply	negative analog supply voltage (−2V)
229,228	`Vssd`	supply	negative digital supply voltage (−2V)
227	`Vssg`	supply	negative pad guard supply voltage (−2V)
226	`Rref`	output	to be connected to external resistor (20kΩ) if internal reference current source is used.
225	`IrefOut`	output	output of internal reference current source
224	`IrefIn`	input	reference current input for internal current DAC; may either be connected to an external reference current source or to the `IrefOut` pin, if internal reference current source is to be used
223	`Voffset`	blocking outp.	should be connected to external blocking capacitor
222	`Idriver`	blocking outp.	"
221	`Vdcl`	blocking outp.	"
220	`Vd`	blocking outp.	"
219	`VcompRef`	blocking outp.	"
218	`AnalogOutDummy`	output	dummy serial analog output, should be subtracted from `AnalogOut`
217	`AnalogOut`	output	serial analog output
216	`Id⟨0⟩`	input (int. pulldown)	active high chip id adress
215	`Id⟨1⟩`	input (int. pulldown)	"
214-211	⋮	⋮	⋮
211	`Id⟨5⟩`	input (int. pulldown)	"
210	`FcsTp`	input	digital test pulse input; the rising edge signals moment of charge injection
209	`SufixReset`	input (int. pulldown)	active high reset signal for bias generator and controller part
208	`notReset`	input	active low pipeline reset signal
207	`DataValid`	output	active high signal indicating valid data on `analogOutDummy` and `analogOut`
206	`Error`	output	active high signal indicating an error condition on the chip
205	`SerLoad`	input	active high load signal for serial line interface
204	`notTrigIn`	LVDS-input	active low readout trigger input
203	`TrigIn`	LVDS-input	active high readout trigger input
202	`n.c.`	n.c.	Not connected
201	`notRclk`	LVDS-input	active low readout clock for data multiplexer
200	`Rclk`	LVDS-input	active high readout clock for data multiplexer
199	`notSclk`	LVDS-input	active low sampling clock; the rising edge signals the sampling point of time
198	`Sclk`	LVDS-input	active high sampling clock; the falling edge signals the sampling point of time

Table D.13: Pads on the rear side of Helix128-2.2/2.3. The first pad in the table corresponds to the uppermost pad of the chip's rear side (with the frontside left).

D.4.4 Top side pads

A pad description for Helix128-2.0 and Helix128-2.1 is given in table D.14 on page 41, the description for Helix128-2.2 in table D.15 on page 42.

D.4.5 Core pads

Some pads have been located in the chip's core. Most of them are for diagnostic purposes, but on Helix128-2.x pad no. 267 `SufixTokenOut` and no. 268 `HelixTokenIn` play an important role in the daisy chain token scheme; in Helix128-2.2/2.3 `SufixTokenOut` can also be obtained from the top side (pad no. 246). The pads for Helix128-2.0 and Helix128-2.1 are explained in table D.16 on page 43, the pads for Helix128-2.2/2.3 in table D.17 on page 44.

Ref. no.	Pin name	Type	Description
266,265	`Gnda`	supply	analog ground (0V)
264,263	`Vssa`	supply	negative analog supply voltage (−2V)
262,261	`Vdda`	supply	positive analog supply voltage (+2V)
260	`TestOut`	output	test channel preamplifier output
259	`HelixTokenOut`	output	token output; must be bonded to pad no. 256 `ReturnTokenIn` if the chip is the last in the daisy chain and for single chip operation (otherwise bonded to pad no. 179 `HelixTokenIn` of following chip in the daisy chain)
258	`ReturnTokenIn`	input	return path token input; must be bonded to pad no. 257 `HelixTokenOut` if the chip is the last in the daisy chain and for single chip operation (otherwise bonded to pad no. 180 `ReturnTokenOut` of following chip in the daisy chain)
257	`SyncOut`⟨0⟩	output	synchronicity monitoring output to neighbouring Helix128-2.0/2.1
256	`SyncOut`⟨1⟩	output	“
255-253	⋮	⋮	⋮
252	`SyncOut`⟨5⟩	output	“
251	`SufixBus`⟨7⟩	test outp.	bias generator data bus; used for verification of correct internal operation; no connection needed for normal operation
250	`SufixBus`⟨6⟩	test outp.	“
249-245	⋮	⋮	⋮
244	`SufixBus`⟨0⟩	test outp.	“
243	`notSel`⟨6⟩	test outp.	select bus in bias generator; strobes access to the *Idriver* DAC; used for verification of correct internal operation; no connection needed for normal operation
242	`notSel`⟨5⟩	test outp.	select bus in bias generator; strobes access to the *Isf* DAC; used for verification of correct internal operation; no connection needed for normal operation
241	`notSel`⟨4⟩	test outp.	select bus in bias generator; strobes access to the *Ipipe* DAC; used for verification of correct internal operation; no connection needed for normal operation

Table D.14: Pads on the top side of Helix128-2.0/2.1. The first pad in the table corresponds to the uppermost pad of the chip's top side (with the frontside left).

Ref. no.	Pin name	Type	Description
266,265	`Gnda`	supply	analog ground (0V)
264,263	`Vssa`	supply	negative analog supply voltage (-2V)
262,261	`Vdda`	supply	positive analog supply voltage (+2V)
260	`TestOut`	output	test channel preamplifier output
259c	`GndComp`	supply	Reference voltage for comparators' AC coupling (0V)
259b	`VssComp`	supply	Comparators' most negative supply (-2V)
259a	`VddComp`	supply	Comparators' most positive supply (+2V)
259	`notHelixTokenIn`	input	Reserved for future use
258	`notReturnTokenOut`	output	Reserved for future use
257a	`ReturnTokenOut`	output	to be connected to pad no. 180a `ReturnTokenIn` of predecessing Helix128-2.2/2.3 if the chip is nonleading in a daisy chain (not to be connected for single chip operation and if the chip is the first in a daisy chain)
257	`SyncOut`$\langle 0\rangle$	output	synchronicity monitoring output to neighbouring Helix128-2.2./2.3
256	`SyncOut`$\langle 1\rangle$	output	“
255-253	⋮	⋮	⋮
252	`SyncOut`$\langle 5\rangle$	output	“
251	`HelixTokenIn`	input	to be connected to pad no. 187 `HelixTokenOut` of predecessing Helix128-2.2/2.3 if the chip is nonleading in a daisy chain (not to be connected for single chip operation and if the chip is the first in a daisy chain)
250	`notFailsafeReturnTokenOut`	output	Reserved for future use.
249	`FailsafeReturnTokenOut`	output	Reserved for future use.
248	`FailsafeHelixTokenIn`	input	Reserved for future use.
247	`FailsafeHelixTokenOut`	output	Reserved for future use.
246	`SufixTokenOut`	output	Output of token generator (see pad no. 267)
245-240a	`n.c.`		Removed

Table D.15: Pads on the top side of Helix128-2.2/2.3. The first pad in the table corresponds to the uppermost pad of the chip's top side (with the frontside left).

Ref. no.	Pin name	Type	Description
267	`SufixTokenOut`	output	initial token out of first chip in daisy chain; to be bonded to pad no. 268 `HelixTokenIn` for the first chip in a daisy chain and for single chip operation (otherwise not to be connected)
268	`HelixTokenIn`	input	internally connected to the adjacent pad no. 182; to be bonded to pad no. 267 `SufixTokenOut` for the first chip in a daisy chain and for single chip operation (otherwise not to be connected)
269	`TrigMon`	test outp.	test pad to probe the `TrigMon` signal (no connection needed for normal operation)
270	`WriteMon`	test outp.	`WriteMon` signal
271	`Trigger`	test outp.	`Trigger` signal
272	`notTrigger`	test outp.	`notTrigger` signal
273	`notReset`	test outp.	`notReset` signal
274	`notTReset`	test outp.	`notTReset` signal
275	`Voffset`	test outp.	buffer *Voffset* voltage
276	`Vdcl`	test outp.	pipeamp *Vdcl* voltage
277	`Vd`	test outp.	pipeamp *Vd* voltage
278	`VcompRef`	test outp.	comparator *VcompRef* voltage
279	`Vfs`	test outp.	shaper *Vfs* voltage
280	`Vfp`	test outp.	preamplifier *Vfp* voltage

Table D.16: Description of the Helix128-2.0 and Helix128-2.1 core pads. The first pad in the table corresponds to the lowest right hand side core pad (with the frontside left).

Ref. no.	Pin name	Type	Description
267	`SufixTokenOut`	output	initial token out of first chip in daisy chain; to be bonded to pad no. 268 `HelixTokenIn` for the first chip in a daisy chain and for single chip operation (otherwise not to be connected)
268	`HelixTokenIn`	input	internally connected to the adjacent pad no. 182; to be bonded to pad no. 267 `SufixTokenOut` for the first chip in a daisy chain and for single chip operation (otherwise not to be connected)
269	`TrigMon`	test outp.	test pad to probe the `TrigMon` signal (no connection needed for normal operation)
270	`WriteMon`	test outp.	`WriteMon` signal
271	`Trigger`	test outp.	`Trigger` signal
272	`notTrigger`	test outp.	`notTrigger` signal
273	`notReset`	test outp.	`notReset` signal
274	`notTReset`	test outp.	`notTReset` signal
275	`Voffset`	test outp.	buffer *Voffset* voltage
276	`Vdcl`	test outp.	pipeamp *Vdcl* voltage
277	`Vd`	test outp.	pipeamp *Vd* voltage
278	`VcompRef`	test outp.	comparator *VcompRef* voltage
279	`Vfs`	test outp.	shaper *Vfs* voltage
280	`Vfp`	test outp.	preamplifier *Vfp* voltage

Table D.17: Description of the Helix128-2.2/2.3 core pads. The first pad in the table corresponds to the lowest right hand side core pad (with the frontside left).

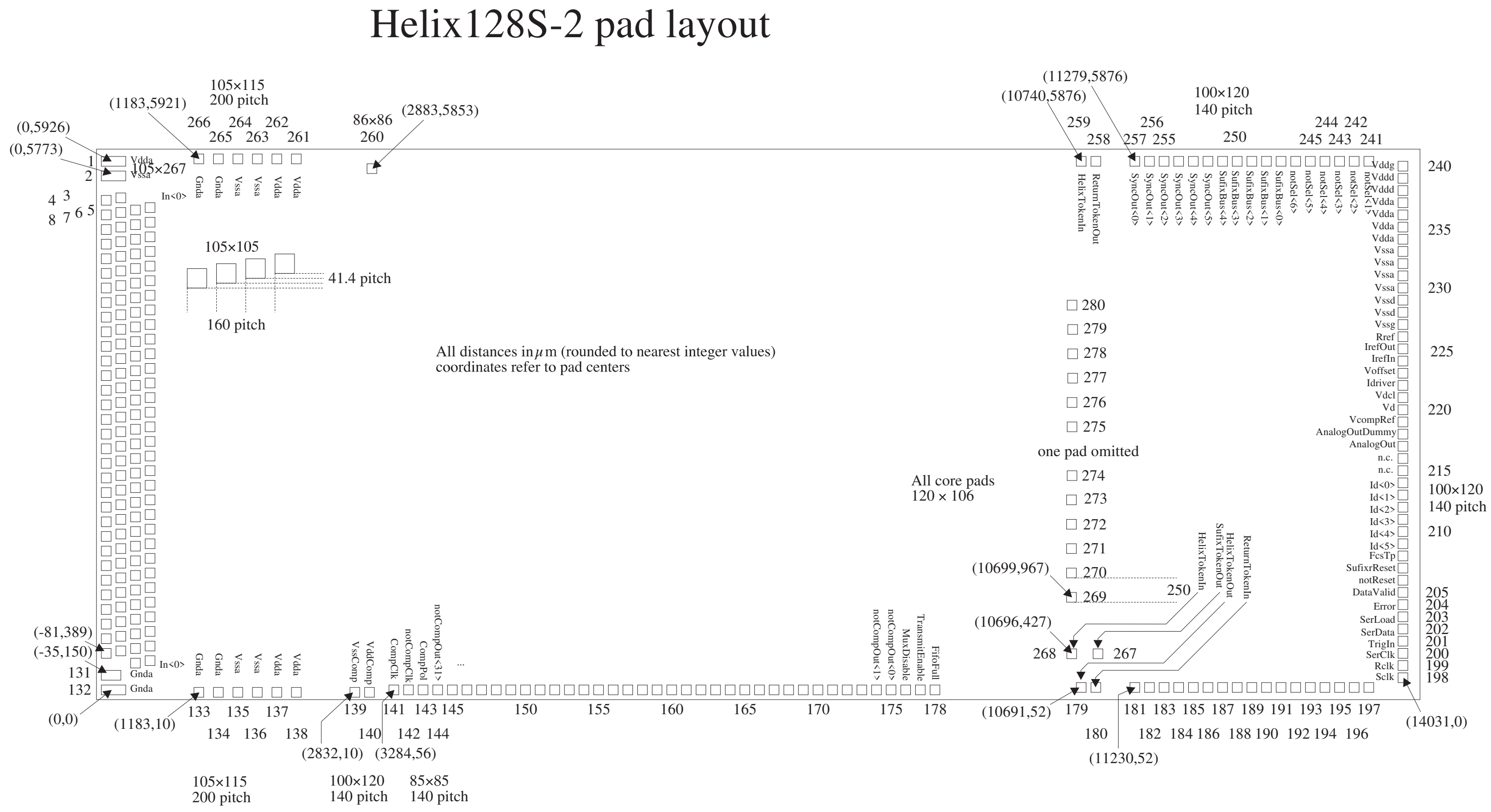


Figure D.17: Schematic drawing of the Helix128-2.0 pad locations; the overall chip dimension is 14,385μm x 6,146 μm. The frontside (facing the detector) is the bottom side in this view; in the descriptions we will refer to this side as the left side in regard of the "normal" signal flow from left to right.

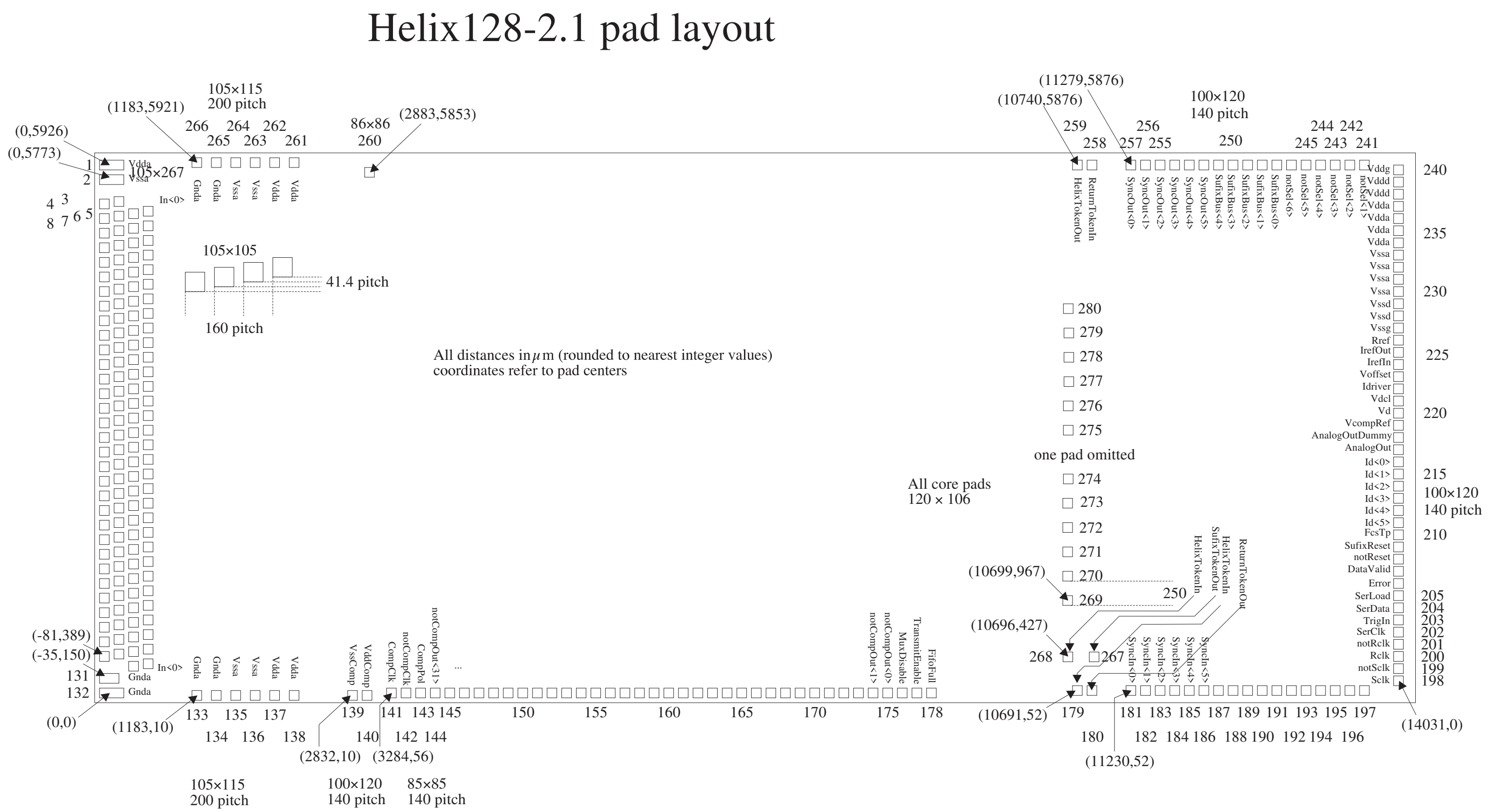


Figure D.18: Schematic drawing of the Helix128-2.1 pad locations. The `Sclk` and `Rclk` pads are now differential CMOS inputs.

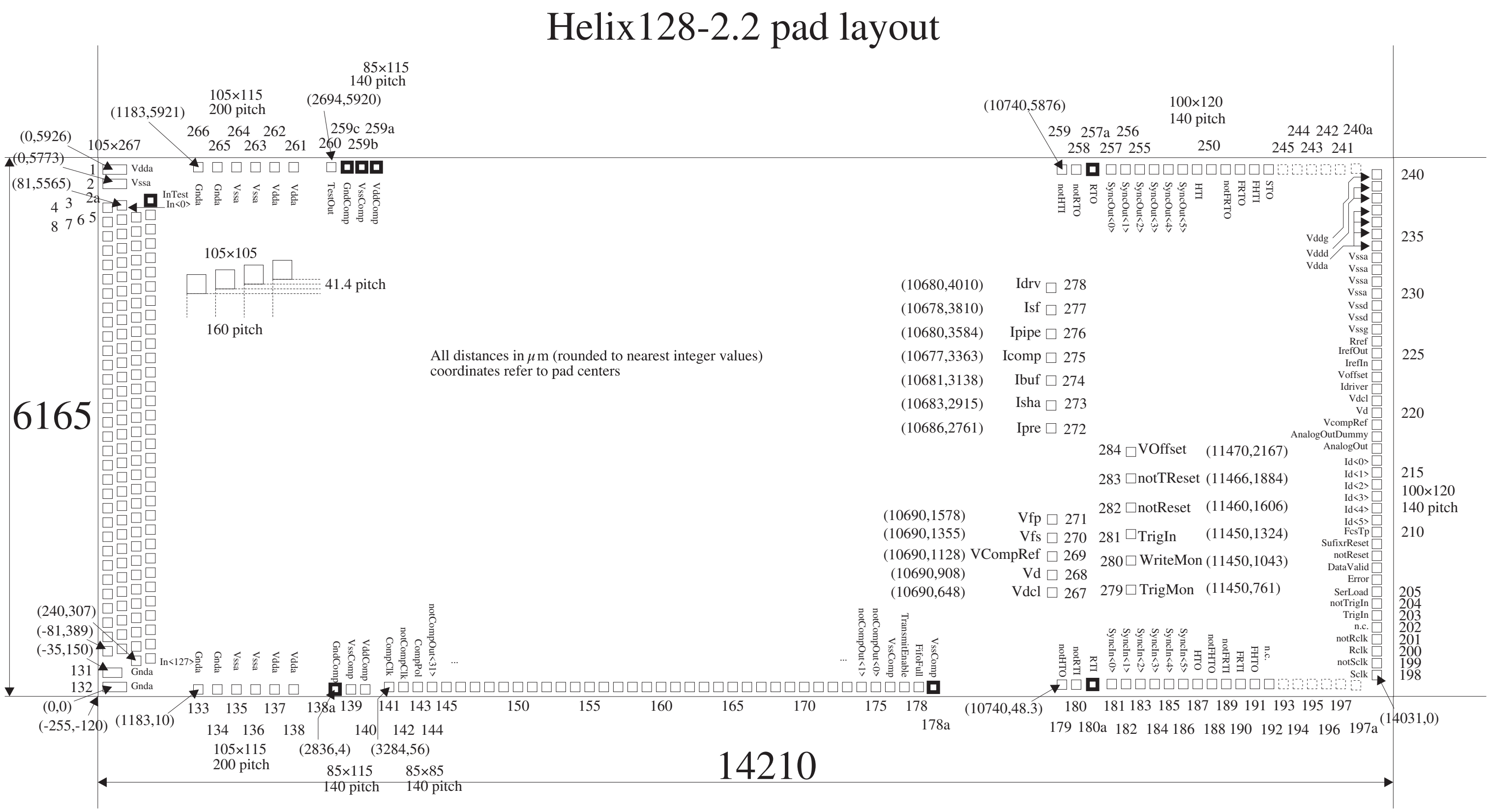


Figure D.19: Schematic drawing of the Helix128-2.2/2.3 pad locations. Token pads and power supply pads for the comparator outputs have been added.

D.5 Appendix: List of Known Problems

D.5.1 Helix128-2.0

1. Multi-event buffer non functional (1);
   Due to unfavorable routing of `Sclk` the chip has to be reset after each trigger. The employment of Helix128-2.0 should be restricted to laboratory evaluation.

2. Multi-event buffer (2);
   At certain well defined conditions a trigger can halt the chip (due to an unhandled condition in the pipeline logic)

3. *VcompRef* adjustment;
   VcompRef is the discriminator reference voltage of the comparators. It runs from -2V to +2V in 128 steps, giving a resolution of $\approx$ 31mV. Compared to the response to a signal of $1\mathrm{MIP}_{\mathrm{Si}}$ (24.000 electrons) of $\approx$ 50mV, this is much to coarse.

4. `Sclk` and `Rclk`;
   `Sclk` and `Rclk` are unipolar (nondifferential) signals which may cause excess noise on the chip, especially at fast `Rclk` timings.

5. `SerClk` and `Rclk`;
   `Rclk` must run faster than `SerClk` otherwise data might be lost.

6. `DataValid`, `AnalogOut` and `AnalogOutDummy`;
   `AnalogOut` and `AnalogOutDummy` jitter with respect to `DataValid`. The jitter can be up to 4 `Rclk` cycles, but is the same for all chips that have their `notReset` released at the same time.

7. Offset of `AnalogOut` and `AnalogOutDummy`;
   Due to unfavorable voltage level transitions in the pipeline readout amplifier, `AnalogOut` and `AnalogOutDummy` have a `Sclk`-dependent offset, which limits the dynamic range.

8. Crosstalk of switching comparator to all channels;
   Feedback via the open-collector discriminator outputs at the chip's bottom side to the amplifier inputs is suspected.

9. Pairwise crosstalk between channels (2n,2n+1) of approx. 8 %;
   Even if the pattern follows an asymmetry in the pipeline, the origin is not yet clear.

10. Reduced radiation hardness;
    Connected to problem 7 the pipeline amplifier fails at total doses in excess of 50 krad.

D.5.2 Helix128-2.1

Problems 1, 3, 4, 6 have been solved.

D.5.3 Helix128-2.2

Problems 7 and 10 have been solved. Problem 8 has greatly diminished and is perhaps not a problem any more.

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