High-Conductance States on a Neuromorphic Hardware System

Bernhard Kaplan, Daniel Brüderle, Johannes Schemmel and Karlheinz Meier

***Abstract*— Under typical synaptical stimulation, cortical neurons exhibit a total membrane conductance which, compared to a situation without any input spikes, is significantly increased. This results in a shorter membrane time constant and thus in an increased capability of the neuron to detect coincidences in its synaptic input. For this study, a neuromorphic hardware device was utilized, which does not provide direct access to its membrane conductances. Motivated by the aim of finding biologically realistic configuration regimes for the chip operation, a purely spike-based method for the estimation of membrane conductances is presented, allowing to test the hardware membrane dynamics. A proof of principle is given by pure software simulations. Hardware results are presented which illustrate the functionality of the method and show the possibility to generate high-conductance states in the utilized VLSI[1] neurons. In the final section, limits and useful implications of the proposed method are discussed.**

I. Introduction

High-Conductance States

Membrane dynamics of single neurons play an important role in neural information processing. Activity measurements in the cortex show that the dynamical properties of a membrane are strongly influenced by the total of its synaptically induced conductances [1], [2], [3], [4]. In this context, it is useful to distinguish between two states of neuronal activation: *Up* states or *activated* states, where the membrane is depolarized by increased extracellular activity and the embedded cell fires irregularly, and *down* states, where both intra- and extracellular activity follow low-frequency rhythms [5]. In the activated state, which is also called the *high-conductance state*, neurons show stochastic firing behavior and an enhanced responsiveness towards input stimuli.

The high-conductance state determines the properties of a single neuron's membrane within an active network. There is experimental evidence for its existence within in-vivo networks, e.g. in awake and attentive animals [2], [3], or in-vitro in localized sub-populations [4].

It is characteristic for neurons in the high-conductance state to exhibit a low input resistance, a depolarized membrane with large membrane potential fluctuations, dominant inhibitory conductances and a stochastical response to stimulation patterns due to fluctuating background activity [2], [6].

In [7] and [8], a model based on leaky integrate-and-fire neurons that can exhibit high-conductance states is described and analyzed. There, the membrane potential $V(t)$ is shown to follow the so-called effective reversal potential $V_{\text{eff}}(t)$ with the membrane time constant $\tau_m(t)$. $V_{\text{eff}}(t)$ is defined as the so-called difference current $I_D(t)$ between excitation and inhibition divided by the total membrane conductance $g_T(t)$:

$$V_{\text{eff}}(t) = \frac{I_D(t)}{g_T(t)} = \frac{g_E(t)E_E - g_I(t)|E_I|}{g_T(t)} \quad . \tag{1}$$

Here, $g_E(t)$ and $g_I(t)$ denote the sum of synaptically induced excitatory and inhibitory conductances, respectively, while E_E represents the excitatory and E_I the inhibitory reversal potential. The membrane time constant $\tau_m(t)$ is determined by the total membrane capacitance C_m and the total conductance $g_T(t) = g_l + g_E(t) + g_I(t)$, where g_l models a permanent and constant leakage conductance:

$$\tau_m(t) = \frac{C_m}{g_l + g_E(t) + g_I(t)} \quad . \tag{2}$$

This membrane time constant determines the temporal resolution capability of the neuron, because a small $\tau_m(t)$ makes the membrane potential immediately follow the effective reversal potential and therewith follow the synaptic input. Consequently, a neuron with a small $\tau_m(t)$ can perform well as a coincidence detector because it is able to immediately detect changes in input correlation.

Hidden Parameters and Computational Complexity

Neural behavior can be characterized by a variety of dimensions, e.g. spike rates, membrane potential traces, currents and conductances, amongst others. Depending on the observed system, it can be necessary to deduce unaccessible or with difficulty measurable magnitudes from easily accessible ones. E.g. for in-vivo and in-vitro recordings, the strength of a synaptic connection typically has to be deduced from the correlation of spiking and membrane activity of its pre- and post-synaptic neurons [9], [10]. The dynamics of multiple ion channels of various types are often combined to one total electric conductance of the membrane patch they are located on. This conductance can be accessed via patch-clamp techniques, during which voltages are applied and the resulting currents can be measured [11]. Another example for hidden variables is the assumed depletion of readily releasable vesicles at synapses in use, a popular explanation for the known phenomenon of short-term synaptic depression [12]. In general, models of neuronal and synaptic dynamics often involve variables which are hard to observe in-vivo or in-vitro.

If such a model - typically expressed by a set of differential equations - is numerically computed in software simulations,

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[1]Very Large Scale Integration

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any variable can be accessed arbitrarily. Together with the full flexibility in defining environmental conditions, this model transparency is one main reason for the wide and successful usage of software simulators in modeling neuroscience. Still, the more complex the underlying model becomes, the more computationally expensive its simulation will be [13]. Despite strong efforts towards sophisticated optimization techniques and parallelization of simulations, this fact creates a rather slowly receding limit for the range of computable network sizes and experiment durations.

Neuromorphic Hardware

The hardware system utilized in this study [14], [15] provides a way to avoid the scaling problem of software simulators. Due to its intrinsic parallelism in neural circuit operation, its speedup factor of up to 10^5 compared to emulated biological time is independent of the size of the implemented network. Furthermore, the software advantages like selectable parameters, definable topologies and adjustable environmental conditions also hold for the hardware system, although in a more limited way. Due to the physical nature of the analog model emulation, most variables and programmable parameters within the system are subject to electronic phenomena like noise, parasitic leakages and crosstalk.

As a major difference to pure software approaches, the only accessible hardware observables that are relevant in this context are the network's spike output, its membrane potentials and possibly evolving synaptic weights. Membranic conductances or currents are not directly accessible, so if necessary, they have to be deduced from the accessible observables. Since the sub-threshold membrane potentials have to be acquired via an oscilloscope connected to the hardware and then need to be integrated into the operating and evaluating software [16], [17] via TCP/IP sockets [18], this acquisition channel is rather slow and inefficient. The neuromorphic system design has been optimized for the access to all action potentials generated during an experiment via a fast digital connection. Thus, a deduction of hidden variables from nothing but the spike output is highly desirable.

One implication of high-conductance states which is especially interesting for the operation of neuromorphic hardware systems, namely a possible non-monotonous output vs. input rate relation of a neuron, is described e.g. in [6]: If a neuron is stimulated by excitatory and inhibitory input spike trains with the same rate and if excitation is dominating, for increasing input rates its output rate will also grow. But if the total membrane conductance gets larger due to the stimulus, the impact of the incoming spikes can start to decrease because of a faster membrane respectively shorter and thus less efficient post-synaptic potentials (PSPs). The phenomenon can be used to generate self-stabilizing states of network activity [6], which has the potential of serving as a mechanism for counterbalancing hardware-specific inhomogeneities and fluctuations.

For future biologically realistic experiments on the neuromorphic system, but also for the basic specification of hardware subunits, finding a working point in the high-conductance regime is essential. In the following, we study and exploit the effects of synaptical contributions to the total membrane conductance and consequently - in conjunction with the correlation of the applied input spike trains - on the output spike rate. We propose a purely spike-based and hence hardware-compatible method to estimate the amount of necessary synaptic stimulation in order to operate within a high-conductance state. Differences and hardware specific advantages of this method compared to a similar one introduced in [19] will be discussed in section IV.

II. Setup and Methods

A. Hardware Neuron Model

The coincidence detector experiment described below was conducted on a mixed-signal VLSI neuromorphic hardware device, which comprises 384 neurons per chip with 256 inputs each. The hardware neuron circuits implement a leaky integrate-and-fire model with conductance-based synapses. A detailed description of the hardware system can be found in [14], [15], [20]. In future up to 16 chips can be interconnected. The chip was produced using a standard $180\,\mathrm{nm}$ CMOS[2] process and is the prototype of a large wafer-scale integration system [21], [22] which is currently under development.

The neurons' membrane potentials obey the following differential equation:

$$-C_m \frac{dV}{dt} = g_l(V - E_l) + \sum_j p_j(t) g_j(t)(V - E_E) + \sum_k p_k(t) g_k(t)(V - E_I) \quad . \tag{3}$$

The constant C_m stands for the total membrane capacitance. The three summands on the right hand side represent three different ion channels: The first one models a continuous leakage which drives the membrane to its resting potential E_l with a constant conductance of g_l. The two remaining terms model the excitatory and inhibitory ion channels with their reversal potentials E_E and E_I, respectively. The index j of the first sum runs over all excitatory synapses, index k in the second sum over all inhibitory synapses. The conductance courses $g_{j,k}(t)$ are shaped as very sharp increases to the individual maximum values $g_{j,k}^{\max}$, followed by an exponential decrease with a time constant τ_{syn}. Each synapse has an open probability $p_{j,k}(t)$, which can be modified by short-term plasticity mechanisms [23]. Furthermore, for every synapse the maximum conductance $g_{j,k}^{\max}$ can be modified by spike-time dependent plasticity (STDP). The implementation of both long- and short-term plasticity mechanisms are described in detail in [14], [15] and are not further discussed here since only static synapses are used throughout this study. Once the membrane voltage exceeds its threshold voltage V_{thresh}, the neuron fires an action potential, then is pulled to a reset voltage V_{reset}, remaining there for some refractory period τ_{ref}, and afterwards follows the forces of its leakage, excitatory and inhibitory mechanisms again.

[2]Complementary Metal Oxide Semiconductor

B. Simulator NEST and Meta-Language PyNN

The software simulator NEST [24], [25] is a framework for simulating large networks of biologically realistic neurons. It provides various synapse types, recording devices and neuron models and can be extended by user-written modules. The neuron model utilized in the simulations presented here exactly implements Equation 3 and is described in detail in [26]. Just like the utilized hardware, NEST can be interfaced through the Python-based [27], simulator-independent scripting language PyNN [17], [28], allowing for a unified description and analysis of the performed experiments [16].

C. Spike-Based High-Conductance State Test

Test Concept: The basic idea of the proposed high-conductance state test is to estimate the total membrane conductance of a neuron by its ability to separate excitatory PSPs which are temporally close. The integration of successive PSPs on a membrane is less likely to cause an action potential if the temporal course of these PSPs is shorter. Assuming fixed time constants for the input-triggered increase and decrease of $g_E(t)$, the shape of the resulting PSP is shortened or stretched by the total membrane conductance. Thus, compared to a low-conductance regime, in a high-conductance state successive input spikes have to be temporally closer to cause an increase in output firing rate, which can be regarded as a better temporal resolution capability of the neuron.

In other words, the low-pass filter property of the membrane determines its quality as a coincidence detector. This makes it possible to deduce the total membrane conductance merely from input and output spike data. Figure 1 illustrates the effect of different total membrane conductances on the superposition of PSPs. The same sequence of spikes - a single spike followed by a quadruple - arrives at a relatively slow (solid line) and at a fast (dashed line) membrane. Due to the resulting different temporal courses of the PSPs, those on the slow membrane add up to a larger effective amplitude compared to those on the fast membrane.

Test Setup: For testing the input driven responsiveness of a membrane, a single neuron with a constant leakage conductance g_l is utilized. In order to vary the externally driven component of the membrane conductance, it receives a set of uncorrelated Poisson spike trains through N_E excitatory and N_I inhibitory synapses. Each spike train has the same firing rate ν_{in}. The decay time constants τ_{syn} and the maxima $g_E^{\max}$ ($g_I^{\max}$) for the excitatory (inhibitory) conductances are kept constant during all experiments. The aim of the test is to find an average synaptic conductance $\overline{g_{\text{syn}}} \equiv \langle g_E(t) + g_I(t) \rangle$ which results in a high-conductance state. With given values for τ_{syn}, $g_E^{\max}$ and $g_I^{\max}$, the temporal integration over N_E excitatory and N_I inhibitory spike trains with firing rate ν_{in} leads to the following average total synaptically induced conductance:

$$\overline{g_{\text{syn}}} = \tau_{\text{syn}}\, \nu_{\text{in}}\, (N_E\, g_E^{\max} + N_I\, g_I^{\max}) \quad . \tag{4}$$

To control $\overline{g_{\text{syn}}}$, the frequency ν_{in} is varied. If all other parameters remained constant, this would result in a corresponding variation of the average membrane potential and, hence, of the output firing rate. An increased output rate deteriorates the responsiveness of the membrane because of the reset mechanism which clamps the membrane potential to the reset potential and makes the neuron insensitive to input for a refractory period of $\tau_{\text{ref}} = 1\,\text{ms}$. This could possibly lead to systematic distortions in the results of the proposed method. In order to circumvent such undesired correlations between the average membrane potential, the output rate and the responsiveness of the membrane, the output rate is kept low (ν_{out} is typically around 4 Hz) by changing the ratio N_E/N_I while keeping the sum $N_E g_E^{\max} + N_I g_I^{\max}$ constant.

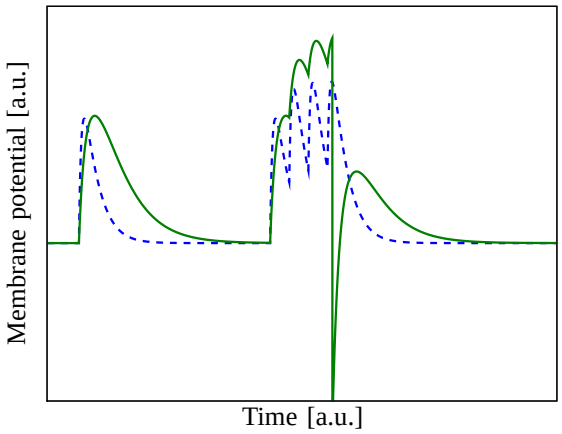

Fig. 1. NEST Simulation: Overlapping PSPs on a membrane with high (dashed line) and low (solid line) total conductance. Membrane potential and time axis in arbitrary units. For this schematical example, the total membrane conductance has been determined by varying g_l. The shown PSPs result from conductance time courses with identical decay times. The conductance amplitudes for both the high and the low conductance membrane have been adjusted such that the amplitudes of the single (leftmost) PSPs become the same in both cases. This results in illustratively different maximum amplitudes of the four overlapping PSPs triggered by identical input spikes. For the fast, i.e. higher conductance membrane, the accumulated potential is not high enough to reach the arbitrarily set spike threshold, while for the slow one it is. The instantaneous membrane depolarization during an action potentials is not modeled in NEST, but the reset mechanism clearly indicates the spike position.

In addition to the Poisson type background, a test stimulus is injected into the neuron via a fixed number of excitatory synapses, which consists of periodic packages of n_{pack} equidistant spikes. The period T_{PP} from package to package is kept constant, while the inter-spike interval T_{ISI} within one package is varied from 0 ms to $T_{\text{ISI}}^{\max} \equiv \frac{T_{\text{PP}}}{n_{\text{pack}}}$. With $T_{\text{ISI}} = T_{\text{ISI}}^{\max}$, one package exactly fills T_{PP}. This approach guarantees that the total spike rate fed into the neuron through the test synapses is independent of T_{ISI}. The test stimulus is weakly connected to the neuron, its contribution to the total synaptic conductance (never more than 5%) is neglected in the following. Its absolute contribution to the output firing rate is of no interest, while the *change* in the output rate resulting from the variation of T_{ISI} is evaluated. Testing the response of the membrane without any Poisson background is not possible in this framework, since

the desired output rate can not be established with the test stimulus only.

Figure 2 exemplarily illustrates the test setup: a neuron receives input from Poisson spike trains of a certain frequency ν_{in} (only a subset is shown) and additionally from a test stimulus consisting of the packages of equidistant spikes. When the periodic spike packages arrive, the output rate temporarily increases, indicated by an output spike histogram.

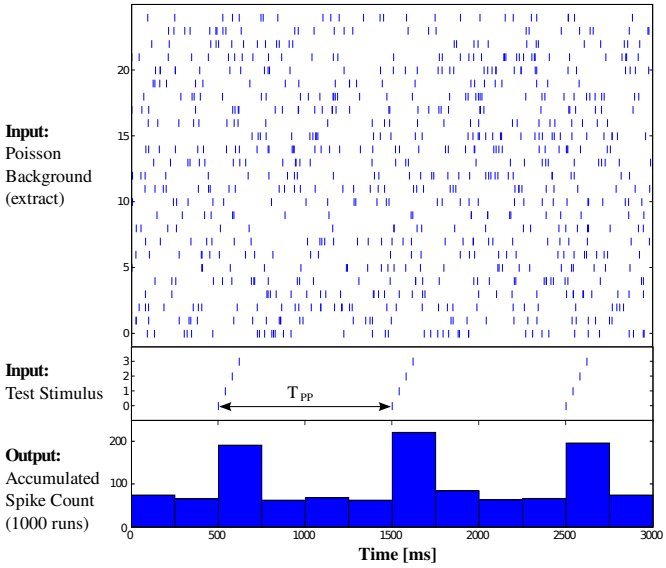

Fig. 2. NEST Simulation: Example of the spike-based method for membrane temporal resolution evaluation. Shown are input and output of a neuron under test. Top: Raster plot of parts of the Poisson background with $\nu_{\text{in}} = 10\,\text{Hz}$. Middle: Test stimulus fed into the neuron. Bottom: Resulting output spike count histogram accumulated over 1000 runs.

The mean output rate over the whole experiment duration is dependent on T_{ISI}, because shorter time intervals lead to stronger accumulation of PSPs on the membrane. But as discussed above, for a constant T_{ISI} the output rate also depends on the total membrane conductance respectively on the width of a PSP. Hence, sweeping T_{ISI} for various values of $\overline{g_{\text{syn}}}$ (regulated via ν_{in}) and measuring the resulting output firing rate will result in different response curves showing the temporal resolution capability of the neuron.

In the following, all output rates indicated with an f actually represent the difference between the output rate acquired with a specific test stimulus configuration minus the output rate with no test stimulus at all, $f(T_{\text{ISI}}) \equiv \nu_{\text{out}}^{\text{stim}}(T_{\text{ISI}}) - \nu_{\text{out}}^{\text{nostim}}$. This is done because only the response to the test stimulus is of interest, while the response to the output rate caused by the Poisson background is not. The background determines the conductance state and thus the responsiveness of the neuron, whereas the test stimulus is needed to get quantitative information about the conductance state of the neuron.

To be able to distinguish the output response curves for different conductance states, a characterizing critical quantity τ_{res} is defined as follows: τ_{res} is the critical time interval $T_{\text{PP}}^{\text{crit}}$ between test spikes at which the output rate falls below a certain threshold frequency

$$f_{\text{crit}} \equiv f_{\text{min}} + \frac{1}{2}\left(f_{\text{max}} - f_{\text{min}}\right) \quad . \tag{5}$$

Here, f_{min} is the minimum output rate, i.e. the saturation rate which is reached for a certain value of T_{ISI} and not under-run if T_{ISI} gets larger. The maximum output firing rate resulting from closely coincident input spikes is f_{max}. See Figure 3 for illustration.

III. Results

If not explicitly stated differently, the basic set of parameters applied for the software runs is the following:

Neuron:

$C_m = 0.2\,\text{nF}$, $g_l = 2\,\text{nS}$, $V_{\text{reset}} = -80.0\,\text{mV}$, $E_I = -75.0\,\text{mV}$, $E_l = -70.0\,\text{mV}$, $V_{\text{thresh}} = -57.0\,\text{mV}$, $E_E = 0.0\,\text{mV}$.

Synapses:

$\tau_{\text{syn}} = 20\,\text{ms}$, $g_E^{\text{max}} = 0.4\,\text{nS}$, $g_I^{\text{max}} = 1.6\,\text{nS}$.

The leakage conductance g_l has been chosen particularly low in order to have a slow membrane for the unstimulated case. If applicable on the hardware system, the remaining parameters were chosen according to [26], aiming at biologically realistic models. However, in a few cases the values were chosen to better fit the hardware system: For instance, the choice of rather large synaptic time constants reflects hardware limitations, because the chosen speedup factor for the hardware system does support only time constants in the range of 20 to $50\,\text{ms}$. Furthermore, in order to provide the necessary amount of total synaptic stimulation, the maximum synaptic conductances are large as well, since the number of synapses to a hardware neuron is limited. It also has to be noted that neither g_l nor C_m are directly measurable for the hardware. Still, the time constant of the hardware membrane under no stimulation, $\tau_{m,\text{rest}} = \frac{C_m}{g_l}$, can be easily measured. By varying a steering current which controls the invisible g_l, $\tau_{m,\text{rest}}$ can be calibrated close to the desired value.

A. Proof of Principle via Software Simulation

Determining a Membrane's Temporal Resolution Capability: In order to avoid that hardware-specific behavior might wrongly confirm the functionality of the proposed method, it is first verified qualitatively utilizing the software simulator NEST. The NEST neuron model and the parameter values are chosen to optimally resemble the hardware. Still, quantitatively equal results from hardware and software are not to be expected, since subtle non-linear parasitic hardware effects are not included in the NEST model. Some of them will be discussed in the hardware result section.

To find the membrane temporal resolution measure τ_{res}, the test stimulus was applied with a package period of $T_{\text{PP}} = 1000\,\text{ms}$. Each package had $n_{\text{pack}} = 4$ spikes, with T_{ISI} being varied from 0 ms to 250 ms. The target output rate was set to $\nu_{\text{target}} = 4\,\text{Hz}$.

Figure 3 shows the result for a background Poisson rate of $\nu_{\text{in}} = 4$ Hz, fed into $N_E = 48$ excitatory and $N_I = 51$ inhibitory synapses. The plot shows the expected decrease in

the output firing rate with growing T_{ISI} due to decreasing overlap of PSPs in the test stimulus. Every data point represents the mean value from 250 runs with 10 seconds simulated time each, the error-bars denote the standard error of means (SEM). Also shown in the plot is $f_{\text{crit}} = f_{\text{min}} + \frac{1}{2}(f_{\text{max}} - f_{\text{min}})$, indicated by the dotted horizontal line. The value of T_{ISI} where the curve crosses f_{crit} defines the temporal resolution capability τ_{res} of the neuron.

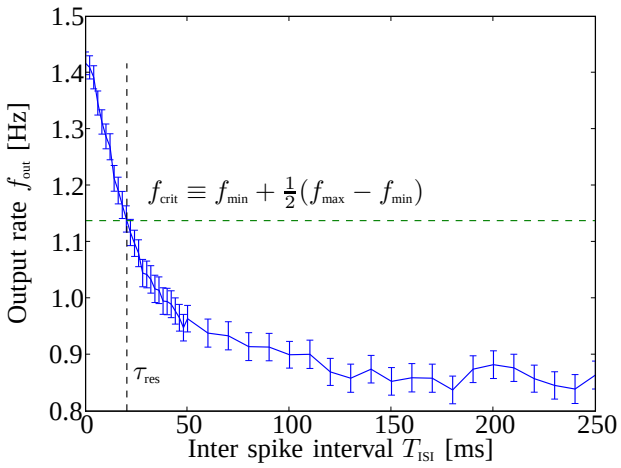

Fig. 3. Neuron output firing rate vs. inter-spike interval of applied test spikes. The horizontal dotted line shows f_{crit}. f_{min} is defined by the mean output rate for T_{ISI} in $[150\,\text{ms}, 250\,\text{ms}]$. The vertical dotted line indicates the temporal resolution τ_{res} defined in the text.

Background Activity Increases Membrane Temporal Resolution: The membrane temporal resolution τ_{res} has been evaluated for various Poisson background rates ν_{in}. Figure 4 shows τ_{res} as a function of ν_{in}. The dependence is obvious: The membrane temporal resolution capability respectively the coincidence detection property improve for higher Poisson background rates. If the synaptic contribution to the total membrane conductance is large enough – in the plot starting at approximately $\nu_{\text{in}}^{\text{sat}} \approx 15\,\text{Hz}$ – the temporal resolution capability saturates, limited by the time constant τ_{syn} of the synaptic conductance decay. In this state, the membrane potential is nearly immediately following the synaptic stimulation. Since the output rate is dynamically adjusted via N_E and N_I, the critical input rate $\nu_{\text{in}}^{\text{sat}}$ that is sufficient for a saturation of τ_{res} corresponds to two critical values N_E^{sat} and N_I^{sat} as well.

Following Equation 4, this results in a quantitative estimation for the necessary amount of synaptically induced conductance for the neuron,

$$\overline{g_{\text{syn}}^{\text{sat}}} = \tau_{\text{syn}}\,\nu_{\text{in}}^{\text{sat}}\,(N_E^{\text{sat}}\,g_E^{\text{max}} + N_I^{\text{sat}}\,g_I^{\text{max}}) \quad . \tag{6}$$

For this example with $N_E^{\text{sat}} = 44$, $N_I^{\text{sat}} = 52$ and $\nu_{\text{in}}^{\text{sat}} = 15\,\text{Hz}$, an average synaptic conductance of $\overline{g_{\text{syn}}^{\text{sat}}} \approx 30\,\text{nS}$ is needed to reach a maximum responsiveness of the membrane. This is a more than ten-fold increase compared to the pure leakage conductance g_l.

In [29], the transition of a membrane into the high-conductance state is defined by a ratio of 5:1 between its total conductance and its pure leakage conductance. The input rate which is necessary to create this amount of total conductance for the described experiment is indicated by a dashed line in Figure 4.

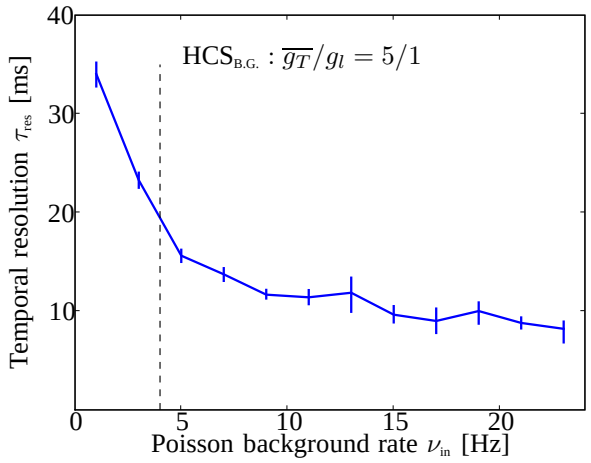

Fig. 4. NEST Simulation: Temporal resolution τ_{res} of a membrane plotted versus the applied background input rate ν_{in}, acquired with the method proposed in Section II-C. Note the saturation for input rates larger than approx. 15 Hz. The vertical dashed line represents the input frequency necessary to generate a high-conductance state according to the definition given in [29].

B. High-Conductance States in Silicon

As indicated above, variations from the pure software results are to be expected, since the hardware is subject to electronic phenomena like noise, crosstalk, parasitic capacitances and leakages. Those introduce distortions in the dynamics which are hard to be mapped to the available standard neuron models in NEST. E.g., the circuits which generate the synaptic conductance courses exhibit weight dependent leakage conductances towards their corresponding reversal potentials. These leakages are activity and temperature dependent plus subject to process variations during the production of the chip, hence they are hard to be quantified. Furthermore, the generated conductance courses are implemented as increasing and decreasing currents, which are routed via wires to sub-circuits where they control physical conductances to the reversal potential. The wires and switches for these currents have capacitances which impose a loss of synaptic efficacy for low input rates and an activity dependent low-pass filtering effect. Compensation methods for the parasitic leakages are under development, but not yet considered for this study. Their effect on the temporal resolution capability of the hardware neuron membrane is difficult to be estimated. Thus, a theoretical prediction for the transition to a high-conductance state as defined in [29] and as indicated in Figure 4 can not be made for this system. Despite these issues, the proposed test method provides the possibility to find high-conductance regimes on the hardware system.

For the hardware model, the neuron parameters are chosen identically to the software simulations (see Section III-A) if possible. As stated above, for a hardware neuron circuit the absolute value of g_l can not be directly accessed, but the membrane time constant in rest can be measured. A hardware control current which determines g_l was set to a minimum value, resulting in a membrane time constant of $\tau_{m,\text{rest}} = (16 \pm 3)\,\text{ms}$.

The hardware synapse parameters were set such that the neuron's output rate could be kept in approximately the same range as in the software simulations throughout the covered range of input rates. The synaptic hardware weights correspond to quantized biological conductance increases of $g_E^{\text{max}} \approx 1.5\,\text{nS}$ and $g_I^{\text{max}} \approx 6\,\text{nS}$, with decay time constants of $\tau_{\text{syn}} = (27 \pm 8)\,\text{ms}$.

Figure 5 shows the result of the proposed high-conductance state test conducted on a hardware neuron with the given parameters. Like in Figure 4, the decrease of τ_{res} as a function of ν_{in} and the saturation from a certain input rate can both be observed.

Analogously to Section III-A, the critical amount of synaptic conductance can be determined for this hardware neuron. In the shown example setup, saturation is reached from $\nu_{\text{in}} \approx 17\,\text{Hz}$, with $N_E^{\text{sat}} = 28$ and $N_I^{\text{sat}} = 27$. Together with the values for g_E^{max}, g_I^{max} and τ_{syn}, the necessary average synaptically induced leakage to put the hardware neuron into a maximally input sensitive regime is $\overline{g_{\text{syn}}^{\text{sat}}} \approx 94\,\text{nS}$. Due to the hardware specific effects mentioned above, this value has to be interpreted with care. The difference compared to the NEST model is assumed to be caused mainly by the capacitance of the wires which route the synaptic conductance courses and which - as mentioned above - distort the synaptic impact on the neuron in efficacy and time, depending on the input rate. This capacitance probably also explains the large values of τ_{res} for small background rates, where the given values for τ_{syn} and $\tau_{m,\text{rest}}$ suggest smaller values - especially since in the NEST reference experiment τ_{res} decreased very fast with growing synaptic stimulation. But as can be seen from the data, it is still possible to find a level of background stimulation which is sufficient to put the neuron into a high-conductance state.

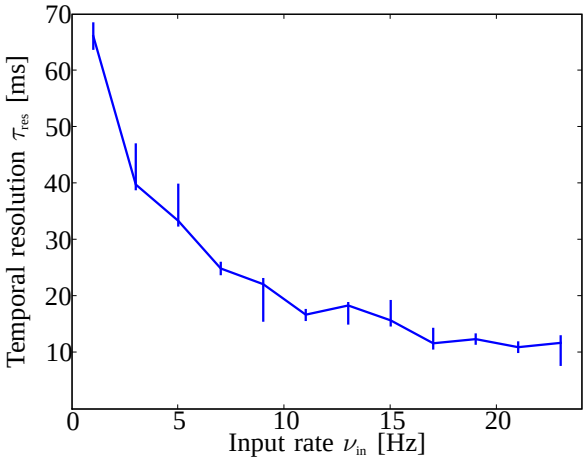

Fig. 5. Hardware: Temporal resolution τ_{res} of a VLSI membrane plotted versus the applied background input rate ν_{in}. Saturation is reached at approximately 17 Hz.

IV. Discussion

For a neuromorphic hardware system, we have presented a spike-based method which allows to find the amount of synaptic stimulation necessary for a neuron to operate in a high-conductance state. In order to avoid possible misleading hardware-specific behavior, we first have tested our approach by pure software simulations. Subsequently, we have applied the method to the hardware system, and the results clearly demonstrate the functionality of the proposed technique. Compared to possible alternatives based on e.g. sub-threshold analyses via oscilloscope, this method is faster and can be robustly automated. Both speed and robustness are particularly important for the hardware system since the presented high-conductance state test has to be applied for several neurons in order to find a reliable setting that is valid for the whole chip. This is necessary because leakage conductances towards the resting potential, parasitic leakages towards reversal potentials and parasitic capacitances affecting post synaptic currents' shapes can differ from circuit to circuit. A comparison between test results acquired from different neurons, which are not shown in this paper, yields qualitatively equal results.

A similar method applied to neuron models in software is described in [19] and is also spike-based, but has a few draw-backs compared to the presented one. This is mainly due to portability issues for the hardware platform, which does not offer the flexibility for artificial setups as software simulators do. First, the method in [19] requires in the order of 30 synaptic inputs which synchronously generate very strong conductance courses. This is hard to be adopted for the presented system, because the hardware platform is limited in terms of both number of synaptic inputs and the available range and reliability of synaptic efficacies. Additionally, sending more than 4 perfectly synchronous spikes into one neuron at a time is not possible on the utilized chip, although the technically necessary and automatically generated fan-out of input spike times in the order of tenths of biological milliseconds is probably negligible. Sweeping arbitrary input firing rates is not possible either, the proposed ranges of up to $150\,\text{Hz}$ (corresponds to $15\,\text{MHz}$ in chip time domain) exceed the hardware bandwidths. Furthermore, the method proposed in [19] brings difficulties for automation due to the fact that it requires the detection of peaks in inter-spike interval histograms which often are ambiguous. An algorithm needs to find the height of a peak that is not necessarily the global, but just a local maximum within the histogram, and can be determined only by its expected location. Finally, the fact that the measure τ_{res} suggested in this paper is given in millisecond dimension represents an intuitive quantity for a neuron's temporal resolution capability.

One drawback of the presented approach is that changing

the ratio of excitatory to inhibitory stimuli in order to keep the output rate in a low range makes it difficult to apply the proposed method to many neurons at the same time - which would have made the presented test faster. Furthermore, the functionality of the method is dependent on the output firing rate: If the output rate without test stimulus $\nu_{\text{out}}^{\text{nostim}}$ is chosen too large, the firing rate with applied test stimulus and hence the difference rate $f(T_{\text{ISI}}) = \nu_{\text{out}}^{\text{stim}}(T_{\text{ISI}}) - \nu_{\text{out}}^{\text{nostim}}$ would not decrease monotonously - as seen in Figure 3 - and thus finding the critical quantity τ_{res} would not be possible. We interpret this as a too high firing sensitivity which leads to a high probability that the first test spike within a package already triggers an output spike and pulls the membrane to the reset potential. This effectively reduces the impact of the following spikes due to the reset mechanism and has to be avoided. Thus, for the proposed method the quality of the important signal $f(T_{\text{ISI}})$ strongly depends on the output rate. In order to benefit from the scalability advantages of neuromorphic systems also for this high-conductance state test, neuron-specific output rate calibration mechanisms are needed. These calibration mechanisms could be based on modifications of individual weights taking into account that the total input conductance stays constant during the adjustment of weights and is determined by the input rate. A neuron-specific firing threshold calibration could also be used to adjust the output rate, a feature which will be implemented in successor systems.

Nevertheless, the spike-based high-conductance state test provides an automatable tool for tuning neuromorphic systems towards an input-sensitive regime even if direct measurement of conductances is impossible. The principle might help to avoid extra wiring and analog-to-digital converters in future neuromorphic designs since the indirect conductance access method during a system's specification phase can be sufficient. Thus, prototypes could exploit more of the available chip area. More spike-based methods, e.g. for the calibration of leakage conductances and for the specification of analog noise, are currently under development.

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